REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY Thomas M. Hess	DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444
STANDARDIZED MILITARY DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Thomas M. Hess APPROVED BY Monica L. Poelking DRAWING APPROVAL DATE 93-05-07 REVISION LEVEL	MICROCIRCUIT, DIGITAL, CMOS, VMEbus ADDRESS CONTROLLER, MONOLITHIC SILICON SIZE A | CAGE CODE 67268 | 5962-92009 SHEET 1 OF 33

DESC FORM 193
JUL 91

5962-E236-93

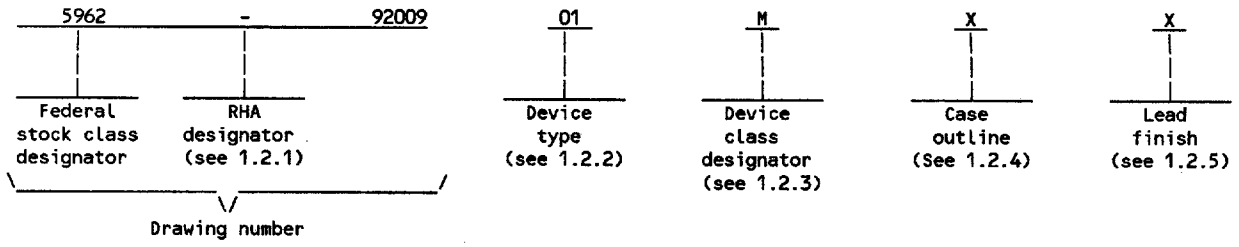
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

9004708 0004565 731

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	VAC068A	VMEbus address controller

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA7-P145	145	Pin grid array
Y	See figure 1	160	Flat pack

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Storage temperature range	-65°C to +150°C
Voltage on any pin with respect to ground	-0.5 V dc to +7.0 V dc
Power dissipation (P_D)	1.5 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (Θ_{JC})	
Case outline X	See MIL-STD-1835
Case outline Y	10 °C/W
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Case operating temperature range (T_C)	-55°C to +125°C
Supply voltage (V_{CC})	5.0 V dc ±10%

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) . . . . . XX percent 2/

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Values will be added when they become available.

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 105 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified 1/	Group A subgroups	Device type	Limit		Unit
					Min	Max	
Input low voltage	V_{IL}		1,2,3	All		0.8	V
Input high voltage	V_{IH}				2.0		
Output low voltage	V_{OL}	V_{CC} = MIN, I_{OL} = 8 mA 2/				0.6	
		V_{CC} = MIN, I_{OL} = 48 mA 3/					
Output high voltage	V_{OH}	V_{CC} = MIN, I_{OH} = -3 mA 3/			2.4		
		V_{CC} = MIN, I_{OH} = -8 mA 2/					
Input leakage current	I_{IL}	V_{CC} = MAX $0.0\ V \le V_{IN} \le V_{CC}$ V			-10	+10	µA
Output leakage current	I_{OL}	VCC = MAX $0.0\ V \le V_{OUT} \le V_{CC}$ V 4/			-10	+10	
		VCC = MAX $0.6\ V \le V_{OUT} \le 2.4$ V 5/					
Input clamp voltage	V_{IK}	V_{CC} = MIN, I_{IN} = -18 mA				-1.2	V
		I_{IN} = 18 mA			V_{CC} + 1.2		
Power supply current	I_{CC}	V_{CC} = 5.5 V, V_{IN} = 0.0 V, 5.5 V				150	mA
Input capacitance	C_{IN}	V_{CC} = 5.0 V, T = 25°C, f = 1 MHz, (see 4.4.1c)	4			10	pF
Output capacitance	C_{OUT}	V_{CC} = 5.0 V, T = 25°C, f = 1 MHz (see 4.4.1c)	4			15	
Functional testing		See4.4.1b	7,8				

See footnotes at end of table

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified 1/	Group A subgroups	Device type	Limit		Unit
					Min	Max	
RESET[O] to WORD[L] 6/	t_{A1}	Global Reset See figure 3	9,10,11	ALL	5T		ns
WORD[O] to RESET high, WORD[H] 6/	t_{A2}				10T		
LA[31:8],FCi, R/W valid to PAS[L] 6/	t_{B1}	Register Write See figure 3			10		
LD[31:16] valid to DSACKi[L] 6/	t_{B2}				5		
PAS[O] to DSACKi[L] 15/	t_{B3}				5+T	40+2T	
PAS[1] to DSACKi[H] 15/	t_{B4}				4	33	
PAS[1] to LA[31:8], FCi, R/W(Hold Time) 6/	t_{B5}				5		
LA[31:8], FCi, R/W Valid to PAS[O](Set-Up Time) 6/	t_{C1}	Register Read See figure 3			10		
PAS[O] to DSACKi[L] 15/	t_{C2}				5	40+T	
PAS[O] to LD[31:16] Valid 15/	t_{C3}				7	58	
PAS[1] to DSACKi[H] 15/	t_{C4}				5	18	
PAS[1] to LA[31:8], FCi, R/W(Hold Time) 6/	t_{C5}				5		
PAS[O] to LD[31:16] Invalid 14/ 15/	t_{C6}				5+3T	45+ 3.5T	

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified 1/	Group A subgroups	Device type	Limit		Unit
					Min	Max	
LA[31:8], FCi, R/W to PAS[O] (Set-Up Time) 6/	t_{D1}	Local Access Via Local Bus See figure 3	9,10,11	ALL	10		ns
PAS[O] to ASIZ1/O, WORD Valid 15/	t_{D2}				6	37	
PAS[O] to Chip Select[L] 15/7/8/	t_{D3}				5	38	
PAS[O] tO DSACKi[L] 15/9/	t_{D4}				PI1+5	PI1+28 +T	
PAS[O] to IORD/IOWR[L] 15/10/	t_{D5}				PI3+5	PI3+53 +T	
PAS[1] to LA[31:8], FCi, R/W(Hold Time) 6/	t_{D6}				5		
PAS[1] to ASIZ1/O WORD Invalid 15/	t_{D7}				6	42	
PAS[1] to Chip Select[H] 15/7/	t_{D8}				3	39	
PAS[1] to DSACKi[H] 15/	t_{D9}				4	18	
PAS[1] to IORD[H]/IOWR[H] 15/10/	t_{D10}				PI3+3	PI3+25 +T	
PAS[O] to ASIZ1/O, WORD Valid 15/	t_{E1}	Local Access Via VMEbus See figure 3			6	37	
PAS[O] to Chip Select[L] 15/11/	t_{E2}				5	38	
PAS[O] to DSACKi[L] 15/12/	t_{E3}				P12+5	P12+33 +T	

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified 1/	Group A subgroups	Device type	Limit		Unit
					Min	Max	
PAS[0] to IORD[L], IOWR[L] 10/15/	t_{E4}	Local Access Via VMEbus See figure 3	9,10,11	ALL	P13+5	P13+53 +T	ns
PAS[1] to ASIZ1/0, WORD Invalid 15/	t_{E5}				6	42	
PAS[1] to Chip Select[H] 10/15/	t_{E6}				3	39	
PAS[1] to DSACKi[H] 13/15/	t_{E7}				4	18	
PAS[1] to IORD[H], IOWR[H] 10/15/	t_{E8}				P13+3	P13+25 +T	
VAS[0] to SLSELi[L] or ICFSEL[L] 15/	t_{F1}	VMEbus Slave/Slave Block Access See figure 3			2	27	
LAEN[1] to LA[31:8] Valid 15/	t_{F2}				3	27	
VAS[1] to SLSELi[H] or ICFSEL[L] 15/	t_{F3}				5	23	
LAEN[0] to LA[31:0] Valid 15/	t_{F4}				10	33	
LA[31:8], FCi, R/W to PAS[0] (Set-Up Time) 6/	t_{G1}	VMEbus Master Access See figure 3			10		
PAS[0] to ASIZ1/0, WORD Valid 15/	t_{G2}				6	37	
PAS[0] to MWB[L] 15/	t_{G3}				10	35	
ABEN[0] to A[31:8] Valid 15/	t_{G4}				2	20	

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified 1/	Group A subgroups	Device type	Limit		Unit
					Min	Max	
PAS[1] to LA[31:8], FCi, R/W (Hold Time) 6/	t_{G5}	VMEbus Master Access See figure 3	9,10,11	ALL	5		ns
PAS[1] to ASIZ1/0, WORD Invalid 15/	t_{G6}				6	42	
PAS[1] to MWB[H] 15/	t_{G7}				2	36	
ABEN[1] to A[31:8] Invalid 15/	t_{G8}				1	11	
LA[31:8], FCi, R/W Valid to PAS[0] (Set-Up Time) 6/	t_{H1}	Master Block Transfer Initiation Cycle See figure 3			10		
PAS[0] to ASIZ1/0, WORD Valid 15/	t_{H2}				6	37	
PAS[0] to DSACKi[L] 15/	t_{H3}				5+T	40+2T	
PAS[0] to MWB[L] 15/	t_{H4}				10	35	
PAS[1] to ASIZ1/0, WORD (Hold Time) 15/	t_{H5}				6	42	
PAS[1] to DSACKi[H] 15/	t_{H6}				4	18	
PAS[1] to MWB[H] 15/	t_{H7}				2	36	
ABEN[0] to A[31:8] Valid 15/	t_{H8}				2	20	
LAEN[1], FCi Valid to LA[31:8] Valid 15/	t_{H9}				3	27	
PAS[L], FCi Valid to LDMACK[L] 15/	t_{H10}				1	31	

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

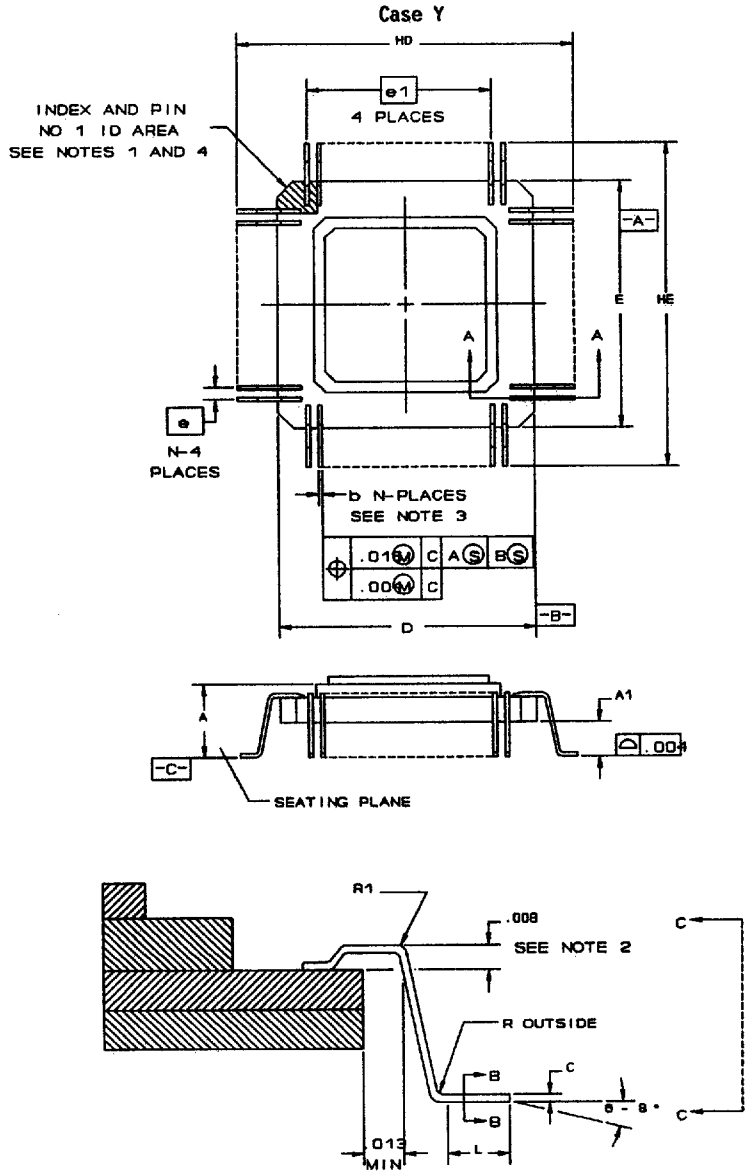
Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified 1/	Group A subgroups	Device type	Limit		Unit
					Min	Max	
BLT[1] to LA[31:8] Incremented 15/	t_{I1}	Boundary Crossing See figure 3	9,10,11	ALL	1	33	ns
LADO[0] to A[31:8] Incremented 15/	t_{I2}				4	33	
LA[31:8], FCi, R/W Valid to PAS[0] (Set-Up Time) 6/	t_{J1}	PIO Output See figure 3			10		
LD[31:16] to PAS[0] (Set-Up Time) 6/	t_{J2}				5		
PAS[0] to DSACKi[L] 15/	t_{J3}				T+5	40	
PAS[0] to PIO[13:0] Valid 15/	t_{J4}				3	63+2T	
PAS[1] to DSACKi[H] 15/	t_{J5}				4	18	
PAS[1] to LA[31:8], FCi, R/W (Hold Time) 6/	t_{J6}				5		
PAS[1] to LD[31:16] Invalid 15/	t_{J7}				5	45	
LA[31:8], FCi, R/W Valid to PAS[0] (Set-Up Time) 6/	t_{K1}	PIO Input See figure 3			10		
PIO[13:0] to PAS[0] (Set-Up Time) 6/	t_{K2}				5		
PAS[0] to DSACKi[L] 15/	t_{K3}				5	T+40	
PAS[0] toLD[31:16] Valid 15/	t_{K4}				7	58+T	

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified 1/	Group A subgroups	Device type	Limit		Unit
					Min	Max	
PAS[1] to DSACKi[H] 15/	t_{K5}	PIO Input See figure 3	9,10,11	ALL	4	18	ns
PAS[1] to LA[31:8], FCi, R/W (Hold Time) 6/	t_{K6}				5		
PAS[1] to LD[31:16] Invalid 15/	t_{K7}				5	45	
Frequency of Operation 6/		Clock Inputs See figure 3			1	40	
Cycle time 6/	1				25	1000	
Clock Pulse Width (measured from 1.5V to 1.5V) 6/	2,3				11.25		
Rise and Fall time 6/	4,5					5	

1/ All testing to be performed using worst-case test conditions. The following pins are active low: RESET, WORD, R/W, PAS, DSACKi, R/W, ASIZ, ASIZO, ASIZ1, IORD, IOWR, SLSELO, SLSEL1, IOSEL3, IOSEL4, IOSEL5, ICFSEL, MWB, ABEN, LDMACK, BLT, FCIACK, MWB, FPUCS, DRAMCS, CACHIN, IOSELO, IOSEL1, SHRCS, VICSEL, DDIR, VSBSEL, VICLBR, REFGT. The asterisk (*) is used to indicate active low signals.
2/ VMEbus signals (Low Drive, all VMEbus Daisy Chain Signals) and all non-VMEbus signals.
3/ VMEbus signals (AS*, DS1*, DS0*, BCLR*, SYSCLK*) and VMEbus signals (Meduim Drive, All non-High, non-Low Drive Signals).
4/ VMEbus pins. All outputs disabled.
5/ Non-VMEbus pins, all outputs disabled.
6/ Tested initially and at process and design changes. Thereafter guaranteed, if not tested, to the limits specified in table I.
7/ Chip select can be any of DRAMCS*, EPROMCS*, SHRCS*, VSBSEL*, FPUCS*, CS*, or IOSELi*.
8/ The Decode Control register provides facilities to conditon DRAMCS* or boundary decodes with the assertion of PAS*.
9/ PI1 is the programmable interval for EPROMCS*, SHRCS*, and IOSELi* in the DSACKi* Control register.
10/ PI3 is the programmable interval for IORD and IOWR in the Decode Control register.
11/ Chip select can be any of DRAMCS*, EPROMCS*, SHRCS*, or VSBEL*.
12/ PI2 is the programmable interval for EPROMCS*, SHRCS*, DRAMCS*, or VSBSEL* in the Decode Control register.
13/ SLSELi* redirection is enabled in the Decode Control register.
14/ The maximum time LD[31:16] invalid is PAS[0] +3.5T or PAS[1] whichever occurs first.
15/ Minimum limits for subgroups 9,10,11 are guaranteed but, not tested.



SECTION A-A

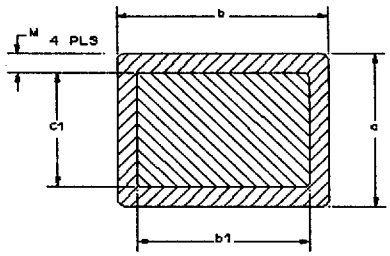
FIGURE 1. Case outline.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-92009
		REVISION LEVEL	SHEET 12

DESC FORM 193A
JUL 91

9004708 0004576 517

Case Y



Symbol	Variation							
	Inches				Millimeters			
	Min	Nom	Max	Note	Min	Nom	Max	Note
A	.080		.110		2.04		2.80	
A1	0.22	0.30	0.38		0.56	0.76	0.98	
b	.006		.015	3	0.15		0.33	3
b1	.006		.013	3	0.15		0.38	3
c	.002		.008	3	0.05		0.20	3
c1	.004		.008	3	0.10		0.20	3
D/E	1.098	1.102	1.106		27.94	28.05	28.15	
e	.025 BSC				0.64 BSC			
e1	.800 BSC				20.36 BSC			
HD/HE	1.218	1.228	1.238		31.00	31.26	31.51	
L	.012	.020	.028		0.31	0.51	0.71	
M			.0015				0.038	
N	160			4	160			4
ND/NE	40			5	40			5
R	.011		.025		0.28		0.64	
R1	.010				2.55			
Notes	6				6			

Notes:
1. A terminal 1 identification mark shall be located at the index corner in the shaded area shown. Terminal 1 is located immediately adjacent to and counterclockwise from the index corner. Terminal numbers increase in a counterclockwise direction when viewed as shown.
2. Generic lead attach dogleg depiction. May be flat configuration.
3. Dimensions b and c include lead finish; dimensions b1 and c1 apply to base metal only. Dimension M applies to plating thickness.
4. Dimension N: number of terminals
5. Dimension ND/NE: Number of terminals per package edge.
6. The leads of this package style shall be protected from mechanical distortion and damage such that dimensions pertaining to relative lead/body "true position" and lead "coplanarity" are always maintained until the next higher level package attachment process is complete. Package lead protection mechanisms (tie bars, carriers, etc) are not shown on the drawing, however when microcircuit devices contained in this package style are shipped for use in government equipment, or shipped directly to the Government as spare parts or mechanical qualification samples, lead 'true position' and "coplanarity" protection shall be in place.

FIGURE 1. Case outline. - Continued

Case Outline X

Terminal No.	Symbol	Terminal No.	Symbol	Terminal No.	Symbol
A1	A_{23}	D13	PIO8/IOSEL4	M14	LA14
A2	A_{20}	D14	VICSEL	M15	LA18
A3	A_{17}	D15	PIO12/SHRCS	N1	ID14
A4	A_{16}	E1	LADI	N2	FCIACK*
A5	A_{14}	E2	ABEN	N3	CPUCLK
A6	A_{12}	E3	LDMACK	N4	FC2
A7	A_{10}	E13	V_{SS}	N5	V_{CC}
A8	A_{08}	E14	LA31	N6	V_{SS}
A9	A_{25}	E15	LA28	N7	LD23
A10	A_{27}	F1	BLT	N8	LD24
A11	A_{29}	F2	PIO4/IORD	N9	V_{SS}
A12	A_{31}	F3	V_{SS}	N10	V_{CC}
A13	A_{30}	F13	LA29	N11	DRAMCS*
A14	PIO2/TXDB	F14	LA26	N12	V_{SS}
A15	V_{CC}	F15	LA27	N13	LA11
B1	PIO13/IOSEL2	G1	REFGT	N14	LA12
B2	A_{22}	G2	VSBSEL	N15	LA16
B3	A_{19}	G3	VICLBR	P1	ASIZ0*
B4	A_{18}	G13	V_{SS}	P2	FC0
B5	A_{15}	G14	LA24	P3	LAEN
B6	A_{13}	G15	LA25	P4	R/W*
B7	A_{11}	H1	ICFSEL	P5	DSACK0*
B8	A_{09}	H2	SLSEL0	P6	LD16
B9	A_{24}	H3	V_{CC}	P7	LD18
B10	A_{26}	H13	V_{CC}	P8	LD22
B11	A_{28}	H14	LA22	P9	LD27
B12	PIO1/RXDA	H15	LA23	P10	LD29
B13	PIO3/RXDB	J1	SLSEL1	P11	LD31
B14	PIO6/IOSEL3	J2	IDIO	P12	EPROMCS*
B15	PIO9/IOSEL5	J3	V_{SS}	P13	CACHINH*
C1	DDIR	J13	V_{CC}	P14	LA8
C2	SWDEN	J14	IOSEL1	P15	LA10
C3	A_{21}	J15	LA21	R1	FC1
C4	V_{SS}	K1	ID8	R2	PAS*
C5	V_{CC}	K2	ID9	R3	DSACK1*
C6	V_{SS}	K3	V_{SS}	R4	LD19
C7	V_{CC}	K13	V_{SS}	R5	LD21
C8	V_{SS}	K14	LA17	R6	LD17
C9	V_{CC}	K15	LA19	R7	LD20
C10	V_{SS}	L1	ID11	R8	LD25
C11	PIO0/TXDA	L2	ID12	R9	LD26
C12	PIO5/IOWR	L3	ID15	R10	LD28
C13	PIO7	L13	LA13	R11	LD30
C14	PIO10	L14	LA15	R12	MWB*
C15	LA30	L15	LA20	R13	FPUCS*
D1	PIO11	M1	ID13	R14	RESET*
D2	VAS	M2	WORD	R15	IOSEL0*
D3	LADO	M3	ASIZ1		
D4	LOCATOR PIN	M13	LA9		

FIGURE 2. Terminal connections.

Case Outline Y

Terminal No.	Symbol	Terminal No.	Symbol	Terminal No.	Symbol
1	V_{SS}	55	LA9	109	V_{CC}
2	SLSEL1	56	LA12	110	A10
3	ID8	57	LA10	111	A12
4	ID10	58	LA14	112	A11
5	ID9	59	LA13	113	A13
6	V_{SS}	60	LA16	114	V_{SS}
7	ID11	61	LA15	115	A14
8	ID12	62	LA18	116	A15
9	ID13	63	V_{SS}	117	A16
10	ID14	64	LA17	118	A17
11	WORD	65	LA20	119	A18
12	ID15	66	IOSEL1	120	V_{CC}
13	FCIACK	67	V_{CC}	121	A19
14	ASIZ0	68	LA19	122	A20
15	ASIZ1	69	LA21	123	V_{SS}
16	CPUCLK	70	LA22	124	V21
17	FC0	71	LA23	125	A22
18	FC1	72	V_{CC}	126	A23
19	FCZ	73	V_{SS}	127	LADO
20	LAEN	74	LA25	128	SWDEN
21	PAS	75	LA27	129	PIO13-IOSEL2
22	R/W	76	LA24	130	VAS
23	V_{CC}	77	LA26	131	LDMACK
24	DSACK1	78	LA29	132	DDIR
25	DSACK0	79	LA28	133	ABEN
26	LD19	80	LA31	134	PIO11
27	V_{SS}	81	PIO12-SHRCS	135	V_{SS}
28	LD16	82	LA30	136	PIO4-IORD
29	LD21	83	VICSEL	137	LADI
30	LD18	84	V_{SS}	138	VSBSEL
31	LD23	85	PIO10	139	VICLBR
32	LD17	86	PIO9-IOSEL5	140	BLT
33	LD20	87	PIO8-IOSEL4	141	REFGT
34	LD22	88	PIO7	142	SLSELO
35	LS25	89	PIO6-IOSEL3	143	ICFSEL
36	LD24	90	V_{CC}	144	V_{CC}
37	V_{SS}	91	PIO5-IOWR		
38	LD26	92	PIO3-RXDB		
39	LD28	93	PIO2-TXDB		
40	LD27	94	PIO1-RXDA		
41	LD29	95	PIO0-TXDA		
42	V_{CC}	96	A30		
43	LD30	97	A28		
44	LD31	98	A31		
45	MWB	99	V_{SS}		
46	FPUCS	100	A26		
47	EPROMCS	101	A29		
48	DRAMCS	102	A24		
48	CACHIN	103	V_{CC}		
50	RESET	104	A27		
51	V_{SS}	105	A25		
52	LA11	106	A9		
53	LA8	107	A8		
54	IOSELO	108	VSS		

Figure 2. Terminal connections. - Continued

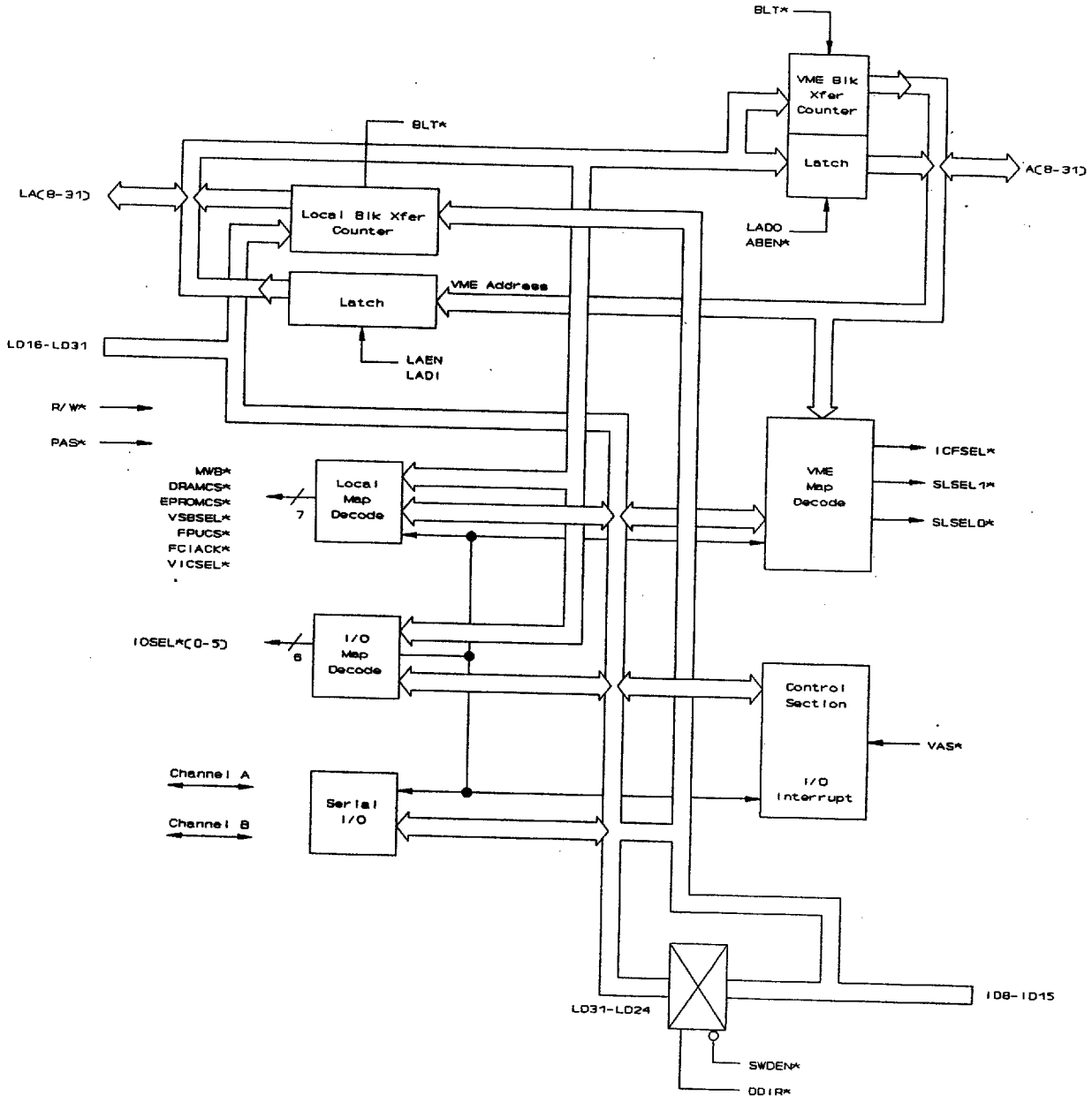
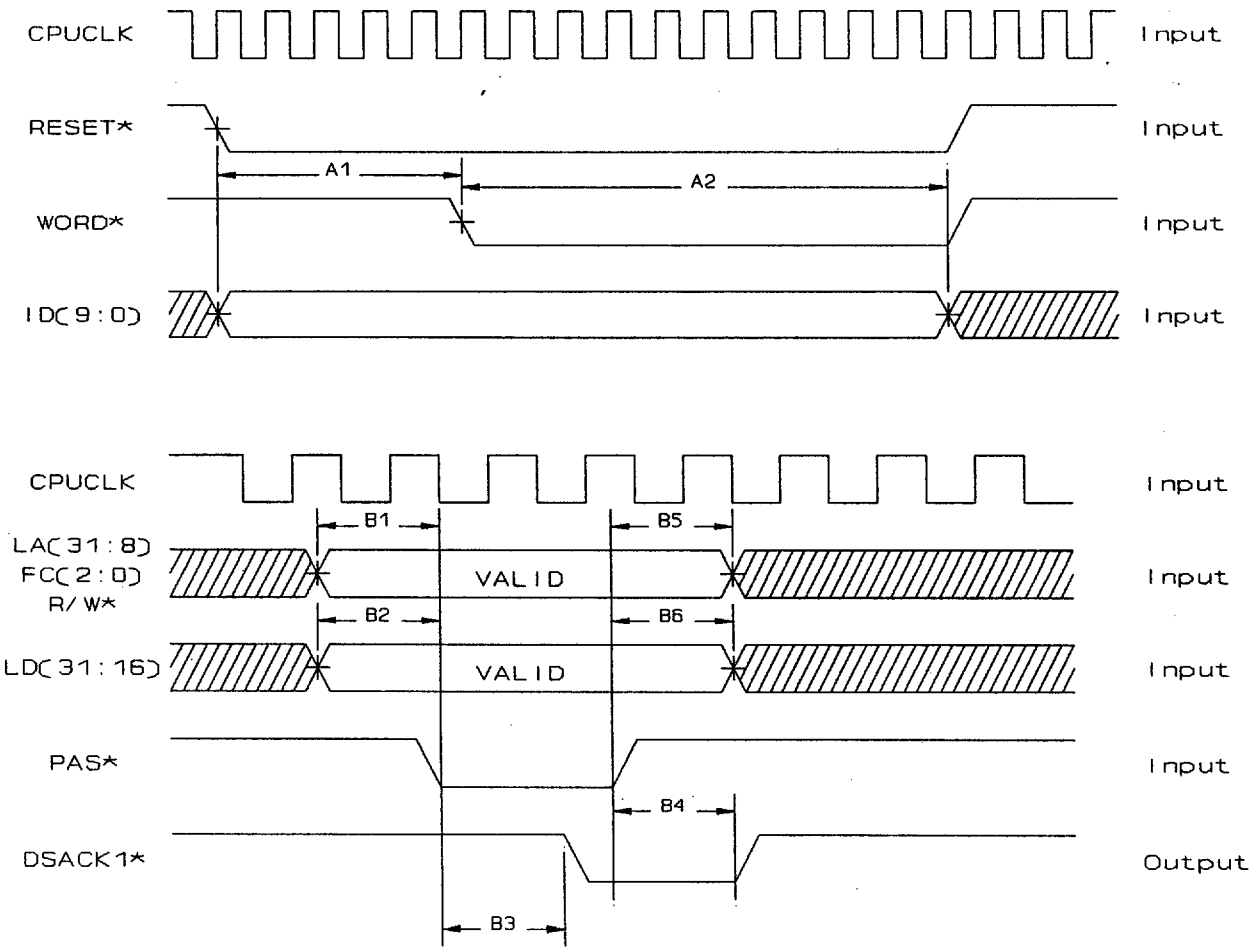


FIGURE 3. Block diagram.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-92009
		REVISION LEVEL	SHEET 16

DESC FORM 193A
JUL 91

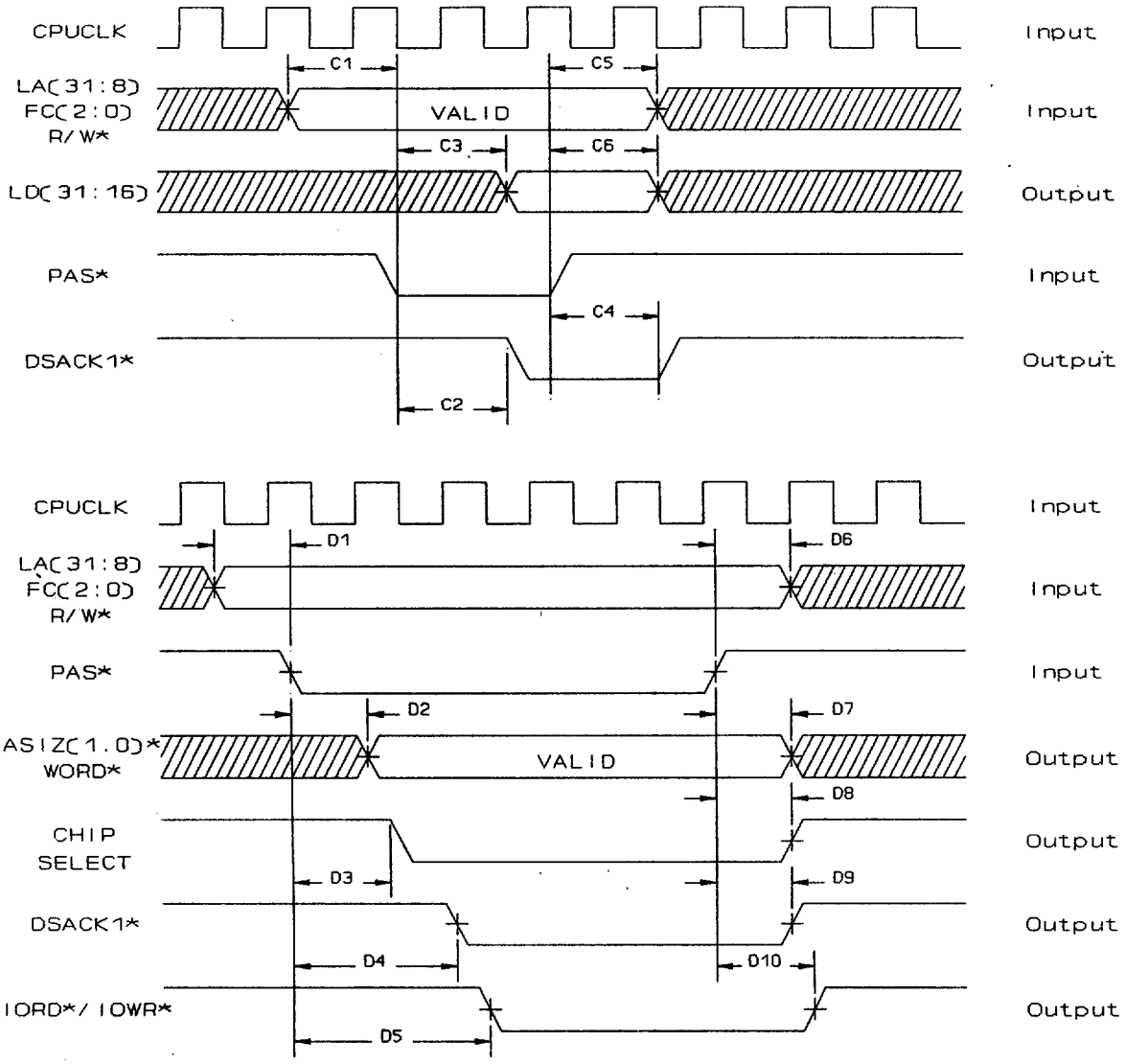
9004708 0004580 T48



* - Indicates an active low signal

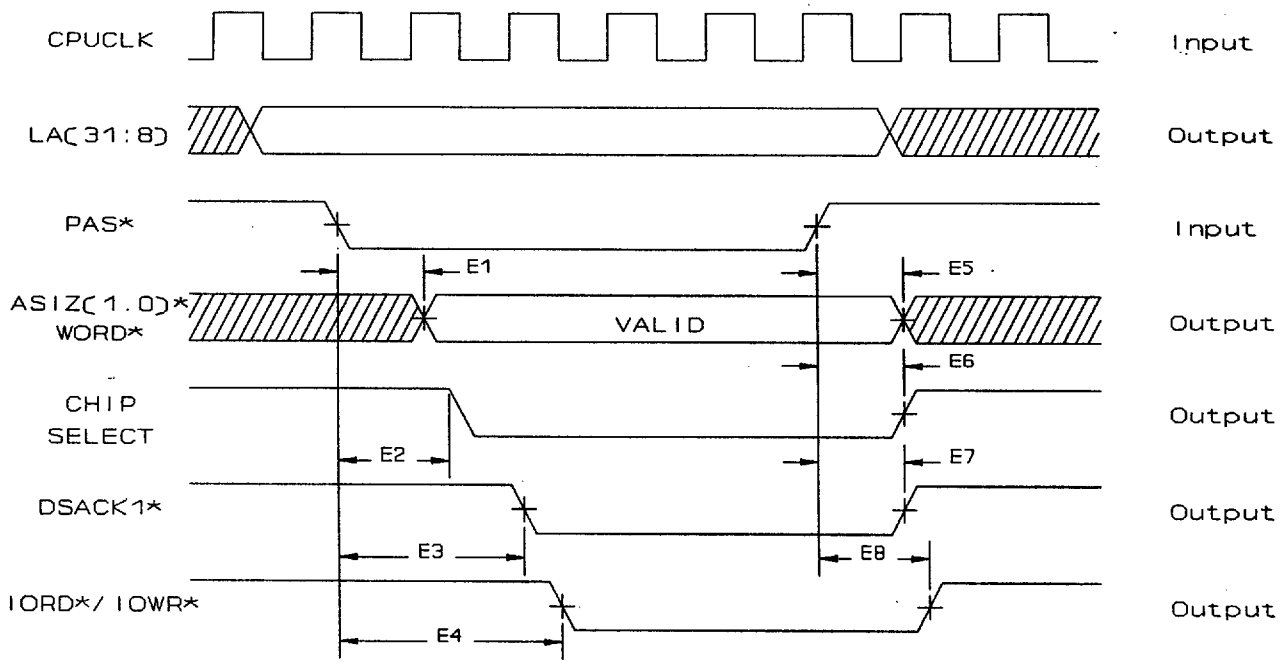
FIGURE 4. Timing waveforms.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-92009
		REVISION LEVEL	SHEET 17



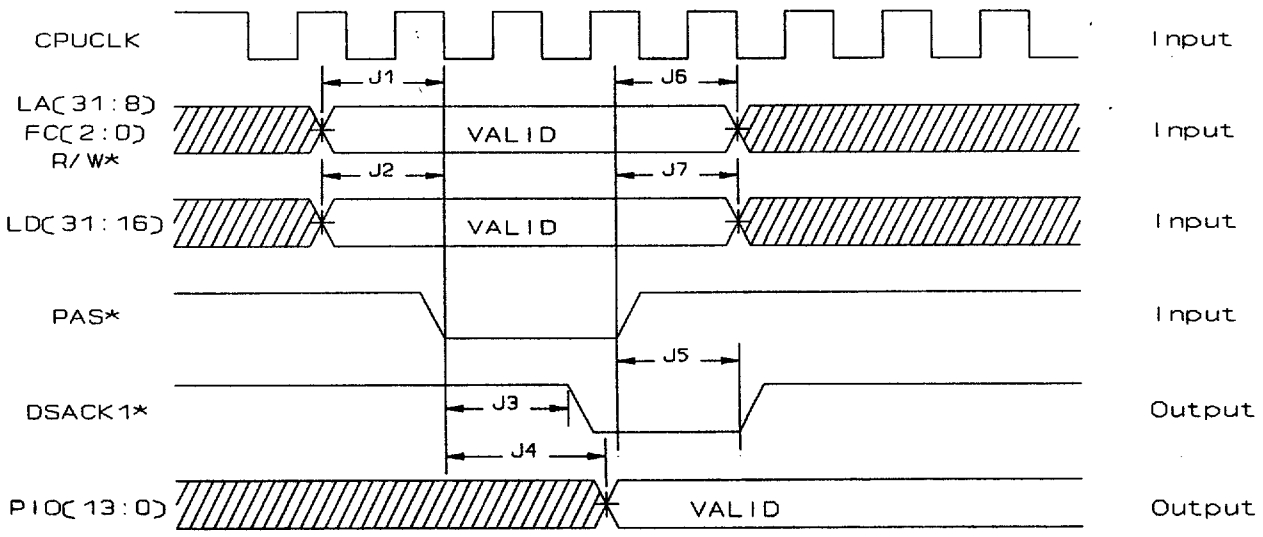
* - Indicates an active low signal

FIGURE 4. Timing waveforms. - Continued



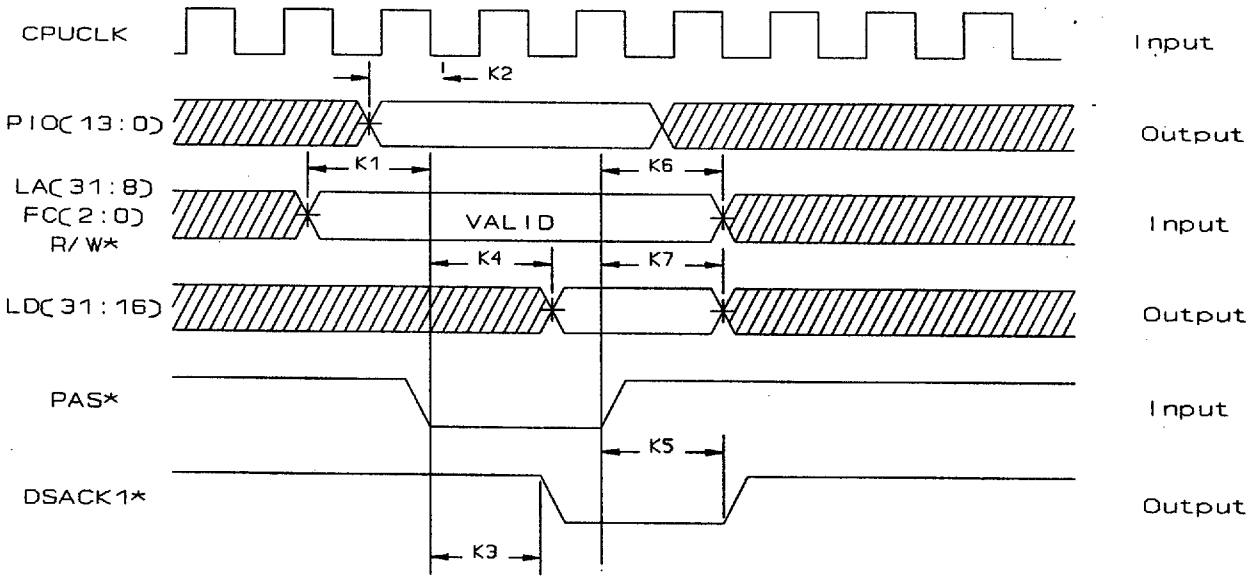
* - Indicates an active low signal

FIGURE 4. Timing waveforms. - Continued



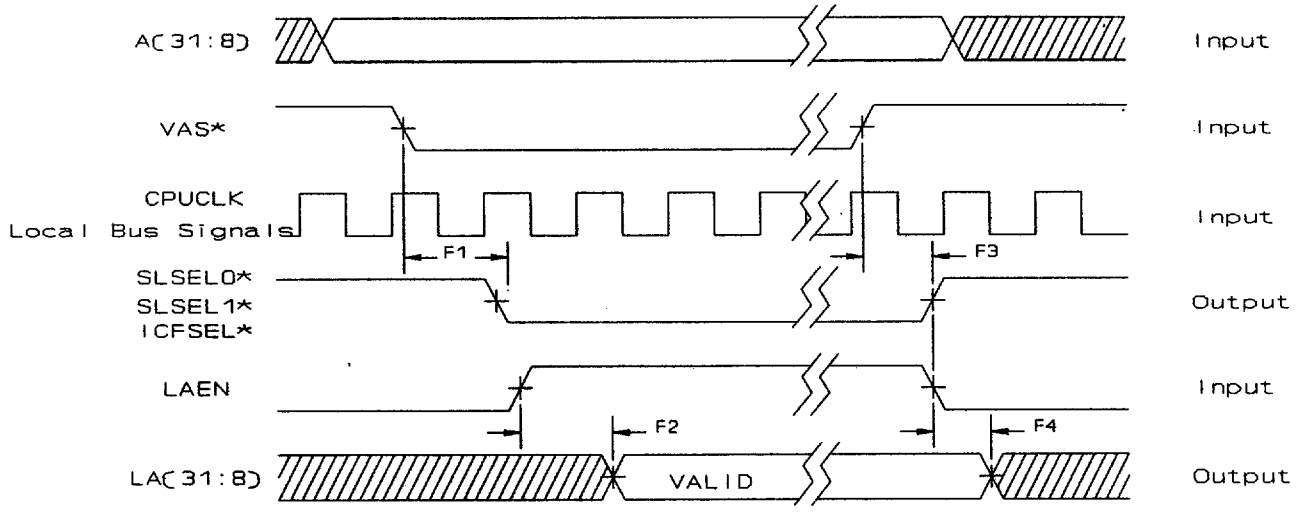
* - Indicates an active low signal

FIGURE 4. Timing waveforms. - Continued



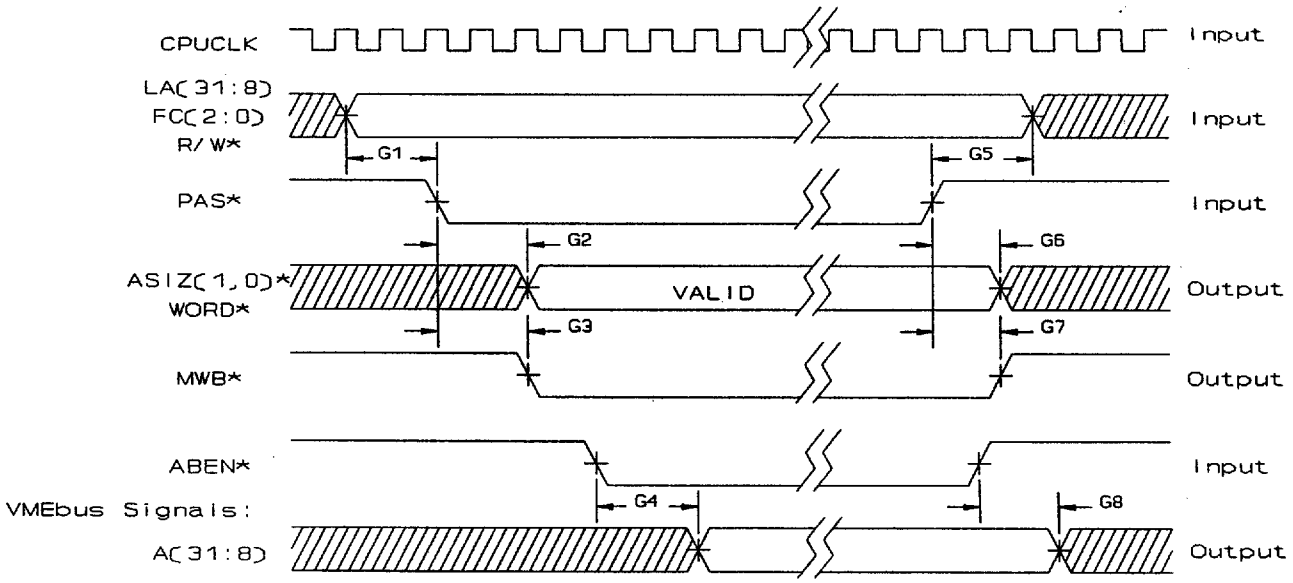
* - Indicates an active low signal

FIGURE 4. Timing waveforms. - Continued



* - Indicates an active low signal

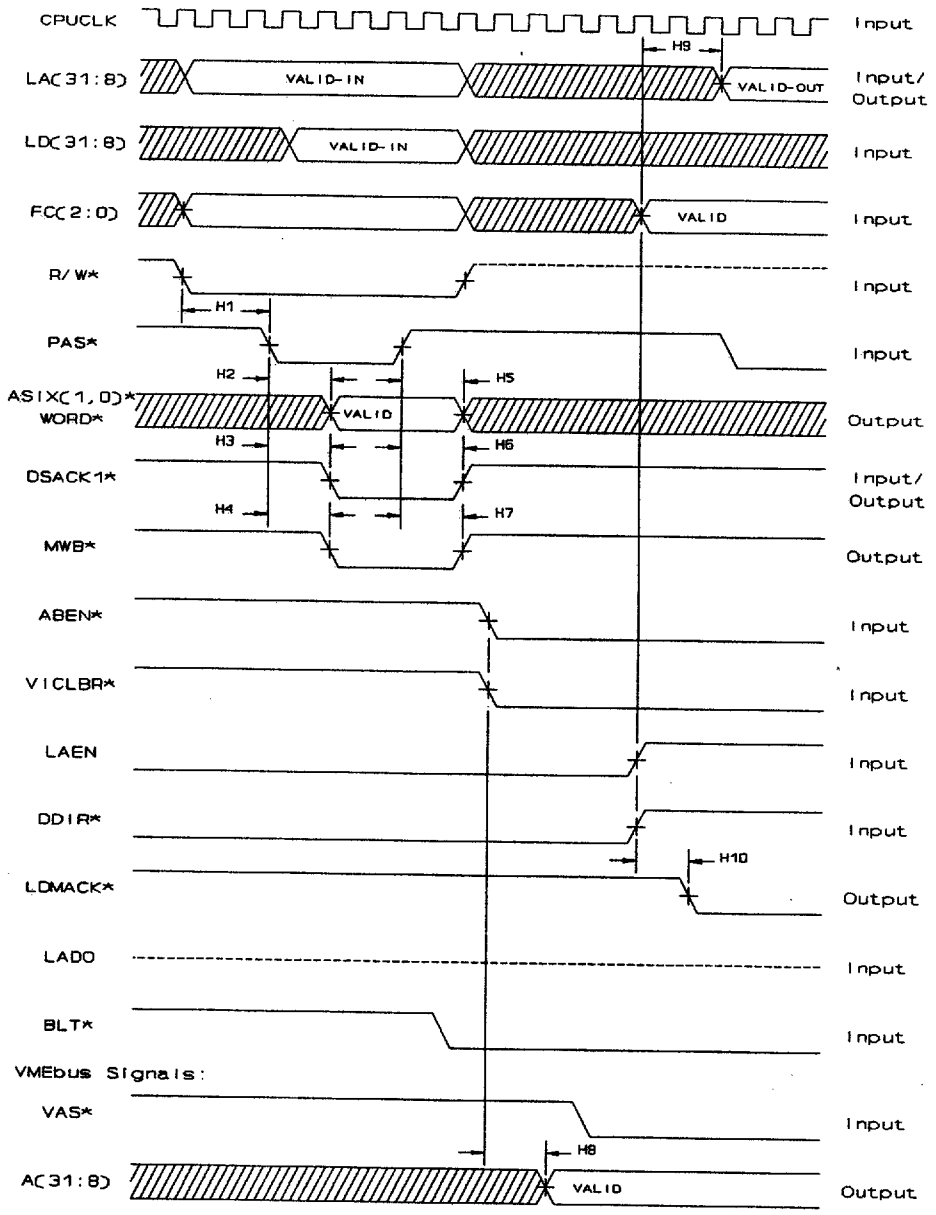
FIGURE 4. Timing waveforms. - Continued



* - Indicates an active low signal

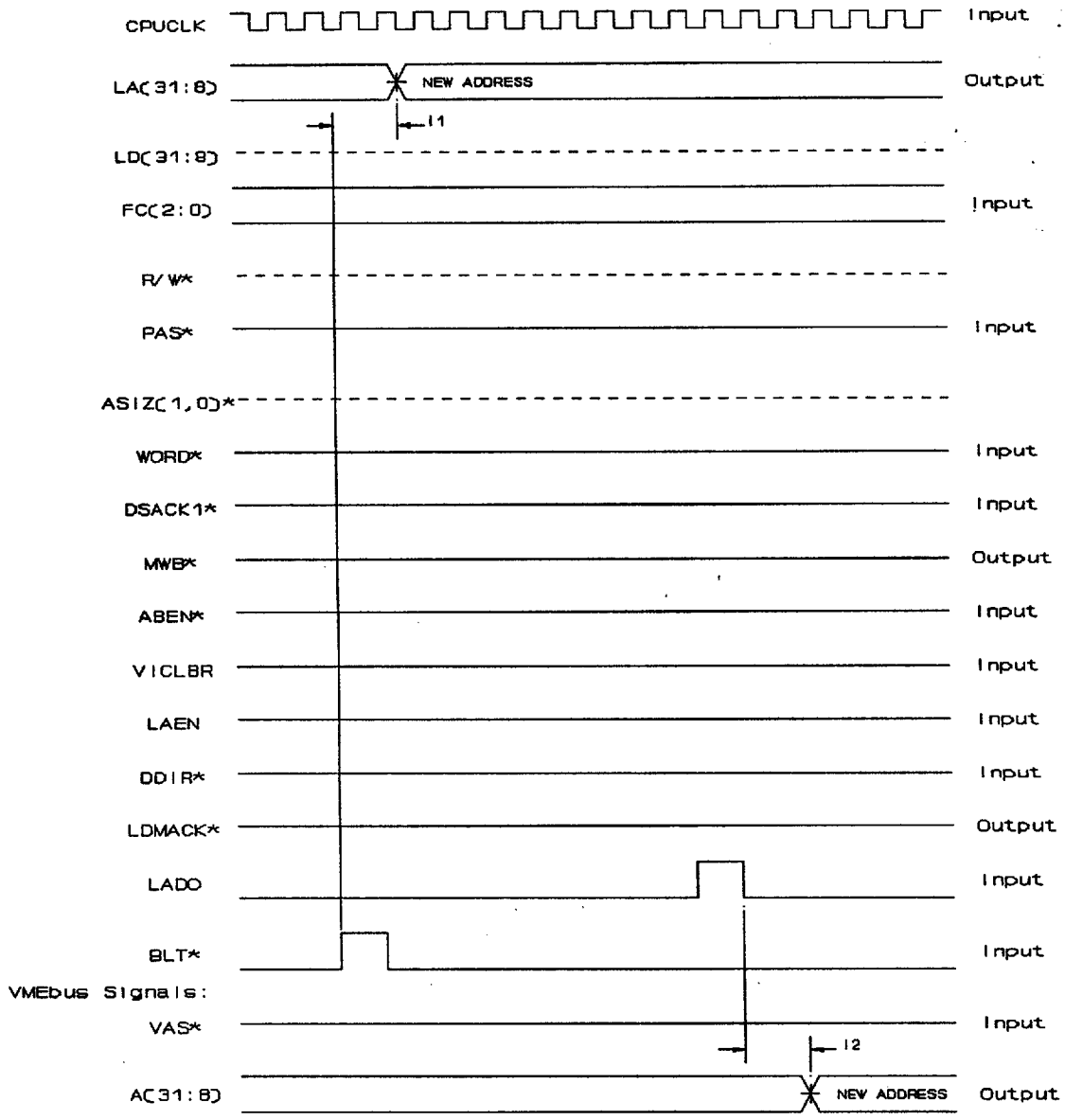
FIGURE 4. Timing waveforms. - Continued

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-92009
		REVISION LEVEL	SHEET 23



* - Indicates an active low signal

FIGURE 4. Timing waveforms. - Continued



* - Indicates an active low signal

FIGURE 4. Timing waveforms. - Continued

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as *modified herein*. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device classes B and S, the test circuit shall be submitted to the qualifying activity. For device classes M, B, and S, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes B and S, subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4(C_{IN} and C_{OUT}) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)			Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)			1, 7		1, 7
Final electrical parameters (see 4.2)	1/ 1,2,3,7 8,9,10,11	1/ 1,2,3,7 8,9,10,11	2/ 1,2,3,7 8,9,10,11	1/ 1,2,3,7 8,9,10,11	2/ 1,2,3,7 8,9,10,11
Group A test requirements (see 4.4)	1,2,3,4, 7,8,9,10 11	1,2,3,4, 7,8,9,10 11	1,2,3,4, 7,8,9,10 11	1,2,3,4, 7,8,9,10 11	1,2,3,4, 7,8,9,10 11
Group B end-point electrical parameters (see 4.4)			2,8a,10		
Group C end-point electrical parameters (see 4.4)	2,8a,10	2,8a,10		2,8a,10	2,8a,10
Group D end-point electrical parameters (see 4.4)	2,8a,10	2,8a,10	2,8a,10	2,8a,10	2,8a,10
Group E end-point electrical parameters (see 4.4)	2,8a,10	2,8a,10	2,8a,10	2,8a,10	2,8a,10

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table II herein. For device class S steady-state life tests, the test circuit shall be submitted to the qualifying activity.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.3.1 Additional criteria for device classes M and B. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition C or D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class B, the test circuit shall be submitted to the qualifying activity. For device classes M and B, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331 and Table III.

Table III. Pin descriptions.

Symbol	Name and function
A[31:8]	The VMEbus address signals are three-state input/outputs.
AS	The VMEbus address strobe signal is an input signal that responds to both 5962-92010 and VMEbus generated address strobes.
ID[15:8]	The VMEbus isolated data bus signals are three-state input/outputs used to interface local data [15:8] to the VMEbus D [15:8] in conjunction with transparent latching bidirectional I/O buffers. They also are used to interface with local 8-bit I/O peripherals via the Device Location and DSACKi Control registers.
LD[31:16]	The local data bus signals are three-state input/outputs used to write or read the local data bus and for writing and reading the on-chip control registers. Note: The IDbus connects to LD[15:8] and 5962-92010 connects to LD[7:0].
LA[31:8]	The local address bus signals are three-state input/outputs used as inputs during a VMEbus master cycle and to access on-chip control registers. They are used for output during local or slave accesses.
PAS	The local-processor address strobe is an input that indicates to the the device that a valid address is present on the address bus. This signal is typically driven by either 5962-92010 or the local processor.
R/W	The local read/write signal is an input. When high, the signal indicates that the current cycle is a read. When low, the current cycle is a write. This signal is typically driven by either the 5962-92010 or the local processor.
RESET	Reset is an input signal for the 5962-92010 . It is used alone or in conjunction with WORD to reset the the device internal registers. There are two reset types that may be implemented, and both of them are discussed in the reset section.
WORD	This signal is both and input and three-state input/output and is active under programmable control from the appropriate region attribute register and controls the length of the data field. When it is asserted, the data path is 16 bits wide. When deasserted, a 32-bit data path is set. It is also used as an input in conjunction with RESET to set the device registers. It is typically connected to the 5962-92010 as an output.
ASIZ1, ASIZ0	These are the address size signals and are three-state input/outputs. They are used to specify the address size of an access. They are active under programmable control from the appropriate region attribute register. These signals are typically driven to the 5962-92010 along with WORD to determine address and data path size. ASIZ0 / ASIZ1 / Addressing Mode 0 / 0 / User-defined 0 / 1 / A32 1 / 0 / A16 1 / 1 / A24
DSACK1/0	These are the data sizing acknowledge signals and are rescinding three-state input/outputs. They are generated for any of the device select outputs except CS and VSBSEL accesses. DSACK0 or DSACK1 can be selectively disabled or enabled in the DSACK1 Control register.

Table III. Pin descriptions. - Continued

Symbol	Name and function
FC2/0	These are the function code input signals. They are used by the device to determine the local access type and are typically driven by the local processor or the 5962-92010 as shown in the following tables: FC2 FC1 FC0 Cycle 0 0 1 User data space 0 1 0 Supervisor data space 1 1 0 Supervisor program space 1 1 1 CPU space FC2 FC1 Cycle 0 0 Slave block transfer 0 1 Local DMA 1 0 Slave Access 1 1 DRAM refresh
MWB	This is the module-wants-bus output signal. It is asserted under programmable control of the appropriate region attribute register and indicates that a VMEbus assess is occurring. This signal is typically connected to the 5962-92010.
FCIACK	This is the local interrupt output signal. It indicates that the current cycle is an interrupt acknowledge cycle. This signal is typically connected to the 5962-92010. It is asserted during local the device interrupt cycles, or when HIACKEN is enabled in the PIO Direction register or when IOSEL5 address space is accessed when enabled in the PIO Function register.
DRAMCS	This is the DRAM chip select output signal. It is asserted when the local address maps into region 0 as defined by the DRAM Upper Limit Address register. It is also asserted when redirection is enabled in the device Decode Control register.
EPROMCS	This is the EPROM chip select output signal. It is asserted after a global reset, during a local access to EPROM address space, and during redirection of SLSEL1 on the local bus via the device Decode register.
FPUCS	This is the floating-point-unit chip select output signal. It is asserted when a floating-point coprocessor access is occurring. This is decoded from the processor function codes or under programmable control i the PIO Function register to be asserted in the IOSEL4 address range.
VSBSEL	This is the VSB (VME Subsystem Bus) select output signal. It is used to identify accesses to a daughterboard of VSB. It is asserted when enabled from the appropriate region attribute register.
REFGT	This is the refresh grant output signal. It is asserted during a DRAM refresh cycle and is typically decoded from the 5962-92010 function codes (FC1 and FC2).
LBR	This is the 5962-92010 local bus request input signal. It is used to signal the device when the 5962-92010 requests the local bus. It is typically connected to the 5962-92010 LBR signal.
CS	This is the 5962-92010 chip select input signal. It is asserted when the fixed address of the 5962-92010 is present on the local address bus. This signal is typically connected to the 5962-92010 chip select signal (CS).
BLT	This is the block transfer input signal. It is used to determine when a block transfer is in progress and to increment internal address counters during a boundary crossing. This signal is typically connected to the 5962-92010.

Table III. Pin descriptions. - Continued

Symbol	Name and function
CACHINH	This is the cache inhibit signal and is an open collector output. It is asserted when enabled in either the Region Attribute registers or in the A24 Space Base Address register. It is also asserted on access to the DRAM Mailbox and VMEbus A16 address space (Region 6). It may be connected to the CDIS signal on 680X0-type processors.
LDMACK	This is the local DMA activity output signal. It is asserted when there is DMA activity mapped into a particular region. It is typically decoded from the 5962-92010 function codes (FC1 and FC2).
CPUCLK	This is the CPU clock input signal. It is typically connected to the system CPU clock. Maximum frequency is 50 MHz.
SLSEL0	This is the slave select 0 output signal. It is asserted when enabled by a comparison of its base address register and the address on the VMEbus. It indicates to the 5962-92010 that a slave operation is pending.
SLSEL1	This is the slave select 1 output signal. It is asserted when enabled by a comparison of its base address register and the address on the VMEbus. It indicates to the 5962-92010 that a slave operation is pending.
ICFSEL	This is the interprocessor communications output signal. It is asserted under programmable control of a comparison of its base address register and the address on the VMEbus. it indicates a 5962-92010 interprocessor communication access.
IOSEL1/0	These are 2 of the 6 I/O select output signals. They are asserted when the local bus address matches their fixed memory location. They are also used in conjunction with the IDbus when programmed in the PIO Function register.
PIO0-TXDA	The PIO0-TXDA signal is programmed to serve either as general-purpose I/O pin bit 0, or as an output for the UART channel-A transmit signal.
PIO1-RXDA	The PIO1-RXDA signal is programmed to serve as either general-purpose I/O pin bit 1, or as an input for the UART channel-A receiver signal.
PIO2-TXDB	The PIO2-TXDB signal is programmed to serve as either general-purpose I/O pin bit 2, or as an output for the UART channel-B transmit signal.
PIO3-RXDB	The PIO3-RXDB signal is programmed to serve as either general-purpose I/O pin bit 3, or as an input for the UART channel-B receiver signal.
PIO4-IORD	The PIO4-IORD signal is programmed to serve as either general-purpose I/O pin bit 4, or as an output for the read enable signal (local I/O accesses).
PIO5-IOWR	The PIO5-IOWR signal is programmed to serve as either general-purpose I/O pin bit 5, or as an output for the write enable signal (local I/O accesses).
PIO6-IOSEL3	The PIO6-IOSEL3 signal is programmed to serve as either general-purpose I/O pin bit 6, or as an output for the IOSEL3 enable signal (local fixed-map I/O select).
PIO7-Interrupt Request	The PIO7-Interrupt Request signal is used as either general-purpose I/O pin bit 7, or as an output for interrupt requests on one of PIO 7, 10, or 11 (programmed in the Interrupt Control register).
PIO8-IOSEL4	The PIO8-IOSEL4 signal is programmed to serve as either general-purpose I/O pin bit 8, or as an output for the IOSEL4 enable signal (local fixed-map I/O select). IOSEL4 accesses also assert FPUCS when so programed in the PIO Function register.
PIO9-IOSEL5	The PIO9-IOSEL5 signal is programmed to serve as either general-purpose I/O pin bit 9, or as an output for the IOSEL5 enable signal (local fixed-map I/O select). IOSEL5 accesses also assert FCIACK when so programmed in the PIO Function register.

Table III. Pin descriptions. - Continued

Symbol	Name and function
PIO10-INTERRUPT REQUEST	The PIO10-Interrupt Request signal is used as either general-purpose I/O pin bit 10, or as a programmed interrupt request as programmed Interrupt Control register.
PIO11-INTERRUPT REQUEST	The PIO11-Interrupt Request signal is used as either general-purpose I/O pin bit 11, or as an output for interrupt requests as programmed in the Interrupt Control register.
PIO12-SHRCS	The PIO12-SHRCS signal is programmed to serve as either general-purpose I/O pin bit 12, or as an output for shared resource chip select.
PIO13-IOSEL2	The PIO13-IOSEL2 signal is programmed to serve as either general-purpose I/O pin bit 13, or as an output for the IOSEL2 enable signal (local fixed-map I/O select).
SWDEN	The swap data enable signal is an input used in conjunction with DDIR to swap data to or from the Isolated Data bus signals ID[15:8] to the Local Data LD[15:8] bus. This signal is typically connected to the 5962-92010.
DDIR	The data direction signal is an input typically connected to the 5962-92010.
LADO	The latch address out signal is an input used to latch the local address out to the VMEbus. It is typically connected to the 5962-92010. LADO is also used to increment internal address counters during a VMEbus boundary crossing.
LADI	The latch address in signal is an input used to latch the local address from the VMEbus.
LAEN	The local address bus enable signal is an input used by the device to indicate that the 5962-92010 has bus mastership of the local bus.
ABEN	The VMEbus address enable signal is an input used to indicate that the 5962-92010 is driving the VMEbus address bus.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.