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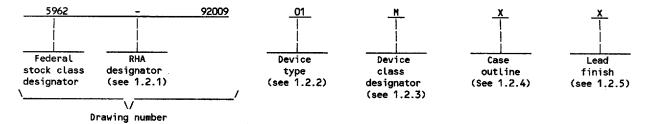
<u>DISTRIBUTION STATEMENT A.</u> Approved for public release; distribution is unlimited.

5962-**E236-93**

9004708 0004565 731 **=**

1. SCOPE

- 1.1 <u>Scope</u>. This drawing forms a part of a one part one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.
 - 1.2 PIN. The PIN shall be as shown in the following example:



- 1.2.1 RHA designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.
 - 1.2.2 <u>Device type(s)</u>. The device type(s) shall identify the circuit function as follows:

Device type	Generic number	<u>Circuit function</u>
01	VACO68A	VMEbus address controller

1.2.3 <u>Device class designator</u>. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class

Device requirements documentation

M

Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883

B or S

Certification and qualification to MIL-M-38510

Q or V

Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
. X	CMGA7-P145	145	Pin grid array
Y	See figure 1	160	Flat pack

1.2.5 <u>Lead finish</u>. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes Λ, B, and C are considered acceptable and interchangeable without preference.

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1.3 Absolute maximum ratings. 1/ Storage temperature range - - - - - - - - - - - - - - - - - --65°C to +150°C Voltage on any pin with respect to ground - - - - - --0.5 V dc to +7.0 V dc Power dissipation (P_D) - - - - - - - - - - - Lead temperature (soldering, 10 seconds) - - - - - -1.5 W +260°C Thermal resistance, junction-to-case (Θ_{JC}) Case outline X -----See MIL-STD-1835 Case outline Y ----- 10 °C/W Junction temperature (T_J) - - - - - - - - - - - - -+175°C 1.4 <u>Recommended operating conditions</u>. -55°C to +125°C 1.5 <u>Digital logic testing for device classes Q and V.</u> Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) XX percent 2/ 2. APPLICABLE DOCUMENTS 2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein. **SPECIFICATIONS** MILITARY - Microcircuits, General Specification for. MIL-M-38510 MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for. **STANDARDS** MILITARY MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers. MIL-STD-883 - Test Methods and Procedures for Microelectronics. MIL-STD-1835 - Microcircuit Case Outlines. BULLETIN **MILITARY** MIL-BUL-103 - List of Standardized Military Drawings (SMD's). HANDBOOK MILITARY MIL-HDBK-780 - Standardized Military Drawings. (Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.) 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. 2/ Values will be added when they become available. STANDARDIZED SIZE 5962-92009 MILITARY DRAWING A DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444 REVISION LEVEL SHEET 3

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2.2 <u>Order of precedence</u>. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

- 3.1 <u>Item requirements</u>. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.
- 3.2 <u>Design, construction, and physical dimensions</u>. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.
 - 3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.
 - 3.2.2 <u>Terminal connections</u>. The terminal connections shall be as specified on figure 2.
 - 3.2.3 Block diagram. The block diagram shall be as specified on figure 3.
 - 3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be specified when available.
- 3.3 <u>Electrical performance characteristics and postirradiation parameter limits</u>. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.
- 3.4 <u>Electrical test requirements</u>. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.
- 3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.
- 3.5.1 <u>Certification/compliance mark</u>. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.
- 3.6 <u>Certificate of compliance</u>. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a GML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.
- 3.7 <u>Certificate of conformance</u>. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.
- 3.8 <u>Notification of change for device class M</u>. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.
- 3.9 <u>Verification and review for device class M</u>. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.
- 3.10 <u>Microcircuit group assignment for device classes M, B, and S</u>. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 105 (see MIL-M-38510, appendix E).
- 3.11 <u>Serialization for device class S</u>. All device class S devices shall be serialized in accordance with MIL-M-38510.

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TABLE I. <u>Electrical performance characteristics</u>.

	Test	Symbol 1	Conditio -55°C ≤ T _C : 4.5 V ≤ V _{CC} unless oth	ons ≤ +125°C ≤ 5.5 V	Group A subgroups	Device type	 		Unit	
			unless other specified	erwise d <u>1</u> /			Min	Max		
	Input low voltage	۸ ^{IF}			1,2,3	All		0.8	٧	
	Input high voltage	v _{IH}					2.0			
	Output low voltage	V _{OL}	V _{CC} - MIN, I _{OL}	= 8 mA ² /				0.6		
			V _{CC} - MIN, I _{OL}	- 48 mA					1	
	Output high voltage	V _{OH}	V _{CC} - MIN, I _{OH}	= -3 mA	<u> </u>		2.4			
			V _{CC} - MIN. I _{OH}	= -8 mA						
	Input leakage current	IIL	VCG = MAX 0.8 V \(\leq\)VIN \(\leq\)				-10	+10	μA	
	Output leakage current	I _{OL}	VCC = MAX 0.0 V ≤ V _{OUT} ≤	v _{cc} v <u>4</u> /			-10	+10		
			VCC - MAX 0.6 V \leq VOUT \leq	: 2.4 V <u>5</u> /						
	Input clamp voltage	v _{IK}	V _{CC} = MIN III	N = -18 mA				-1.2	V	
			I _I	N = 18 mA			Vcc +			
	Power supply current	^I cc	V _{CC} = 5.5 V, V _{IN} = 0.0 V, 5	5.5 V				150	mA	·
	Input capacitance	CIN	V _{CC} = 5.0 V, T = 25°C, f = (see 4.4.1c)	1 MHz,	4			10	pF	
;	Output capacitance	Сопт	V _{CC} = 5.0 V, T = 25°C, f = (see 4.4.1c)	1 MHz	4			15		
	Functional testing		See4.4.1b		7,8	1] .
iee 1	footnotes at end of table	<u>.L</u>	1-		1	<u>.l</u>	<u> </u>	<u> </u>	<u></u>	J
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Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C	Group A	Device	L	imit	Un
		-55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified <u>1</u> /	subgroups	type	Min	Max	
RESET[0] to WORD[L] 6/	t _{A1}	Global Reset See figure 3	9,10,11	ALL	5Т		n
WORD[0] to RESET high, WORD[H] 6/	t _{A2}				10т		
LA[31:8],FCi, R/W valid to PAS[L] 6/	^t B1	Register Write See figure 3			10		
LD[31:16] valid to DSACKI[L] <u>6</u> /	t _{B2}	·			5		
PASEO3 to DSACKIEL3 15/	t _{B3}				5+T	40+2T	
PAS[1] to DSACK[[H]	^t B4				4	33	
PASE1] to LAE31:8], FCi, R/W(Hold Time) 6/	t _{B5}				5		
LA[31:8], FCi, R/W Valid to PAS[0](Set-Up Time) 6/	^t c1	Register Read See figure 3			10		
PAS[0] to DSACKi[L]	t _{C2}				5	40+T	
PASEO] to LDE31:16] Valid 15/	t _{c3}				7	58	
PAS[1] to DSACKi[H] 15/	t _{C4}				5	18	
PASE13 to LAE31:83, FCi, R/W(Hold Time)	t _{C5}				5		,
PASEO3 to LDE31:163 Invalid	t _{C6}				5+3T	45+ 3.5T	

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Test	Symbol	Conditions $-55^{\circ}C \leq T_{C} \leq +125^{\circ}C$	Group A	Device	Li	mit	Uni
		-55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified <u>1</u> /	subgroups	type	Min	Max	
LA[31:8], FCi, R/W to PAS[O] (Set-Up Time)	^t D1	Local Access Via Local Bus See figure 3	9,10,11	ALL	10		ns
PAS[O] to ASIZ1/O, WORD Valid 15/	t _{D2}				6	37	
15/7/8/ PAS[0] to Chip Select[L]	t _{D3}				5	38	
PAS[0] to DSACKi[L]	t _{D4}				PI1+5	PI1+28 +T	
PASEO] to IORD/IOWREL]	t _{D5}				P13+5	P13+53 +T	
PASE11 to LAE31:83, FCi, R/W(Hold Time)	t _{D6}				5		
PASE1] to ASIZ1/O WORD Invalid 15/	t _{D7}				6	42	
15/7/ PAS[1] to Chip Select[H]	t _{D8}				3	39	
PAS[1] to DSACK1[H] 15/	t _{D9}				4	18	
PASE1] to IORDEH]/IOWREH]	t _{D10}				P13+3	PI3+25 +T	
PASEO] to ASIZ1/O, WORD Valid <u>15</u> /	t _{E1}	Local Access Via VMEbus See figure 3			6	37	
PAS[0] to Chip Select[L]	t _{E2}				5	38	
PASEO3 to DSACKIEL3	t _{E3}				P12+5	P12+33 +T	

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- .	1	Conditions				_	
Test	Symbol	-55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified <u>1</u> /	Group A subgroups	Device type	Lir Min	Max	Unit
10/15/ PASEOJ to IORDELJ, IOWRELJ	t _{E4}	Local Access Via VMEbus See figure 3	9,10,11	ALL	P13+5	P13+53 +T	ns
PAS[1] to ASIZ1/O, WORD Invalid <u>15</u> /	t _{E5}				6	42	
<u>10/15</u> / PAS[1] to Chip Select[H]	t _{E6}				3	39	
1 <u>3/15</u> / PAS[1] to DSACK1[H]	t _{E7}				4	18	
10/15/ PASE1] to IORD[H], IOWR[H]	t _{E8}				P13+3	P13+25 +T	
VAS[0] to SLSELi[L] or ICFSEL[L]	^t F1	VMEbus Slave/Slave Block Access See figure 3			2	27	
LAEN[1] to LA[31:8] Valid 15/	t _{F2}				3	27	
VAS[1] to SLSELi[H] or ICFSEL[L] <u>15</u> /	t _{F3}				5	23	
LAEN[0] to LA[31:0] Valid 15/	t _{F4}				10	33	
LA[31:8], FCi, R/W to PAS[O] (Set-Up Time) <u>6</u> /	^t G1	VMEbus Master Access See figure 3			10		
PASEOD to ASIZ1/O, WORD Valid 1 <u>5</u> /	t _{G2}				6	37	
PASEO] to MWB[L] 15/	t _{G3}				10	35	
ABEN[0] to A[31:8] Valid 15/	t _{G4}				2 ·	20	

See footnotes at end of table.

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Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C	Group A	Device		_imit	Unit
		-55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified <u>1</u> /	subgroups		Min	Max	
PAS[1] to LA[31:8], FCi, R/W (Hold Time) <u>6</u> /	t _{G5}	VMEbus Master Access See figure 3	9,10,11	ALL	5		ns
PAS[1] to ASIZ1/O, WORD Invalid <u>15</u> /	t _{G6}				6	42	
PAS[1] to MWB[H] 15/	t _{G7}			:	2	36	
ABEN[1] to A[31:8] Invalid 15/	t _{G8}				1	11	
LA[31:8], FCi, R/W Valid to PAS[0] (Set-Up Time)	^t H1	Master Block Transfer Initiation Cycle See figure 3			10		
PAS[O] to ASIZ1/O, WORD Valid	t _{H2}				6	37	
PAS[0] to DSACKi[L]	t _{H3}				5+T	40+2T	
PAS[0] to MWB[L]	t _{H4}				10	35	
PASE1] to ASIZ1/O, WORD (Hold Time)	t _{H5}				6	42	
PAS[1] to DSACK1[H] 15/	t _{H6}	1			4	18	
PASE1] to MWBEH]	t _{H7}				2	36	
ABEN[0] to A[31:8] Valid 15/	t _{H8}				2	20	
LAEN[1], FCi Valid to LA[31:8] Valid 15/	t _{H9}				3	27	
PAS[L], FCi Valid to LDMACK[L] 15/	t _{H10}	1	ļ		1	31	7

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Test	Symbol	Condit -55°C ≤ T _C	ions ≤ +125°C	Group A	Device	Limit		Unit
		4.5 V ≤ V _C unless of specifi	$T_C \le +125^{\circ}C$ Group A subgroups otherwise ified $\underline{1}/$	type	Min	Max		
BLT[1] to LA[31:8] Incremented <u>15</u> /	^t I1	Boundary Cros See figure 3	sing	9,10,11	ALL	1	33	ns
LADO[0] to A[31:8] Incremented 15/	t ₁₂					4	33	
LA[31:8], FCi, R/W Valid to PAS[0] (Set-Up Time)	t _{J1}	PIO Output See figure 3				10		
LD[31:16] to PAS[0] (Set-Up Time)	t _{J2}					5		
PASEOJ to DSACKIELJ 15/	t _{J3}					T+5	40	
PASEO] to PIOE13:0] Valid 15/	t _{J4}					3	6 3 +2T	
PAS[1] to DSACKi[H] 15/	t _{J5}					4	18	
PAS[1] to LA[31:8], FCi, R/W (Hold Time)	t _{J6}					5		
PAS[1] to LD[31:16] Invalid 15/	t _{J7}					5	45	
LAE31:8], FCi, R/W Valid to PASEO] (Set-Up Time) 6/	^t K1	PIO Input See figure 3				10		
PIO[13:0] to PAS[0] (Set-Up Time) 6/	^t K2					5		
PAS[O] to DSACKi[L] 15/	^t k3					5 T+40	T+40	
PAS[0] toLD[31:16] Valid 15/	^t K4					7	58+T	
See footnotes at end of table							<u> </u>	
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TABLE I. <u>Electrical performance characteristics</u>.

Test	Symbol	Conditions $-55^{\circ}C \le T_C \le +125^{\circ}C$ $4.5 \ V \le V_{CC} \le 5.5 \ V$	Group A	Device	Lim	iit	Unit
		unless otherwise specified 1/	subgroups	type	Min	Max	
PAS[1] to DSACKi[H] 15/	t _{K5}	PIO Input See figure 3	9,10,11	ALL	4	18	ns
PAS[1] to LA[31:8], FCi, R/W (Hold Time) <u>6</u> /	t _{K6}				5		
PAS[1] to LD[31:16] Invalid <u>15</u> /	t _{K7}				5	45	
Frequency of Operation 6/		Clock Inputs See figure 3			1	40	
Cycle time <u>6</u> /	1				25	1000	
Clock Pulse Width (measured from 1.5V to 1.5V)	2,3				11.25		
Rise and Fall time	4,5					5	

- 1/ All testing to be performed using worst-case test conditions. The following pins are active low: RESET, WORD, R/W, PAS, DSACKI, R/W, ASIZ, ASIZO, ASIZO, ASIZO, IONE, SLSELO, SLSELO, IOSELS, IOSEL4, IOSEL5, ICFSEL, MWB, ABEN, LDMACK, BLT, FCIACK, MWB, FPUCS, DRAMCS, CACHIN, IOSELO, IOSEL1, SHRCS, VICSEL,
- DDIR, VSBSEL, VICLBR, REFGT. The asterisk (*) is used to indicate active low signals.

 VMEbus signals (Low Drive, all VMEbus Daisy Chain Signals) and all non-VMEbus signals.

 VMEbus signals (AS*, DS1*, DS0*, BCLR*, SYSCLK*) and VMEbus signals (Meduim Drive, All non-High, non-Low Drive Signals).
- VMEbus pins. All outputs disabled.
- Non-VMEbus pins, all outputs disabled.
- Tested initially and at process and design changes. Thereafter guaranteed, if not tested, to the limits specified in table I.
- specified in table I.

 7/ Chip select can be any of DRAMCS*, EPROMCS*, SHRCS*, VSBSEL*, FPUCS*, CS*, or IOSELi*.

 8/ The Decode Control register provides facilities to condition DRAMCS* or boundary decodes with the assertion of PAS*.

 9/ PI1 is the programmable interval for EPROMCS*, SHRCS*, and IOSELi* in the DSACKi* Control register.

 10/ PI3 is the programmable interval for IORD and IOWR in the Decode Control register.

 11/ Chip select can be any of DRAMCS*, EPROMCS*, SHRCS*, or VSBEL*.

 12/ PI2 is the programmable interval for EPROMCS*, SHRCS*, DRAMCS*, or VSBSEL* in the Decode Control register.

 13/ SLSELi* redirection is enabled in the Decode Control register.

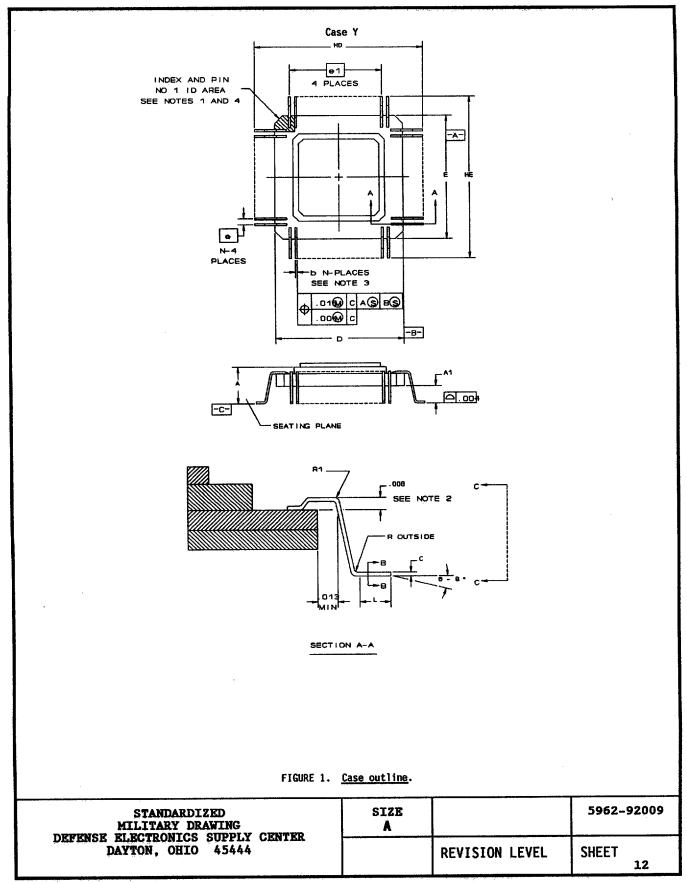
 14/ The maximum time LD[31:16] invalid is PAS[0] +3.5T or PAS[1] whichever occurs first.

- $\overline{15}$ / Minimum limits for subgroups 9,10,11 are guaranteed but, not tested.

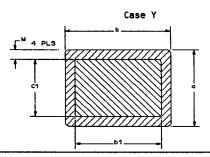
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	Variation	1						
Symbol		Inc	hes			Millin	neters	4
	Min	Nom	Max	Note	Nin	Nom	Max	Note
A	.080		.110		2.04		2.80	
A1	0.22	0.30	0.38		0.56	0.76	0.98	
b	.006		.015	3	0.15		0.33	3
b1	.006		.013	3	0.15		0.38	3
С	.002		.008	3	0.05		0.20	3
c1	.004		.008	3	0.10		0.20	3
D/E	1.098	1.102	1.106		27.94	28.05	28.15	
e		.025 BSC				0.64 BSC	·	
e1		.800 BSC				20.36 BSC		
HD/HE	1.218	1.228	1.238		31.00	31.26	31.51	
L	.012	.020	.028		0.31	0.51	0.71	
М			.0015				0.038	
N		160		4		160	<u> </u>	4
ND/NE		40		5		40		5
R	.011		.025		0.28		0.64	
R1	.010				2.55			
Notes			5	<u> </u>			6	<u> </u>

Notes:

 A terminal 1 identification mark shall be located at the index corner in the shaded area shown. Terminal 1 is located immediately adjacent to and counterclockwise from the index corner. Terminal numbers increase in a counterclockwise direction when viewed as shown.

Generic lead attach dogleg depiction. May be flat configuration.

 Dimensions b and c include lead finish; dimensions b1 and c1 apply to base metal only. Dimension M applies to plating thickness.

4. Dimension N: number of terminals

5. Dimension ND/NE: Number of terminals per package edge.

The leads of this package style shall be protected from mechanical distortion and damage such that dimensions pertaining to relative lead/body "true position" and lead "coplanarity" are always maintained until the next higher level package attachment process is complete. Package lead protection mechanisms (tie bars, carriers, etc) are not shown on the drawing, however when microcircuit devices contained in this package style are shipped for use in government equipment, or shipped directly to the Government as spare parts or mechanical qualification samples, lead 'true position' and "coplanarity" protection shall be in place.

FIGURE 1. Case outline. - Continued

STANDARDIZED
MILITARY DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE
A

REVISION LEVEL SHEET
13

DESC FORM 193A JUL 91

= 9004708 0004577 453 **==**

		- (Case Outline X			
Terminal No.	Symbol	Terminal No.	Symbol	Tannin-l N		
A 1	A ₂₃	D13	PIO8/IOSEL4	Terminal No.	Symbol	
A2	A20	D14		M14	LA14	
A3	A20 A17	D15	VICSEL	M15	LA18	
A4	And		PIO12/SHRCS	N1	ID14	
A5	A16	E1	LADI	N2	FCIACK	*
A6	A14	E2	ABEN	N3	CPUCLK	
A7	A ₁₂ A ₁₀	E3	LDMACK	N4	FC2	
A8	^1 0	E13	V LÄ31	N5		
	⁴ 08	E14	LÄ31	N6	Vcc	
A9	A25 A27 A29	E15	LA28	N7	VSS LD23	
A10	A ₂₇	F1	BLT	N8	LD24	
A11	A ₂₉	F2	PIO4/IORD	N9	LUZ4	
A12	731	F3		NTO	Vss Vcc Dramcs	
A13	A ₃₀ PIO2/TXDB	F13	V _{SS} LA29		v _C C	
A14	PĬŎ2/TXDB	F14	LA26	N11	DRAMCS	•
A15	٧٥٥	F15		N12	v _{ss}	
B1	V _{CC} PIO13/IOSEL2	G1	LA27	N13	V _{SS} LA11	
B2	A ₂₂	G2	REFGT	N14	LA12	
в3	Acc		VSBSEL	N15	LA16	
84	A19	G3	VICLBR	P1	ASIZO*	
B5	A18	G13	V SS LA24	P2	FCO	
B6	A15	G14		P3	LAEN	
B7	A13	G15	LA25	P4	R/W*	
B8	A ₁₁	H1	ICFSEL	P5	DSACKO*	
	A ₀₉	H2	SLSELO	P6	LD16	
89	A ₂₄	H3	Vcc	P7		
B10	A ₂₆	H13	You	P8	LD18	
B11	A26 A28 PIO1/RXDA	H14	VCC LA22	P9	LD22	
B12	PĪŎ1/RXDA	H15	LA23		LD27	
B13	PIO3/RXDB	J1	SLSEL1	P10	LD29	
B14	PIO6/IOSEL3	J2		P11	LD31	
B15	PIO9/IOSEL5	J3	IDIO	P12	EPROMCS:	
C1	DDIR	J13	V _{SS} VCC IOSEL1	P13	CACHINH	k
c2	SWDEN		V _{CC}	P14	LA8	
C3		J14	IOSEL1	P15	LA10	
C4 .	A21	J15	LA21	R1	FC1	
C5	Vss Vcc Vss Vcc Vss Vcc	K1	ID8	R2	PAS*	
C6	CCC	K2	ID9	R3	DSACK1*	
C7	.vss	K3	Vee	R4	LD19	
	Vcc	K13	V _{SS} V _{SS} LA17	R5	LD21	
c8	vss	K14	LÃÎ7	R6	LD17	
C9	v _{cc}	K15	LA19	R7		
C10	VSS	L1	ID11	R8	LD20	
C11	VSS PIOO/TXDA	L2	ID12		LD25	
C12	PIO5/IOWR	L3	ID15	R9	LD26	•
C13	P107	L13		R10	LD28	
C14	P1010	L14	LA13	R11	LD30	
C15	LA30	L15	LA15	R12	MWB*	
D1	PI011	M1	LA20	R13	FPUCS*	
D2	VAS	M2	ID13	R14	RESET*	
03	LADO	M2 M3	WORD	R15	IOSELO*	
D4	LOCATOR PIN	M13	ASIZ1 La9			
C)		FIGURE 2. <u>T</u>	erminal connection	<u>15</u> .	***************************************	
MIL	TANDARDIZED ITARY DRAWING TRONICS SUPPI		SIZE			5962-920

REVISION LEVEL

SHEET

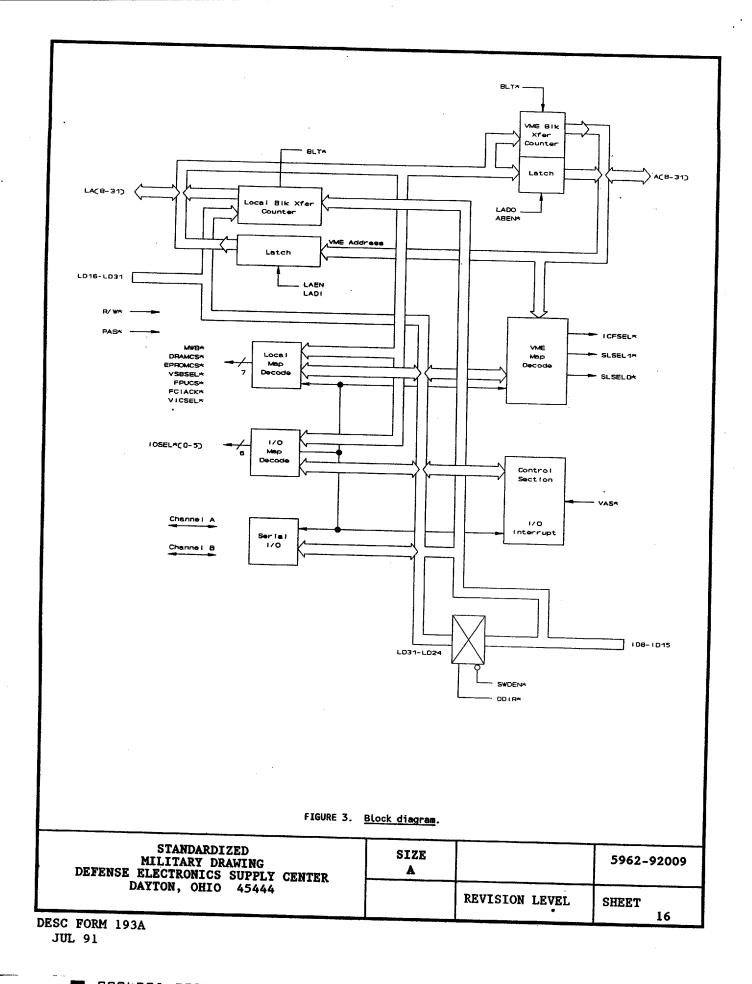
JUL 91

DESC FORM 193A

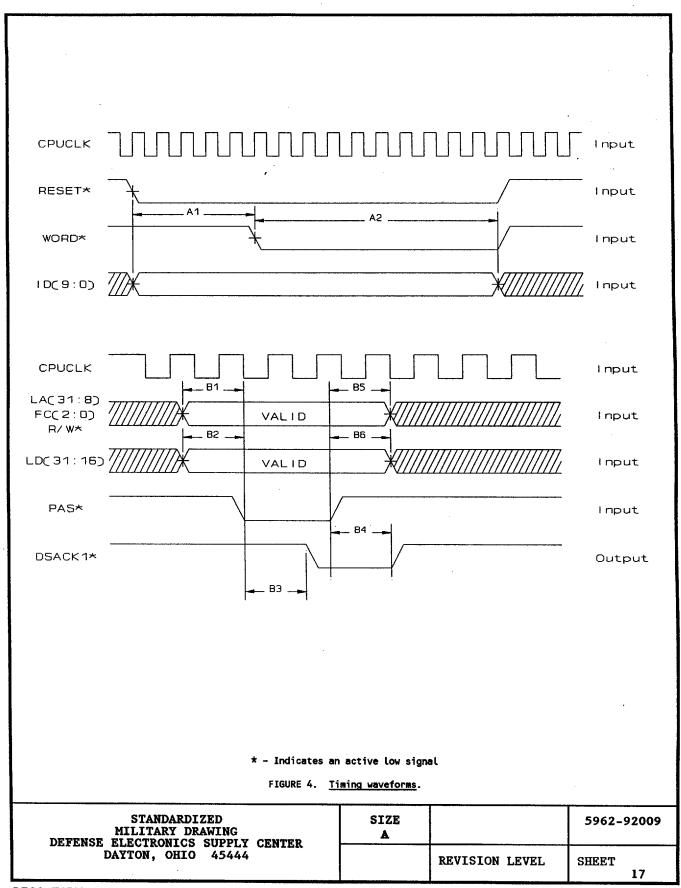
■ 9004708 0004578 39T ■

Terminal No. Symbol Terminal No. Symbol Terminal No. Symbol 1			va	ase Outline Y			
2 SIŠEL1 56 LA12 110 AÅD 3 108 57 LA10 111 A12 4 1010 58 LA14 112 A11 5 109 59 LA13 113 A13 A13 6 VSS 60 LA16 114 VSS 7 1071 61 LA15 115 A74 8 1072 62 LA18 116 A15 9 1073 65 VSS 100 1073 65 VSS 100 1073 65 VSS 101 1074 64 LA17 118 A17 101 1014 65 LA20 102 119 A18 103 119 65 LA20 103 119 A18 104 ASIZO 68 LA21 122 A20 104 ASIZO 68 LA21 122 A20 105 A22 124 A20 106 CPUCLK 70 LA22 125 A22 107 FCO 71 LA23 125 A22 107 FCO 71 LA23 125 A22 109 FCZ 73 VCS 127 LADO 109 FCZ 73 VCS 127 LADO 109 FCZ 75 LA27 129 PI013-105EL2 11 PAS 75 LA27 129 PI013-105EL2 12 PAS 75 LA27 129 PI013-105EL2 12 PAS 75 LA26 131 LDMACK 124 DSACKO 79 LA28 133 ABEN 127 VSS 81 PI012-SHRCS 135 VSS 130 LA20 136 PIO2-SHRCS 135 VSS 131 LA22 132 NSS 131 LA22 132 NSS 133 LA20 136 PIO2-SHRCS 135 VSS 131 LA22 139 VYCSEL 137 LADI 277 VSS 81 PI012-SHRCS 135 VSS 131 LA22 132 NSS 131 LA22 132 NSS 131 LA22 132 NSS 133 LA20 PIO3-SHRCS 135 VSS 134 LA22 139 VYCSEL 137 LADI 277 VSS 81 PI012-SHRCS 135 VSS 131 LA22 132 NSS 131 LA22 132 NSS 131 LA22 132 NSS 133 LA20 NSS 134 LA22 135 NSS 135 LA26 PIO2-TORD 144 VCC 151 NSS 151 LA25 159 PIO1-TORD 151 NSS 152 LA27 129 PI013-TOSEL2 154 NSS 155 LA27 139 PIO2-TORD 157 NSS 158 LA29 132 NSS 159 LA28 133 ABEN 151 LA22 139 VYCLURR 151 LA23 135 NSS 151 LA23 135 NSS 152 LA31 134 LOPACK 152 NSS 153 LA26 PIO2-TORD 153 LA26 PIO2-TORD 154 LA26 PIO2-TORD 155 LA26 PIO2-TORD 155 LA26 PIO2-TORD 155 LA27 129 PIO1-TORD 156 LA27 NSS 157 LA26 131 LOPACK 157 NSS 158 LA27 129 PIO1-TORD 158 A3 NSS 159 LA27 129 PIO1-TORD 159 NSS 150 LA26 PIO2-TORD 150 LA26 PIO2-TORD 150 LA26 PIO2-TORD 150 LA27 PIO2-TORD 150 LA26 PIO2-TORD 150 LA27 PIO2-TORD 150 LA26 PIO2-TORD 150 LA27 PIO2-TORD 150 LA28 PIO2-TORD 150 LA26 PIO2-TORD 150 LA27 PIO2-TORD 150 LA26 PIO2-TORD 150 LA26 PIO2-TORD 150 LA26 PIO2-TORD 150 LA27 PIO2-TORD	Terminal No.	Symbol	Terminal No.	Symbol	Terminal No.	Symbol	
3 108 57 LA10 111 A12 4 1010 58 LA14 112 A11 5 109 59 LA13 113 A13 6 VSS 60 LA16 114 VSS 7 1011 61 LA15 115 A14 8 1012 62 LA18 116 A15 9 1013 63 VSS 117 A16 10 1014 64 LA17 118 A17 11 WORD 65 LA20 119 A18 12 1015 66 105EL1 120 VCC 135 FLAKK 67 VCC 121 A19 14 A312D 68 LA19 122 A20 15 A312D 68 LA19 122 A20 15 A312D 68 LA19 122 A20 15 A312D 68 LA21 123 VSS 16 CPUCLK 70 LA23 125 A22 17 FCO 71 LA23 125 A22 18 FC1 72 VCC 126 A23 19 FC2 75 VSS 127 LA00 21 LAEN 74 LA27 129 SUBBN 22 PAN 76 LA27 129 P133-105EL2 22 PAN 76 LA27 129 P133-105EL2 23 VSC 77 LA26 131 134 P1011 24 D19 80 LA31 134 P1011 27 VSS 81 P1012-SHRCS 135 VSS 28 LB16 82 LB16 82 LB29 132 DB6K-10RB 27 VSS 81 P1012-SHRCS 135 VSS 28 LB16 82 LB16 82 P109-105EL5 140 BLT 31 LD23 85 P109 LO21 83 VSSSEL 32 LD17 86 P109-105EL5 140 BLT 33 LD20 87 P109-105EL5 140 BLT 34 LD22 88 P107 142 SISED 34 LD24 90 VCC 144 REFET 35 LS25 89 P106-105EL5 140 BLT 36 LD24 90 VCC 144 VCC 37 VSS 91 P109-105EL5 140 BLT 36 LD24 90 VCC 144 VCC 37 VSS 91 P109-105EL5 140 BLT 34 LD22 88 P107 142 SISED 35 LD26 97 P103-RNDB 36 LD26 99 P103-RNDB 37 LD28 99 P103-RNDB 38 LD26 99 P103-RNDB 39 LD28 99 P103-RNDB 30 LD28 99 P103-RNDB 31 LD23 99 VSS 34 LD31 98 A31 LD22 A24 44 LD31 98 A31 45 MBB 99 VSS 35 LAB LD31 DD A26 47 EPRONIS 101 A29 48 DAANCS 102 A24 48 DAANCS 102 A24 49 P103-RNDB 35 LD26 99 P103-RNDB 36 LD26 99 P103-RNDB 37 LD28 99 VSS 38 LD30 97 A28 48 DAANCS 102 A24 48 DAANCS 102 A24 48 DAANCS 102 A24 49 P103-RNDB 35 LD26 99 P103-RNDB 36 LD26 99 VSS 37 P100-RNDB 37 LD27 94 P100-RNDB 38 LD26 99 VSS 39 LD28 99 LD21 98 A31 40 LD21 98 A31 41 LD22 BB A31 42 LD31 98 A31 43 LD30 97 A28 44 LD31 98 A31 45 LD30 97 A28 46 DAANDBLEED		v _{ss} '				V _{CC}	
4	2						
5							1
6							,
7					113		
S		V _{SS}		LA16	114		
S	7		61			A74	
9 1013 63 V _{SS} 117 A16 10 1014 64 LA17 118 A17 11 UORD 65 LA20 119 A18 12 1015 66 10SEL1 120 V _C 13 FCIACK 67 V _C 121 A19 14 ASIZO 68 LA19 122 A20 15 ASIZO 69 LA21 123 V _S 16 CPULK 70 LA22 124 V _S 17 FCO 71 LA23 125 A22 17 FCO 71 LA23 125 A22 19 FCZ 73 V _C 126 A23 19 FCZ 73 V _C 127 LA00 20 LAEN 74 LA25 128 SWEN 21 PAS 75 LA27 129 P1013-10SEL2 22 R/V 76 LA24 130 V _S 23 V _C 77 LA26 131 LDMACK 24 DSACKI 78 LA29 132 DDIR 25 DSACKO 79 LA28 133 ABEN 26 LDD 80 LA31 134 P1011 27 V _S 81 P1012-SHRCS 135 V _S 28 LDB 82 LDB 82 LDB 82 LDB 83 VICSEL 137 LA01 27 V _S 81 P1072-SHRCS 135 V _S 30 LDB 84 V _S 31 LD20 87 P109-10SEL5 140 BLT 33 LD20 87 P109-10SEL5 140 BLT 34 LD23 85 P100 139 VICLER 35 LD26 99 P100-10SEL5 140 BLT 36 LD26 99 P100-10SEL5 140 BLT 37 V _S 91 P100-10SEL5 140 BLT 38 LD20 87 P100-10SEL5 140 BLT 39 LD28 93 P100-10SEL5 140 BLT 31 LD29 95 P100-10SEL5 140 BLT 33 LD20 87 P100-10SEL5 140 BLT 34 LD29 95 P100-10SEL5 140 BLT 35 LD26 92 P103-RNDB 44 LD29 95 P100-10SEL5 140 BLT 37 V _S 91 P100-10SEL5 140 BLT 38 LD20 87 P100-10SEL5 140 BLT 39 LD28 93 P100-10SEL5 140 BLT 44 LD29 95 P100-10SEL5 140 BLT 45 LD29 95 P100-10SEL5 140 BLT 47 V _S 91 P103-RNDB 44 LD29 95 P100-10SEL5 140 BLT 47 V _S 91 P103-RNDB 44 LD29 95 P100-10SEL3 143 LGFSEL 44 LD31 98 A31 45 LD31 98 A31 45 LD32 A24 48 CACHIN 103 V _S 48 CACHIN 103 V _S 48 CACHIN 103 V _S 49 P100-10SEL5 140 BLT 40 LD29 95 P100-10SEL5 140 40 LD27 94 P101-RNDB 41 LD29 95 P100-10SEL3 143 LGFSEL 51 LD31 98 A31 52 LD31 98 A31 53 LD31 98 A31 54 LD31 198 P103-10SEL5 P100-10SEL5 55 LB36 P100-10SEL5 P100-10SEL5 56 LD34 P100-10SEL5 P100-10SEL5 57 LB37 P100-10SEL5 58 LB36 P100-10SEL5 59 LB36 P100-10SEL5 50 LB36 P							
100	9						
111 WORD 65 LA20 119 A18 12 ID15 66 IOSEL1 120 V _C C 133 FCIACK 67 V _C C 121 A19 14 ASIZO 68 LA19 122 A20 15 ASIZI 69 LA21 123 V _S 16 CPUCLK 70 LA22 124 V _C 17 FCO 71 LA23 125 V _S 18 FCI 72 V _C C 126 A23 19 FCZ 73 V _C C 126 A23 19 FCZ 73 V _C C 126 A23 19 FCZ 73 V _C C 127 LADO 20 LAEN 74 LA27 129 PIO13-IOSEL2 21 PAS 75 LA26 131 LDMACK . 22 R/W 76 LA24 130 VAS 22 R/W 76 LA24 130 VAS 24 DSACKO 79 LA28 133 ABEN 26 LD19 80 LA31 134 PIO11 27 V _S 81 PIO12-SHRCS 135 V _S 28 LD16 82 LA30 136 PIO4-IORD 29 LD21 83 VICSEL 137 LADI 30 LD18 84 V _S 138 VICSEL 137 LADI 31 LD23 85 PIO10 139 VICLBR 31 LD23 85 PIO10 139 VICLBR 32 LD17 86 PIO9-IOSEL5 140 BLT 33 LD20 87 PIO8-IOSEL4 141 REFGT 34 LD22 88 PIO7 142 SILSELO 35 LS25 89 PIO6-IOSEL3 143 ICFSEL 36 LD24 90 V _C 77 A28 44 LD22 88 PIO7 142 SILSELO 45 HWB 99 V _S 46 FFUCS 100 A26 47 FFROMCS 101 A29 48 CACHIN 103 V _S 51 LB28 93 PIO2-TIOB 40 LD27 94 PIO1-RXDA 41 LD29 95 PIO0-TXDA 42 V _C 96 A30 43 LAB 107 A8 54 ID30 RESET 104 A27 55 LASE 104 A27 55 LASE 105 A25 56 LAB 107 A8 57 LAB 107 A8 58 LAB 107 A8 59 LAB 107 A8 50 RESET 104 A27 51 V _S 105 A25 52 LAT1 106 A9 53 LAB 107 A8 54 IOSELO 108 VSS				LÃŶ7			
12							
133 FCIACK 67 V,C 121 AP 14 ASIZO 68 LA19 122 AZO 15 ASIZI 69 LA21 123 V,S 16 CPUCLK 70 LA22 124 VZ 17 FCO 71 LA23 125 V,S 18 FC1 72 V,C 126 AZ3 19 FCZ 73 V,C 127 LADO 19 FCZ 73 V,C 127 LADO 20 LAEN 74 LA27 129 PIOT3-IOSEL2 21 PAS 75 LA24 130 VAS 22 R/W 76 LA24 130 VAS 24 DSACKO 79 LA28 133 ABEN 25 DSACKO 79 LA28 133 ABEN 26 LD19 80 LA31 134 PIOT1 27 VS,S 81 PIOT2-SHRCS 135 V,S 28 LD16 82 LA30 136 PIO-1ORD 29 LD21 83 VICSEL 137 LADI 30 LD18 84 V,S 138 VSSSEL 31 LD23 85 PIOT0 31 LD23 85 PIOT0 32 LD17 86 PIO9-IOSELS 140 BLT 33 LD20 87 PIO8-IOSELS 140 BLT 34 LD22 88 PIOT 142 SILSELO 35 LS25 89 PIOF 10SELS 141 REFGT 35 LS25 89 PIOF 10SELS 141 REFGT 36 LD24 90 V,C 141 REFGT 37 V,S 91 PIOS-IOSELS 143 ICFSEL 37 V,S 91 PIOS-IOSELS 140 BLT 38 LD20 87 PIOR-IOSELS 141 REFGT 35 LS25 89 PIOF 10SELS 141 REFGT 36 LD24 90 V,C 141 REFGT 37 V,S 91 PIOS-IOWR 38 LD28 93 PIOT-INDR 40 LD27 94 PIOT-RNDA 41 LD29 95 PIOG-ITRDA 42 V,C 96 AJO 44 LD31 98 AJ1 45 HWB 99 V,S 52 LD11 AZ9 53 LAB 107 AZ8 54 LD31 98 AJ1 55 LASELO 108 AZ6 64 FPUCS 100 AZ6 64 FPUCS 100 AZ6 65 PIOS-IOWR 65 PIOS-IOWR 65 PIOS-IOWR 65 PIOS-IOWR 67 PIOS-IOWR 67 PIOS-IOWR 67 PIOS-IOWR 68 AJO 68 CACHIN 103 V,CC 68 AJO 68 CACHIN 104 V,CC 68 AJO 68 CACHIN 1							
14 ASIZO 68 LA19 122 A20 15 ASIZT 69 LA21 123 V _S 16 CPUCLK 70 LA22 124 VŽI 17 FCO 71 LA23 125 A22 18 FC1 72 V _{CC} 126 A23 19 FCZ 73 V _{CC} 127 LADO 20 LAEN 74 LŽŠ5 128 SUDEN 21 PAS 75 LA27 129 PIOT3-IOSEL2 22 R/N 76 LA24 130 VAS 23 V _{CC} 777 LA26 131 LDNACK 24 DŠACKI 78 LA29 132 DDIR 25 DSACKO 79 LA28 133 ABEN 26 LD19 80 LA31 34 PIOT1 27 V _S 28 1 PIOT2-SHRCS 135 V _S 29 LD21 83 VICSEL 137 LADI 29 LD21 83 VICSEL 137 LADI 30 LD18 84 V _{SS} 31 LD25 85 PIOTO 33 LD20 87 PIOS-IOSEL5 140 BLT 34 LD22 88 PIOT 35 LS25 89 PIOG-IOSEL5 140 BLT 36 LD22 88 PIOT 37 V _S 38 LD20 87 PIOS-IOSEL5 140 BLT 37 V _S 38 LD20 87 PIOS-IOSEL5 140 BLT 37 V _S 38 LD20 87 PIOS-IOSEL5 140 BLT 39 LD22 88 PIOT 142 SLSELD 31 LD22 88 PIOT 142 SLSELD 32 LD27 94 PIOT-NDA 33 LD20 87 PIOS-IOSEL5 140 BLT 34 LD22 88 PIOT 142 SLSELD 35 LS25 89 PIOG-IOSEL5 140 BLT 36 LD24 90 V _{CC} 37 V _S 38 LD20 87 PIOS-IOSEL5 140 BLT 39 LD22 88 PIOT 142 SLSELD 37 V _S 38 LD20 87 PIOS-IOSEL5 140 BLT 39 LD22 88 PIOT 142 SLSELD 31 LD22 88 PIOT 142 SLSELD 32 LD17 86 PIOT-NDA 34 LD22 88 PIOT-NDA 35 LD26 92 PIOS-NDA 44 LD27 94 PIOT-NDA 45 MB 99 V _S 37 V _S 38 LD28 93 PIOC-IOSEL3 143 ICFSEL 48 CACHIN 103 V _S 47 EPROMCS 101 A29 48 DRAMCS 101 A29 49 PIOT-NDA 40 LD27 94 PIOT-NDA 41 LD29 95 PIOT-NDA 42 V _{CC} 43 LD30 97 A28 44 LD31 98 A31 45 MB 99 V _S 55 LAB DRAMCS 107 A8 50 RESET 104 A27 51 V _S 51 LAB DRAMCS 107 A8 51 LOSELD 108 VSS						372	
15 ASIZT 69 LA21 123 V _S 16 CPUCLK 70 LA22 124 VŽ1 17 FCO 71 LA23 125 A22 18 FC1 72 V _{CC} 126 A23 19 FCZ 73 V _{CC} 127 LADO 20 LAEN 74 LÅ25 128 SWDEN 21 PAS 75 LA27 129 P1013-IOSEL2 22 R/W 76 LA24 150 VAS 23 V _{CC} 131 LDMACK 24 DŠACKI 78 LA29 132 DDIR 25 DSACKO 79 LA28 133 ABEN 26 LD19 80 LA31 134 P1011 27 V _S 81 P1072-SHRCS 135 V _S 28 LĎ16 82 LA30 136 P104-IORD 29 LD21 83 VICSEL 137 LADI 30 LD18 84 V _S 29 LD21 83 VICSEL 137 LADI 30 LD18 84 V _S 31 LD23 85 P1070 139 VICLBR 31 LD23 85 P1070 139 VICLBR 33 LD20 87 P108-IOSEL5 140 BLT 33 LD20 87 P108-IOSEL5 140 BLT 34 LD22 88 P107 142 SLSELD 35 LS25 89 P106-IOSEL5 140 BLT 36 LD24 90 V _{CC} 37 V _S 38 LD20 87 P108-IOSEL5 140 BLT 36 LD24 90 V _{CC} 37 V _S 38 LD20 87 P108-IOSEL5 140 BLT 36 LD24 90 V _{CC} 41 LD29 95 P100-TXDA 42 V _C 43 LD29 95 P100-TXDA 44 LD29 95 P100-TXDA 45 MWB 99 V _S 46 FPUCS 100 A26 47 EPRONCS 101 A29 48 DRAMCS 102 A24 44 LD31 98 A31 45 MWB 99 V _S 50 RESET 104 A27 51 V _S 51 LAS 107 A8 54 IOSELO 108 VSS				¥ Ç 4		A17	
16 CPUCLK 70 LA22 124 V27 17 FCO 71 LA23 125 A22 18 FC1 72 Vcc 126 A23 19 FCZ 73 Vcc 127 LADO 20 LAEN 74 LA25 128 SUDEN 21 PAS 75 LA27 129 P1013-IOSEL2 21 PAS 75 LA27 129 P1013-IOSEL2 22 R/W 76 LA24 130 VAS 23 Vc 777 LA26 131 LDMACK . 24 DSACKI 78 LA29 132 DDLR 25 DSACKO 79 LA28 133 ABEN 26 LD19 80 LA31 34 P1001 27 Vs 81 P10012-SHRCS 135 Vs 28 LD16 82 LA30 136 P1004-IOSEL 29 LD21 83 VICSEL 137 LADI 27 US 138 VICSEL 137 LADI 28 LD18 84 Vs 138 VICSEL 137 LADI 30 LD18 84 Vs 138 VICSEL 137 LADI 31 LD23 85 P1001 139 VICLER 31 LD23 85 P1001 139 VICLER 33 LD20 87 P108-IOSEL5 140 BLT 33 LD20 87 P108-IOSEL5 140 BLT 34 LD22 88 P107 142 SLSELD 35 LS25 89 P106-IOSEL3 143 ICFSEL 36 LD24 90 VC 142 SLSELD 37 Vs 94 P101-RNDA 40 LD27 94 P101-RNDA 41 LD29 95 P100-TNDA 42 VC 96 A30 43 LD30 RSSEL 450 P102 A24 44 LD31 98 A31 45 HWB 99 Vs 46 FPUCS 100 A26 47 EPROMCS 101 A29 48 DRAMCS 102 A24 48 CACHIN 103 VCC 51 LOSELD 108 VSS							
17 FCO 71 LA23 125 A22 18 FC1 72 VCC 1266 A25 19 FCZ 735 VCS 127 LADO 20 LAEN 74 LÄ55 128 SUPEN 21 PAS 75 LA27 129 PI013-IOSEL2 22 R/W 76 LA24 130 VAS 23 VCC 77 LA26 131 LDMACK 24 DŠÁCK1 78 LA29 132 DDIR 25 DSACKO 79 LA28 133 ABEN 26 LD19 80 LA31 134 PI011 27 VS 81 PI0012-SHRCS 135 VS 28 LD16 82 LA30 136 PI04-IORD 29 LD21 83 VICSEL 137 LADI 30 LD18 84 VS 138 VSSSL 31 LD23 85 PI010 139 VICLBR 31 LD23 85 PI091 139 VICLBR 33 LD00 87 PI08-IOSEL4 141 REFGT 34 LD22 88 PIO7 35 LS25 89 PI06-IOSEL3 143 ICFSEL 37 VS 91 PI05-IOWR 38 LD24 90 VCC 37 VS 91 PI05-IOWR 40 LD27 94 PI01-RNDA 40 LD27 95 PI00-TXDA 41 LD29 95 PI00-TXDA 42 VCC 96 A30 43 LD30 97 A28 44 LD31 98 A31 45 MWB 99 VS 46 FPUCS 100 A26 47 EPROMCS 101 A29 48 DRAMCS 102 A24 48 DRAMCS 102 A24 48 DRAMCS 102 A24 48 DRAMCS 102 A24 48 DRAMCS 101 A29 53 LA8 107 A8 54 LOSELO 108 VSS						v _s s	
18							
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17				Vcc			
21 PAS 75 L27 129 P1013-IOSEL2 22 R/W 76 L224 130 VAS 23 V _{CC} 77 LA26 131 LDMACK 24 DSACK1 78 LA29 132 DD1R 25 DSACKO 79 LA28 133 ABEN 26 LD19 80 LA31 134 P1011 27 V _S 81 P1012-SHRCS 135 V _S 28 LD16 82 LA30 136 P104-IORD 29 LD21 83 VICSEL 137 LADI 30 LD18 84 V _{SS} 31 LD23 85 P1010 139 VICLBR 31 LD23 85 P1001 139 VICLBR 32 LD17 86 P109-IOSEL5 140 BLT 33 LD20 87 P108-IOSEL4 141 REFGT 34 LD22 88 P107 142 SLSELD 35 LS25 89 P106-IOSEL3 143 ICFSEL 36 LD24 90 V _{CC} 144 V _{CC} 37 V _S 91 P105-IOWR 38 LD26 92 P103-RXDB 39 LD28 93 P106-TXDA 40 LD27 94 P101-RXDA 41 LD29 95 P100-TXDA 42 V _{CC} 96 A30 43 LD30 97 A28 44 LD31 98 A31 45 MWB 99 V _S 46 FPUCS 101 A29 47 EPRONCS 101 A29 48 CACHIN 103 V _{SS} 51 LSE 59 SP 52 LA11 106 A9 53 LAB 105EL0 108 VSS Figure 2. Terminal connections Continued				VSS			
22 R/N 76 L24 130 VAS 23 VCC 77 LA26 131 LDMACK 24 DSACK1 78 LA29 132 DDIR 25 DSACKO 79 LA28 133 ABEN 26 LD19 80 LA31 134 PIO11 27 VSS 81 PIO12-SHRCS 135 VSS 28 LD16 82 LA30 136 PIG4-IORD 29 LD21 83 VICSEL 137 LADI 30 LD18 84 VSS 138 VSSSEL 31 LD23 85 PIO10 139 VICLBR 31 LD23 85 PIO10 139 VICLBR 32 LD17 86 PIO9-IOSEL5 140 BLT 33 LD20 87 PIO8-IOSEL4 141 REFGT 34 LD22 88 PIO7 142 SLSELO 35 LS25 89 PIO6-IOSEL3 143 ICFSEL 36 LD24 90 VCC 37 VSS 91 PIO5-IOWR 38 LD26 92 PIO3-RXDB 39 LD28 93 PIO6-TXDA 40 LD27 94 PIO1-RXDA 41 LD29 95 PIO0-TXDA 42 VCC 96 A30 43 LD31 98 A31 45 MWB 99 VSS 46 FPUCS 100 A26 47 EPROMCS 101 A29 48 CACHIN 103 VCC 50 RESET 104 A27 51 VSS 105 A25 52 LA11 106 A9 53 LA8 107 A8 54 IOSELO 108 VSS	20						
23	21						2
23	22			LA24	130	VAS	
24 DŠĀCKI 78 L29 132 DDIR 25 DSACKO 79 LA28 133 ABEN 26 LD19 80 LA31 134 PIO11 27 V _S 81 PIO12-SHRCS 135 V _S 28 LD16 82 LA30 136 PIO4-TORD 29 LD21 83 VICSEL 137 LADI 30 LD18 84 V _{SS} 138 VSBSEL 31 LD23 85 PIO10 139 VICLBR 32 LD17 86 PIO9-IOSEL5 140 BLT 33 LD20 87 PIO8-IOSEL4 141 REF6T 34 LD22 88 PIO7 142 SLSELO 35 LS25 89 PIO6-IOSEL3 143 ICFSEL 36 LD24 90 V _{CC} 144 V _{CC} 37 V _S 91 PIO5-IOWR 38 LD26 92 PIO3-RXDB 39 LD28 93 PIO2-TXDB 40 LD27 94 PIO1-RXDB 41 LD29 95 PIO0-TXDA 42 V _{CC} 96 A30 44 LD31 98 A31 45 MWB 99 V _S 46 FPUCS 100 A28 47 EPROMCS 101 A29 48 DRANCS 102 A24 48 CACHIN 103 V _{CC} 51 LA8 IOSELO 108 VSS Figure 2. Terminal connections Continued	23	Vcc	77	LA26			
25 DSACKO 79 LA28 133 ABEN 26 LD19 80 LA31 134 P1011 27 VS 8 81 P1012-SHRCS 135 VS 8	24	DŠŘCK1					
26	25						
27	26						
28 LÖY6 82 LA30 136 PÎĞ4-IORD 29 LD21 83 VICSEL 137 LADI 30 LD18 84 V _S S 138 VSBSEL 31 LD23 85 PIÖ10 139 VICLBR 32 LD17 86 PIO9-IOSEL5 140 BLT 33 LD20 87 PIO8-IOSEL4 141 REFGT 34 LD22 88 PIO7 142 SLSELD 35 LS25 89 PIO6-IOSEL3 143 ICFSEL 36 LD24 90 V _{CC} 37 V _S 91 PIO5-IOWR 38 LD26 92 PIO3-RXDB 39 LD28 93 PIO2-TXDB 40 LD27 94 PIO1-RXDA 41 LD29 95 PIO0-TXDA 42 V _{CC} 96 A30 43 LD30 97 A28 44 LD31 98 A31 45 MWB 99 V _S 46 FPUCS 100 A26 47 EPROMCS 101 A29 48 DRANCS 102 A24 48 DRANCS 102 A24 48 CACHIN 103 V _{CC} 50 RESET 104 A27 51 V _S S 105 A25 52 LA11 106 A9 53 LA8 107 A8 54 IOSELO 108 VSS Figure 2. Terminal connections - Continued	27						
29	28	"SS _A				TSS DTOK-TORD	
30 LD18 84 V _S 138 VSBSEL 31 LD23 85 PI010 139 VICLBR 32 LD17 86 PI09-IOSEL5 140 BLT 33 LD20 87 PIO8-IOSEL4 141 REFGT 34 LD22 88 PIO7 142 SLSELO 35 LS25 89 PI06-IOSEL3 143 ICFSEL 36 LD24 90 V _C 144 V _{CC} 37 V _S 91 PI05-IOWR 38 LD26 92 PIO3-RXDB 39 LD28 93 PIO2-TXDB 39 LD28 93 PIO2-TXDB 40 LD27 94 PIO1-RXDA 41 LD29 95 PIO0-TXDA 42 V _C 96 A30 43 LD30 97 A28 44 LD31 98 A31 45 MWB 99 V _S 46 FPUCS 100 A26 47 EPROMCS 101 A29 48 CACHIN 103 V _C 50 RESET 104 A27 51 V _S 105 A25 52 LA11 106 A9 53 LA8 107 A8 54 IOSELO 108 VSS Figure 2. <u>Terminal connections</u> Continued	20						
31							
32 LD17 86 PIO9-IOSEL5 140 BLT 33 LD20 87 PIO8-IOSEL4 141 REFGT 34 LD22 88 PIO7 142 SLSELO 35 LS25 89 PIO6-IOSEL3 143 ICFSEL 36 LD24 90 VCC 144 VCC 37 VSS 91 PIO5-IOWR 38 LD26 92 PIO3-RXDB 39 LD28 93 PIO2-TXDB 40 LD27 94 PIO1-RXDA 41 LD29 95 PIO0-TXDA 42 VCC 96 A30 44 LD31 98 A31 45 MWB 99 VSS 46 FPUCS 100 A26 47 EPROMCS 101 A29 48 CACHIN 103 VCC 51 VSS 105 A25 52 LA11 106 A9 53 LOSELO 108 VSS Figure 2. Terminal connections Continued				V _{SS.}			
33	31 						
34 L022 88 PIO7 142 SLSELO 35 LS25 89 PIO6-IOSEL3 143 ICFSEL 36 LD24 90 VCC 144 VCC 37 VS 91 PIO5-IOWR 38 LD26 92 PIO3-RXDB 39 LD28 93 PIO2-TXDB 40 LD27 94 PIO1-RXDA 41 LD29 95 PIO0-TXDA 42 VCC 96 A30 43 LD30 97 A28 44 LD31 98 A31 45 MWB 99 VSS 46 FPUCS 100 A26 47 EPROMCS 101 A29 48 DRAMCS 102 A24 48 CACHIN 103 VCC 50 RESET 104 A27 51 VS 105 A25 52 LA11 106 A9 53 LA8 107 A8 54 IOSELO 108 VSS Figure 2. Terminal connections Continued	32						
34 LD22 88 PIO7 142 SLSELO 35 LS25 89 PIO6-IOSEL3 143 ICFSEL 36 LD24 90 V _{CC} 144 V _{CC} 37 V _S 91 PIO5-IOWR 38 LD26 92 PIO3-RXDB 39 LD28 93 PIOC-TXDB 40 LD27 94 PIO1-RXDA 41 LD29 95 PIOO-TXDA 42 V _{CC} 96 A30 43 LD30 97 A28 44 LD31 98 A31 45 MWB 99 V _S 46 FPUCS 100 A26 47 EPROMCS 101 A29 48 DRAMCS 102 A24 48 CACHIN 103 V _{CC} 50 RESET 104 A27 51 V _{SS} 105 A25 52 LA11 106 A9 53 LA8 107 A8 54 IOSELO 108 VSS Figure 2. <u>Terminal connections</u> Continued							
35	34			P107			
36 LD24 90 V _{CC} 144 V _{CC} 37 V _S 91 PIO5-IOWR 38 LD26 92 PIO3-RXDB 39 LD28 93 PIO2-TXDB 40 LD27 94 PIO1-RXDA 41 LD29 95 PIOO-TXDA 42 V _{CC} 96 A30 43 LD30 97 A28 44 LD31 98 A31 45 MWB 99 V _S 46 FPUCS 100 A26 47 EPROMCS 101 A29 48 DRAMCS 102 A24 48 CACHIN 103 V _{CC} 50 RESET 104 A27 51 V _S 105 A25 52 LA11 106 A9 53 LA8 107 A8 54 IOSELO 108 VSS Figure 2. Terminal connections Continued	35						
38				۸۰۰	144		
38		٧ _{ee}	91	PĬŎ5-IOWR			
39	38	LĎŽ6					
40		LD28					
41							
42							
43 LĎ3O 97 A28 444 LD31 98 A31 45 MWB 99 V _S 46 FPUCS 100 A28 47 EPROMCS 101 A29 48 DRAMCS 102 A24 48 CACHIN 103 V _C 50 RESET 104 A27 51 V _S 105 A25 52 LÄ11 106 A9 53 LA8 107 A8 54 IOSELO 108 VSS Figure 2. Terminel connections Continued							
44 LD31 98 A31 45 MWB 99 V _S 46 FPUCS 100 A28 47 EPROMCS 101 A29 48 DRAMCS 102 A24 48 CACHIN 103 V _{CC} 50 RESET 104 A27 51 V _S 105 A25 52 LA11 106 A9 53 LA8 107 A8 54 IOSELO 108 VSS Figure 2. Terminal connections Continued		CC					
45 MWB 99 V _S S 46 FPUCS 100 A26 47 EPROMCS 101 A29 48 DRAMCS 102 A24 48 CACHIN 103 V _C C 50 RESET 104 A27 51 V _S S 105 A25 52 LÄ11 106 A9 53 LAB 107 A8 54 IOSELO 108 VSS Figure 2. Terminal connections Continued STANDARDIZED SIZE 5962-93							
46				A51			
47 EPROMCS 101 A29 48 DRAMCS 102 A24 48 CACHIN 103 V _{CC} 50 RESET 104 A27 51 V _{SS} 105 A25 52 LÄ11 106 A9 53 LA8 107 A8 54 IOSELO 108 VSS Figure 2. Terminal connections Continued STANDARDIZED SIZE 5962-93				v _{ss}			
48 DRAMCS 102 A24 48 CACHIN 103 V _{CC} 50 RESET 104 A27 51 V _S 105 A25 52 LA11 106 A9 53 LA8 107 A8 54 IOSELO 108 VSS Figure 2. Terminal connections Continued STANDARDIZED SIZE 5962-93				A26			
48							
48							
50 RESET 104 A27 51 V _S 105 A25 52 LA11 106 A9 53 LA8 107 A8 54 IOSELO 108 VSS Figure 2. <u>Terminal connections</u> Continued STANDARDIZED SIZE 5962-93			103				
51 V _S S 105 A25 52 LA11 106 A9 53 LA8 107 A8 54 IOSELO 108 VSS Figure 2. <u>Terminal connections</u> Continued STANDARDIZED SIZE 5962-93				A27			
52 LÃ1 106 A9 53 LA8 107 A8 54 IOSELO 108 VSS Figure 2. <u>Terminal connections</u> Continued STANDARDIZED SIZE 5962-92							
53 LA8 107 A8 54 IOSELO 108 VSS Figure 2. <u>Terminal connections</u> Continued STANDARDIZED SIZE 5962-92		L X 1					
54 IOSELO 108 VSS Figure 2. <u>Terminal connections</u> Continued STANDARDIZED SIZE 5962-92							
Figure 2. <u>Terminal connections</u> Continued STANDARDIZED SIZE 5962-92							
STANDARDIZED SIZE 5962-92	J.4	IOSELG	100	V33			
			Figure 2. <u>Termi</u>	nal connections.	- Continued		
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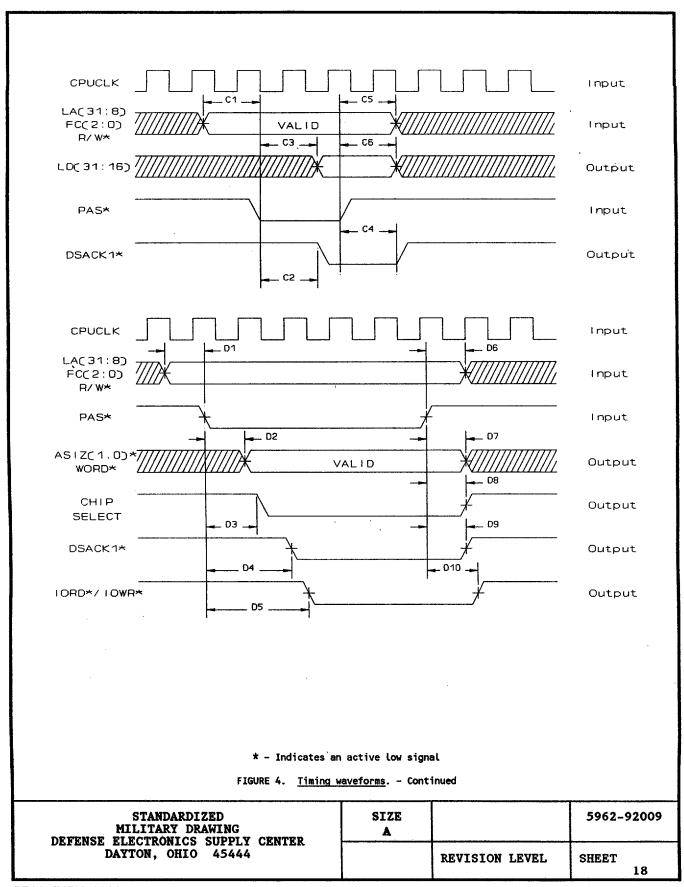
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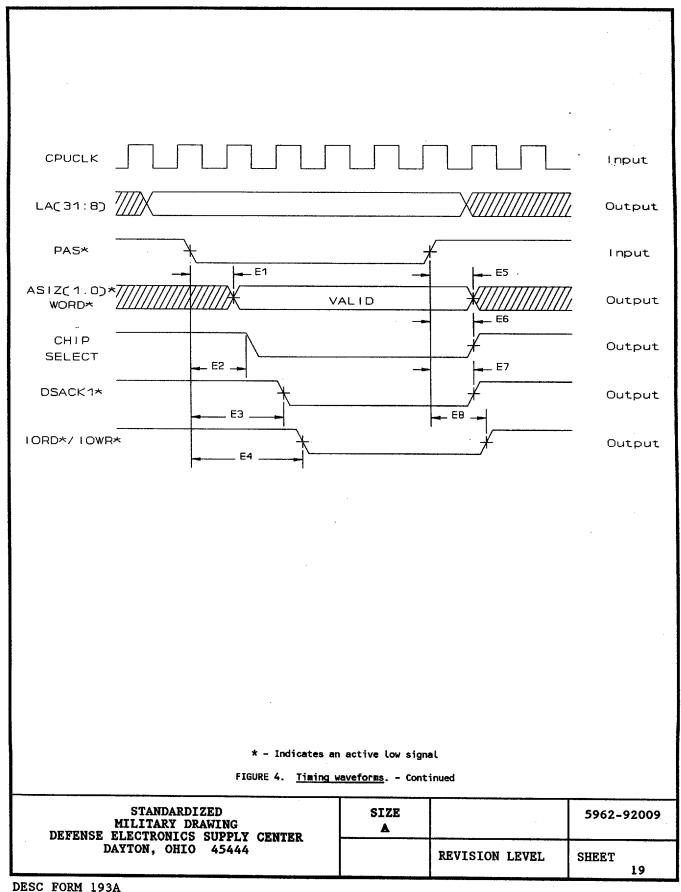
■ 9004708 0004580 T48 **■**



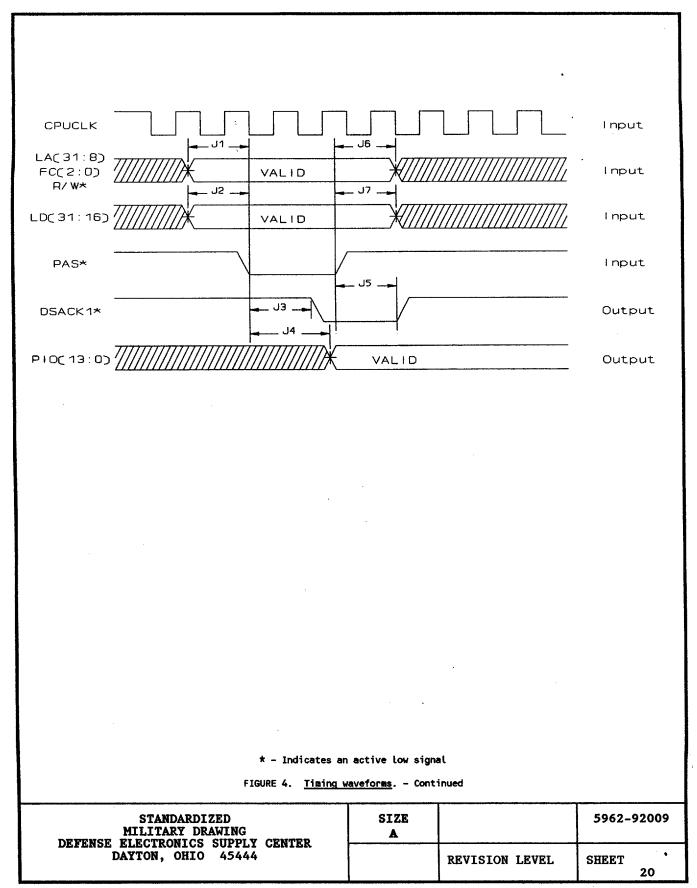
9004708 0004581 984



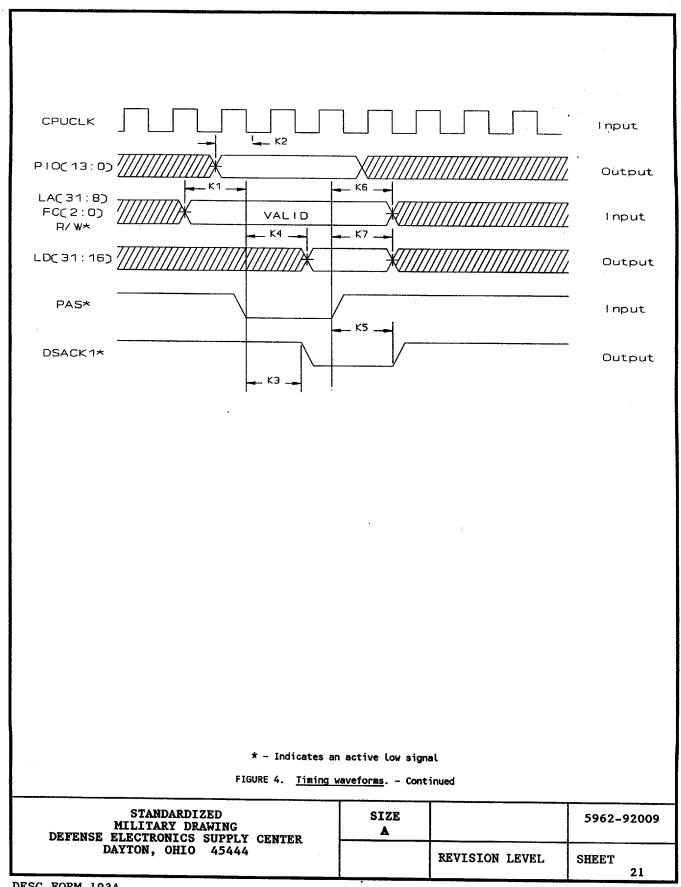
3 9004708 0004582 810

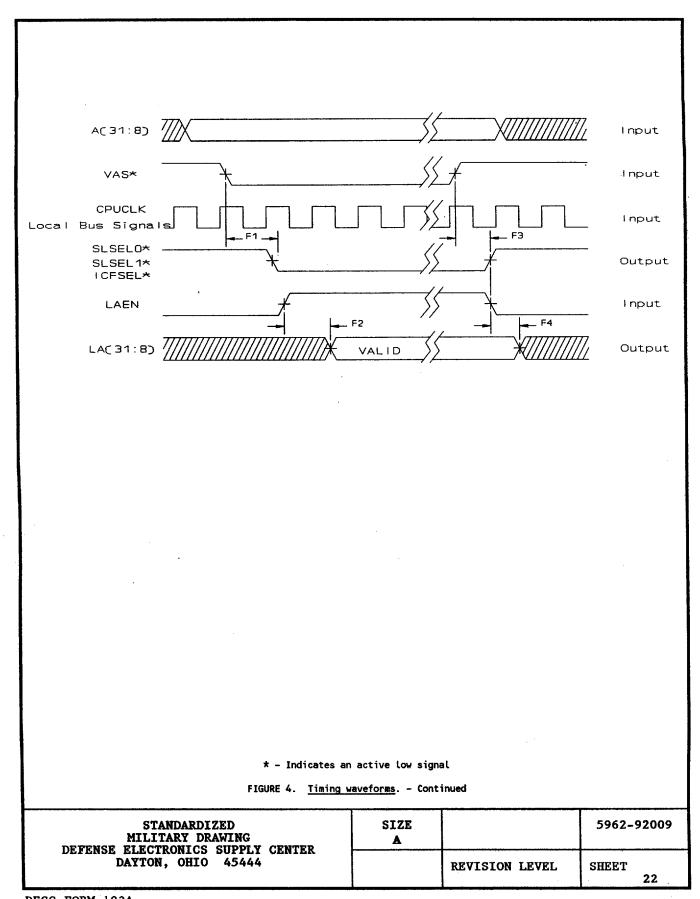


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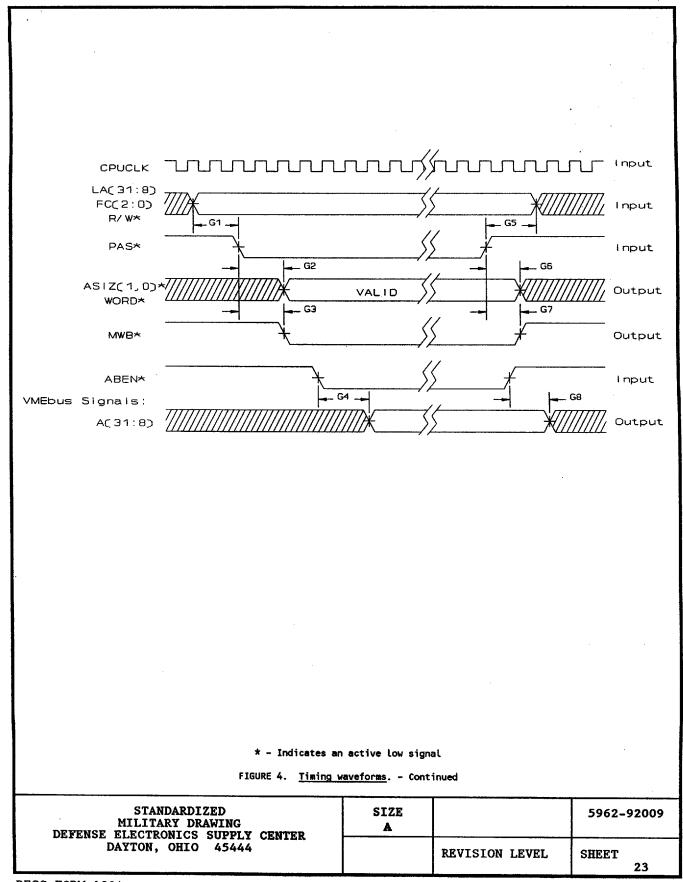


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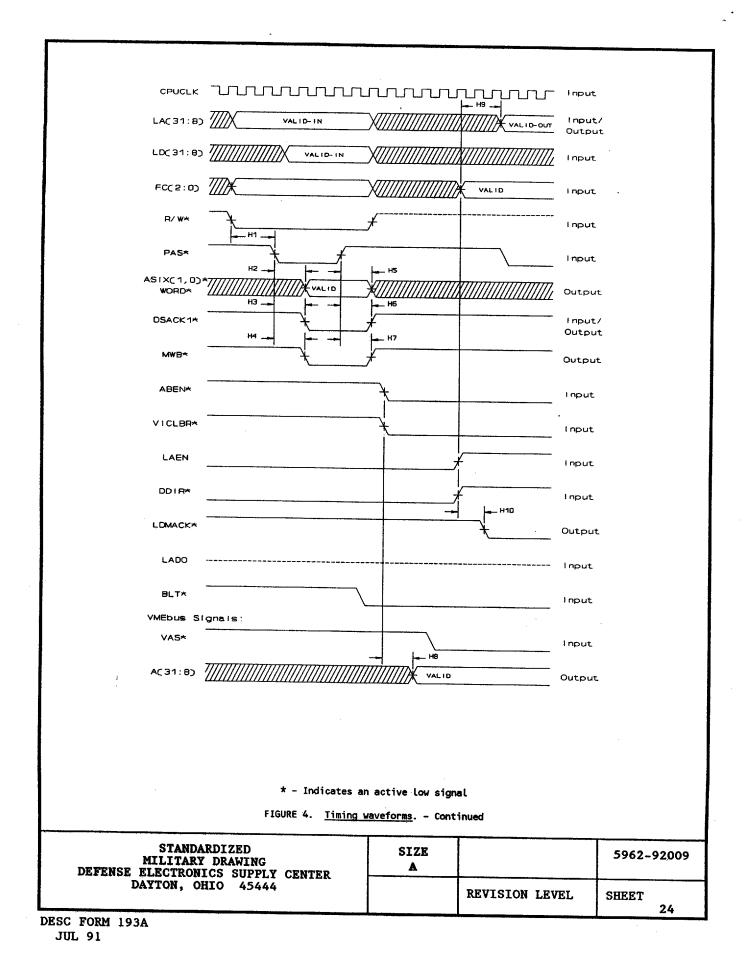




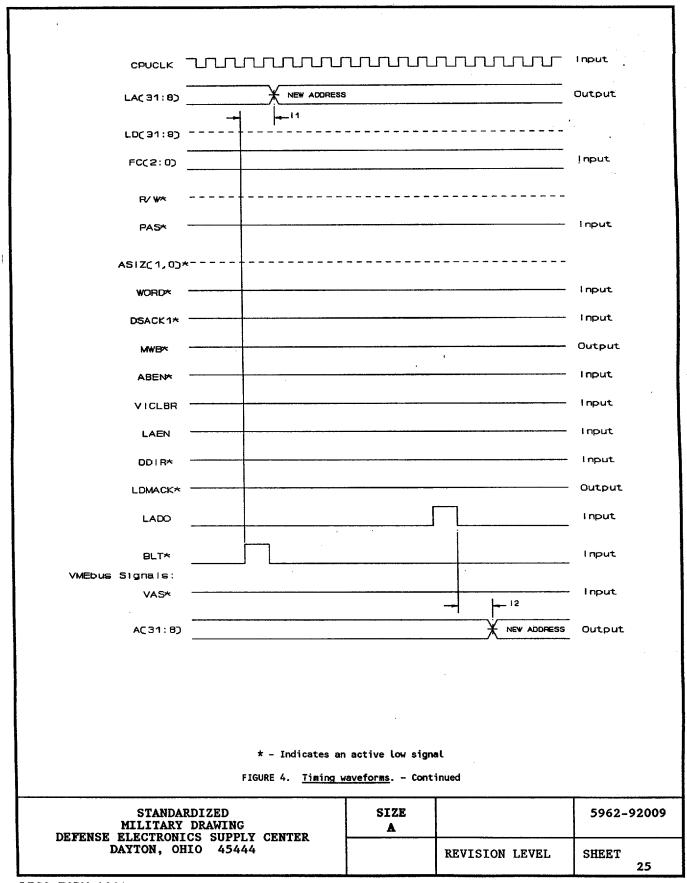
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4. QUALITY ASSURANCE PROVISIONS

- 4.1 <u>Sampling and inspection</u>. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.
- 4.2 <u>Screening</u>. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition C or D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device classes B and S, the test circuit shall be submitted to the qualifying activity. For device classes M, B, and S, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.
 - (2) $T_A = +125$ °C, minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein.
- 4.2.2 Additional criteria for device classes Q and V.
 - a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.
 - b. Interim and final electrical test parameters shall be as specified in table II herein.
 - c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.
- 4.3 Qualification inspection.
- 4.3.1 <u>Qualification inspection for device classes B and S.</u> Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).
- 4.3.2 <u>Qualification inspection for device classes Q and V.</u> Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).
- 4.4 <u>Conformance inspection</u>. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

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- b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes B and S, subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).
- c. Subgroup 4(C_{IN} and C_{OUT}) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

TABLE II. <u>Electrical test requirements</u>.

Test requirements		Subgroups Mance with MI MI 5005, table	Subgroups (in accordance with MIL-I-38535, table III)		
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)			1, 7		1, 7
Final electrical parameters (see 4.2)	1/ 1,2,3,7 8,9,10,11	1/ 1,2,3,7 8,9,10,11	2/ 1,2,3,7 8,9,10,11	1/ 1,2,3,7 8,9,10,11	2/ 1,2,3,7 8,9,10,11
Group A test requirements (see 4.4)	1,2,3,4, 7,8,9,10 11	1,2,3,4, 7,8,9,10	1,2,3,4, 7,8,9,10 11	 1,2,3,4, 7,8,9,10 11	1,2,3,4, 7,8,9,10
Group B end-point electrical parameters (see 4.4)			2,8a,10		
Group C end-point electrical parameters (see 4.4)	2,8a,10	2,8a,10		2,8a,10	2,8a,10
Group D end-point electrical parameters (see 4.4)	2,8a,10	2,8a,10	2,8a,10	2,8a,10	2,8a,10
Group E end-point electrical parameters (see 4.4)	2,8a,10	2,8a,10	2,8a,10	2,8a,10	2,8a,10

^{1/} PDA applies to subgroup 1.

4.4.2 <u>Group B inspection.</u> The group B inspection end-point electrical parameters shall be as specified in table II herein. For device class S steady-state life tests, the test circuit shall be submitted to the qualifying activity.

4.4.3 <u>Group C inspection</u>. The group C inspection end-point electrical parameters shall be as specified in table II herein.

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 $[\]frac{2}{2}$ / PDA applies to subgroups 1 and 7.

- 4.4.3.1 Additional criteria for device classes M and B. Steady-state life test conditions, method 1005 of MIL-STD-883:
 - a. Test condition C or D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class B, the test circuit shall be submitted to the qualifying activity. For device classes M and B, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.
 - b. $T_A = +125$ °C, minimum.
 - c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.
- 4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.
- 4.4.4 <u>Group D inspection</u>. The group D inspection end-point electrical parameters shall be as specified in table II herein.
- 4.4.5 <u>Group E inspection</u>. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D.
 - a. End-point electrical parameters shall be as specified in table II herein.
 - b. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25\,^{\circ}\text{C} \pm 5\,^{\circ}\text{C}$, after exposure, to the subgroups specified in table II herein.
 - c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.
 - PACKAGING
- 5.1 <u>Packaging requirements</u>. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.
 - 6. NOTES
- 6.1 <u>Intended use</u>. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.
- 6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.
- 6.1.2 <u>Substitutability</u>. Device classes B and Q devices will replace device class M devices.
- 6.2 <u>Configuration control of SMD's</u>. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).
- 6.3 <u>Record of users</u>. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.
- 6.4 <u>Comments</u>. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

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6.5 <u>Abbreviations, symbols, and definitions</u>. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331 and Table III.

Table III. Pin descriptions.

Symbol	Name and function				
A[31:8]	The VMEbus address signals are three-state input/outputs.				
AS	The VMEbus address strobe signal is an input signal that responds to both 5962-92010 and VMEbus generated address strobes.				
ID[15:8]	The VMEbus isolated data bus signals are three-state input/outputs used to interface local data [15:8] to the VMEbus D [15:8] in conjunction with transparent latching bidirectional I/O buffers. They also are used to interface with local 8-bit I/O peripherals via the Device Location and DSACKi Control registers.				
LD[31:16]	The local data bus signals are three-state input/outputs used to write or read the local data bus and for writing and reading the on-chip control registers. Note: The IDbus connects to LD[15:8] and 5962-92010 connects to LD[7:0].				
LA[31:8]	The local address bus signals are three-state input/outputs used as inputs during a VMEbus master cycle and to access on-chip control registers. They are used for output during local or slave accesses.				
PAS	The local-processor address strobe is an input that indicates to the the device that a valid address is present on the address bus. This signal is typically driven by either 5962-92010 or the local processor.				
R/W	The local read/write signal is an input. When high, the signal indicates that the current cycle is a read. When low, the current cycle is a write. This signal is typically driven by either the 5962-92010 or the local processor.				
RESET	Reset is an input signal for the 5962-92010 . It is used alone or in conjunction with WORD to reset the device internal registers. There are two reset types that may be implemented, and both of them are discussed in the reset section.				
WORD	This signal is both and input and three-state input/output and is active under programmable control from the appropriate region attribute register and controls the length of the data field. When it is asserted, the data path is 16 bits wide. When deasserted, a 32-bit data path is set. It is also used as an input in conjunction with RESET to set the device registers. It is typically connected to the 5962-92010 as an output.				
ASIZ1, ASIZO	These are the address size signals and are three-state input/outputs. They are used to specify the address size of an access. They are active under programmable control from the appropriate region attribute register. These signals are typically driven to the 5962-92010 along with WORD to determine address and data path size.				
	ASIZO ASIZ1 Addressing Mode 0 0 User-defined 0 1 A32 1 0 A16 1 1 A24				
DSACK1/O	These are the data sizing acknowledge signals and are rescinding three-state input/outputs. They are generated for any of the device select outputs except CS and VSBSEL accesses. DSACKO or DSACK1 can be selectively disabled or enabled in the DSACK1 Control register.				

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Table III. Pin descriptions. - Continued

Symbol	Name and function			
FC2/0	These are the function code input signals. They are used by the device to determine the local access type and are typically driven by the local processor or the 5962-92010 as shown in the following tables:			
	FC2 FC1 FC0 Cycle 0 0 1 User data space 0 1 0 Supervisor data space 1 1 0 Supervisor program space 1 1 1 CPU space			
	FC2 FC1 Cycle 0 0 Slave block transfer 0 1 Local DMA 1 0 Slave Access 1 1 DRAM refresh			
MWB	This is the module-wants-bus output signal. It is asserted under programmable control of the appropriate region attribute register and indicates that a VMEbus assess is occurring. This signal is typically connected to the 5962-92010.			
FCIACK	This is the local interrupt output signal. It indicates that the current cycle is an interrupt acknowledge cycle. This signal is typically connected to the 5962-92010. It is asserted during local the device interrupt cycles, or when HIACKEN is enabled in the PIO Direction register or when IOSEL5 address space is accessed when enabled in the PIO Function register.			
DRAMCS	This is the DRAM chip select output signal. It is asserted when the local address maps into region O as defined by the DRAM Upper Limit Address register. It is also asserted when redirection is enabled in the device Decode Control register.			
EPROMCS	This is the EPROM chip select output signal. It is asserted after a global reset, during a local access to EPROM address space, and during redirection of SLSEL1 on the local bus via the device Decode register.			
FPUCS	This is the floating-point-unit chip select output signal. It is asserted when a floating-point coprocessor access is occurring. This is decoded from the processor function codes or under programmable control i the PIO Function register to be asserted in the IOSEL4 address range.			
VSBSEL	This is the VSB (VME Subsystem Bus) select output signal. It is used to identify accesses to a daughterboard of VSB. It is asserted when enabled from the appropriate region attribute register.			
REFGT	This is the refresh grant output signal. It is asserted during a DRAM refresh cycle and is typically decoded from the 5962-92010 function codes (FC1 and FC2).			
LBR	This is the 5962-92010 local bus request input signal. It is used to signal the device when the 5962-92010 requests the local bus. It is typically connected to the 5962-92010 LBR signal.			
cs	This is the 5962-92010 chip select input signal. It is asserted when the fixed address of the 5962-92010 is present on the local address bus. This signal is typically connected to the 5962-92010 chip select signal (CS).			
BLT	This is the block transfer input signal. It is used to determine when a block transfer is in progress and to increment internal address counters during a boundary crossing. This signal is typically connected to the 5962-92010.			

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Table III. Pin descriptions. - Continued

Symbol	Name and function
CACHINH	This is the cache inhibit signal and is an open collector output. It is asserted when enabled in either the Region Attribute registers or in the A24 Space Base Address register. It is also asserted on access to the DRAM Mailbox and VMEbus A16 address space (Region 6). It may be connected to the CDIS signal on 680XO-type processors.
LDMACK	This is the local DMA activity output signal. It is asserted when there is DMA activity mapped into a particular region. It is typically decoded from the 5962-92010 function codes (FC1 and FC2).
CPUCLK	This is the CPU clock input signal. It is typically connected to the system CPU clock. Maximum frequency is 50 MHz.
SLSELO	This is the slave select 0 output signal. It is asserted when enabled by a comparison of its base address register and the address on the VMEbus. It indicates to the 5962-92010 that a slave operation is pending.
SLSEL1	This is the slave select 1 output signal. It is asserted when enabled by a comparison of its base address register and the address on the VMEbus. It indicates to the 5962-92010 that a slave operation is pending.
ICFSEL	This is the interprocessor communications output signal. It is asserted under programmable control of a comparison of its base address register and the address on the VMEbus. it indicates a 5962-92010 interprocessor communication access.
IOSEL1/0	These are 2 of the 6 I/O select output signals. They are asserted when the local bus address matches their fixed memory location. They are also used in conjunction with the IDbus when programmed in the PIO Function register.
PIOO- TXDA	The PIOO-TXDA signal is programmed to serve either as general-purpose I/O pin bit O, or as an output for the UART channel-A transmit signal.
PIO1- RXDA	The PIO1-RXDA signal is programmed to serve as either general-purpose I/O pin bit 1, or as an input for the UART channel-A receiver signal.
PIO2- TXDB	The PIO2-TXDB signal is programmed to serve as either general-purpose I/O pin bit 2, or as an output for the UART channel-B transmit signal.
PIO3- RXDB	The PIO3-RXDB signal is programmed to serve as either general-purpose I/O pin bit 3, or as an input for the UART channel-B receiver signal.
PIO4- IORD	The PIO4-IORD signal is programmed to serve as either general-purpose I/O pin bit 4, or as an output for the read enable signal (local I/O accesses).
PIO5- IOWR	The PIO5-IOWR signal is programmed to serve as either general-purpose I/O pin bit 5, or as an output for the write enable signal (local I/O accesses).
PI06- IOSEL3	The PIO6-IOSEL3 signal is programmed to serve as either general-purpose I/O pin bit 6, or as an output for the IOSEL3 enable signal (local fixed-map I/O select).
PIO7- Interrupt Request	The PIO7-Interrupt Request signal is used as either general-purpose I/O pin bit 7, or as a output for interrupt requests on one of PIO 7, 10, or 11 (programmed in the Interrupt Control register).
PIO8- IOSEL4	The PIO8-IOSEL4 signal is programmed to serve as either general-purpose I/O pin bit 8, or as an output for the IOSEL4 enable signal (local fixed-map I/O select). IOSEL4 accesses also assert FPUCS when so programmed in the PIO Function register.
PIO9- IOSEL5	The PIO9-IOSEL5 signal is programmed to serve as either general-purpose I/O pin bit 9, or as an output for the IOSEL5 enable signal (local fixed-map I/O select). IOSEL5 accesses also assert FCIACK when so programmed in the PIO Function register.

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Table III. Pin descriptions. - Continued

Symbol	Name and function
PIO10- INTERRUPT REQUEST	The PIO10-Interrupt Request signal is used as either general-purpose I/O pin bit 10, or as a programmed interrupt request as programmed Interrupt Control register.
PIO11- INTERRUPT REQUEST	The PIO11-Interrupt Request signal is used as either general-purpose I/O pin bit 11, or as an output for interrupt requests as programmed in the Interrupt Control register.
PIO12- SHRCS	The PIO12-SHRCS signal is programmed to serve as either general-purpose I/O pin bit 12, or as an output for shared resource chip select.
PIO13- IOSEL2	The PIO13-IOSEL2 signal is programmed to serve as either general-purpose I/O pin bit 13, or as an output for the IOSEL2 enable signal (local fixed-map I/O select).
SWDEN	The swap data enable signal is an input used in conjunction with DDIR to swap data to or from the Isolated Data bus signals ID[15:8] to the Local Data LD[15:8] bus. This signal is typically connected to the 5962-92010.
DDIR	The data direction signal is an input typically connected to the 5962-92010.
LADO	The latch address out signal is an input used to latch the local address out to the VMEbus. It is typically connected to the 5962-92010. LADO is also used to increment internal address counters during a VMEbus boundary crossing.
LADI	The latch address in signal is an input used to latch the local address from the VMEbus.
LAEN	The local address bus enable signal is an input used by the device to indicate that the 5962-92010 has bus mastership of the local bus.
ABEN	The VMEbus address enable signal is an input used to indicate that the 5962-92010 is driving the VMEbus address bus.

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6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document <u>listing</u>
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or \$)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML~38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

- 6.7.1 <u>Sources of supply for device classes B and S</u>. Sources of supply for device classes B and S are listed in QPL-38510.
- 6.7.2 <u>Sources of supply for device classes Q and V</u>. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.
- 6.7.3 <u>Approved sources of supply for device class M</u>. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

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