REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Technical and editorial changes throughout. -LTG.	98-06-30	M. L. Poelking

REV																				
SHEET																				
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	

REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A		A	A	
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Thomas M. Hess

CHECKED BY
Thomas M. Hess

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
97-12-01

REVISION LEVEL
A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

MICROCIRCUIT, DIGITAL, RADIATION HARDENED, 1750 CHIP SET, MULTICHIP MICROCIRCUIT, SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-96847**

SHEET 1 OF 33

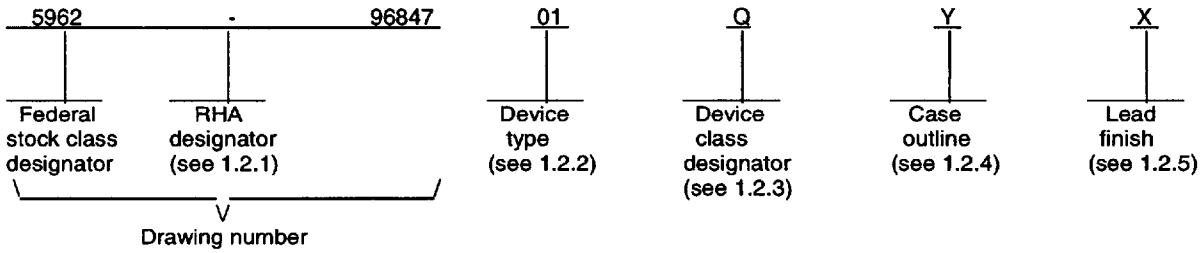
DSCC FORM 2233
APR 97

5962-E321-98

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Minimum Operating Period
01	RX1750	Microprocessor, multichip module	50 ns
02	RX1750	Microprocessor, multichip module	55 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Y	See figure 1	200	Quad flat package 1/

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ The lid for this outline is Nickle plated Kovar, No gold is used on the lid.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{DD})	-0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to V_{DD} + 0.5 V dc
DC output voltage range (V_{OUT})	-0.5 V dc to V_{DD} + 0.5 V dc
DC input current (I_{IN}) 3/	±50 mA
DC output current (I_{OUT}) 4/	±50 mA
Power dissipation,(f = 20 Mhz) (P_D)	2.5 W (peak)
Lead temperature (soldering, 5 seconds)	+270°C
Maximum junction temperature (T_J)	+175°C
Thermal resistance, junction-to-case (θ_{JC})	≤ 1.0°C/W
ESD	Class 1 (1000 V)
Storage temperature range	-65°C to +150°C

1.4 Recommended operating conditions.

Supply voltage range (V_{DD})	4.5 V dc to 5.5 V dc
DC input voltage range (V_{IN})	-0.3 V dc to V_{DD} + 0.3 V dc
DC output voltage range (V_{OUT})	-0.3 V dc to V_{DD} + 0.3 V dc
DC input current (I_{IN}) 3/	±10 mA
DC output current (I_{OUT}) 4/	±12 mA
Capacitive output load (C_L) 5/	50 pF
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	98 percent 2/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.
MIL-STD-1750A - 16 Bit Computer Instruction Set Architecture.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ All voltages are with respect to V_{SS} terminal and T_C = -55°C to +125°C, unless otherwise specified.
3/ High impedance (input or output in three-state), driver or receiver type = input, output, or bidirectional.
4/ Low impedance (enabled), driver or receiver type = output or bidirectional.
5/ f = 20 MHz, no dc load, driver or receiver type = output or bidirectional 12 mA, maximum capacitance scales with inverse of frequency, V_{DD} = 4.5 V dc.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Switching test circuit and waveforms. The switching test circuit and waveforms shall be as specified on figure 4.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as specified on figure 5.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Units
					Min	Max	
High level input threshold voltage 3/ Pin groups CMOS in 4/	V_{IH}	$V_{DD} = 5.5\ V$	1, 2, 3	All		3.85	V
Low level input threshold voltage 3/ Pin groups CMOS in 4/	V_{IL}	$V_{DD} = 4.5\ V$	1, 2, 3	All	1.35		V
Quiescent supply current	I_{DDSB}	$V_{DD} = 5.5\ V$, $f_C = 0\ Hz$	1, 2, 3	All		100	mA
Operating supply current	I_{DD}	$V_{DD} = 5.5\ V$, $f_C = 16.6\ MHz$	1, 2, 3	01, 02		300	mA
High level input current, pin gropus INHI 5/	I_{IH}	$V_{DD} = 5.5\ V$, $V_{IH} = V_{DD}$	1, 2, 3	All	-10	10	μA
High level input current Pin groups ALLINPD 6/	I_{IH2}	$V_{DD} = 5.5\ V$, $V_{IH} = V_{DD}$	1, 2, 3	All	50	550	μA
High level input current Pin groups ALLINMPD 7/	I_{IH3}	$V_{DD} = 5.5\ V$, $V_{IH} = V_{DD}$	1, 2, 3	All	.050	1.5	mA
Low level input current Pin groups INLW 8/	I_{IL}	$V_{DD} = 5.5\ V$, $V_{IL} = V_{SS}$	1, 2, 3	All	-10	10	μA
Low level input current Pin groups ALLINPU 9/	I_{IL1}	$V_{DD} = 5.5\ V$, $V_{IL} = V_{SS}$	1, 2, 3	All	-550	-50	μA
Low level input current Pin groups ALLINMPU 10/	I_{IL2}	$V_{DD} = 5.5\ V$, $V_{IL} = V_{SS}$	1, 2, 3	All	-1.5	-.050	mA
High level output voltage 19/ Pin groups ALL12 11/	V_{OH}	$V_{DD} = 4.5\ V$, $I_{OH} = -12\ mA$	1, 2, 3	All	4.0		V
Low level output voltage 19/ Pin groups ALL12 11/	V_{OL}	$V_{DD} = 4.5\ V$, $I_{OL} = 12\ mA$	1, 2, 3	All		0.5	V
High level output current 19/ Pin groups ALL12 11/	I_{OH}	$V_{DD} = 4.5\ V$, $V_{OH} = 4\ V$	1, 2, 3	All		-12	mA

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Units
					Min	Max	
Low level output current Pin grooups ALL12 11/	I_{OL}	$V_{DD} = 4.5\ V$, $V_{OH} = 0.5\ V$	1, 2, 3	All	12		mA
Three-state high level output leakage current Pin gropus TRIBIHI 12/	I_{OZH}	$V_{DD} = 5.5\ V$, $V_{OH} = 5.5\ V$	1, 2, 3	All		18	μA
Three-state low level output leakage current Pin groups TRIBILW 12/	I_{OZL}	$V_{DD} = 5.5\ V$, $V_{OL} = 0.0\ V$	1, 2, 3	All	-18		μA
Three-state high level output leakage current Pin groups TRIBIPU 14/	I_{OZL1}	$V_{DD} = 5.5\ V$, $V_{OL} = 0.0\ V$	1, 2, 3	All	-550	-50	μA
three-state high level output leakage current Pin groups TRIBIODPU 15/	I_{OZL2}	$V_{DD} = 5.5\ V$, $V_{OL} = 0.0\ V$	1, 2, 3	All	-1.5	-.050	μA
High level output ground bounce voltage 16/	V_{GBH}	$V_{IL} = 0.0\ V$, $V_{IH} = V_{DD}$	1, 2, 3	All		0.1	V
Low level output ground bounce voltage 16/	V_{GBL}	$V_{IL} = 0.0\ V$, $V_{IH} = V_{DD}$	1, 2, 3	All		0.3	V
Input capacitance 16/	C_{IN}	$V_{IN} = 0\ V$, $f = 1.0\ MHz$, see 4.5.1c	4, 5, 6	All		9	pF
Output capacitance 16/	C_{OUT}	$V_{OUT} = 0\ V$, $f = 1.0\ MHz$, see 4.5.1c	4, 5, 6	All		14	pF
Functional test per approved vector set 17/		$V_{IL} = 0.0\ V$, $V_{IH} = V_{DD}$, see 4.5.1b	7, 8A, 8B	All			pass
Minimum operating period	t_{MIN}		9, 10, 11	1		50	ns
				2		55	
Output rise and fall times 16/ 18/ 20/	t_{ro}, t_{fo}	$C_L = 60\ pF$	9, 10, 11	All		2.5	ns

TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Units
					Min	Max	
Propagation delay time, HCLK to PIO	t_{PHL3}, t_{PLH3}	$V_{IL} = 0.0\ V$, $V_{IH} = V_{DD}$, see figure 4	9, 10, 11	All	6	36	ns
Propagation delay time, HCLK to DOUTENA	t_{PLH4}, t_{PHL4}		9, 10, 11	All	5	33	ns
Propagation delay time, HCLK to CPUPARITY	t_{PLH6}, t_{PHL6}		9, 10, 11	All	10.8	43	ns
Propagation delay time, HCLK to CPUWDATAn	t_{PLH9}, t_{PHL9}		9, 10, 11	All	8.4	32.9	ns
Propagation delay time, HCLK to WRITE	t_{PLH10}, t_{PHL10}		9, 10, 11	All	7	48	ns
Propagation delay time, HCLK to SIOE	t_{PLH12}		9, 10, 11	All	9	42	ns
	t_{PHL12}		9, 10, 11	All	10	40	ns
Propagation delay time, HCLK to READ	t_{PLH13}, t_{PHL13}		9, 10, 11	All	7	36.5	ns
					7	36	
Propagation delay time, HCLK to LINSTF	t_{PLH15}, t_{PHL15}		9, 10, 11	All	9.5	37.7	ns
Propagation delay time, HCLK to LRMW	t_{PLH17}, t_{PHL17}		9, 10, 11	All	7.0	30	ns
Propagation delay time, HCLK to CPUADDRn	t_{PLH18}, t_{PHL18}		9, 10, 11	All	8.8	33	ns
Propagation delay time, HCLK to SYSCLKD	t_{PLH19}, t_{PHL19}		9, 10, 11	All	5.5	29	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Units
					Min	Max	
Propagation delay time, HCLK to DMAGRNT	t_{PLH21}, t_{PHL21}	$V_{IL} = 0.0\ V$, $V_{IH} = V_{DD}$, see figure 4	9, 10, 11	All	5.0	37.2	ns
Propagation delay time, CPUDATA(0:15) to SCPE02	t_{PLH23}		9, 10, 11	All	4.0	90	ns
Propagation delay time, CPUDATA (0:19) to SCPE03	t_{PLH24}		9, 10, 11	All	5.0	90	ns
Propagation delay time, HCLK to BNK0	t_{PLH25}, t_{PHL25}		9, 10, 11	All	9.1	32.6	ns
Propagation delay time, HCLK to BNK1	t_{PLH26}, t_{PHL26}		9, 10, 11	All	9.1	32.6	ns
Propagation delay time, HCLK to BNK2	t_{PLH27}, t_{PHL27}		9, 10, 11	All	9.1	32.6	ns
Propagation delay time, BNK(0:2) to SCPE03	t_{PLH28}		9, 10, 11	All	5.0	90	ns
Setup time, HCLK to READDATA	t_{su5}		9, 10, 11	All		5.0	ns
Setup time, HCLK to LACKN	t_{su6}		9, 10, 11	All		14	ns
Setup time, HCLK to READDATAP1	t_{su7}		9, 10, 11	All		1.0	ns
Setup time, HCLK to READDATAP2	t_{su8}		9, 10, 11	All		1.0	ns
Setup time, HCLK to DMARQST	t_{su20}		9, 10, 11	All		0	ns
Hold time, HCLK to READDATA	t_{h5}		9, 10, 11	All		13	ns
Hold time, HCLK to LACKN	t_{h6}		9, 10, 11	All		9.0	ns
Hold time, HCLK to READDATAP1	t_{h7}		9, 10, 11	All		13	ns
Hold time, HCLK to READDATAP2	t_{h8}		9, 10, 11	All		13	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Units
					Min	Max	
Output enable time, CPU3MEN to CPUADDRn	t_{PLZ1}	$V_{IL} = 0.0\ V$, $V_{IH} = V_{DD}$, see figure 4	9, 10, 11	All	0	21	ns
Output disable time, CPU3MEN to CPUADDR	t_{PZL1}		9, 10, 11	All	0	21	ns
Output enable time, CPU2MEN to CPUWDATAn	t_{PLZ2}, t_{PHZ2}		9, 10, 11	All	0	15	ns
Output disable time, CPU2MEN to CPUWDATAn	t_{PZL2}, t_{PZH2}		9, 10, 11	All	0	15	ns
Output enable time, CPU2MEN to CPUPARITY	t_{PLZ3}, t_{PHZ3}		9, 10, 11	All	0	15	ns
Output disable time, CPU2MEN to CPUPARITY	t_{PZL3}, t_{PZH3}		9, 10, 11	All	0	15	ns

1/ Devices supplied to this drawing have been characterized through all levels M, D, L, R, F, G, and H of irradiation. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, $T_A = +25°C$.
2/ Vector sets for all group A tests shall be specified in the test program maintained by the manufacturer.
3/ This test is not required for VCP test bus pins, V_{IH}, V_{IL}, and BIPU12, TRIPU12 Pin groups.
4/ CMOSIN pin group is derived from all buffer types with a CMOS input. This included: IN, INPU, INPD, BIPU12, TRIBU12, INMPU.
5/ INHI pin group is derived from the following buffer types: IN, INPU.
6/ ALLINPD pin group is derived from the following buffer types: INPD.
7/ ALLINMPD pin group is derived from the following buffer types: INMPD, (Pin 192 NFTSE)
8/ INLW pin group is derived from the following buffer types: IN, INPD.
9/ ALLINPU pin group is derived from the following buffer types: INPU.
10/ ALLINMPU pin group is derived from the following buffer types: INMPU, (PIN 184 NFTRN, PIN 52 SELECTN).
11/ ALL12 pin group is derived from all buffer types that have 12 mA drive capability. This includes: OUT12, TRIPU12, BIPU12.
12/ TRIBIHI pin group is derived from the following buffer types: TRIPU12, BIPU12.
13/ TRIBILW pin group is derived from the following buffer types: OUTOD12,(PIN 187 VCPACKN).
14/ TRIBIPU pin group is derived from the following buffer types: TRIPU12, BIPU12.
15/ TRIBIODPU pin group is derived from the following buffer types: OUTODP12 (PIN 169 TINTREQN).
16/ If not tested, shall be guaranteed to the limits specified in table IA.
17/ Conditions for the use of functional test vectors are specified.
18/ Input rise and fall times (t_{rf} and t_{fl}) shall not exceed 5.0 ns between the 10% and 90% points as referenced to the V_{IH} and V_{IL} difference.
19/ Test not required for open drain output pin TINTREQn pin number 169.
20/ Measured between 1.0 V from rail to midpoint.

TABLE IB. SEP test limits by storage cell and chip set. (All device types) 1/ 2/ 3/

Storage cell type 4/	Effective LET (no upsets) [MeV/(cm²/mg)]	Maximum cell cross section (LET = 120) σ (cm²)	Maximum chip cross section (LET = 120) σ (cm²)
Chip set total	≥20		4.54E-03

1/ For SEP test conditions, see 4.5.4.4 herein.
2/ T_A = +125°C, worst case conditions.
3/ The MCM chipset is comprised of ten different memory cell types, many with unique SEP characteristics; consequently the chipset SEP response is not adequately defined by a single SEP LET threshold and saturation cross-section. The Government has conducted SEP tests of these chips with assistance from the manufacturer to determine the SEP responses of the chipset and its various storage cell types. Based on this test data, the chipset SEP rate calculated from the SEP cell data for a typical space environment (the 90% worst-case environment in a geosynchronous equatorial orbit) is 3E-5 upsets/chipset-day.
4/ Individual storage cell types versus chip type calculations have not been made for this device. Representative values are available in 5962-94667.

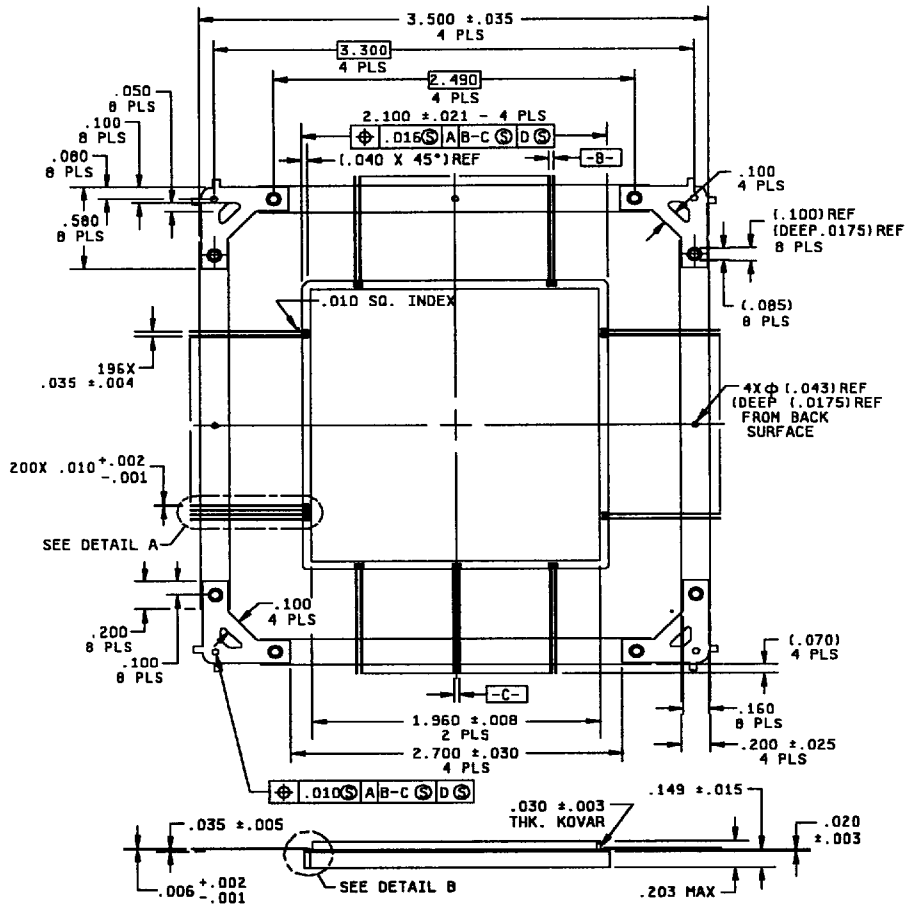


FIGURE 1. Case outline.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE **A**		**5962-96847**
		REVISION LEVEL A	SHEET **12**

DSCC FORM 2233
APR 97

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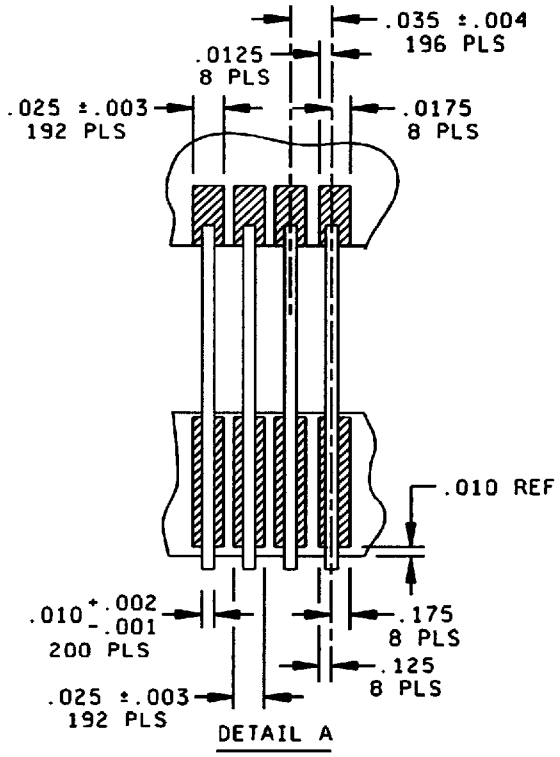


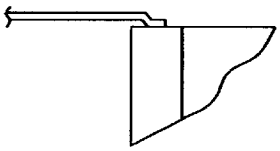


FIGURE 1. Case outline. - Continued

Device type	All		Device type	All	
Case outline	Y		Case outline	Y	
Terminal number	Signal name	Signal type 1/	Terminal number	Signal name	Signal type 1/
1	VCP1	BI	51	CLKA	OUT
2	VCP5	BI	52	SELECTN	IN
3	VCP3	BI	53	INT11N	IN
4	MODEFPP2	IN	54	WRITE	OUT
5	LINSTF	TRI	55	INT12N	IN
6	CPUADDR16	TRI	56	INT10N	IN
7	NFTSFPP2	IN	57	INT08N	IN
8	NFTDOUTN	OUT	58	INT13N	IN
9	MODEFPP1	IN	59	INT14N	IN
10	VCP6	BI	60	INT15N	IN
11	NFTDI	IN	61	INT02N	IN
12	VCP0	BI	62	PWRDWN	IN
13	VCP2	BI	63	CPUWDATA6	TRI
14	VCP4	BI	64	CPUWDATA5	TRI
15	MMUSEL	IN	65	CPUWDATA0	TRI
16	TMRCLK	IN	66	CPUWDATA1	TRI
17	VCP7	BI	67	INT01N	OUT
18	VDD	+POWER	68	VDD	+POWER
19	MRSTN	IN	69	CPUWDATA4	TRI
20	VDD	+POWER	70	VDD	+POWER
21	READDATA31	IN	71	CPUWDATA2	TRI
22	VDD	+POWER	72	VDD	+POWER
23	INTREQN	OUT	73	NFTSCPU2	IN
24	VDD	+POWER	74	VSS	-POWER
25	CPUADDR8	TRI	75	MODECPU2	IN
26	VSS	-POWER	76	VSS	-POWER
27	CPUADDR7	TRI	77	ALUFLTO	OUT
28	VSS	-POWER	78	VSS	-POWER
29	CPUADDR15	TRI	79	CPUPARITY	TRI
30	VSS	-POWER	80	VSS	-POWER
31	CPUADDR11	TRI	81	CPUWDATA7	TRI
32	CPUADDR17	TRI	82	CPUWDATA9	TRI
33	CPUADDR12	TRI	83	CPUWDATA8	TRI
34	CPUADDR14	TRI	84	READDATA29	IN
35	CPUADDR9	TRI	85	CPUWDATA3	TRI
36	CPUADDR19	TRI	86	CPUWDATA10	TRI
37	CPUADDR10	TRI	87	CPUWDATA11	TRI
38	CPUADDR18	TRI	88	CPUWDATA12	TRI
39	CPUADDR13	TRI	89	CPUWDATA14	TRI
40	CPUADDR4	TRI	90	CPUWDATA13	TRI
41	ASFLTO	OUT	91	CPU2MEN	IN
42	MMUWRTO	OUT	92	SCPE02	OUT
43	PROTFLT346	IN	93	READDATA25	IN
44	READ	OUT	94	CPUWDATA15	TRI
45	DMAGRNT	OUT	95	SCP2A	IN
46	SIOE	OUT	96	SCP2B	IN
47	NFTSCPU3	IN	97	SCP1B	IN
48	MODECPU3	IN	98	SCP1A	IN
49	SCPE03	OUT	99	VCPBPT	OUT
50	CPU3MEN	IN	100	DI4	IN

See footnotes at end of table.

FIGURE 2. Terminal connections.

Device type	All		Device type	All	
Case outline	Y		Case outline	Y	
Terminal number	Signal name	Signal type 1/	Terminal number	Signal name	Signal type 1/
101	DI3	IN	151	PARFLTI	IN
102	DI7	IN	152	ILLIOX	IN
103	DI5	IN	153	READDATA4	IN
104	DI6	IN	154	DMARQST	IN
105	DI2	IN	155	READDATA19	IN
106	DI1	IN	156	READDATA17	IN
107	DI0	IN	157	READDATA18	IN
108	READDATA30	IN	158	READDATA24	IN
109	VCPSELN	IN	159	READDATA22	IN
110	DOR5	OUT	160	READDATA23	IN
111	VCPRDE	IN	161	READDATA26	IN
112	DOR6	OUT	162	TSTCLK	IN
113	DOR7	OUT	163	CPUADDR3	TRI
114	DOR4	OUT	164	DMAMPF	IN
115	DOR1	OUT	165	DMACPF	IN
116	DOR0	OUT	166	ASFLTI	IN
117	DOR3	OUT	167	CLKOUT	OUT
118	VDD	+POWER	168	VDD	+POWER
119	DOR2	OUT	169	TINTREQN	ODOUT
120	VDD	+POWER	170	VDD	+POWER
121	ALUFLTI	IN	171	BNK0	TRI
122	VDD	+POWER	172	VDD	+POWER
123	DOUTENA	OUT	173	NFTSFPP1	IN
124	VDD	+POWER	174	VSS	-POWER
125	READDATA21	IN	175	BNK2	TRI
126	VSS	-POWER	176	VSS	-POWER
127	READDATA16	IN	177	HCLK	CLKIN
128	VSS	-POWER	178	VSS	-POWER
129	READDATA28	IN	179	PIO	OUT
130	VSS	-POWER	180	VSS	-POWER
131	READDATA27	IN	181	EXPMEM	IN
132	VSS	-POWER	182	MMUWRTI	IN
133	READDATA20	IN	183	CPUADDR1	TRI
134	READDATA12	IN	184	NFTRN	IN
135	READDATA13	IN	185	MODECPU1	IN
136	READDATA15	IN	186	READDATAP2	IN
137	READDATA14	IN	187	VCPACKN	ODOUT
138	READDATA11	IN	188	CONSOLEN	IN
139	READDATA10	IN	189	CPUADDR5	TRI
140	READDATA9	IN	190	LACKN	IN
141	READDATA8	IN	191	MEMTIMEN	OUT
142	PARFLTO	OUT	192	NFTSE	IN
143	READDATA0	IN	193	SYSCLKD	OUT
144	READDATA7	IN	194	BNK1	TRI
145	READDATA2	IN	195	LRMW	TRI
146	READDATA3	IN	196	CPUADDR0	TRI
147	READDATA5	IN	197	CPUADDR2	TRI
148	READDATA6	IN	198	READDATAP1	IN
149	FPPPRESN	IN	199	CPUADDR6	TRI
150	READDATA1	IN	200	NFTSCPU1	IN

1/ BI - Bidirectional (input/output)
IN - Input
OUT - Output
CLK - System clock
OD - Open drain
TRI - Three-state output

FIGURE 2. Terminal connections - continued.

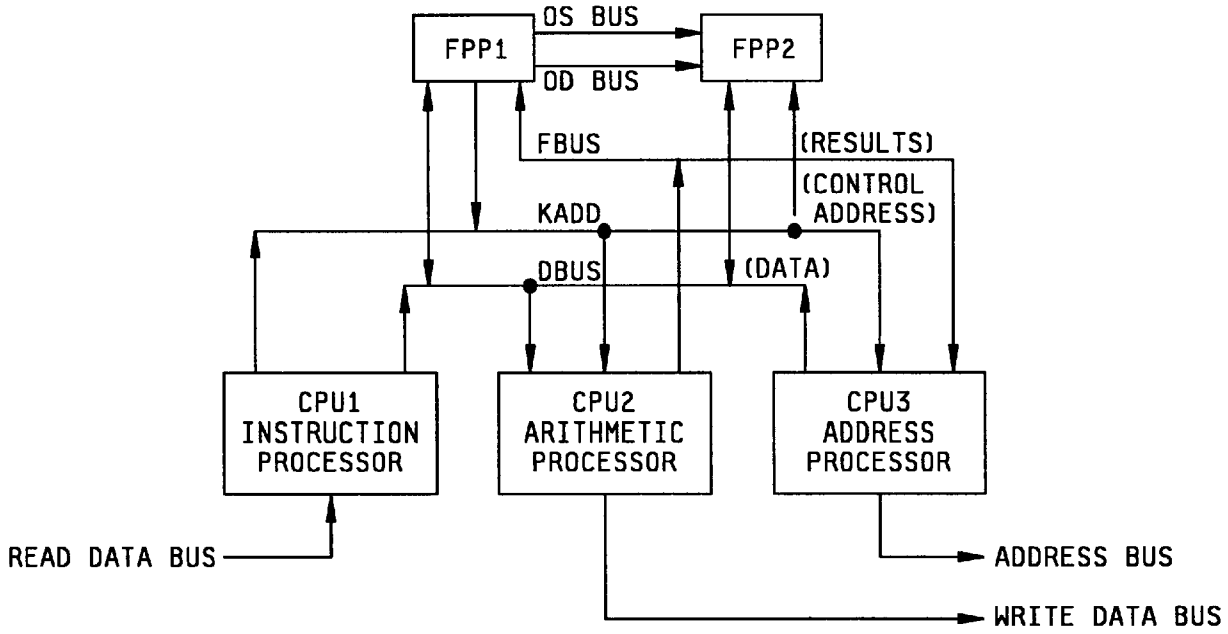
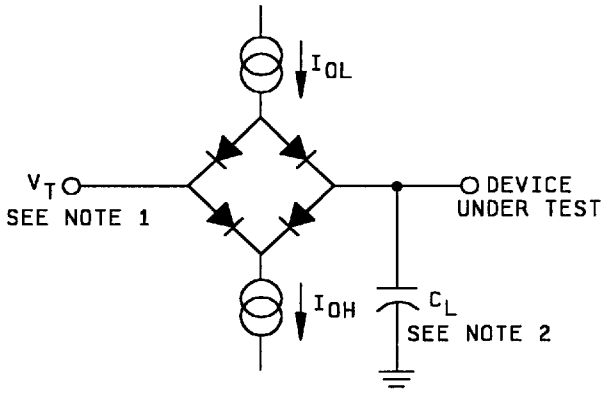


FIGURE 3. Block diagram.



Notes:

1. VT is a variable dependant upon the test parameter.
2. Load capacitance (C_L) includes jig and probe capacitance. For bidirectional output pins, C_L = 115 pF; for all other outputs, C_L = 85 pF.

FIGURE 4. Switching test circuit and waveforms.

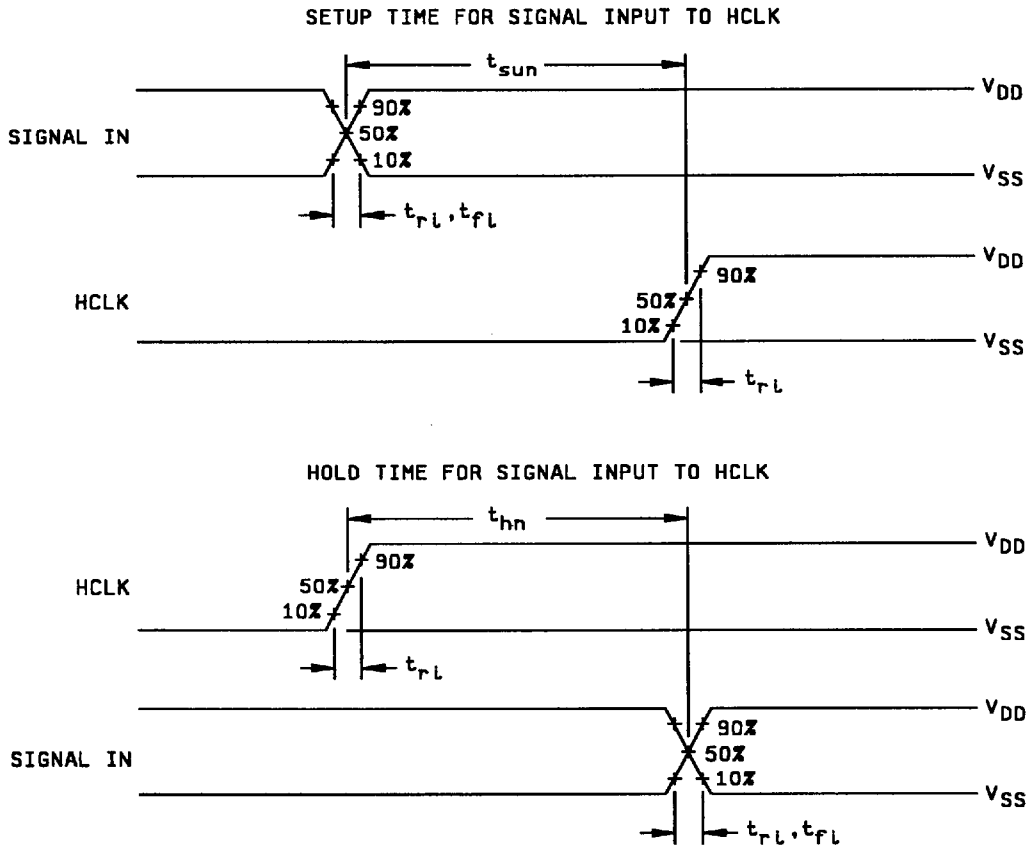


FIGURE 4. Switching test circuit and waveforms - continued.

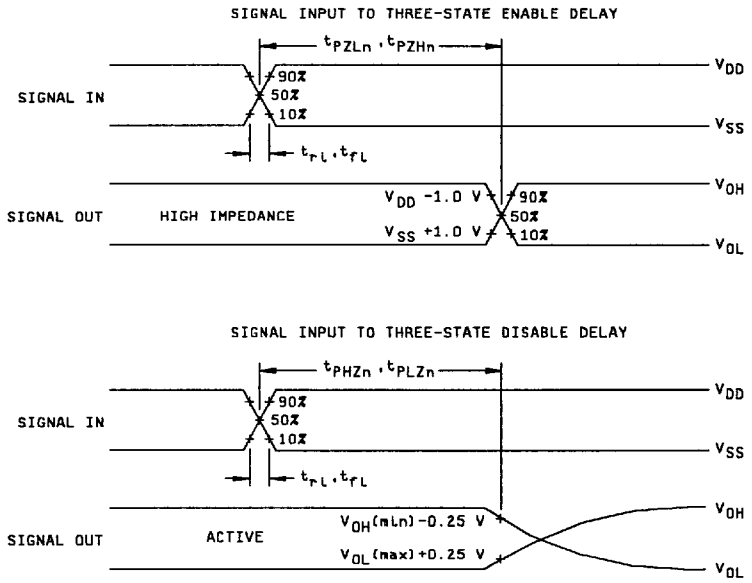


FIGURE 4. Switching test circuit and waveforms - continued.

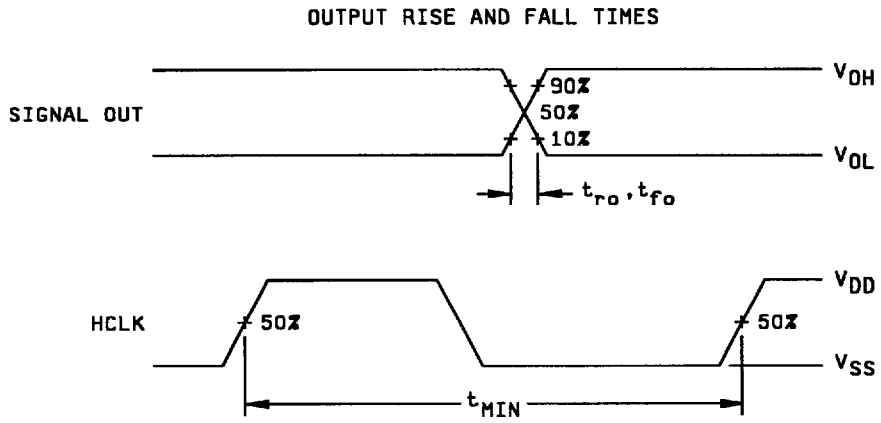
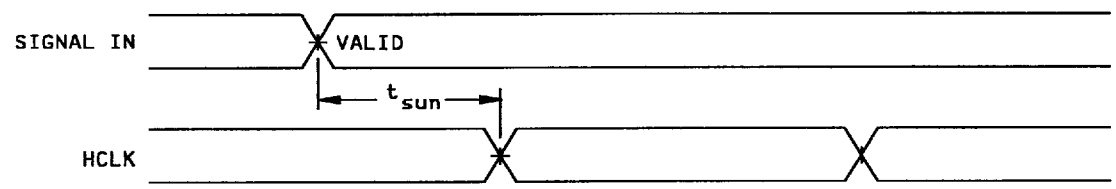
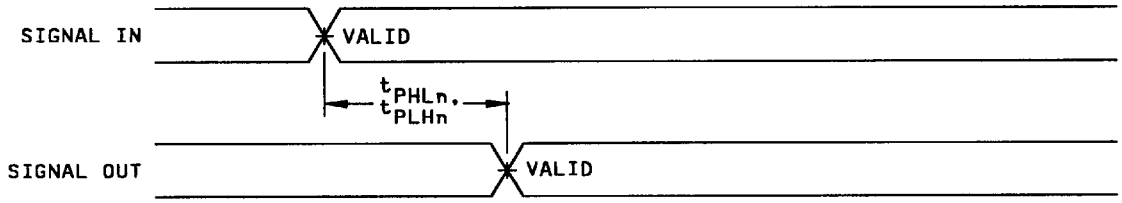


FIGURE 4. Switching test circuit and waveforms - continued.

SETUP TIME FOR SIGNAL INPUT TO HCLK



PROPAGATION DELAY OF SIGNAL FORM INPUT TO OUTPUT



PROPAGATION DELAY FROM HCLK TO SIGNAL OUTPUT

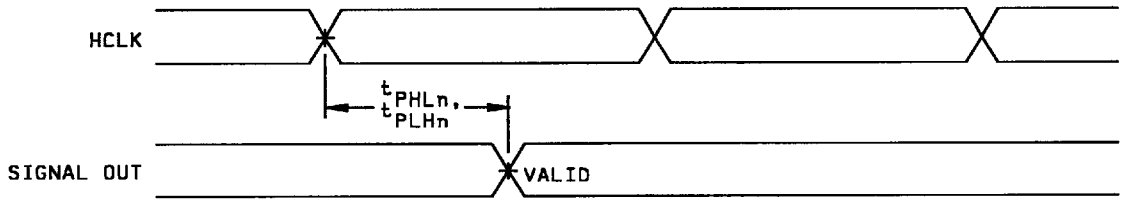


FIGURE 4. Switching test circuit and waveforms - continued.

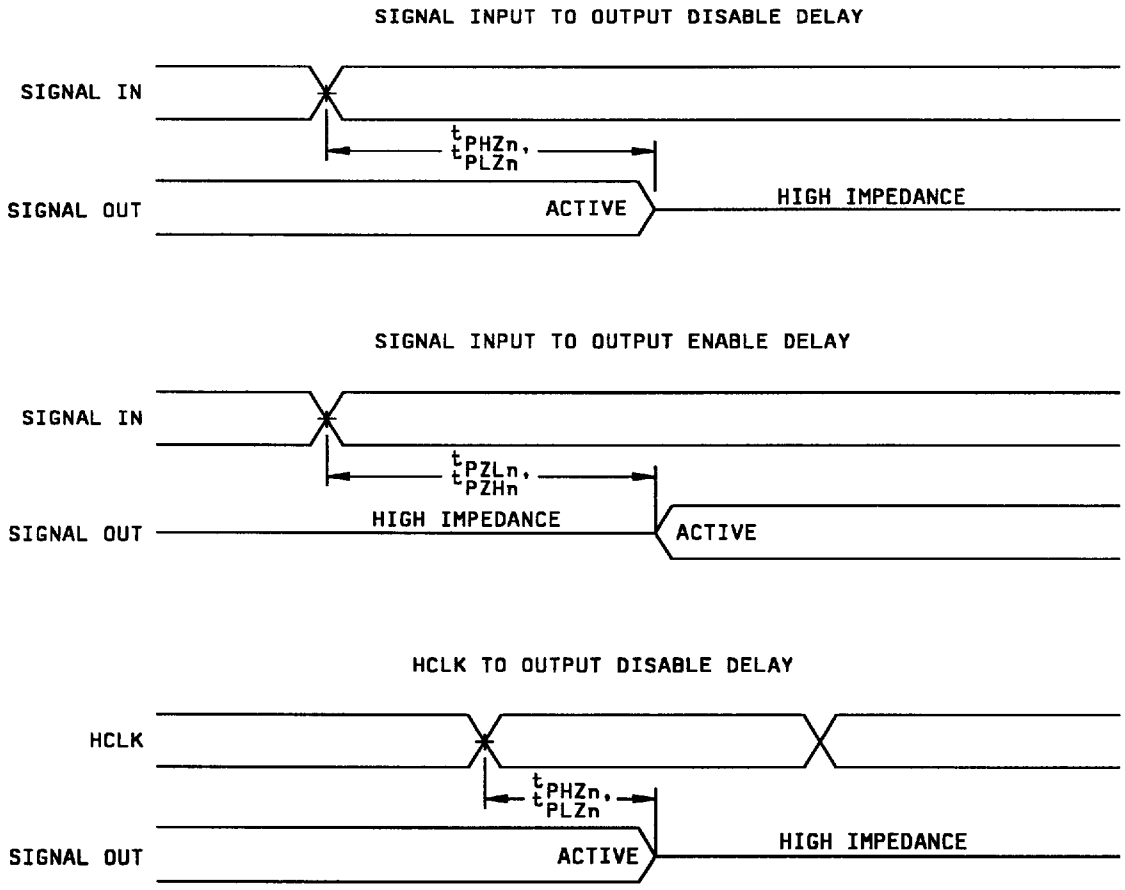


FIGURE 4. Switching test circuit and waveforms - continued.

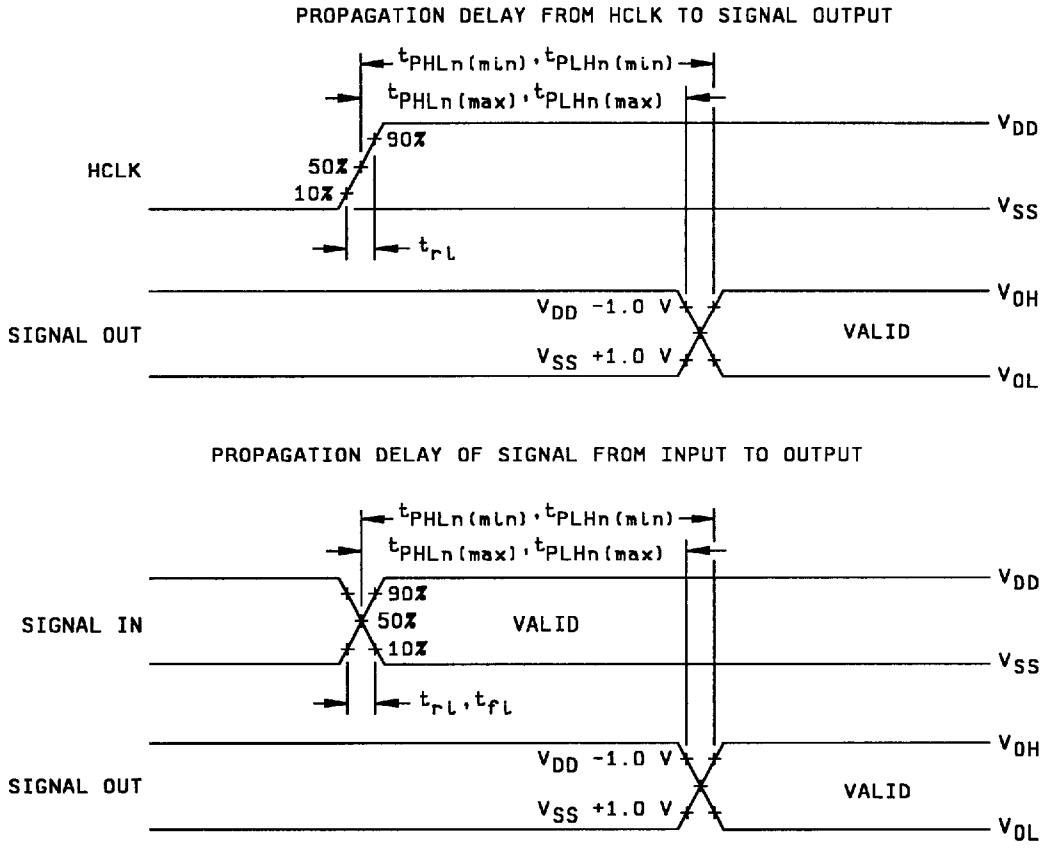
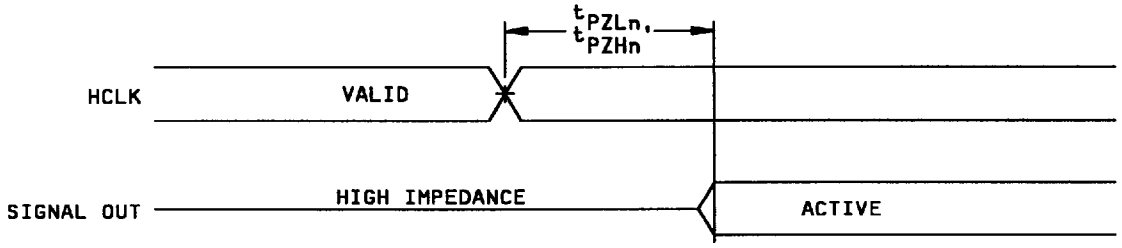


FIGURE 4. Switching test circuit and waveforms - continued.

HCLK TO OUTPUT ENABLE DELAY



HOLD TIME FOR SIGNAL INPUT FROM HCLK

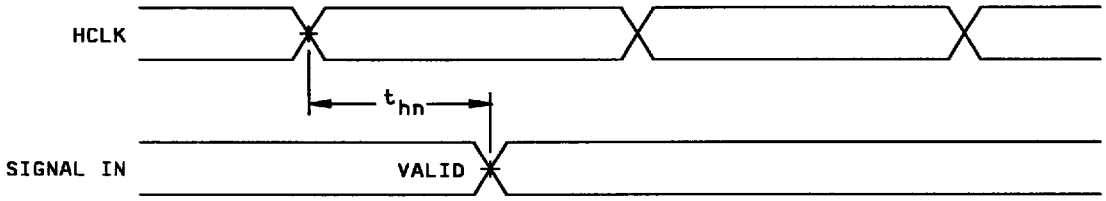


FIGURE 4. Switching test circuit and waveforms - continued.

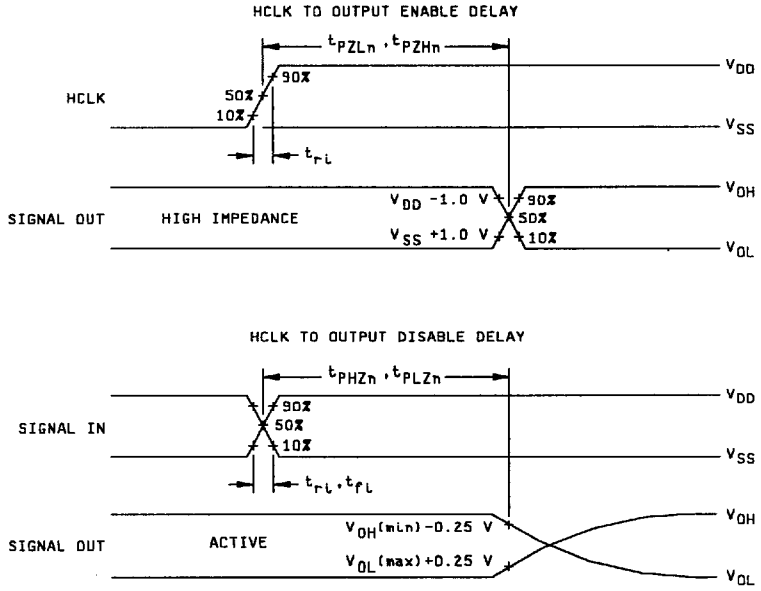


FIGURE 4. Switching test circuit and waveforms - continued.

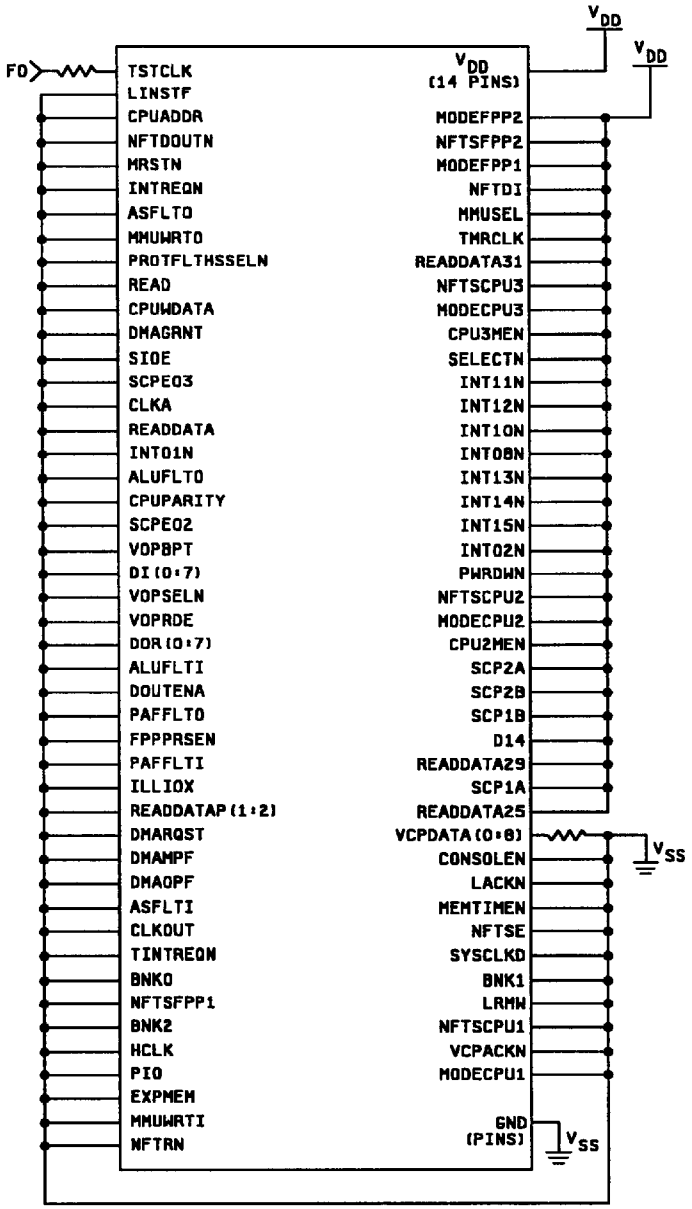


FIGURE 5. Radiation exposure circuit.

Notes:

1. F0 = 1 MHz, 0-5 v square wave to TSTCLK.
2. V_{DD} = 5.5 V ± 0.5 V, V_{SS} = 0.0 V ± 0.5 V.
3. VCPDATA (0:8) toground through 10 KΩ resistor.
4. The following pins are connected to ground:
19, 26, 28, 30, 74, 78, 80, 101 - 109, 111, 121, 125 - 141, 143 - 161, 164 - 166, 173, 174, 176, 177, 178, 180, 181, 182, 184, 185, 186, 188, 190, 192, 198, 200.

The following pins are connected to ground through a 10 kΩ resistor:
1, 2, 3, 10, 12, 13, 14, 17

The following pins are connected to V_{DD} (+5.5 v):
4, 7, 9, 11, 15, 16, 18, 20, 21, 22, 24, 47, 48, 50, 52, 53, 55 - 62, 68, 70, 72, 73, 75, 84, 91, 93, 95 - 98, 100, 118, 120, 122, 124, 168, 170, 172.

Pin 162, TSTCLK, should be supplied by a 1 Mhz, 0 - 5 V square wave via the coax cable connected to the test fixture. This line should be terminated in 50 Ω either at the functions generator or by observing the signal on an oscilloscope terminated in 50 Ω. Upon power-up, the GVSC enters the reset state. However, to guarantee reset, MRSTN (pin 19) must also be held LOW. The TSTCLK signal is applied so that the memory timeout counter is cleared.

FIGURE 5. Radiation exposure circuit. - Continued

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Element evaluation.

4.2.1 Microcircuit dice. Microcircuit dice shall be produced on a QML certified line and probed at wafer level according to the manufacturer's QM plan.

4.2.2 Capacitors. Capacitor element evaluation shall be performed according to the manufacturer's QM plan.

4.2.3 Package evaluation. Packages shall be electrically tested by the package manufacturer. Element evaluation shall be performed according to the manufacturer's QM plan.

4.3 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.3.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.3.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

d. Those devices whose measured characteristics, after burn-in, exceed the specified delta (Δ) limits or electrical parameter limits specified in table IIB, are defective and shall be removed from the lot. The verified failures divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot and the lot shall be accepted or rejected based on the PDA specified in the manufacturer's QM plan.

4.4 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.5.1 through 4.5.4).

4.5 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.5.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroups 4, 5, and 6 (C_{IN} and C_{OUT} measurements), if not tested, shall be guaranteed to the limits specified in table IA.

4.5.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.5.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.5.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.5.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Pre-Seal Pre-Burn-in (See 4.3)		1,2 7, 8A,9, 10	1, 2, 7, 8A, 9 10
Pre seal electrical parameters (see 4.3)		1, 2, 3, 7, 8A 8B, 9, 10, 11	1, 2, 3, 7, 8A 8B, 9, 10, 11
Initial (pre burn-in) electrical parameters (see 4.3)		1, 7, 9	1, 7, 9
Dynamic burn-in (see 4.3)		Required	Required
Interim (post dynamic burn-in) electrical parameters (see 4.3)		1, 2, 3, 7, 8A, 8B, 9, 10, 11 2/ 3/	1, 2, 3, 7, 8A, 8B, 9, 10, 11 2/ 3/
Static burn-in (see 4.3)	Required	Required	Required
Final electrical parameters (see 4.3)	1, 2, 3, 7, 8A, 8B, 9, 10, 11 1/	1, 2, 3, 7, 8A, 8B, 9, 10, 11 2/ 3/	1, 2, 3, 7, 8A, 8B, 9, 10, 11 2/ 3/
Group A test requirements (see 4.5)	1, 2, 3, 4, 5, 6, 7 8A, 8B, 9, 10, 11 4/	1, 2, 3, 4, 5, 6, 7 8A, 8B, 9, 10, 11 4/	1, 2, 3, 4, 5, 6, 7 8A, 8B, 9, 10, 11 4/
Group C end-point electrical parameters (see 4.5)	1, 7	1, 2, 3, 7, 8A, 8B, 9, 10, 11 3/	1, 2, 3, 7, 8A, 8B, 9, 10, 11 3/
Group D end-point electrical parameters (see 4.5)	1, 7	1, 7	1, 7
Group E end-point electrical parameters (see 4.5)	1, 7 5/	1, 7 5/	1, 7 5/

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.
3/ After completion of life test, or burn-in, deltas shall be calculated and shall meet the requirements of table IIB herein.
4/ See 4.5.1c.
5/ 3.5 volt Rigel vectors are excluded from group E functional requirements.

TABLE IIB. Delta limits at +25°C.

Test 1/	Delta limit (all device types)
I_{DDSB}	±20% of the initial measured value or ±200 µA, whichever magnitude is greater
I_{IH}, I_{IL}, I_{OZH}, I_{OZL}	±10% of the initial measured value or ±1.0 µA, whichever magnitude is greater
V_{OH1}, V_{OH2}, V_{OL1}, V_{OL2}	±10% of the initial measured value or ±50 mV, whichever magnitude is greater

1/ The above parameters shall be tested in accordance with table IA and shall be recorded before and after the required burn-in and life tests to determine the delta.

4.5.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. Alldevice classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 and as specified herein.

4.5.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5K rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ± 5°C. The test shall be performed at initial qualification and after any design on process changes which may affect the radiation responses of the device.

4.5.4.2 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.5.4.3 Dose rate upset testing. Dose rate upset testing shall be performed in accordance with test method 1021 of MIL-STD-883 and as specified herein.

a. Transient dose rate upset testing for class M devices shall be performed at initial qualification and after any design or process changes which may effect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535. Device parametric parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-PRF-38535.

4.5.4.4 Single event phenomena (SEP). SEP testing shall be required on class V devices. SEP testing shall be performed on the SEC or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM standard F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be normal to the die surface and 60 degrees to the normal, inclusive (i.e., $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be greater than 100 errors or $\geq 10^7$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ion/cm^2/s. The cross section shall be verified to be flux independent by measuring the cross section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be $\geq$ 20 microns in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be V_{DD} = 4.5 V dc for the upset measurements and V_{DD} = 5.5 V dc for the latchup measurements.

g. For SEP test limits, see table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply CenterColumbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Number of transients (SEP).

e. Occurance of latchup (SEP).

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 98-06-30

Approved sources of supply for SMD 5962-96847 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962H9684701QYC	34168	RX1750-01
5962H9684702QYC	34168	RX1750-02

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34168	Honeywell, Inc. Solid State Electronics Center 12001 Hwy 55 Plymouth, MN 55441-4744

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.