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MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

Military 6226

Advance Information

128K x 8 Bit Static Random Access Memory

SRAM

The 6226 is a 1,048,576 bit static random access memory organized as 131,072 words of 8 bits, fabricated using high performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

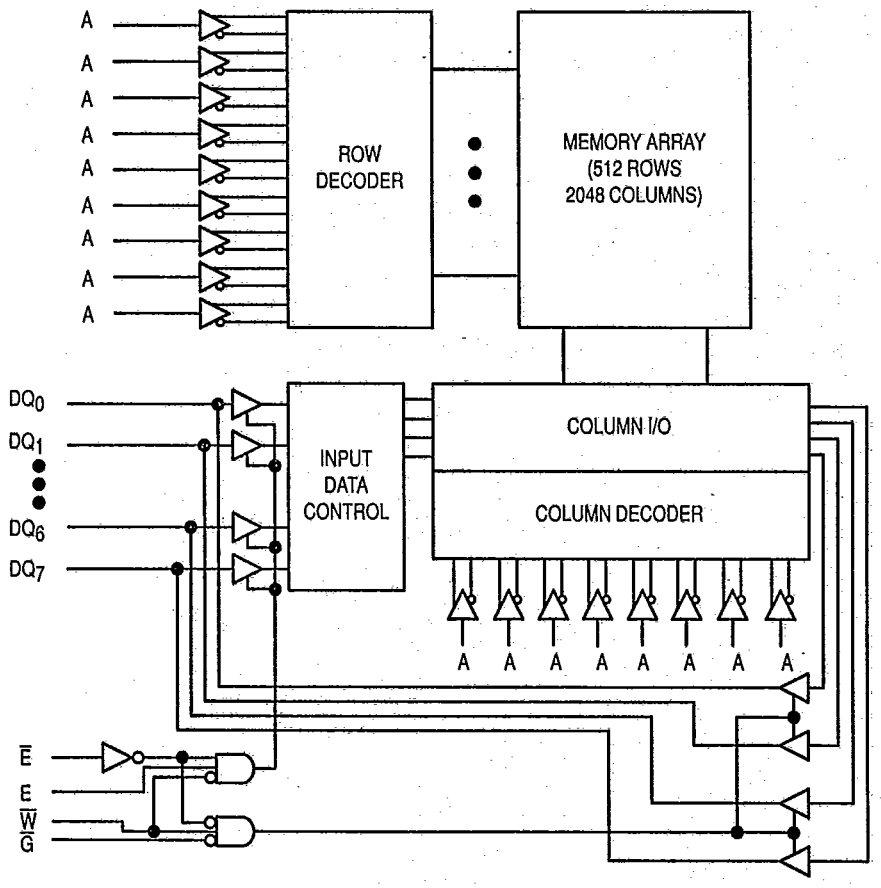
The 6226 is equipped with both chip enable (E) and output enable (G) inputs, allowing for greater system flexibility. Either input, when high, will force the outputs to high impedance.

The 6226 is available in a 600 mil, 32 lead ceramic DIL and in a 550 x 850 mil, 32 lead surface-mount LCC package.

- Single 5.0 V ± 10% Power Supply
- Full Access Time — 35 ns Max.
- Equal Address and Chip Enable Access Time
- Three State Outputs
- Fully TTL Compatible
- Low Power Dissipation: 150/140/130 mA Maximum, Active AC
  35 ns = 150 mA
  45 ns = 140 mA
  55 ns = 130 mA

AVAILABLE AS
1) JAN: N/A
2) SMD: Pending
3) 883C: 6226 - XX/BXAJC
X = CASE OUTLINE AS FOLLOWS:
PACKAGE: DIL: X
LCC: U
XX = Speed in ns (35, 45, 55)
The letter "M" appears after the speed on LCC

BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

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BURN-IN CONDITIONS:								
V_{CC} = 5.0 V(min)/ 6.0 V(max), R_1 = 39.2 kΩ ± 20%, C_1 = 0.1 µF ± 20%, V_H = 3.0 V(min)/5.0 V(max), V_L = −0.5 V(min)/0.0 V(max),								
CP1:	100 kHz	CP6:	3.125 kHz	CP11:	97.66 Hz	CP16:	3.052 Hz	
CP2:	50 kHz	CP7:	1.563 kHz	CP12:	48.83 Hz	CP17:	1.526 Hz	
CP3:	25 kHz	CP8:	0.781 kHz	CP13:	24.41 Hz	CP18:	0.763 Hz	
CP4:	12.5 kHz	CP9:	0.391 kHz	CP14:	12.21 Hz	CP19:	0.382 Hz	
CP5:	6.25 kHz	CP10:	0.195 kHz	CP15:	6.104 Hz	CP20:	0.191 Hz	

PIN NAME and FUNCTIONS

$A_0 - A_{16}$	Address Inputs
$\overline{W}$	Write Enable
$\overline{E}$, E	Chip Enable
$\overline{G}$	Output Enable
$DQ_0 - DQ_7$	Data Input/Output
V_{CC}	+ 5.0 V Power Supply
V_{SS}	Ground
N.C.	No Connection

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit.

PIN ASSIGNMENTS

Function	DIL	LCC	Burn-In (Condition-D)
N.C.	1	1	N.C.
A_{16}	2	2	CP2
A_{14}	3	3	CP3
A_{12}	4	4	CP4
A_7	5	5	CP5
A_6	6	6	CP6
A_5	7	7	CP7
A_4	8	8	CP8
A_3	9	9	CP9
A_2	10	10	CP10
A_1	11	11	CP11
A_0	12	12	CP12
DQ_0	13	13	CP20 to R_1
DQ_1	14	14	CP20 to R_1
DQ_2	15	15	CP20 to R_1
V_{SS}	16	16	GND
DQ_3	17	17	CP20 to R1
DQ_4	18	18	CP21 to R1
DQ_5	19	19	CP21 to R_1
DQ_6	20	20	CP21 to R_1
DQ_7	21	21	CP21 to R_1
$\overline{E}$	22	22	GND
A_{10}	23	23	CP18
$\overline{G}$	24	24	CP19
A_{11}	25	25	CP17
A_9	26	26	CP16
A_8	27	27	CP15
A_{13}	28	28	CP14
$\overline{W}$	29	29	CP1
E	30	30	HIGH
A_{15}	31	31	CP13
V_{CC}	32	32	V_{CC}, C_1 to GND

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TRUTH TABLE						
$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	I/O Pin	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High Z	—
L	H	H	Read	I_{CCA}	High Z	—
L	L	H	Read	I_{CCA}	D_{OUT}	Read Cycle
L	X	L	Write	I_{CCA}	D_{IN}	Write Cycle

X = Don't Care

ABSOLUTE MAXIMUM RATINGS (See Note)			
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{IN}, V_{OUT}	−0.5 to V_{CC} + 5.0	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias (T_A = 25°C)	T_{bias}	−55 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Temperature Range	T_A	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = −55°C to +125°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS					
Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.5 *	—	0.8	V

* V_{IL} (min) = −0.5 Vdc; V_{IL} (min) = −3.0 Vdc (pulse width ≤ 20 ns)

DC CHARACTERISTICS					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	±5.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{OUT} = 0 to V_{CC})	$I_{lkg(O)}$	—	—	±5.0	µA
AC Supply Current (I_{OUT} = 0 mA) 6226-35: t_{AVAV} = 35 ns 6226-45: t_{AVAV} = 45 ns 6226-55: t_{AVAV} = 55 ns	I_{CCA} I_{CCA} I_{CCA}	— — —	— — —	150 140 130	mA mA mA
TTL Standby Current ($\overline{E}$ = V_{IH}, No Restrictions on Other Inputs)	I_{SB1}	—	30	40	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} – 2.0 V, No Restrictions on Other Inputs)	I_{SB2}	—	20	30	mA
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)					
Characteristic		**Symbol**	**Typ**	**Max**	**Unit**
Input Capacitance	All Inputs Except $\overline{E}$, E and DQ $\overline{E}$, E	C_{in}	4.0 5.0	6.0 7.0	pF pF
I/O Capacitance	DQ	$C_{I/O}$	5.0	7.0	pF

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AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = – 55°C to +125°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level	1.5 V
Input Pulse levels	0 to 3.0 V
Input Rise/Falls Time	≥ 5.0 ns
Output Timing Measurement Reference Level	1.5 V
Output Load	See Figure 1A

READ CYCLE (See Note 1)

Parameter	Symbol Standard	Symbol Alternate	6226-35		6226-45		6226-55		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	35	—	45	—	55	—	ns	2
Address Access Time	t_{AVQV}	t_{AA}	—	35	—	45	—	55	ns	—
Enable Access Time	t_{ELQV}	t_{ACS}	—	35	—	45	—	55	ns	—
Output Enable Access Time	t_{GLQV}	t_{OE}	—	15	—	15	—	20	ns	—
Output Hold from Address Change	t_{AXQX}	t_{OH}	5.0	—	5.0	—	5.0	—	ns	—
Enable Low to Output Active	t_{ELQX}	t_{LZ}	5.0	—	5.0	—	5.0	—	ns	3, 4, 5
Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	—	15	—	15	—	20	ns	3, 4, 5
Output Enable to Output Active	t_{GLQX}	t_{LZ}	0	—	0	—	0	—	ns	3, 4, 5
Output Enable to Output High-Z	t_{GLQZ}	t_{HZ}	0	15	0	15	0	20	ns	3, 4, 5
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	ns	5
Power Down Time	t_{EHICCL}	t_{PD}	—	35	—	45	—	55	ns	5

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. A any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQX} max is less than t_{GHQX} min, both for a given device and from device to device.
4. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
5. These parameters are periodically sampled and not 100% tested.
6. Device is continuously selected ($\overline{E}$ = V_{IL}, E = V_{IH}, $\overline{G}$ = V_{IL}).
7. Address valid prior to coincident with $\overline{E}$ going low/E going high.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Note 1)										
Parameter	Symbol Standard	Symbol Alternate	6226-35		6226-45		6226-55		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	35	—	45	—	55	—	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	ns	—
Address Valid to End of Write	t_{AVWH}	t_{AW}	20	—	20	—	30	—	ns	—
Write Pulse Width	t_{WLWH}	t_{WP}	20	—	20	—	30	—	ns	—
Data Valid to End of Write	t_{DVWH}	t_{DW}	15	—	15	—	20	—	ns	—
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	ns	—
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	15	0	15	0	20	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	t_{OW}	0	—	0	—	0	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	ns	—

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low/E high and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
4. Parameters is sampled and not 100% tested.
5. A any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

AC TEST LOADS

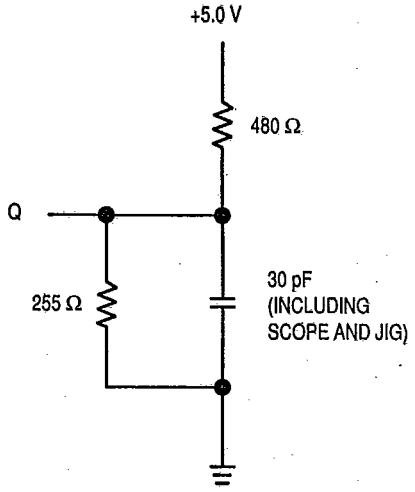

Figure 1A.

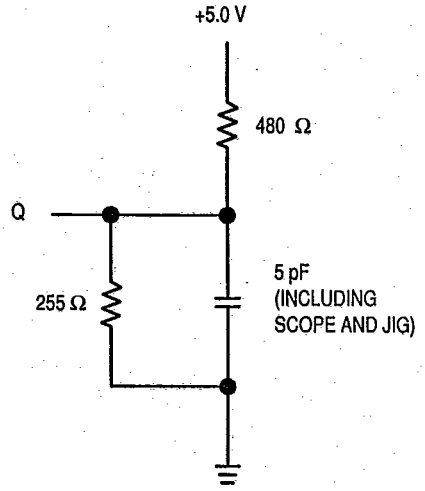

Figure 1B.

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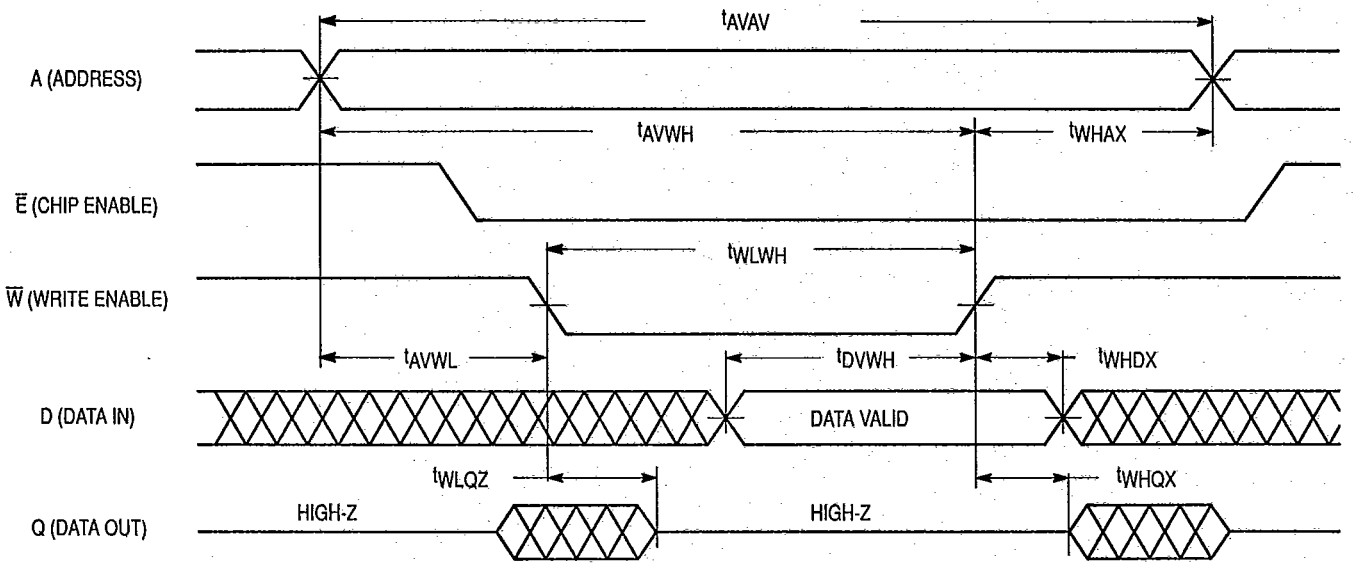
WRITE CYCLE 2 ($\overline{E}$ Controlled, See Note 1)										
Parameter	Symbol Standard	Symbol Alternate	6226-35		6226-45		6226-55		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	35		45		55		ns	2
Address Setup Time	t_{AVEL}	t_{AS}	0		0		0		ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	20		25		30		ns	
Enable to End of Write	t_{ELEH}	t_{CW}	20		25		30		ns	3, 4
Write Pulse Width	t_{WLEH}	t_{WP}	20		25		30		ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	15		15		20		ns	
Data Hold Time	t_{EHDX}	t_{DH}	0		0		0		ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0		0		0		ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low/E high and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
4. If $\overline{E}$ goes high coincident with or after $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 1 ($\overline{W}$ Controlled)



TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

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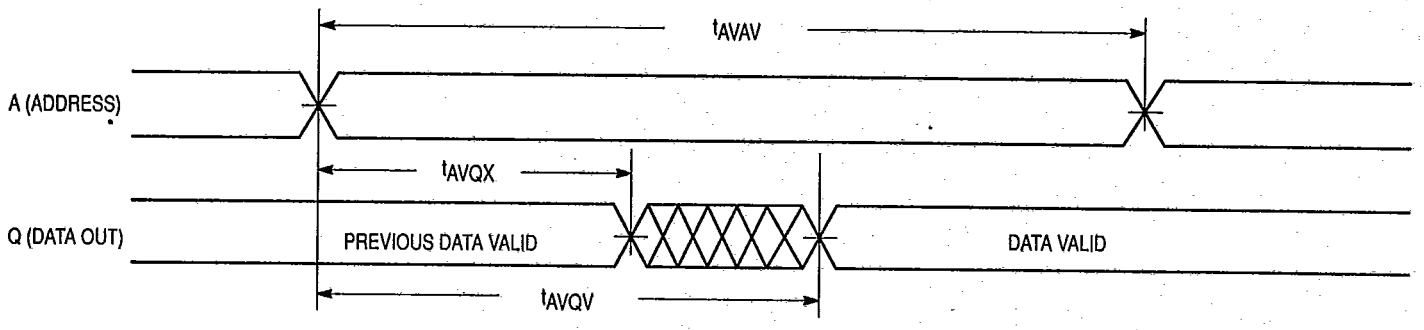
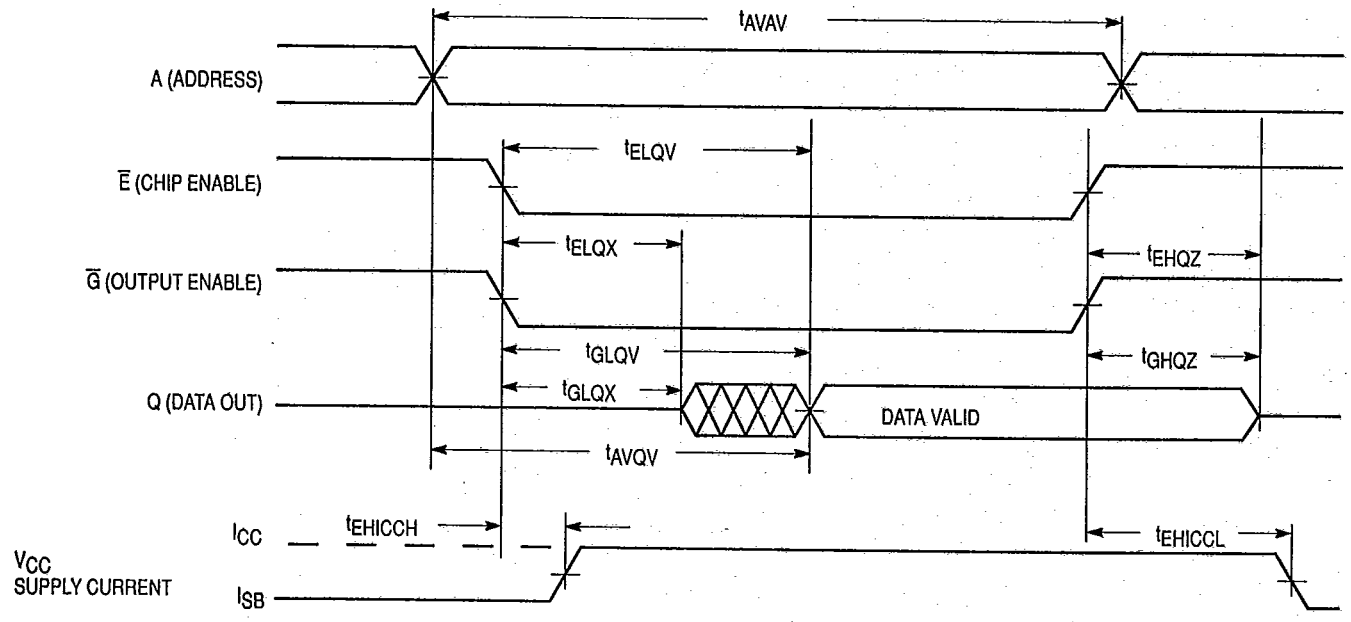
READ CYCLE 1 (See Note 6 above)



READ CYCLE 2 (See Note 7 above)



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WRITE CYCLE 2 ($\overline{E}$ Controlled)