



**HIGH SPEED OPTICALLY  
COUPLED ISOLATOR  
PHOTODARLINGTON OUTPUT**

**APPROVALS**

- UL recognised, File No. E91231

**DESCRIPTION**

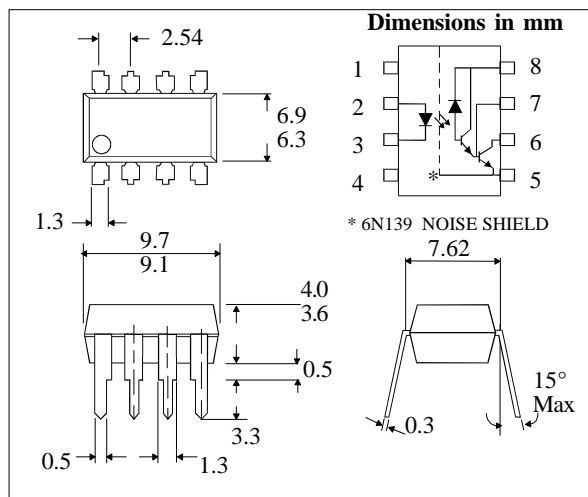
These diode-darlington optocouplers use a light emitting diode and an integrated high gain photon detector to provide 2500Volts<sub>RMS</sub> electrical isolation between input and output. Separate connection for the photodiode bias and output darlington collector improve the speed up to a hundred times that of a conventional photo-darlington coupler by reducing the base-collector capacitance.

**FEATURES**

- High speed - DC to 300kBits/s operation
- High Common Mode Transient Immunity 10kV/μs typical
- TTL Compatible - 0.1V V<sub>OL</sub> typical
- Base access allows Gain Bandwidth Adjustment
- Low Input Current Requirement - 0.5mA
- High Current Transfer Ratio - 2000% typ.
- Open Collector Output
- 2500V<sub>RMS</sub> Withstand Test Voltage, 1 min
- 6N139 has improved noise shield which gives superior common mode rejection
- Options :-  
10mm lead spread - add G after part no.  
Surface mount - add SM after part no.  
Tape&reel - add SMT&R after part no.
- All electrical parameters 100% tested
- Custom electrical selections available

**APPLICATIONS**

- Line receivers
- Digital logic ground isolation
- Telephone ring detector
- Current loop receiver



**ABSOLUTE MAXIMUM RATINGS  
(25°C unless otherwise specified)**

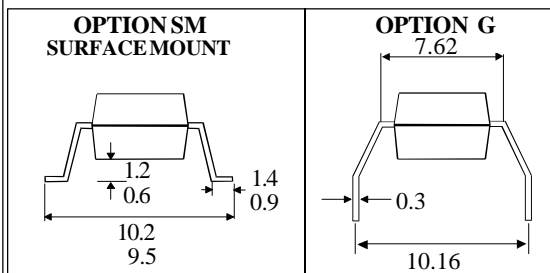
Storage Temperature \_\_\_\_\_ -55°C to + 125°C  
 Operating Temperature \_\_\_\_\_ -40°C to + 85°C  
 Lead Soldering Temperature  
 (1/16 inch (1.6mm) from case for 10 secs) 260°C

**INPUT DIODE**

Average Forward Current \_\_\_\_\_ 20mA ( 1 )  
 Peak Forward Current \_\_\_\_\_ 40mA  
 ( 50% duty cycle, 1ms pulse width )  
 Peak Transient Current \_\_\_\_\_ 1.0A  
 (equal to or less than 1μs P.W., 300 pps)  
 Reverse Voltage \_\_\_\_\_ 5V  
 Power Dissipation \_\_\_\_\_ 35mW ( 2 )

**DETECTOR**

Output Current \_\_\_\_\_ 60mA ( 3 )  
 Emitter-base Reverse Voltage \_\_\_\_\_ 5V  
 Supply and Output Voltage  
 6N138 \_\_\_\_\_ -0.5 to +7V  
 6N139 \_\_\_\_\_ -0.5 to +18V  
 Power Dissipation \_\_\_\_\_ 100mW ( 4 )



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**ELECTRICAL CHARACTERISTICS (  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  Unless otherwise noted )**

PARAMETER	SYM	DEVICE	MIN	TYP*	MAX	UNITS	TEST CONDITION
Current Transfer Ratio (note 5, 6)	CTR	6N139	400	2000		%	$I_F = 0.5\text{mA}, V_O = 0.4\text{V}$ $V_{CC} = 4.5\text{V}$
		6N139	500	2000		%	$I_F = 1.6\text{mA}, V_O = 0.4\text{V}$ $V_{CC} = 4.5\text{V}$
		6N138	300	2000		%	$I_F = 1.6\text{mA}, V_O = 0.4\text{V}$ $V_{CC} = 4.5\text{V}$
Logic Low Output Voltage (note 6)	$V_{OL}$	6N139		0.1	0.4	V	$I_F = 1.6\text{mA}, I_O = 6.4\text{mA}$ $V_{CC} = 4.5\text{V}$
		6N139		0.1	0.4	V	$I_F = 5\text{mA}, I_O = 15\text{mA}$ $V_{CC} = 4.5\text{V}$
		6N139		0.1	0.4	V	$I_F = 12\text{mA}, I_O = 24\text{mA}$ $V_{CC} = 4.5\text{V}$
		6N138		0.1	0.4	V	$I_F = 1.6\text{mA}, I_O = 4.8\text{mA}$ $V_{CC} = 4.5\text{V}$
Logic High Output Current (note 6)	$I_{OH}$	6N139		0.1	100	$\mu\text{A}$	$I_F = 0\text{mA}$ $V_O = V_{CC} = 18\text{V}$
		6N138		0.001	250	$\mu\text{A}$	$I_F = 0\text{mA}$ $V_O = V_{CC} = 7\text{V}$
Logic Low Supply Current (note 6)	$I_{CCL}$			0.2		$\text{mA}$	$I_F = 1.6\text{mA}, V_O = \text{open}$ $V_{CC} = 5\text{V}$
Logic High Supply Current (note 6)	$I_{CCH}$			10		$\mu\text{A}$	$I_F = 0\text{mA}, V_O = \text{open}$ $V_{CC} = 5\text{V}$
Input Forward Voltage	$V_F$			1.45	1.7	V	$I_F = 1.6\text{mA}, T_A = 25^\circ\text{C}$
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.8		$\text{mV}/^\circ\text{C}$	$I_F = 1.6\text{mA}$
Input Reverse Voltage	$V_R$		5			V	$I_R = 10\mu\text{A}, T_A = 25^\circ\text{C}$
Input Capacitance	$C_{IN}$			60		$\text{pF}$	$f = 1\text{MHz}, V_F = 0$
Input-output Isolation Voltage	$V_{ISO}$		2500	5000		$V_{RMS}$	R.H.equal to or less than 50%, $t = 1\text{min}$ . $T_A = 25^\circ\text{C}$
Resistance (Input to Output) (note 7)	$R_{I-O}$			$10^{12}$		$\Omega$	$V_{I-O} = 500\text{V dc}$
Capacitance (Input to Output) (note 7)	$C_{I-O}$			0.6		$\text{pF}$	$f = 1\text{MHz}$

\* All typicals at  $T_A = 25^\circ\text{C}$

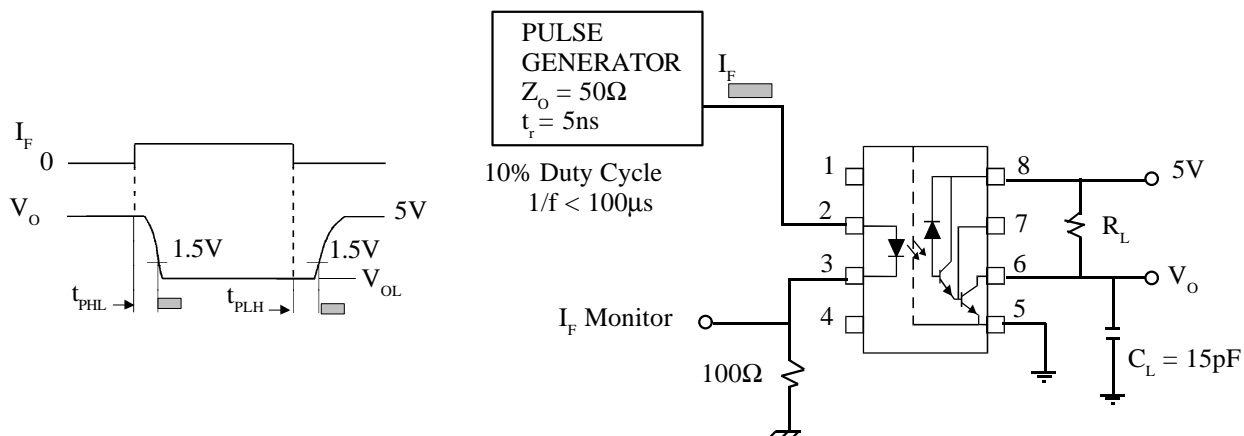
**SWITCHING SPECIFICATIONS AT  $T_A = 25^\circ\text{C}$  ( $V_{CC} = 5\text{V}$  Unless otherwise noted )**

PARAMETER	SYM	DEVICE	MIN	TYP	MAX	UNITS	TESTCONDITION
Propagation Delay Time to Logic Low at Output ( fig 1 )( note6,8 )	$t_{PHL}$	6N139		5.0	25	$\mu\text{s}$	$I_F = 0.5\text{mA}, R_L = 4.7\text{k}\Omega$
		6N139		0.2	1	$\mu\text{s}$	$I_F = 12\text{mA}, R_L = 270\Omega$
		6N138		1.0	10	$\mu\text{s}$	$I_F = 1.6\text{mA}, R_L = 2.2\text{k}\Omega$
Propagation Delay Time to Logic High at Output ( fig 1 )( note6,8 )	$t_{PLH}$	6N139		1.0	60	$\mu\text{s}$	$I_F = 0.5\text{mA}, R_L = 4.7\text{k}\Omega$
		6N139		1.0	7	$\mu\text{s}$	$I_F = 12\text{mA}, R_L = 270\Omega$
		6N138		4.0	35	$\mu\text{s}$	$I_F = 1.6\text{mA}, R_L = 2.2\text{k}\Omega$
Common Mode Transient Immunity at Logic High Level Output ( fig 2 )( note9 )	$CM_H$		1000	10000		$\text{V}/\mu\text{s}$	$I_F = 0\text{mA}, V_{CM} = 10V_{PP}$ $R_L = 2.2\text{k}\Omega$
Common Mode Transient Immunity at Logic Low Level Output ( fig 2 )( note9 )	$CM_L$		-1000	-10000		$\text{V}/\mu\text{s}$	$I_F = 1.6\text{mA}, V_{CM} = 10V_{PP}$ $R_L = 2.2\text{k}\Omega$

**NOTES:-**

1. Derate linearly above  $50^\circ\text{C}$  free air temperature at a rate of  $0.4 \text{ mA}/^\circ\text{C}$ .
2. Derate linearly above  $50^\circ\text{C}$  free air temperature at a rate of  $0.7 \text{ mW}/^\circ\text{C}$ .
3. Derate linearly above  $25^\circ\text{C}$  free air temperature at a rate of  $0.7 \text{ mA}/^\circ\text{C}$ .
4. Derate linearly above  $25^\circ\text{C}$  free air temperature at a rate of  $2.0 \text{ mW}/^\circ\text{C}$ .
5. CURRENT TRANSFER RATIO is defined as the ratio of output collector current,  $I_O$ , to the forward LED input current,  $I_F$  times 100%.
6. Pin 7 open.
7. Device considered a two-terminal device: pins 1,2,3, and 4 shorted together and pins 5,6,7 and 8 shorted together.
8. Use of a resistor between pin 5 and 7 will decrease gain and delay time.
9. Common mode transient immunity in Logic High level is the maximum tolerable (positive)  $dV_{CM}/dt$  on the leading edge of the common mode pulse  $V_{CM}$  to assure that the output will remain in a Logic High state (i.e.  $V_O > 2.0\text{V}$ ). Common mode transient immunity in Logic Low level is the maximum tolerable (negative)  $dV_{CM}/dt$  on the trailing edge of the common mode pulse signal,  $V_{CM}$  to assure that the output will remain in Logic Low state (i.e.  $V_O < 0.8\text{V}$ ).

**FIG.1 SWITCHING TEST CIRCUIT**



**FIG. 2 TEST CIRCUIT FOR TRANSIENT IMMUNITY AND TYPICAL WAVEFORMS**

