Complete 12-Bit Sampling A/D Converter for Digital Signal Processing

AD1332

FEATURES

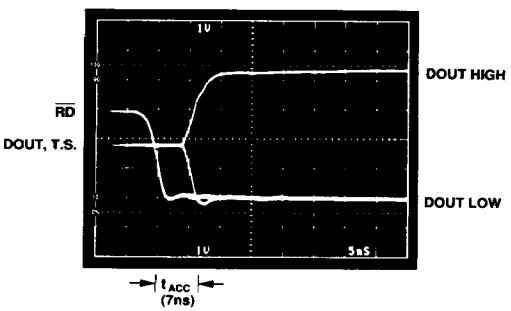
Complete A/D System for DSP Includes:
- **4th Order Antialiasing Filter**
- **12-Bit Sampling A/D Converter**
- **32-Word FIFO Memory**
- **Fully Asynchronous, High Speed Digital Interface**

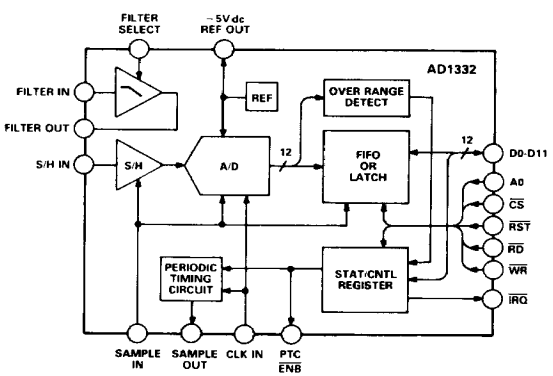
Sample Rate up to 125 kHz
Entire System Is Dynamically Specified
15 ns Data Access Time Allows "No Wait State" Interface to: ADSP-2100 (A), TMS320C25 DSP56000, NECμPD77230

APPLICATIONS

Sonar Signal Processing
Vibration Analysis
Ultrasound Imaging
PC Data Acquisition
High Speed Modems
Motion Control
Speech Processing

DATA ACCESS TIME
(Typical at +25°C)





AD1332 Block Diagram

PRODUCT DESCRIPTION

The AD1332 is a complete, 12-bit A/D converter system optimized for use in high speed digital signal processing (DSP) applications. The device consists of a fourth order antialiasing filter, a 12-bit sampling A/D, a fully asynchronous high speed digital interface and a 32-word FIFO memory. The AD1332 is manufactured using highly reliable advanced hybrid circuit assembly techniques and is packaged in a 40-pin hermetic DIP.

The antialiasing filter is an active four-pole Butterworth. Cutoff frequencies (f_C) are user-selectable (capacitor programmable), and operation is specified for f_C up to 50 kHz. The filter may be bypassed entirely if desired.

The 12-bit sampling A/D converter can convert ±5 V full-scale signals at sample rates up to 125 kHz. The rate is programmable by means of a single external clock. The entire converter system is specified and tested for signal-to-noise ratio and total harmonic distortion.

The digital interface provides a true asynchronous link between the A/D and a high speed microprocessor. Data transfer is controlled by generating an interrupt signal when data is available. Interrupts can be generated when the FIFO is full (32 words), half-full (16 words), or when a single word of data is ready (FIFO bypassed). In addition, the AD1332 can generate an interrupt signal when the A/D conversion results are overrange.

The AD1332 provides a completely specified and tested system that bridges the interface and specification gap between A/D converters and high speed DSP.

This is an abridged version of the data sheet. To obtain a complete data sheet, contact your nearest sales office.

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AD1332—SPECIFICATIONS (T_A = +25°C, V_S = ±15 V, V_{DD} = +5 V, unless otherwise noted)

	AD1332BD			AD1332TD			
	Min	Typ	Max	Min	Typ	Max	Units
FILTER (C1–C4 = 500 pF ±1%)							
Input Impedance	8	10		8	10		kΩ
Voltage Range	±10			±10			V
Output Voltage Range $R_L \geq 4$ k	±10			±10			V
Corner Frequency, Accuracy		±2			±2		%
Drift		±0.01			±0.01		%/°C
Gain[1] @ dc	−0.05		+0.05	−0.05		+0.05	dB
0.8 f_C	−1		+1	−1		+1	dB
f_C		−3			−3		dB
4 f_C		−48	−45		−48	−45	dB
10 f_C		−76			−76		dB
Settling Time to 0.01%, 10 V Step		100	125		100	125	μs
Offset		±2	±5		±2	±5	mV
Drift		±20	±100		±20	±100	μV/°C
Noise		75			75		μV rms
SAMPLING A/D CONVERTER[2]							
Input Impedance	4	5		4	5		kΩ
Voltage Range		−5 to +5			−5 to +5		V
Output Coding		Offset Binary			Offset Binary		
CLK IN Frequency	0.5		2.5	0.5		2.5	MHz
High Time	200			200			ns
Low Time	200			200			ns
Sampling Rate (f_S)			125			125	kHz
S/H							
Acquisition Time			2.8			2.8	μs
Droop Rate		0.25	0.5		0.25	0.5	mV/ms
Over Temperature		Doubles Every 10°C			Doubles Every 10°C		
Aperture Delay Time		15			15		ns
Static Characteristics							
Integral Nonlinearity		±1/2	±1		±1/2	±1	LSB
Over Temperature			±1			±1	LSB
Resolution for No Missing Codes	12			12			Bits
Over Temperature	12			12			Bits
−Full-Scale Error		±1	±2		±1	±2	LSB
Over Temperature		±2	±8		±2	±13	LSB
+Full-Scale Error		±1	±2		±1	±2	LSB
Over Temperature		±2	±8		±2	±13	LSB
PSRR, $\pm V_S$		±1/2			±1/2		LSB/V
Dynamic Characteristics[1, 3]							
With Filter (f_C = 50 kHz)							
Signal-to-Noise Ratio, f_{IN} = 38.7 kHz	70	72		70	72		dB
Total Harmonic Distortion, f_{IN} = 38.7 kHz		−82	−72		−82	−72	dB
Intermodulation Distortion, f_{IN1} = 32.8 kHz & f_{IN2} = 34.3 kHz		−82	−72		−82	−72	dB
Without Filter							
Signal-to-Noise Ratio, f_{IN} = 60.9 kHz	70	72		70	72		dB
Total Harmonic Distortion, f_{IN} = 60.9 kHz		−78	−68		−78	−68	dB
Intermodulation Distortion, f_{IN1} = 58.7 kHz & f_{IN2} = 60.9 kHz		−78	−68		−78	−68	dB
Reference Voltage	−5.05		−4.95	−5.05		−4.95	V
Output Current	±1	±2		±1	±2		mA
Drift		±10	±30		±10	±30	ppm/°C

	AD1332BD			AD1332TD			
	Min	Typ	Max	Min	Typ	Max	Units
DIGITAL INPUTS[1]							
$\overline{RD}$, $\overline{WR}$, $\overline{CS}$, $\overline{RST}$, A0,							
D0–D11, PTC $\overline{ENB}$							
Input Voltage, Logic Low			+0.8			+0.8	V
Input Voltage, Logic High	+2.0			+2.25			V
Input Current			±200			±200	μA
SAMPLE IN, CLK IN							
Input Voltage, Logic Low			+1.5			+1.5	V
Input Voltage, Logic High	+3.5			+3.5			V
Input Current			±10			±10	μA
Input Capacitance		5			5		pF
$\overline{RST}$ LOW Pulse Width	10			10			ns
DIGITAL OUTPUTS[1]							
D0–D11, SAMPLE OUT							
Output Voltage, Logic Low[5]			+0.4			+0.4	V
Output Voltage, Logic High							
D0–D11[5]	+2.4			+2.4			V
SAMPLE OUT, I_{OH} = −0.4 mA	+4.0			+4.0			V
High Impedance Leakage Current			±200			±200	μA
$\overline{IRQ}$, PTC $\overline{ENB}$							
Output Voltage, Logic Low[5]			+0.4			+0.4	V
Off-State Leakage			±10			±10	μA
Output Capacitance		5			5		pF
$\overline{IRQ}$ LOW to D0–D11 Valid[4]			0			0	ns
POWER REQUIREMENTS							
Operating Range							
$\pm V_S$	±11.4		±15.75	±11.4		±15.75	V
V_{DD}	+4.75		+5.25	+4.75		+5.25	V
$+V_S$ Supply Current		50	57		50	57	mA
$-V_S$ Supply Current		48	57		48	57	mA
$+V_{DD}$ Supply Current		6	15		6	15	mA
Consumption							
$\pm V_S$ = ±12 V		1.2	1.4		1.2	1.4	W
$\pm V_S$ = ±15 V		1.5	1.75		1.5	1.75	W
TEMPERATURE RANGE							
Operating and Specified	−40		+85	−55		+125	°C
Storage	−65		+150	−65		+150	°C

NOTES
[1]Guaranteed over operating temperature range, tested at +25°C only.
[2]f_{CLK} = 2.5 MHz, SAMPLE IN connected to SAMPLE OUT, PTC $\overline{ENB}$ = Low.
[3]THD of harmonics 2-7 of the fundamental. SNR of fundamental less harmonics 2-7.
[4]$\overline{RD}$, $\overline{CS}$, A0 = "Low;" $\overline{WR}$, $\overline{RST}$ = "High."
[5]I_{OL} = 4 mA, I_{OH} = −4 mA for AD1332BD. I_{OL} = 3.2 mA, I_{OH} = −3.2 mA for AD1332TD.
Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD1332BD	−40°C to +85°C	DH-40A
AD1332TD/883B	−55°C to +125°C	DH-40A

*D = Hermetic Ceramic DIP. For outline information see Package Information section.

SWITCHING CHARACTERISTICS

(over operating temperature and power supply voltage range, with C_{OUT} = 30 pF or 100 pF except where noted)

Parameter	Description	Conditions	Min	Max	Units
READ CYCLE					
t_{RC}	Read Cycle Time	C_{OUT} = 30 pF	25		ns
		C_{OUT} = 100 pF	35		ns
t_A	Data Access Time	C_{OUT} = 30 pF		15	ns
		C_{OUT} = 100 pF		25	ns
		C_{OUT} = 150 pF		35	ns
t_{LZ}	Output Low Z Time		2		ns
t_{HZ}	Output High Z Time	C_{OUT} = 30 pF		15	ns
		C_{OUT} = 100 pF		25	ns
t_{OH}	Output Hold Time		2		ns
t_{A0RD}	A0 Valid to $\overline{RD}$ LOW		3		ns
t_{RDA0}	$\overline{RD}$ HIGH to A0 Invalid		3		ns
t_{A0CS}	A0 Valid to $\overline{CS}$ LOW		3		ns
t_{CSA0}	$\overline{CS}$ HIGH to A0 Invalid		3		ns
WRITE CYCLE					
t_{WC}	Write Cycle Time		15		ns
t_{WP}	Write Pulse Width		5		ns
t_{SU}	Data Setup Time		2		ns
t_{IH}	Input Hold Time		4		ns
t_{A0WR}	A0 Valid to $\overline{WR}$ LOW		3		ns
t_{WRA0}	$\overline{WR}$ HIGH to A0 Invalid		3		ns
t_{A0CS}	A0 Valid to $\overline{CS}$ LOW		3		ns
t_{CSA0}	$\overline{CS}$ HIGH to A0 Invalid		3		ns

NOTE
Specifications subject to change without notice.
Specifications are guaranteed but not tested.

ABSOLUTE MAXIMUM RATINGS*

$+V_S$ to APWR/ASIG GND . . . . . +18 V
$-V_S$ to APWR/ASIG GND . . . . . −18 V
V_{DD} to DGND . . . . . +7 V
APWR/ASIG GND to DGND . . . . . −0.3 V to +0.3 V
Analog Input to APWR/ASIG GND
S/H IN, FILTER IN, C1vg-C4vg . . . . . $-V_S$ to $+V_S$
Digital Input to APWR GND
SAMPLE IN, CLK IN . . . . . −0.3 V to +7 V
Digital Input to DGND
D0–D11, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, A0, $\overline{RST}$,
PTC $\overline{ENB}$ . . . . . −0.3 V to V_{DD} +0.3 V
Output Short Circuit Duration
FILTER OUT, REF OUT or C1wv-C4wv . . . . . Indefinite
Digital Output . . . . . 1 Output for 1 sec
Lead Temperature Range,
Soldering for 10 sec . . . . . +300°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.