Am29841A/Am29843A/Am29845A
Am29941A/Am29943A/Am29945A

High-Performance Bus Interface Latches

DISTINCTIVE CHARACTERISTICS

- High-speed parallel latches
  - transparent t_{PD} = 5.0 ns typical
- Buffered common latch enable, clear and preset input
- Three-state outputs glitch-free during power-up and down. Outputs have Schottky clamp to ground
- I_{OL}: 48 mA Commercial, 32 mA Military
- Higher speed, lower power versions of the Am29841, Am29843, and Am29845
- Am29900A DIP pinout option reduces lead inductance on V_{CC} and GND pins

GENERAL DESCRIPTION

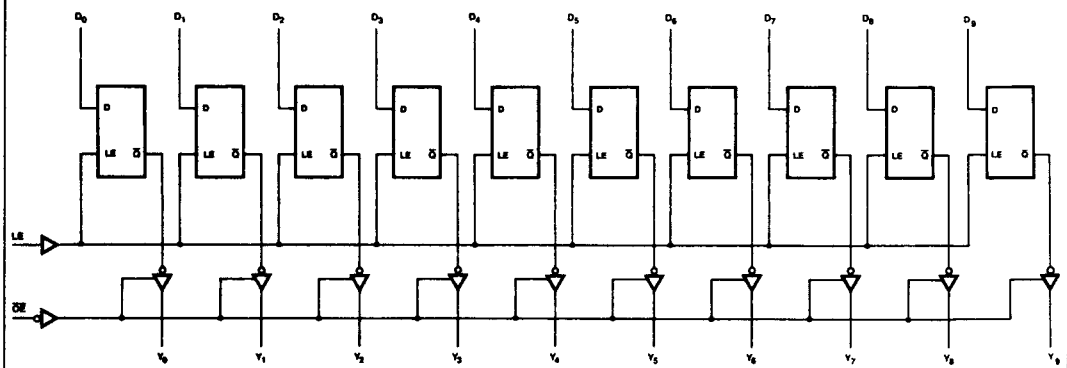
The Am29841A, Am29843A, and Am29845A Buffered Latches are designed to eliminate the extra devices required to buffer stand alone latches and to provide extra data width for wider address/data paths or buses carrying parity. The Am29800A latches are produced with AMD's exclusive IMOX* bipolar process, and feature typical propagation delays of 5 ns, as well as high-capacitive drive capability.

The Am29841A is a buffered, 10-bit version of the popular '373 function. The Am29843A is a 9-bit wide buffered latch with Preset ($\overline{PRE}$) and Clear ($\overline{CLR}$) — ideal for parity bus interfacing in high-performance microprogrammed systems. The Am29845A, an 8-bit buffered latch, has all the 9-bit controls, plus multiple enables ($\overline{OE_1}$, $\overline{OE_2}$, $\overline{OE_3}$), to allow multi-user control of the interface; e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$. The device is ideal for use as an output port requiring high I_{OL}/I_{OH}.

The Am29800A latches are available in the standard package options: DIPs, PLCCs, LCCs, SOICs, and Flatpacks. In addition, a DIP pinout option, featuring center V_{CC} and GND pins, reduces the lead inductance of the V_{CC} and GND pins. The ordering part numbers for latches with this pinout are the Am29941A, Am29943A, and Am29945A; their pinouts are shown later in this data sheet.

BLOCK DIAGRAMS**

Am29841A



BD001056

*IMOX is a trademark of Advanced Micro Devices, Inc.
**See following pages for additional Block Diagrams.

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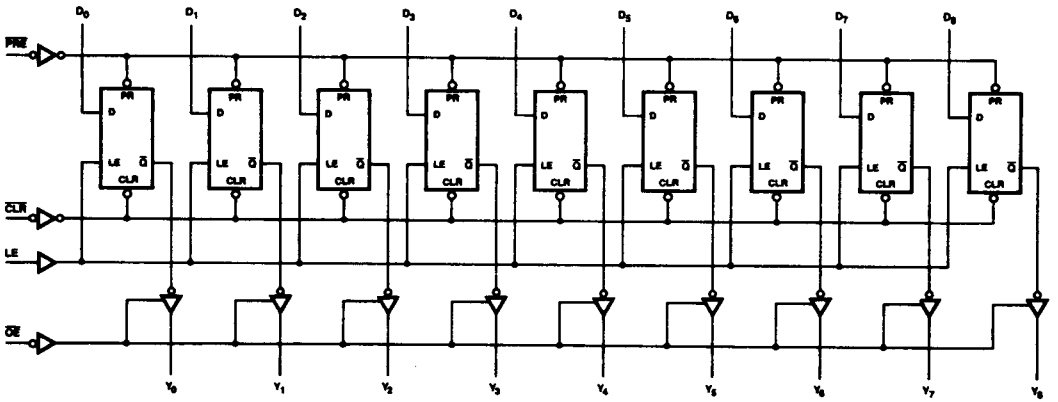
BLOCK DIAGRAMS (Cont'd.)

Am29843A



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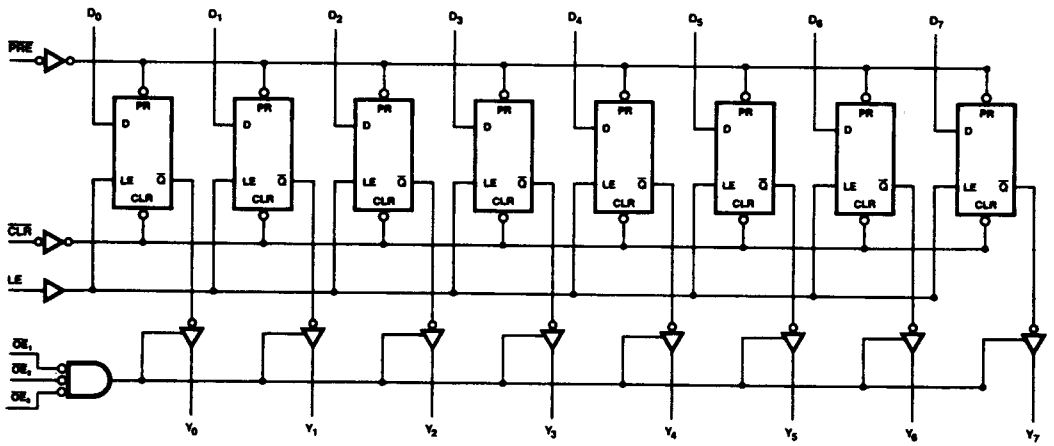
Am29845A



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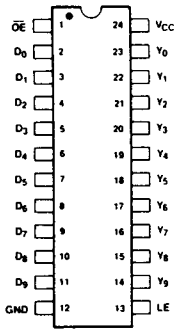
CONNECTION DIAGRAMS
Top View

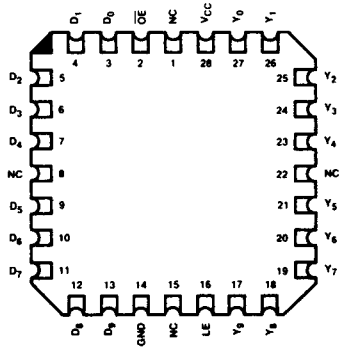
Am29841A

DIPs*



CD001380

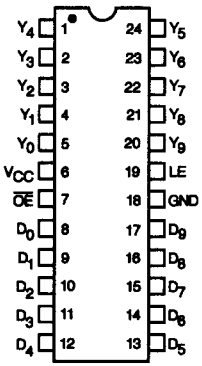
LCC**



CD001390

Am29941A

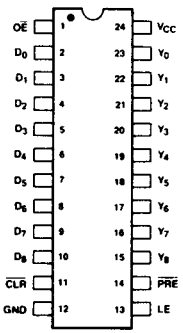
DIPs



CD010722

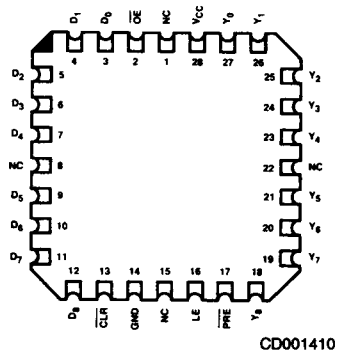
Am29843A

DIPs*



CD001400

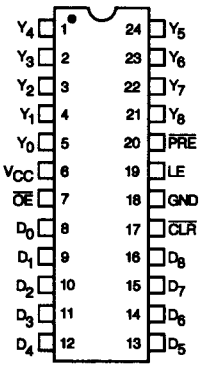
LCC**



CD001410

Am29943A

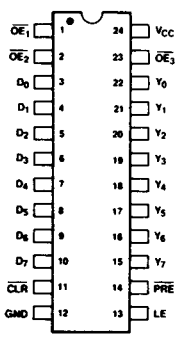
DIPs



CD010723

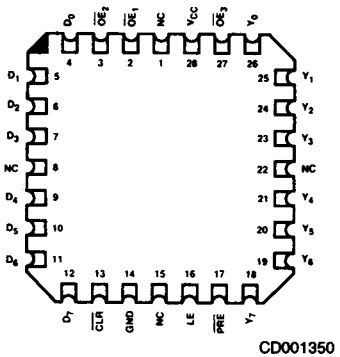
Am29845A

DIPs*



CD001340

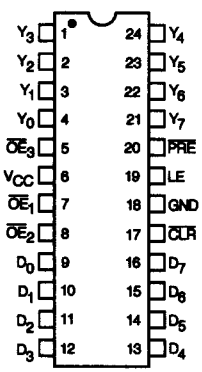
LCC**



CD001350

Am29945A

DIPs



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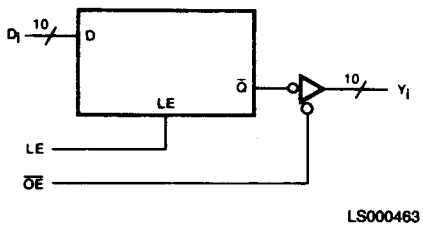
*Also available in 24-Pin Flatpack and Small Outline packages; pinout identical to DIPs.
**Also available in 28-Pin PLCC; pinout identical to LCC.

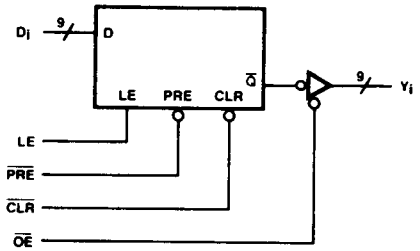
LOGIC SYMBOLS

Am29841A



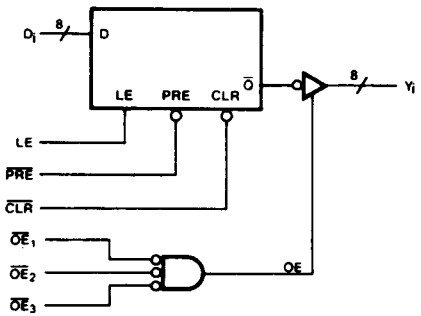
LS000463

Am29843A



LS000473

Am2985A



LS000443

FUNCTION TABLES

Am29841A

Inputs			Internal	Outputs	
$\overline{OE}$	LE	D_I	$\overline{Q}_I$	Y_I	Function
H	X	X	X	Z	Hi-Z
H	H	L	H	Z	Hi-Z
H	H	H	L	Z	Hi-Z
H	L	X	NC	Z	Latched (Hi-Z)
L	H	L	H	L	Transparent
L	H	H	L	H	Transparent
L	L	X	NC	NC	Latched

H = HIGH
L = LOW
X = Don't Care

NC = No Change
Z = High Impedance

FUNCTION TABLES (Cont'd.)

Am29843A

Inputs					Internal	Outputs	
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_I	$\overline{Q}_I$	Y_I	Function
H	H	H	X	X	X	Z	Hi-Z
H	H	H	H	L	H	Z	Hi-Z
H	H	H	H	H	L	Z	Hi-Z
H	H	H	L	X	NC	Z	Latched (Hi-Z)
H	H	L	H	L	H	L	Transparent
H	H	L	H	H	L	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	L	H	Preset
L	H	L	X	X	H	L	Clear
L	L	L	X	X	L	H	Preset
L	H	H	L	X	H	Z	Latched (Hi-Z)
H	L	H	L	X	L	Z	Latched (Hi-Z)

Am29845A

	Inputs				Internal	Outputs	
OE*	$\overline{CLR}$	$\overline{PRE}$	LE	D_I	$\overline{Q}_I$	Y_I	Function
L	H	H	X	X	X	Z	Hi-Z
L	H	H	H	L	H	Z	Hi-Z
L	H	H	H	H	L	Z	Hi-Z
L	H	H	L	X	NC	Z	Latched (Hi-Z)
H	H	H	H	L	H	L	Transparent
H	H	H	H	H	L	H	Transparent
H	H	H	L	X	NC	NC	Latched
H	H	L	X	X	L	H	Preset
H	L	H	X	X	H	L	Clear
H	L	L	X	X	L	H	Preset
L	L	H	L	X	H	Z	Latched (Hi-Z)
L	H	L	L	X	L	Z	Latched (Hi-Z)

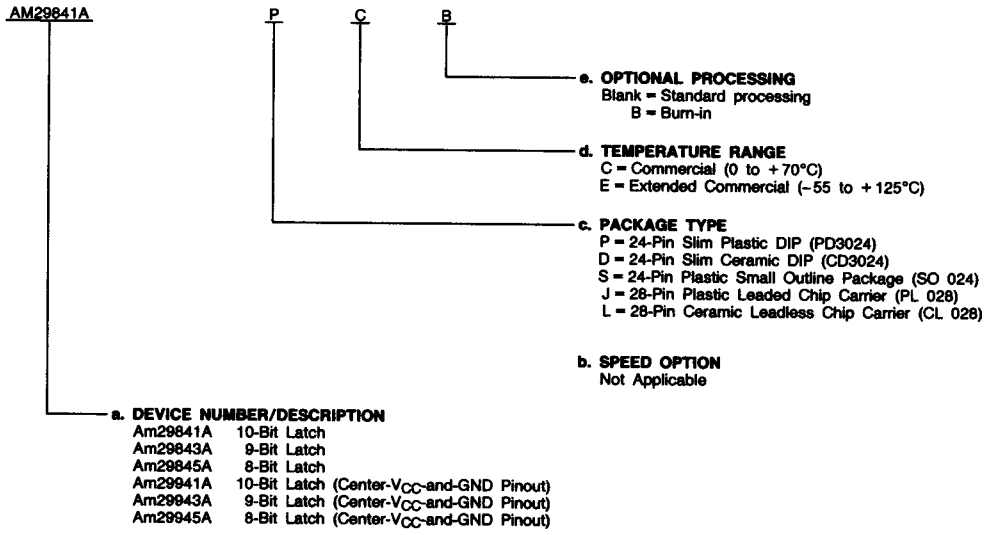
*OE is an Active HIGH internal signal produced as follows:

$\overline{OE}_1$	$\overline{OE}_2$	$\overline{OE}_3$	OE
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

H = HIGH
L = LOW
NC = No Change
Z = High Impedance
X = Don't Care

ORDERING INFORMATION
Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM29841A	PC, PCB, DC, DCB, DE, SC, JC, LC
AM29843A	
AM29845A	
AM29941A	PC, PCB, DC, DCB, DE
AM29943A	
AM29945A	

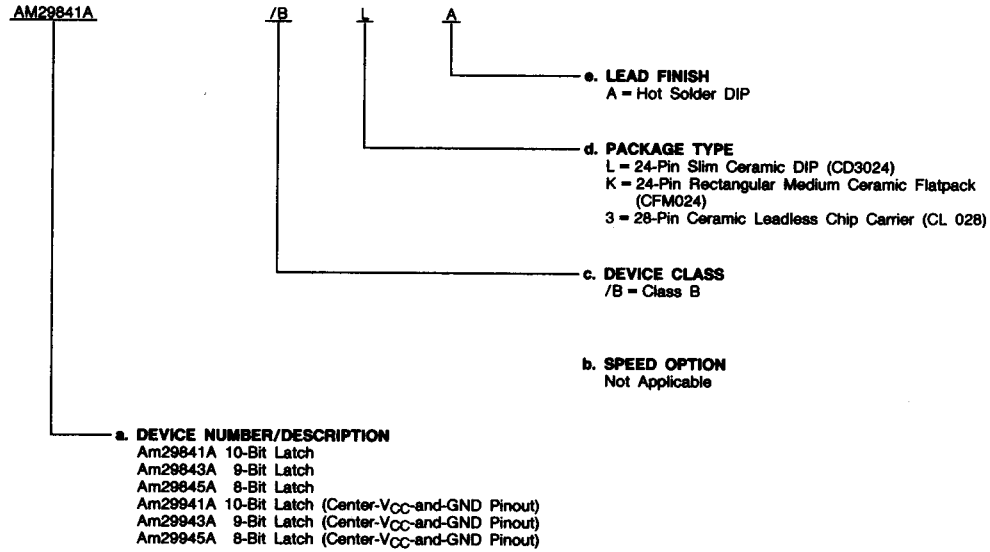
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM29841A	/BLA, /BKA, /B3A
AM29843A	
AM29845A	
AM29941A	/BLA
AM29943A	
AM29945A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

D_i Data Inputs (Input)
D_i are the latch data inputs.

Y_i Data Outputs (Output)
Y_i are the three-state data outputs.

LE Latch Enable (Input, Active HIGH)
The latches are transparent when LE is HIGH. Input data is latched on a HIGH-to-LOW transition.

Am29841A

$\overline{OE}$ Output Enable (Input, Active LOW)
When $\overline{OE}$ is LOW, the latch data is passed to the Y_i outputs. When $\overline{OE}$ is HIGH, the Y_i outputs are in the high-impedance state.

Am29843A

$\overline{OE}$ Output Enable (Input, Active LOW)
When $\overline{OE}$ is LOW, the latch data is passed to the Y_i outputs. When $\overline{OE}$ is HIGH, the Y_i outputs are in the high-impedance state.

$\overline{PRE}$ Preset (Input, Active LOW)
When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. $\overline{PRE}$ overrides the $\overline{CLR}$ pin. $\overline{PRE}$ will set the latch independent of the state of $\overline{OE}$.

$\overline{CLR}$ Clear (Input, Active LOW)
When $\overline{CLR}$ is LOW, the internal latch is cleared. When $\overline{CLR}$ is LOW, the outputs are LOW if $\overline{OE}$ is LOW and $\overline{PRE}$ is HIGH. When $\overline{CLR}$ is HIGH, data can be entered into the latch.

Am29845A

$\overline{OE}_i$ Output Enables (Input, Active LOW)
When $\overline{OE}_1$, $\overline{OE}_2$, and $\overline{OE}_3$ are all LOW, the latch data is passed to the Y_i outputs. If any or all $\overline{OE}_i$ are HIGH, the Y_i outputs are put in a high impedance state.

$\overline{PRE}$ Preset (Input, Active LOW)
When $\overline{PRE}$ is LOW, the outputs are HIGH if all $\overline{OE}_i$ are LOW. $\overline{PRE}$ overrides the $\overline{CLR}$ pin. $\overline{PRE}$ will set the latch independent of the state of $\overline{OE}$.

$\overline{CLR}$ Clear (Input, Active LOW)
When $\overline{CLR}$ is LOW, the internal latch is cleared. When $\overline{CLR}$ is LOW, the Y_i outputs are LOW if all $\overline{OE}_i$ are LOW and $\overline{PRE}$ is HIGH. When $\overline{CLR}$ is HIGH, data can be entered into the latch.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
for High Output State ..... −0.5 V to +5.5 V
DC Input Voltage ..... −1.5 V to +6.0 V
DC Output Current, into Outputs ..... 100 mA
DC Input Current ..... −30 mA to +5.0 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V

Military (M) and Extended Commercial (E) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15 mA	2.4		Volts
			I_{OH} = −24 mA	2.0		
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OL} = 32 mA		0.5	Volts
			COM'L, I_{OL} = 48 mA		0.5	
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 1)		2.0		Volts
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs (Note 1)			0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = 5.5 V, I_{IN} = −18 mA			−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = 5.5 V, V_{IN} = 0.4 V			−0.5	mA
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 2.7 V			50	µA
I_I	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 5.5 V			100	µA
I_{OZL}	Output Off-State Current (High Impedance)	V_{CC} = 5.5 V	V_O = 0.4 V		−50	µA
I_{OZH}			V_O = 2.7 V		50	
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_{OUT} = 0 V (Note 2)		−75	−250	mA
I_{OFF}	Bus Leakage Current	V_{CC} = 0 V, V_{OUT} = 2.9 V			100	µA
I_{CC}	Supply Current	V_{CC} = 5.5 V, Outputs Unloaded	Outputs LOW		97	mA
			Outputs HIGH		70	
			Outputs Hi-Z		81	

Notes: 1. Input thresholds are tested during DC parameter testing, and may be tested in combination with other DC parameters.
2. Not more than one output shorted at a time. Duration of the short-circuit test should not exceed one second.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

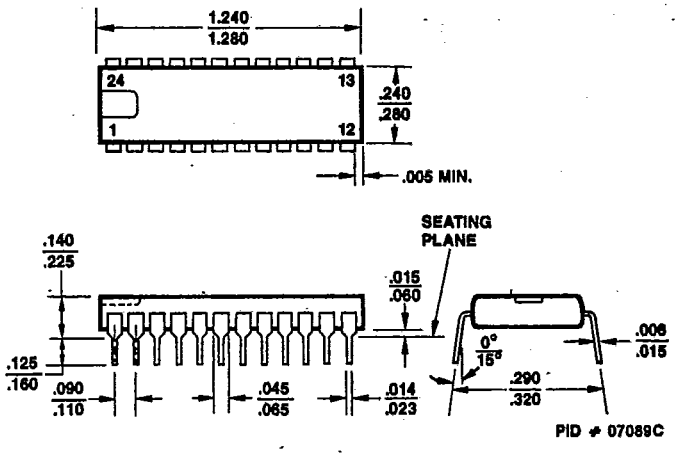
Parameter Symbol	Parameter Description		Test Conditions*	COMMERCIAL		MILITARY		Units
				Min.	Max.	Min.	Max.	
t_{PLH}	Data (D_i) to Output Y_i (LE = HIGH)		C_L = 50 pF R_1 = 500 Ω R_2 = 500 Ω		7		8.5	ns
t_{PHL}					9		10	ns
t_S	Data to LE Setup Time			2.5		3.5		ns
t_H	Data to LE Hold Time			2.5		3.5		ns
t_{PLH}	Latch Enable (LE) to Y_i				12		13	ns
t_{PHL}					12		13	ns
t_{PLH}	Propagation Delay, Preset to Y_i				12		14	ns
t_{PHL}					12		14	ns
t_{REC}	Preset ($\overline{PRE}$ ↓) to LE Setup Time			4		5		ns
t_{PLH}	Propagation Delay, Clear to Y_i				13		14	ns
t_{PHL}					13		14	ns
t_{REC}	Clear ($\overline{CLR}$ ↓) to LE Setup Time			7		8		ns
t_{PWH}	LE Pulse Width	HIGH		4		5		ns
t_{PWL}	Preset Pulse Width	LOW		5		7		ns
t_{PWL}	Clear Pulse Width	LOW		4		5		ns
t_{ZH}	Output Enable Time $\overline{OE}$ ↑ to Y_i				10.5		13.5	ns
t_{ZL}					11.5		14.5	ns
t_{HZ}	Output Disable Time $\overline{OE}$ ↓ to Y_i				8		10	ns
t_{LZ}					8		10	ns

*See Test Circuit and Waveforms.

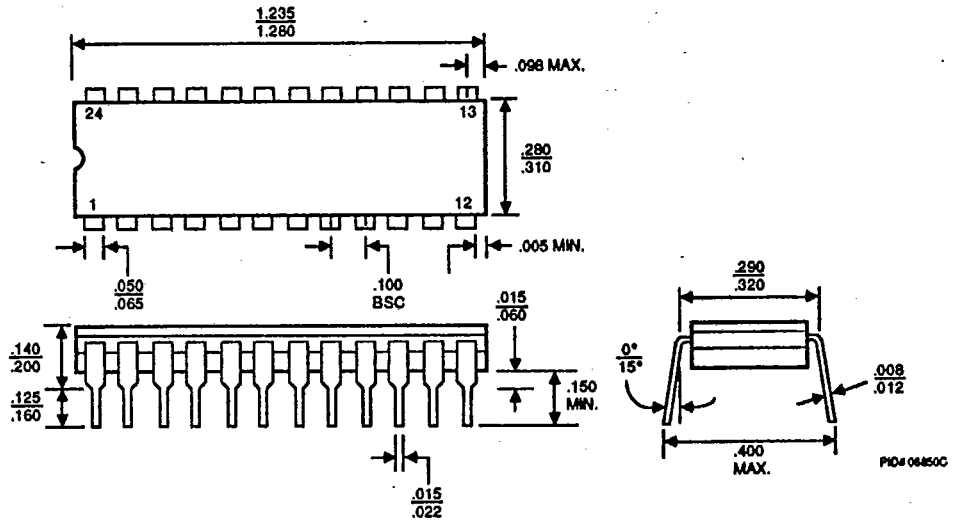
PACKAGE OUTLINES*

T-90-20

PD3024



CD3024

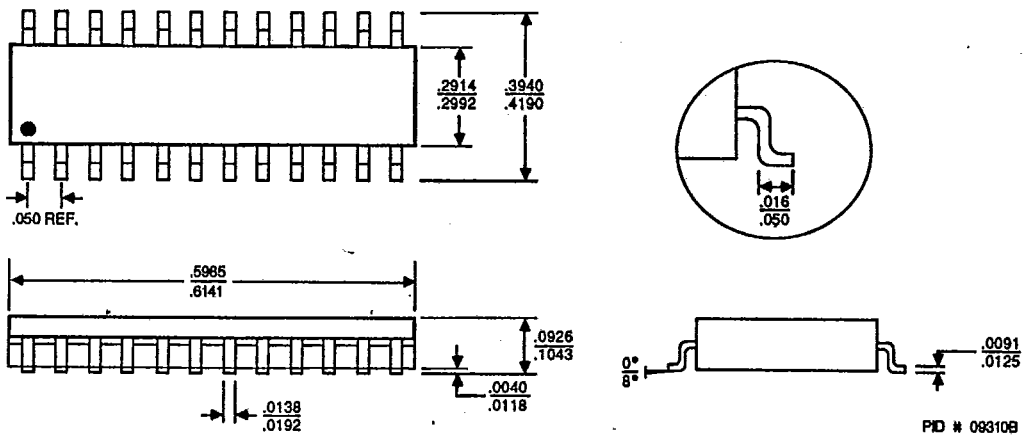


*For reference only.

PACKAGE OUTLINES (Cont'd.)

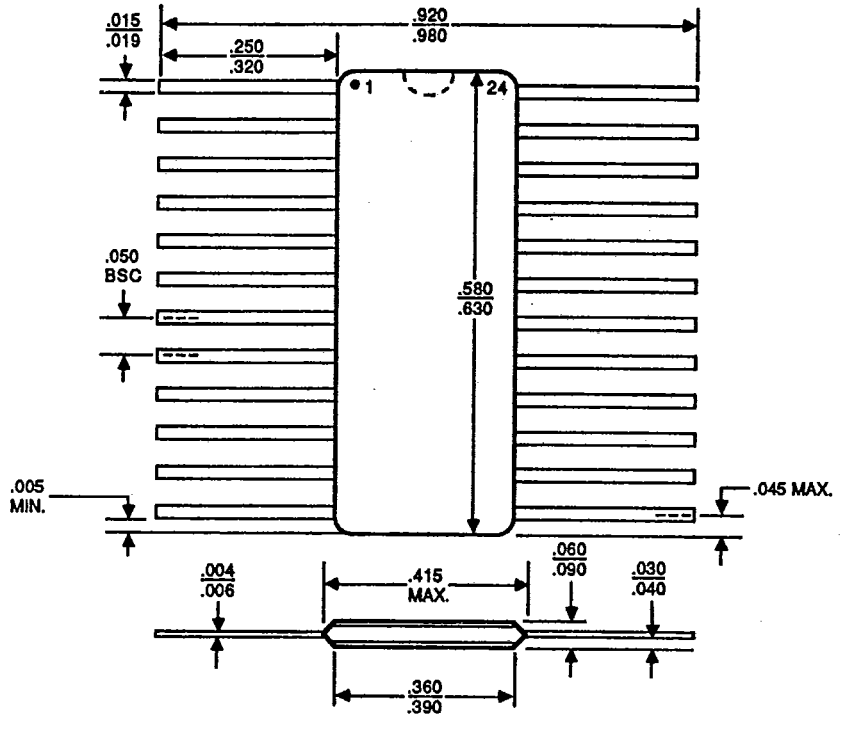
T-90-20

SO 024



PID # 09310B

CFM024

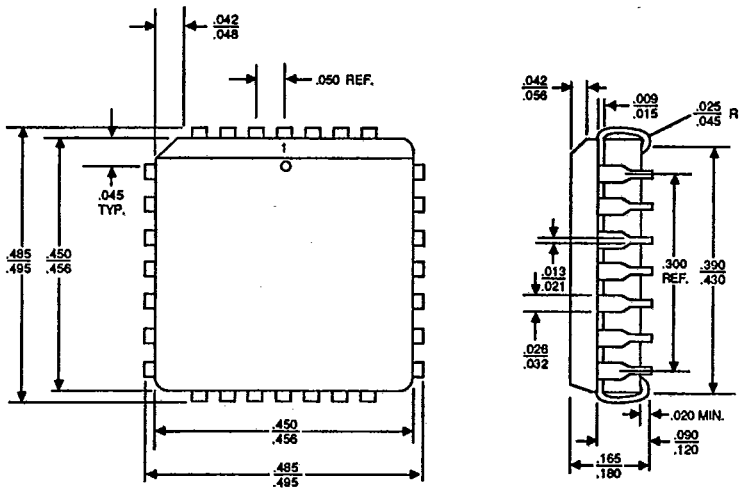


PID # 07371C

PACKAGE OUTLINES (Cont'd.)

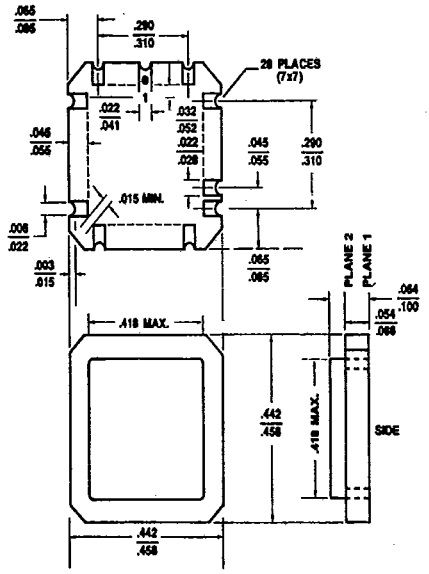
T-90-20

PL 028



PID # 06751E

CL 028



PID # 06595D

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