CY14B108K, CY14B108M

8-Mbit (1024 K × 8/512 K × 16) nvSRAM with Real Time Clock

Features

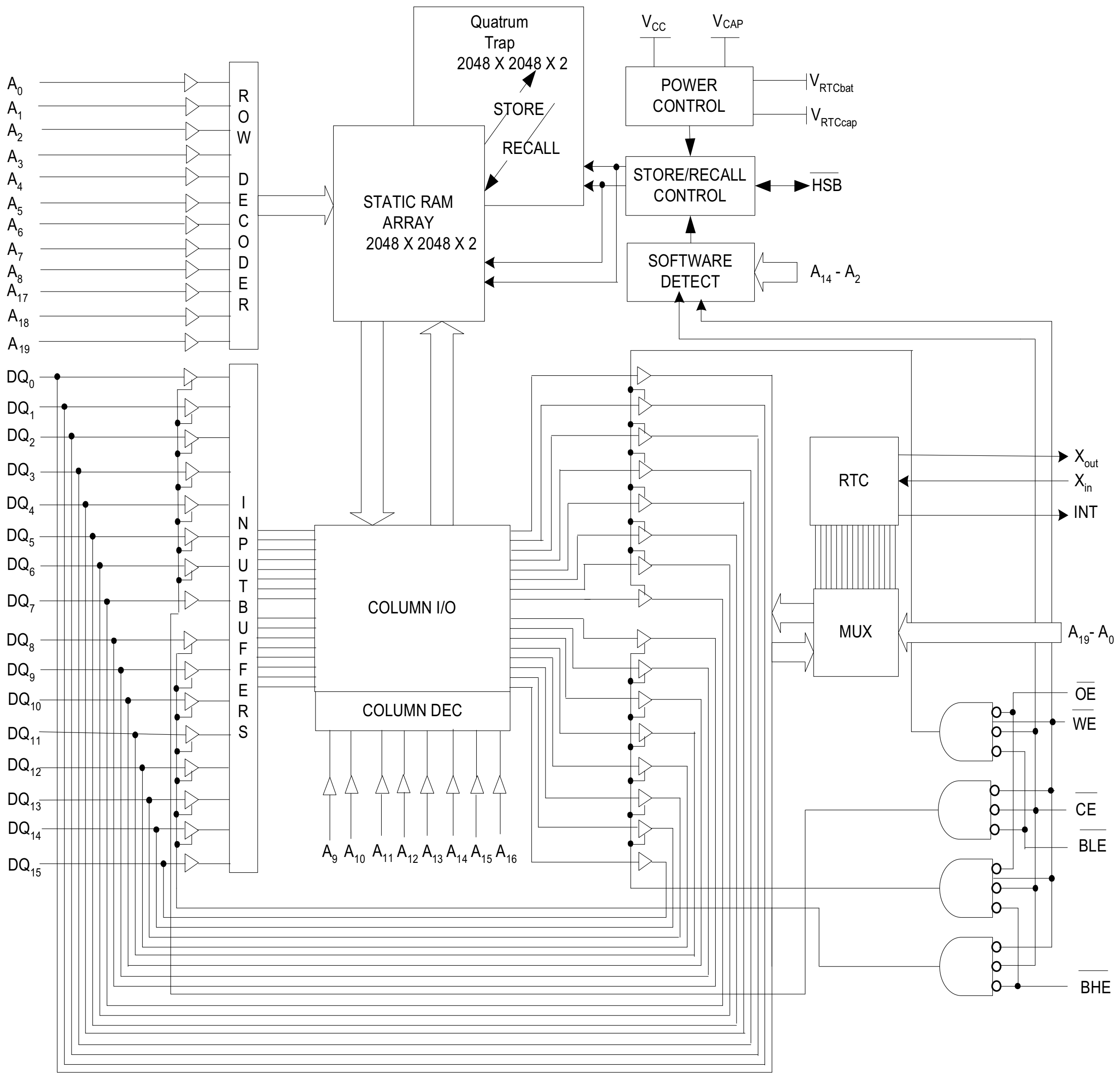
- 25 ns and 45 ns access times
- Internally organized as 1024 K × 8 (CY14B108K) or 512 K × 16 (CY14B108M)
- Hands off automatic STORE on power-down with only a small capacitor
- STORE to QuantumTrap nonvolatile elements is initiated by software, device pin, or AutoStore on power-down
- RECALL to SRAM initiated by software or power-up
- High reliability
- Infinite Read, Write, and RECALL cycles
- 1 million STORE cycles to QuantumTrap
- 20 year data retention
- Single 3 V +20%, –10% operation
- Data integrity of Cypress nonvolatile static RAM (nvSRAM) combined with full-featured real time clock (RTC)
- Watchdog timer
- Clock alarm with programmable interrupts
- Capacitor or battery backup for RTC
- Industrial temperature
- 44 and 54-pin thin small outline package (TSOP) Type II
- Pb-free and restriction of hazardous substances (RoHS) compliant

Functional Description

The Cypress CY14B108K/CY14B108M combines a 8-Mbit nonvolatile static RAM (nvSRAM) with a full featured RTC in a monolithic integrated circuit. The embedded nonvolatile elements incorporate QuantumTrap technology producing the world's most reliable nonvolatile memory. The SRAM is read and written infinite number of times, while independent nonvolatile data resides in the nonvolatile elements.

The RTC function provides an accurate clock with leap year tracking and a programmable, high accuracy oscillator. The alarm function is programmable for periodic minutes, hours, days, or months alarms. There is also a programmable watchdog timer for process control.

Logic Block Diagram [1, 2, 3]

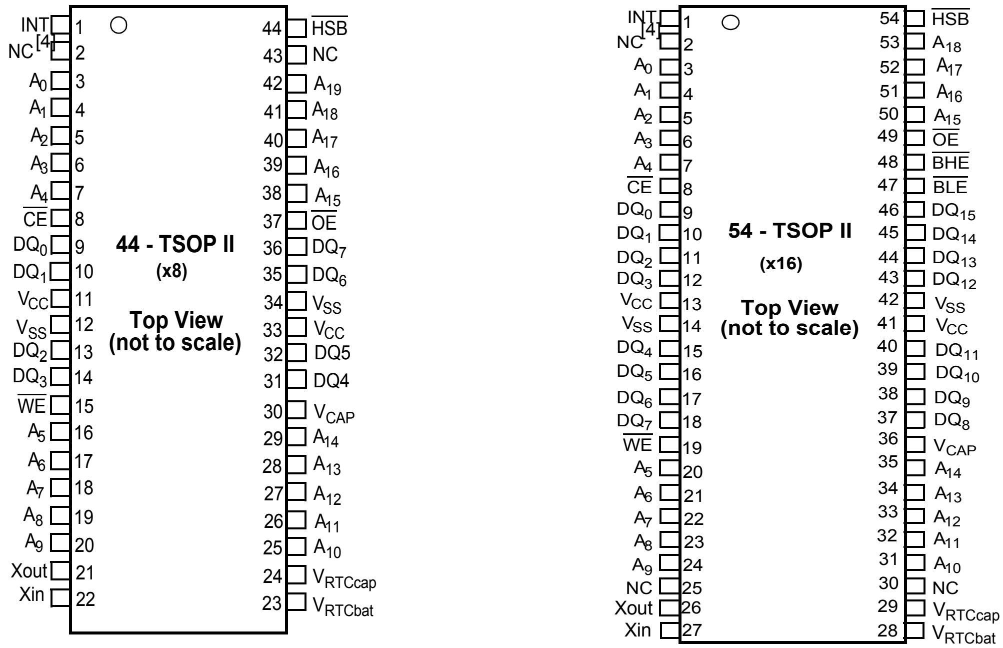


Notes
1. Address A_0–A_{19} for × 8 configuration and Address A_0–A_{18} for × 16 configuration.
2. Data DQ_0–DQ_7 for × 8 configuration and Data DQ_0–DQ_{15} for × 16 configuration.
3. BHE and BLE are applicable for × 16 configuration only.

Contents

Pinouts

Figure 1. Pin Diagram – 44-pln and 54-pin TSOP II



Note
4. Address expansion for 16-Mbit. NC pin not connected to die.

Pin Definitions

Pin Name	I/O Type	Description
A_0–A_{19}	Input	Address inputs. Used to select one of the 1,048,576 bytes of the nvSRAM for × 8 configuration.
A_0–A_{18}		Address inputs. Used to select one of the 524,288 words of the nvSRAM for × 16 configuration.
DQ_0–DQ_7	Input/Output	Bidirectional data I/O lines for × 8 configuration. Used as input or output lines depending on operation.
DQ_0–DQ_{15}		Bidirectional data I/O lines for × 16 configuration. Used as input or output lines depending on operation.
NC	No connect	No connects. This pin is not connected to the die.
$\overline{WE}$	Input	Write Enable input, Active LOW. When selected LOW, data on the I/O pins is written to the specific address location.
$\overline{CE}$	Input	Chip Enable input, Active LOW. When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{OE}$	Input	Output Enable, Active LOW. The active LOW $\overline{OE}$ input enables the data output buffers during read cycles. Deasserting $\overline{OE}$ HIGH causes the I/O pins to tristate.
$\overline{BHE}$	Input	Byte High Enable, Active LOW. Controls DQ_{15}–DQ_8.
$\overline{BLE}$	Input	Byte Low Enable, Active LOW. Controls DQ_7–DQ_0.
X_{out}	Output	Crystal connection. Drives crystal on start up.
X_{in}	Input	Crystal connection. For 32.768 kHz crystal.
V_{RTCcap}	Power supply	Capacitor supplied backup RTC supply voltage. Left unconnected if V_{RTCbat} is used.
V_{RTCbat}	Power supply	Battery supplied Backup RTC supply voltage. Left unconnected if V_{RTCcap} is used.
INT	Output	Interrupt output. Programmable to respond to the clock alarm, the watchdog timer, and the power monitor. Also programmable to either active HIGH (push or pull) or LOW (open drain).
V_{SS}	Ground	Ground for the device. Must be connected to ground of the system.
V_{CC}	Power supply	Power supply inputs to the device. 3.0 V +20%, –10%.
$\overline{HSB}$	Input/Output	Hardware STORE Busy ($\overline{HSB}$).When LOW this output indicates that a Hardware STORE is in progress. When pulled LOW external to the chip it initiates a nonvolatile STORE operation. After each Hardware and Software STORE operation, $\overline{HSB}$ is driven HIGH for a short time (t_{HHHD}) with standard output high current and then a weak internal pull-up resistor keeps this pin HIGH (external pull-up resistor connection optional).
V_{CAP}	Power supply	AutoStore capacitor. Supplies power to the nvSRAM during power loss to store data from SRAM to nonvolatile elements.

Device Operation

The CY14B108K/CY14B108M nvSRAM is made up of two functional components paired in the same physical cell. These are a SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Data in the SRAM is transferred to the nonvolatile cell (the STORE operation), or from the nonvolatile cell to the SRAM (the RECALL operation). Using this unique architecture, all cells are stored and recalled in parallel. During the STORE and RECALL operations SRAM read and write operations are inhibited. The CY14B108K/CY14B108M supports infinite reads and writes similar to a typical SRAM. In addition, it provides infinite RECALL operations from the nonvolatile cells and up to 1 million STORE operations. See Truth Table For SRAM Operations on page 27 for a complete description of read and write modes.

SRAM Read

The CY14B108K/CY14B108M performs a read cycle when $\overline{CE}$ and $\overline{OE}$ are LOW, and $\overline{WE}$ and $\overline{HSB}$ are HIGH. The address specified on pins A_{0-19} or A_{0-18} determines which of the 1,048,576 data bytes or 524,288 words of 16 bits each are accessed. Byte enables ($\overline{BHE}$, $\overline{BLE}$) determine which bytes are enabled to the output, in the case of 16-bit words. When the read is initiated by an address transition, the outputs are valid after a delay of t_{AA} (read cycle 1). If the read is initiated by $\overline{CE}$ or $\overline{OE}$, the outputs are valid at t_{ACE} or at t_{DOE}, whichever is later (read cycle 2). The data output repeatedly responds to address changes within the t_{AA} access time without the need for transitions on any control input pins. This remains valid until another address change or until $\overline{CE}$ or $\overline{OE}$ is brought HIGH, or $\overline{WE}$ or $\overline{HSB}$ is brought LOW.

SRAM Write

A write cycle is performed when $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{HSB}$ is HIGH. The address inputs must be stable before entering the write cycle and must remain stable until $\overline{CE}$ or $\overline{WE}$ goes HIGH at the end of the cycle. The data on the common I/O pins DO_{0-15} are written into the memory if it is valid for t_{SD} time before the end of a $\overline{WE}$ controlled write or before the end of an $\overline{CE}$ controlled write. The Byte Enable inputs ($\overline{BHE}$, $\overline{BLE}$) determine which bytes are written, in the case of 16-bit words. Keep $\overline{OE}$ HIGH during the entire write cycle to avoid data bus contention on common I/O lines. If $\overline{OE}$ is left LOW, internal circuitry turns off the output buffers t_{HZWE} after $\overline{WE}$ goes LOW.

AutoStore Operation

The CY14B108K/CY14B108M stores data to the nvSRAM using one of three storage operations. These three operations are: Hardware STORE, activated by the $\overline{HSB}$; Software STORE, activated by an address sequence; AutoStore, on device power-down. The AutoStore operation is a unique feature of QuantumTrap technology and is enabled by default on the CY14B108K/CY14B108M.

During a normal operation, the device draws current from V_{CC} to charge a capacitor connected to the V_{CAP} pin. This stored charge is used by the chip to perform a single STORE operation. If the voltage on the V_{CC} pin drops below V_{SWITCH}, the part automatically disconnects the V_{CAP} pin from V_{CC}. A STORE operation is initiated with power provided by the V_{CAP} capacitor.

Note If the capacitor is not connected to V_{CAP} pin, AutoStore must be disabled using the soft sequence specified in Preventing AutoStore on page 8. In case AutoStore is enabled without a capacitor on V_{CAP} pin, the device attempts an AutoStore operation without sufficient charge to complete the Store. This corrupts the data stored in nvSRAM.

Figure 2. AutoStore Mode

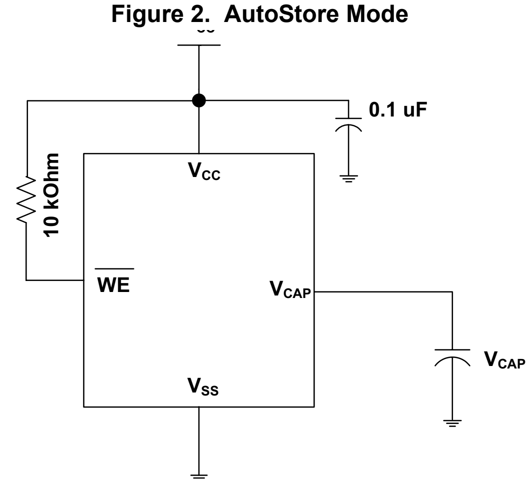


Figure 2 shows the proper connection of the storage capacitor (V_{CAP}) for automatic STORE operation. Refer to DC Electrical Characteristics on page 18 for the size of the V_{CAP}. The voltage on the V_{CAP} pin is driven to V_{CC} by a regulator on the chip. A pull-up should be placed on $\overline{WE}$ to hold it inactive during power-up. This pull-up is effective only if the $\overline{WE}$ signal is tristate during power-up. Many MPUs tristate their controls on power-up. This should be verified when using the pull-up. When the nvSRAM comes out of power-on-RECALL, the MPU must be active or the $\overline{WE}$ held inactive until the MPU comes out of reset.

To reduce unnecessary nonvolatile STOREs, AutoStore, and Hardware STORE operations are ignored unless at least one write operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a write operation has taken place. The $\overline{HSB}$ signal is monitored by the system to detect if an AutoStore cycle is in progress.

Hardware STORE (HSB) Operation

The CY14B108K/CY14B108M provides the HSB pin to control and acknowledge the STORE operations. The HSB pin is used to request a Hardware STORE cycle. When the HSB pin is driven LOW, the CY14B108K/CY14B108M conditionally initiates a STORE operation after t_{DELAY}. An actual STORE cycle begins only if a write to the SRAM has taken place since the last STORE or RECALL cycle. The HSB pin also acts as an open drain driver (internal 100 kΩ weak pull-up resistor) that is internally driven LOW to indicate a busy condition when the STORE (initiated by any means) is in progress.

Note After each Hardware and Software STORE operation HSB is driven HIGH for a short time (t_{HHHD}) with standard output high current and then remains HIGH by internal 100 kΩ pull-up resistor.

SRAM write operations that are in progress when HSB is driven LOW by any means are given time (t_{DELAY}) to complete before the STORE operation is initiated. However, any SRAM write cycles requested after HSB goes LOW are inhibited until HSB returns HIGH. In case the write latch is not set, HSB is not driven LOW by the CY14B108K/CY14B108M. But any SRAM read and write cycles are inhibited until HSB is returned HIGH by MPU or other external source.

During any STORE operation, regardless of how it is initiated, the CY14B108K/CY14B108M continues to drive the HSB pin LOW, releasing it only when the STORE is complete. Upon completion of the STORE operation, the nvSRAM memory access is inhibited for t_{LZHSB} time after HSB pin returns HIGH. Leave the HSB unconnected if it is not used.

Hardware RECALL (Power-Up)

During power-up or after any low power condition (V_{CC}< V_{SWITCH}), an internal RECALL request is latched. When V_{CC} again exceeds the V_{SWITCH} on powerup, a RECALL cycle is automatically initiated and takes $t_{HRECALL}$ to complete. During this time, the HSB pin is driven LOW by the HSB driver and all reads and writes to nvSRAM are inhibited.

Software STORE

Data is transferred from the SRAM to the nonvolatile memory by a software address sequence. The CY14B108K/CY14B108M Software STORE cycle is initiated by executing sequential CE or OE controlled read cycles from six specific address locations in exact order. During the STORE cycle, an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. After a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of reads from specific addresses is used for STORE initiation, it is important that no other read or write accesses intervene in the sequence, or the sequence is aborted and no STORE or RECALL takes place.

To initiate the Software STORE cycle, the following read sequence must be performed:

1. Read address 0x4E38 Valid READ
2. Read address 0xB1C7 Valid READ
3. Read address 0x83E0 Valid READ
4. Read address 0x7C1F Valid READ
5. Read address 0x703F Valid READ
6. Read address 0x8FC0 Initiate STORE cycle

The software sequence may be clocked with CE controlled reads or OE controlled reads, with WE kept HIGH for all the six READ sequences. After the sixth address in the sequence is entered, the STORE cycle commences and the chip is disabled. HSB is driven LOW. After the t_{STORE} cycle time is fulfilled, the SRAM is activated again for the read and write operation.

Software RECALL

Data is transferred from the nonvolatile memory to the SRAM by a software address sequence. A software RECALL cycle is initiated with a sequence of read operations in a manner similar to the Software STORE initiation. To initiate the RECALL cycle, perform the following sequence of CE or OE controlled read operations:

1. Read address 0x4E38 Valid READ
2. Read address 0xB1C7 Valid READ
3. Read address 0x83E0 Valid READ
4. Read address 0x7C1F Valid READ
5. Read address 0x703F Valid READ
6. Read address 0x4C63 Initiate RECALL cycle

Internally, RECALL is a two step procedure. First, the SRAM data is cleared; then, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time, the SRAM is again ready for read and write operations. The RECALL operation does not alter the data in the nonvolatile elements.

Table 1. Mode Selection

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$, $\overline{BLE}$[5]	A_{15}–A_0[6]	Mode	I/O	Power
H	X	X	X	X	Not selected	Output High Z	Standby
L	H	L	L	X	Read SRAM	Output data	Active
L	L	X	L	X	Write SRAM	Input data	Active
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8B45	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Disable	Output data Output data Output data Output data Output data Output data	Active[7]
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4B46	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Enable	Output data Output data Output data Output data Output data Output data	Active[7]
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8FC0	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile STORE	Output data Output data Output data Output data Output data Output High Z	Active I_{CC2}[7]
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4C63	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile RECALL	Output data Output data Output data Output data Output data Output High Z	Active[7]

Preventing AutoStore

The AutoStore function is disabled by initiating an AutoStore disable sequence. A sequence of read operations is performed in a manner similar to the Software STORE initiation. To initiate the AutoStore disable sequence, the following sequence of $\overline{CE}$ or $\overline{OE}$ controlled read operations must be performed:

1. Read address 0x4E38 Valid READ
2. Read address 0xB1C7 Valid READ
3. Read address 0x83E0 Valid READ
4. Read address 0x7C1F Valid READ
5. Read address 0x703F Valid READ
6. Read address 0x8B45 AutoStore Disable

AutoStore is re-enabled by initiating an AutoStore enable sequence. A sequence of read operations is performed in a manner similar to the software RECALL initiation. To initiate the AutoStore enable sequence, the following sequence of $\overline{CE}$ or $\overline{OE}$ controlled read operations must be performed:

1. Read address 0x4E38 Valid READ
2. Read address 0xB1C7 Valid READ
3. Read address 0x83E0 Valid READ
4. Read address 0x7C1F Valid READ
5. Read address 0x703F Valid READ
6. Read address 0x4B46 AutoStore Enable

If the AutoStore function is disabled or re-enabled, a manual STORE operation (hardware or software) must be issued to save the AutoStore state through subsequent power-down cycles. The part comes from the factory with AutoStore enabled.

Notes

5. $\overline{BHE}$ and $\overline{BLE}$ are applicable for × 16 configuration only.
6. While there are 20 address lines on the CY14B108K (19 address lines on the CY14B108M), only the 13 address lines (A_{14}–A_2) are used to control software modes. The remaining address lines are don't care.
7. The six consecutive address locations must be in the order listed. $\overline{WE}$ must be HIGH during all six cycles to enable a nonvolatile cycle.

Data Protection

The CY14B108K/CY14B108M protects data from corruption during low voltage conditions by inhibiting all externally initiated STORE and write operations. The low voltage condition is detected when V_{CC} is less than V_{SWITCH}. If the CY14B108K/CY14B108M is in a write mode (both CE and WE are LOW) at power-up, after a RECALL or STORE, the write is inhibited until the SRAM is enabled after t_{LZHSB} (HSB to output active). This protects against inadvertent writes during power-up or brown out conditions.

Noise Considerations

Refer to CY application note AN1064.

Real Time Clock Operation

nvTime Operation

The CY14B108K/CY14B108M offers internal registers that contain clock, alarm, watchdog, interrupt, and control functions. RTC registers use the last 16 address locations of the SRAM. Internal double buffering of the clock and timer information registers prevents accessing transitional internal clock data during a read or write operation. Double buffering also circumvents disrupting normal timing counts or the clock accuracy of the internal clock when accessing clock data. Clock and alarm registers store data in BCD format.

RTC functionality is described with respect to CY14B108K in the following sections. The same description applies to CY14B108M, except for the RTC register addresses. The RTC register addresses for CY14B108K range from 0xFFFF0 to 0xFFFFF, while those for CY14B108M range from 0x7FFF0 to 0x7FFFF. Refer to Table 3 on page 13 and Table 4 on page 14 for a detailed Register Map description.

Clock Operations

The clock registers maintain time up to 9,999 years in one second increments. The time can be set to any calendar time and the clock automatically keeps track of days of the week and month, leap years, and century transitions. There are eight registers dedicated to the clock functions, which are used to set time with a write cycle and to read time during a read cycle. These registers contain the time of day in BCD format. Bits defined as ‘0’ are currently not used and are reserved for future use by Cypress.

Reading the Clock

The double buffered RTC register structure reduces the chance of reading incorrect data from the clock. The user must stop internal updates to the CY14B108K time keeping registers before reading clock data, to prevent reading of data in transition. Stopping the register updates does not affect clock accuracy.

The updating process is stopped by writing a ‘1’ to the read bit ‘R’ (in the flags register at 0xFFFF0), and does not restart until a ‘0’ is written to the read bit. The RTC registers are then read while the internal clock continues to run. After a ‘0’ is written to the read bit (‘R’), all RTC registers are simultaneously updated within 20 ms

Setting the Clock

Setting the write bit ‘W’ (in the flags register at 0xFFFF0) to a ‘1’ stops updates to the time keeping registers and enables the time to be set. The correct day, date, and time is then written into the registers and must be in 24 hour BCD format. The time written is referred to as the “Base Time”. This value is stored in nonvolatile registers and used in the calculation of the current time. Resetting the write bit to ‘0’ transfers the values of timekeeping registers to the actual clock counters, after which the clock resumes normal operation.

If the time written to the timekeeping registers is not in the correct BCD format, each invalid nibble of the RTC registers continue counting to 0xF before rolling over to 0x0 after which RTC resumes normal operation.

Note After ‘W’ bit is set to 0, values written into the timekeeping, alarm, calibration, and interrupt registers are transferred to the RTC time keeping counters in t_{RTCp} time. These counter values must be saved to nonvolatile memory either by initiating a Software/Hardware STORE or AutoStore operation. While working in AutoStore disabled mode, perform a STORE operation after t_{RTCp} time while writing into the RTC registers for the modifications to be correctly recorded.

Backup Power

The RTC in the CY14B108K is intended for permanently powered operation. The V_{RTCcap} or V_{RTCbat} pin is connected depending on whether a capacitor or battery is chosen for the application. When the primary power, V_{CC}, fails and drops below V_{SWITCH} the device switches to the backup power supply.

The clock oscillator uses very little current, which maximizes the backup time available from the backup source. Regardless of the clock operation with the primary source removed, the data stored in the nvSRAM is secure, having been stored in the nonvolatile elements when power was lost.

During backup operation, the CY14B108K consumes 0.35 µA (Typical) at room temperature. User must choose capacitor or battery values according to the application.

Backup time values based on maximum current specifications are shown in the following table. Nominal backup times are approximately two times longer.

Table 2. RTC Backup Time

Capacitor Value	Backup Time
0.1 F	72 hours
0.47 F	14 days
1.0 F	30 days

Using a capacitor has the obvious advantage of recharging the backup source each time the system is powered up. If a battery is used, a 3 V lithium is recommended and the CY14B108K sources current only from the battery when the primary power is removed. However, the battery is not recharged at any time by the CY14B108K. The battery capacity must be chosen for total anticipated cumulative down time required over the life of the system.

Stopping and Starting the Oscillator

The OSCEN bit in the calibration register at 0xFFFF8 controls the enable and disable of the oscillator. This bit is nonvolatile and is shipped to customers in the “enabled” (set to ‘0’) state. To preserve the battery life when the system is in storage, OSCEN must be set to ‘1’. This turns off the oscillator circuit, extending the battery life. If the OSCEN bit goes from disabled to enabled, it takes approximately one second (two seconds maximum) for the oscillator to start.

While system power is off, if the voltage on the backup supply (V_{RTCcap} or V_{RTCbat}) falls below their respective minimum level, the oscillator may fail.The CY14B108K has the ability to detect oscillator failure when system power is restored. This is recorded in the Oscillator fail bit (OSCF) of the flags register at the address 0xFFFF0. When the device is powered on (V_{CC} goes above V_{SWITCH}) the OSCEN bit is checked for “enabled” status. If the OSCEN bit is enabled and the oscillator is not active within the first 5 ms, the OSCF bit is set to ‘1’. The system must check for this condition and then write ‘0’ to clear the flag. Note that in addition to setting the OSCF flag bit, the time registers are reset to the “Base Time” (see Setting the Clock on page 9), which is the value last written to the timekeeping registers. The control or calibration registers and the OSCEN bit are not affected by the ‘oscillator failed’ condition.

The value of OSCF must be reset to ‘0’ when the time registers are written for the first time. This initializes the state of this bit which may have become set when the system was first powered on.

To reset OSCF, set the write bit ‘W’ (in the flags register at 0xFFFF0) to a ‘1’ to enable writes to the Flag register. Write a ‘0’ to the OSCF bit and then reset the write bit to ‘0’ to disable writes.

Calibrating the Clock

The RTC is driven by a quartz controlled crystal with a nominal frequency of 32.768 kHz. Clock accuracy depends on the quality of the crystal and calibration. The crystals available in market typically have an error of $\pm$20 ppm to $\pm$35 ppm. However, CY14B108K employs a calibration circuit that improves the accuracy to +1/–2 ppm at 25 °C. This implies an error of +2.5 seconds to –5 seconds per month.

The calibration circuit adds or subtracts counts from the oscillator divider circuit to achieve this accuracy. The number of pulses that are suppressed (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five calibration bits found in calibration register at 0xFFFF8. The calibration bits occupy the five lower order bits in the calibration register. These bits are set to represent any value between ‘0’ and 31 in binary form. Bit D5 is a sign bit, where a ‘1’ indicates positive calibration and a ‘0’ indicates negative calibration. Adding counts speeds the clock up and subtracting counts slows the clock down. If a binary ‘1’ is loaded into the register, it corresponds to an adjustment of 4.068 or –2.034 ppm offset in oscillator error, depending on the sign.

Calibration occurs within a 64-minute cycle. The first 62 minutes in the cycle may, once per minute, have one second shortened by 128 or lengthened by 256 oscillator cycles. If a binary ‘1’ is loaded into the register, only the first two minutes of the 64-minute cycle are modified. If a binary 6 is loaded, the first 12 are affected, and so on. Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is, 4.068 or –2.034 ppm of adjustment per calibration step in the calibration register.

To determine the required calibration, the CAL bit in the flags register (0xFFFF0) must be set to ‘1’. This causes the INT pin to toggle at a nominal frequency of 512 Hz. Any deviation measured from the 512 Hz indicates the degree and direction of the required correction. For example, a reading of 512.01024 Hz indicates a +20 ppm error. Hence, a decimal value of –10 (001010b) must be loaded into the calibration register to offset this error.

Note Setting or changing the calibration register does not affect the test output frequency.

To set or clear CAL, set the write bit ‘W’ (in the flags register at 0xFFFF0) to ‘1’ to enable writes to the flags register. Write a value to CAL, and then reset the write bit to ‘0’to disable writes.

Alarm

The alarm function compares user programmed values of alarm time and date (stored in the registers 0xFFFF1-5) with the corresponding time of day and date values. When a match occurs, the alarm internal flag (AF) is set and an interrupt is generated on INT pin if alarm interrupt enable (AIE) bit is set.

There are four alarm match fields - date, hours, minutes, and seconds. Each of these fields has a match bit that is used to determine if the field is used in the alarm match logic. Setting the match bit to ‘0’ indicates that the corresponding field is used in the match process. Depending on the match bits, the alarm occurs as specifically as once a month or as frequently as once every minute. Selecting none of the match bits (all 1s) indicates that no match is required and therefore, alarm is disabled. Selecting all match bits (all 0s) causes an exact time and date match.

There are two ways to detect an alarm event: by reading the AF flag or monitoring the INT pin. The AF flag in the flags register at 0xFFFF0 indicates that a date or time match has occurred. The AF bit is set to ‘1’ when a match occurs. Reading the flags register clears the alarm flag bit (and all others). A hardware interrupt pin may also be used to detect an alarm event.

To set, clear or enable an alarm, set the ‘W’ bit (in flags register - 0xFFFF0) to ‘1’ to enable writes to alarm registers. After writing the alarm value, clear the ‘W’ bit back to ‘0’ for the changes to take effect.

Note CY14B108K requires the alarm match bit for seconds (0xFFFF2–D7) to be set to ‘0’ for proper operation of alarm flag and Interrupt.

Watchdog Timer

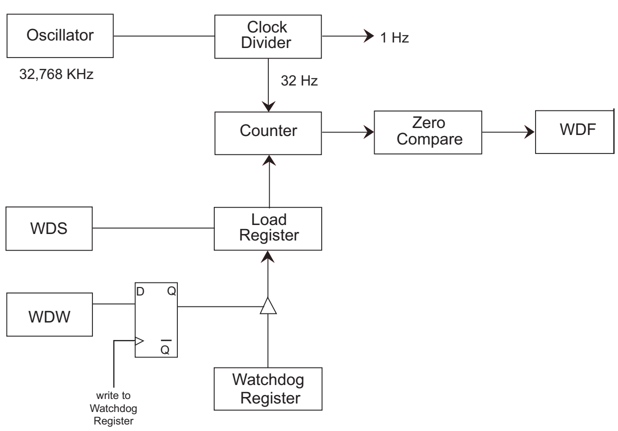
The watchdog timer is a free running down counter that uses the 32 Hz clock (31.25 ms) derived from the crystal oscillator. The oscillator must be running for the watchdog to function. It begins counting down from the value loaded in the watchdog timer register.

The timer consists of a loadable register and a free running counter. On power-up, the watchdog time out value in register 0xFFFF7 is loaded into the counter load register. Counting begins on power-up and restarts from the loadable value any time the watchdog strobe (WDS) bit is set to ‘1’. The counter is compared to the terminal value of ‘0’. If the counter reaches this value, it causes an internal flag and an optional interrupt output. You can prevent the time out interrupt by setting WDS bit to ‘1’ prior to the counter reaching '0'. This causes the counter to reload with the watchdog time out value and to be restarted. As long as the user sets the WDS bit prior to the counter reaching the terminal value, the interrupt and WDT flag never occur.

New time out values are written by setting the watchdog write bit to '0'. When the WDW is '0', new writes to the watchdog time out value bits D5-D0 are enabled to modify the time out value. When WDW is '1', writes to bits D5–D0 are ignored. The WDW function enables a user to set the WDS bit without concern that the watchdog timer value is modified. A logical diagram of the watchdog timer is shown in Figure 3. Note that setting the watchdog time out value to '0' disables the watchdog function.

The output of the watchdog timer is the flag bit WDF that is set if the watchdog is allowed to time out. If the watchdog interrupt enable (WIE) bit in the interrupt register is set, a hardware interrupt on INT pin is also generated on watchdog timeout. The flag and the hardware interrupt are both cleared when user reads the flags registers.

Figure 3. Watchdog Timer Block Diagram



Power Monitor

The CY14B108K provides a power management scheme with power fail interrupt capability. It also controls the internal switch to backup power for the clock and protects the memory from low V_{CC} access. The power monitor is based on an internal band gap reference circuit that compares the V_{CC} voltage to V_{SWITCH} threshold.

As described in the section AutoStore Operation on page 6, when V_{SWITCH} is reached as V_{CC} decays from power loss, a data STORE operation is initiated from SRAM to the nonvolatile elements, securing the last SRAM data state. Power is also switched from V_{CC} to the backup supply (battery or capacitor) to operate the RTC oscillator.

When operating from the backup source, read and write operations to nvSRAM are inhibited and the RTC functions are not available to the user. The RTC clock continues to operate in the background. The updated RTC time keeping registers data are available to the user after V_{CC} is restored to the device (see AutoStore/Power-Up RECALL on page 24).

Interrupts

The CY14B108K has flags register, interrupt register, and interrupt logic that can signal interrupt to the microcontroller. There are three potential sources for interrupt: watchdog timer, power monitor, and alarm timer. Each of these can be individually enabled to drive the INT pin by appropriate setting in the Interrupt register (0xFFFF6). In addition, each has an associated flag bit in the flags register (0xFFFF0) that the host processor uses to determine the cause of the interrupt. The INT pin driver has two bits that specify its behavior when an interrupt occurs.

An interrupt is raised only if both a flag is raised by one of the three sources and the respective interrupt enable bit in interrupts register is enabled (set to '1'). After an interrupt source is active, two programmable bits, H/L and P/L, determine the behavior of the output pin driver on INT pin. These two bits are located in the interrupt register and can be used to drive level or pulse mode output from the INT pin. In pulse mode, the pulse width is internally fixed at approximately 200 ms. This mode is intended to reset a host microcontroller. In the level mode, the pin goes to its active polarity until the flags register is read by the user. This mode is used as an interrupt to a host microcontroller. The control bits are summarized in the following section.

Interrupts are only generated while working on normal power and are not triggered when system is running in backup power mode.

Note CY14B108K generates valid interrupts only after the Power-up RECALL sequence is completed. All events on INT pin must be ignored for $t_{HRECALL}$ duration after powerup.

Interrupt Register

Watchdog Interrupt Enable (WIE). When set to '1', the watchdog timer drives the INT pin and an internal flag when a watchdog time out occurs. When WIE is set to '0', the watchdog timer only affects the WDF flag in flags register.

Alarm Interrupt Enable (AIE). When set to '1', the alarm match drives the INT pin and an internal flag. When AIE is set to '0', the alarm match only affects the AF flags register.

Power Fail Interrupt Enable (PFE). When set to '1', the power fail monitor drives the pin and an internal flag. When PFE is set to '0', the power fail monitor only affects the PF flag in flags register.

High/Low (H/L). When set to a '1', the INT pin is active HIGH and the driver mode is push pull. The INT pin drives HIGH only when V_{CC} is greater than V_{SWITCH}. When set to a '0', the INT pin is active LOW and the drive mode is open drain. The INT pin must be pulled up to Vcc by a 10 k resistor while using the interrupt in active LOW mode.

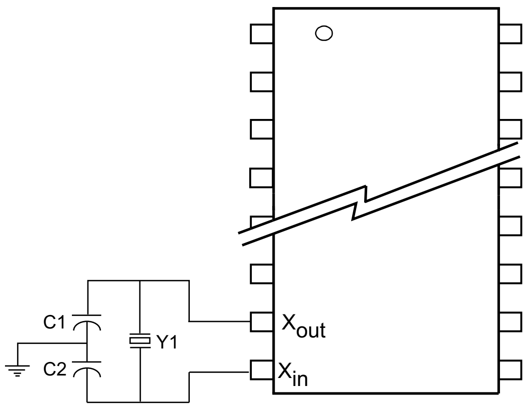
Pulse/Level (P/L). When set to a '1' and an interrupt occurs, the INT pin is driven for approximately 200 ms. When P/L is set to a '0', the INT pin is driven HIGH or LOW (determined by H/L) until the flags register is read.

When an enabled interrupt source activates the INT pin, an external host reads the flags registers to determine the cause. Remember that all flags are cleared when the register is read. If the INT pin is programmed for Level mode, then the condition clears and the INT pin returns to its inactive state. If the pin is programmed for pulse mode, then reading the flag also clears the flag and the pin. The pulse does not complete its specified duration if the flags register is read. If the INT pin is used as a host reset, the flags register is not read during a reset.

Flags Register

The flags register has three flag bits: WDF, AF, and PF, which can be used to generate an interrupt. These flags are set by the watchdog timeout, alarm match, or power fail monitor respectively. The processor can either poll this register or enable interrupts when a flag is set. These flags are automatically reset when the register is read. The flags register is automatically loaded with the value 0x00 on power-up (except for the OSCF bit. See Stopping and Starting the Oscillator on page 10)

Figure 4. RTC Recommended Component Configuration



Recommended Values

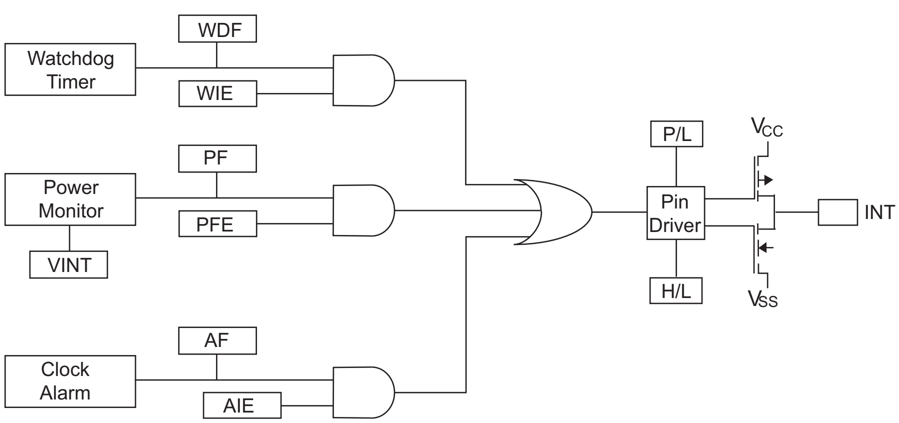
Y_1 = 32.768 KHz (12.5 pF)

C_1 = 12 pF

C_2 = 69 pF

Note: The recommended values for C1 and C2 include board trace capacitance.

Figure 5. Interrupt Block Diagram



WDF - Watchdog Timer Flag
WIE - Watchdog Interrupt Enable
PF - Power Fail Flag
PFE - Power Fail Enable
AF - Alarm Flag
AIE - Alarm Interrupt Enable
P/L - Pulse Level
H/L - High/Low

Table 3. RTC Register Map [8]

Register		BCD Format Data [9]								Function/Range
CY14B108K	CY14B108M	D7	D6	D5	D4	D3	D2	D1	D0	
0xFFFFF	0x7FFFF	10s years				Years				Years: 00–99
0xFFFFE	0x7FFFE	0	0	0	10s months	Months				Months: 01–12
0xFFFFD	0x7FFFD	0	0	10s day of month		Day of month				Day of month: 01–31
0xFFFFC	0x7FFFC	0	0	0	0	0	Day of week			Day of week: 01–07
0xFFFFB	0x7FFFB	0	0	10s hours		Hours				Hours: 00–23
0xFFFFA	0x7FFFA	0	10s minutes			Minutes				Minutes: 00–59
0xFFFF9	0x7FFF9	0	10s seconds			Seconds				Seconds: 00–59
0xFFFF8	0x7FFF8	OSCEN (0)	0	Cal sign (0)	Calibration (00000)					Calibration values [10]
0xFFFF7	0x7FFF7	WDS (0)	WDW (0)	WDT (000000)						Watchdog [10]
0xFFFF6	0x7FFF6	WIE (0)	AIE (0)	PFE (0)	0	H/L (1)	P/L (0)	0	0	Interrupts [10]
0xFFFF5	0x7FFF5	M (1)	0	10s alarm date		Alarm day				Alarm, day of month: 01–31
0xFFFF4	0x7FFF4	M (1)	0	10s alarm hours		Alarm hours				Alarm, hours: 00–23
0xFFFF3	0x7FFF3	M (1)	10 alarm minutes			Alarm minutes				Alarm, minutes: 00–59
0xFFFF2	0x7FFF2	M (1)	10 alarm seconds			Alarm, seconds				Alarm, seconds: 00–59
0xFFFF1	0x7FFF1	10s centuries				Centuries				Centuries: 00–99
0xFFFF0	0x7FFF0	WDF	AF	PF	OSCF[11]	0	CAL (0)	W (0)	R (0)	Flags [10]

Notes

8. Upper Byte D_{15}-D_8 (CY14B108M) of RTC registers are reserved for future use.
9. ( ) designates values shipped from the factory.
10. This is a binary value, not a BCD value.
11. When the user resets OSCF flag bit, the flags register will be updated after t_{RTCp} time.

Table 4. Register Map Detail

Register		Description							
CY14B108K	CY14B108M								
0xFFFFF	0x7FFFF	Time Keeping - Years							
		D7	D6	D5	D4	D3	D2	D1	D0
		10s years				Years			
		Contains the lower two BCD digits of the year. Lower nibble (four bits) contains the value for years; upper nibble (four bits) contains the value for 10s of years. Each nibble operates from 0 to 9. The range for the register is 0–99.							
0xFFFFE	0x7FFFE	Time Keeping - Months							
		D7	D6	D5	D4	D3	D2	D1	D0
		0	0	0	10s month	Months			
		Contains the BCD digits of the month. Lower nibble (four bits) contains the lower digit and operates from 0 to 9; upper nibble (one bit) contains the upper digit and operates from 0 to 1. The range for the register is 1–12.							
0xFFFFD	0x7FFFD	Time Keeping - Date							
		D7	D6	D5	D4	D3	D2	D1	D0
		0	0	10s day of month		Day of month			
		Contains the BCD digits for the date of the month. Lower nibble (four bits) contains the lower digit and operates from 0 to 9; upper nibble (two bits) contains the 10s digit and operates from 0 to 3. The range for the register is 1–31. Leap years are automatically adjusted for.							
0xFFFFC	0x7FFFC	Time Keeping - Day							
		D7	D6	D5	D4	D3	D2	D1	D0
		0	0	0	0	0	Day of week		
		Lower nibble (three bits) contains a value that correlates to day of the week. Day of the week is a ring counter that counts from 1 to 7 then returns to 1. The user must assign meaning to the day value, because the day is not integrated with the date.							
0xFFFFB	0x7FFFB	Time Keeping - Hours							
		D7	D6	D5	D4	D3	D2	D1	D0
		0	0	10s hours		Hours			
		Contains the BCD value of hours in 24 hour format. Lower nibble (four bits) contains the lower digit and operates from 0 to 9; upper nibble (two bits) contains the upper digit and operates from 0 to 2. The range for the register is 0–23.							
0xFFFFA	0x7FFFA	Time Keeping - Minutes							
		D7	D6	D5	D4	D3	D2	D1	D0
		0	10s minutes			Minutes			
		Contains the BCD value of minutes. Lower nibble (four bits) contains the lower digit and operates from 0 to 9; upper nibble (three bits) contains the upper minutes digit and operates from 0 to 5. The range for the register is 0–59.							
0xFFFF9	0x7FFF9	Time Keeping - Seconds							
		D7	D6	D5	D4	D3	D2	D1	D0
		0	10s seconds			Seconds			
		Contains the BCD value of seconds. Lower nibble (four bits) contains the lower digit and operates from 0 to 9; upper nibble (three bits) contains the upper digit and operates from 0 to 5. The range for the register is 0 to 59.							

Table 4. Register Map Detail (continued)

Register		Description							
CY14B108K	**CY14B108M**								
0xFFFF8	**0x7FFF8**	**Calibration/Control**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		OSCEN	0	Calibration sign	Calibration				
OSCEN		Oscillator enable. When set to 1, the oscillator is stopped. When set to 0, the oscillator runs. Disabling the oscillator saves battery or capacitor power during storage.							
Calibration Sign		Determines if the calibration adjustment is applied as an addition (1) to or as a subtraction (0) from the time-base.							
Calibration		These five bits control the calibration of the clock.							
0xFFFF7	**0x7FFF7**	**WatchDog Timer**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		WDS	WDW	WDT					
WDS		Watchdog strobe. Setting this bit to ‘1’ reloads and restarts the watchdog timer. Setting the bit to ‘0’ has no effect. The bit is cleared automatically after the watchdog timer is reset. The WDS bit is write only. Reading it always returns a 0.							
WDW		Watchdog write enable. Setting this bit to 1 disables any WRITE to the watchdog timeout value (D5–D0). This allows the user to set the watchdog strobe bit without disturbing the timeout value. Setting this bit to 0 allows bits D5–D0 to be written to the watchdog register when the next write cycle is complete. This function is explained in more detail in Watchdog Timer on page 10.							
WDT		Watchdog timeout selection. The watchdog timer interval is selected by the 6-bit value in this register. It represents a multiplier of the 32 Hz count (31.25 ms). The range of timeout value is 31.25 ms (a setting of 1) to 2 seconds (setting of 3 Fh). Setting the watchdog timer register to ‘0’ disables the timer. These bits can be written only if the WDW bit was set to 0 on a previous cycle.							
0xFFFF6	**0x7FFF6**	**Interrupt Status/Control**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		WIE	AIE	PFE	0	H/L	P/L	0	0
WIE		Watchdog interrupt enable. When set to ‘1’ and a watchdog timeout occurs, the watchdog timer drives the INT pin and the WDF flag. When set to ‘0’, the watchdog timeout affects only the WDF flag.							
AIE		Alarm interrupt enable. When set to ‘1’, the alarm match drives the INT pin and the AF flag. When set to ‘0’, the alarm match only affects the AF flag.							
PFE		Power fail enable. When set to ‘1’, the power fail monitor drives the INT pin and the PF flag. When set to ‘0’, the power fail monitor affects only the PF flag.							
0		Reserved for future use							
H/L		High/Low. When set to ‘1’, the INT pin is driven active HIGH. When set to ‘0’, the INT pin is open drain, active LOW.							
P/L		Pulse/Level. When set to ‘1’, the INT pin is driven active (determined by H/L) by an interrupt source for approximately 200 ms. When set to ‘0’, the INT pin is driven to an active level (as set by H/L) until the flags register is read.							
0xFFFF5	**0x7FFF5**	**Alarm - Day**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		M	0	10s alarm date		Alarm date			
		Contains the alarm value for the date of the month and the mask bit to select or deselect the date value.							
M		Match. When this bit is set to ‘0’, the date value is used in the alarm match. Setting this bit to ‘1’ causes the match circuit to ignore the date value.							

Table 4. Register Map Detail (continued)

Register		Description							
CY14B108K	CY14B108M								
0xFFFF4	0x7FFF4	**Alarm - Hours**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		M	0	10s alarm hours		Alarm hours			
		Contains the alarm value for the hours and the mask bit to select or deselect the hours value.							
M		Match. When this bit is set to '0', the hours value is used in the alarm match. Setting this bit to '1' causes the match circuit to ignore the hours value.							
0xFFFF3	0x7FFF3	**Alarm - Minutes**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		M	10s alarm minutes			Alarm minutes			
		Contains the alarm value for the minutes and the mask bit to select or deselect the minutes value.							
M		Match. When this bit is set to '0', the minutes value is used in the alarm match. Setting this bit to '1' causes the match circuit to ignore the minutes value.							
0xFFFF2	0x7FFF2	**Alarm - Seconds**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		M	10s alarm seconds			Alarm seconds			
		Contains the alarm value for the seconds and the mask bit to select or deselect the seconds' value.							
M		Match. When this bit is set to '0', the seconds value is used in the alarm match. Setting this bit to '1' causes the match circuit to ignore the seconds value.							
0xFFFF1	0x7FFF1	**Time Keeping - Centuries**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		10s centuries				Centuries			
		Contains the BCD value of centuries. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper digit and operates from 0 to 9. The range for the register is 0-99 centuries.							
0xFFFF0	0x7FFF0	**Flags**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		WDF	AF	PF	OSCF	0	CAL	W	R
WDF		Watchdog timer flag. This read only bit is set to '1' when the watchdog timer is allowed to reach 0 without being reset by the user. It is cleared to '0' when the flags register is read or on power-up							
AF		Alarm flag. This read only bit is set to '1' when the time and date match the values stored in the alarm registers with the match bits = 0. It is cleared when the flags register is read or on power-up.							
PF		Power fail flag. This read only bit is set to '1' when power falls below the power fail threshold V_{SWITCH}. It is cleared to '0' when the flags register is read or on power-up.							
OSCF		Oscillator fail flag. Set to '1' on power-up if the oscillator is enabled and not running in the first 5 ms of operation. This indicates that RTC backup power failed and clock value is no longer valid. This bit survives the power cycle and is never cleared internally by the chip. The user must check for this condition and write '0' to clear this flag. When user resets OSCF flag bit, the bit will be updated after t_{RTCp} time.							
CAL		Calibration mode. When set to '1', a 512 Hz square wave is output on the INT pin. When set to '0', the INT pin resumes normal operation. This bit defaults to 0 (disabled) on power-up.							
W		Write enable: Setting the 'W' bit to '1' freezes updates of the RTC registers. The user can then write to RTC registers, alarm registers, calibration register, interrupt register and flags register. Setting the 'W' bit to '0' causes the contents of the RTC registers to be transferred to the time keeping counters if the time has changed. This transfer process takes t_{RTCp} time to complete. This bit defaults to 0 on power-up.							
R		Read enable: Setting 'R' bit to '1', stops clock updates to user RTC registers so that clock updates are not seen during the reading process. Set 'R' bit to '0' to resume clock updates to the holding register. Setting this bit does not require 'W' bit to be set to '1'. This bit defaults to 0 on power-up.							

Best Practices

nvSRAM products have been used effectively for over 27 years. While ease-of-use is one of the product's main system values, experience gained working with hundreds of applications has resulted in the following suggestions as best practices:

- The nonvolatile cells in this nvSRAM product are delivered from Cypress with 0x00 written in all cells. Incoming inspection routines at customer or contract manufacturer's sites sometimes reprogram these values. Final NV patterns are typically repeating patterns of AA, 55, 00, FF, A5, or 5A. End product's firmware should not assume an NV array is in a set programmed state. Routines that check memory content values to determine first time system configuration, cold or warm boot status, and so on should always program a unique NV pattern (that is, complex 4-byte pattern of 46 E6 49 53 hex or more random bytes) as part of the final system manufacturing test to ensure these system routines work consistently.
- Power-up boot firmware routines should rewrite the nvSRAM into the desired state (for example, AutoStore enabled). While the nvSRAM is shipped in a preset state, best practice is to again rewrite the nvSRAM into the desired state as a safeguard against events that might flip the bit inadvertently such as program bugs and incoming inspection routines.
- The V_{CAP} value specified in this data sheet includes a minimum and a maximum value size. Best practice is to meet this requirement and not exceed the maximum V_{CAP} value because the nvSRAM internal algorithm calculates V_{CAP} charge and discharge time based on this maximum V_{CAP} value. Customers that want to use a larger V_{CAP} value to make sure there is extra store charge and store time should discuss their V_{CAP} size selection with Cypress to understand any impact on the V_{CAP} voltage level at the end of a t_{RECALL} period.
- When base time is updated, these updates are transferred to the time keeping registers when 'W' bit is set to '0'. This transfer takes t_{RTCp} time to complete. It is recommended to initiate software STORE or Hardware STORE after t_{RTCp} time to save the base time into nonvolatile memory.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature .... –65 °C to +150 °C

Maximum accumulated storage time

At 150 °C ambient temperature .... 1000 h

At 85 °C ambient temperature .... 20 Years

Ambient temperature with power applied .... –55 °C to +150 °C

Supply voltage on V_{CC} relative to V_{SS} ....–0.5 V to 4.1 V

Voltage applied to outputs in High Z state ....–0.5 V to V_{CC} + 0.5 V

Input voltage ....–0.5 V to V_{CC} + 0.5 V

Transient voltage (< 20 ns) on any pin to ground potential ....–2.0 V to V_{CC} + 2.0 V

Package power dissipation capability (T_A = 25°C) .... 1.0 W

Surface mount Pb soldering temperature (3 Seconds) .... +260 °C

DC output current (1 output at a time, 1s duration) .... 15 mA

Static discharge voltage (per MIL-STD-883, Method 3015) .... > 2001 V

Latch up current .... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40 °C to +85 °C	2.7 V to 3.6 V

DC Electrical Characteristics

Over the Operating Range (V_{CC} = 2.7 V to 3.6 V)

Parameter	Description	Test Conditions	Min	Typ[12]	Max	Unit
V_{CC}	Power supply		2.7	3.0	3.6	V
I_{CC1}	Average V_{CC} current	t_{RC} = 25 ns t_{RC} = 45 ns Values obtained without output loads (I_{OUT} = 0 mA)	–	–	75 57	mA mA
I_{CC2}	Average V_{CC} current during STORE	All inputs don't care, V_{CC} = Max. Average current for duration t_{STORE}	–	–	20	mA
I_{CC3}	Average V_{CC} current at t_{RC} = 200 ns, $V_{CC(Typ)}$, 25 °C	All inputs cycling at CMOS levels. Values obtained without output loads (I_{OUT} = 0 mA).	–	40	–	mA
I_{CC4}	Average V_{CAP} current during AutoStore cycle	All inputs don't care. Average current for duration t_{STORE}	–	–	10	mA
I_{SB}	V_{CC} standby current	$\overline{CE}$ ≥ (V_{CC} – 0.2 V). V_{IN} ≤ 0.2 V or ≥ (V_{CC} – 0.2 V). W bit set to '0'. Standby current level after nonvolatile cycle is complete. Inputs are static. f = 0 MHz.	–	–	10	mA
I_{IX}[13]	Input leakage current (except $\overline{HSB}$)	V_{CC} = Max, $V_{SS} \le V_{IN} \le V_{CC}$	–2	–	+2	μA
	Input leakage current (for $\overline{HSB}$)	V_{CC} = Max, $V_{SS} \le V_{IN} \le V_{CC}$	–200	–	+2	μA
I_{OZ}	Off state output leakage current	V_{CC} = Max, $V_{SS} \le V_{OUT} \le V_{CC}$, $\overline{CE}$ or $\overline{OE}$ ≥ V_{IH} or $\overline{BHE}/\overline{BLE}$ ≥ V_{IH} or $\overline{WE}$ ≤ V_{IL}	–2	–	+2	μA
V_{IH}	Input HIGH voltage		2.0	–	V_{CC} + 0.5	V
V_{IL}	Input LOW voltage		V_{SS} – 0.5	–	0.8	V
V_{OH}	Output HIGH voltage	I_{OUT} = –2 mA	2.4	–	–	V
V_{OL}	Output LOW voltage	I_{OUT} = 4 mA	–	–	0.4	V
V_{CAP}[14]	Storage capacitor	Between V_{CAP} pin and V_{SS}, 5 V rated	122	150	360	μF

Notes

12. Typical values are at 25 °C, V_{CC}= $V_{CC(Typ)}$. Not 100% tested.
13. The $\overline{HSB}$ pin has I_{OUT} = -2 uA for V_{OH} of 2.4 V when both active HIGH and LOW drivers are disabled. When they are enabled standard V_{OH} and V_{OL} are valid. This parameter is characterized but not tested.
14. Min V_{CAP} value guarantees that there is a sufficient charge available to complete a successful AutoStore operation. Max V_{CAP} value guarantees that the capacitor on V_{CAP} is charged to a minimum voltage during a Power-Up RECALL cycle so that an immediate power-down cycle can complete a successful AutoStore. Therefore it is always recommended to use a capacitor within the specified min and max limits. Refer application note AN43593 for more details on V_{CAP} options.

Data Retention and Endurance

Over the Operating Range

Parameter	Description	Min	Unit
$DATA_R$	Data retention	20	Years
NV_C	Nonvolatile STORE operations	1,000	K

Capacitance

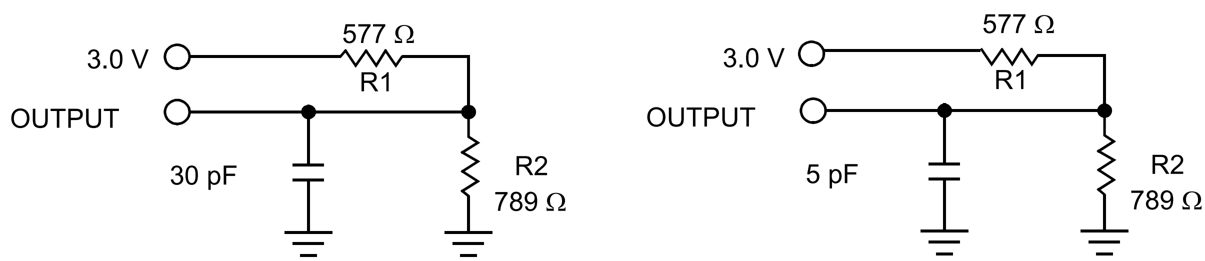
Parameter[15]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, $V_{CC} = V_{CC(Typ)}$	14	pF
C_{OUT}	Output capacitance		14	pF

Thermal Resistance

Parameter[15]	Description	Test Conditions	44-pin TSOP II	54-pin TSOP II	Unit
Θ_{JA}	Thermal resistance (Junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	45.3	44.22	°C/W
Θ_{JC}	Thermal resistance (Junction to case)		5.2	8.26	°C/W

AC Test Loads

Figure 6. AC Test Loads



AC Test Conditions

Input pulse levels ....0 V to 3 V
Input rise and fall times (10%–90%) .... ≤ 3 ns
Input and output timing reference levels .... 1.5 V

Note
15. These parameters are only guaranteed by design and are not tested.

RTC Characteristics

Over the Operating Range

Parameters	Description		Min	Typ [16]	Max	Units
V_{RTCbat}	RTC battery pin voltage		1.8	3.0	3.6	V
I_{BAK}[17]	RTC backup current	T_A (Min)	–	–	0.35	µA
		25 °C	–	0.35	–	µA
		T_A (Max)	–	–	0.5	µA
V_{RTCcap}[18]	RTC capacitor pin voltage	T_A (Min)	1.6	–	3.6	V
		25 °C	1.5	3.0	3.6	V
		T_A (Max)	1.4	–	3.6	V
tOCS	RTC oscillator time to start		–	1	2	sec
t_{RTCp}	RTC processing time from end of ‘W’ bit set to ‘0’		–	–	350	µs
R_{BKCHG}	RTC backup capacitor charge current-limiting resistor		350	–	850	Ω

Notes
16. Typical values are at 25 °C, $V_{CC} = V_{CC(Typ)}$. Not 100% tested.
17. From either V_{RTCcap} or V_{RTCbat}.
18. If V_{RTCcap} > 0.5 V or if no capacitor is connected to V_{RTCcap} pin, the oscillator starts in t_{OCS} time. If a backup capacitor is connected and V_{RTCcap} < 0.5 V, the capacitor must be allowed to charge to 0.5 V for oscillator to start.

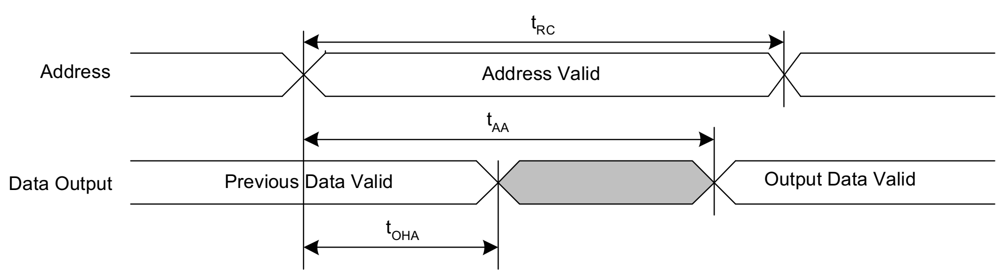
AC Switching Characteristics

Over the Operating Range

Parameters [19]		Description	25 ns		45 ns		Unit
Cypress Parameter	Alt Parameter		Min	Max	Min	Max	
SRAM Read Cycle							
t_{ACE}	t_{ACS}	Chip enable access time	–	25	–	45	ns
t_{RC} [20]	t_{RC}	Read cycle time	25	–	45	–	ns
t_{AA} [21]	t_{AA}	Address access time	–	25	–	45	ns
t_{DOE}	t_{OE}	Output enable to data valid	–	12	–	20	ns
t_{OHA} [21]	t_{OH}	Output hold after address change	3	–	3	–	ns
t_{LZCE} [22, 23]	t_{LZ}	Chip enable to output active	3	–	3	–	ns
t_{HZCE} [22, 23]	t_{HZ}	Chip disable to output inactive	–	10	–	15	ns
t_{LZOE} [22, 23]	t_{OLZ}	Output enable to output active	0	–	0	–	ns
t_{HZOE} [22, 23]	t_{OHZ}	Output disable to output inactive	–	10	–	15	ns
t_{PU} [22]	t_{PA}	Chip enable to power active	0	–	0	–	ns
t_{PD} [22]	t_{PS}	Chip disable to power standby	–	25	–	45	ns
t_{DBE}	-	Byte enable to data valid	–	12	–	20	ns
t_{LZBE} [22]	-	Byte enable to output active	0	–	0	–	ns
t_{HZBE} [22]	-	Byte disable to output inactive	–	10	–	15	ns
SRAM Write Cycle							
t_{WC}	t_{WC}	Write cycle time	25	–	45	–	ns
t_{PWE}	t_{WP}	Write pulse width	20	–	30	–	ns
t_{SCE}	t_{CW}	Chip enable to end of write	20	–	30	–	ns
t_{SD}	t_{DW}	Data setup to end of write	10	–	15	–	ns
t_{HD}	t_{DH}	Data hold after end of write	0	–	0	–	ns
t_{AW}	t_{AW}	Address setup to end of write	20	–	30	–	ns
t_{SA}	t_{AS}	Address setup to start of write	0	–	0	–	ns
t_{HA}	t_{WR}	Address hold after end of write	0	–	0	–	ns
t_{HZWE} [22, 23, 24]	t_{WZ}	Write enable to output disable	–	10	–	15	ns
t_{LZWE} [22, 23]	t_{OW}	Output active after end of write	3	–	3	–	ns
t_{BW}	-	Byte enable to end of write	20	–	30	–	ns

Switching Waveforms

Figure 7. SRAM Read Cycle 1 (Address Controlled) [20, 21, 25]



Notes
19. Test conditions assume signal transition time of 3 ns or less, timing reference levels of $V_{CC}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} and load capacitance shown in Figure 6 on page 19.
20. WE must be HIGH during SRAM read cycles.
21. Device is continuously selected with CE, OE and BHE / BLE LOW.
22. These parameters are only guaranteed by design and are not tested.
23. Measured ±200 mV from steady state output voltage.
24. If WE is LOW when CE goes LOW, the outputs remain in the high impedance state.
25. HSB must remain HIGH during Read and Write cycles.

Switching Waveforms (continued)

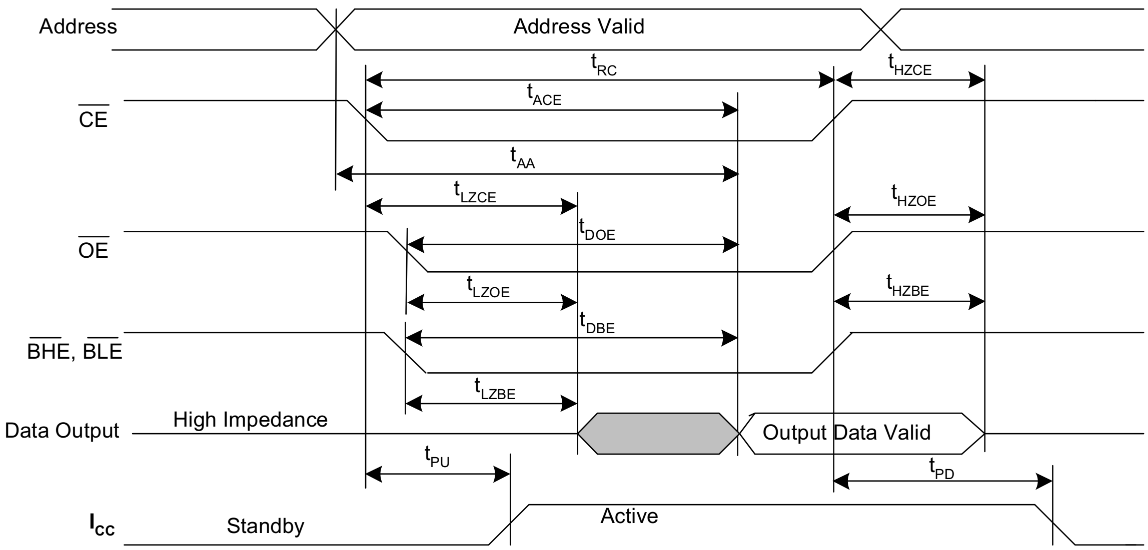


Figure 8. SRAM Read Cycle 2 (CE and OE Controlled) [26, 27, 28]

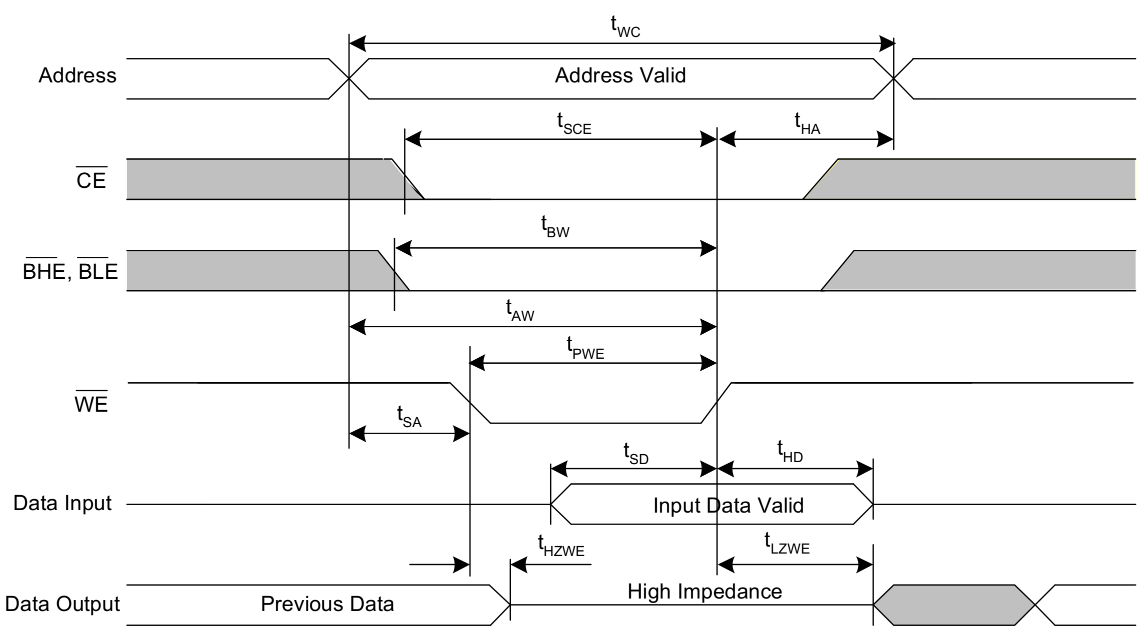


Figure 9. SRAM Write Cycle 1 (WE Controlled) [26, 28, 29, 30]

Notes
26. BHE and BLE are applicable for × 16 configuration only.
27. WE must be HIGH during SRAM read cycles.
28. HSB must remain HIGH during read and write cycles.
29. If WE is LOW when CE goes LOW, the outputs remain in the high impedance state.
30. CE or WE must be ≥ V_{IH} during address transitions.

Switching Waveforms (continued)

Figure 10. SRAM Write Cycle 2 ($\overline{CE}$ Controlled) [31, 32, 33, 34]

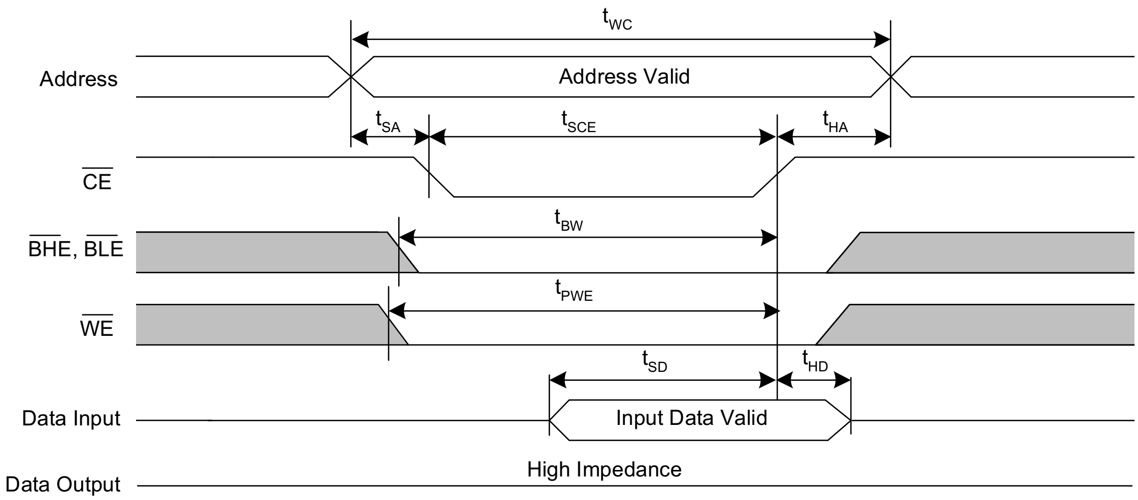
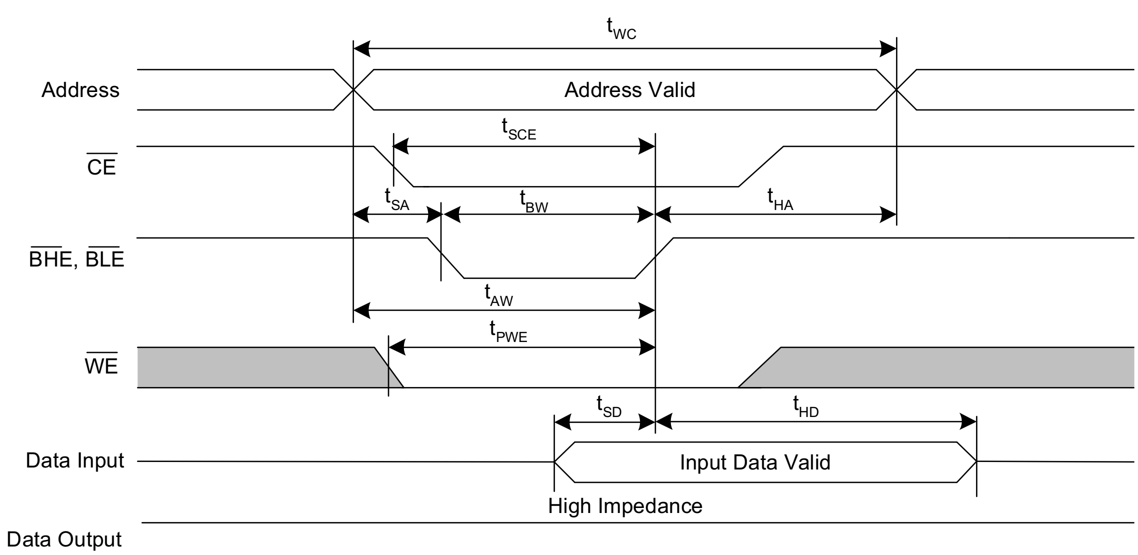


Figure 11. SRAM Write Cycle 3 ($\overline{BHE}$ and $\overline{BLE}$ Controlled) [32, 33, 34, 35, 36]

(Not applicable for RTC register writes)



Notes

31. $\overline{BHE}$ and $\overline{BLE}$ are applicable for × 16 configuration only.
32. If $\overline{WE}$ is LOW when $\overline{CE}$ goes LOW, the outputs remain in the high impedance state.
33. $\overline{HSB}$ must remain HIGH during read and write cycles.
34. $\overline{CE}$ or $\overline{WE}$ must be ≥ V_{IH} during address transitions.
35. While there are 19 address lines on the CY14B108K (18 address lines on the CY14B108M), only 13 address lines (A_{14}–A_2) are used to control software modes. The remaining address lines are don't care.
36. Only $\overline{CE}$ and $\overline{WE}$ controlled writes to RTC registers are allowed. $\overline{BLE}$ pin must be held LOW before $\overline{CE}$ or $\overline{WE}$ pin goes LOW for writes to RTC register.

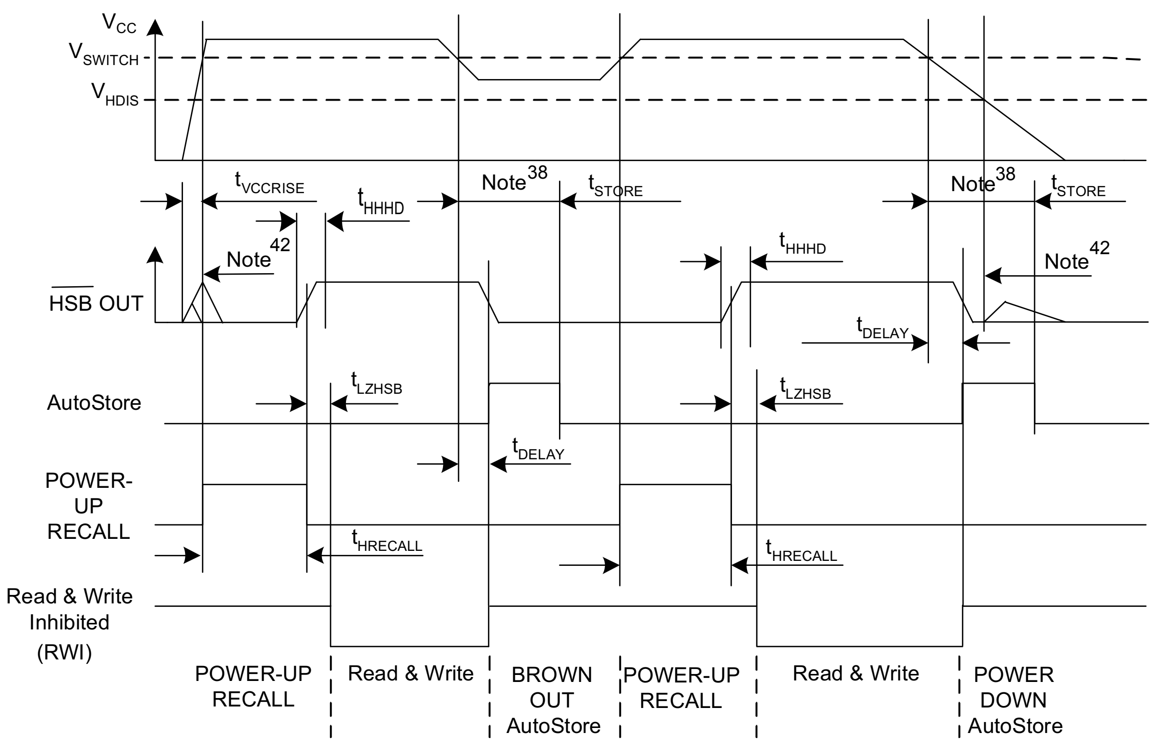
AutoStore/Power-Up RECALL

Over the Operating Range

Parameter	Description	CY14B108K/CY14B108M		Unit
		Min	Max	
$t_{HRECALL}$ [37]	Power-Up RECALL duration	–	20	ms
t_{STORE} [38]	STORE cycle duration	–	8	ms
t_{DELAY} [39]	Time allowed to complete SRAM write cycle	–	25	ns
V_{SWITCH}	Low voltage trigger level	–	2.65	V
$t_{VCCRISE}$ [40]	V_{CC} rise time	150	–	μs
V_{HDIS} [40]	$\overline{HSB}$ output disable voltage	–	1.9	V
t_{LZHSB} [40]	$\overline{HSB}$ to output active time	–	5	μs
t_{HHHD} [40]	$\overline{HSB}$ high active time	–	500	ns

Switching Waveforms

Figure 12. AutoStore or Power-Up RECALL [41]



Notes

37. $t_{HRECALL}$ starts from the time V_{CC} rises above V_{SWITCH}.
38. If an SRAM write has not taken place since the last nonvolatile cycle, no AutoStore or Hardware STORE takes place.
39. On a Hardware STORE and AutoStore initiation, SRAM write operation continues to be enabled for time t_{DELAY}.
40. These parameters are only guaranteed by design and are not tested.
41. Read and Write cycles are ignored during STORE, RECALL, and while V_{CC} is below V_{SWITCH}.
42. During power-up and power-down, $\overline{HSB}$ glitches when $\overline{HSB}$ pin is pulled up through an external resistor.

Software Controlled STORE and RECALL Cycle

Over the Operating Range

Parameter [43, 44]	Description	25 ns Min	25 ns Max	45 ns Min	45 ns Max	Unit
t_{RC}	STORE/RECALL initiation cycle time	25	–	45	–	ns
t_{SA}	Address setup time	0	–	0	–	ns
t_{CW}	Clock pulse width	20	–	30	–	ns
t_{HA}	Address hold time	0	–	0	–	ns
t_{RECALL}	RECALL duration	–	200	–	200	µs
t_{SS} [45, 46]	Soft sequence processing time	–	100	–	100	µs

Switching Waveforms

Figure 13. CE and OE Controlled Software STORE and RECALL Cycle [44]

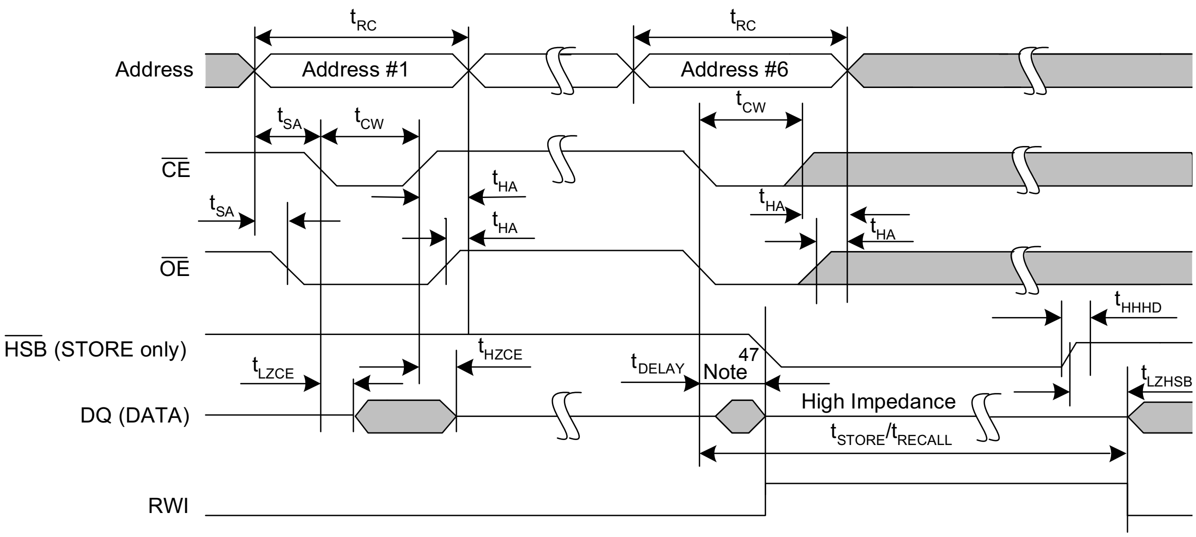
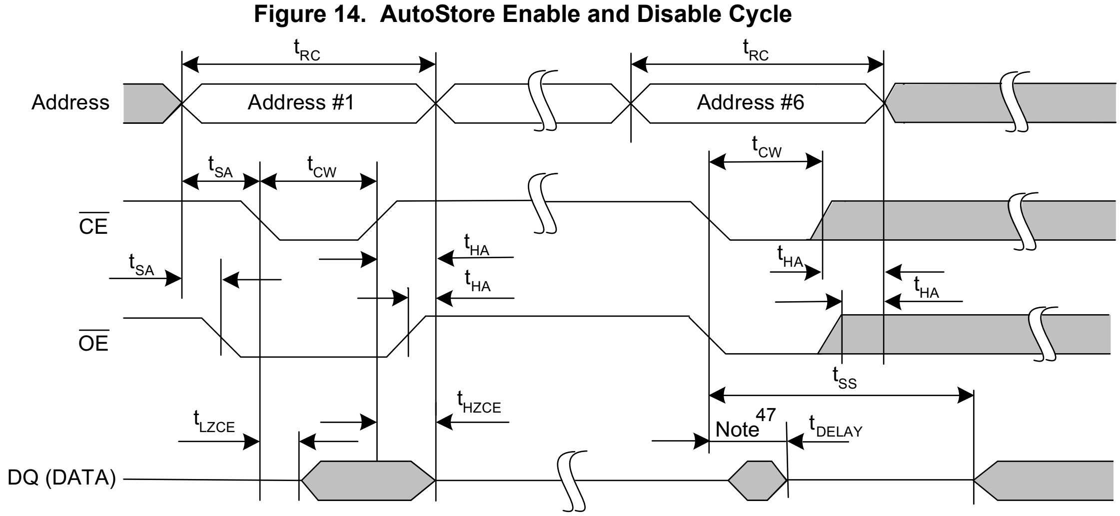


Figure 14. AutoStore Enable and Disable Cycle



Notes

43. The software sequence is clocked with CE controlled or OE controlled reads.
44. The six consecutive addresses must be read in the order listed in Table 1. WE must be HIGH during all six consecutive cycles.
45. This is the amount of time it takes to take action on a soft sequence command. Vcc power must remain HIGH to effectively register command.
46. Commands such as STORE and RECALL lock out I/O until operation is complete which further increases this time. See the specific command.
47. DQ output data at the sixth read may be invalid since the output is disabled at t_{DELAY} time.

Hardware STORE Cycle

Over the Operating Range

Parameter	Description	CY14B108K/CY14B108M		Unit
		Min	Max	
t_{DHSB}	HSB to output active time when write latch not set	–	25	ns
t_{PHSB}	Hardware STORE pulse width	15	–	ns

Switching Waveforms

Figure 15. Hardware STORE Cycle [48]

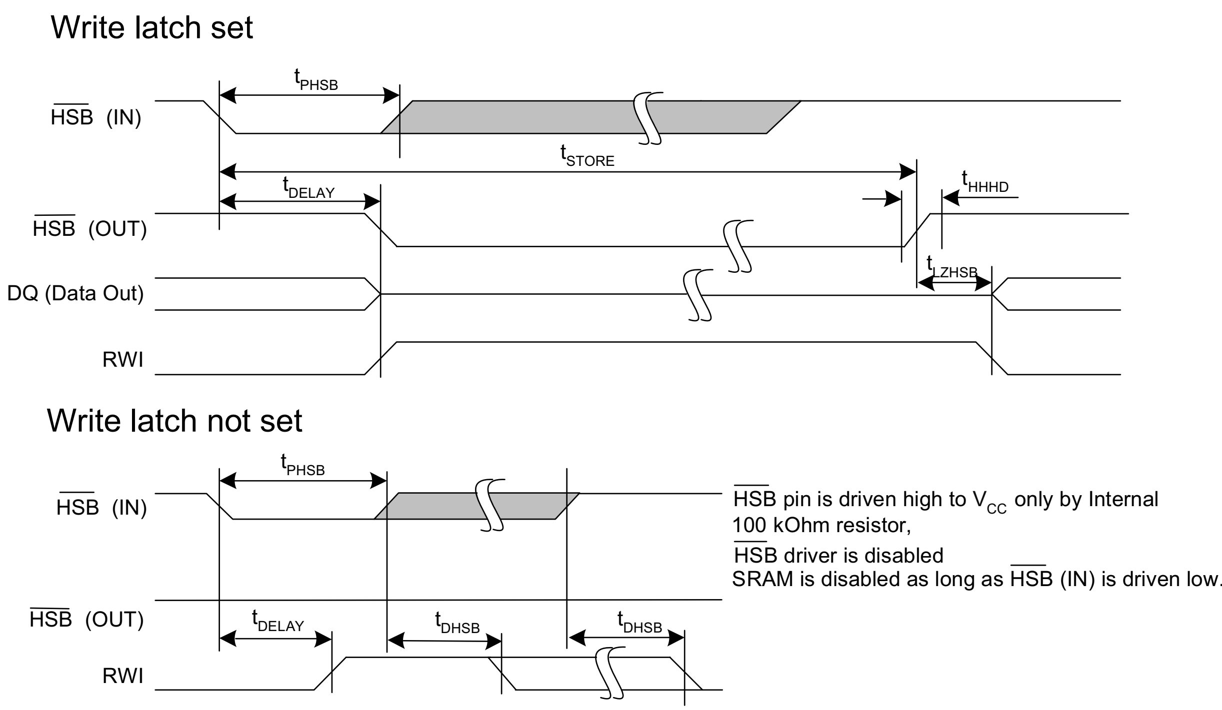
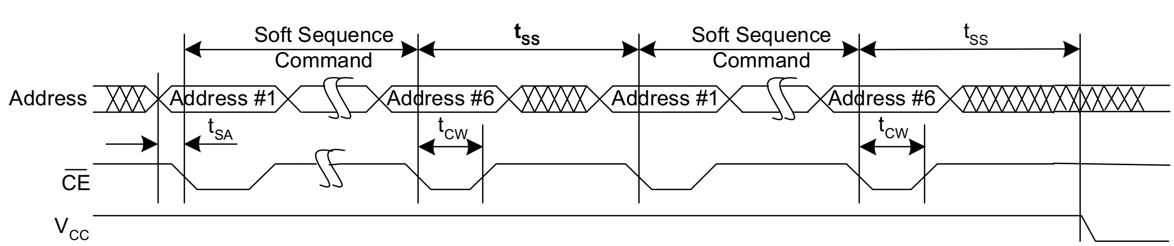


Figure 16. Soft Sequence Processing [49, 50]



Notes

48. If an SRAM write has not taken place since the last nonvolatile cycle, no AutoStore or Hardware STORE takes place.
49. This is the amount of time it takes to take action on a soft sequence command. V_{CC} power must remain HIGH to effectively register command.
50. Commands such as STORE and RECALL lock out I/O until operation is complete which further increases this time. See the specific command.

Truth Table For SRAM Operations

$\overline{HSB}$ should remain HIGH for SRAM Operations.

Table 5. Truth Table for × 8 Configuration

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs and Outputs[51]	Mode	Power
H	X	X	High Z	Deselect/Power-down	Standby
L	H	L	Data out (DQ_0–DQ_7);	Read	Active
L	H	H	High Z	Output disabled	Active
L	L	X	Data in (DQ_0–DQ_7);	Write	Active

Table 6. Truth Table for × 16 Configuration

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$[52]	$\overline{BLE}$[52]	Inputs and Outputs[51]	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-down	Standby
L	X	X	H	H	High Z	Output disabled	Active
L	H	L	L	L	Data out (DQ_0–DQ_{15})	Read	Active
L	H	L	H	L	Data out (DQ_0–DQ_7); DQ_8–DQ_{15} in High Z	Read	Active
L	H	L	L	H	Data out (DQ_8–DQ_{15}); DQ_0–DQ_7 in High Z	Read	Active
L	H	H	L	L	High Z	Output disabled	Active
L	H	H	H	L	High Z	Output disabled	Active
L	H	H	L	H	High Z	Output disabled	Active
L	L	X	L	L	Data in (DQ_0–DQ_{15})	Write	Active
L	L	X	H	L	Data in (DQ_0–DQ_7); DQ_8–DQ_{15} in High Z	Write	Active
L	L	X	L	H	Data in (DQ_8–DQ_{15}); DQ_0–DQ_7 in High Z	Write	Active

Notes

51. Data DQ_0–DQ_7 for × 8 configuration and Data DQ_0–DQ_{15} for × 16 configuration.
52. $\overline{BHE}$ and $\overline{BLE}$ are applicable for × 16 configuration only.

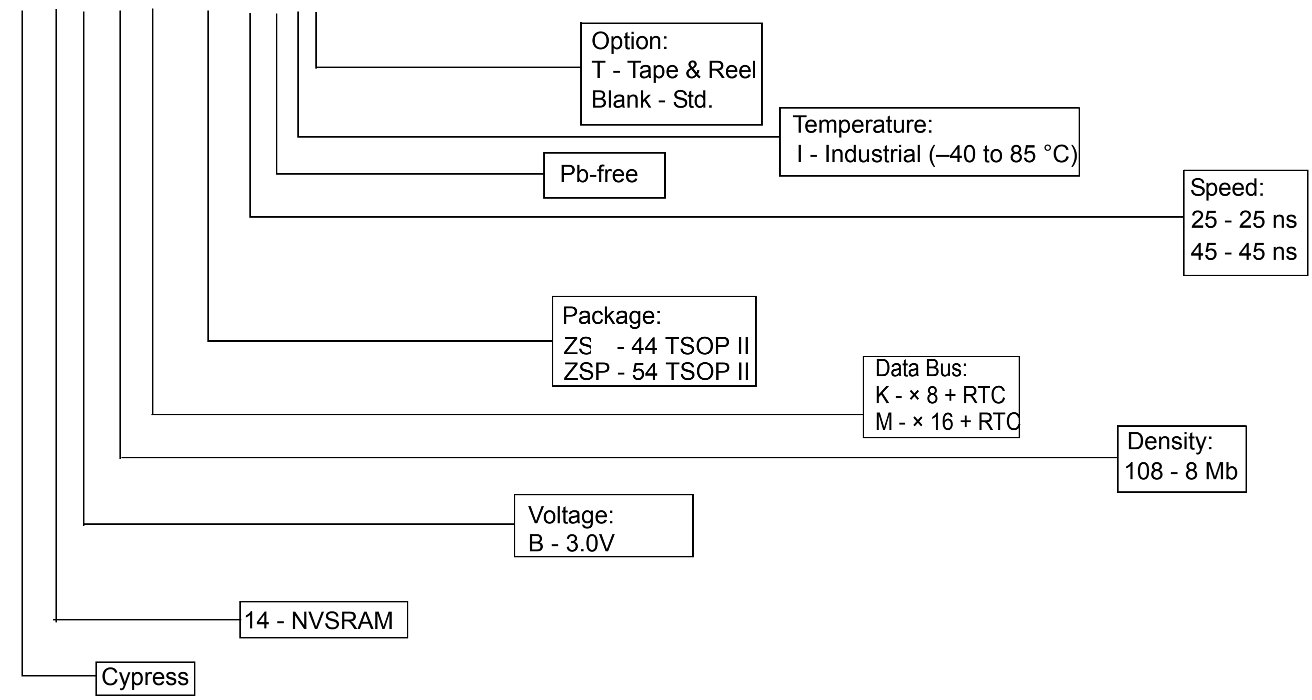
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
25	CY14B108K-ZS25XIT	51-85087	44-pin TSOPII	Industrial
	CY14B108K-ZS25XI	51-85087	44-pin TSOPII	
	CY14B108M-ZSP25XIT	51-85160	54-pin TSOPII	
	CY14B108M-ZSP25XI	51-85160	54-pin TSOPII	
45	CY14B108K-ZS45XIT	51-85087	44-pin TSOPII	
	CY14B108K-ZS45XI	51-85087	44-pin TSOPII	
	CY14B108M-ZSP45XIT	51-85160	54-pin TSOPII	
	CY14B108M-ZSP45XI	51-85160	54-pin TSOPII	

All the above parts are Pb-free.

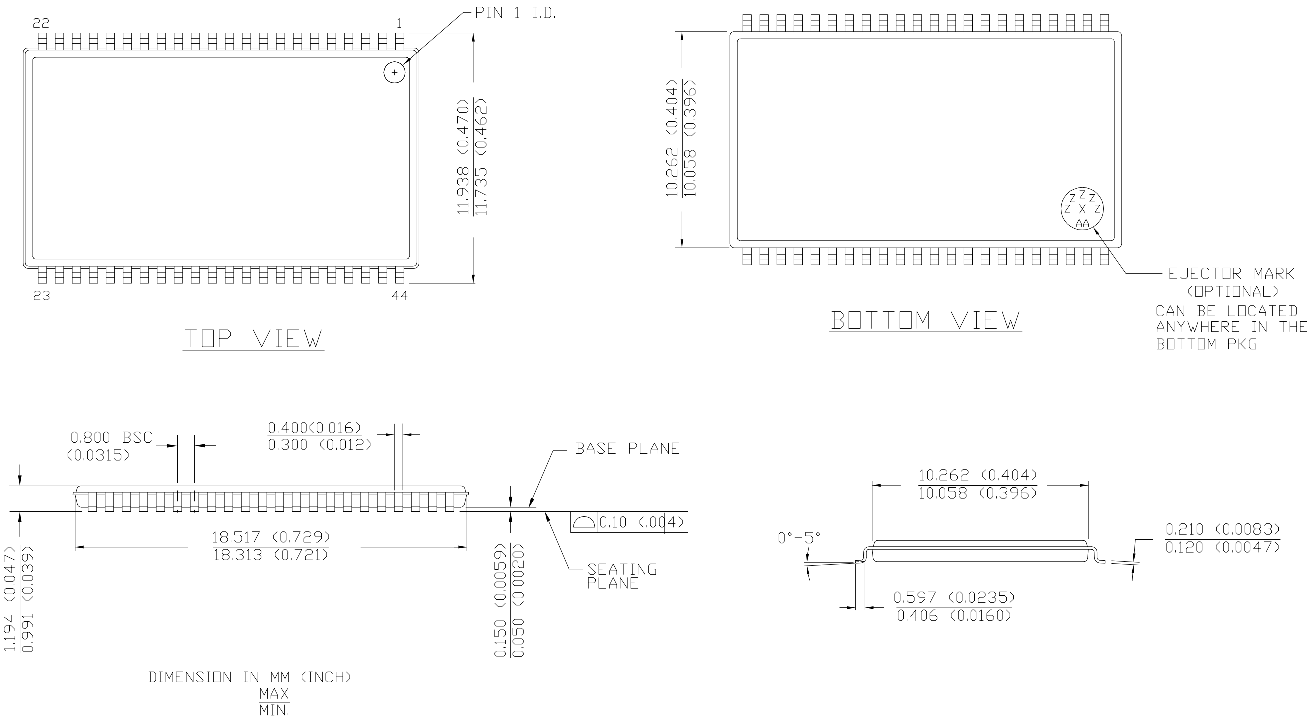
Ordering Code Definitions

CY 14 B 108 K - ZSP 25 X I T



Package Diagrams

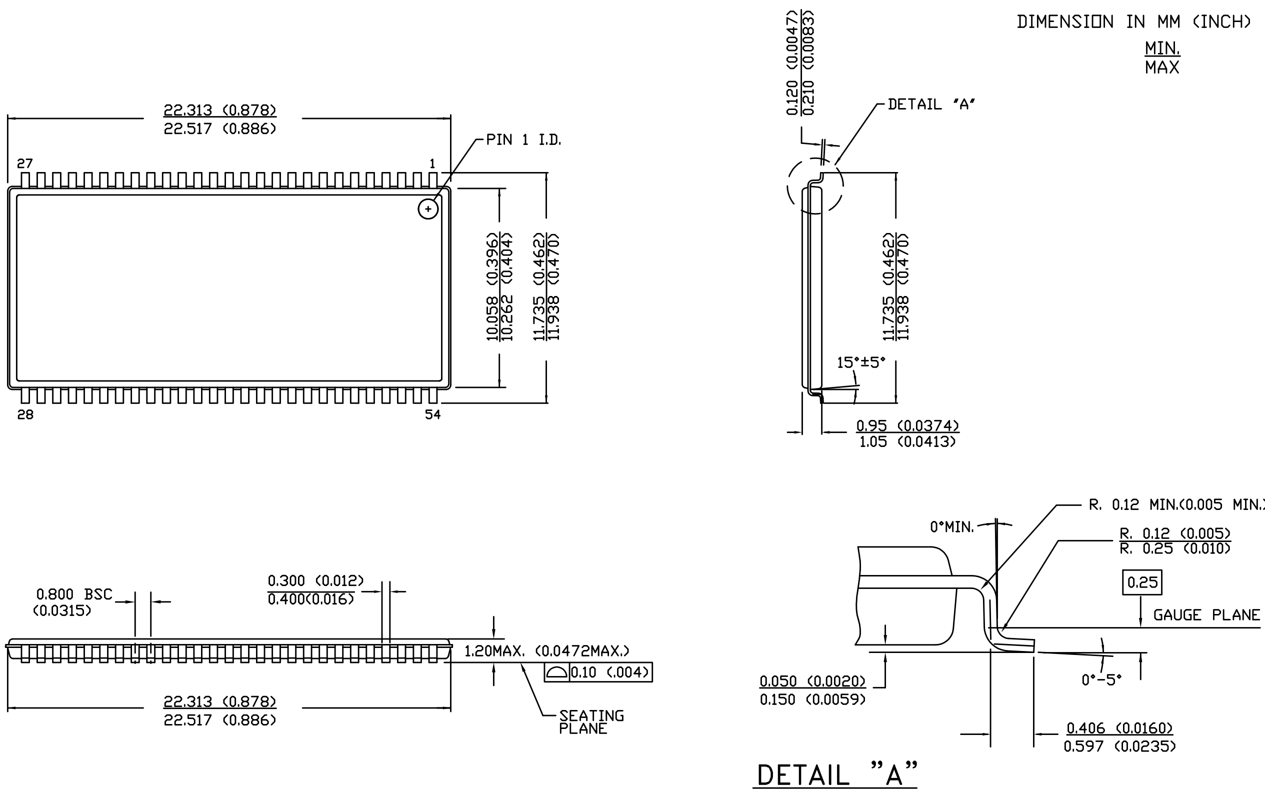
Figure 17. 44-pin TSOP II, 51-85087



51-85087 *C

Package Diagrams (continued)

Figure 18. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm), 51-85160



51-85160 *A

Acronyms

Acronym	Description
AIE	alarm interrupt enable
BCD	binary coded decimal
$\overline{\text{BHE}}$	byte high enable
$\overline{\text{BLE}}$	byte low enable
$\overline{\text{CE}}$	chip enable
CMOS	complementary metal oxide semiconductor
EIA	electronic industries alliance
$\overline{\text{HSB}}$	hardware store busy
I/O	input/output
nvSRAM	non-volatile static random access memory
$\overline{\text{OE}}$	output enable
PFE	power fail interrupt enable
RoHS	restriction of hazardous substances
RTC	real time clock
RWI	read and write inhibited
SRAM	static random access memory
TSOP	thin small outline package
$\overline{\text{WE}}$	write enable
WIE	watchdog interrupt enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
F	Farads
Hz	Hertz
kHz	kilo Hertz
kΩ	kilo ohms
MHz	Mega Hertz
µA	micro Amperes
µF	micro Farads
µs	micro seconds
mA	milli Amperes
ms	milli seconds
ns	nano seconds
Ω	ohms
%	percent
pF	pico Farads
ppm	parts per million
s	seconds
V	Volts
W	Watts

Document History Page

Document Title: CY14B108K/CY14B108M, 8-Mbit (1024 K × 8/512 K × 16) nvSRAM with Real Time Clock Document Number: 001-47378				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2681767	GVCH/PYRS	04/01/09	New Data Sheet
*A	2712462	GVCH/PYRS	05/29/2009	Moved data sheet status from Preliminary to Final Updated AutoStore operation Updated C1, C2 values to 12pF, 69pF from 21pF, 21pF respectively Updated I_{SB} test condition Updated footnote 10 Updated I_{BAK} and V_{RTCcap} parameter values Added R_{BKCHG} parameter to RTC characteristics table Added footnote 14 Referenced footnote 12 to V_{CCRISE}, t_{HHHD} and t_{LZHSB} parameters Updated V_{HDIS} parameter description
*B	2746310	GVCH	07/29/2009	Page 4: Updated Hardware STORE ($\overline{HSB}$) operation description page 4: Updated Software STORE description Updated t_{DELAY} parameter description Updated footnote 24 and added footnote 31 Referenced footnote 31 to Figure 11 and Figure 12
*C	2759948	GVCH	09/04/2009	Removed commercial temperature related specs Removed 20 ns access speed related specs Changed V_{RTCbat} max value from 3.3V to 3.6V Changed R_{BKCHG} min value from 450Ω to 350Ω Updated footnote 14
*D	2828257	GVCH	12/15/2009	Changed STORE cycles to QuantumTrap from 200K to 1 Million Updated I_{BAK} RTC backup current spec unit from nA to µA Added Contents on page 2
*E	2923475	GVCH/AESA	04/27/2010	Table 1: Added more clarity on $\overline{HSB}$ pin operation Hardware STORE (HSB) Operation: Added more clarity on $\overline{HSB}$ pin operation Table 1: Added more clarity on $\overline{BHE}/\overline{BLE}$ pin operation Updated HSB pin operation in Figure 12 Updated footnote 42 Updated Package Diagrams and Sales, Solutions, and Legal Information.
*F	3143765	GVCH	01/17/2011	Updated Setting the Clock description Added footnote 12 Updated W bit description in Register Map Detail table Updated Best Practices Updated thermal resistance values for all packages Added t_{RTCp} parameter to RTC Characteristics table Added Acronyms table and Document Conventions table
*G	3311413	GVCH	07/13/2011	Updated DC Electrical Characteristics (Added Note 14 and referred the same note in V_{CAP} parameter). Updated AC Switching Characteristics (Added Note 19 and referred the same note in Parameters).

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