SSI 78P234
2048 KBit/s PCM Interface Unit

October 1991

DESCRIPTION

The SSI 78P234 PCM Interface Unit is a bipolar integrated circuit which performs the functions of receiving and transmitting PCM signals in an Alternate-Mark-Inversion (AMI) format. The receiver accepts AMI-format line data and provides separated and synchronized TTL-level data and clock outputs. High-density bipolar three-encoded (HDB3) signals are passed through the chip transparently. The transmitter accepts TTL-level data and clock, typically HDB3-encoded, and produces AMI-format pulses of the appropriate shape for transmission. A loopback multiplexer is also provided that permits interchange of the signals between the sections. The SSI 78P234 requires a single 5V supply, and is available in both 20-pin DIP and small outline (SO) packages.

FEATURES

- **High-performance, low-cost solution for 2048 KBit/s PCM interface applications**
- **Both transmit and receive circuitry in a compact, 20-pin package**
- **Compliant with CCITT recommendations G.703 and G.823**
- **Unique clock-recovery circuit, requires no crystals or tuned components**
- **Standard unipolar TTL-level clock and data ports for easy equipment interface**
- **Line-loopback and local-loopback control**
- **Loss-of-signal indication**
- **Available in SO or dual-in-line packages**

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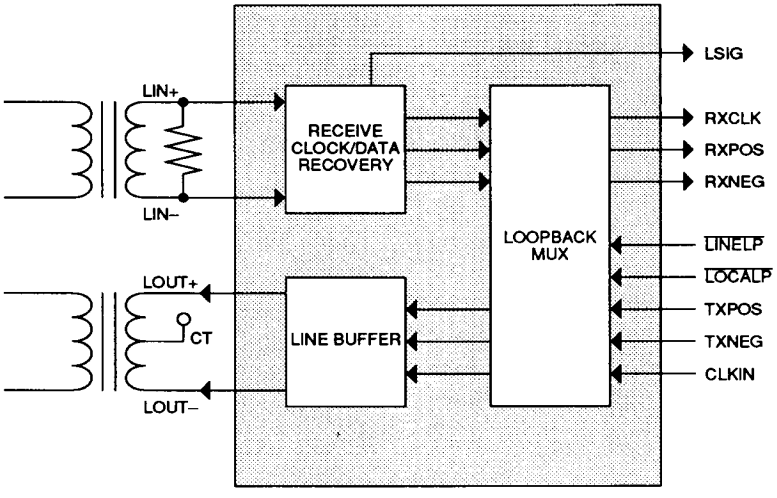
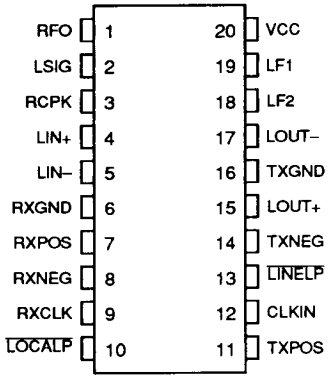
BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

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FUNCTIONAL DESCRIPTION

The device consists of receiver and transmitter sections together with a "loopback" means which permits interchange of signals between the sections (see Figure 1).

RECEIVER

The receiver input is normally transformer-coupled to the source of encoded alternate polarity pulses. To provide a tracking threshold for amplitude-detecting these pulses, the signal is peak detected and a fixed percentage of the peak value is applied to the comparators which detect individual positive and negative pulses. An external R-C network is required to provide the proper storage of the peak reference value. Should the detected peak value fall below an acceptable level, the Loss of Signal (LSIG) output becomes active. This output may be used as a logical control signal or is able to drive a fault indicator LED directly.

Outputs of the data comparators are connected to the clock recovery circuits. The clock recovery system employs a unique phase-locked-oscillator loop which has an auxiliary frequency-sensitive acquisition loop which is active only when cycle-slipping occurs between the received signal rate and the internal oscillator. This system permits the loop to independently lock to the frequency and phase of the incoming data stream without the need for high-precision and/or adjustable oscillators or tuned circuits. Non-precision external components are required, however, to establish the oscillator center frequency and loop bandwidth.

The phase-locked reference oscillator is employed to strobe the detected data into output latches and is also available as an output for externally synchronizing the data.

TRANSMITTER

The transmitter combines unipolar logical inputs with an input clock to provide positive and negative output pulses onto a transformer-coupled line. Note that the transmitter output pulse widths are determined by the input clock width, so that it must be carefully controlled to provide acceptable outputs.

The transmitter pulse selection logical function is arranged so that the simultaneous occurrence of both positive and negative transmit data inputs inhibits the output driver. Moreover, the driver has a current-limiting feature which protects the circuit in the event of a shorted load or inadvertent shorting of an output to the supply voltage.

LOOPBACK CONTROL SECTION

The loopback control section is essentially a multiplexer which is capable of directing received data and clock to the transmitter section, or directing transmit input data and clock to the receiver outputs. This "looping" is controlled by two active low logic signals, $\overline{\text{LINELP}}$ and $\overline{\text{LOCALP}}$, respectively.

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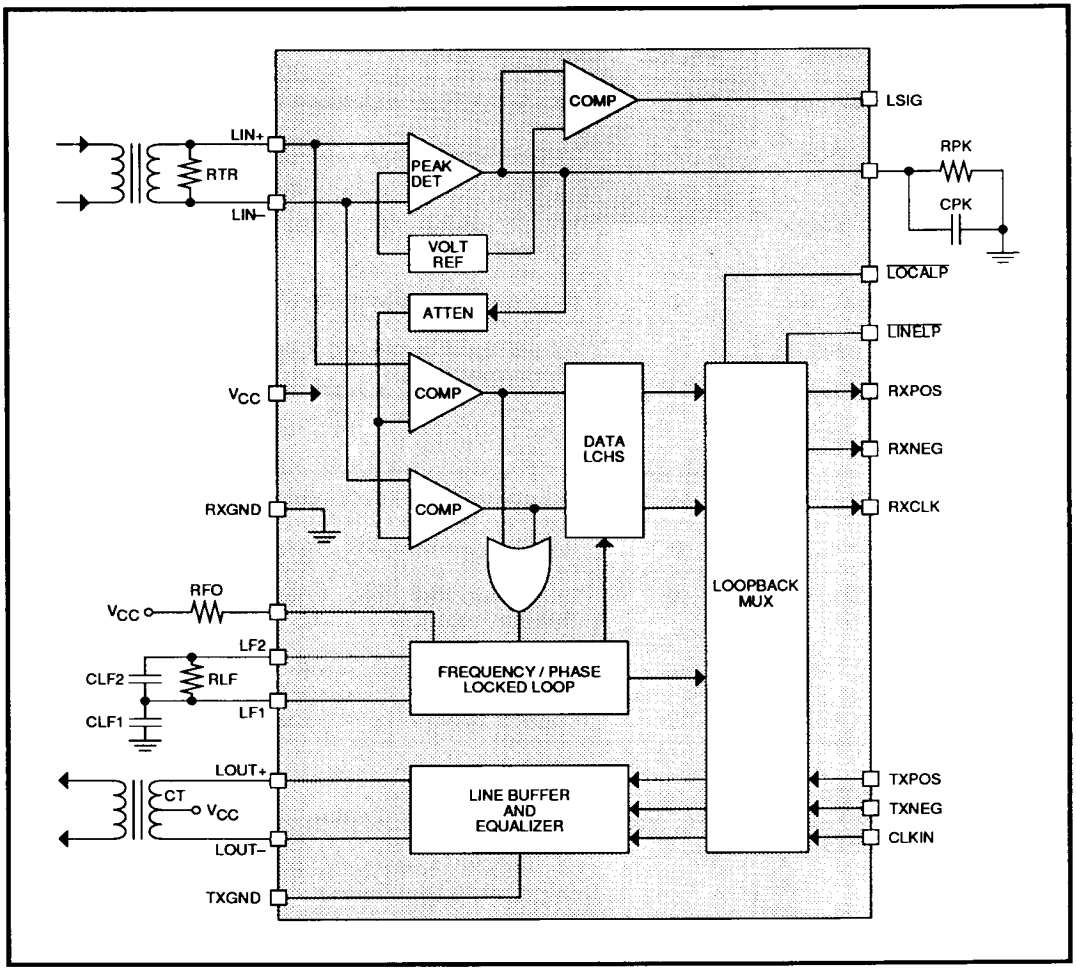

FIGURE 1: SSI 78P234 Functional Diagram

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PIN DESCRIPTION

RECEIVER

I/O	LABEL	PIN NO.	DESCRIPTION
I	LIN+, LIN-	4, 5	Differential inputs, transformer-coupled from line.
O	RXPOS	7	Unipolar receiver output, active as result of positive pulse at inputs.
O	RXNEG	8	Unipolar receiver output, active as result of negative pulse at inputs.
O	RXCLK	9	Clock pulses recovered from line data.
O	LSIG	2	Loss-of-signal output indicating that input signal is less than threshold value.

TRANSMITTER

I	TXPOS	11	Unipolar transmitter data input, active high.
I	TXNEG	14	Unipolar transmitter data input, active high.
I	CLKIN	12	Transmitter clock input. Controls transmit pulse width. Transmit is active when low.
O	LOUT+	15	Output to transformer for positive data pulses.
O	LOUT-	17	Output to transformer for negative data pulses.

LOOPBACK CONTROL

I	$\overline{\text{LINELP}}$	13	Low level causes receiver recovered data and clock to be connected to the transmitter. Data and clock continue to be present at receiver outputs.
I	$\overline{\text{LOCALP}}$	10	Low level causes transmitter input data and clock to be connected to the receiver outputs. Input data continues to be transmitted.

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PIN DESCRIPTION (Continued)

EXTERNAL COMPONENT CONNECTION

I/O	LABEL	PIN NO.	DESCRIPTION
I	RFO	1	Resistor connected to V_{CC} to provide basic center frequency of receiver phase locked loop oscillator.
-	LF1 LF2	19 18	Resistor-capacitor loop filter network to RXGND to establish bandwidth of phase locked loop.
-	RCPK	3	Parallel resistor-capacitor network connected to RXGND to determine charge/discharge characteristics of peak detector.

POWER

-	V_{CC}	20	Positive supply terminal for receiver circuits.
-	RXGND	6	Ground terminal for receiver circuits.
-	TXGND	16	Ground terminal for transmitter driver circuits.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise noted. Operation above absolute maximum ratings may permanently damage the device.)

PARAMETER	RATING
V_{CC}, Supply Voltage	-0.5 to +7.0V
Storage Temperature	-65 to 130°C
Soldering Temperature (10 sec.)	260°C
Voltage Applied to Logic Inputs	-0.5 to +7.0V
Maximum Power Dissipation	600 mW
Junction Operating Temperature	0 to +130°C

NOTE: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.

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RECOMMENDED OPERATING CONDITIONS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Ta	Ambient temperature		0		70	°C
V_{CC}	Power supply voltage		4.75		5.25	V
VIH	High-level input voltage		2.0			V
VIL	Low-level input voltage				0.8	V
IOH	High-level output current	LSIG pin only; VO = 1.5V	-7		-13	mA

EXTERNAL COMPONENTS (Refer to Figure 1 for location of components.)

RFO	Loop center frequency resistor			6.04		KΩ
RLF	Loop filter resistor			10		KΩ
CLF1	Loop filter capacitor			0.015		µF
CLF2	Loop filter capacitor			200		pF
RPK	Peak-detector resistor			36		KΩ
CPK	Peak-detector capacitor		0.0015	0.015	0.15	µF
	Transmit line transformer	Refer to Table 1		---		---

D. C. ELECTRICAL CHARACTERISTICS
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise specified.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
ICC	Supply current	All outputs open			100	mA
IIH	High-level input current	VIH = 2.7V			20	µA
IIL	Low-level input current	VIL = 0.4V			-0.36	mA
VOH	High-level output voltage	IOH = -400 µA	2.7			V
VOL	Low-level output voltage	IOL = 4.0 mA; IOL = 2.0 mA, LSIG pin			0.4	V
RIN	Receiver input resistance		800		1250	Ω

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DYNAMIC CHARACTERISTICS AND TIMING, TRANSMITTER

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise specified. Transmit pulse characteristics are obtained using a line transformer which has the characteristics shown in Table 1, and with the appropriate resistive load. Refer to Figure 2.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TTCF	Transmit clock repetition period			488		nsec
TTC	Transmit clock pulse width			244		nsec
TTCNT	Transmit clock negative transition time				10	nsec
TTCPT	Transmit clock positive transition time				10	nsec
TTPDS TTNDS	Transmit data set-up time		15			nsec
TTPDH TTNDH	Transmit data hold time		0			nsec
TTPL	Transmit positive line pulse width	Measured at transformer	TTC-5		TTC+5	nsec
TTNL	Transmit negative line pulse width		TTPL-5		TTPL+5	nsec
	Transmit line pulses waveshape	See Note				

Note: Characteristics are in accordance with Table 6 and Figure 15 of Rec. G.703.

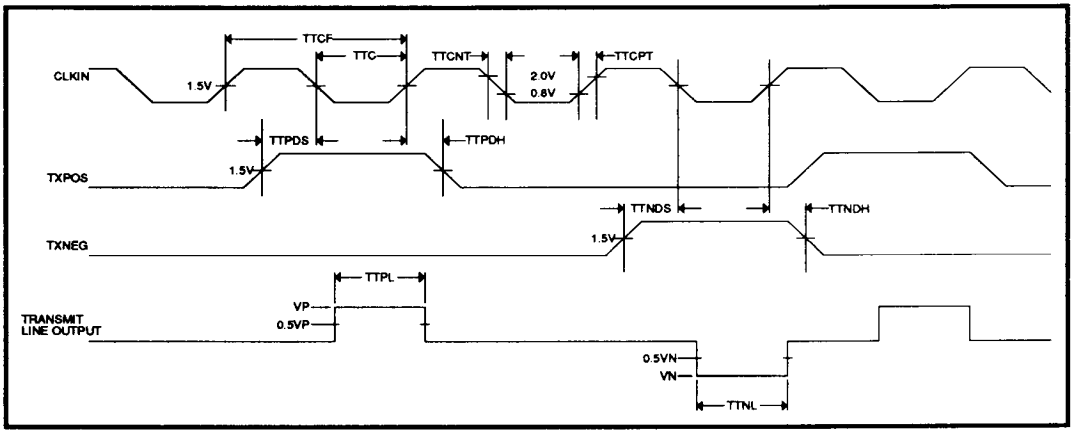

FIGURE 2: Transmit Waveforms

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DYNAMIC CHARACTERISTICS AND TIMING, RECEIVER
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise specified. External component values as specified in Recommended Operating Conditions; see Note 1. Refer to Figure 3.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIN	Input signal voltage		±1.2		±3.9	Vpk
VLOS	Loss-of-signal indicating voltage		±0.5		±1.0	Vpk
TLOS	Loss-of-signal delay time	Timed from removal of input signal; See Note 2	0.7 TPK		1.3 TPK	sec
VDTH	Receive data detection threshold	Relative to peak amplitude	35		45	%
TSTAB	Receiver stabilization time	After application of input signal			5	msec
TRCF	Receive clock period			488		nsec
TRC	Receive clock pulse width			244		nsec
TRCPT	Receive clock positive transition time	C_L = 15 pF			15	nsec
TRCNT	Receive clock negative transition time	C_L = 15 pF			10	nsec
TRDP TRDN	Positive or negative receive data pulse width			488		nsec
TRDPS TRDNS	Receive data set-up time		210			nsec
TRDPH TRDNH	Receive data hold time		210			nsec
	Receive input jitter tolerance high frequency	sine, 18 KHz to 100 KHz	±100			nsec
	Receive input jitter tolerance low frequency	sine, 2.4 KHz	±750			nsec
KD	Clock Recovery Phase Detector Gain	(All 1's Data Pattern)	66		79	µA/Rad
KO	Clock Recovery Phase Locked Oscillator Control Gain		0.40		0.55	Megrad/ sec. Volt

Note 1: Input signal is transformer coupled. In accordance with Paragraph 6.3 of Rec. G.703 and Table 2 of Rec. G.823.

Note 2: TPK = RPK x CPK x ln((VIN + 1.2v)/(VLOS + 1.2v))

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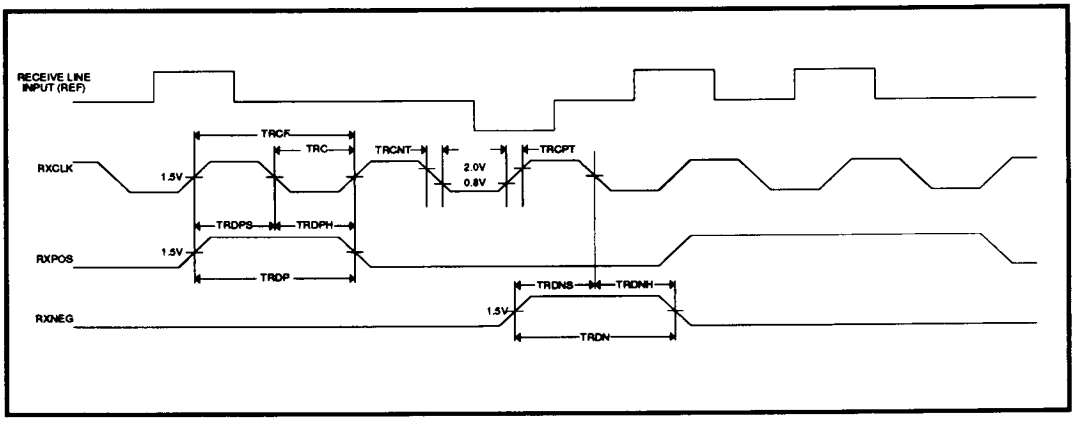

FIGURE 3: Receive Waveforms

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LINE TRANSFORMERS

The SSI 78P234 is designed to connect to 75Ω coaxial or 120Ω symmetrical pair cabling. The transmitter must meet output pulse characteristics as specified by the CCITT (Table 6 of Rec. G.703) for each of these transmission media. It is important to choose a transformer that meets the specifications shown in Table 1 (below) to assure compliance with these requirements.

CHARACTERISTIC		SYMBOL	MIN	NOM	MAX	UNIT
Turns ratio	75Ω coax	N		2.53CT:1		
	120Ω twisted pair			2CT:1		
Primary open circuit inductance		Lp	3			mH
Primary leakage inductance		L1			4.0	µH
Primary volt-time product		ET	5			V-µsec
Primary DC resistance		Rp			2.5	Ω
Interwinding Capacitance		C_w			25	pF

TABLE 1: Transmit Line Transformer Characteristics

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LINE TRANSFORMERS (Continued)

75Ω Coax Connection

Approximate turns ratios for connection to 75Ω coax are: 2.53 CT:1 for the transmitter and 1:1.26 (no CT) for the receiver. Some recommended transformers are listed in Table 2.

RCV/XMIT	TURNS RATIO	PART NUMBER	MANUFACTURER
XMIT	2.53CT:1	PE 64945	Pulse Engineering
XMIT	2.66CT:1	11816	Schott Corporation
RCV	1:1.26	PE 64938	Pulse Engineering

TABLE 2: Recommended Line Transformers for 75Ω Coax Connection

120Ω Symmetrical Pair Connection

Connection to 120Ω symmetrical pair requires a 2CT:1 ratio for the transmitter and 1:1 (no CT) on the receiver. Some recommendations are listed below.

RCV/XMIT	TURNS RATIO	PART NUMBER	MANUFACTURER
XMIT	2CT:1	1323	BH
XMIT	2CT:1	G52J12C	Pan-Mag
XMIT	2CT:1	11815	Schott Corporation
XMIT	1:1:1	PE 64931	Pulse Engineering
RCV	1:1	PE 64935	Pulse Engineering
RCV	1:1:1	G52J111P	Pan-Mag

TABLE 3: Recommended Line Transformers for 120Ω Symmetrical Pair Connection

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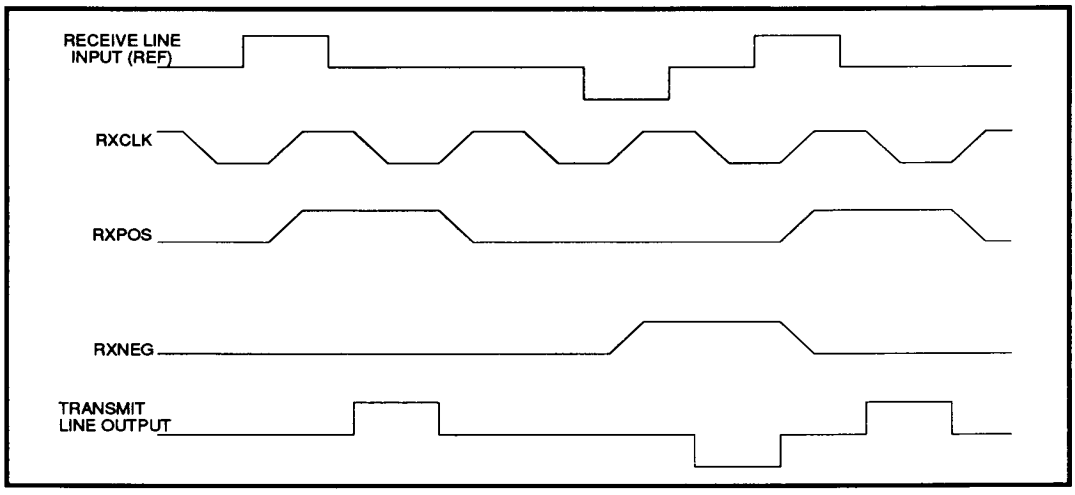

FIGURE 4: Line Loopback Waveforms

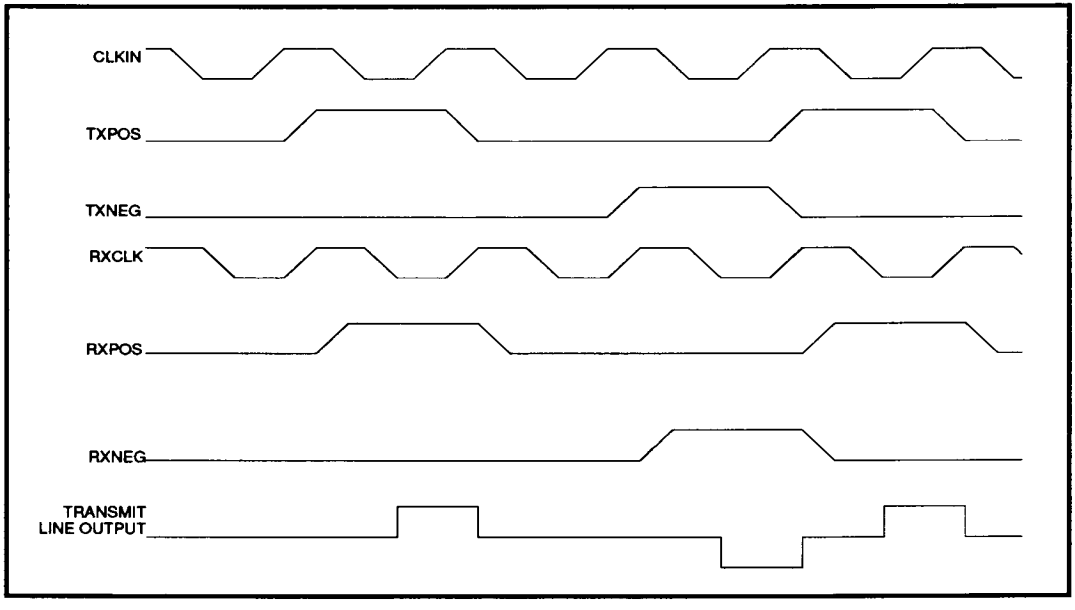

FIGURE 5: Local Loopback Waveforms

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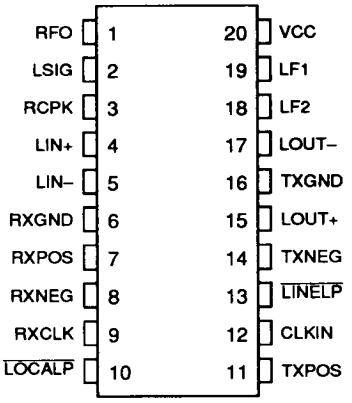
PACKAGE PIN DESIGNATIONS

(Top View)



20-Pin DIP, SO

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PACKAGE MARK
SSI 78P234		
20-Pin Plastic DIP	78P234-CP	78P234-CP
20-Pin SO	78P234-CL	78P234-CL

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