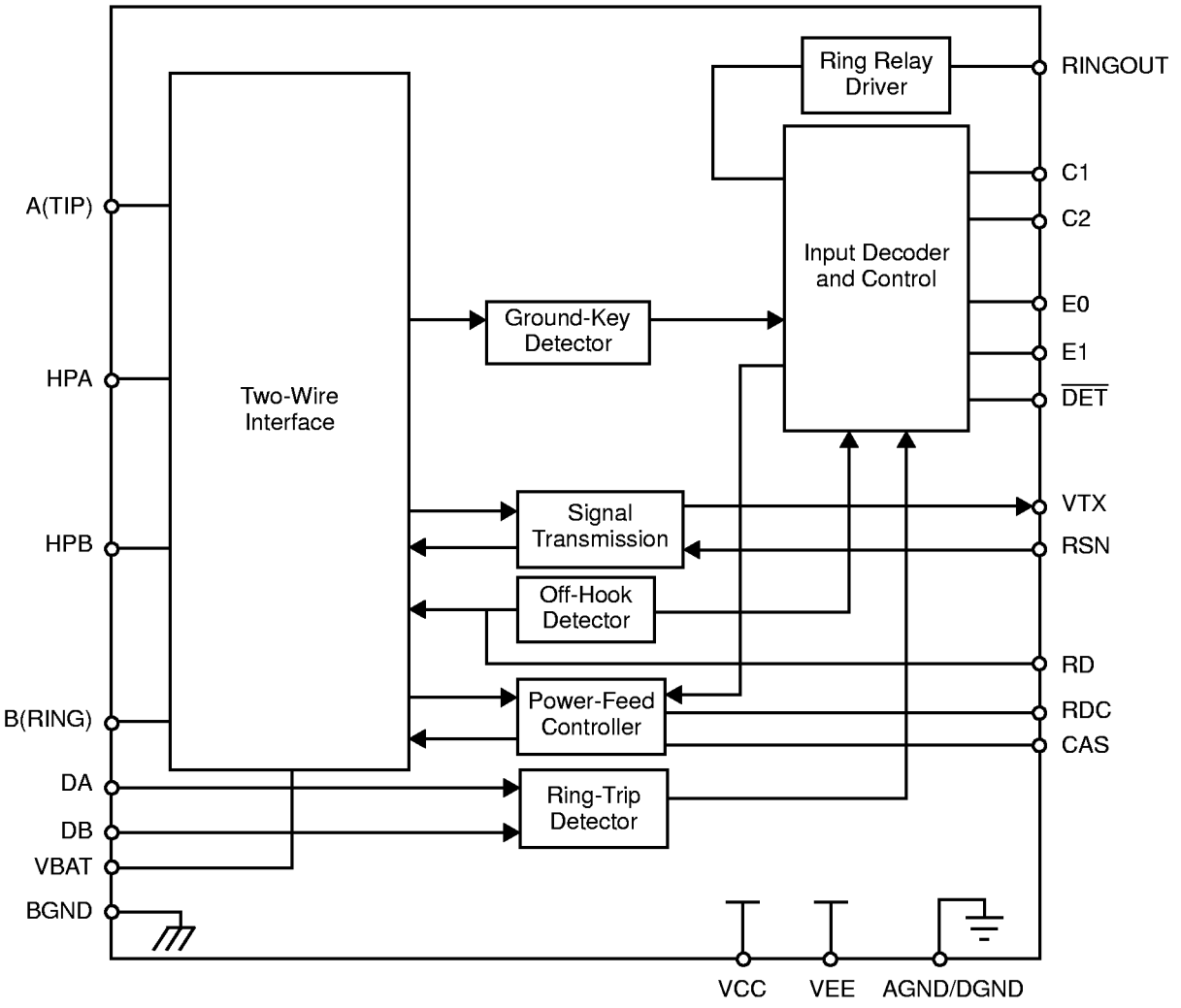
Am79467

Subscriber Line Interface Circuit

DISTINCTIVE CHARACTERISTICS

- Optimized for long-loop operation
- Programmable constant-current feed
- Programmable loop-current detector
- Programmable ground-key detector
- Low standby power
- On-hook transmission
- –24 V to –58 V battery operation
- On-chip relay driver
- Two-wire impedance set by single external impedance

BLOCK DIAGRAM



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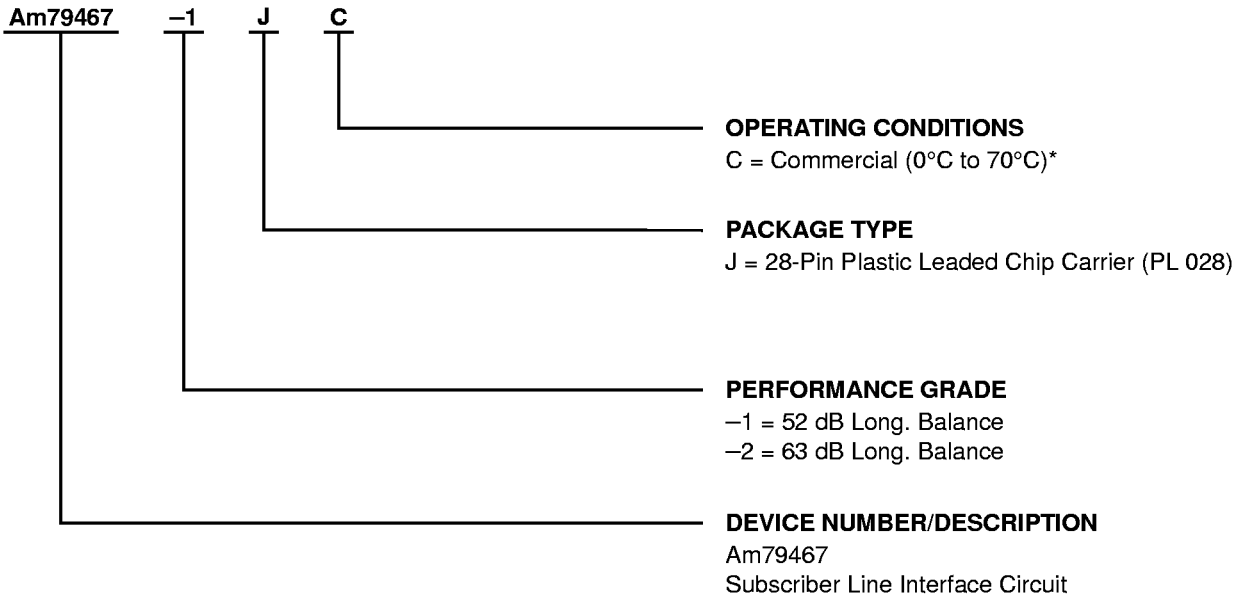
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations		
Am79467	–1 –2	JC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

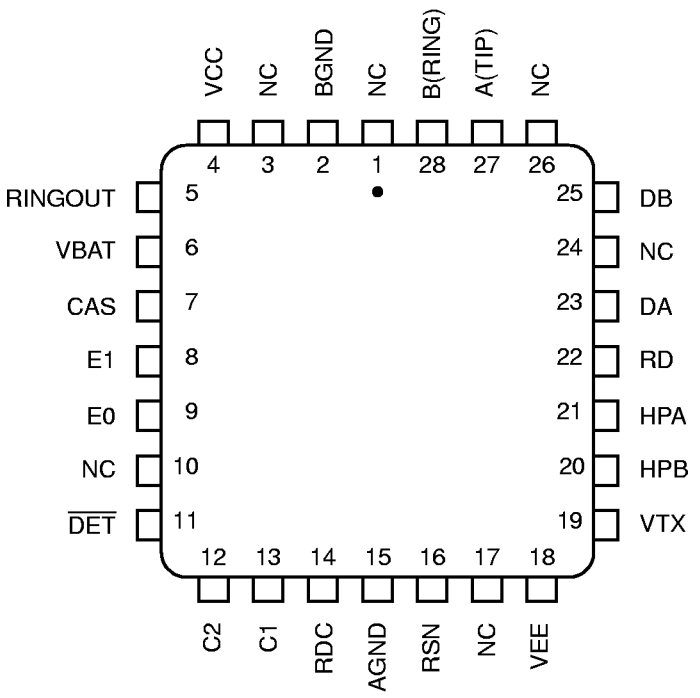
Note:

** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

CONNECTION DIAGRAMS

Top View

28-Pin PLCC



Notes:

1. *Pin 1 is marked for orientation.*
2. *NC = No connect*

PIN DESCRIPTIONS

Pin Names	Type	Description
AGND/DGND	Ground	Analog and digital ground.
A(TIP)	Output	Output of A(TIP) power amplifier.
BGND	Ground	Battery (power) ground.
B(RING)	Output	Output of B(RING) power amplifier.
C2–C1	Input	Decoder. SLIC control pins. C2 is MSB and C1 is LSB. TTL compatible.
CAS	Capacitor	Anti-saturation capacitor pin for capacitor to filter reference voltage when operating in anti-saturation region.
DA	Input	Ring-Trip negative. Negative input to ring-trip comparator.
DB	Input	Ring-Trip positive. Positive input to ring-trip comparator.
$\overline{\text{DET}}$	Output	Switchhook detector. When enabled, a logic Low indicates that selected condition is detected. The detect condition is selected by the logic inputs (C2–C1 and E0–E1). The output is open-collector with a built-in 15 kΩ pull-up resistor.
E0	Input	$\overline{\text{DET}}$ enable. A logic High disables $\overline{\text{DET}}$. A logic Low enables $\overline{\text{DET}}$.
E1	Input	Ground-key enable. A logic High connects the off-hook/ring-trip detector to $\overline{\text{DET}}$, and a logic Low connects the ground-key/ring-trip detector to $\overline{\text{DET}}$.
HPA	Capacitor	High-pass filter capacitor. A(TIP) side of high-pass filter capacitor.
HPB	Capacitor	High-pass filter capacitor. B(RING) side of high-pass filter capacitor.
NC	—	No connect. This pin not internally connected.
RD	Resistor	Detect resistor. Detector threshold set and filter pin.
RDC	Resistor	DC feed resistor. Connection point for the DC feed current programming network. The other end of the network connects to the receiver summing node (RSN). V_{RDC} is negative for normal polarity and positive for reverse polarity.
RINGOUT	Output	Ring relay driver. Open-collector driver with emitter internally connected to BGND.
RSN	Input	Receiver summing node. The metallic current (AC and DC) between A(TIP) and B(RING) is equal to 1000 times the current into this pin. The networks that program receive gain, two-wire impedance, and feed resistance all connect to this node.
VBAT	Battery	Battery supply.
VCC	Power	+5 V power supply.
VEE	Power	–5 V power supply.
VTX	Output	Transmit audio. This output is a unity gain version of the A(TIP) and B(RING) metallic voltage. VTX also sources the two-wire input impedance programming network.

ABSOLUTE MAXIMUM RATINGS

Storage temperature . . . . . –60°C to +150°C

V_{CC} with respect to AGND/DGND . . . . . 0.5 V to +7 V

V_{EE} with respect to AGND/DGND . . . . . 0.5 V to –7 V

V_{BAT} with respect to AGND/DGND . . . 0.5 V to –70 V

BGND with respect to AGND/DGND . . . +3 V to –3 V

A(TIP) or B(RING) to BGND:

- Continuous . . . . . V_{BAT} to +2 V
- 10 ms (f = 0.1 Hz) . . . . . V_{BAT} – 20 V to +5 V
- 1 µs (f = 0.1 Hz). . . . . V_{BAT} – 40 V to +10 V
- 250 ns (f = 0.1 Hz) . . . . . V_{BAT} – 70 V to +15 V

Current from A(TIP) or B(RING). . . . . 70 mA

Current through relay driver . . . . . 50 mA

Ring relay supply voltage. . . . . 0 V to V_{BAT} + 75 V

DA and DB inputs:

- Voltage on ring-trip inputs . . . . . V_{BAT} to 0 V
- Current into ring-trip inputs . . . . . ±5 mA

C2–C1, E0, E1, $\overline{DET}$

- Input voltage . . . . . 0 V to V_{CC}
- Output voltage ($\overline{DET}$ not active) . . . . . 0 V to V_{CC}
- Output current ($\overline{DET}$) . . . . . 5 mA

Power Dissipation ($T_A \leq 70°C$):

- Continuous . . . . . 1.5 W
- Peak (t < 100 ms, t_{REP} > 1 s) . . . . . 4 W

Note: *Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never be exposed to this temperature. Operation above 145°C junction temperature may degrade device reliability. See the SLIC Packaging Considerations for more information.*

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient temperature . . . . . 0°C to +70°C*

V_{CC} . . . . . 4.75 V to 5.25 V

V_{EE} . . . . . –4.75 V to –5.25 V

V_{BAT} . . . . . –24 V to –58 V

AGND/DGND . . . . . 0 V

BGND with respect to AGND/DGND . . . . . –100 mV to +100 mV

Operating Ranges define those limits between which device functionality is guaranteed.

** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

ELECTRICAL CHARACTERISTICS

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Transmission Performance						
2-wire return loss	200 Hz to 500 Hz 500 Hz to 1 kHz 1.0 kHz to 3.4 kHz	25 27 23			dB	1, 4
Z_{VTX}, Analog output impedance			3	20	Ω	4
V_{VTX}, Analog output offset voltage	0°C to +70°C –40°C to +85°C	–35 –40		+35 +40	mV	— 4
Overload level, 2-wire and 4-wire	R_L = 600 Ω	3.1			Vpk	2
Overload level	Load impedance > 20 kΩ	3.1				
THD, Total harmonic distortion	1.0 kHz, 0 dBm		–65	–54	dB	5
THD, on-hook	0 dBm, R_L = 900 Ω, Battery = –51 V			–35.5		
Longitudinal Performance						
Longitudinal to metallic L-T, L-4 balance	200 Hz to 3.4 kHz –1 parts*	52			dB	
Longitudinal to metallic L-T, L-4 balance	200 Hz to 1 kHz: –2 parts* 0°C to +70°C –40°C to +85°C	 63 55				— 4
	1 kHz to 3.4 kHz: –2 parts* 0°C to +70°C –40°C to +85°C	 58 55				— 4
Longitudinal signal generation 4-L	200 Hz to 4 kHz, normal polarity	45	55			
Longitudinal current per pin (A or B)	Active state	25	35		mArms	
Longitudinal impedance (A or B)	0 Hz to 100 Hz		20	35	Ω/pin	
Idle Channel Noise						
C-message weighted noise	2-wire: 0°C to +70°C –40°C to +85°C		+7	+10 +12	dBrnC	— 4
	4-wire: 0°C to +70°C –40°C to +85°C		+7	+10 +12		— 4
Psophometric weighted noise	2-wire: 0°C to +70°C –40°C to +85°C		–83	–80 –78	dBmp	4
	4-wire: 0°C to +70°C –40°C to +85°C		–83	–80 –78		
Receive Summing Node (RSN)						
RSN DC voltage	I_{RSN} = 0 mA		0		V	4
RSN impedance	200 Hz to 3.4 kHz		10	20	Ω	
RSN current to metallic loop-current gain	300 Hz to 3.4 kHz 0°C to +70°C –40°C to +85°C	988 980	1000 1000	1012 1020		

Note:
** Performance Grade*

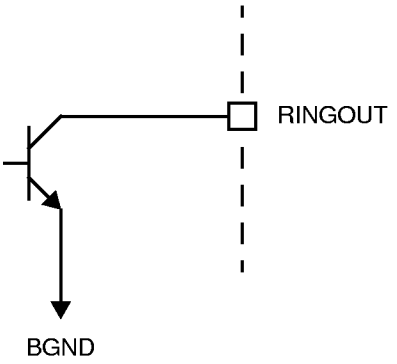
ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Insertion Loss and Balance Return Signal (2-Wire to 4-Wire, 4-Wire to 2-Wire, and 4-Wire to 4-Wire, See Test Circuits A and B)						
Gain accuracy over temperature	0 dBm, 1 kHz 0°C to +70°C −40°C to +85°C	−0.15 −0.20	0 0	+0.15 +0.20	dB	3 4
Gain accuracy over frequency	300 Hz to 3.4 kHz (relative to 1 kHz): 0°C to +70°C −40°C to +85°C	−0.10 −0.15		+0.10 +0.15	dB	3 4
Gain tracking	+3 dBm to −55 dBm (relative to 0 dBm): 0°C to +70°C −40°C to +85°C	−0.10 −0.15		+0.10 +0.15	dB	3, 4 4
Group delay	0 dBm, 1 kHz		5.3		µs	5
Line Characteristics						
Long loops, Active state	BAT = −50 V, R_{LDC} = 2000 Ω	21			mA	4
I_L, Loop current accuracy	I_L in constant-current region	$0.915I_L$	I_L	$1.085I_L$	mA	
I_L, Accuracy, Standby state	$I_L = \frac{\lvert V_{BAT}\rvert - 3\ V}{R_L + 1800}$ T_A = 25°C	$0.8I_L$	I_L	$1.2I_L$	mA	
I_L, Loop current	Disconnect, R_L = 0			100	µA	
VAB, Open Circuit voltage	V_{BAT} = −50 V	42.8			V	
Power Supply Rejection Ratio (V_{RIPPLE} = 100 mVrms), Active Normal State						
V_{CC} V_{EE} V_{BAT}	50 Hz to 3.4 kHz 50 Hz to 3.4 kHz 50 Hz to 3.4 kHz	30 30 35	40 36 41		dB	5
Effective internal resistance	CAS pin to GND		60		kΩ	4
Off-Hook Detector						
On-threshold	R_D = 33 kΩ	11.3		17.3	mA	
Off-threshold	R_D = 33 kΩ	9.85		14.7	mA	
Hysteresis	R_D = 33 kΩ	0		3.2	mA	
Power Dissipation, Battery = −58 V						
On-hook Open Circuit state			25		mW	
On-hook Standby state			50		mW	
On-hook Active state	R_L = ∞, V_{BAT} = −50 V		145	300	mW	
Off-hook Active state	R_L = 0 Ω R_L = 300 Ω R_L = 600 Ω		1.5 1.4 1.2	1.8 1.6 1.4	W	

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Supply Currents, Battery = −58 V						
I_{CC}, on-hook V_{CC} supply current	Open Circuit state Standby state Active state, V_{BAT} = −50 V		1.2 1.7 4.8	2.0 2.5 6.5	mA	
I_{EE}, on-hook V_{EE} supply current	Open Circuit state Standby state Active state, V_{BAT} = −50 V		0.5 0.9 1.9	1.3 1.6 3.0		
I_{BAT}, on-hook V_{BAT} supply current	Open Circuit state Standby state Active state, V_{BAT} = −50 V		0.3 0.7 2.6	1.2 1.6 4.5		
Ground-Key Detector Thresholds						
I_A and I_B delta to trigger the ground-key detector		8	12	17	mA	
I_A and I_B delta to clear the triggered ground-key detector		3	7	12		
Hysteresis		3	5	8		
Ring-Trip Detector Input						
Bias current		−500	−100		nA	
Offset voltage	Source resistance = 0 to 2 MΩ	−50	0	+50	mV	
Input resistance	Unbalanced Balanced	1 3			MΩ	4
Input common mode range		V_{BAT}		−2	V	
Logic Inputs (C2–C1, E0, E1)						
V_{IH}, Input High voltage		2.0			V	
V_{IL}, Input Low voltage				0.8		
I_{IH}, Input High current	All inputs except E1	−75		40	µA	
Input High current	Input E1	−75		45		
I_{IL}, Input Low current		−500				
Logic Output ($\overline{DET}$)						
V_{OH}, Output Low voltage	I_{OUT} = 0.8 mA, 15 kΩ to V_{CC}			0.40	V	
V_{OL}, Output High voltage	I_{OUT} = −0.1 mA, 15 kΩ to V_{CC}	2.4				
Internal pull-up resistor		8		25	kΩ	
Relay Driver Output (RINGOUT)						
On voltage	I_{OL} = 25 mA		+0.2	+0.75	V	
Off leakage	V_{OH} = +12 V			10	µA	

RELAY DRIVER SCHEMATIC

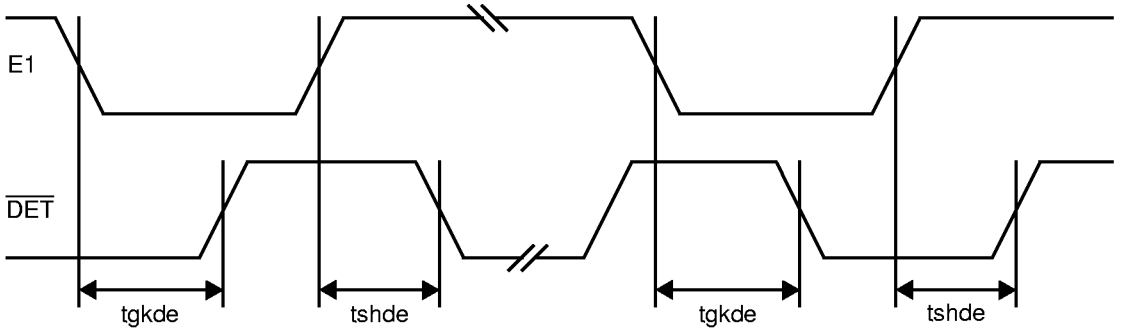


SWITCHING CHARACTERISTICS

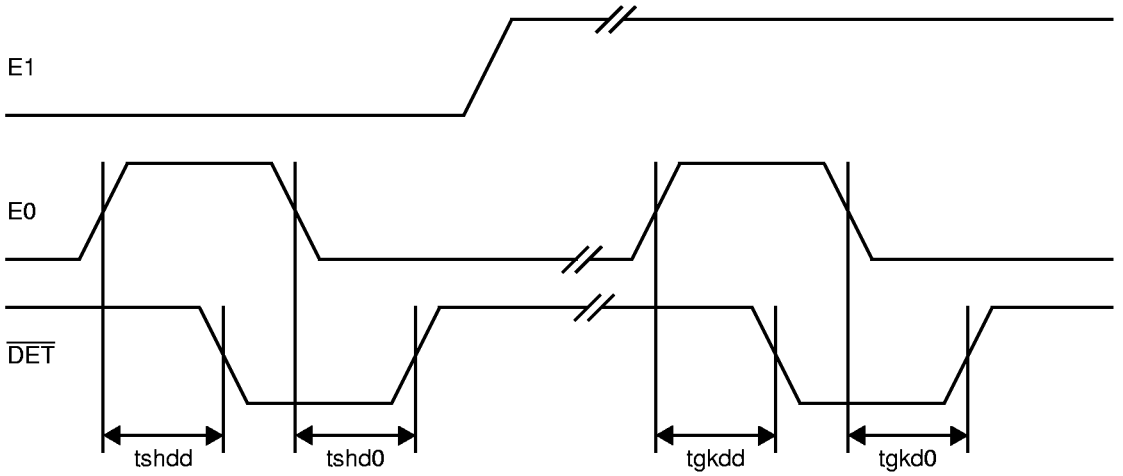
Symbol	Parameter	Test Conditions	Temperature Ranges	Min	Typ	Max	Unit	Note
tgkde	E1 Low to $\overline{DET}$ High (E0 = 1)	Ground-Key Detect state R_L open, R_G connected (See Figures E and F)	0°C to +70°C −40°C to +85°C			3.8 4.0	µs	4
	E1 Low to $\overline{DET}$ Low (E0 = 1)		0°C to +70°C −40°C to +85°C			1.1 1.6		
tgkdd	E0 High to $\overline{DET}$ Low (E1 = 0)		0°C to +70°C −40°C to +85°C			1.1 1.6		
tgkd0	E0 Low to $\overline{DET}$ High (E1 = 0)		0°C to +70°C −40°C to +85°C			3.8 4.0		
tshde	E1 High to $\overline{DET}$ Low (E0 = 1)	Switchhook Detect state R_L = 600 Ω, R_G open (See Figures E and F)	0°C to +70°C −40°C to +85°C			1.2 1.7		
	E1 High to $\overline{DET}$ High (E0 = 1)		0°C to +70°C −40°C to +85°C			3.8 4.0		
tshdd	E0 High to $\overline{DET}$ Low (E1 = 1)		0°C to +70°C −40°C to +85°C			1.1 1.6		
tshd0	E0 Low to $\overline{DET}$ High (E1 = 1)		0°C to +70°C −40°C to +85°C			3.8 4.0		

SWITCHING WAVEFORMS

E1 to $\overline{\text{DET}}$



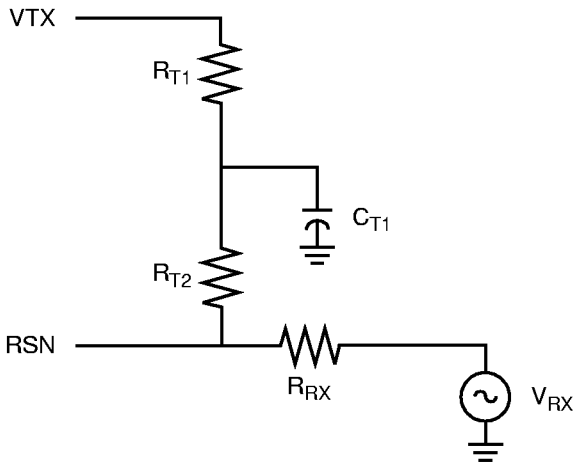
E0 to $\overline{\text{DET}}$



Note:
All delays measured at 1.4 V level.

Notes:

1. *Unless otherwise noted, test conditions are BAT = –52 V, V_{CC} = +5 V, V_{EE} = –5 V, R_L = 600 Ω, C_{HP} = 18 nF, R_{DC1} = R_{DC2} = 52.3 kΩ, C_{DC} = 0.68 µF, R_D = 33 kΩ, no fuse resistors, D_1 = 1N400x, two-wire AC input impedance is a 600 Ω resistance synthesized by the programming network shown below.*



Where: R_{T1} = R_{T2} = R_{RX} = 300 kΩ, C_{T1} = 150 pF*

* C_{T1} is not required when 23 dB two-wire return loss at higher voice frequencies is acceptable. If C_{T1} is not used, R_{T1} and R_{T2} can be combined into one resistor. If this SLIC is used with a DSLAC™ device, C_{T1} is not required.

2. *Overload level is defined when THD = 1%.*
3. *Balance return signal is the signal generated at V_{TX} by V_{RX}. This specification assumes the two-wire AC load impedance matches the programmed impedance.*
4. *Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.*
5. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*

Table 1. SLIC Decoding

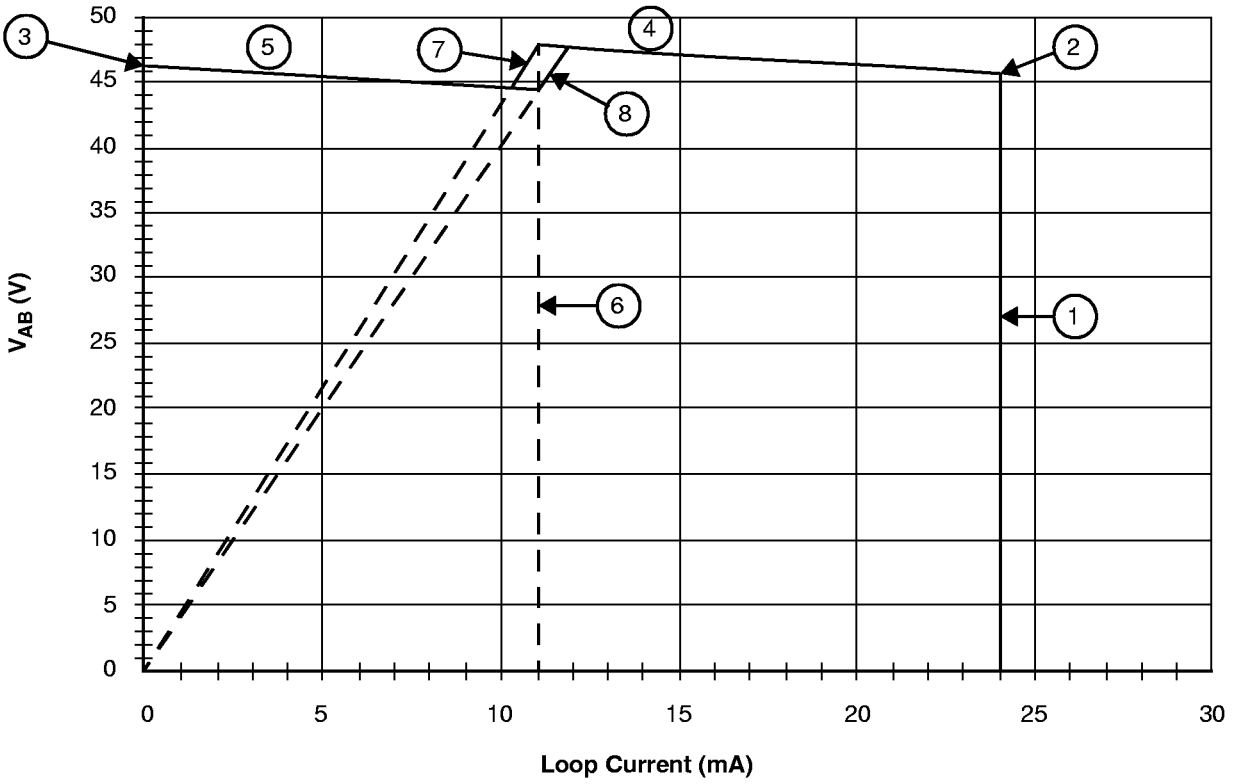
State	E1	C1	C2	Two-Wire Status	Detector Mode	$\overline{\text{DET}}$ Output
0	0	0	0	Open Circuit	No active detector	Logic level High
1	0	0	1	Active	Ground-key detector	Ground key
2	0	1	0	Ringing	No active detector	Logic level High
3	0	1	1	Standby	Ground-key detector	Ground key
4	1	0	0	Open Circuit	No active detector	Logic level High
5	1	0	1	Active	Loop-current detector	Loop-current status
6	1	1	0	Ringing	Ring-trip detector	Ring-trip status
7	1	1	1	Standby	Loop-current detector	Loop-current status

Note:
E0 = 1. For E0 = 0, $\overline{\text{DET}}$ = logic level High.

Table 2. User-Programmable Components

$Z_T = 1000(Z_{2WIN} - 2R_F)$	Where Z_T is connected between the VTX and RSN pins. The fuse resistors are R_F, and Z_{2WIN} is the desired 2-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.
$Z_{RX} = \frac{Z_T}{2}$	Where Z_{RX} is connected from V_{RX} to the RSN pin and Z_T is defined above. This equation sets the receive gain to 0 dB when the SLIC is terminated with an impedance equal to Z_{2WIN}.
$R_{DC1} + R_{DC2} = \frac{2500\ V}{I_{LOOP}}$ $C_{DC} = 30\ ms\left(\frac{1}{R_{DC1}} + \frac{1}{R_{DC2}}\right)$	Where R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the RDC pin. R_{DC1} and R_{DC2} are approximately equal. I_{LOOP} is the desired loop current in the constant-current region.
$R_D = \frac{365}{I_T}$, $C_D = \frac{0.5\ ms}{R_D}$	Where R_D and C_D form the network connected from RD to –5 V and I_T is the threshold current between on hook and off hook.
$C_{CAS} = \frac{1}{(1.2 \bullet 10^5)f_c}$	Where C_{CAS} is the regulator filter capacitor and f_c is the desired filter cut-off frequency.

DC FEED CHARACTERISTICS



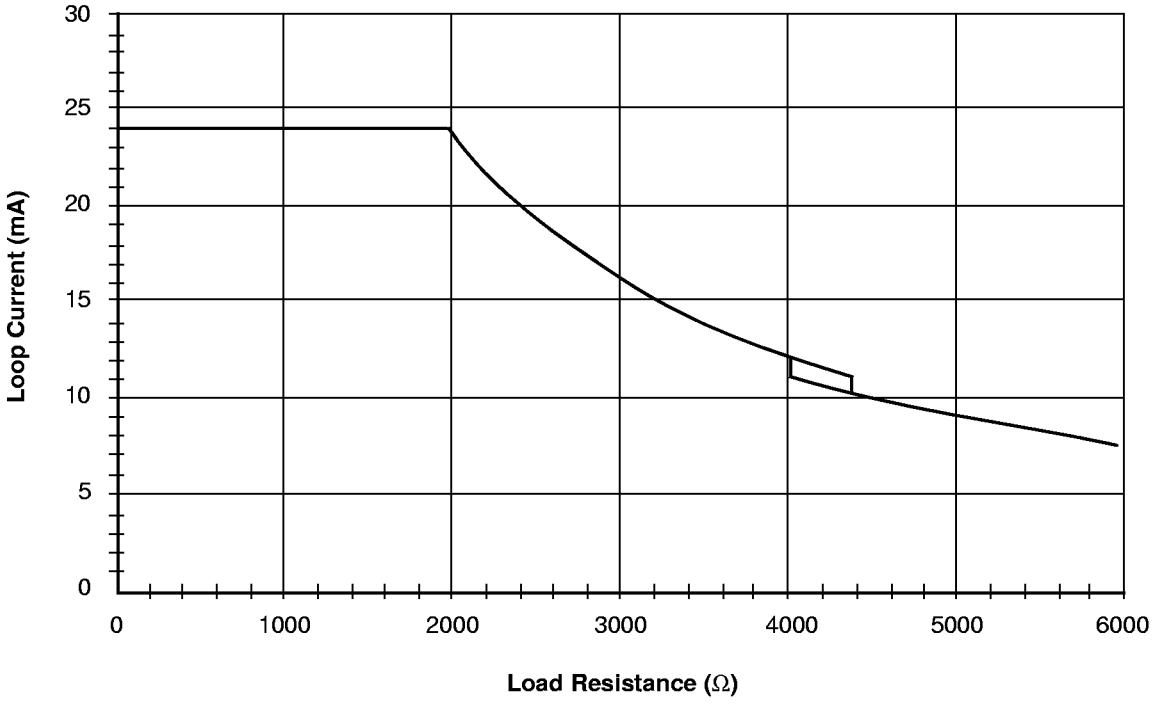
R_{DC} = 104.6 kΩ
V_{BAT} = 51.3 V
R_D = 33 kΩ

Notes:

1. *Constant-current region:* $I_L = \frac{2500}{R_{DC}}$
2. *Anti-sat (battery tracking) turn-on:* $V_{AB} = 0.96|V_{BAT}| - 3.65$
3. *Open Circuit voltage:* $V_{AB} = 1.025|V_{BAT}| - 6.23$
4. *Anti-sat region ($I_L > I_{DET}$):* $V_{AB} = 0.96|V_{BAT}| - 3.65 + \frac{2500}{600} - I_L\left(\frac{R_{DC}}{600}\right)$
5. *Anti-sat region ($I_L < I_{DET}$):* $V_{AB} = 1.025|V_{BAT}| - 6.23 - I_L\left(\frac{R_{DC}}{600}\right)$
6. *Loop-detect (I_{DET}) threshold:* $I_{DET} = \frac{365}{R_D}$
7. *Anti-sat transition region, off-hook to on-hook*
8. *Anti-sat transition region, on-hook to off-hook*

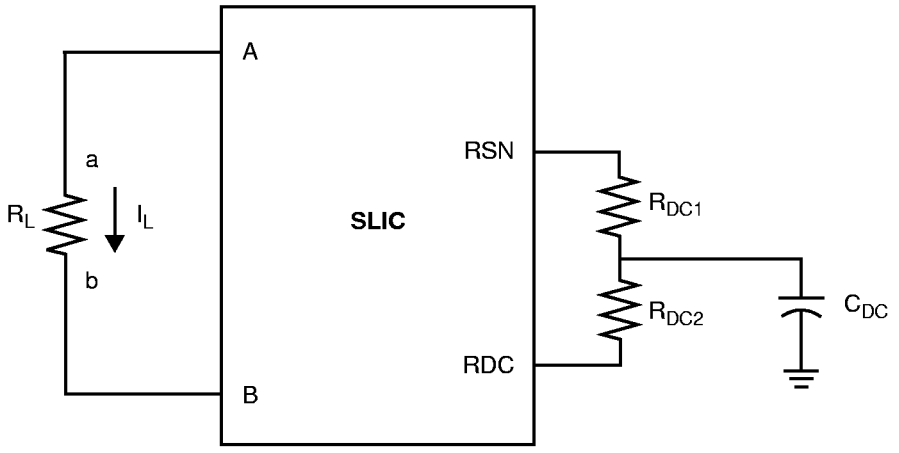
a. V_A–V_B (V_{AB}) Voltage vs. Loop Current (Typical)

DC FEED CHARACTERISTICS (continued)



R_{DC} = 104.6 kΩ
V_{BAT} = 51.3 V
R_D = 33 kΩ

b. Loop Current vs. Load Resistance (Typical)

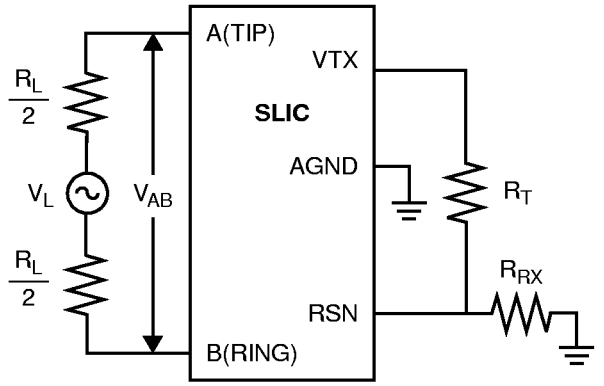


Feed current programmed by R_{DC1} and R_{DC2}

c. Feed Programming

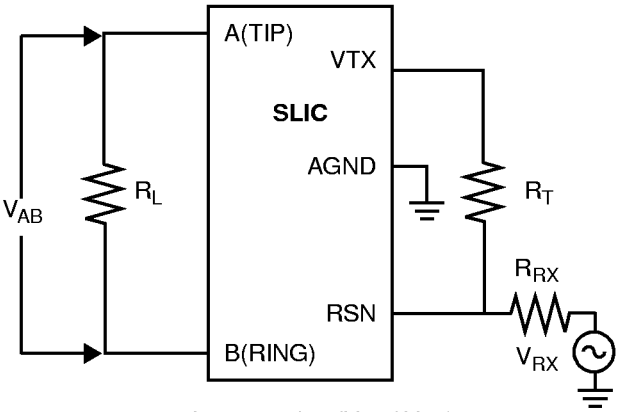
Figure 1. DC Feed Characteristics

TEST CIRCUITS



$I_{L2-4} = 20 \log (V_{TX} / V_{AB})$

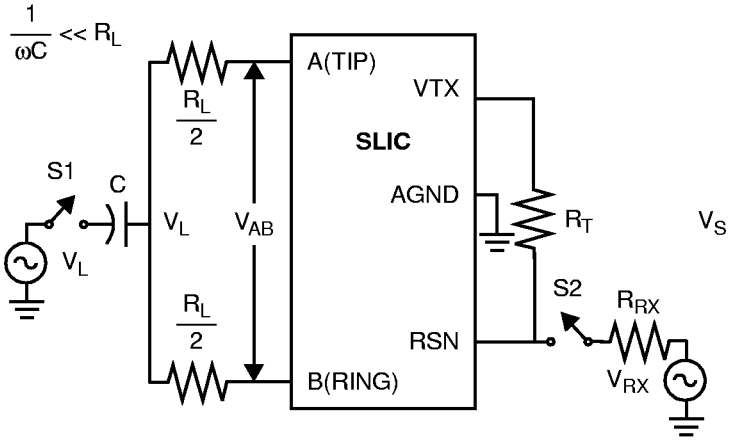
A. Two- to Four-Wire Insertion Loss



$I_{L4-2} = 20 \log (V_{AB} / V_{RX})$

$BRS = 20 \log (V_{TX} / V_{RX})$

B. Four- to Two-Wire Insertion Loss and Balance Return Signal



S2 Open, S1 Closed:

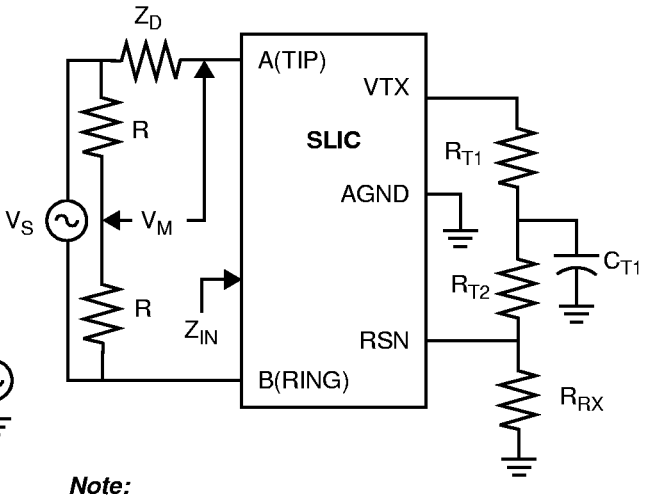
L-T Long. Bal. = 20 log (V_{AB} / V_L)

L-4 Long. Bal. = 20 log (V_{TX} / V_L)

S2 Closed, S1 Open:

4-L Long. Sig. Gen. = 20 log (V_L / V_{RX})

C. Longitudinal Balance



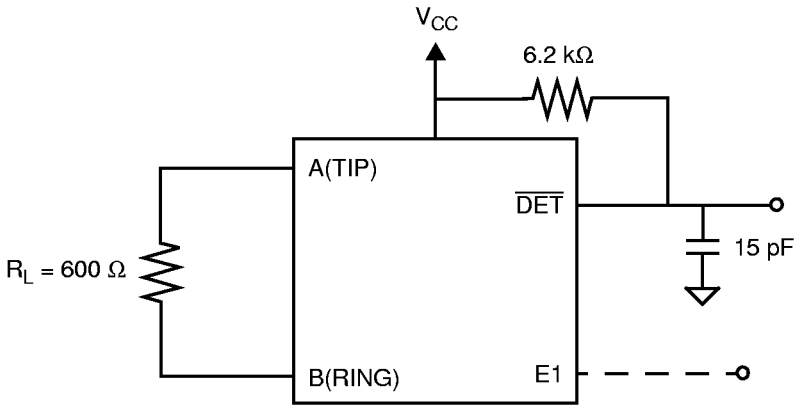
Note:

Z_D is the desired impedance (e.g., the characteristic impedance of the line).

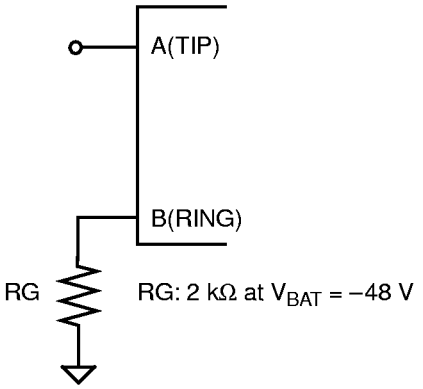
$R_L = 20 \log (2 V_M / V_S)$

D. Two-Wire Return Loss Test Circuit

TEST CIRCUITS (continued)

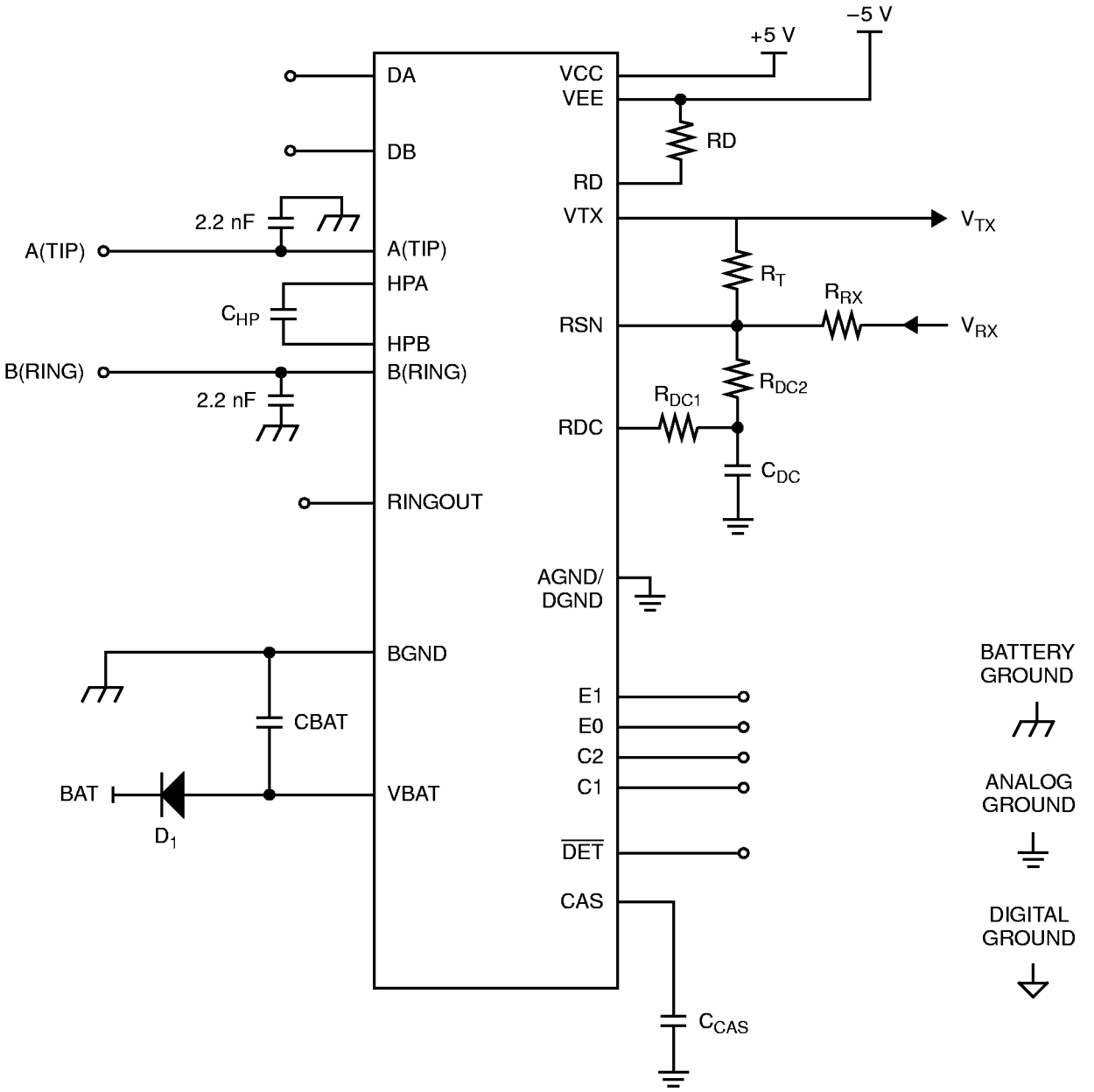


E. Loop-Detector Switching



F. Ground-Key Switching

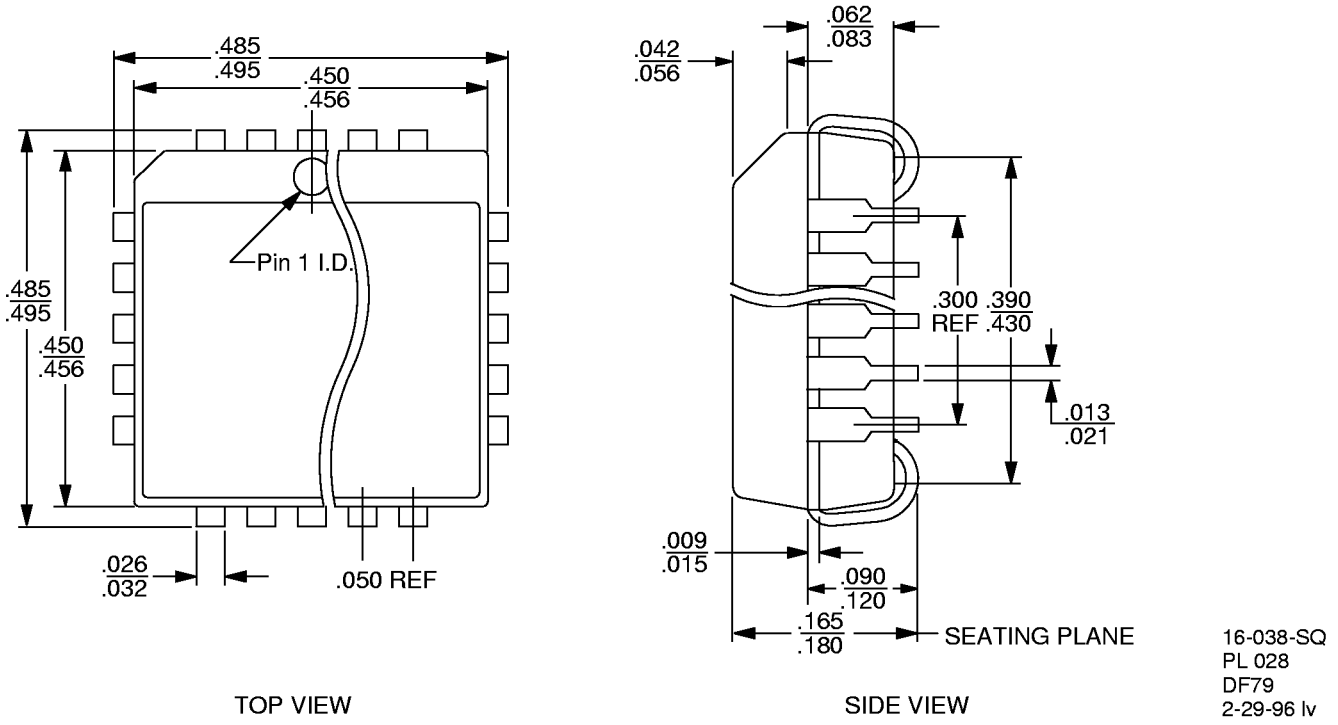
TEST CIRCUITS (continued)



G. Am79467 Test Circuit

PHYSICAL DIMENSION

PL028



TOP VIEW

SIDE VIEW

REVISION SUMMARY

Revision A to Revision B

- Minor changes to the data sheet style and format were made to conform to AMD standards.
- Electrical Characteristics—Under Longitudinal Performance, the specifications for Longitudinal to Metallic moved from the Typ column to the Min column.
- Table 2—The equation on the second row was revised.

Revision B to Revision C

- Minor changes to the data sheet style and format were made to conform to AMD standards.

Revision C to Revision D

- The physical dimension (PL028) was added to the Physical Dimension section.
- Deleted the Ceramic DIP and Plastic DIP packages and references to them.
- Updated the Pin Description table to correct inconsistencies.