Integrated Device Technology, Inc.

512K x 8 CMOS STATIC RAM MODULE

PRELIMINARY
IDT7M4048

T-46-23-14

FEATURES:

- High density 4 megabit CMOS static RAM module
- Equivalent to the JEDEC standard for future monolithic 512K x 8 static RAMs
- Fast access time: 17ns (max.)
- Low power consumption (L version)
  - — Active: 110mA (max.)
  - — CMOS Standby: 1.4mA (max.)
  - — Data Retention: 800µA (max.) Vcc = 2V
- Surface mounted LCCs (leadless chip carriers) on a 32-pin, 600 mil ceramic DIP substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible

DESCRIPTION:

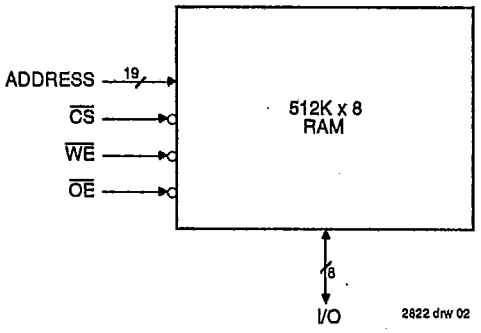
The IDT7M4048 is a 4 megabit (512K x 8) CMOS static RAM module constructed on a co-fired ceramic substrate using four 1 Megabit static RAMs and a decoder. The IDT7M4048 is available with access times as fast as 17ns. For low power applications, the IDT7M4048 version offers a data retention current of 800µA and a standby current of 1.4mA.

The IDT7M4048 is packaged in a 32-pin ceramic DIP. This results in a package 1.7 inches long and 0.6 inches wide, packing 4 megabits into the JEDEC DIP footprint.

All inputs and outputs of the IDT7M4048 are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

All IDT military module semiconductor components are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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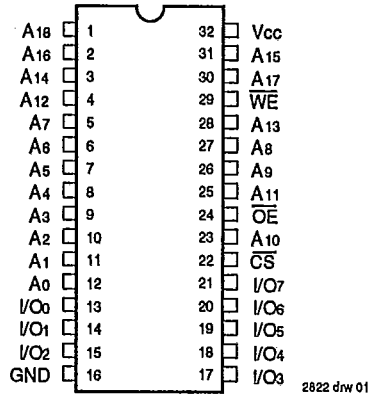
MILITARY TEMPERATURE RANGE APRIL 1992

DSC-7074/1

PIN CONFIGURATION



2822 drw 01

DIP
TOP VIEW

PIN NAMES

I/O0-7	Data Inputs/Outputs
A0-18	Addresses
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
Vcc	Power
GND	Ground

2822 tbl 01

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	DOUT	Active
Read	L	H	H	High-Z	Active
Write	L	X	L	DIN	Active

2822 tbl 09

CAPACITANCE[1] (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	50	pF
CIN(C)	Input Capacitance ($\overline{CS}$)	VIN = 0V	10	pF
COUT	Output Capacitance	VOUT = 0V	40	pF

NOTE:
1. This parameter is guaranteed by design, but not tested.

2822 tbl 10

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Military	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TA	Operating Temperature	-55 to +125	°C
TBIAS	Temperature Under Bias	–65 to +135	°C
TSTG	Storage Temperature	–65 to +160	°C
IOUT	DC Output Current	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2822 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6	V
VIL	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE:
1. VIL = -2.0V for pulse width less than 10ns.

2822 tbl 03

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%

2822 tbl 04

DC ELECTRICAL CHARACTERISTICS

(Vcc = 5V ± 10%, TA = -55°C to +125°C)

Symbol	Parameter	Test Conditions	7M4048SxxCB, 7M4048LxxCB				Unit
			17ns-55ns		60ns-120ns		
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage	Vcc = Max., VIN = GND to Vcc	—	20	—	20	µA
$\|I_{LO}\|$	Output Leakage	Vcc = Max., $\overline{CS}$ = VIH, VOUT = GND to Vcc	—	20	—	20	µA
VOL	Output Low Voltage	Vcc = Min., IOL = 2mA(1), IOL = 8mA(2)	—	0.4	—	0.4	V
VOH	Output High Voltage	Vcc = Min., IOH = -1mA(1), IOH = -4mA(2)	2.4	—	2.4	—	V
ICC	Dynamic Operating Current	Vcc = Max., $\overline{CS}$ ≤ VIL; f = fMAX, Outputs Open	—	240	—	110	mA
ISB	Standby Supply Current (TTL Levels)	$\overline{CS}$ ≥ VIH, Vcc = Max., f = fMAX, Outputs Open	—	120	—	12	mA
ISB1	Full Standby Supply Current (CMOS Levels)	$\overline{CS}$ ≥ Vcc - 0.2V, VIN ≥ Vcc - 0.2V or ≤ 0.2V	—	60	—	4	mA
		Very Low Power Version(3)	—	60	—	1.4	mA

NOTES:
1. For 17ns-55ns versions only.
2. For 60ns-120ns versions only.
3. L version only.

2822 tbl 05

DATA RETENTION CHARACTERISTICS(5)

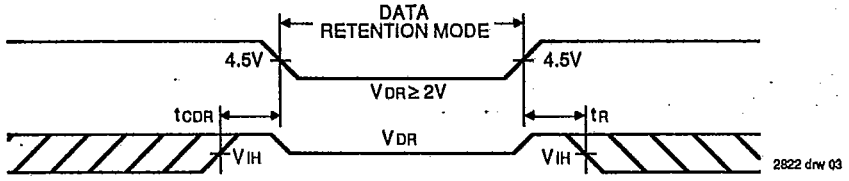
(TA = -55°C to +125°C)

Symbol	Parameter	Test Condition	Min.	Max. Vcc @ 2.0V	Unit
VDR	Vcc for Data Retention	—	2.0	—	V
ICCDR	Data Retention Current	$\overline{CS}$ ≥ Vcc - 0.2V	—	2(4)	mA
tCDR(3)	Chip Deselect to Data Retention Time	VIN ≤ Vcc - 0.2V or	0	—	ns
tR(3)	Operation Recovery Time	VIN ≥ 0.2V	tRC(2)	—	ns

NOTES:
1. Vcc = 2V, TA = +25°C.
2. tRC = Read Cycle Time.
3. This parameter is guaranteed by design, but not tested.
4. For 60ns-120ns versions, ICCDR=800µA.
5. L version only.

2822 tbl 09

DATA RETENTION WAVEFORM



2822 drw 03

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2822 tbl 07

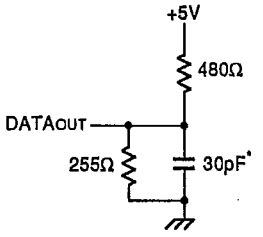


Figure 1. Output Load

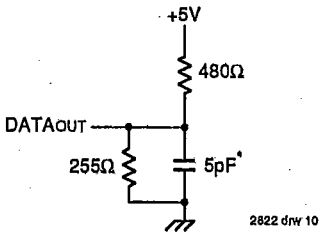


Figure 2. Output Load
(for t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, t_{OW} and t_{CLZ})

* Including scope and jig

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	7M4048SxxCB, 7M4048LxxCB										Unit
		-17[3]		-20[3]		-25		-30		-35		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
t_{RC}	Read Cycle Time	17	—	20	—	25	—	30	—	35	—	ns
t_{AA}	Address Access Time	—	17	—	20	—	25	—	30	—	35	ns
t_{ACS}	Chip Select Access Time	—	17	—	20	—	25	—	30	—	35	ns
t_{OE}	Output Enable to Output Valid	—	8	—	10	—	12	—	15	—	15	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	7	—	8	—	12	—	12	—	15	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	0	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	12	—	13	—	14	—	16	—	20	ns
t_{OH}	Output Hold from Address Change	1	—	3	—	3	—	3	—	3	—	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	17	—	20	—	25	—	30	—	35	ns
Write Cycle												
t_{WC}	Write Cycle Time	17	—	20	—	25	—	30	—	35	—	ns
t_{WP}	Write Pulse Width	14	—	15	—	17	—	20	—	25	—	ns
t_{AS}[2]	Address Set-up Time	3	—	3	—	3	—	0	—	0	—	ns
t_{AW}	Address Valid to End of Write	17[4]	—	18	—	20	—	25	—	30	—	ns
t_{CW}	Chip Select to End of Write	17	—	18	—	20	—	25	—	30	—	ns
t_{DW}	Data to Write Time Overlap	10	—	12	—	15	—	17	—	20	—	ns
t_{DH}[2]	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WR}[2]	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	10	—	13	—	15	—	15	—	15	ns
t_{OW}[1]	Output Active from End of Write	2	—	2	—	2	—	5	—	5	—	ns

2822 tbl 08

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. t_{AS}=0ns for $\overline{CS}$ controlled write cycles. t_{DH}, t_{WR}= 3ns for $\overline{WE}$ controlled write cycles.
3. Preliminary specifications only.
4. t_{AW}=14ns for $\overline{CS}$ controlled write cycles.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	7M4048SxxCB, 7M4048LxxCB										Unit
		-45		-55		-60[3]		-65[3]		-70		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
t_{RC}	Read Cycle Time	45	—	55	—	65	—	65	—	70	—	ns
t_{AA}	Address Access Time	—	45	—	55	—	60	—	65	—	70	ns
t_{ACS}	Chip Select Access Time	—	45	—	55	—	60	—	65	—	70	ns
t_{OE}	Output Enable to Output Valid	—	25	—	30	—	30	—	35	—	45	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	20	—	20	—	25	—	25	—	30	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	5	—	5	—	3	—	5	—	0	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	20	—	20	—	25	—	25	—	40	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	10	—	10	—	—	10	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	45	—	55	—	65	—	65	—	70	ns
Write Cycle												
t_{WC}	Write Cycle Time	45	—	55	—	65	—	65	—	70	—	ns
t_{WP}	Write Pulse Width	35	—	45	—	50	—	55	—	55	—	ns
t_{AS}	Address Set-up Time	5	—	5	—	0	—	0	—	0	—	ns
t_{AW}	Address Valid to End of Write	40	—	50	—	60	—	65	—	65	—	ns
t_{CW}	Chip Select to End of Write	40	—	50	—	60	—	65	—	65	—	ns
t_{DW}	Data to Write Time Overlap	20	—	20	—	30	—	30	—	35	—	ns
t_{DH}	Data Hold Time	0[2]	—	0[2]	—	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0[2]	—	0[2]	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	15	—	20	—	25	—	25	—	30	ns
t_{OW}[1]	Output Active from End of Write	5	—	5	—	0	—	0	—	0	—	ns

2622 tbl 06

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. tAS=0ns for $\overline{CS}$ controlled write cycles. tDH, tWR= 5ns for $\overline{WE}$ controlled write cycles.
3. Preliminary specifications only.

AC ELECTRICAL CHARACTERISTICS

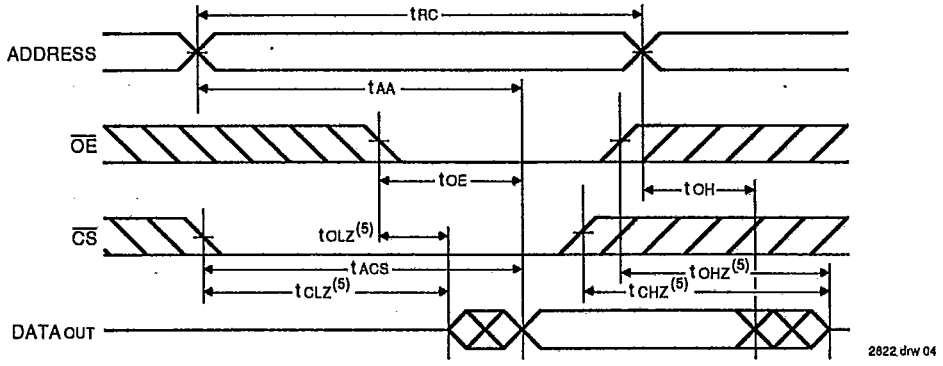
(Vcc = 5V ± 10%, TA = -55°C to +125°C)

Symbol	Parameter	7M4048SxxCB, 7M4048LxxCB						Unit
		-85		-100		-120		
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
tRC	Read Cycle Time	85	—	100	—	120	—	ns
tAA	Address Access Time	—	85	—	100	—	120	ns
tACS	Chip Select Access Time	—	85	—	100	—	120	ns
tOE	Output Enable to Output Valid	—	48	—	50	—	60	ns
tOHZ(1)	Output Disable to Output in High Z	—	33	—	35	—	40	ns
tOLZ(1)	Output Enable to Output in Low Z	0	—	0	—	0	—	ns
tCLZ(1)	Chip Select to Output in Low Z	5	—	5	—	5	—	ns
tCHZ(1)	Chip Deselect to Output in High Z	—	43	—	45	—	50	ns
tOH	Output Hold from Address Change	10	—	10	—	10	—	ns
tPU(1)	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
tPD(1)	Chip Deselect to Power-Down Time	—	85	—	100	—	120	ns
Write Cycle								
tWC	Write Cycle Time	85	—	100	—	120	—	ns
tWP	Write Pulse Width	65	—	75	—	90	—	ns
tAS	Address Set-up Time	2	—	5	—	5	—	ns
tAW	Address Valid to End of Write	82	—	90	—	100	—	ns
tCW	Chip Select to End of Write	80	—	85	—	100	—	ns
tDW	Data to Write Time Overlap	38	—	40	—	45	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tWHZ(1)	Write Enable to Output in High Z	—	33	—	35	—	40	ns
tOW(1)	Output Active from End of Write	0	—	0	—	0	—	ns

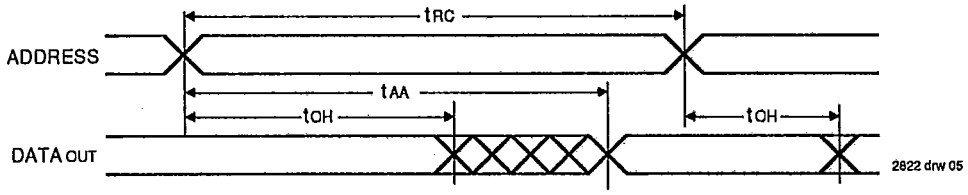
NOTE:
1. This parameter is guaranteed by design, but not tested.

2822 tbl 08

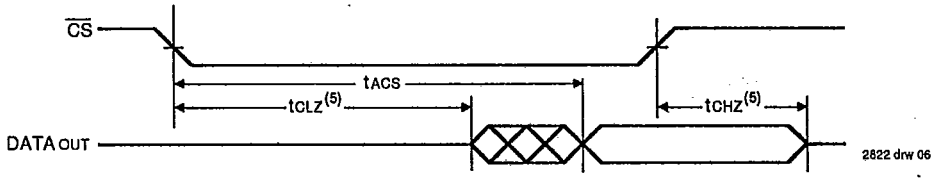
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state. This parameter is guranateed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)

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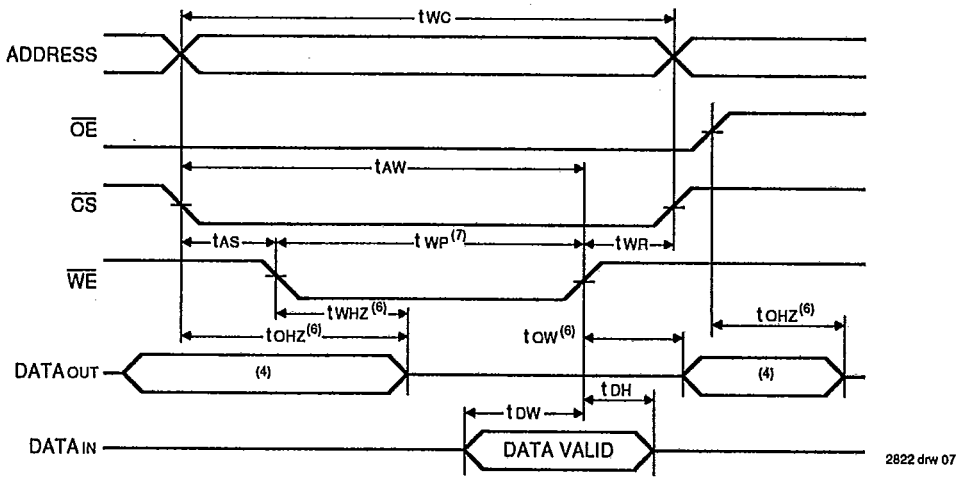
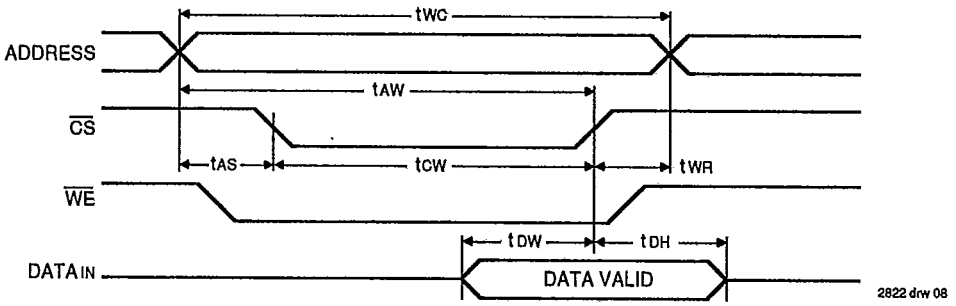
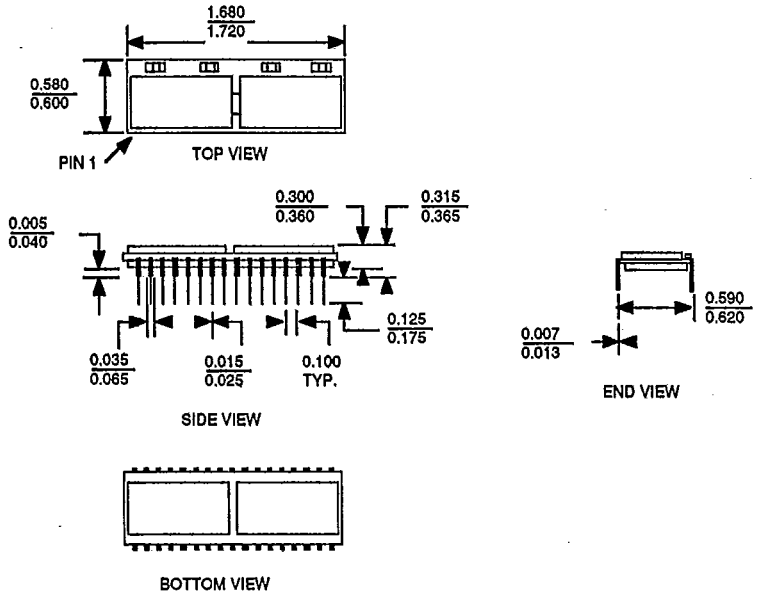


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse ((tWP) > tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

PACKAGE DIMENSIONS



BOTTOM VIEW