FEATURES

- SURFACE MOUNT PACKAGE
- MONOLITHIC MOS TECHNOLOGY
- LOW COST
- HIGH VOLTAGE OPERATION—350V
- LOW QUIESCENT CURRENT—2mA
- NO SECOND BREAKDOWN
- HIGH OUTPUT CURRENT—120 mA PEAK

APPLICATIONS

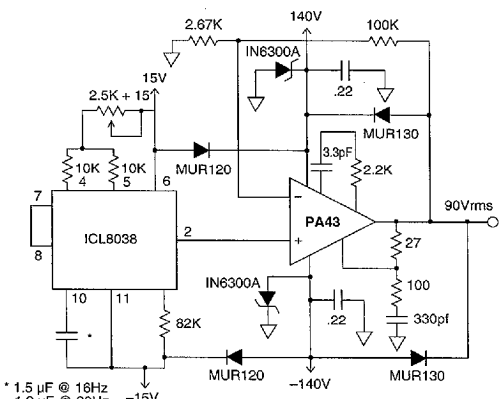
- TELEPHONE RING GENERATOR
- PIEZO ELECTRIC POSITIONING
- ELECTROSTATIC TRANSDUCER & DEFLECTION
- DEFORMABLE MIRROR FOCUSING

DESCRIPTION

The PA43 is a high voltage monolithic MOSFET operational amplifier achieving performance features previously found only in hybrid designs while increasing reliability. Inputs are protected from excessive common mode and differential mode voltages. The safe operating area (SOA) has no second breakdown limitations and can be observed with all type loads by choosing an appropriate current limiting resistor. External compensation provides the user flexibility in choosing optimum gain and bandwidth for the application.

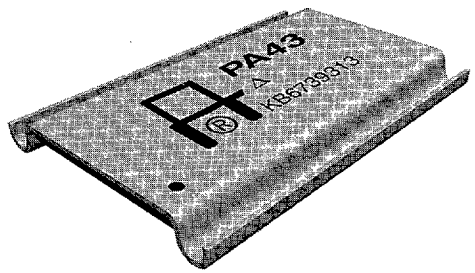
The PA43 is packaged in a non-hermetic surface mountable dual in line package and all circuitry is isolated from the case.

TYPICAL APPLICATION

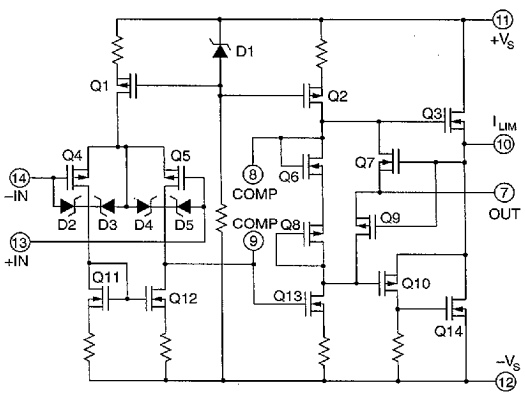


Telephone Ring Generator

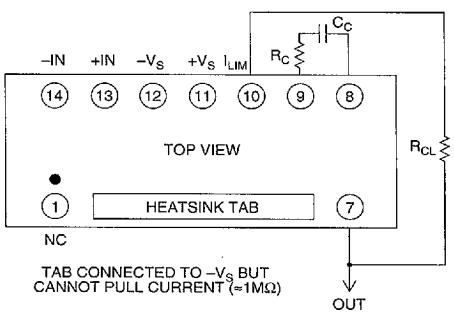
The PA43 is set for a gain of 38.5 boosting the 2.33V signal to 90V. The recommended compensation for gains above 30 is used. If capacitive loading is at least 330pF at all times, the recommended snubber network may be omitted. The 27 ohm resistor sets current limit to a nominal value of 111mA to insure peak currents out of at least 78mA.



EQUIVALENT SCHEMATIC



EXTERNAL CONNECTIONS



PHASE COMPENSATION

Gain	C_c	R_c
1	18pF	2.2KΩ
≥10	10pF	2.2KΩ
≥30	3.3pF	2.2KΩ

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	350V
OUTPUT CURRENT, continuous within SOA	60 mA
OUTPUT CURRENT, peak	120 mA
POWER DISSIPATION, continuous @ T_C = 25°C	9W
INPUT VOLTAGE, differential	±16 V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder – 10 sec	220°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
TEMPERATURE RANGE, powered (case)	–55 to +125°C

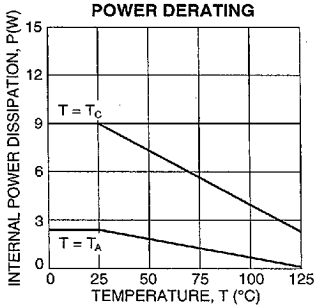
SPECIFICATIONS

PARAMETER	TEST CONDITIONS[1]	PA43 MIN	PA43 TYP	PA43 MAX	UNITS
INPUT					
OFFSET VOLTAGE, initial			15	30	mV
OFFSET VOLTAGE, vs. temperature[4]	Full temperature range		70	130	µV/°C
OFFSET VOLTAGE, vs supply			20	32	µV/V
OFFSET VOLTAGE, vs time			75		µV √kh
BIAS CURRENT, initial			50	200	pA
BIAS CURRENT, vs supply			2	20	pA/V
OFFSET CURRENT, initial			50	200	pA
INPUT IMPEDANCE, DC			10^{11}		Ω
INPUT CAPACITANCE			5		pF
COMMON MODE, voltage range		$\pm V_S$–12			V
COMMON MODE REJECTION, DC	V_{CM} = ±90V DC	84	94		dB
NOISE, broad band	10kHz BW, R_S = 1KΩ		50		µV RMS
NOISE, low frequency	1-10 Hz		110		µV p-p
GAIN					
OPEN LOOP at 15Hz	R_L = 5KΩ	94	106		dB
BANDWIDTH, open loop			1.6		MHz
POWER BANDWIDTH	C_C = 10pf, 280V p-p		26		kHz
PHASE MARGIN	Full temperature range		60		°
OUTPUT					
VOLTAGE SWING	I_O = 40mA	$\pm V_S$–12	$\pm V_S$–10		V
CURRENT, peak[5]		120			mA
CURRENT, continuous		60			mA
SETTLING TIME to .1%	C_C = 10pF, 10V step, A_V = –10		12		µs
SLEW RATE	C_C = OPEN		40		V/µs
CAPACITIVE LOAD	A_V = +1	10			nF
RESISTANCE[6], no load	R_{CL} = 0		150		Ω
RESISTANCE[6], 20mA load	R_{CL} = 0		25		Ω
POWER SUPPLY					
VOLTAGE[3]	See Note 3	±50	±150	±175	V
CURRENT, quiescent			1.6	2.0	mA
THERMAL					
RESISTANCE, AC junction to case	F > 60Hz		7	10	°C/W
RESISTANCE, DC junction to case	F < 60Hz		12	14	°C/W
RESISTANCE, junction to air	Full temperature range		55		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	°C

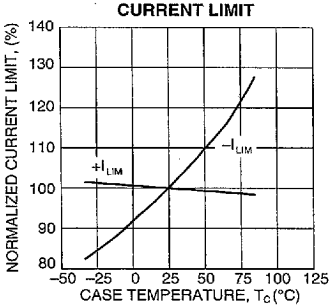
NOTES:
1. Unless otherwise noted T_C = 25°C, C_C = 18pF, R_G = 2.2KΩ. DC input specifications are ± value given. Power supply voltage is typical rating.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
3. Derate maximum supply voltage .5 V/°C below case temperature of 25°C. No derating is needed above T_C = 25°C.
4. Sample tested by wafer to 95%.
5. Guaranteed but not tested.
6. The selected value of R_{CL} must be added to the values given for total output resistance.

CAUTION The PA43 is constructed from MOSFET transistors. ESD handling procedures must be observed.

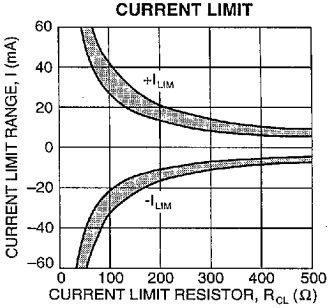
POWER DERATING



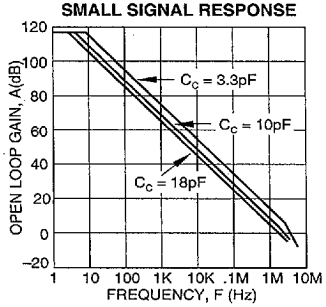
CURRENT LIMIT



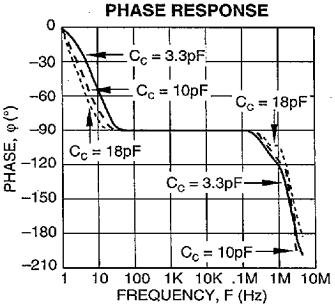
CURRENT LIMIT



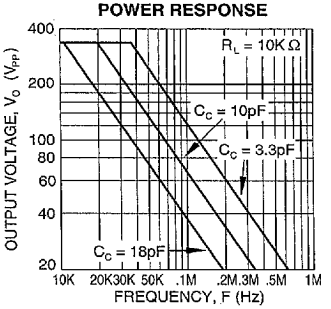
SMALL SIGNAL RESPONSE



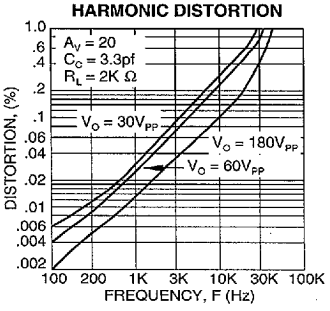
PHASE RESPONSE



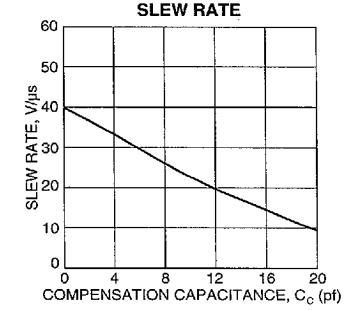
POWER RESPONSE



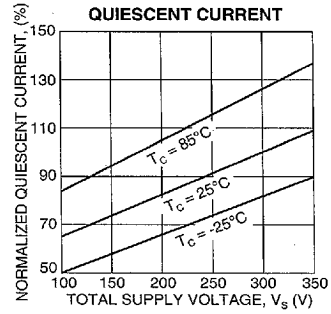
HARMONIC DISTORTION



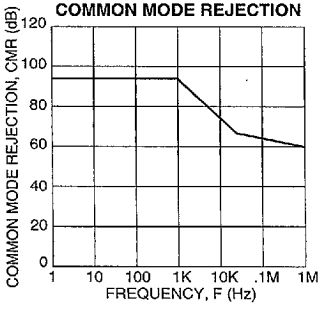
SLEW RATE



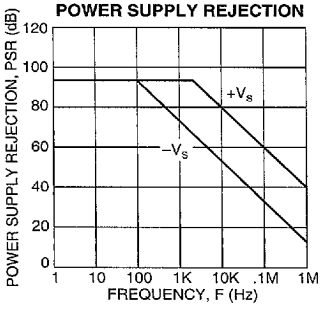
QUIESCENT CURRENT



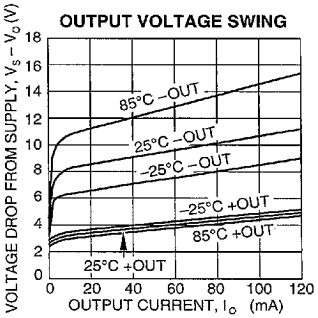
COMMON MODE REJECTION



POWER SUPPLY REJECTION



OUTPUT VOLTAGE SWING



GENERAL

Please read the "General Operating Considerations" section of the data book, which covers stability, supplies, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the applications notes.

CURRENT LIMIT

For proper operation the current limit resistor, R_{CL}, must be connected as shown in the external connection diagram. The minimum value is 33 ohms, however for optimum reliability the resistor value should be set as high as possible. The value can be estimated as follows with the maximum practical value of 500 ohms.

$$R_{CL} = \frac{3}{I_{LIM}}$$

Use the typical performance graphs as a guide for expected variations in current limit value with a given R_{CL} and variations over temperature. The selected value of R_{CL} must be added to the specified typical value of output resistance to calculate the total output resistance. Since the load current passes through R_{CL} the value selected also affects the output voltage swing according to:

$$V_R = I_O * R_{CL}$$

where V_R is the voltage swing reduction.

When the amplifier is current limiting, there may be small signal spurious oscillation present during the current limited portion of the negative half cycle. The frequency of the oscillation is not predictable and depends on the compensation, gain of the amplifier, and load. The oscillation will cease as the amplifier comes out of current limit.

INPUT PROTECTION

The PA43 inputs are protected against common mode voltages up the supply rails and differential voltages up to ±16 volts as well as static discharge. Differential voltages exceeding 16 volts will be clipped by the protection circuitry. However, if more than a few milliamps of current is available from the overload source, the protection circuitry could be destroyed. The protection circuitry includes 300 ohm current limiting resistors at each input, but this may be insufficient for severe overloads. It may be necessary to add external resistors to the application circuit where severe overload conditions are expected. Limiting input current to 1mA will prevent damage.

STABILITY

The PA43 has sufficient phase margin when compensated for unity gain to be stable with capacitive loads of at least 10 nF. However, the low pass circuit created by the sumpoint (–in) capacitance and the feedback network may add phase shift and cause instabilities. As a general rule, the sumpoint load resistance (input and feedback resistors in parallel) should be 1K ohm or less at low gain settings (up to 10). Alternatively, use a bypass capacitor across the feedback resistor. The time constant of the feedback resistor and bypass capacitor combination should match the time constant of the sumpoint resistance and sumpoint capacitance.

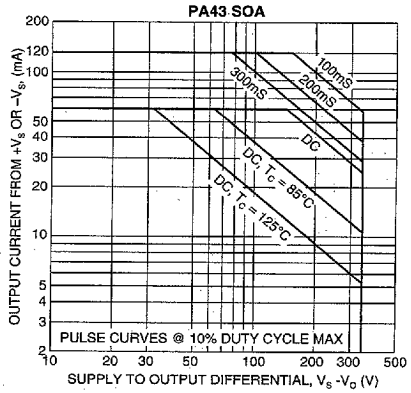
The PA43 is externally compensated and performance can be tailored to the application. Use the graphs of small signal gain and phase response as well as the graphs for slew rate and power response as a guide. The compensation capacitor C_C must be rated at 350V working voltage. The compensation capacitor and associated resistor R_C must be mounted closely to the amplifier pins to avoid spurious oscillation. An NPO capacitor is recommended for compensation.

SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the die metallization.
2. The temperature of the output MOSFETs.

NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.



HEATSINKING

The solder connection of the heat tab to a large foil area of the printed circuit board will result in thermal performance better than the 55°C/W junction to air rating of the PA43. This may be adequate heatsinking but the large number of variables involved suggest temperature measurements be made on the top of the package. Do not allow this temperature exceed 85°C. When additional heatsinking is required there are several sources for glue-on heat sinks which will fit on top of the PA43. They are available with fins running the length of the package or across it. Several sources for these heatsinks are listed below along with part numbers.

	AAVID	EIRC	THERMALLOY
Lengthwise fins	50110	145	6011
Crosswise fins	501200	144	6012

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