International
IOR Rectifier

Data Sheet No. PD 10034-E

Series PVN012

Microelectronic Power IC

HEXFET® Power MOSFET Photovoltaic Relay

Single Pole, Normally Open, 0-20V, 2.5A AC/ 4.5A DC

General Description

The PVN012 Series Photovoltaic Relay at 100 milliohms features the lowest possible on-state resistance in a miniature package — lower than a comparable reed relay.

The PVN012 is a single-pole, normally open solid-state relay. It utilizes a GenerationV HEXFET output switch, driven by an integrated circuit photovoltaic generator of novel construction. The output switch is controlled by radiation from a GaAlAs light emitting diode (LED) which is optically isolated from the photovoltaic generator.

These units exceed the performance capabilities of electromechanical relays in life, sensitivity, stable on-resistance, miniaturization, magnetic insensitivity and ruggedness. They are ideally suited for switching high currents or low level signals without distortion or injection of electrical noise.

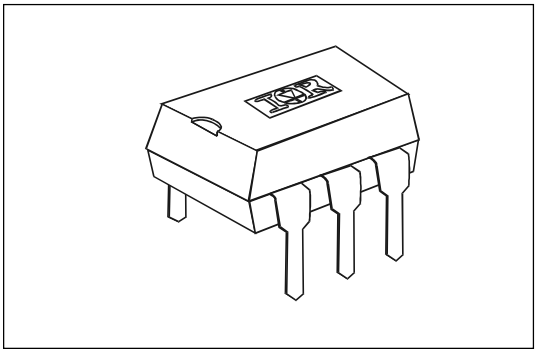
Series PVN012 Relays are packaged in a 6-lead molded DIP package with either through-hole or surface mount (gull-wing) terminals. They are available in standard plastic shipping tubes or on tape-and-reel. Please refer to part identification information opposite.

Applications

- Portable Electronics
- Programmable Logic Controllers
- Computers and Peripheral Devices
- Audio Equipment
- Power Supplies and Power Distribution
- Instrumentation

Features

- 100mΩ On-Resistance
- GenV HEXFET output
- Bounce-free operation
- 2.5 - 4.5 Amp capacity
- Linear AC/DC operation
- 4,000 V_{RMS} I/O isolation
- Solid-State reliability
- UL recognized
- ESD Tolerance:
  - 4000V Human Body Model
  - 500V Machine Model



Part Identification

PVN012	through-hole
PVN012S	surface-mount
PVN012S-T	surface-mount, tape and reel

(HEXFET is the registered trademark for International Rectifier Power MOSFETs)

Electrical Specifications (-40°C ≤ T_A ≤ +85°C unless otherwise specified)

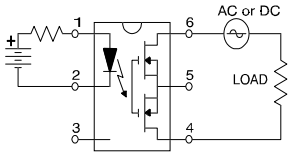
INPUT CHARACTERISTICS	Limits	Units
Minimum Control Current (see figure 1)	3.0	mA
Maximum Control Current for Off-State Resistance @ T_A = +25°C	0.4	mA
Control Current Range (Caution: current limit input LED, see figure 6)	3.0 to 25	mA
Maximum Reverse Voltage	7.0	V

OUTPUT CHARACTERISTICS		Limits	Units
Operating Voltage Range		0 to ±20	V(DC or AC peak)
Maximum Continuous Load Current @ T_A=+40°C, 5mA Control (see figure 1)			
	A Connection	2.5	A (DC or AC)
	B Connection	3.0	A (DC)
	C Connection	4.5	A (DC)
Maximum Pulsed Load Current @T_A=+25°C, (100 ms @ 10% duty cycle)			
	A Connection	6.0	A (DC or AC)
Maximum On-State Resistance @T_A=+25°C, for 1A pulsed load, 5mA Control (see figure 4)			
	A Connection	100	mΩ
	B Connection	65	
	C Connection	40	
Minimum Off-State Resistance @ T_A=+25°C, ±16V_{DC}		0.16 x 10^8	Ω
Maximum Turn-On Time @T_A=+25°C (see figure 7), for 1A, 20 V_{DC} load, 5mA Control		5.0	ms
Maximum Turn-Off Time @T_A=+25°C (see figure 7), for 1A, 20 V_{DC} load, 5mA Control		0.5	ms
Maximum Output Capacitance @ 20V_{DC} (see figure 2)		300	pF

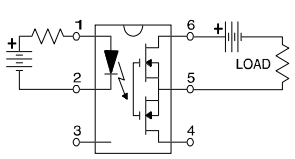
GENERAL CHARACTERISTICS		Limits	Units
Minimum Dielectric Strength, Input-Output		4000	V_{RMS}
Minimum Insulation Resistance, Input-Output, @T_A=+25°C, 50%RH, 100V_{DC}		10^{12}	Ω
Maximum Capacitance, Input-Output		1.0	pF
Maximum Pin Soldering Temperature (10 seconds maximum)		+260	°C
Ambient Temperature Range:	Operating	-40 to +85	
	Storage	-40 to +100	

Connection Diagrams

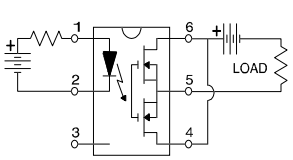
"A" Connection



"B" Connection



"C" Connection



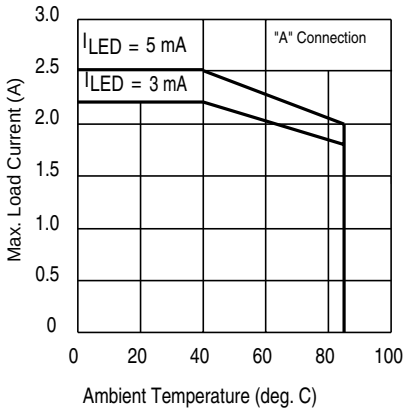


Figure 1. Current Derating Curves*

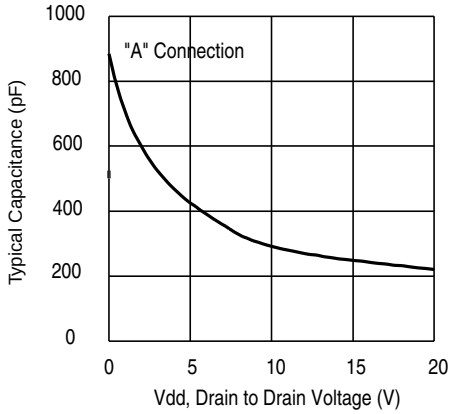


Figure 2. Typical Output Capacitance

* Derating of 'B' and 'C' connection at +85°C will be 70% of that specified at +40°C and is linear from +40°C to +85°C.

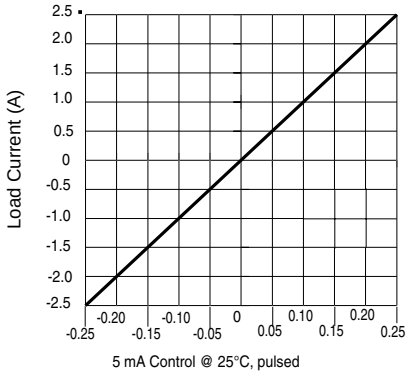


Figure 3. Linearity Characteristics

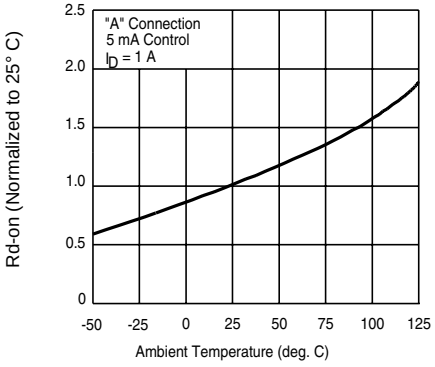


Figure 4. Typical Normalized On-Resistance

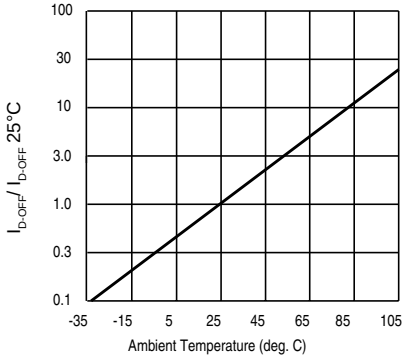


Figure 5. Typical Normalized Off-State Leakage

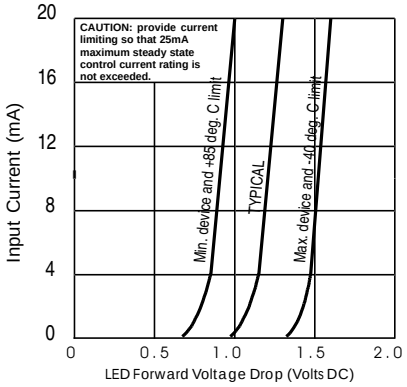


Figure 6. Input Characteristics (Current Controlled)

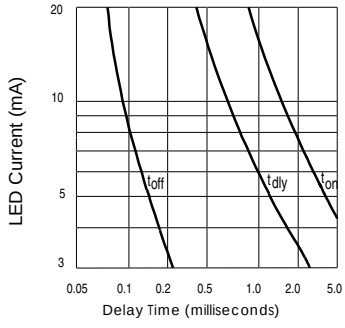


Figure 7. Typical Delay Times

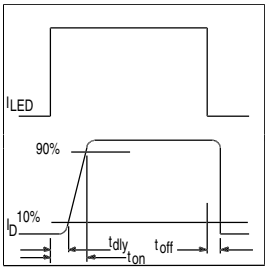


Figure 8. Delay Time Definitions

Case Outlines