- **'ACT2150A is Recommended for New Designs**

- **Fast Address to Match Valid Delay – Two Speed Ranges: 35 ns and 45 ns**

- **512 × 9 Internal RAM**

- **300-Mil 24-Pin Ceramic Side-Brazed or Plastic Dual-In-Line or Small Outline Packages**

- **Max Power Dissipation: 660 mW**

- **On-Chip Parity Generation and Checking**

- **Parity Error Output/Force Parity Error Input**

- **On-Chip Address/Data Comparator**

- **Asynchronous, Single-Cycle Reset**

- **Easily Expandable**

- **Fully Static**

- **Reliable SMOS (Scaled NMOS) Technology**

- **TTL- and CMOS Compatible Inputs and Outputs**

DW, JD, OR NT PACKAGE
(TOP VIEW)

$\overline{\text{RESET}}$	1	24	V_{CC}
A5	2	23	A1
A4	3	22	A0
A3	4	21	A8
A2	5	20	A7
D3	6	19	A6
D0	7	18	D5
D1	8	17	D4
D2	9	16	D7
$\overline{\text{W}}$	10	15	D6
$\overline{\text{PE}}$	11	14	MATCH
GND	12	13	$\overline{\text{S}}$
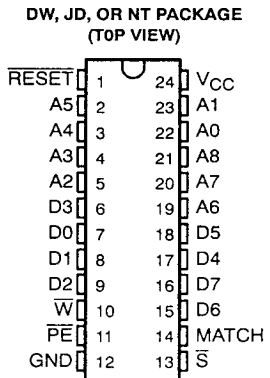
description

This 8-bit-slice cache address comparator consists of a high-speed 512 × 9 static RAM array, parity generator, parity checker, and 9-bit high-speed comparator. It is fabricated using N-channel silicon gate technology for high speed and simple interface with MOS and bipolar TTL circuits. The cache address comparator is easily cascadable for wider tag addresses or deeper tag memories. Significant reductions in cache memory component count, board area, and power dissipation can be achieved with this device.

When $\overline{\text{S}}$ is low and $\overline{\text{W}}$ is high, the cache address comparator compares the contents of the memory location addressed by A0-A8 with the data on D0-D7 plus generated parity. An equality is indicated by the high level on the MATCH output. A low-level output from $\overline{\text{PE}}$ signifies a parity error in the internal RAM data. $\overline{\text{PE}}$ is an N-channel open-drain output for easy OR-tying. During a write cycle ($\overline{\text{S}}$ and $\overline{\text{W}}$ low), data on D0-D7 plus generated even parity are written in the 9-bit memory location addressed by A0-A8. Also during write, a parity error may be forced by holding $\overline{\text{PE}}$ low.

A $\overline{\text{RESET}}$ input is provided for initialization. When $\overline{\text{RESET}}$ goes low, all 512 × 9 RAM locations are cleared and the MATCH output is forced high.

The cache address comparator operates from a single 5-V supply and is offered in a 24-pin 300-mil ceramic side-brazed or plastic dual-in-line packages and plastic "Small Outline" packages. The device is fully TTL compatible and is characterized for operation from 0°C to 70°C.

for complete data sheet

The complete version of this data sheet and application information can be obtained by calling the DVP Applications Group at 214-997-5762.

TEXAS INSTRUMENTS

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TMS2150A
512 × 8 CACHE ADDRESS COMPARATOR

MATCH OUTPUT DESCRIPTION

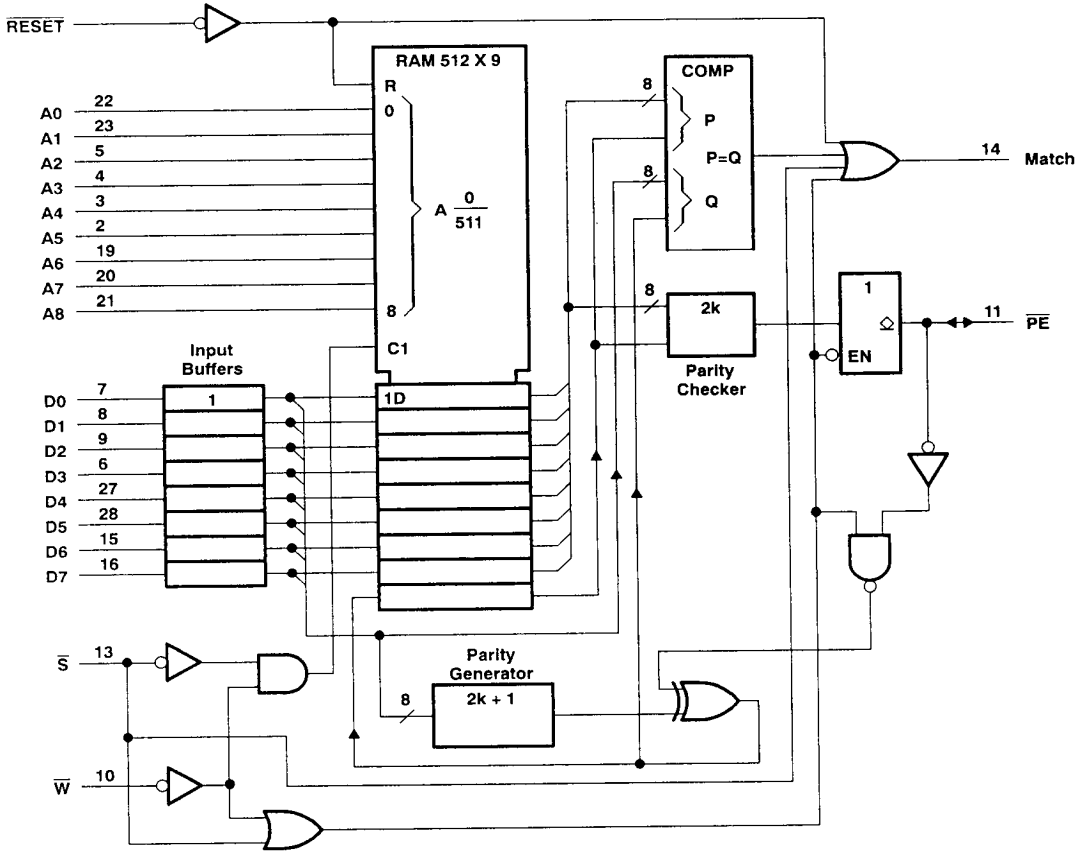MATCH = V_{OH} if: $[A0-A8] = D0-D7$ + parity,
  or: $\overline{RESET} = V_{IL}$.
  or: $\overline{S} = V_{IH}$,
  or: $\overline{W} = V_{IL}$

MATCH = V_{OL} if: $[A0-A8] \neq D0-D7$ + parity,
  with $\overline{RESET} = V_{IH}$,
  $\overline{S} = V_{IL}$, and $\overline{W} = V_{IH}$

FUNCTION TABLE

OUTPUTS		FUNCTION DESCRIPTION
MATCH	$\overline{PE}$	
L	L	Parity Error
L	H	Not Equal
H	L	Undefined Error
H	H	Equal

logic diagram (positive logic)

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