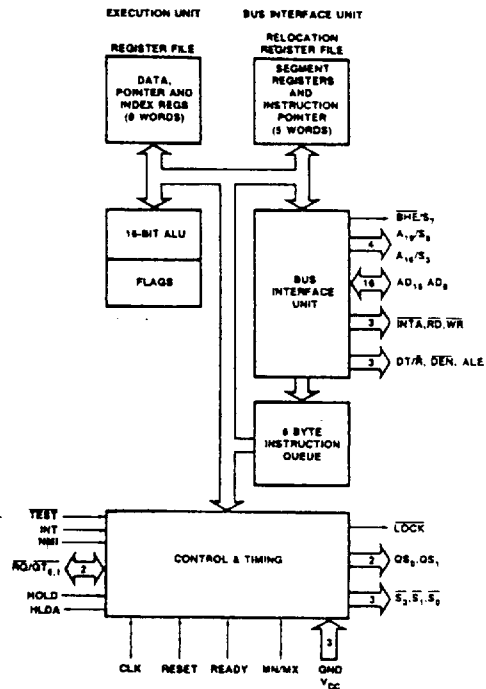


Radiation Hardened 80C86RP

High Speed CMOS
16-Bit Microprocessor

*For Space
Applications*

SEI's 80C86RP (RP for RAD-PAK®) high speed CMOS microcircuit features a minimum 100 kilorad (Si) total dose tolerance. Using SEI's radiation hardened RAD-PAK® packaging technology, the 80C86RP is fully equivalent to the commercial Intel's M80C86 16-bit CMOS microprocessor. The 80C86RP is of static design. Internal registers, counters and latches are static and require no refresh as with dynamic circuit design. This eliminates the minimum operating frequency restriction placed on other microprocessors. The 80C86RP can be single stepped using only the CPU clock. This state can be maintained for as long as is necessary. This operation allows simple interface circuitry to provide critical information for bringing up the system. The 80C86RP is partitioned logically into two processing units. The first is the Bus Interface Unit (BIU) and the second is the Execution Unit (EU). These units can interact directly but for the most part performs separate asynchronous operational processors. The bus interface unit provides the functions related to instruction fetching and queueing, operand fetch and store, and address relocation. The overlap of instruction pre-fetching provided by this unit serves to increase processor performance through improved bus bandwidth utilization. Up to 6 bytes of instruction stream can be queued while waiting for decoding and execution.

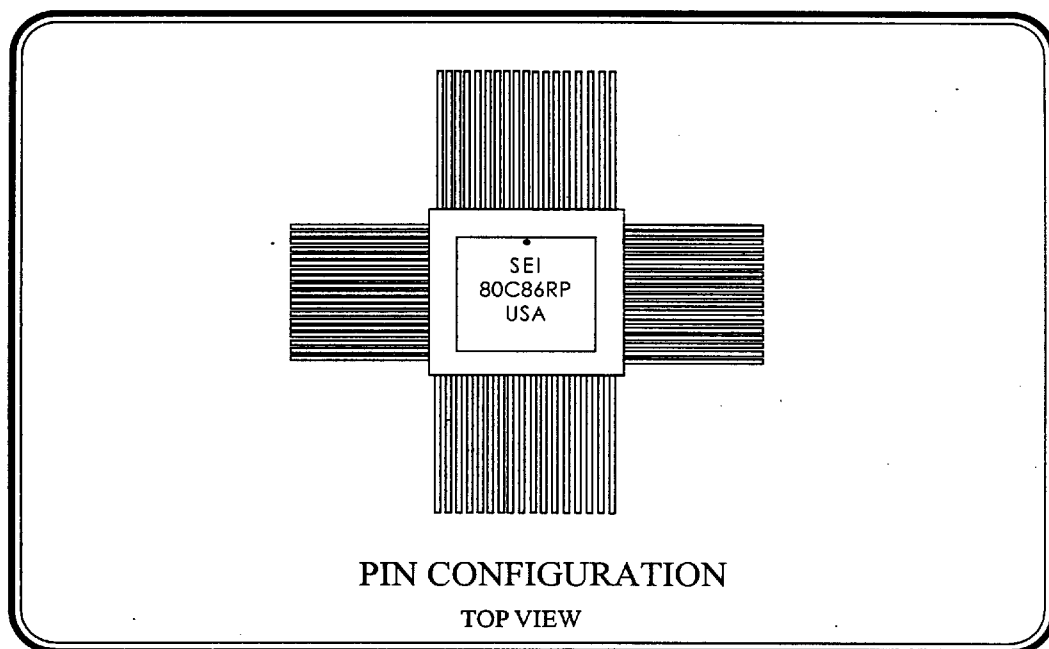


**SPACE
ELECTRONICS
INCORPORATED**

Tel.: (619)452-4167 FAX: (619)452-5499
INTERNET: 102005.1635@COMPUSERVE.COM

Radiation Hardened 80C86RP

High Speed CMOS
16-Bit Microprocessor



Features

- 16-bit CMOS Microprocessor
- Pin Compatible with Intel M80C86
- RAD-PAK® Radiation Hardened Against Natural Space Radiation
- Total Dose Hardness >100 krad (Si)
- Package:
 - 44 Pin RAD-PAK® quad flat pack (650 mils x 650 mils)
 - Weight: 12 grams
- Frequency Range:
 - D.C. to 5 MHz
- 24 Operand Addressing Modes
- High Performance CHMOS Technology
 - Single 5 Volt Power Supply
 - Low Power Supply Current:
 - Standby: 500 uA typical,
 - Operation: 10 mA/MHz typical
- 8 and 16-Bit Signed and Unsigned Arithmetic
 - Binary or Decimal
 - Multiply and Divide
- Bus-Hold Circuitry Eliminates Pull-Up Resistors
- Screening per TM 5004
- QCI per TM5005

Specifications and design are subject to change without notice.



March 1995

For Further Information Contact:

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4031 Sorrento Valley Blvd., San Diego, CA 92121
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80C86RP ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Positive Supply Voltage	V_{CC}	-0.5	7.0	V
DC Voltage to Outputs, (During High-Z State)		-0.5	7.0	V
Output Current into Outputs, (Low)			20	mA
DC Input Voltage	V_{IN}	-0.5	7.0	V
Power Dissipation	P_D		1000	mW
Storage Temperature Range	T_s	-65	+150	°C
Operating Temperature Range	T_A	-55	+125	°C

80C86RP OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Positive Supply Voltage	V_{DD}	4.75	5.25	V
High Level Input Voltage	V_{IH}	2.2		V
Low Level Input Voltage	V_{IL}		0.8	V
Case Operating Temperature Range	T_C	-55	+125	°C

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80C86RP DC CHARACTERISTICS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Low Voltage	V_{IL}		+0.8	V
Input High Voltage, (All inputs except clock and MN/MX\)	V_{IH}	2.2		V
Clock and MN/MX\ Input High Voltage	V_{CH}	$V_{CC}-0.8$		V
Output Low Voltage, $I_{OL}=2.5mA$	V_{OL}		0.4	V
Output High Voltage $I_{OH}=-2.5mA$ $I_{OH}=-100\mu A$	V_{OH}	3.0 $V_{CC}-0.4$		V
Power Supply Current $V_{IL}=GND, V_{IH}=V_{CC}$	I_{CC}		10	mA/MHz
Standby Supply Current $V_{IN}=V_{CC}$ or GND Outputs Unloaded CLK=GND or V_{CC}	I_{CCS}		500	μA
Input Leakage Current: $0V \leq V_{IN} \leq V_{CC}$	I_{LI}		± 1.0	μA
Input Leakage Current : (Bus Hold Low)	I_{BHL}	40	400	μA
Input Leakage Current : (Bus Hold High)	I_{BHH}	-40	-400	μA
Output Leakage Current: $V_{OUT}=GND$ or V_{CC}	I_{LO}		± 10	μA
Capacitance of Input Buffer, (All inputs except AD_0 - AD_{15} , RQVGT\)	C_{IN}		10	pF
Capacitance of I/O Buffer (AD_0 - AD_{15} , RQVGT\)	C_{IO}		20	pF
Output Capacitance	C_{OUT}		15	pF



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80C86RP TIMING REQUIREMENTS (MIN MODE)

PARAMETER	SYMBOL	MIN	MAX	UNITS
CLK Cycle Period ³	TCLCL	125		ns
CLK Low Time ³	TCLCH	68		ns
CLK High Time ³	TCHCL	44		ns
CLK Rise Time From 1.0V to 3.5V ¹	TCH1CH2		10	ns
CLK Fall Time From 3.5V to 1.0V ¹	TCL2CL1		10	ns
Data in Setup Time ³	TDVCL	20		ns
Data in Hold Time ³	TCLDX	10		ns
RDY Setup Time ³	TR1VCL	35		ns
RDY Hold Time ³	TCLR1X	0		ns
READY Setup Time ³	TRYHCH	68		ns
READY Hold Time ³	TCHRYX	20		ns
READY Inactive to CLK ³	TRYLCL	-8		ns
HOLD Setup Time ³	THVCH	20		ns
INTR, NMI, TEST\ Setup Time ³	TINVCH	15		ns
Input Rise Time (Except CLK) From 0.8V to 2.0V ¹	TILIH		15	ns
Input Fall Time (Except CLK) From 2.0V to 0.8V ¹	TIHIL		15	ns



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80C86RP TIMING RESPONSES (MIN MODE)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Address Valid Delay ^{4,5}	TCLAV	0	60	ns
Address Hold Time ¹	TCLAX	10		ns
Address Float Delay ²	TCLAZ	TCLAX	50	ns
ALE Width ¹	TLHLL	TCLCH-10		ns
ALE Active Delay ⁵	TCLLH		50	ns
ALE Inactive Delay ⁵	TCHLL		55	ns
Address Hold Time to ALE Inactive ¹	TLLAX	TCHCL-10		ns
Data Valid Delay ^{2,4}	TCLDV	0	60	ns
Data Hold Time ¹	TCLDX-2	10		ns
Data Hold Time After WR ¹	TWHDX	TCLCH-30		ns
Control Active Delay 1 ^{4,5}	TCVCTV	0	70	ns
Control Active Delay 2 ¹	TCHCTV	10	60	ns
Control Inactive Delay ^{4,5}	TCVCTX	0	70	ns
Address Float to READ Active ¹	TAZRL	0		ns
RD\ Active Delay ^{4,5}	TCLRL	0	100	ns
RD\ Inactive Delay ^{4,5}	TCLRH	0	80	ns
RD\ Inactive to Next Address Active ¹	TRHAV	TCLCL-40		ns
HLDA Valid Delay ¹	TCLHAV	10	100	ns
RD\ Width ¹	TRLRH	2TCLCL-50		ns
WR\ Width ¹	TWLWH	2TCLCL-40		ns
Address Valid to ALE Low ¹	TAVAL	TCLCH-40		ns
Output Rise Time From 0.8V to 2.0V ¹	TOLOH		15	ns
Output Fall Time From 2.0V to 0.8V ¹	TOHOL		15	ns



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80C86RP TIMING REQUIREMENTS (MAX MODE)

PARAMETER	SYMBOL	MIN	MAX	UNITS
CLK Cycle Period ³	TCLCL	125		ns
CLK Low Time ³	TCLCH	68		ns
CLK High Time ³	TCHCL	44		ns
CLK Rise Time From 1.0V to 3.5V ¹	TCH1CH2		10	ns
CLK Fall Time From 3.5V to 1.0V ¹	TCL2CL1		10	ns
Data in Setup Time ⁵	TDVCL	20		ns
Data in Hold Time ⁵	TCLDX	10		ns
RDY Setup Time ³	TRIVCL	35		ns
RDY Hold Time ³	TCLR1X	0		ns
READY Setup Time ⁵	TRYHCH	88		ns
READY Hold Time ³	TCHRYX	20		ns
READY Inactive to CLK ⁵	TRYLCL	-8		ns
Setup Time for Recognition (INTR, NMI, TEST) ⁵	TINVCH	15		ns
RQVGT\ Setup Time ³	TGVCH	15		ns
RQ\ Hold Time ³	TCHGX	30		ns
Input Rise Time (Except CLK) From 0.8V to 2.0V ¹	TILIH		15	ns
Input Fall Time (Except CLK) From 2.0V to 0.8V ¹	TIHIL		15	ns



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80C86RP TIMING RESPONSES (MAX MODE)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Command Active Delay ¹	TCLML	5	35	ns
Command Inactive Delay ¹	TCLMH	5	35	ns
READY Active to Status Passive ¹	TRYHSH		65	ns
Status Active Delay ^{2,4,5}	TCHSV	0	60	ns
Status Inactive Delay ^{4,5}	TCLSH	0	70	ns
Address Valid Delay ^{4,5}	TCLAV	0	60	ns
Address Hold Time ¹	TCLAX	10		ns
Address Float Delay ¹	TCLAZ	TCLAX	50	ns
Status Valid to ALE High ¹	TSVLH		20	ns
Status Valid to MCE High ¹	TSVMCH		30	ns
CLK Low to ALE Valid ¹	TCLLH		20	ns
CLK Low to MCE High ¹	TCLMCH		25	ns
ALE Inactive Delay ¹	TCHLL	4	18	ns
Data Valid Delay ^{4,5}	TCLDV	0	60	ns
Data Hold Time ⁵	TCHDX	10		ns
Control Active Delay ¹	TCVNV	5	45	ns
Control Inactive Delay ¹	TCVNX	10	45	ns
Address Float to Read Active ¹	TAZRL	0		ns
RD Active Delay ^{4,5}	TCLRL	0	100	ns
RD Inactive Delay ^{4,5}	TCLRH	0	80	ns
RD Inactive to Next Address Active ¹	TRHAV	TCLCL-40		ns
Direction Control Active Delay ¹	TCHDTL		50	ns
Direction Control Inactive Delay ¹	TCHDTH		30	ns
GT Active Delay ¹	TCLGL	0	50	ns
GT Inactive Delay ¹	TCLGH	0	50	ns
RD Width ¹	TRLRH	2TCLCL-50		ns
Output Rise Time From 0.8V to 2.0V ¹	TOLOH		15	ns
Output Fall Time From 2.0V to 0.8V ¹	TOHOL		15	ns



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Notes:

1. Guaranteed by design only.
2. Tested in Max. Mode only.
3. Tested by application of signal.
4. Minimum specification limit set to Zero(0) to record actual response.
5. Measured and recorded.

80C86RP Package Ordering Guide

Package Style	Case Outline	1/	Description
Q	Q-44		44 Pin Flat Package

Note:

1/ For outline information, see Appendix A (Package Information - Outline Dimension)



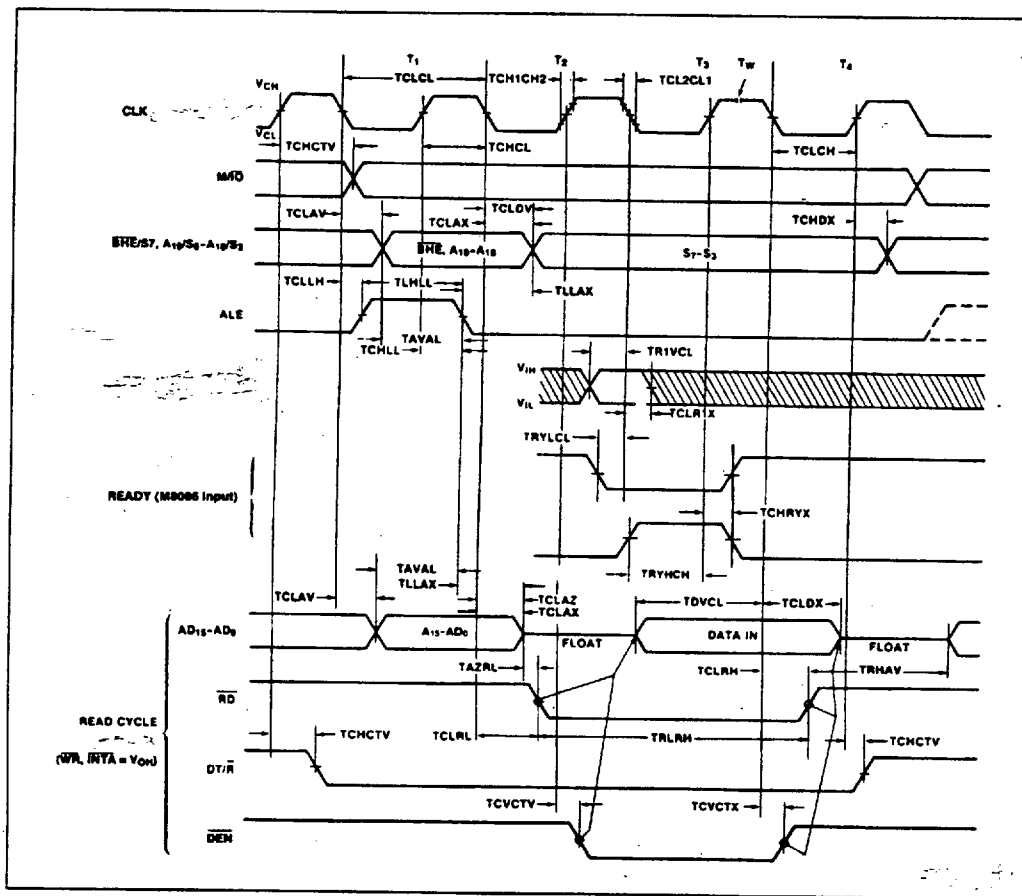
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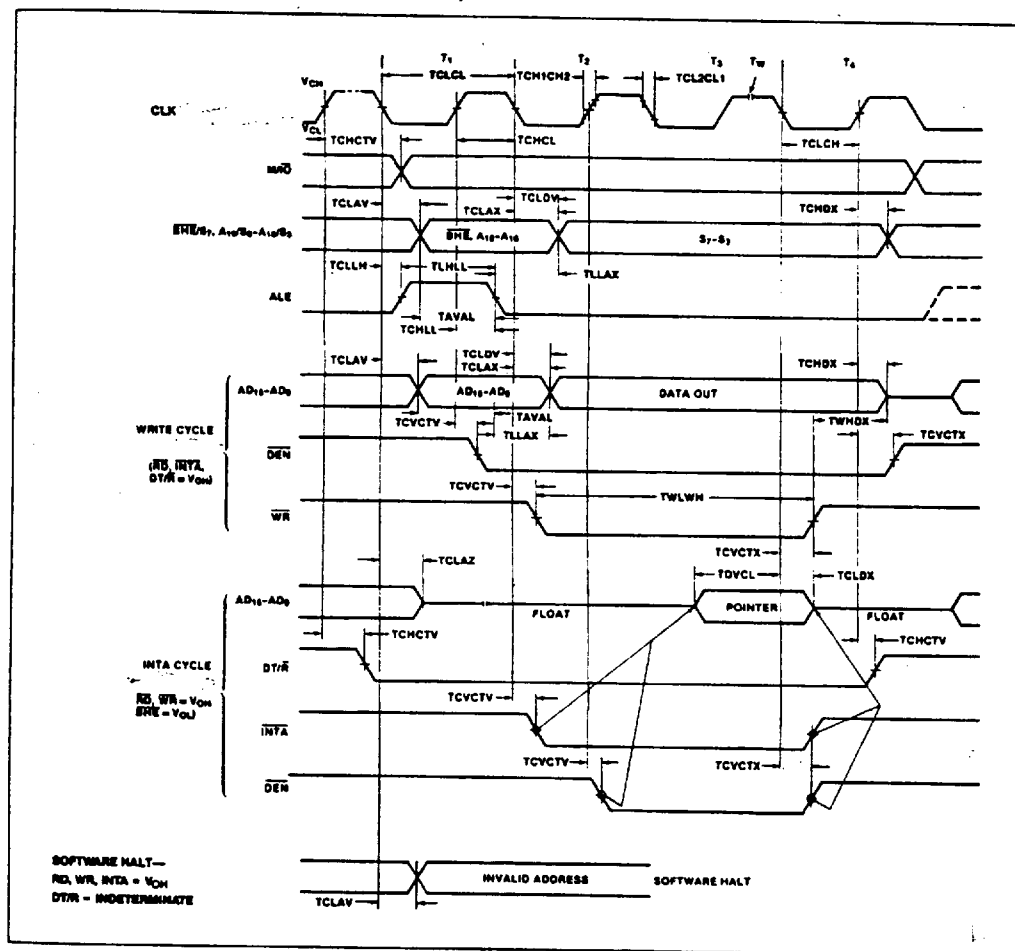
MINIMUM MODE



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MINIMUM MODE (Continued)



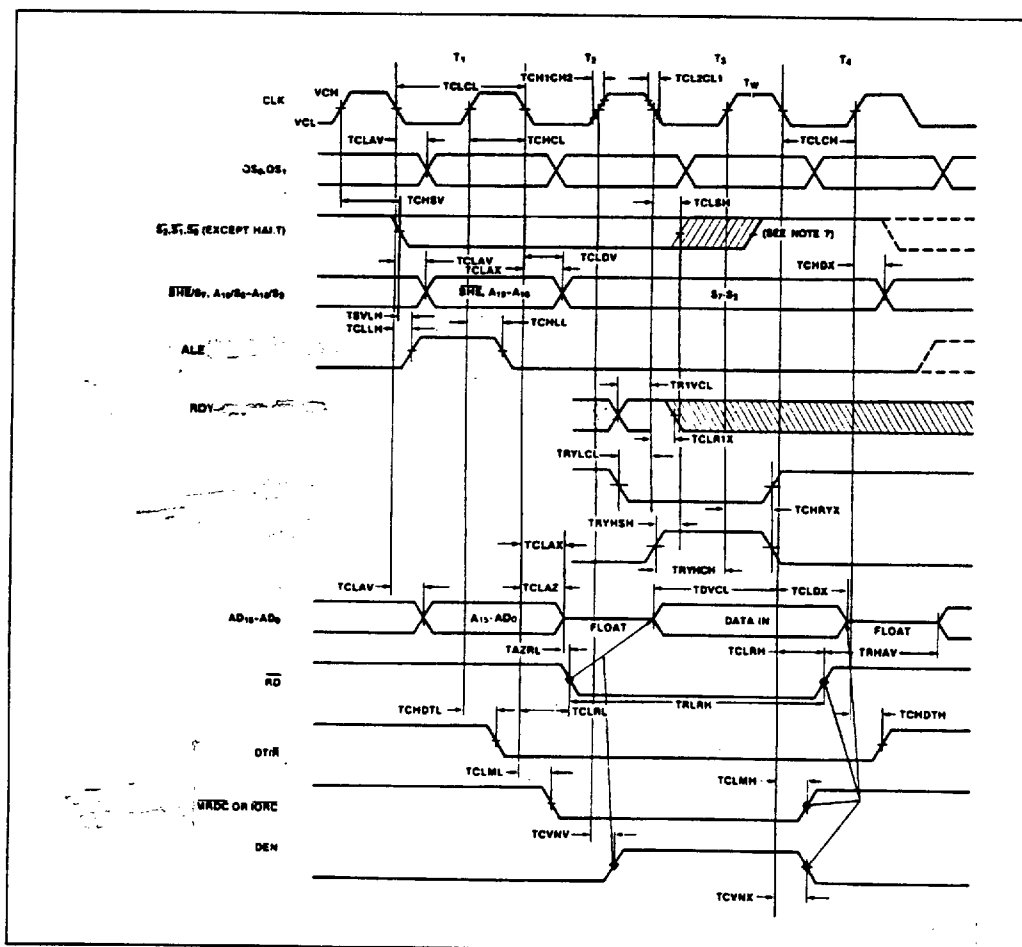
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MAXIMUM MODE



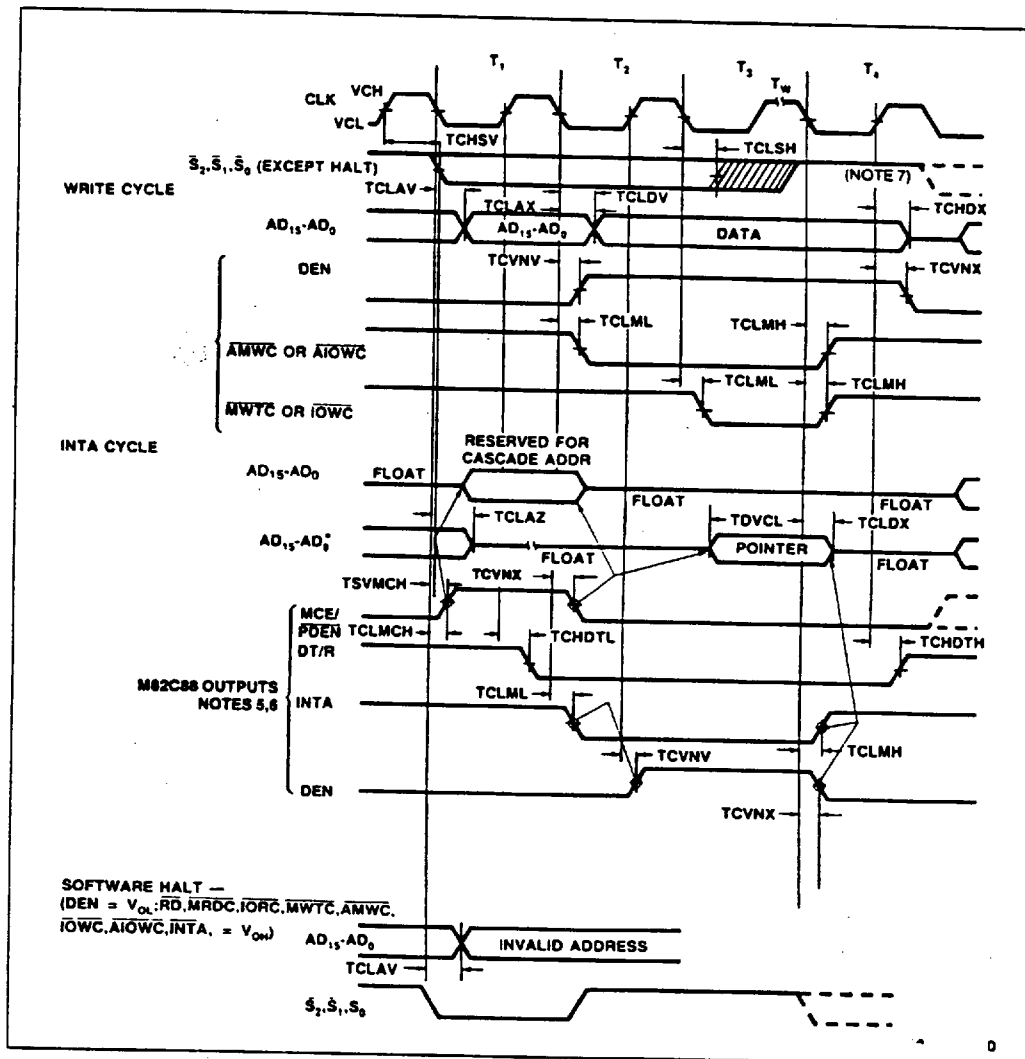
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MAXIMUM MODE (Continued)



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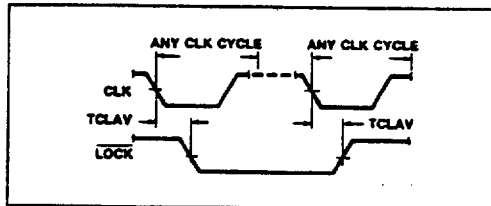
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ASYNCHRONOUS SIGNAL RECOGNITION

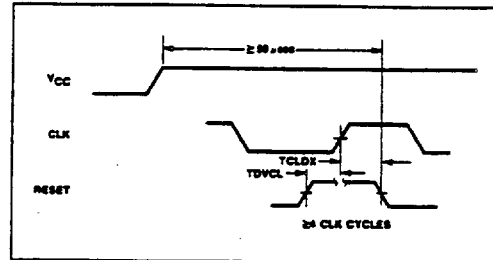


NOTE: Setup requirements for asynchronous signals only to guarantee recognition at next CLK.

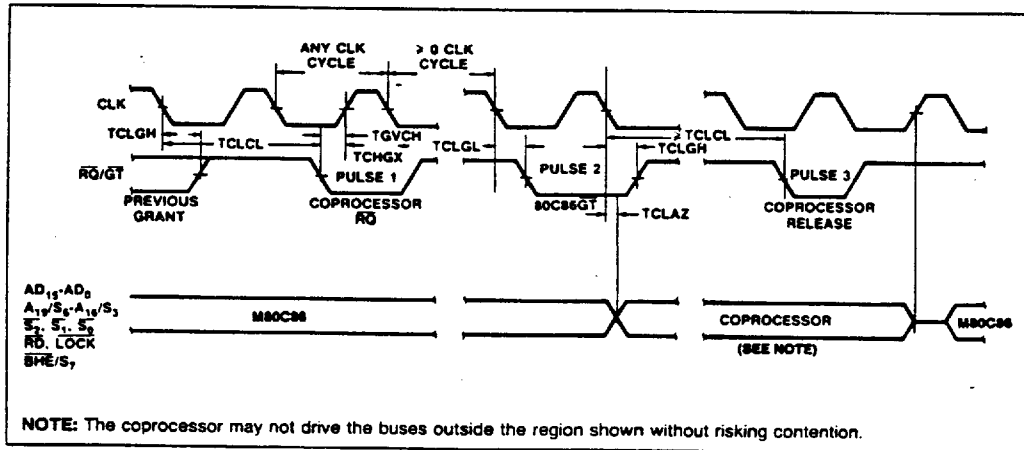
BUS LOCK SIGNAL TIMING (MAXIMUM MODE ONLY)



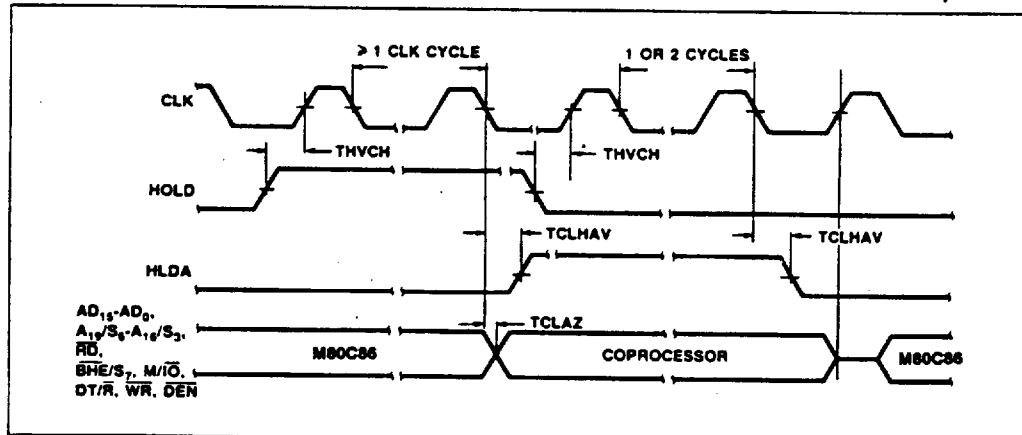
RESET TIMING



REQUEST/GRANT SEQUENCE TIMING (MAXIMUM MODE ONLY)



HOLD/HOLD ACKNOWLEDGE TIMING (MINIMUM MODE ONLY)



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80C86RP PINOUT DESCRIPTION

PIN	SIGNAL	DESCRIPTION	PIN	SIGNAL	DESCRIPTION
1	NC	No Connect	23	NC	No Connect
2	GND	Ground	24	RESET	Reset
3	AD14	Address Data Bus	25	RDY	Ready
4	AD13	Address Data Bus	26	TEST\	Test\
5	AD12	Address Data Bus	27	QS1	Queue Status
6	AD11	Address Data Bus	28	QS0	Queue Status
7	AD10	Address Data Bus	29	S0\	Status
8	AD9	Address Data Bus	30	S1\	Status
9	AD8	Address Data Bus	31	S2\	Status
10	AD7	Address Data Bus	32	LOCK\	Lock\
11	AD6	Address Data Bus	33	RQ\GT1\	Request/ Grant
12	AD5	Address Data Bus	34	RQ\GT0\	Request/ Grant
13	AD4	Address Data Bus	35	RD\	Read
14	AD3	Address Data Bus	36	MN/MX\	Minimum/ Maximum
15	AD2	Address Data Bus	37	BHE/S7	Bus High Enable/ Status
16	AD1	Address Data Bus	38	A19/S6	Address/ Status
17	AD0	Address Data Bus	39	NC	No Connect
18	NC	No Connect	40	A18/S5	Address/ Status
19	NMI	Non-Maskable Interrupt	41	A17/S4	Address/ Status
20	INTR	Interrupt Request	42	A16/S3	Address/ Status
21	CLK	Clock	43	AD15	Address Data Bus
22	GND	Ground	44	Vcc	+5V Power Supply Pin



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