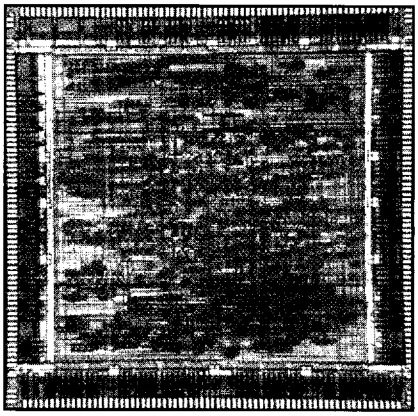
Rockwell

Cyclone Series™ GaAs Gate Arrays

Introduction



The sub-micron Cyclone Series™ of GaAs gate arrays from Rockwell represent the culmination of over ten years of research and development. The Cyclone Series allow new levels of performance due to an enhanced heterojunction MESFET (HMESFET) that provides better DC noise margin than other GaAs MESFET technologies.

The HMESFET process also features an advanced polyimide dielectric for reduced capacitance and a highly planarized architecture. The HMESFET's inherently superior noise margin and relative immunity to variations in temperature yields devices that exhibit superior speed at relatively low power dissipation.

Features

- Three array sizes from 30,000 to 100,000 raw gates
- Operating speeds up to 1GHz
- Advanced HMESFET process for better performance than other GaAs MESFET technologies
- Channelless sea-of-gates architecture
- 0.5 micron effective gate length
- TTL, ECL, and PECL compatible I/O cells
- 3-layer metal for routing and power distribution
- 3-input primary cell can be configured into NOR, NAND, or AND-OR-INVERT functions
- 40 pS delay @ 0.15 mW for 3-input NOR; 85 pS delay @ 0.25 mW for buffered 3-input NOR
- Low, regular, and high drive macrocell options
- Commercial (0 to +70 °C), industrial (-40 to +85 °C), and military (-55 to +125 °C) operating temperature ranges available
- Standard power supplies — ECL-only: -2 V; mixed ECL/TTL or TTL-only: +3.3 V & -2 V; PECL-only: +5 V and +3 V
- Cadence, Mentor*, and Viewlogic* CAD support
- Synopsys Design Compiler™ for logic synthesis*
- Verilog-XL for behavior modeling & simulation
- GT-Estimater™ (Gate Timer): PC-based gate delay and power estimation software*
- At-speed testing up to 660 MHz (1.3 GHz in multiplexed mode)

* Contact factory for availability

Cyclone Series Gate Array Features

Array	Raw Gates	Usable Gates[1]	D Flip Flops[1,2]	I/O Cells[3]	Package[4]
CC100K	98K	34.3K	5.7K	164	256 LDCC
CC60K	60K	21K	3.5K	140	196 LDCC
CC30K	30.3K	10.6K	1.8K	112	164 LDCC

NOTES:

[1] Estimate based on 35% utilization of core cells. [2] Based on minimally configured D flip flop using 6 core cells.

[3] Each I/O cell can be used for a TTL, ECL, or PECL type input output, bi-directional or high drive clock buffer. Some restrictions may apply to the utilization of I/O. Refer to the design manual for more information.

[4] Low cost package option planned.

The Cyclone arrays offer programmable digital IC performance in an industry-standard ASIC platform. The Cyclone Series' sea-of-gates architecture, combined with an advanced high density cell design, provide integration levels up to 100,000 available equivalent gates — to meet the challenge of today's most demanding applications.

Rockwell's world class manufacturing capability offers low cost assembly and packaging. Statistical Process Control (SPC) helps to ensure that products are built right the first time. High speed testing is available using an HP83000 VLSI tester capable of 660 MHz (1.3 GHz in mux mode).

Applications

The Cyclone Series of gate arrays are designed for use in today's most demanding high performance products. Applications that strain the capabilities of CMOS or that cannot handle the high power dissipation of ECL or BiCMOS are ideal for Cyclone arrays. In CMOS-based systems, the Cyclone Series opens up bottlenecks and will interface directly with CMOS, allowing the system designer to achieve the highest performance at the most economical cost. Extended temperature capabilities make the Cyclone Series perfect for harsh environments such as communications or military/aerospace applications.

Computers: Cache Controllers, Data Encryption, Error Detection and Correction, Memory Controllers, Data Switching, Math Co-Processors;

Communications: SONET Multiplexing and Switching, ATM Controllers, Video and Data Compression, Cellular Base Station Controllers;

Testers: Pin Electronics, Formatting & Switching Data;

Digital Signal Processing: Real-Time Processing, Video and Imaging Processing, Data Acquisition Signal Processing, Direct Digital Synthesis;

Medical: MRI, Sensor Multiplexing, Data Analysis and Control.

Enhanced Technology

The Cyclone Series is fabricated using a 0.5 micron L_{EFF} gate with three layers of metal for signal routing and power distribution. The process features high noise margins, low input capacitance, relatively low power, and high output drive current. The typical loaded gate delay for a buffered 3-input NOR is 85 picoseconds.

Second Generation GaAs Process

Fabrication of the Cyclone Series is accomplished using an advanced HMESFET process. This process employs a 0.5µ channel, self-aligned gate (see figure 1). A heterojunction is formed by the AlGaAs junction and the GaAs substrate. A highly reliable multi-layer interconnect structure is achieved by using AlCu, the metal most commonly used in VLSI silicon processing.

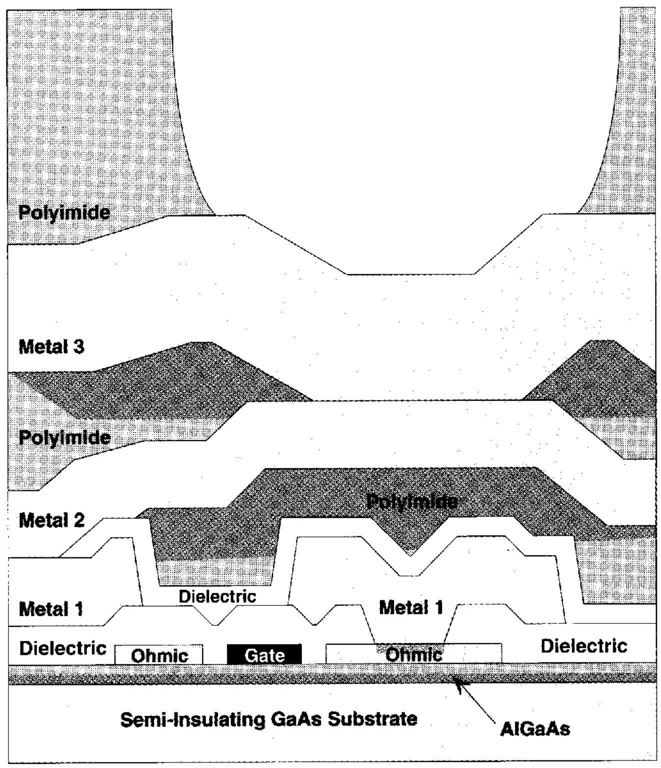


Figure 1
HMESFET cross-section: 0.5µ effective gate lengths, three layers of metal, and polyimide dielectric.

The HMESFET process also uses tapered contacts and vias, in addition to a polyimide dielectric for increased interconnect performance.

The combination of a small feature size and heterostructure device provides both high gate density and low power dissipation. The typical power dissipation for a gate delay is only 0.25 mW (fanout = 1).

Metal Routing for Personalizations

The many years of volume CMOS manufacturing experience and extensive research into new materials has enabled Rockwell to develop a superior metal routing scheme that allows for increased cell utilization. Interconnection flexibility is achieved by using all three metal layers for signal and power routing (see figure 2).

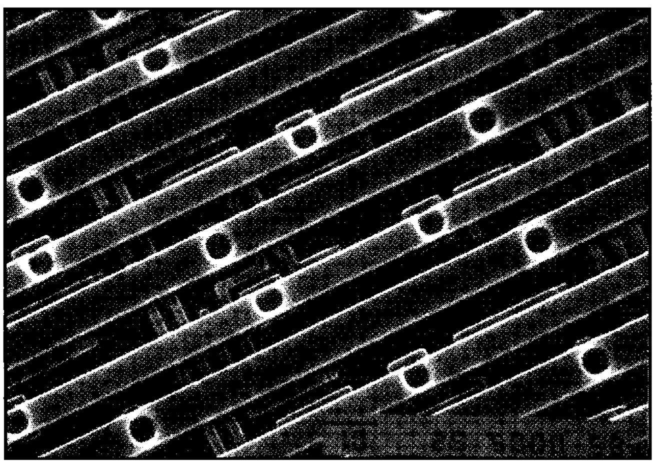


Figure 2
Scanning electron microscope photo showing three layer metallization of the Cyclone Series HMESFET process.

For maximized performance, Rockwell has developed an advanced polyimide dielectric for a highly planarized process and reduced capacitance in metal lines. The use of this state-of-the-art dielectric significantly increases each macro's drive capability, thereby reducing the delay on long or critical paths.

Placement and routing of metal interconnect is automated and optimized through the use of Cadence's "Gate Ensemble" (TANGATE). Some of Gate Ensemble's features include: timing driven placement (net and path constrained), soft grouping of macros, clock tree synthesis, incremental layout changes, and highly accurate distributed RC calculations.

Architecture

The Cyclone Series gate array architecture is based on an advanced 0.5 micron (effective gate length) heterojunction MESFET technology implemented as inherently power efficient direct-coupled FET logic (DCFL) with a super-buffer option. This unique approach yields the highest speed performance with the lowest possible power dissipation.

The Cyclone Series gate arrays enable the designer to optimize the overall chip design for the best speed-power product. In a typical gate array design, only portions of the circuit in a critical path require the fastest performance available. Therefore, the Cyclone core cells are based on an efficient low power and high density design that includes additional structures which allow a circuit designer to selectively boost the performance of speed-critical sections without increasing the number of core cells required for a given combinatorial function.

Core cells in the Cyclone arrays are configured as 3-input gates that are optimized for both gate density and route-ability in a channelless architecture. Each core cell can support a NAND, NOR, or AND-OR-INVERT function taking full advantage of all 3 inputs without sacrificing speed or performance. This is achieved by the higher gate clamping voltage of HMESFET devices.

D-type flip-flops require only 6 core cells in the Cyclone array, in contrast to a typical 2-input core cell approach that uses 10 or more core cells per flip-flop. Further, the addition of an extra FET and diode (shared between two core cells in the Cyclone arrays) further increases macro design flexibility by providing a power efficient super-buffer option.

Input and Output (I/O) Cells

Every I/O cell in the Cyclone array can be fully configured as an input, output, bidirectional, or high drive clock buffer. When used as an input buffer, the HMESFETs high noise margin in conjunction with built-in feedback and hysteresis circuit provide excellent input noise margin and stability for TTL, ECL, and PECL levels supported by the Cyclone arrays. Other I/O functions such as 3-state and open drain functions are also available. To reduce system noise due to the fast slew rate of the internal GaAs FETs, TTL output buffers with slew rate control are also supported.

Clock Trees

During layout or pre-placement of macrocells, optimized clock trees may be synthesized for the Cyclone arrays. In a typical CC100K design that is heavily populated with flip-flops, clock trees can easily support frequencies above 1GHz.

Power Supplies

The Cyclone Series utilizes industry-standard power supplies. In an ECL-only configuration, -2 V is the only power form required. In designs that utilize mixed ECL/TTL or TTL only, the chip requires -2 V and +3.3 V supplies. Power supply variation is required to be controlled within ±5%. The ECL-only version can be operated in PECL mode with +5 V and +3 V supplies.

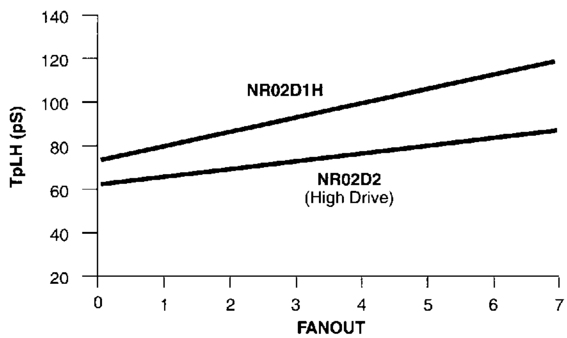


Figure 3
Comparison of gate delay for high drive vs. standard drive macrocells.

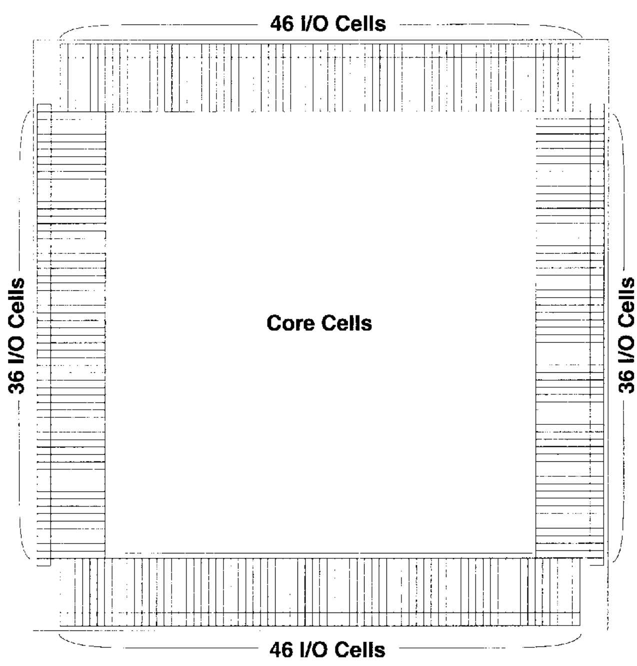
GT-Estimater™ (Gate Timing Modeler)

The GT-Estimater is a path delay calculator available for Rockwell ASIC products. This application features a graphical interface and runs on any PC with Windows™ 3.1. The GT-Estimater lets the designer quickly estimate delays for critical paths for any sequence of gates — allowing quick comparisons of alternate strategies. GT-Estimater accounts for intrinsic delays, wiring capacitance, and input pin capacitance. Wiring capacitance can be entered directly or GT-Estimater will calculate approximate capacitance per fanout based on gate density, cell pitch, and process dependent parameters.

Macrocell Library

Internal macrocells include both combinatorial and sequential functions with complexities ranging from simple logic gates to larger functions such as full adders and multiplexers. Many of the macrocells include high drive versions. The benefit of high drive over standard drive is the greater fanout capacity with less of an impact on propagation delay (see figure 3).

Block Diagram: The CC100K



List of Macrocells in the Cyclone Series Library

Following is a representative list of the macrocells available for designs in the Cyclone arrays. New cells are under development and the customer is advised to consult with the factory for desired functions not represented in this list.

Most cells are available with multiple drive/speed options. The performance of some selected macrocells can be seen on page 6. For complete specifications on the entire library, see the Cyclone Series Gate Array Design Manual.

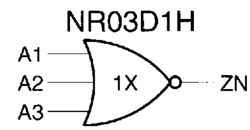
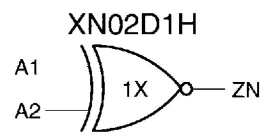
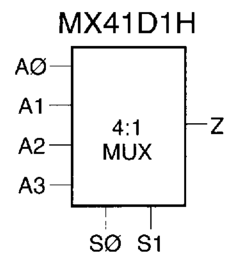
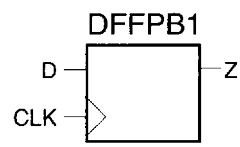
Cell Name	Function	# of Cells
Input/Output Cells - ECL/PECL		
PE4BCD	Non-Inverting Bi-Directional ECL Buffer with Clock Driver	1 I/O Cell
PE4BD1	Non-Inverting Bi-Directional ECL Buffer with 1X Drive	1 I/O Cell
PE4BD2	Non-Inverting Bi-Directional ECL Buffer with 2X Drive	1 I/O Cell
PE4BFD1	Inverting Bi-Directional ECL Buffer with 1X Drive	1 I/O Cell
PE4BFD2	Inverting Bi-Directional ECL Buffer with 2X Drive	1 I/O Cell
PE4CD1	Non-Inverting ECL Input Buffer with Clock Driver	1 I/O Cell
PE4DCD	Differential Non-Inverting ECL Input Buffer with Clock Driver	2 I/O Cells
PE4DD1	Differential Non-Inverting ECL Input Buffer with 1X Drive	2 I/O Cells
PE4DD2	Differential Non-Inverting ECL Input Buffer with 2X Drive	2 I/O Cells
PE4DFD1	Differential Inverting ECL Input Buffer with 1X Drive	2 I/O Cells
PE4DFD2	Differential Inverting ECL Input Buffer with 2X Drive	2 I/O Cells
PE4ID1	Non-Inverting ECL Input Buffer with 1X Drive	1 I/O Cell
PE4ID2	Non-Inverting ECL Input Buffer with 2X Drive	1 I/O Cell
PE4IFD1	Inverting ECL Input Buffer with 1X Drive	1 I/O Cell
PE4IFD2	Inverting ECL Input Buffer with 2X Drive	1 I/O Cell
PE4OD1	50 Ohm ECL Output Buffer	1 I/O Cell
PE4OD2	25 Ohm ECL Output Buffer	2 I/O Cells
Input/Output Cells - TTL		
PT4BD1	Bi-Directional TTL Buffer with Open Drain	1 I/O Cell
PT4BZD1	Bi-Directional TTL Buffer with Tri-State Enable	1 I/O Cell
PT4ID1	Non-Inverting TTL Input Buffer with 1X Drive	1 I/O Cell
PT4CD1	Non-Inverting TTL Input Buffer with Clock Driver	1 I/O Cell
PT4OD1	Open Drain TTL Output Buffer	1 I/O Cell
PT4ZD1	Tri-State TTL Output Buffer	1 I/O Cell
Simple Gates		
AO01D1	2/2 AND-OR-Invert with 1X Drive	4
AO01D1H	2/2 AND-OR-Invert with 1X Drive and High Speed	4
AO04D1	2/1 AND-OR-Invert with 1X Drive	2
AO04D1H	2/1 AND-OR-Invert with 1X Drive and High Speed	2
AO04D2	2/1 AND-OR-Invert with 2X Drive	§
AO05D1	2/1/1 AND-OR-Invert with 1X Drive	4
AO05D1H	2/1/1 AND-OR-Invert with 1X Drive and High Speed	4
DC24D1	2 to 4 Line Decoder with 1X Drive	§
DC38D1	3 to 8 Line Decoder with 1X Drive	§
DR04D1	4-Bit Parallel-In/Parallel-Out Shift Register	§
DR08D1	8-Bit Parallel-In/Parallel-Out Shift Register	§
IN01D1	Inverter with 1X Drive	2
IN01D2	Inverter with 2X Drive	4
IN01D1H	Inverter with 1X Drive and High Speed	2
ND02D1	2-Input NAND with 1X Drive	2
ND02D1H	2-Input NAND with 1X Drive and High Speed	2
ND02D2	2-Input NAND with 2X Drive	§
NI01D1	Non-Inverting Buffer with 1X Drive	§
NI01D2	Non-Inverting Buffer with 2X Drive	§
NR02D1	2-Input NOR with 1X Drive	2
NR02D1H	2-Input NOR with 1X Drive and High Speed	2
NR02D2	2-Input NOR with 2X Drive	4
NR03D1	3-Input NOR with 1X Drive	2
NR03D1H	3-Input NOR with 1X Drive and High Speed	2
NR03D2	3-Input NOR with 2X Drive	§
NR04D1	4-Input NOR with 1X Drive	4
NR04D1H	4-Input NOR with 1X Drive and High Speed	4
NR05D1	5-Input NOR with 1X Drive	4
NR05D1H	5-Input NOR with 1X Drive and High Speed	4
NR06D1	6-Input NOR with 1X Drive	4
NR06D1H	6-Input NOR with 1X Drive and High Speed	4
NR07D1	7-Input NOR with 1X Drive	6
NR07D1H	7-Input NOR with 1X Drive and High Speed	6
NR08D1	8-Input NOR with 1X Drive	6

Cell Name	Function	# of Cells
***Simple Gates** (continued)*		
NR08D1H	8-Input NOR with 1X Drive and High Speed	6
OA04D1	2/1 OR-AND-Invert with 1X Drive	2
OA04D1H	2/1 OR-AND-Invert with 1X Drive and High Speed	2
OA04D2	2/1 OR-AND-Invert with 2X Drive	§
SCCNNB	Synchronous Counter (Buffered) with CLEAR	§
SCCNNN	Synchronous Counter with CLEAR	§
SCSNNB	Synchronous Counter (Buffered) with SET	§
SCSNNN	Synchronous Counter with SET	§
SR04D1	4-Bit Serial-In/Parallel-Out Shift Register	§
SR08D1	8-Bit Serial-In/Parallel-Out Shift Register	§
XN02D1H	2-Input Exclusive-NOR with 1X Drive and High Speed	4
XN02D2	2-Input Exclusive-NOR with 2X Drive	§
XO02D1	2-Input Exclusive-OR with 1X Drive	3
XO02D1H	2-Input Exclusive-OR with 1X Drive and High Speed	3
XO02D2	2-Input Exclusive-OR with 2X Drive	§
Adders		
FAD1	1-Bit Full Adder with 1X Drive	10
FAD1H	1-Bit Full Adder with 1X Drive and High Speed	10
FAD4CH	4-Bit Full Adder with Carry Look-Ahead, 1X Drive and High Speed	§
HAD1	1-Bit Half Adder with 1X Drive	5
HAD1H	1-Bit Half Adder with 1X Drive and High Speed	6
Flip Flops		
DFCTSB	D Flip-Flop (positive edge triggered) Buffered with SCAN, CLEAR, Q and QN	§
DFFP01	D Flip-Flop (positive edge triggered) Unbuffered	4
DFFPB1	D Flip-Flop (positive edge triggered) Buffered	8
DFFPC0	D Flip-Flop (positive edge triggered) Buffered with CLEAR	8
DFFPGU	D Flip-Flop (positive edge triggered) Unbuffered Pass Gate	5
DFFPS0	D Flip-Flop (positive edge triggered) Buffered with SET	8
DFPCA0	D Flip-Flop (positive edge triggered) Unbuffered - High Speed	12
DFPCA1	D Flip-Flop (positive edge triggered) Buffered - High Speed	12
DFPCS0	D Flip-Flop (positive edge triggered) Buffered with SET and CLEAR	8
DFSTSB	D Flip-Flop (positive edge triggered) Buffered with SCAN, SET, Q and QN	§
MDFPB1	D Flip-Flop (positive edge triggered) Buffered with Q and 2-Input Mux	§
MDFPC1	D Flip-Flop (positive edge triggered) Buffered with CLEAR and 2-Input Mux	§
MDFPS1	D Flip-Flop (positive edge triggered) Buffered with SET and 2-Input Mux	§
Multiplexers		
MX21D1	2-to-1 Multiplexer with 1X Drive	5
MX21D1H	2-to-1 Multiplexer with 1X Drive and High Speed	5
MX41D1	4-to-1 Multiplexer with 1X Drive	10
MX41D1H	4-to-1 Multiplexer with 1X Drive and High Speed	10
MX81D1	8-to-1 Multiplexer with 1X Drive	§
Latches		
LACNNB	D Latch (active high) Buffered with CLEAR	§
LACNNN	D Latch (active high) Unbuffered with CLEAR	§
LANTNB	D Latch (active high) Buffered	§
LANTNN	D Latch (active high) Unbuffered	§
LASNNB	D Latch (active high) Buffered with SET	§
LASNNN	D Latch (active high) Unbuffered with SET	§

NOTE: § Currently in development. Contact factory for availability.

Macrocell Examples

(V_{TT} = -2.0V, V_{CC} = V_{CCA} = GND, T_C = 25 °C, Propagation delay: intrinsic)

Parameter		Min	Typ	Max	Units	Function/Symbol
Propagation Delay A1, A2, A3 to ZN	rising falling	49 28	82 40	86 42	pS pS	**H3-input NOR, Drive 1**
Load Dependent Delay, (Delay/fF)	rising falling	0.26 0.42	0.37 0.59	0.39 0.62	pS/fF pS/fF	
Input Capacitance		—	15	15	fF	
Power Dissipation		—	0.60	0.90	mW	
Propagation Delay A1, A2 to ZN	rising falling	110 75	150 115	158 121	pS pS	**H2-input XNOR, Drive 1**
Load Dependent Delay, (Delay/fF)	rising falling	0.22 0.80	0.32 0.99	0.34 1.04	pS/fF pS/fF	
Input Capacitance		—	25	25	fF	
Power Dissipation		—	1.13	1.79	mW	
Propagation Delay SØ, S1 to Z	rising falling	171 163	271 250	285 263	pS pS	**H4:1 Multiplexer, Drive 1**
Propagation Delay AØ, A1, A2, A3 to Z	rising falling	108 130	167 207	175 217	pS pS	
Load Dependent Delay, (Delay/fF)	rising falling	0.26 0.42	0.39 0.63	0.41 0.66	pS/fF pS/fF	
Input Capacitance		—	9	—	fF	
Power Dissipation		—	1.86	2.8	mW	
Propagation Delay CLK to Q	rising falling	138 165	182 221	191 232	pS pS	**Buffered D Flip-Flop Positive Edge Triggered**
T_{SET-UP}		195	260	273	pS	
T_{HOLD}		Ø	Ø	Ø	pS	
Load Dependent Delay, (Delay/fF)	rising falling	0.37 0.52	0.44 0.68	0.46 0.71	pS/fF pS/fF	
Input Capacitance		—	18	18	fF	
Power Dissipation		—	2.17	3.4	mW	

Absolute Maximum Ratings [1]

Symbol	Parameter	Value	Unit	Notes
T_{STOR}	Storage Temperature	-65 to +150	°C	
T_J	Junction Temperature	-55 to +150	°C	
T_C	Case Temperature Under Bias	-55 to +125	°C	
V_{TTL}	TTL Supply Voltage	-0.5 to +4.5	V	
V_{SS}	ECL Supply Voltage	-2.5 to +0.5	V	
V_{SS}(PECL)	PECL Supply Voltage	+2.5 to +0.5	V	
V_{CC}(PECL)	PECL Supply Voltage	+2.5 to +5.5	V	
V_{TTLIN}	Voltage Applied to Any TTL Input; Continuous	-1.0 to +4.3	V	[2]
V_{ECLIN}	Voltage Applied to Any ECL Input; Continuous	-3.0 to +1.0	V	[2]
V_{PECLIN}	Voltage Applied to Any PECL Input; Continuous	+2.0 to +6.0	V	[2]
I_{IN}	Current Into Any Input	-0.5 to +1	mA	
V_{TTLOUT}	Voltage Applied to Any TTL Output	-1.0 to +5.0	V	[5]
V_{ECLOUT}	Voltage Applied to Any ECL Output	-3.0 to +0.5	V	[3]
$V_{PECLOUT}$	Voltage Applied to Any PECL Output	+2.0 to +5.5	V	[4]
I_{TTLOUT}	Current From Any TTL Output; Continuous	-50 to +50	mA	
I_{ECLOUT}	Current From Any ECL Output; Continuous	-50	mA	
$I_{PECLOUT}$	Current From Any PECL Output; Continuous	-50	mA	
V_{BB}	Threshold Reference Voltage for ECL	-3.0 to +1.0	V	[6]
I_{BB}	Current Into ECL Reference	-0.5 to +1.0	mA	
V_{TT}	Load Terminating Voltage for ECL Output	-6.0 to +6.0	V	

NOTES:

[1] Sustained application may result in damage to the device. Each parameter may be applied to the device one at a time.
[2] Device under test is powered up with nominal supply voltages. [3] Subject to I_{ECLOUT} and power dissipation.
[4] Subject to $I_{PECLOUT}$ and power dissipation. [5] Output in high impedance state. [6] Device with V_{BB} input option.

Recommended Operating Conditions [1]

Symbol	Parameter	Min	Nom	Max	Notes
V_{TTL}	TTL Supply Voltage	+3.1 V	+3.3 V	+3.5 V	[2]
V_{SS}	ECL Supply Voltage	-1.9 V	-2.0 V	-2.1 V	[2]
V_{CC}(PECL)	PECL Supply Voltage	+4.8 V	+5.0 V	+5.2 V	[2]
V_{SS}(PECL)	PECL Supply Voltage	+2.9 V	+3.0 V	+3.1 V	[2]
R_{LOAD}	ECL/PECL Output Termination Load	50 Ohms	50 Ohms	50 Ohms	[3]
T_{CC}	Commercial Case Temperature	0 °C	—	+70 °C	[4]
T_{CI}	Industrial Case Temperature	-40 °C	—	+85 °C	[4]
T_{CM}	Military Case Temperature	-55 °C	—	+125 °C	[4]

NOTES:

[1] Most negative power supply should be applied first. [2] Power supply variation should be within ±5%.
[3] For 25 Ohms load, 2 output buffers may be paralleled. [4] Case temperature measured at the heat-sink side of the package.

DC Characteristics (Over Recommended Operating Conditions)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions	Notes
TTL I/O							
V_{OH}	Output Voltage High	2.4	—	—	V	I_{OH} = -4.0 mA	[1]
V_{OL}	Output Voltage Low	—	—	0.4	V	I_{OL} = +8.0 to 16 mA	[1]
V_{IH}	Input Voltage High	2.0	—	V_{TTL}+1	V		
V_{IL}	Input Voltage Low	0	—	0.8	V		
I_{IH}	Input High Current	—	—	200	µA	V_{IN} = 2.4 V	
I_{IL}	Input Low Current	-50	—	—	µA	V_{IN} = 0.4 V	
I_{OZH}	3-state Output Leakage Current High	—	—	200	µA	V_{OUT} = 2.4 V	
I_{OZL}	3-state Output Leakage Current Low	-100	—	—	µA	V_{OUT} = 0.4 V	
I_{OZC}	Open Collector Output Leakage	—	—	200	µA	V_{OUT} = 2.4 V	
ECL I/O							
V_{OH}	Output Voltage High	-0.9	-0.8	—	V		
V_{OL}	Output Voltage Low	—	-1.8	-1.7	V		
V_{IH}	Input Voltage High	-1.1	-1.0	—	V	V_{BB} = -1.3 V	[2]
V_{IL}	Input Voltage Low	—	-1.6	-1.5	V	V_{BB} = -1.3 V	[2]
I_{IH}	Input High Current	—	—	200	µA	V_{IN} = -1.0 V	
I_{IL}	Input Low Current	-50	—	—	µA	V_{IN} = -1.6 V	
V_{BBS}	Internal Reference Voltage Out	-1.4	-1.3	-1.2	V		
PECL I/O [3]							
V_{OH}	Output Voltage High	4.1	4.2	—	V		
V_{OL}	Output Voltage Low	—	3.2	3.3	V		
V_{IH}	Input Voltage High	3.9	4.0	—	V	V_{BB} = 3.7 V	[2]
V_{IL}	Input Voltage Low	—	3.4	3.5	V	V_{BB} = 3.7 V	[2]
I_{IH}	Input High Current	—	—	200	µA	V_{IN} = +4.0 V	
I_{IL}	Input Low Current	-50	—	—	µA	V_{IN} = +3.4 V	
V_{BBS}	Internal Reference Voltage Out	3.6	3.7	3.8	V		

NOTES:

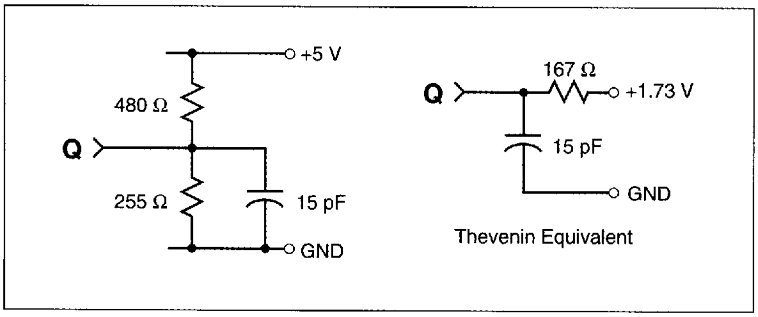
[1] TTL output buffer supports both +5 V system load and +3.3 V system load.

[2] Typical reference voltage is applied externally to device under test. Using an internal reference voltage generator may degrade VIH and VIL over power supply variation.

[3] Requires both +5 V and +3 V power supplies to operate an ECL-only device in the PECL mode.

AC Test Load for Output Buffers

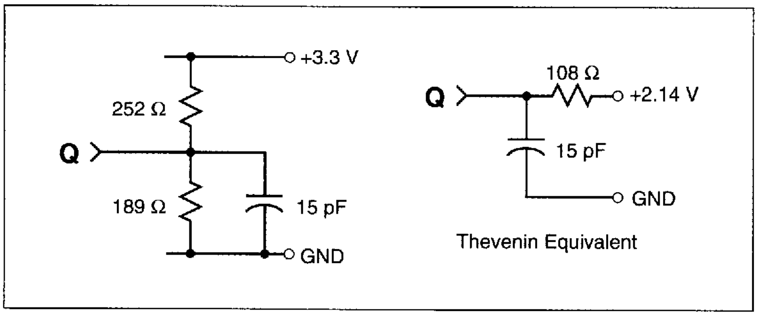
1. TTL Output Load[1]
   a) Load from +5 V System



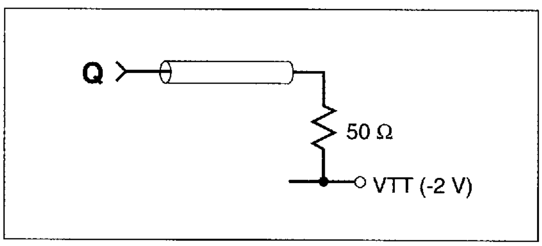
NOTES:

[1] TTL power supply for Cyclone arrays is +3.3 V only.

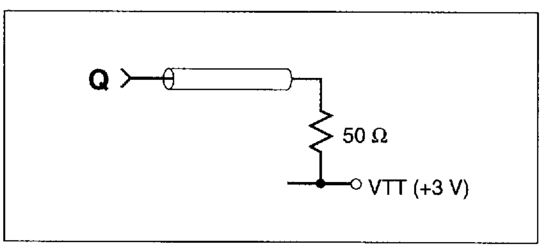
   b) Load from +3.3 V System



2. ECL Output Load

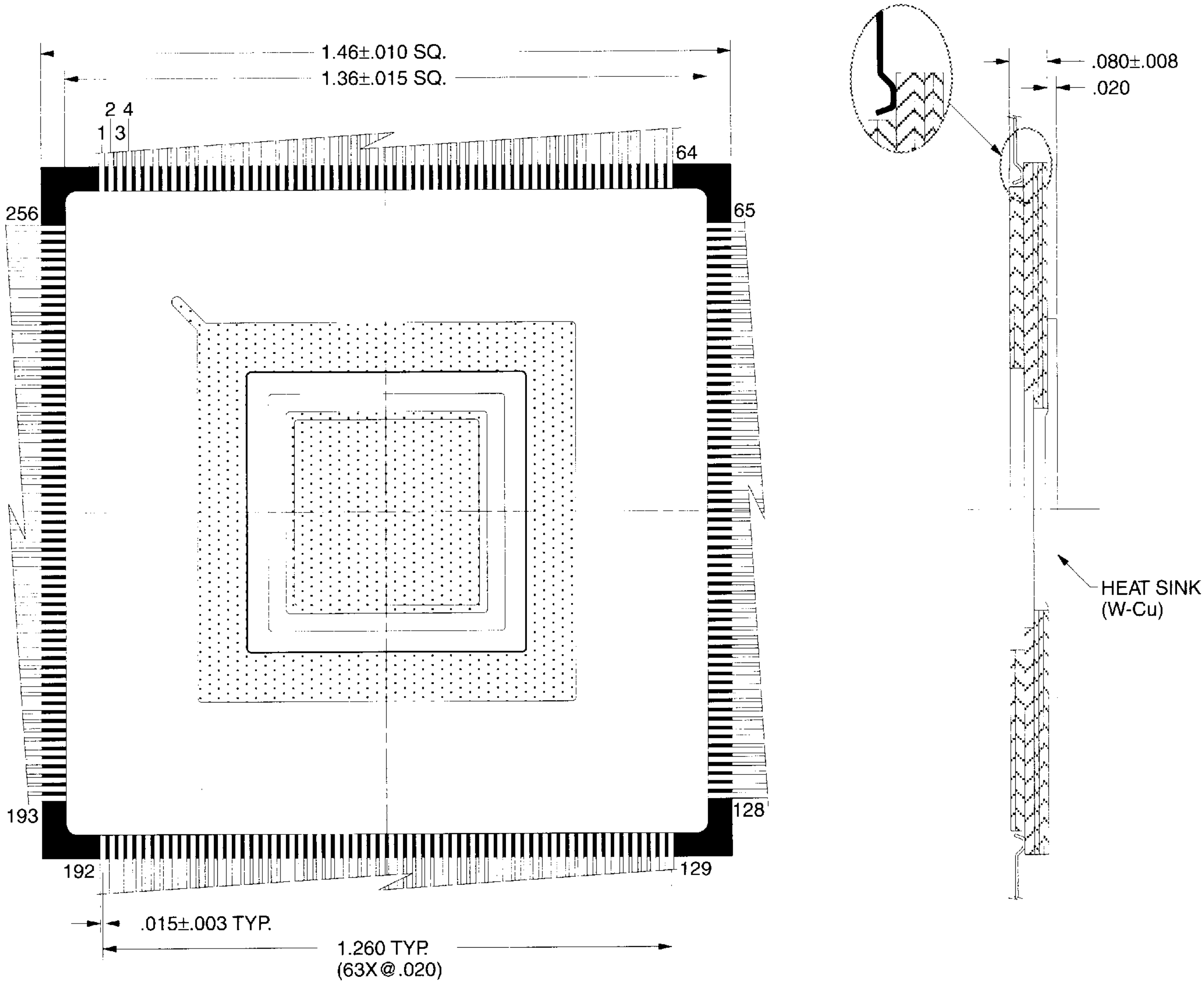


3. PECL Output Load



Packaging

Shown below is the surface-mount 256-pin leaded ceramic chip carrier available for CC100K gate array designs. All packages offered for the Cyclone Series of gate arrays are high performance, cavity-down, multi-layer ceramic packages that feature a copper-tungsten heat sink for efficient thermal transfer. The 256-pin package provides excellent performance featuring controlled impedance isolated signal planes, good cross talk control, and very low thermal resistance. Contact factory for the latest information regarding packages for the CC30K and CC60K.



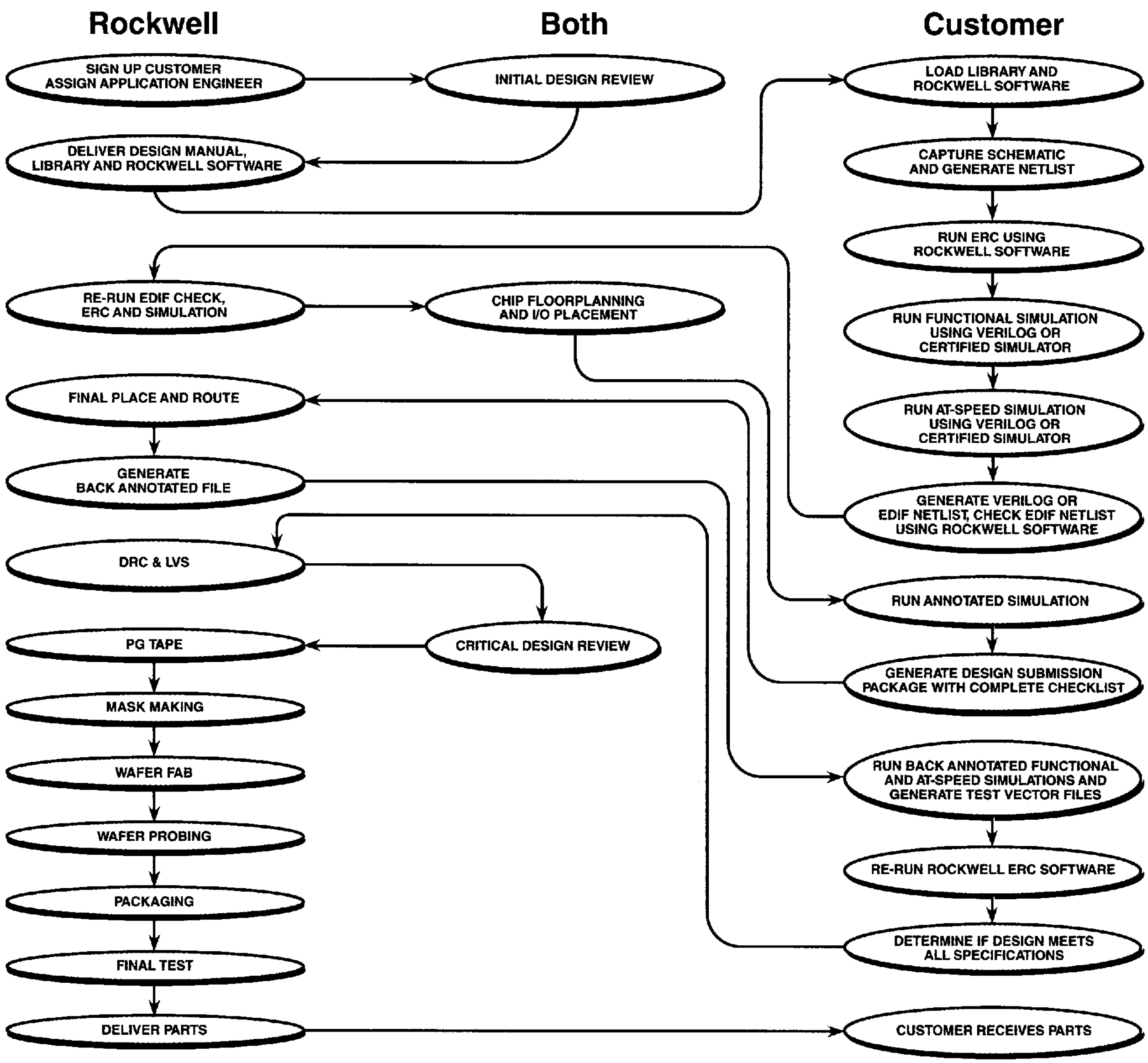
NOTES:
1. METALIZATION/PLATING:
   TUNGSTEN (OR EQUIV.) + NICKEL (80μ" MIN.) + GOLD (60μ" MIN.)
2. ALL TOLERANCES UNLESS SPECIFIED: ±1%, NOT LESS THAN .005
3. ALL DIMENSIONS IN INCHES

Implementation

The Rockwell gate array implementation flow is designed to be efficient, flexible, and reliable. Rockwell offers customers the choice to do their own ASIC design, or have Rockwell engineers perform a turn-key implementation based on a detailed set of specifications. A Rockwell engineer is assigned to every customer at the start of a project to track progress and answer questions. In every design, the following steps are normally performed by Rockwell's application engineers.

- Final placement of macrocells
- Routing of metal interconnection
- Extraction of back-annotated net-lengths
- Final design rule checks
- Verification of layout-versus-schematic

The flowchart below summarizes a typical gate array project and the delegation of the various tasks.



Design Support

Cyclone Series designs are currently supported on Cadence platforms. Front-end design support is also currently under development for Mentor and Viewlogic platforms. Additional support is planned for logic synthesis through Synopsys.

The HP83000 VLSI Tester

The state-of-the-art HP83000 features a tester-per-pin architecture. The HP83000 can test at a maximum rate of 660 MHz on pins used for data generation and acquisition or bi-directional I/O. 1.3 GHz rates are achievable by multiplexing. The tester features 10 pS resolution and 50 pS accuracy. A sophisticated interface between the test head and a wafer probe station allows at-speed tests to be performed on processed wafers.

Test Vector Requirements

For all designs in a Cyclone Series gate array, Rockwell requires that the customer supply functional test vectors in combination with either a set of critical path vectors or a set of at-speed vectors. The use of at-speed or critical path delay vectors depends on the specific requirements of each customer, and a brief description of each follows:

Functional Vectors - These vectors are used to test the functionality of the ASIC and can be performed on devices in die form or after they are packaged. The functional vectors specify combinations of input stimuli and the resulting outputs for all paths. These vectors can be generated from simulations at 10 MHz. Functional vectors must be timing-independent.

Critical Path Delay Vectors - These vectors are used to verify the timing of critical paths. The timing relationships between all input stimuli and their associated effect on outputs of critical paths must be well-defined.

At-Speed Vectors - These vectors verify timing requirements and at-speed functionality. At-speed testing is carried out on the HP83000 VLSI tester. At-speed tests can be performed on packaged devices or on processed wafers. At-speed vectors should be generated from logic/timing simulations at full speed.

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