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SSI 78P233A
DS-1 Line Interface

January 1992

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DESCRIPTION

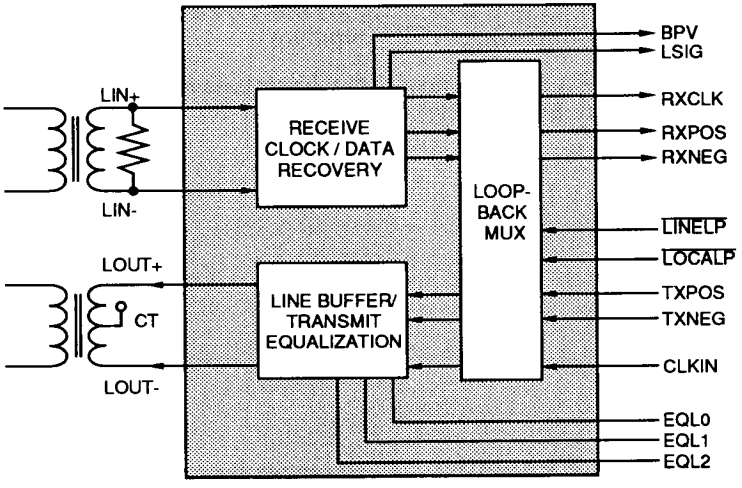
The SSI 78P233A DS-1 Line Interface is a bipolar integrated circuit that provides the interface functions necessary to convert DS-1-level signals to TTL-level and conversely. The receiver section accepts alternate-mark-inversion (AMI) encoded line data and provides separated and synchronized data and clock outputs. The transmitter section accepts data and clock and produces AMI pulses of appropriate shape for transmission. A loopback multiplexer is also provided that permits interchange of the signals between the sections.

The 78P233A requires a single 5V supply. It is available in a standard, 600-mil DIP package.

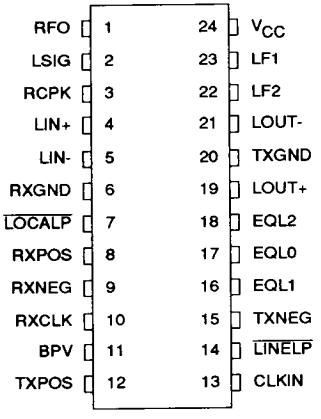
FEATURES

- **Single-chip transmit and receive DS-1 Line Interface**
- **Unique clock recovery circuit, requires no crystals or tuned components**
- **Variable jitter tolerance, adjustable with external components**
- **Pulse-shape transmission conformant with AT&T Compatibility Bulletin 119 specifications**
- **Six different line equalization settings for pulse-shaping at the DSX-1 level**
- **Two alternate transmit settings for 6V-peak pulses**
- **Standard unipolar TTL-level clock & data ports for easy equipment interface**
- **Line-loopback and local-loopback control**
- **Loss-of-signal indication**
- **Bipolar violation detection**

BLOCK DIAGRAM



PIN DIAGRAM



24-Pin DIP

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The device consists of receiver and transmitter sections together with a "loopback" means which permits interchange of signals between the sections (See Figure 1).

RECEIVER

The receiver input is normally transformer-coupled to the source of encoded alternate polarity pulses. To provide a tracking threshold for amplitude-detecting these pulses, the signal is peak detected and a fixed percentage of the peak value is applied to the comparators which detect individual positive and negative pulses. An external R-C network is required to provide the proper storage of the peak reference value. Should the detected peak value fall below an acceptable level, the Loss of Signal (LSIG) output becomes active. This output may be used as a logical control signal or is able to drive a fault indicator LED directly.

Outputs of the data comparators are connected to the clock recovery circuits. The clock recovery system employs a unique phase-locked-oscillator loop which has an auxiliary frequency-sensitive acquisition loop which is active only when cycle-slipping occurs between the received signal rate and the internal oscillator. This system permits the loop to independently lock to the frequency and phase of the incoming data stream without the need for high-precision and/or adjustable oscillators or tuned circuits. Non-precision external components are required, however, to establish the oscillator center frequency and loop bandwidth.

The phase-locked reference oscillator is employed to strobe the detected data into output latches and is also available as an output for externally synchronizing the data.

Additional circuits are provided to detect received bipolar violations. These deviations from the alternate mark inversion format are detected when two or more successive pulses of the same polarity are received. A resultant violation output is in time coincidence with the violating received signal output.

TRANSMITTER

The transmitter combines unipolar logical inputs with an input clock to provide positive and negative output pulses onto a transformer-coupled line.

Internal equalizer networks are selected by combinations of the three Equalizer Select inputs so that the waveform at the terminal end of various lengths of cable is as required. Note that the transmitter output pulse widths are determined by the input clock width, so that it must be carefully controlled to provide acceptable outputs.

The transmitter pulse selection logical function is arranged so that the simultaneous occurrence of both positive and negative transmit data inputs inhibits the output driver. Moreover, the driver has a current-limiting feature which protects the circuit in the event of a shorted load or inadvertent shorting of an output to the supply voltage.

LOOPBACK CONTROL SECTION

The loopback control section is essentially a multiplexer which is capable of directing received data and clock to the transmitter section, or directing transmit input data and clock to the receiver outputs. This "looping" is controlled by two active low logic signals, $\overline{\text{LINELP}}$ and $\overline{\text{LOCALP}}$, respectively.

The bipolar violation output is held inactive when the circuits are in the Local Loopback mode.

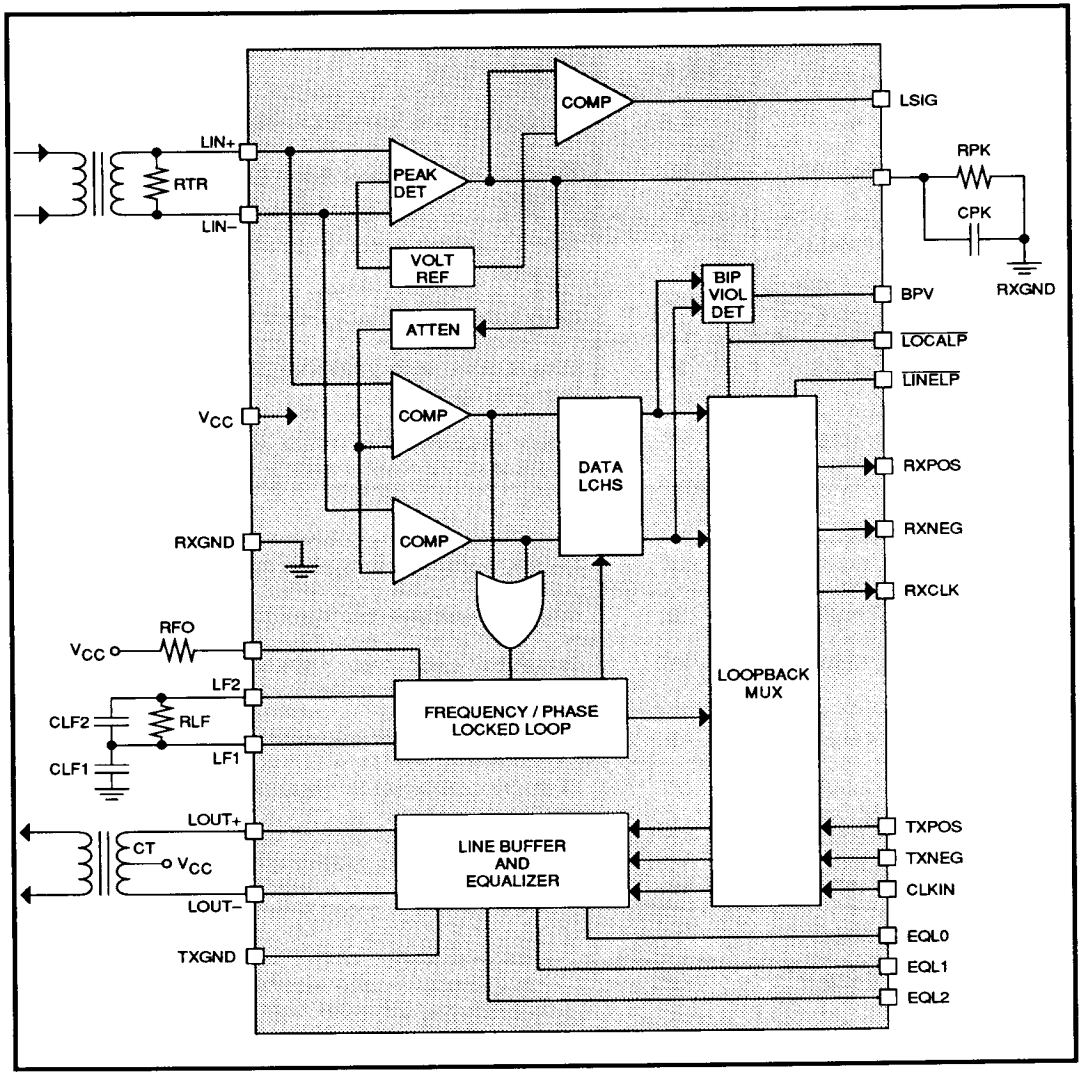


FIGURE 1: Functional Diagram

PIN DESCRIPTION

RECEIVER

I/O	LABEL	PIN NO.	DESCRIPTION
I	LIN+, LIN-	4, 5	Differential inputs, transformer-coupled from line.
O	RXPOS	8	Unipolar receiver output, active as result of positive pulse at inputs.
O	RXNEG	9	Unipolar receiver output, active as result of negative pulse at inputs.
O	RXCLK	10	Clock pulses recovered from line data.
O	LSIG	2	Loss-of-signal output indicating that input signal is less than threshold value.
O	BPV	11	Bipolar violation output, active as a result of successive pulses at inputs of same polarity.

TRANSMITTER

I	TXPOS	12	Unipolar transmitter data input, active high.
I	TXNEG	15	Unipolar transmitter data input, active high.
I	CLKIN	13	Transmitter clock input. Controls transmit pulse width. Transmit is active when low.
O	LOUT+	19	Output to transformer for positive data pulses.
O	LOUT-	21	Output to transformer for negative data pulses.
I	EQL0 EQL1 EQL2	17 16 18	Line equalizer control signals. Selected according to Table 1 for various cable lengths.

LOOPBACK CONTROL

I	$\overline{\text{LINELP}}$	14	Low level causes receiver recovered data and clock to be connected to the transmitter. Data and clock continue to be present at receiver outputs.
I	$\overline{\text{LOCALP}}$	7	Low level causes transmitter input data and clock to be connected to the receiver outputs. Input data continues to be transmitted.

PIN DESCRIPTION (continued)

EXTERNAL COMPONENT CONNECTION

I/O	LABEL	PIN NO.	DESCRIPTION
I	RFO	1	Resistor connected to Vcc to provide basic center frequency of receiver phase locked loop oscillator.
-	LF1 LF2	23 22	Resistor-capacitor loop filter network to RXGND to establish bandwidth of phase locked loop.
-	RCPK	3	Parallel resistor-capacitor network connected to RXGND to determine charge/discharge characteristics of peak detector.

POWER

-	Vcc	24	Positive supply terminal for receiver circuits.
-	RXGND	6	Ground terminal for receiver circuits.
-	TXGND	20	Ground terminal for transmitter driver circuits.

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ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise noted. Operation above absolute maximum ratings may permanently damage the device.)

PARAMETER	RATING	UNIT
Vcc, Supply Voltage	-0.5 to +7.0	V
Storage Temperature	-65 to 130	°C
Soldering Temperature (10 sec.)	260	°C
Voltage Applied to Logic Inputs	-0.3 to Vcc +0.3	V
Maximum Power Dissipation	800	mW
Junction Operating Temperature	0 to +130	°C
NOTE: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.		

RECOMMENDED OPERATING CONDITIONS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Ta	Ambient temperature		0		70	°C
Vcc	Power supply voltage		4.75		5.25	V
VIH	High-level input voltage		2.0			V
VIL	Low-level input voltage				0.8	V
IOH	High-level output current	LSIG pin only; VO = 1.5V	-7		-13	mA

EXTERNAL COMPONENTS (Refer to Figure 1 for location of components.)

RFO	Loop center frequency resistor	1% tolerance		6.04		kΩ
RLF	Loop filter resistor			12.0		kΩ
CLF1	Loop filter capacitor			0.022		µF
CLF2	Loop filter capacitor			430.0		pF
RPK	Peak-detector resistor			36.0		kΩ
CPK	Peak-detector capacitor		0.0015	0.015	0.15	µF
	Transmit line transformer	Refer to Table 3		---		---

D. C. ELECTRICAL CHARACTERISTICS
(T_A = 0°C to 70°C, Vcc = 5V ± 5%, unless otherwise specified.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
ICC	Supply current	All outputs open		83	110	mA
IIH	High-level input current	VIH = 2.7V			20	µA
IIL	Low-level input current	VIL = 0.4V			-0.36	mA
VOH	High-level output voltage	IOH = -400 µA	2.7			V
VOL	Low-level output voltage	IOL = 2.0 mA		0.48	0.6	V
		IOL = 2.0 mA, LSIG pin			0.4	V
RIN	Receiver input resistance		800	1000	1250	Ω

DYNAMIC CHARACTERISTICS AND TIMING, TRANSMITTER
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise specified. Transmit pulse characteristics are obtained using a line transformer which has the characteristics shown in Table 3. Refer to Figure 2.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TTCF	Transmit clock repetition period			648		nsec
TTC	Transmit clock pulse width			324		nsec
TTCNT	Transmit clock negative transition time				10	nsec
TTCPT	Transmit clock positive transition time				10	nsec
TTPDS TTNDS	Transmit data set-up time		15			nsec
TTPDH TTNDH	Transmit data hold time		0			nsec
TTPL	Transmit positive line pulse width	See Note 1	TTC-5		TTC+5	nsec
TTNL	Transmit negative line pulse width	See Note 1	TTPL-5		TTPL+5	nsec
POL	Transmit line pulses power level	See Note 2				
	Transmit line pulses waveshape	See Notes 2 & 3				

Note 1: Measured at transformer with minimum line equalization

Note 2: Characteristics are in accordance with AT&T Compatibility Bulletin 119, Table 1 and Table 3 for line lengths and equalizer settings as shown in Table 1 of this document.

Note 3: Characteristics are in accordance with Table 2 for equalizer settings shown therein.

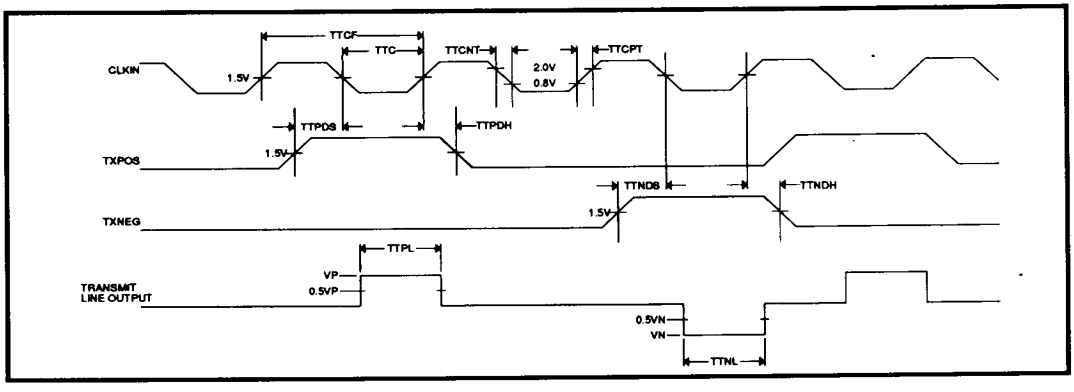


FIGURE 2: Transmit Waveforms

DYNAMIC CHARACTERISTICS AND TIMING, RECEIVER
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise specified. External component values as specified in Recommended Operating Conditions; see Note 1. Refer to Figure 3.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIN	Input signal voltage		±1.5		±3.7	Vpk
VLOS	Loss-of-signal indicating voltage		±0.5		±1.0	Vpk
TLOS	Loss-of-signal delay time	Timed from removal of input signal; See Note 2	0.7TPK		1.3TPK	sec
VDTH	Receive data detection threshold	Relative to peak amplitude	65		75	%
TSTAB	Receiver stabilization time	After application of input signal			5	msec
TRCF	Receive clock period			648		nsec
TRC	Receive clock pulse width		314	324	334	nsec
TRCPT	Receive clock positive transition time	C_L = 25 pF		5	10	nsec
	rise time	C_L = 25 pF; 10% - 90%		35	50	nsec
TRCNT	Receive clock negative transition time	C_L = 25 pF		3	10	nsec
	fall time	C_L = 25 pF; 10% - 90%		10	15	nsec
TRDP TRDN	Positive or negative receive data pulse width			648		nsec
TRDPS TRDNS	Receive data set-up time		290			nsec
TRDPH TRDNH	Receive data hold time		290			nsec
TRBV	Receive bipolar violation pulse width			648		nsec
TRBVS	Receive bipolar violation set-up time		290			nsec
TRBVH	Receive bipolar violation hold time		290			nsec
	Receive input jitter tolerance high frequency	sine, 10 kHz to 100 kHz	±100			nsec
	Receive input jitter tolerance low frequency	sine, 300 Hz or less	±4			µsec

DYNAMIC CHARACTERISTICS AND TIMING, RECEIVER (Continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
KD	Clock Recovery Phase Detector Gain	(All 1's Data Pattern)	66		79	µA/Rad
KO	Clock Recovery Phase Locked Oscillator Control Gain		0.15		0.20	Megrad/ sec. Volt
Note 1: Input signal is transformer coupled, and in accordance with AT&T Compatibility Bulletin 119, Table 1, and Table 2 or Table 3; also, as attenuated by 0 to 655 feet of ABAM* cable.						
Note 2: TPK = RPK x CPK x ln((VIN + 1.2V)/(VLOS + 1.2V))						
* ABAM is the trade name for 22-gauge twisted-pair cable manufactured by AT&T.						

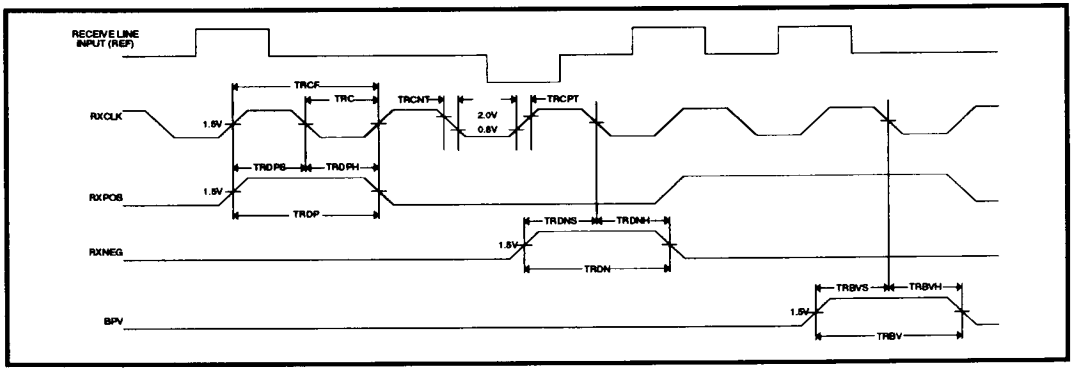


FIGURE 3: Receive Waveforms

TABLE 1: Equalizer Settings for Standard DSX-Level (3V-Peak Nominal) Pulses Versus ABAM Cable Length

CABLE LENGTH IN FEET	EQUALIZER SETTING		
	EQL0	EQL1	EQL2
0 to 50	0	0	0
51 to 131	1	0	0
131 to 262	0	1	0
262 to 393	1	1	0
393 to 524	0	0	1
524 to 655	1	0	1
Note: Output meets AT&T compatibility Bulletin 119, Figure 3, measured at the crossconnect. The only external transmit components required are a transformer as specified in Table 3 and proper line termination resistance.			

TABLE 2: Equalizer Settings for Non-DSX-Level (6V-Peak Nominal) Pulses

PULSE CHARACTERISTICS	EQUALIZER SETTING		
	EQL0	EQL1	EQL2
Rectangular 6.0 ± 0.6V pulse, 10% to 40% trailing edge overshoot	0	1	1
Rectangular 6.0 ± 0.6V pulse, less than 10% trailing edge overshoot	1	1	1
Note: Output waveform at transformer secondary; terminated in 100Ω load.			

TABLE 3: Transmit Line Transformer Characteristics
(Transmit line transformer characteristics are as specified below or as in Tautron's specification for part #5924-8301, Rev. A, 10/3/89).

CHARACTERISTIC	SYMBOL	MIN	NOM	MAX	UNIT
Turns ratio	N		1CT:1		
Primary open circuit inductance	Lp	1.25			mH
Primary leakage inductance	L1			2.0	µH
Primary volt-time product	ET	10			V-µsec
Primary DC resistance	Rp			1.0	Ω
Secondary DC resistance	Rs			1.0	Ω
Effective primary distributed capacitance	C'			15	pF

TABLE 4: Recommended Transmit Line Transformers

MANUFACTURER	PART NO.
AIE Magnetics	318-0765
AT&T	2745 AG
Pan-Mag (Tamura Corporation of America)	PHT-019
Pulse Engineering	PE 64936

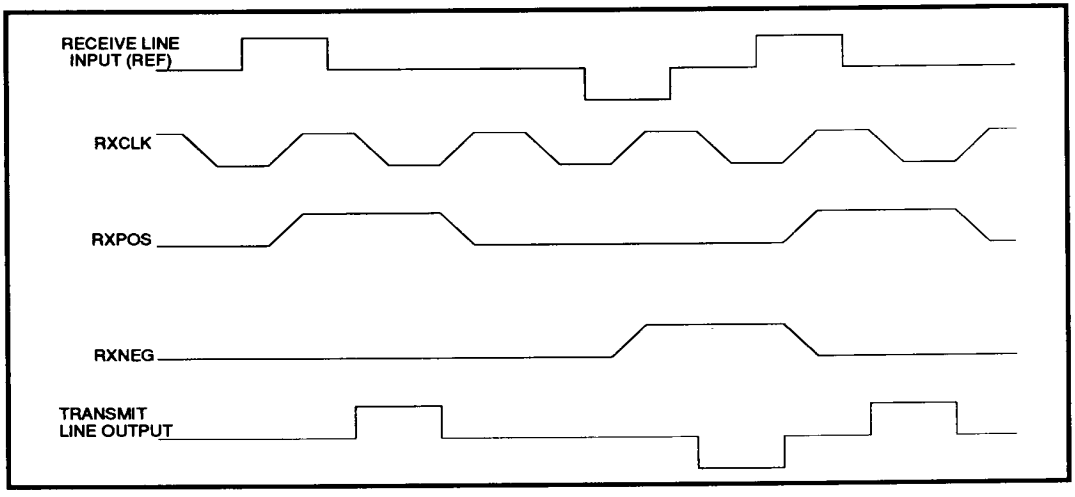


FIGURE 4: Line Loopback Waveforms

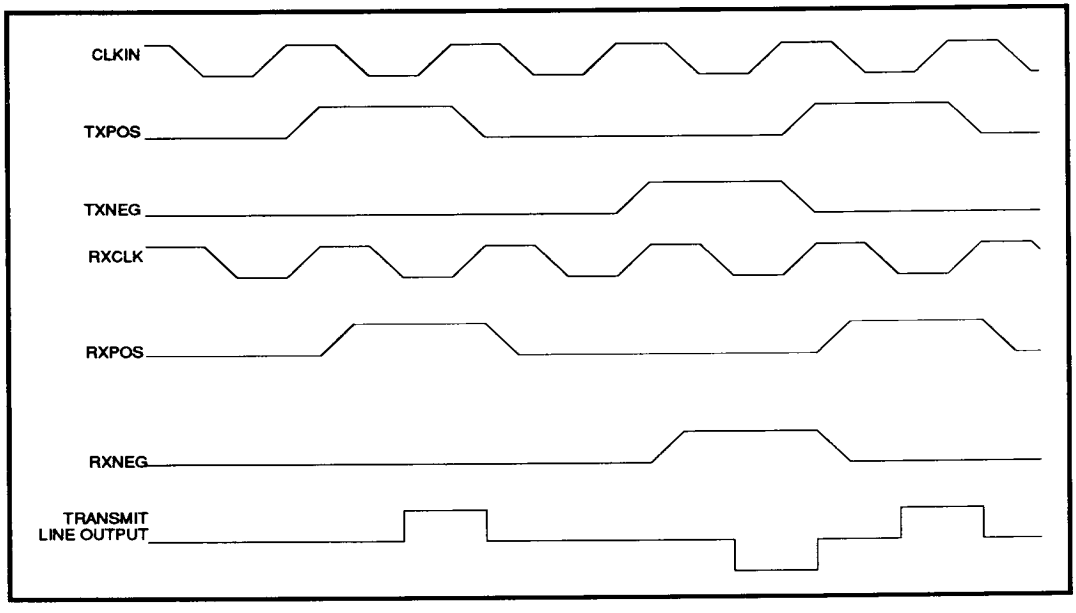
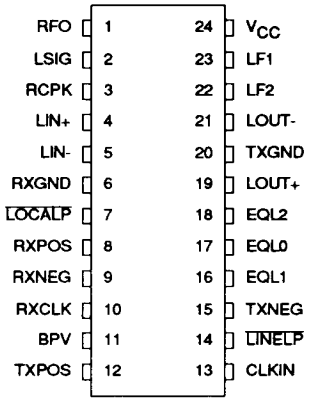


FIGURE 5: Local Loopback Waveforms

PACKAGE PIN DESIGNATIONS

(Top View)



24-Pin DIP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 78P233A, DS-1 Line Interface - 24-Pin		
Standard Width Plastic DIP (600 mil)	78P233A-CP	78P233A-CP

Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680, (714) 573-6000, FAX (714) 573-6914