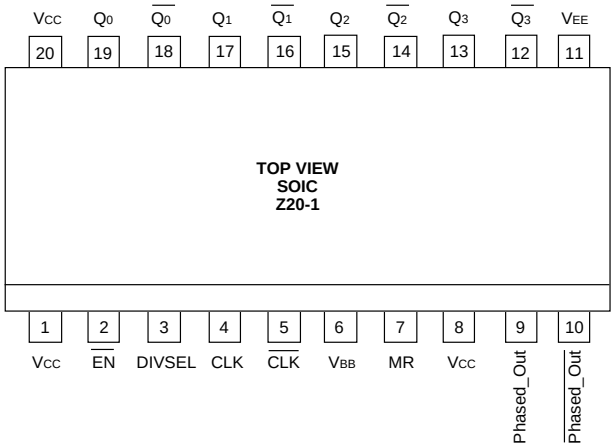
5V/3.3V ÷2, ÷4/6 CLOCK GENERATION CHIP

FEATURES

- **3.3V and 5V power supply options**
- **50ps output-to-output skew**
- **Synchronous enable/disable**
- **Master Reset for synchronization**
- **Internal 75KΩ input pull-down resistors**
- **Available in 20-pin SOIC package**

PIN CONFIGURATION/BLOCK DIAGRAM



DESCRIPTION

The SY10/100EL38/L are low skew ÷2, ÷4/6 clock generation chips designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The devices can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. In addition, by using the V_{BB} output, a sinusoidal source can be AC-coupled into the device. If a single-ended input is to be used, the V_{BB} output should be connected to the $\overline{CLK}$ input and bypassed to ground via a 0.01µF capacitor. The V_{BB} output is designed to act as the switching reference for the input of the EL38/L under single-ended input conditions. As a result, this pin can only source/sink up to 0.5mA of current.

The common enable ($\overline{EN}$) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

The Phase_Out output will go HIGH for one clock cycle whenever the ÷2 and the ÷4/6 outputs are both transitioning from a LOW to a HIGH. This output allows for clock synchronization within the system.

Upon start-up, the internal flip-flops will attain a random state; the master reset (MR) input allows for the synchronization of the internal dividers, as well as for multiple EL38/Ls in a system.

PIN NAMES

Pin	Function
CLK	Differential Clock Inputs
$\overline{EN}$	Synchronous Enable
MR	Master Reset
V_{BB}	Reference Output
Q_0, Q_1	Differential ÷2 Outputs
Q_2, Q_3	Differential ÷4/6 Outputs
DIVSEL	Frequency Select Input

TRUTH TABLE

CLK	$\overline{EN}$	MR	Function
Z	L	L	Divide
ZZ	H	L	Hold Q_{0-3}
X	X	H	Reset Q_{0-3}

NOTE:

Z = LOW-to-HIGH transition

ZZ = HIGH-to-LOW transition

DIVSEL	Q_2, Q_3 OUTPUTS
0	Divide by 4
1	Divide by 6

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DC ELECTRICAL CHARACTERISTICS[1]

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

Symbol	Parameter	T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{EE}	Power Supply Current													mA
	10EL	35	50	65	35	—	65	35	—	65	35	—	65	
	100EL	35	50	65	35	—	65	35	—	65	35	—	75	
V_{BB}	Output Reference Voltage 10EL	-1.43	—	-1.30	-1.38	—	-1.27	-1.35	—	-1.25	-1.31	—	-1.19	V
	100EL	-1.38	—	-1.26	-1.38	—	-1.26	-1.38	—	-1.26	-1.38	—	-1.26	
I_{IH}	Input High Current	—	—	150	—	—	150	—	—	150	—	—	150	µA

NOTE:

1. Parametric values specified at: 5 volt Power Supply Range 100EL38 Series: -4.2V to -5.5V.
   10EL38 Series -4.75V to -5.5V.
   3 volt Power Supply Range 10/100EL38L Series: -3.0V to -3.8V.

AC ELECTRICAL CHARACTERISTICS[1]

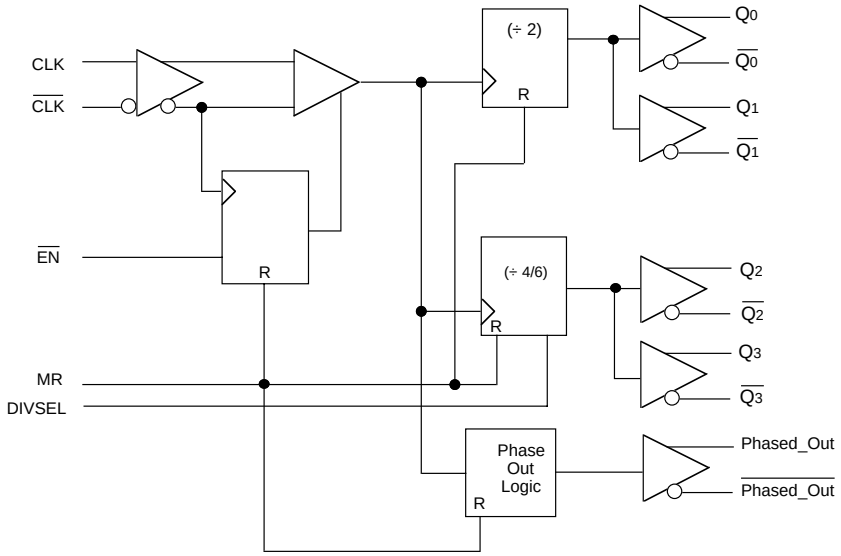
V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

Symbol	Parameter	T_A = -40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{MAX}	Maximum Toggle Frequency	1000	—	—	1000	—	—	1000	—	—	1000	—	—	MHz
t_{PLH} t_{PHL}	Propagation Delay to Output													ps
	CLK → Output (Diff.)	950	—	1150	950	—	1150	970	—	1170	1050	—	1250	
	CLK → Output (S.E.)	900	—	1200	900	—	1200	920	—	1220	1000	—	1300	
	MR → Output	600	—	900	600	—	900	600	—	900	600	—	900	
t_{skew}	Within-Device Skew[2] Q_0 — Q_3	—	—	50	—	—	50	—	—	50	—	—	50	ps
	All	—	—	75	—	—	75	—	—	75	—	—	75	
	Part-to-Part Q_0 — Q_3 (Diff.)	—	—	200	—	—	200	—	—	200	—	—	200	
	All	—	—	240	—	—	240	—	—	240	—	—	240	
t_S	Set-up Time $\overline{EN}$ → $\overline{CLK}$	300	150	—	—	150	—	—	150	—	—	150	—	ps
	DIVSEL → CLK	300	—	—	—	—	—	—	—	—	—	—	—	
t_H	Hold Time $\overline{CLK}$ → $\overline{EN}$	400	150	—	400	150	—	400	150	—	400	150	—	ps
	CLK → DIVSEL	400	200	—	400	200	—	400	200	—	400	200	—	
V_{PP}	Minimum Input Swing[3] CLK	250	—	—	250	—	—	250	—	—	250	—	—	mV
V_{CMR}	Common Mode Range[4] CLK	–1.3	—	–0.4	–1.4	—	–0.4	–1.4	—	–0.4	–1.4	—	–0.4	V
t_{RR}	Reset Recovery Time	—	—	100	—	—	100	—	—	100	—	—	100	ps
t_{PW}	Minimum Pulse Width CLK	800	—	—	800	—	—	800	—	—	800	—	—	ps
	MR	700	—	—	700	—	—	700	—	—	700	—	—	
t_r t_f	Output Rise/Fall Times Q (20% —80%)	280	—	550	280	—	550	280	—	550	280	—	550	ps

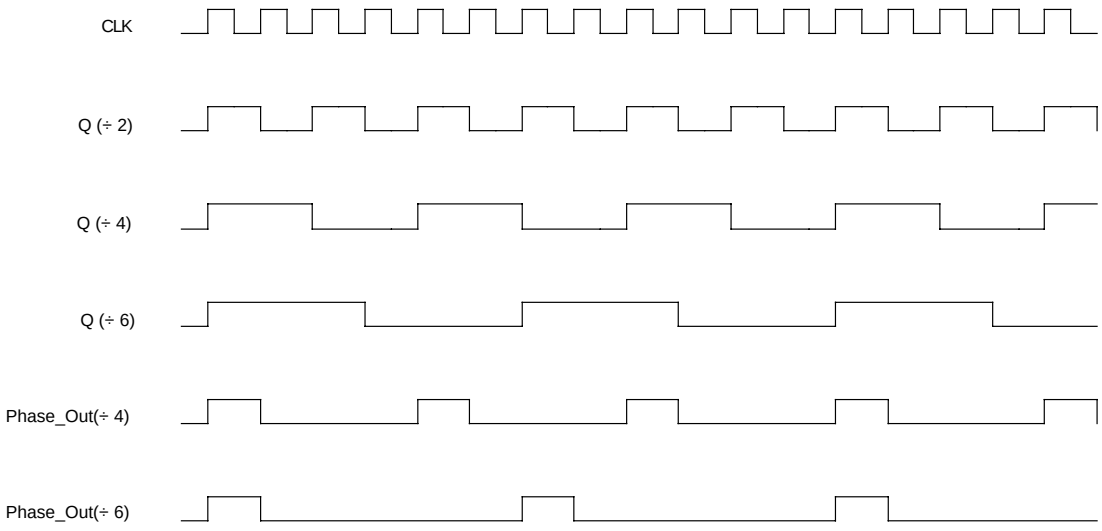
NOTES:

1. Parametric values specified at: 5 volt Power Supply Range 100EL38 Series: -4.2V to -5.5V.
   10EL38 Series -4.75V to -5.5V.
   3 volt Power Supply Range 10/100EL38L Series: -3.0V to -3.8V.
2. Skew is measured between outputs under identical transitions.
3. Minimum input swing for which AC parameters are guaranteed. The device will function reliably with differential inputs down to 100mV.
4. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP} min. and 1V. The lower end of the CMR range varies 1:1 with V_{EE}. The numbers in the spec table assume a nominal V_{EE} = –3.3V. Note for PECL operation, the V_{CMR} (min) will be fixed at 3.3V – IV_{CMR} (min)I.

LOGIC DIAGRAM



TIMING DIAGRAMS



PRODUCT ORDERING CODE

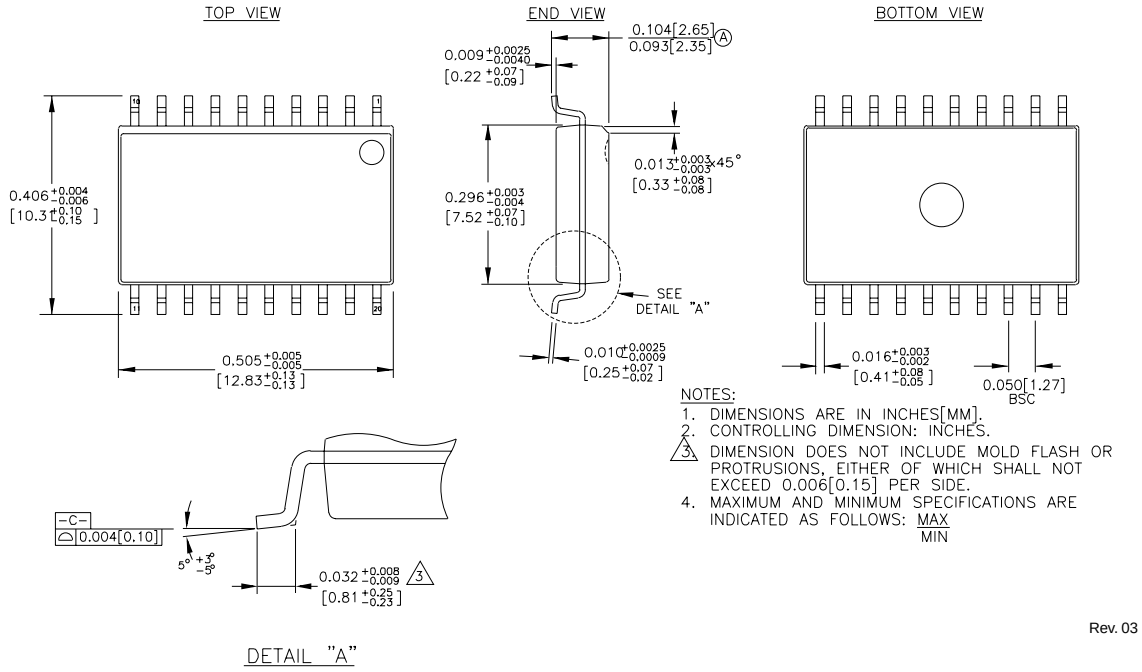
3.3V

Ordering Code	Package Type	Operating Range	V_{EE} Range (V)
SY10EL38LZC	Z20-1	Commercial	-3.0 to -3.8
SY10EL38LZCTR	Z20-1	Commercial	-3.0 to -3.8
SY100EL38LZC	Z20-1	Commercial	-3.0 to -3.8
SY100EL38LZCTR	Z20-1	Commercial	-3.0 to -3.8

5V

Ordering Code	Package Type	Operating Range	V_{EE} Range (V)
SY10EL38ZC	Z20-1	Commercial	-4.75 to -5.5
SY10EL38ZCTR	Z20-1	Commercial	-4.75 to -5.5
SY100EL38ZC	Z20-1	Commercial	-4.2 to -5.5
SY100EL38ZCTR	Z20-1	Commercial	-4.2 to -5.5

20 LEAD SOIC .300" WIDE (Z20-1)



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