HG62S Series
High-Speed CMOS Gate Array

HITACHI®

Description

The HG62S series free-channel gate arrays utilize a 0.8-μm CMOS process with triple metal interconnect technology. The series consists of 6 master slices ranging from 26,054 to 250,000 raw gates. The internal gate delay is as low as 0.3 ns/gate for ultrahigh-speed operation.

The macrocells are functionally compatible with the HG62E/F series, including RAM availability.

With the HG62S, it is easy to design high-speed, high-performance systems with on-chip autodiagnosis support.

Features

- Ultrahigh-speed operation (F0: fanout; Al: line length):
  - — Internal (2-input power NAND, FO = 2, Al = 2 mm): 0.3 ns typ
  - — Input buffer (FO = 2, Al = 2 mm): 1.2 ns typ
  - — Output buffer (C_L = 50 pF): 3.5 ns typ
- High density: 26,054–250,000 raw gates
- Autodiagnosis: Automatic test circuit and test pattern generation
- RAM capability
  - — Various single and dual-port RAMS
  - — Built-in autodiagnosis function

Table 1 Ordering Information

Item	HG62S026	HG62S038	HG62S058	HG62S079	HG62S125	HG62S250
Gate count	26,054	38,169	58,572	79,315	125,132	250,000
Pad count	144	172	208	240	296	400

Table 2 Maximum Available Signal Pins

Package Type	HG62S026	HG62S038	HG62S058	HG62S079	HG62S125	HG62S250
DILP64S	60	60				
QFP-100	96	96	96			
QFP-136	128	128	128	128		
QFP-168		152	152	152		
QFP-208			(under dev)	(under dev)	(under dev)	
QFP-232				(under dev)	(under dev)	
PLCC-68	(under dev)	(under dev)				
PLCC-84	(under dev)	(under dev)				
PGA-135	(under dev)	(under dev)	(under dev)	(under dev)		
PGA-179		(under dev)	163	163		
PGA-240				(under dev)	208	
PGA-256				(under dev)	224	224
PGA-299					(under dev)	(under dev)
PGA-400						256

Note: (under dev): Under development

- Macro cell library variation
  - — Functional compatibility with HG62E/F series (basic gates, flip-flops, etc.)
  - — Power-type cell variation
  - — Normal or scan type latches and flip-flops
- Wide variety of input and output cells
  - — Input, output, and I/O buffers
  - — TTL or CMOS levels
  - — Reduced noise output buffers
  - — Driving capacity: I_{OL} = 2, 8, 16 mA
  - — Oscillator, Schmitt-trigger inputs, pull up/down resistors
- Package variety: Multiple high pin count packages
- Design support environment
  - — Hierarchical design support
  - — Fault simulator for test pattern evaluation
  - — Automatic test pattern generation
  - — Local design support center
  - — EWS (engineering workstation) support

Logic Design Cautions

Number of Usable Gates

In free-channel gate arrays, basic cell area is utilized for routing. Therefore, the actual gate count depends on the logic circuit. Table 3 shows approximate gate counts.

If RAM is used, Hitachi needs to know the memory density (word/bit organization) and random logic gate counts to quote the best master slice selection.

Autodiagnosis

Automatic generation of high fault coverage (more than 90%) test circuits and test patterns requires the following:

- Two dedicated pins for test functions (figure 1).
- Scan type cells for all latches, flip-flops, and shift registers. Calculations for timing design and gate count estimation should use macro cells with the scan function. The names of macro cells with the scan function start with "T". For example, FD (normal) → (TFD) (scan type).
- Scan-type cells for RAM circuits under certain conditions. Autodiagnosis is also available for circuits with RAM, and the RAM itself can be autodiagnosed. Even when autodiagnosis is not required for RAM but only for the peripheral circuits, use RAM cells with the scan function (table 4, case 2).

Table 3 Approximate Actual Gate Counts

Master	HG62S026	HG62S038	HG62S058	HG62S079	HG62S125	HG62S250
Usable gates (1,000 gates)	9.1–10.4	13.3–15.2	20.5–23.4	27.7–31.7	43.7–50.1	85.5–100

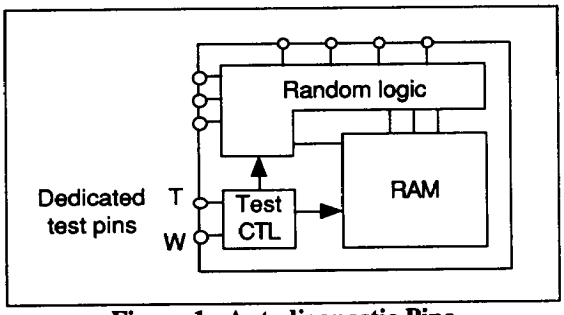


Figure 1 Autodiagnostic Pins

Blocks

Logically connected circuits can be placed in a block during layout. The maximum number of gates in a block should be 4,000. Also, the total number of gates in all blocks should be less than 60% of the total number of gates.

Gate Delay Time

Gate delay time calculations are more accurate using actual routing information. However, a rough estimation is needed to prevent timing design errors in the pre-route design phase. Gate delay times are estimated as follows:

$$t_{PLH} = t_{OLH} + (K_{lh} \times C_L)$$
$$t_{PHL} = t_{OHL} + (K_{hl} \times C_L)$$
$$C_L = \Sigma C_{AL} + 0.05 \times \Sigma LV$$

Where:

C_{AL}: Estimate load capacitance per fanout
LV: Input load constant

The macro cell library lists the t_{OLH}, t_{OHL}, K and LV constants for each MACRO Cell.

In delay time calculations, the estimate load capacitance per fanout depends on whether the circuits are part of a block layout (table 5).

Table 4 Autodiagnosis and RAM

	Case 1		Case 2		Case 3		Case 4	
	Random Logic	RAM	Random Logic	RAM	Random Logic	RAM	Random Logic	RAM
Autodiagnosis	Yes	Yes	Yes	No	No	Yes	No	No
Cell type	Scan	Scan	Scan	Scan	No scan	Scan	No scan	No scan

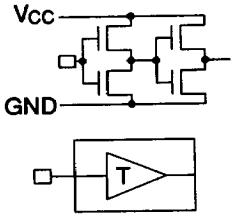
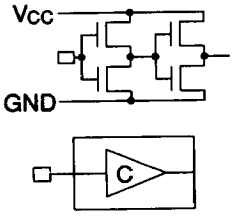
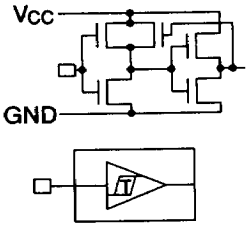
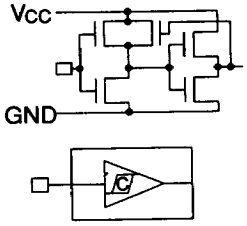
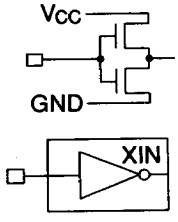
Table 5 Load Capacitance

		Not in Block	
	In Block	S026–S058	S079–S250
C_{AL}	0.12	0.35	0.55

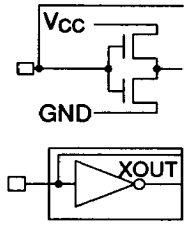
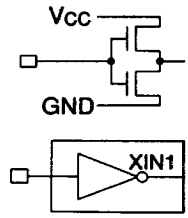
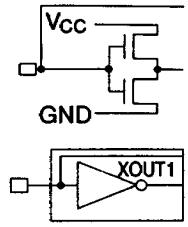
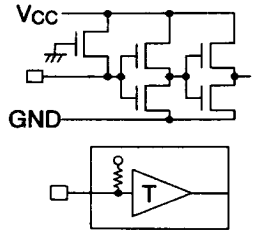
Note: Gate delay time distribution: 35%–180%
V_{CC} = 5 V ± 5%, Ta = –20°C to +75°C

Macro Cell Library

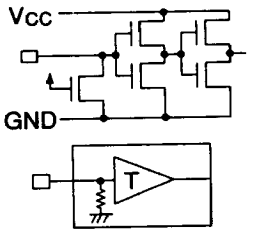
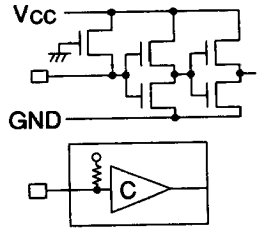
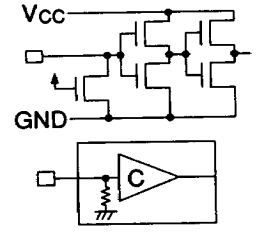
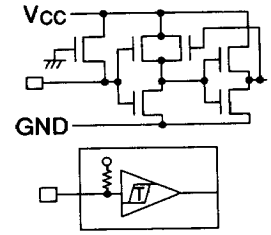
I/O Buffers

Macro Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Delay Input Name	Delay Output Name	t_{plh} (ns) t_{olh}	t_{plh} (ns) K_{lh}	t_{phl} (ns) t_{ohl}	t_{phl} (ns) K_{hl}
TTL-level input buffer IT		—	—		D1			0.65	0.27	1.65	0.17
CMOS-level input buffer IC		—	—		D1			0.93	0.27	0.83	0.22
Schmitt-trigger TTL-level input buffer ITS		—	—		D1			2.80	0.17	2.50	0.27
Schmitt-trigger CMOS-level input buffer ICS		—	—		D1			2.47	0.28	2.20	0.30
OSC in (2–20 MHz) XIN		—	—		D1			3.10	0.80	3.20	0.80

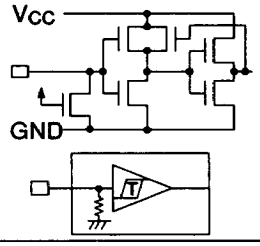
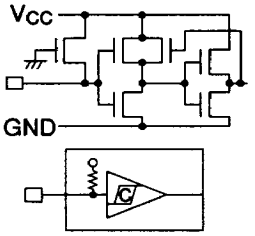
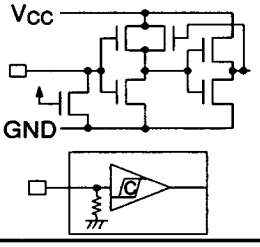
I/O Buffers (cont)

Macro						Delay					
								t_{plh} (ns)		t_{phl} (ns)	
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Input Name	Output Name	t_{olh}	K_{lh}	t_{ohl}	K_{hl}
OSC out (2–20 MHz) XOUT		—	—		D1			4.00	1.20	2.50	0.90
OSC in XIN1		—	—		D1			3.10	40.0	3.20	40.0
OSC out XOUT1		—	—		D1			4.00	1.20	2.50	0.90
TTL-level input buffer with pull-up ITU		—	—		D2			0.65	0.27	1.65	0.17

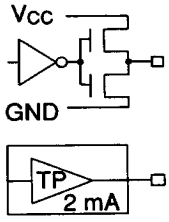
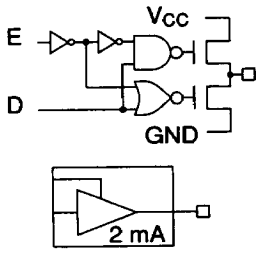
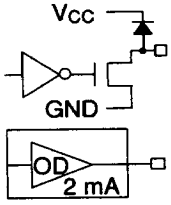
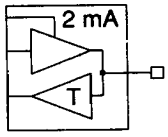
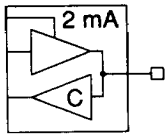
I/O Buffers (cont)

Macro Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Delay Input Name	Delay Output Name	t_{plh} (ns) t_{olh}	t_{plh} (ns) K_{lh}	t_{phl} (ns) t_{ohl}	t_{phl} (ns) K_{hl}
TTL-level input buffer with pull-down ITD		—	—		D2			0.65	0.27	1.65	0.17
CMOS-level input buffer with pull-up ICU		—	—		D2			0.93	0.27	0.83	0.22
CMOS-level input buffer with pull-down ICD		—	—		D2			0.93	0.27	0.83	0.22
Schmitt-trigger TTL-level input buffer with pull-up ITSU		—	—		D2			2.80	0.17	2.50	0.27

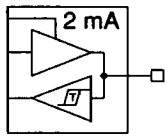
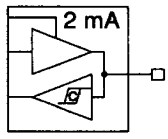
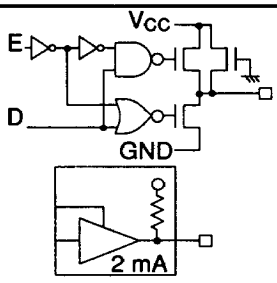
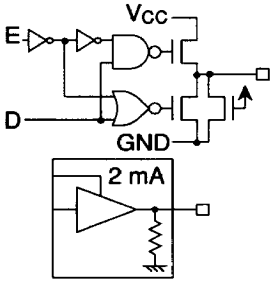
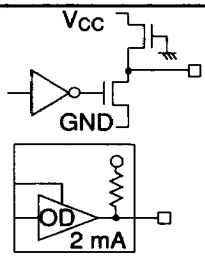
I/O Buffers (cont)

Macro						Delay					
								t_{plh} (ns)		t_{phl} (ns)	
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Input Name	Output Name	t_{olh}	K_{lh}	t_{ohl}	K_{hl}
Schmitt-trigger TTL-level input buffer with pull-down ITSD		—	—		D2			2.80	0.17	2.50	0.27
Schmitt-trigger CMOS-level input buffer with pull-up ICSU		—	—		D2			2.47	0.28	2.20	0.30
Schmitt-trigger CMOS-level input buffer with pull-down ICSD		—	—		D2			2.47	0.28	2.20	0.30

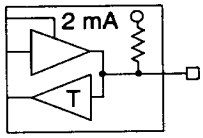
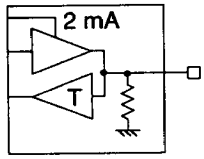
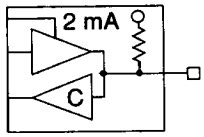
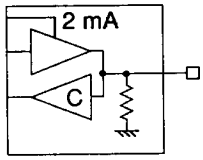
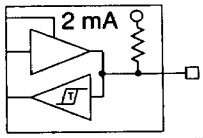
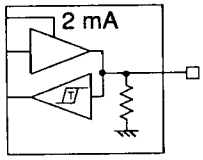
I/O Buffers (I_{OL} = 2 mA)

Macro: Function and Macro Name	Macro: Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Sym-bol No.	Delay: In-put Name	Delay: Out-put Name	Delay: t_{plh} (ns) t_{olh}	Delay: t_{plh} (ns) K_{lh}	Delay: t_{phl} (ns) t_{ohl}	Delay: t_{phl} (ns) K_{hl}
Totem-pole output OT1		—	5		D1			1.20	0.14	1.00	0.18
Three-state output OZ1		—	5 6		D1	E D		1.40 1.20	0.14	1.20 1.00	0.18
Open-drain output ODN1		—	5		D1			1.20 (t_{olz})	— (K_{lz})	1.00 (t_{ozl})	0.18 (K_{zl})
TTL-level I/O buffer ITO1	Output circuit: See OZ1 Input circuit: See IT 	—	5 6		D2	E D		1.40 1.20 0.65	0.14 0.27	1.20 1.00 1.65	0.18 0.17
CMOS-level I/O buffer ICO1	Output circuit: See OZ1 Input circuit: See IC 	—	5 6		D2	E D		1.40 1.20 0.93	0.14 0.27	1.20 1.00 0.83	0.18 0.22

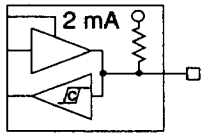
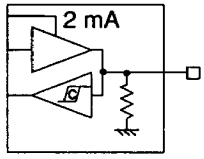
I/O Buffers (I_{OL} = 2 mA) (cont)

Macro: Function and Macro Name	Macro: Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Sym-bol No.	Delay: In-put Name	Delay: Out-put Name	Delay: t_{plh} (ns) t_{olh}	Delay: t_{plh} (ns) K_{lh}	Delay: t_{phl} (ns) t_{ohl}	Delay: t_{phl} (ns) K_{hl}
TTL-level I/O buffer with Schmitt-trigger ITSO1	Output circuit: See OZ1 Input circuit: See ITS 	—	5 6		D2	E D		1.40 1.20 2.80	0.14 0.17	1.20 1.00 2.50	0.18 0.27
CMOS-level I/O buffer with Schmitt-trigger ICSO1	Output circuit: See OZ1 Input circuit: See ICS 	—	5 6		D2	E D		1.40 1.20 2.47	0.14 0.28	1.20 1.00 2.20	0.18 0.30
Three-state output buffer with pull-up OZ1U		—	5 6		D2	E D		1.40 1.20	0.14 	1.20 1.00	0.18
Three-state output buffer with pull-down OZ1D		—	5 6		D2	E D		1.40 1.20	0.14 	1.20 1.00	0.18
Open-drain output buffer with pull-up ODN1U			5		D2			1.20 (t_{olz})	— (K_{lz})	1.00 (t_{ozl})	0.18 (K_{zl})

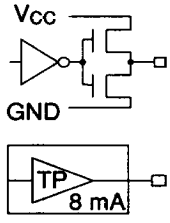
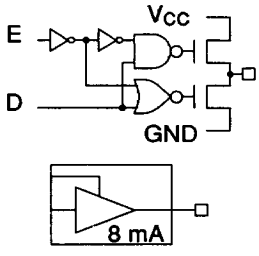
I/O Buffers (I_{OL} = 2 mA) (cont)

Macro: Function and Macro Name	Macro: Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{plh} (ns) t_{olh}	Delay: t_{plh} (ns) K_{lh}	Delay: t_{phl} (ns) t_{ohl}	Delay: t_{phl} (ns) K_{hl}
TTL-level I/O buffer with pull-up ITO1U	Output circuit: See OZ1U Input circuit: See IT 	—	5 6		D2	E D		1.40 1.20 0.65	0.14 0.27	1.20 1.00 1.65	0.18 0.17
TTL-level I/O buffer with pull-down ITO1D	Output circuit: See OZ1D Input circuit: See IT 	—	5 6		D2	E D		1.40 1.20 0.65	0.14 0.27	1.20 1.00 1.65	0.18 0.17
CMOS-level I/O buffer with pull-up ICO1U	Output circuit: See OZ1U Input circuit: See IC 	—	5 6		D2	E D		1.40 1.20 0.93	0.14 0.27	1.20 1.00 0.83	0.18 0.22
CMOS-level I/O buffer with pull-down ICO1D	Output circuit: See OZ1D Input circuit: See IC 	—	5 6		D2	E D		1.40 1.20 0.93	0.14 0.27	1.20 1.00 0.83	0.18 0.22
TTL-level Schmitt-trigger I/O with pull-up ITSO1U	Output circuit: See OZ1U Input circuit: See ITS 	—	5 6		D2	E D		1.40 1.20 2.80	0.14 0.17	1.20 1.00 2.50	0.18 0.27
TTL-level Schmitt-trigger I/O with pull-down ITSO1D	Output circuit: See OZ1D Input circuit: See ITS 	—	5 6		D2	E D		1.40 1.20 2.80	0.14 0.17	1.20 1.00 2.50	0.18 0.27

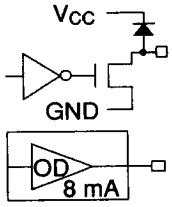
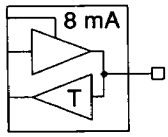
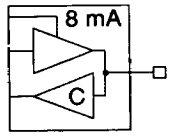
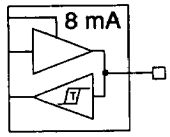
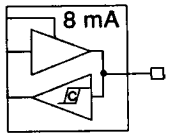
I/O Buffers (I_{OL} = 2 mA) (cont)

Macro: Function and Macro Name	Macro: Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{plh} (ns) t_{olh}	Delay: t_{plh} (ns) K_{lh}	Delay: t_{phl} (ns) t_{ohl}	Delay: t_{phl} (ns) K_{hl}
CMOS-level Schmitt-trigger I/O with pull-up ICSO1U	Output circuit: See OZ1U Input circuit: See ICS 	—	5 6		D2	E D		1.40 1.20 2.47	0.14 0.28	1.20 1.00 2.20	0.18 0.30
CMOS-level Schmitt-trigger I/O with pull-down ICSO1D	Output circuit: See OZ1D Input circuit: See ICS 	—	5 6		D2	E D		1.40 1.20 2.47	0.14 0.28	1.20 1.00 2.20	0.18 0.30

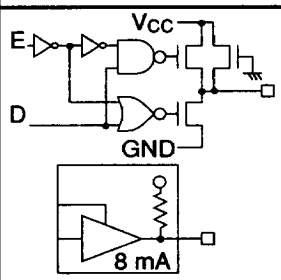
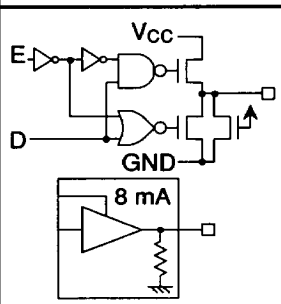
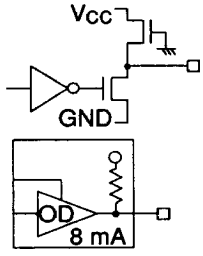
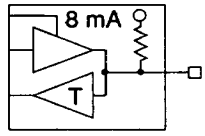
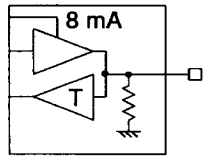
I/O Buffers (I_{OL} = 8 mA)

Macro: Function and Macro Name	Macro: Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{plh} (ns) t_{olh}	Delay: t_{plh} (ns) K_{lh}	Delay: t_{phl} (ns) t_{ohl}	Delay: t_{phl} (ns) K_{hl}
Totem-pole output OT3		—	5		D1			2.00	0.04	2.20	0.06
Three-state output OZ3		—	5 6		D1	E D		2.20 2.00	0.04 	2.40 2.20	0.06

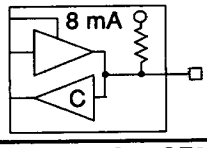
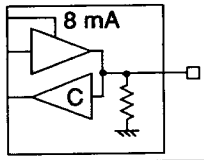
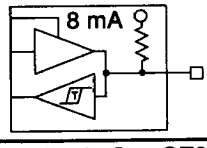
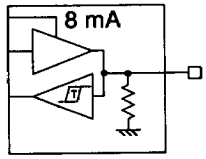
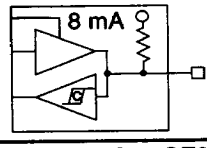
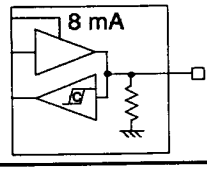
I/O Buffers (I_{OL} = 8 mA) (cont)

Macro: Function and Macro Name	Macro: Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Sym-bol No.	Delay: In-put Name	Delay: Out-put Name	Delay: t_{plh} (ns) t_{olh}	Delay: t_{plh} (ns) K_{lh}	Delay: t_{phl} (ns) t_{ohl}	Delay: t_{phl} (ns) K_{hl}
Open-drain output ODN3		—	5		D1			2.00 (t_{olz})	— (K_{lz})	2.20 (t_{ozl})	0.06 (K_{zl})
TTL-level I/O buffer ITO3	Output circuit: See OZ3 Input circuit: See IT 	—	5 6		D2	E D		2.20 2.00 0.65	0.04 0.27	2.40 2.20 1.65	0.06 0.17
CMOS-level I/O buffer ICO3	Output circuit: See OZ3 Input circuit: See IC 	—	5 6		D2	E D		2.20 2.00 0.93	0.04 0.27	2.40 2.20 0.83	0.06 0.22
TTL-level I/O buffer with Schmitt-trigger ITSO3	Output circuit: See OZ3 Input circuit: See ITS 	—	5 6		D2	E D		2.20 2.00 2.80	0.04 0.17	2.40 2.20 2.50	0.06 0.27
CMOS-level I/O buffer with Schmitt-trigger ICSO3	Output circuit: See OZ3 Input circuit: See ICS 	—	5 6		D2	E D		2.20 2.00 2.47	0.04 0.28	2.40 2.20 2.20	0.06 0.30

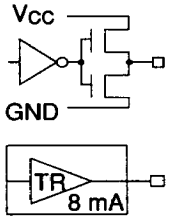
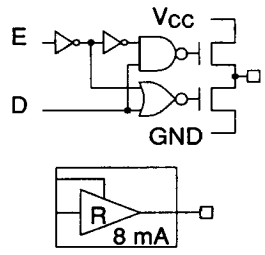
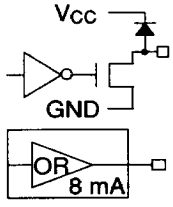
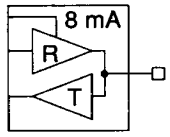
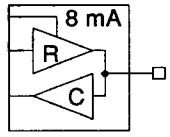
I/O Buffers (I_{OL} = 8 mA) (cont)

Macro: Function and Macro Name	Macro: Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{plh} (ns) t_{olh}	Delay: t_{plh} (ns) K_{lh}	Delay: t_{phl} (ns) t_{ohl}	Delay: t_{phl} (ns) K_{hl}
Three-state output buffer with pull-up OZ3U		—	5 6		D2	E D		2.20 2.00	0.04	2.40 2.20	0.06
Three-state output buffer with pull-down OZ3D		—	5 6		D2	E D		2.20 2.00	0.04	2.40 2.20	0.06
Open-drain output buffer with pull-up ODN3U			5		D2	E		2.00 (t_{olz})	— (K_{lz})	2.20 (t_{ozl})	0.06 (K_{zl})
TTL-level I/O buffer with pull-up ITO3U	Output circuit: See OZ3U Input circuit: See IT 	—	5 6		D2	E D		2.20 2.00 0.65	0.04 0.27	2.40 2.20 1.65	0.06 0.17
TTL-level I/O buffer with pull-down ITO3D	Output circuit: See OZ3D Input circuit: See IT 	—	5 6		D2	E D		2.20 2.00 0.65	0.04 0.27	2.40 2.20 1.65	0.06 0.17

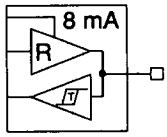
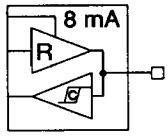
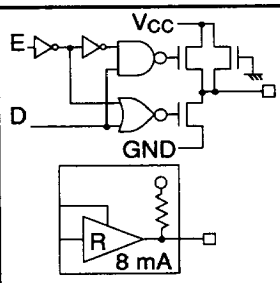
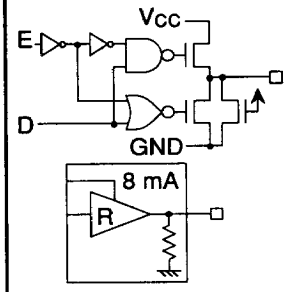
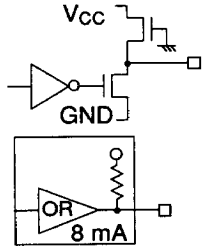
I/O Buffers (I_{OL} = 8 mA) (cont)

Macro: Function and Macro Name	Macro: Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{plh} (ns) t_{olh}	Delay: t_{plh} (ns) K_{lh}	Delay: t_{phl} (ns) t_{ohl}	Delay: t_{phl} (ns) K_{hl}
CMOS-level I/O buffer with pull-up ICO3U	Output circuit: See OZ3U Input circuit: See IC 	—	5 6		D2	E D		2.20 2.00 0.93	0.04 0.27	2.40 2.20 0.83	0.06 0.22
CMOS-level I/O buffer with pull-down ICO3D	Output circuit: See OZ3D Input circuit: See IC 	—	5 6		D2	E D		2.20 2.00 0.93	0.04 0.27	2.40 2.20 0.83	0.06 0.22
TTL-level Schmitt-trigger I/O with pull-up ITSO3U	Output circuit: See OZ3U Input circuit: See ITS 	—	5 6		D2	E D		2.20 2.00 2.80	0.04 0.17	2.40 2.20 2.50	0.06 0.27
TTL-level Schmitt-trigger I/O with pull-down ITSO3D	Output circuit: See OZ3D Input circuit: See ITS 	—	5 6		D2	E D		2.20 2.00 2.80	0.04 0.17	2.40 2.20 2.50	0.06 0.27
CMOS-level Schmitt-trigger I/O with pull-up ICSO3U	Output circuit: See OZ3U Input circuit: See ICS 	—	5 6		D2	E D		2.20 2.00 2.47	0.04 0.28	2.40 2.20 2.20	0.06 0.30
CMOS-level Schmitt-trigger I/O with pull-down ICSO3D	Output circuit: See OZ3D Input circuit: See ICS 	—	5 6		D2	E D		2.20 2.00 2.47	0.04 0.28	2.40 2.20 2.20	0.06 0.30

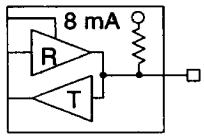
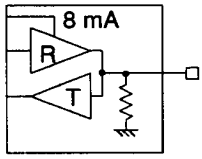
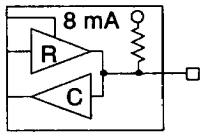
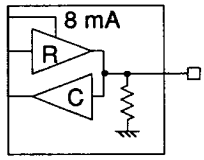
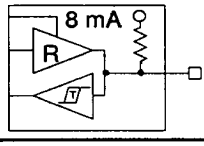
GND Noise Reduction Buffers (I_{OL} = 8 mA)

Macro: Function and Macro Name	Macro: Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{plh} (ns) t_{olh}	Delay: t_{plh} (ns) K_{lh}	Delay: t_{phl} (ns) t_{ohl}	Delay: t_{phl} (ns) K_{hl}
Totem-pole output OT3R		—	2		D1			5.90	0.05	8.70	0.07
Three-state output OZ3R		—	3 3		D1	E D		6.10 5.90	0.05	8.90 8.70	0.07
Open-drain output ODN3R		—	2		D1			5.90 (t_{olz})	— (K_{lz})	8.70 (t_{ozl})	0.07 (K_{zl})
TTL-level I/O buffer ITO3R	Output circuit: See OZ3 Input circuit: See IT 	—	3 3		D2	E D		6.10 5.90 0.65	0.05 0.27	8.90 8.70 1.65	0.07 0.17
CMOS-level I/O buffer ICO3R	Output circuit: See OZ3 Input circuit: See IC 	—	3 3		D2	E D		6.10 5.90 0.93	0.05 0.27	8.90 8.70 0.83	0.07 0.22

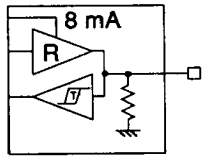
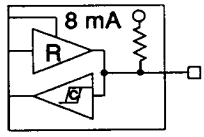
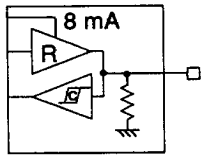
GND Noise Reduction Buffers (I_{OL} = 8 mA) (cont)

Macro		Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Delay					
								t_{plh} (ns)		t_{phl} (ns)	
Function and Macro Name	Equiv. Circuit and Symbol					In-put Name	Out-put Name	t_{olh}	K_{lh}	t_{ohl}	K_{hl}
TTL-level I/O buffer with Schmitt-trigger ITSO3R	Output circuit: See OZ3R Input circuit: See ITS 	—	3 3		D2	E D		6.10 5.90 2.80	0.05 0.17	8.90 8.70 2.50	0.07 0.27
CMOS-level I/O buffer with Schmitt-trigger ICSO3R	Output circuit: See OZ3R Input circuit: See ICS 	—	3 3		D2	E D		6.10 5.90 2.47	0.05 0.28	8.90 8.70 2.20	0.07 0.30
Three-state output buffer with pull-up OZ3RU		—	3 3		D2	E D		6.10 5.90	0.05 	8.90 8.70	0.07
Three-state output buffer with pull-down OZ3RD		—	3 3		D2	E D		6.10 5.90	0.05 	8.90 8.70	0.07
Open-drain output buffer with pull-up ODN3RU			2		D2			5.90 (t_{olz})	— (K_{lz})	8.70 (t_{ozl})	0.07 (K_{zl})

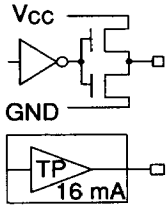
GND Noise Reduction Buffers (I_{OL} = 8 mA) (cont)

Macro						Delay					
								t_{plh} (ns)		t_{phl} (ns)	
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Sym-bol No.	In-put Name	Out-put Name	t_{olh}	K_{lh}	t_{ohl}	K_{hl}
TTL-level I/O buffer with pull-up ITO3RU	Output circuit: See OZ3RU Input circuit: See IT 	—	3 3		D2	E D		6.10 5.90 0.65	0.05 0.27	8.90 8.70 1.65	0.07 0.17
TTL-level I/O buffer with pull-down ITO3RD	Output circuit: See OZ3RD Input circuit: See IT 	—	3 3		D2	E D		6.10 5.90 0.65	0.05 0.27	8.90 8.70 1.65	0.07 0.17
CMOS-level I/O buffer with pull-up ICO3RU	Output circuit: See OZ3RU Input circuit: See IC 	—	3 3		D2	E D		6.10 5.90 0.93	0.05 0.27	8.90 8.70 0.83	0.07 0.22
CMOS-level I/O buffer with pull-down ICO3RD	Output circuit: See OZ3RD Input circuit: See IC 	—	3 3		D2	E D		6.10 5.90 0.93	0.05 0.27	8.90 8.70 0.83	0.07 0.22
TTL-level Schmitt-trigger I/O with pull-up ITSO3RU	Output circuit: See OZ3RU Input circuit: See ITS 	—	3 3		D2	E D		6.10 5.90 2.80	0.05 0.17	8.90 8.70 2.50	0.07 0.27

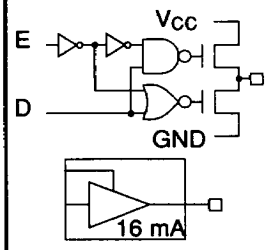
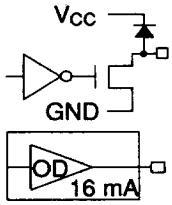
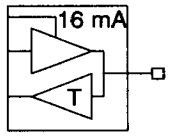
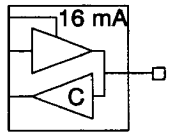
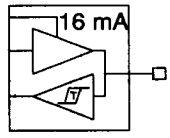
GND Noise Reduction Buffers (I_{OL} = 8 mA) (cont)

Macro: Function and Macro Name	Macro: Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{plh} (ns) t_{olh}	Delay: t_{plh} (ns) K_{lh}	Delay: t_{phl} (ns) t_{ohl}	Delay: t_{phl} (ns) K_{hl}
TTL-level Schmitt-trigger I/O with pull-down ITSO3RD	Output circuit: See OZ3D Input circuit: See ITS 	—	3 3		D2	E D		6.10 5.90 2.80	0.05 0.17	8.90 8.70 2.50	0.07 0.27
CMOS-level Schmitt-trigger I/O with pull-up ICSO3RU	Output circuit: See OZ3U Input circuit: See ICS 	—	3 3		D2	E D		6.10 5.90 2.47	0.05 0.28	8.90 8.70 2.20	0.07 0.30
CMOS-level Schmitt-trigger I/O with pull-down ICSO3RD	Output circuit: See OZ3D Input circuit: See ICS 	—	3 3		D2	E D		6.10 5.90 2.47	0.05 0.28	8.90 8.70 2.20	0.07 0.30

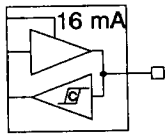
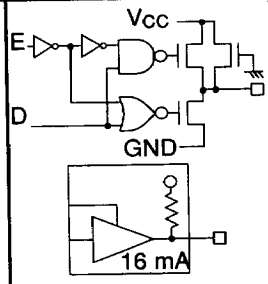
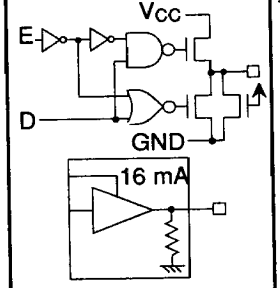
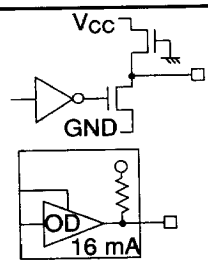
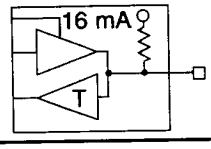
I/O Buffers (I_{OL} = 16 mA)

Macro: Function and Macro Name	Macro: Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{plh} (ns) t_{olh}	Delay: t_{plh} (ns) K_{lh}	Delay: t_{phl} (ns) t_{ohl}	Delay: t_{phl} (ns) K_{hl}
Totem-pole output OT6		—	5		D1			2.00	0.025	2.40	0.028

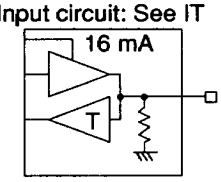
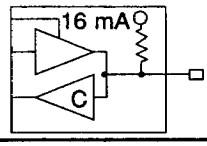
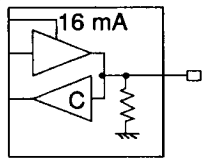
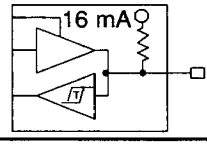
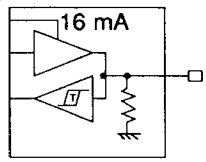
I/O Buffers (I_{OL} = 16 mA) (cont)

Macro: Function and Macro Name	Macro: Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{plh} (ns) t_{olh}	Delay: t_{plh} (ns) K_{lh}	Delay: t_{phl} (ns) t_{ohl}	Delay: t_{phl} (ns) K_{hl}
Three-state output buffer OZ6		—	5 6		D1	E D		2.20 2.00	0.025	2.60 2.40	0.028
Open-drain output ODN6		—	5		D1			2.00 (t_{olz})	— (K_{lz})	2.40 (t_{ozl})	0.028 (K_{zl})
TTL-level I/O buffer ITO6	Output circuit: See OZ6 Input circuit: See IT 	—	5 6		D2	E D		2.20 2.00 0.65	0.025 0.27	2.60 2.40 1.65	0.028 0.17
CMOS-level I/O buffer ICO6	Output circuit: See OZ6 Input circuit: See IC 	—	5 6		D2	E D		2.20 2.00 0.93	0.025 0.27	2.60 2.40 0.83	0.028 0.22
TTL-level I/O buffer with Schmitt-trigger ITSO6	Output circuit: See OZ6 Input circuit: See ITS 	—	5 6		D2	E D		2.20 2.00 2.80	0.025 0.17	2.60 2.40 2.50	0.028 0.27

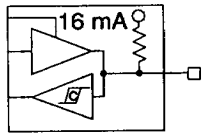
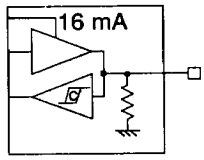
I/O Buffers (I_{OL} = 16 mA) (cont)

Macro: Function and Macro Name	Macro: Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{plh} (ns) t_{olh}	Delay: t_{plh} (ns) K_{lh}	Delay: t_{phl} (ns) t_{ohl}	Delay: t_{phl} (ns) K_{hl}
CMOS-level I/O buffer with Schmitt-trigger ICSO6	Output circuit: See OZ6 Input circuit: See ICS 	—	5 6		D2	E D		2.20 2.00 2.47	0.025 0.28	2.60 2.40 2.20	0.028 0.30
Three-state output buffer with pull-up OZ6U		—	5 6		D2	E D		2.20 2.00	0.025 	2.60 2.40	0.028
Three-state output buffer with pull-down OZ6D		—	5 6		D2	E D		2.20 2.00	0.025 	2.60 2.40	0.028
Open-drain output buffer with pull-up ODN6U			5		D2			2.00 (t_{olz})	— (K_{lz})	2.40 (t_{ozl})	0.028 (K_{zl})
TTL-level I/O buffer with pull-up ITO6U	Output circuit: See OZ6U Input circuit: See IT 	—	5 6		D2	E D		2.20 2.00 0.65	0.025 0.27	2.60 2.40 1.65	0.028 0.17

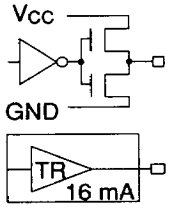
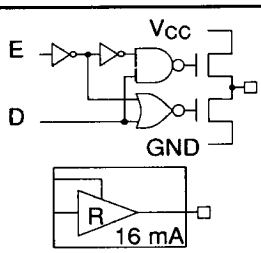
I/O Buffers (I_{OL} = 16 mA) (cont)

Macro: Function and Macro Name	Macro: Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{plh} (ns) t_{olh}	Delay: t_{plh} (ns) K_{lh}	Delay: t_{phl} (ns) t_{ohl}	Delay: t_{phl} (ns) K_{hl}
TTL- level I/O buffer with pull-down ITO6D	Output circuit: See OZ6D Input circuit: See IT 	—	5 6		D2	E D		2.20 2.00 0.65	0.025 0.27	2.60 2.40 1.65	0.028 0.17
CMOS-level I/O buffer with pull-up ICO6U	Output circuit: See OZ6U Input circuit: See IC 	—	5 6		D2	E D		2.20 2.00 0.93	0.025 0.27	2.60 2.40 0.83	0.028 0.22
CMOS-level I/O buffer with pull-down ICO6D	Output circuit: See OZ6D Input circuit: See IC 	—	5 6		D2	E D		2.20 2.00 0.93	0.025 0.27	2.60 2.40 0.83	0.028 0.22
TTL-level Schmitt-trigger I/O with pull-up ITSO6U	Output circuit: See OZ6U Input circuit: See ITS 	—	5 6		D2	E D		2.20 2.00 2.80	0.025 0.17	2.60 2.40 2.50	0.028 0.27
TTL-level Schmitt-trigger I/O with pull-down ITSO6D	Output circuit: See OZ6D Input circuit: See ITS 	—	5 6		D2	E D		2.20 2.00 2.80	0.025 0.17	2.60 2.40 2.50	0.028 0.27

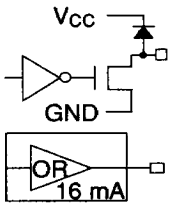
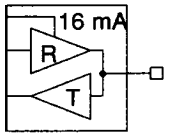
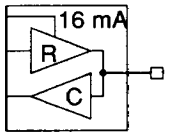
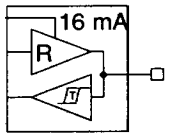
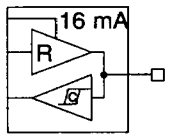
I/O Buffers (I_{OL} = 16 mA) (cont)

Macro: Function and Macro Name	Macro: Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{plh} (ns) t_{olh}	Delay: t_{plh} (ns) K_{lh}	Delay: t_{phl} (ns) t_{ohl}	Delay: t_{phl} (ns) K_{hl}
CMOS-level Schmitt-trigger I/O with pull-up ICSO6U	Output circuit: See OZ6U Input circuit: See ITS 	—	5 6		D2	E D		2.20 2.00 2.47	0.025 0.28	2.60 2.40 2.20	0.028 0.30
CMOS-level Schmitt-trigger I/O with pull-down ICSO6D	Output circuit: See OZ6D Input circuit: See ITS 	—	5 6		D2	E D		2.20 2.00 2.47	0.025 0.28	2.60 2.40 2.20	0.028 0.30

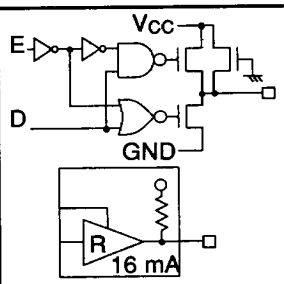
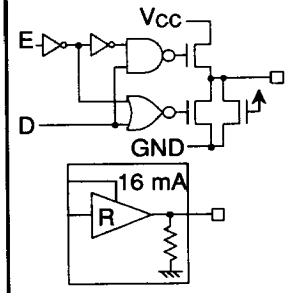
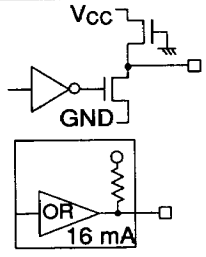
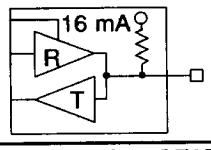
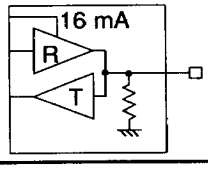
GND Noise Reduction Buffers (I_{OL} = 16 mA)

Macro: Function and Macro Name	Macro: Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{plh} (ns) t_{olh}	Delay: t_{plh} (ns) K_{lh}	Delay: t_{phl} (ns) t_{ohl}	Delay: t_{phl} (ns) K_{hl}
Totem-pole output OT6R		—	2		D1			9.80	0.04	10.8	0.06
Three-state output OZ6R		—	3 3		D1	E D		10.0 9.80	0.04	11.0 10.8	0.06

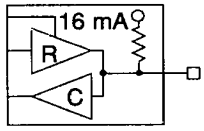
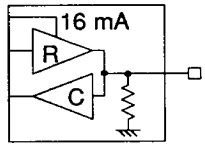
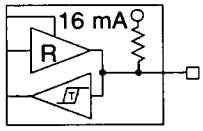
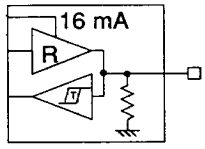
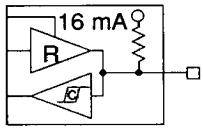
GND Noise Reduction Buffers (I_{OL} = 16 mA) (cont)

Macro		Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Delay					
								t_{plh} (ns)		t_{phl} (ns)	
Function and Macro Name	Equiv. Circuit and Symbol					In-put Name	Out-put Name	t_{olh}	K_{lh}	t_{ohl}	K_{hl}
Open-drain output ODN6R		—	2		D1			9.80 (t_{olz})	— (K_{lz})	10.8 (t_{ozl})	0.06 (K_{zl})
TTL-level I/O buffer ITO6R	Output circuit: See OZ6 Input circuit: See IT 	—	3 3		D2	E D		10.0 9.80 0.65	0.04 0.27	11.0 10.8 1.65	0.06 0.17
CMOS-level I/O buffer ICO6R	Output circuit: See OZ6 Input circuit: See IC 	—	3 3		D2	E D		10.0 9.80 0.93	0.04 0.27	11.0 10.8 0.83	0.06 0.22
TTL-level I/O buffer with Schmitt-trigger ITSO6R	Output circuit: See OZ6 Input circuit: See ITS 	—	3 3		D2	E D		10.0 9.80 2.80	0.04 0.17	11.0 10.8 2.50	0.06 0.27
CMOS-level I/O buffer with Schmitt-trigger ICSO6R	Output circuit: See OZ6 Input circuit: See ICS 	—	3 3		D2	E D		10.0 9.80 2.47	0.04 0.28	11.0 10.8 2.20	0.06 0.30

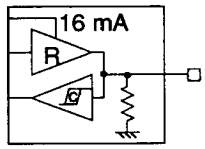
GND Noise Reduction Buffers (I_{OL} = 16 mA) (cont)

Macro: Function and Macro Name	Macro: Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{plh} (ns) t_{olh}	Delay: t_{plh} (ns) K_{lh}	Delay: t_{phl} (ns) t_{ohl}	Delay: t_{phl} (ns) K_{hl}
Three-state output buffer with pull-up OZ6RU		—	3 3		D2	E D		10.0 9.80	0.04	11.0 10.8	0.06
Three-state output buffer with pull-down OZ6RD		—	3 3		D2	E D		10.0 9.80	0.04	11.0 10.8	0.06
Open-drain output buffer with pull-up ODN6RU			2		D2			9.80 (t_{olz})	— (K_{lz})	10.8 (t_{ozl})	0.06 (K_{zl})
TTL-level I/O buffer with pull-up ITO6RU	Output circuit: See OZ6RU Input circuit: See IT 	—	3 3		D2	E D		10.0 9.80 0.65	0.04 0.27	11.0 10.8 1.65	0.06 0.17
TTL-level I/O buffer with pull-down ITO6RD	Output circuit: See OZ6RD Input circuit: See IT 	—	3 3		D2	E D		10.0 9.80 0.65	0.04 0.27	11.0 10.8 1.65	0.06 0.17

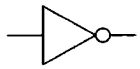
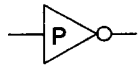
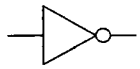
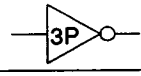
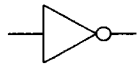
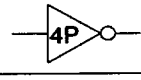
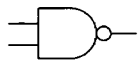
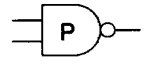
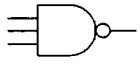
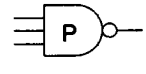
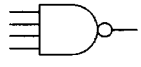
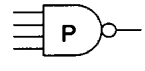
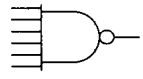
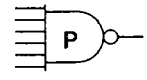
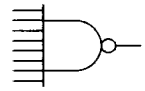
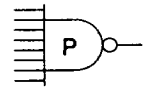
GND Noise Reduction Buffers (I_{OL} = 16 mA) (cont)

Macro						Delay					
								t_{plh} (ns)		t_{phl} (ns)	
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Sym-bol No.	In-put Name	Out-put Name	t_{olh}	K_{lh}	t_{ohl}	K_{hl}
CMOS-level I/O buffer with pull-up ICO6RU	Output circuit: See OZ6RU Input circuit: See IC 	—	3 3		D2	E D		10.0 9.80 0.93	0.04 0.27	11.0 10.8 0.83	0.06 0.22
CMOS-level I/O buffer with pull-down ICO6RD	Output circuit: See OZ6RD Input circuit: See IC 	—	3 3		D2	E D		10.0 9.80 0.93	0.04 0.27	11.0 10.8 0.83	0.06 0.22
TTL-level Schmitt-trigger I/O with pull-up ITSO6RU	Output circuit: See OZ6RU Input circuit: See ITS 	—	3 3		D2	E D		10.0 9.80 2.80	0.04 0.17	11.0 10.8 2.50	0.06 0.27
TTL-level Schmitt-trigger I/O with pull-down ITSO6RD	Output circuit: See OZ6RD Input circuit: See ITS 	—	3 3		D2	E D		10.0 9.80 2.80	0.04 0.17	11.0 10.8 2.50	0.06 0.27
CMOS-level Schmitt-trigger I/O with pull-up ICSO6RU	Output circuit: See OZ6RU Input circuit: See ITS 	—	3 3		D2	E D		10.0 9.80 2.47	0.04 0.28	11.0 10.8 2.20	0.06 0.30

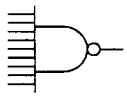
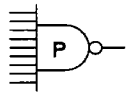
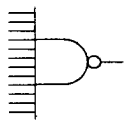
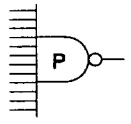
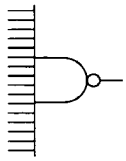
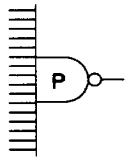
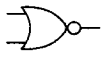
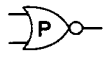
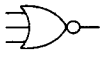
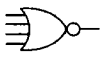
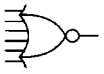
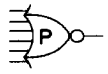
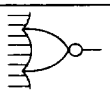
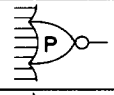
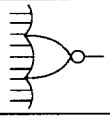
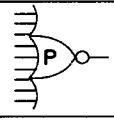
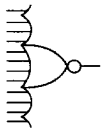
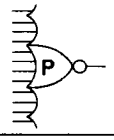
GND Noise Reduction Buffers (I_{OL} = 16 mA) (cont)

Macro						Delay					
								t_{plh} (ns)		t_{phl} (ns)	
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	In-put Name	Out-put Name	t_{olh}	K_{lh}	t_{ohl}	K_{hl}
CMOS-level Schmitt-trigger I/O with pull-down ICSO6RD	Output circuit: See OZ6RD Input circuit: See ITS 	—	3 3		D2	E D		10.0 9.80	0.04	11.0 10.8	0.06
								2.47	0.28	2.20	0.30

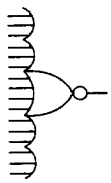
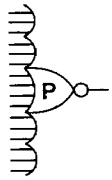
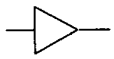
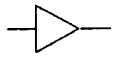
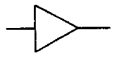
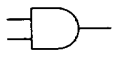
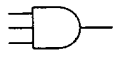
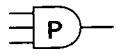
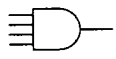
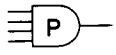
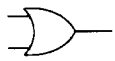
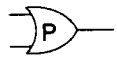
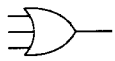
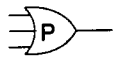
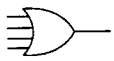
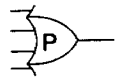
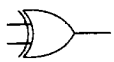
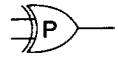
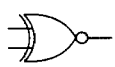
Power Gates

Macro						Delay			
						t_{plh} (ns)		t_{phl} (ns)	
Function and Macro Name	Equivalent Circuit	Equiv. Gate Count	LV	Clamp Level when Open	Symbol	t_{olh}	K_{lh}	t_{ohl}	K_{hl}
Power inverter NAP1		1	2	@		0.18	0.30	0.30	0.30
Power inverter NA3P		2	3	@		0.91	0.24	0.31	0.24
Power inverter NA4P		2	4	@		0.20	0.18	0.32	0.18
2-input power NAND NAP2		2	2	@		0.16	0.30	0.20	0.42
3-input power NAND NAP3		3	2	@		0.18	0.30	0.22	0.58
4-input power NAND NAP4		4	2	@		0.20	0.30	0.25	0.70
6-input power NAND NAP6		5	1	@		0.48	0.30	0.85	0.30
8-input power NAND NAP8		7	1	@		0.52	0.30	0.95	0.30

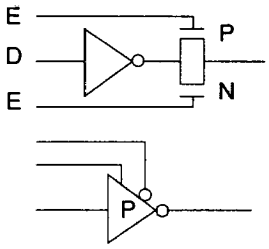
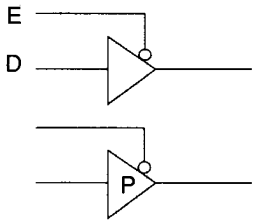
Power Gates (cont)

Macro						Delay			
						t_{plh} (ns)		t_{phl} (ns)	
Function and Macro Name	Equivalent Circuit	Equiv. Gate Count	LV	Clamp Level when Open	Symbol	t_{olh}	K_{lh}	t_{ohl}	K_{hl}
9-input power NAND NAP9		7	1	@		0.52	0.30	0.95	0.30
12-input power NAND NAP-12		9	1	@		0.52	0.30	1.28	0.30
16-input power NAND NAP16		13	1	@		0.52	0.30	0.88	0.42
2-input NOR NRP2		2	2	#		0.28	0.50	0.24	0.30
3-input NOR NRP3		3	2	#		0.30	0.74	0.26	0.30
4-input NOR NRP4		4	2	#		0.32	0.98	0.28	0.30
6-input NOR NRP6		5	1	#		0.74	0.30	0.55	0.30
8-input NOR NRP8		7	1	#		0.90	0.30	0.55	0.30
9-input NOR NRP9		7	1	#		0.90	0.30	0.55	0.30
12-input NOR NRP12		9	1	#		1.02	0.30	0.58	0.30

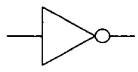
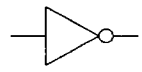
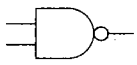
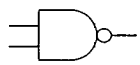
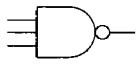
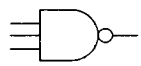
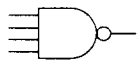
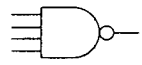
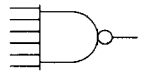
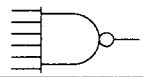
Power Gates (cont)

Macro						Delay			
						t_{plh} (ns)		t_{phl} (ns)	
Function and Macro Name	Equivalent Circuit	Equiv. Gate Count	LV	Clamp Level when Open	Symbol	t_{olh}	K_{lh}	t_{ohl}	K_{hl}
16-input NOR NRP16		13	1	#		1.00	0.50	0.62	0.30
Power buffer ANP		2	1	@		0.20	0.30	0.38	0.30
Power buffer AN3P		3	2	@		0.20	0.24	0.34	0.24
Power buffer AN4P		3	2	@		0.22	0.18	0.36	0.18
2-input power AND ANP2		2	1	@		0.46	0.30	0.38	0.30
3-input power AND ANP3		3	1	@		0.50	0.30	0.40	0.30
4-input power AND ANP4		3	1	@		0.58	0.30	0.42	0.30
2-input power OR ORP2		2	1	#		0.52	0.30	0.46	0.30
3-input power OR ORP3		3	1	#		0.57	0.30	0.52	0.30
4-input power OR ORP4		3	1	#		0.64	0.30	0.62	0.30
2-input power EOR EORP		4	2	#		0.37	0.50	0.50	0.42
2-input power ENOR ENRP		4	2	#		0.37	0.50	0.48	0.42

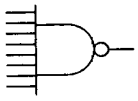
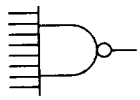
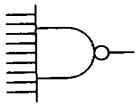
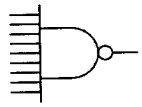
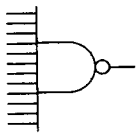
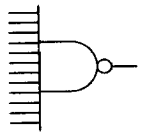
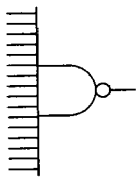
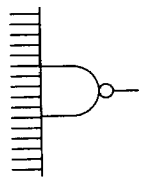
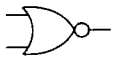
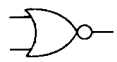
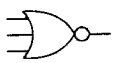
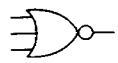
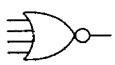
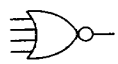
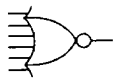
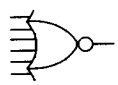
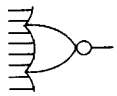
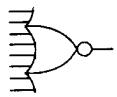
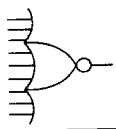
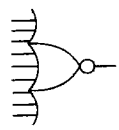
Three-State Power Gates

Macro					Delay					
							t_{plh} (ns)		t_{phl} (ns)	
Function and Macro Name	Equivalent Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	In-put Name	Out-put Name	t_{olh}	K_{lh}	t_{ohl}	K_{hl}
3-state power inverter (internal) NAZP		2	0.5 0.5 2	– – @	D E/E		0.58 0.28	0.40	0.44 0.40	0.38
3-state power buffer (internal) ANZP		4	2 2	# @	D E		0.50 0.60	0.30	0.40 0.50	0.30

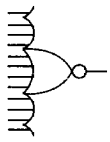
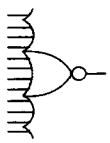
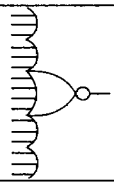
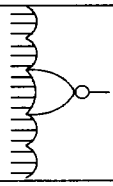
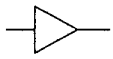
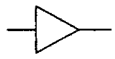
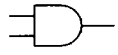
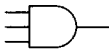
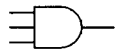
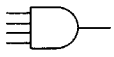
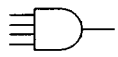
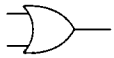
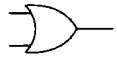
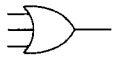
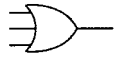
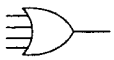
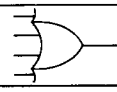
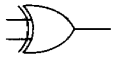
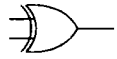
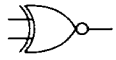
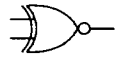
Gates

Macro						Delay			
						t_{plh} (ns)		t_{phl} (ns)	
Function and Macro Name	Equivalent Circuit	Equiv. Gate Count	LV	Clamp Level when Open	Symbol	t_{olh}	K_{lh}	t_{ohl}	K_{hl}
Inverter NA1		1	1	@		0.16	0.50	0.28	0.50
2-input NAND NA2		1	1	@		0.18	0.50	0.30	0.76
3-input NAND NA3		2	1	@		0.22	0.50	0.32	1.08
4-input NAND NA4		2	1	@		0.24	0.50	0.34	1.36
6-input NAND NA6		5	1	@		0.38	0.50	0.75	0.50

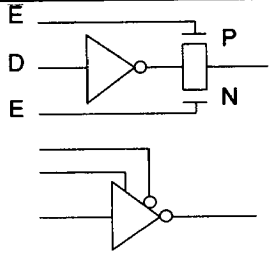
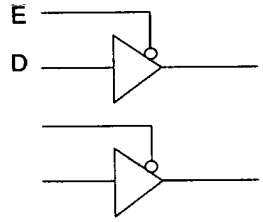
Gates (cont)

Macro						Delay			
						t_{plh} (ns)		t_{phl} (ns)	
Function and Macro Name	**Equivalent Circuit**	**Equiv. Gate Count**	**LV**	**Clamp Level when Open**	**Symbol**	t_{olh}	K_{lh}	t_{ohl}	K_{hl}
8-input NAND NA8		6	1	@		0.42	0.50	0.85	0.50
9-input NAND NA9		7	1	@		0.42	0.50	0.85	0.50
12-input NAND NA12		8	1	@		0.42	0.50	1.18	0.50
16-input NAND NA16		11	1	@		0.42	0.50	0.78	0,76
2-input NOR NR2		1	1	#		0.20	0.92	0.38	0.50
3-input NOR NR3		2	1	#		0.22	1.34	0.43	0.50
4-input NOR NR4		2	1	#		0.24	1.80	0.50	0.50
6-input NOR NR6		5	1	#		0.64	0.50	0.45	0.50
8-input NOR NR8		6	1	#		0.80	0.50	0.45	0.50
9-input NOR NR9		7	1	#		0.80	0.50	0.45	0.50

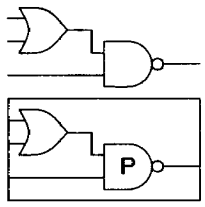
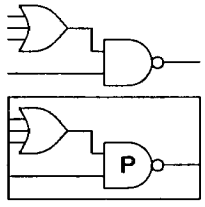
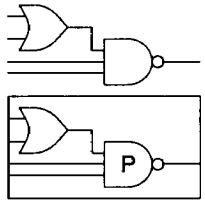
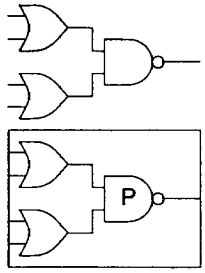
Gates (cont)

Macro						Delay			
						t_{plh} (ns)		t_{phl} (ns)	
Function and Macro Name	Equivalent Circuit	Equiv. Gate Count	LV	Clamp Level when Open	Symbol	t_{olh}	K_{lh}	t_{ohl}	K_{hl}
12-input NOR NR12		8	1	#		0.92	0.50	0.48	0.50
16-input NOR NR16		11	1	#		0.90	0.92	0.52	0.50
Buffer AN1		1	1	@		0.34	0.50	0.26	0.50
2-input AND AN2		2	1	@		0.36	0.50	0.28	0.50
3-input AND AN3		2	1	@		0.40	0.50	0.30	0.50
4-input AND AN4		3	1	@		0.48	0.50	0.32	0.50
2-input OR OR2		2	1	#		0.42	0.50	0.36	0.50
3-input OR OR3		2	1	#		0.47	0.50	0.42	0.50
4-input OR OR4		3	1	#		0.54	0.50	0.52	0.50
2-input EOR EOR		3	2	#		0.27	0.92	0.40	0.76
2-input ENOR ENR		3	2	#		0.27	0.92	0.38	0.76

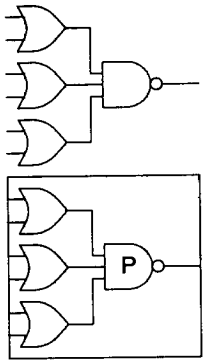
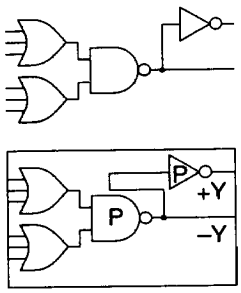
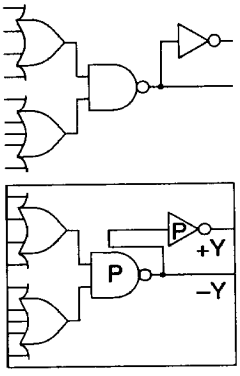
Three-State Gates

Macro					Delay					
							t_{plh} (ns)		t_{phl} (ns)	
Function and Macro Name	Equivalent Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	In-put Name	Out-put Name	t_{olh}	K_{lh}	t_{ohl}	K_{hl}
3-state inverter (internal) NAZ		1	0.5 0.5 1	@	D E/$\overline{E}$		0.48 0.18	0.65	0.34 0.30	0.62
3-state buffer (internal) ANZ		3	2 2	# @	D $\overline{E}$		0.40 0.50	0.50	0.30 0.40	0.50

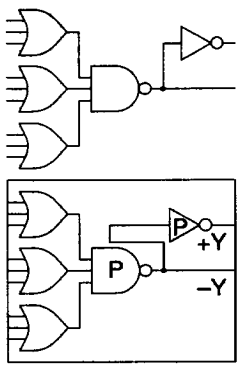
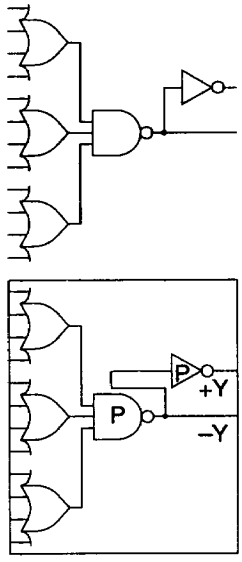
AND-NOR, OR-NAND Power Gates

Macro						Delay					
								t_{plh} (ns)		t_{phl} (ns)	
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Input Name	Output Name	t_{olh}	K_{lh}	t_{ohl}	K_{hl}
2-OR NAND NAR23P		3	2	# # @	A1	OR NAND		0.33 0.33	0.50	0.48 0.48	0.42
3-OR NAND NAR34P		4	2	# # # @	A2	OR NAND		0.40 0.40	0.74	0.48 0.48	0.42
2-OR 3-NAND NAR24P		4	2	# # @ @	A2	OR NAND		0.40 0.40	0.50	0.48 0.48	0.58
2-wide, 2-input OR-NAND NA2R2P		4	2	# # # #	A1			0.40	0.50	0.53	0.42

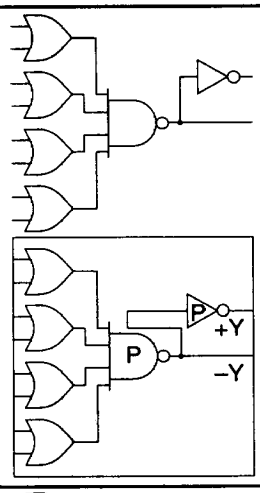
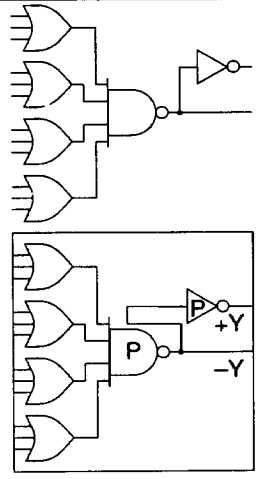
AND-NOR, OR-NAND Power Gates (cont)

Macro						Delay					
								t_{plh} (ns)		t_{phl} (ns)	
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Sym-bol No.	In-put Name	Out-put Name	t_{olh}	K_{lh}	t_{ohl}	K_{hl}
3-wide, 2-input OR-NAND NA3R2P		6	2	# # # # # #	A3			0.42	0.50	0.60	0.58
2-wide, 3-input OR-NAND NA2R3NP		7	2	# # # # # #	A2		+Y	0.72	0.30	0.97	0.30
							–Y	0.77	0.74	0.57	0.42
2-wide, 4-input OR-NAND NA2R4NP		9	2	# # # # # # # # #	A4		+Y	0.72	0.30	1.00	0.30
							–Y	0.80	0.98	0.57	0.42

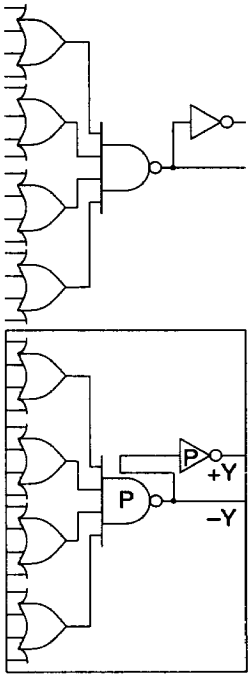
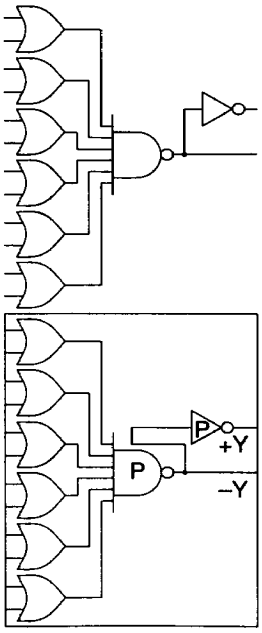
AND-NOR, OR-NAND Power Gates (cont)

Macro						Delay					
								t_{plh} (ns)		t_{phl} (ns)	
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Sym-bol No.	In-put Name	Out-put Name	t_{olh}	K_{lh}	t_{ohl}	K_{hl}
3-wide, 3-input OR-NAND NA3R3NP		10	2	# # # # # # # # # #			+Y	0.79	0.30	1.00	0.30
							–Y	0.80	0.74	0.64	0.58
3-wide, 4-input OR-NAND NA3R4NP		13	2	# # # # # # # # # # # #			+Y	0.79	0.30	1.28	0.30
							–Y	1.08	0.98	0.64	0.58

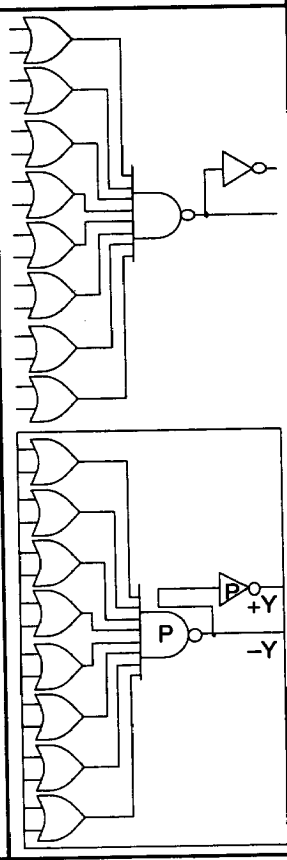
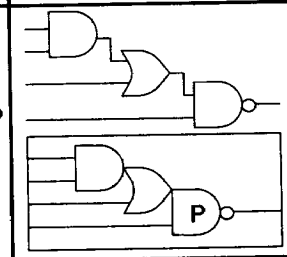
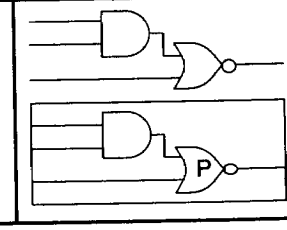
AND-NOR, OR-NAND Power Gates (cont)

Macro						Delay					
								t_{plh} (ns)		t_{phl} (ns)	
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Sym-bol No.	In-put Name	Out-put Name	t_{olh}	K_{lh}	t_{ohl}	K_{hl}
4-wide, 2-input OR-NAND NA4R2NP		10	2	@ @ @ @ @ @ @ @	A4		+Y	0.75	0.30	0.77	0.30
							–Y	0.57	0.50	0.60	0.70
4-wide, 3-input OR-NAND NA4R3NP		13	2	# # # # # # # # # # # #			+Y	0.95	0.30	1.28	0.30
							–Y	1.08	0.74	0.80	0.70

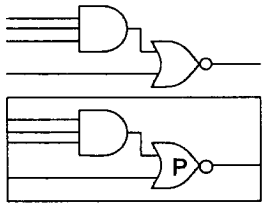
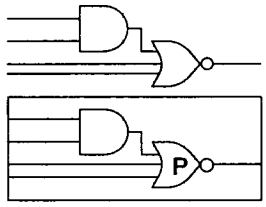
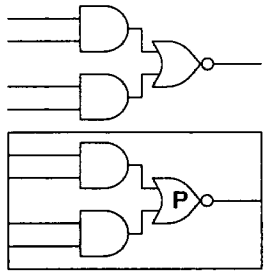
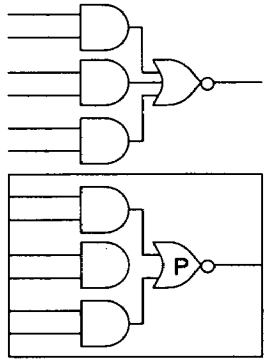
AND-NOR, OR-NAND Power Gates (cont)

Macro						Delay					
								t_{plh} (ns)		t_{phl} (ns)	
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Sym-bol No.	In-put Name	Out-put Name	t_{olh}	K_{lh}	t_{ohl}	K_{hl}
4-wide, 4-input OR-NAND NA4R4NP		17	2	# # # # # # # # # # # # # # # # # # # #	A5		+Y	1.02	0.30	1.57	0.30
							–Y	1.37	0.98	0.87	0.70
6-wide, 2-input OR-NAND NA6R2NP		9	1	@ @ @ @ @ @ @ @ @ @ @ @ @			+Y	0.70	0.50	0.67	0.30
							–Y	0.82	0.30	0.90	0.30

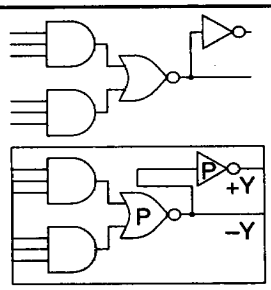
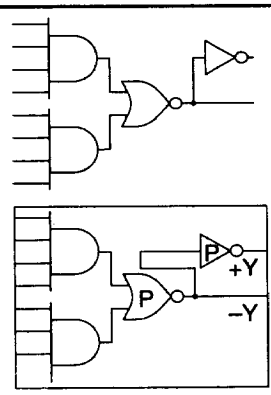
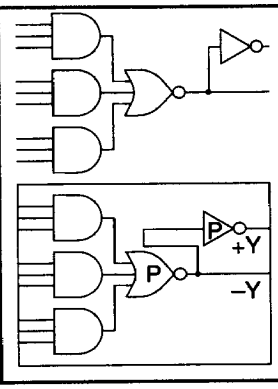
AND-NOR, OR-NAND Power Gates (cont)

Macro						Delay					
								t_{plh} (ns)		t_{phl} (ns)	
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Sym-bol No.	In-put Name	Out-put Name	t_{olh}	K_{lh}	t_{ohl}	K_{hl}
8-wide, 2-input OR-NAND NA8R2NP		12	1	@ @ @ @ @ @ @ @ @ @ @ @ @ @ @	A5		+Y	0.73	0.74	0.67	0.30
							–Y	0.82	0.30	0.93	0.30
2-AND-OR-NAND NARA24P		4	2	@ @ # @	A1	AND		0.33	0.50	0.53	0.58
						OR		0.33		0.53	
						NAND		0.33		0.40	
2-AND-NOR NRA23P		3	2	@ @ #	A1	AND		0.37	0.50	0.50	0.42
						NOR		0.36		0.50	

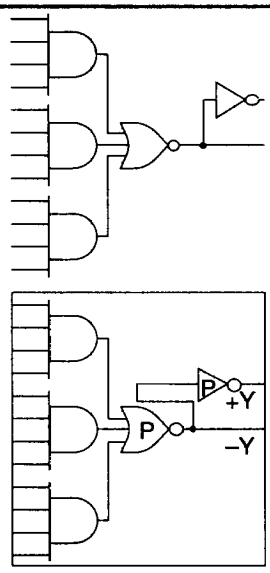
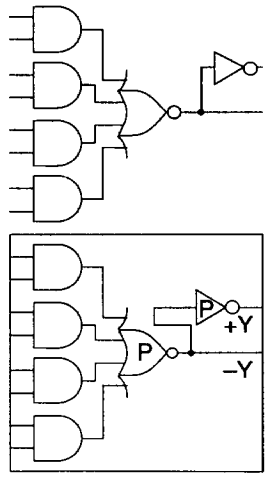
AND-NOR, OR-NAND Power Gates (cont)

Macro						Delay					
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	In-put Name	Out-put Name	t_{plh} (ns)		t_{phl} (ns)	
								t_{olh}	K_{lh}	t_{ohl}	K_{hl}
3-AND-NOR NRA34P		4	2	@ @ @ #	A2	AND NOR		0.37 0.36	0.50	0.50 0.50	0.58
2-AND-3-NOR NRA24P		4	2	@ @ # #	A2	AND NOR		0.38 0.38	0.74	0.50 0.50	0.42
2-wide 2-input AND-NOR NR2A2P		4	2	@ @ @ @	A1			0.40	0.50	0.53	0.42
3-wide 2-input AND-NOR NR3A2P		6	2	@ @ @ @ @ @	A3			0.46	0.74	0.60	0.42

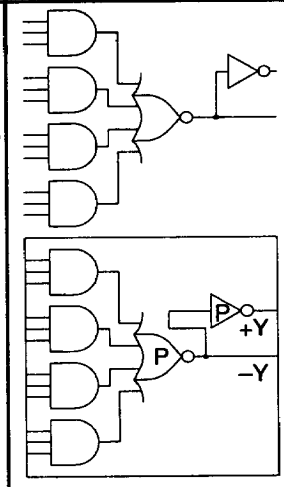
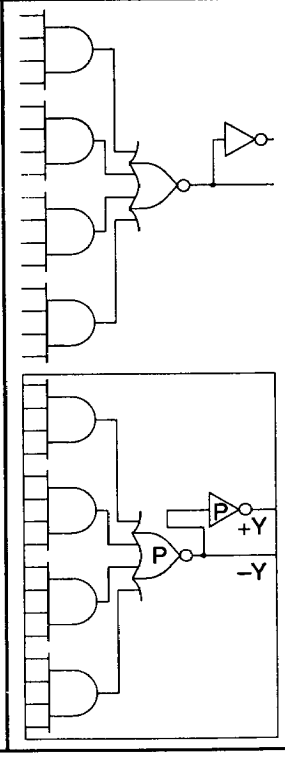
AND-NOR, OR-NAND Power Gates (cont)

Macro						Delay					
								t_{plh} (ns)		t_{phl} (ns)	
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Sym-bol No.	In-put Name	Out-put Name	t_{olh}	K_{lh}	t_{ohl}	K_{hl}
2-wide 3-input AND-NOR NR2A3NP		7	2	@ @ @ @ @ @	A2		+Y	1.05	0.30	0.60	0.30
							–Y	0.40	0.50	0.90	0.58
2-wide 4-input AND-NOR NR2A4NP		9	2	@ @ @ @ @ @ @ @	A4		+Y	1.05	0.30	0.60	0.30
							–Y	0.40	0.50	0.90	0.70
3-wide 3-input AND-NOR NR3A3NP		10	2	@ @ @ @ @ @ @ @ @			+Y	1.08	0.30	0.80	0.30
							–Y	0.60	0.74	0.93	0.58

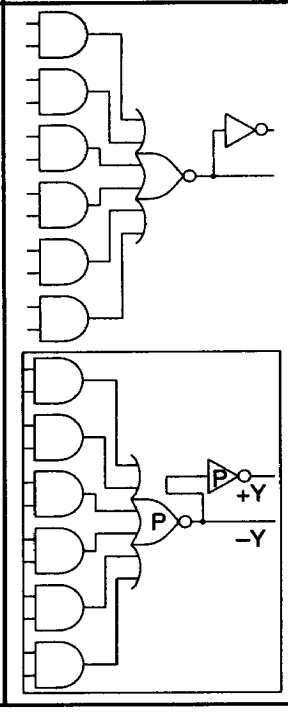
AND-NOR, OR-NAND Power Gates (cont)

Macro						Delay					
								t_{plh} (ns)		t_{phl} (ns)	
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Sym-bol No.	In-put Name	Out-put Name	t_{olh}	K_{lh}	t_{ohl}	K_{hl}
3-wide 4-input AND-NOR NR3A4NP		13	2	@ @ @ @ @ @ @ @ @ @ @ @			+Y	1.15	0.30	1.00	0.30
							–Y	0.80	0.74	1.00	0.70
4-wide 2-input AND-NOR NR4A2NP		9	2	# # # # # # # # #	A4		+Y	0.82	0.30	0.77	0.30
							–Y	0.57	0.98	0.67	0.42

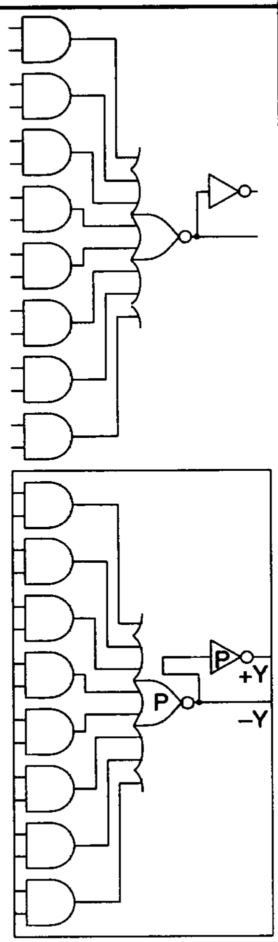
AND-NOR, OR-NAND Power Gates (cont)

Macro						Delay					
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Input Name	Output Name	t_{plh} (ns)		t_{phl} (ns)	
								t_{olh}	K_{lh}	t_{ohl}	K_{hl}
4-wide 3-input AND-NOR NR4A3NP		13	2	@ @ @ @ @ @ @ @ @ @ @ @			+Y	0.85	0.30	0.80	0.30
							–Y	0.60	0.98	0.70	0.58
4-wide 4-input AND-NOR NR4A4NP		17	2	@ @ @ @ @ @ @ @ @ @ @ @	A5		+Y	1.25	0.30	1.02	0.30
							–Y	0.82	0.98	1.10	0.70

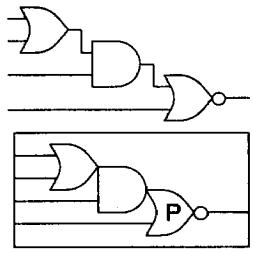
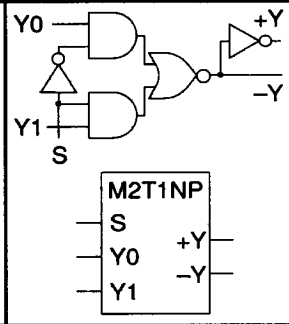
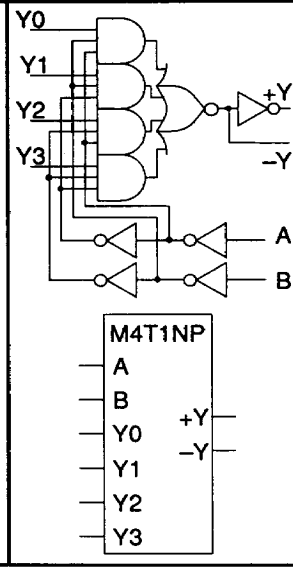
AND-NOR, OR-NAND Power Gates (cont)

Macro						Delay					
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Sym-bol No.	In-put Name	Out-put Name	t_{plh} (ns)		t_{phl} (ns)	
								t_{olh}	K_{lh}	t_{ohl}	K_{hl}
6-wide 2-input AND-NOR NR6A2NP		9	1	# # # # # # # # # # # #			+Y	0.90	0.30	1.00	0.30
							–Y	0.80	0.30	0.75	0.30

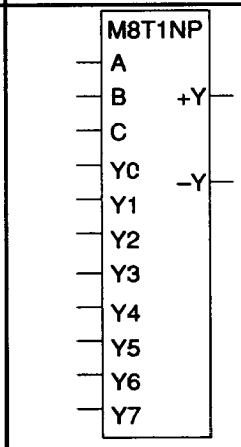
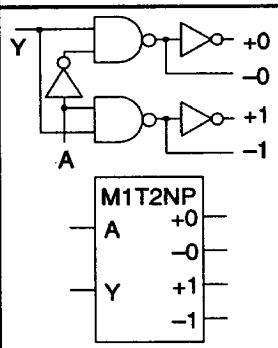
AND-NOR, OR-NAND Power Gates (cont)

Macro			LV	Clamp Level when Open	Symbol No.	Delay					
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count				Input Name	Output Name	t_{plh} (ns)		t_{phl} (ns)	
								t_{olh}	K_{lh}	t_{ohl}	K_{hl}
8-wide 2-input AND-NOR NR8A2NP		12	1	# # # # # # # # # # # # # # # #	A5		+Y	0.90	0.30	1.08	0.30
							–Y	0.88	0.30	0.75	0.30

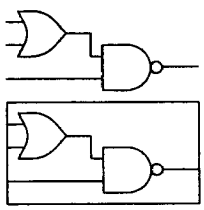
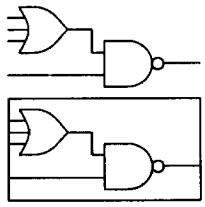
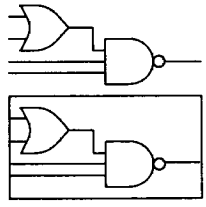
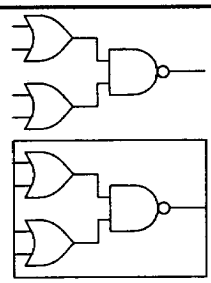
AND-NOR, OR-NAND Power Gates (cont)

Macro						Delay					
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Sym-bol No.	In-put Name	Out-put Name	t_{plh} (ns)		t_{phl} (ns)	
								t_{olh}	K_{lh}	t_{ohl}	K_{hl}
2-OR-AND-NOR NRAR24P		4	2	# # @ #	A1	OR		0.56	0.74	0.54	0.42
						AND		0.50		0.48	
						NOR		0.40		0.42	
2-to-1 multi-plexer M2T1NP		6	2 2 2	# # #	B2	Y0	+Y	0.83	0.30	0.55	0.30
						Y1		0.83		0.55	
						S		0.98		0.88	
						Y0	–Y	0.40	0.50	0.63	0.42
						Y1		0.40		0.63	
						S		0.73		0.78	
4-to-1 multi-plexer M4T1NP		15	1 1 2 2 2 2	# # # # # #	B4	Y0	+Y	1.20	0.30	0.82	0.30
						Y1		1.20		0.82	
						Y2		1.20		0.82	
						Y3		1.20		0.82	
						A		1.40		1.25	
						B		1.40		1.25	
						Y0	–Y	0.67	0.98	1.00	0.58
						Y1		0.67		1.00	
						Y2		0.67		1.00	
						Y3		0.67		1.00	
						A		1.10		1.20	
						B		1.10		1.20	

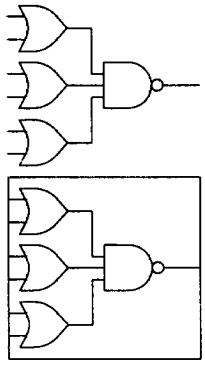
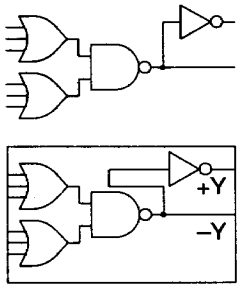
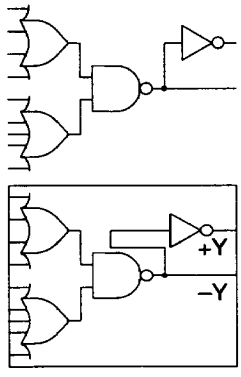
AND-NOR, OR-NAND Power Gates (cont)

Macro						Delay					
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Input Name	Output Name	t_{plh} (ns)		t_{phl} (ns)	
								t_{olh}	K_{lh}	t_{ohl}	K_{hl}
8-to-1 multiplexer M8T1NP		23	1	# # # # # # # # # # #	B6	Y0–Y7	+Y	1.37	0.30	1.30	0.58
						A		2.10		1.83	
						B					
						C					
						Y0–Y7	–Y	1.45	0.30	1.57	0.30
						A		1.98		2.30	
						B					
						C					
1-to-2 demultiplexer M1T2NP		7	2 4	# @	B3	Y	+0	0.62	0.30	0.63	0.30
						A		0.69		0.70	
						Y	+1	0.62	0.30	0.63	0.30
						A		0.62		0.63	
						Y	–0	0.43	0.30	0.47	0.42
						A		0.50		0.54	
						Y	–1	0.43	0.30	0.47	0.42
						A		0.43		0.47	

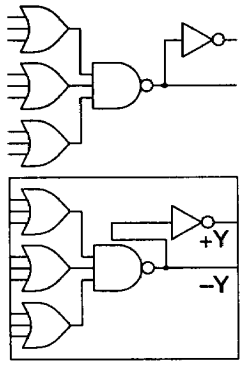
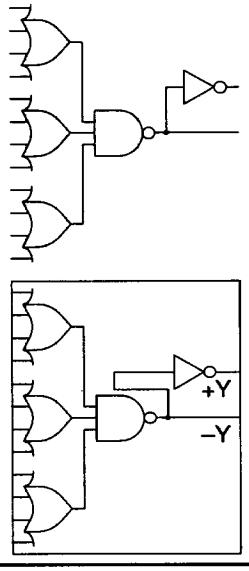
AND-NOR, OR-NAND Gates (Normal)

Macro						Delay					
								t_{plh} (ns)		t_{phl} (ns)	
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Input Name	Output Name	t_{olh}	K_{lh}	t_{ohl}	K_{hl}
2-OR NAND NAR23		2	1	# # @	A1	OR NAND		0.23 0.23	0.92	0.38 0.38	0.76
3-OR NAND NAR34		2	1	# # # @	A2	OR NAND		0.30 0.30	1.34	0.38 0.38	0.76
2-OR 3-NAND NAR24		2	1	# # @ @	A2	OR NAND		0.30 0.30	0.92	0.38 0.38	1.08
2-wide, 2-input OR-NAND NA2R2		2	1	# # # #	A1			0.30	0.92	0.43	0.76

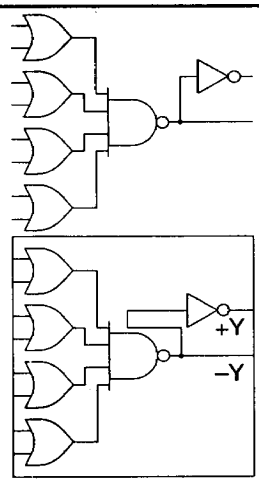
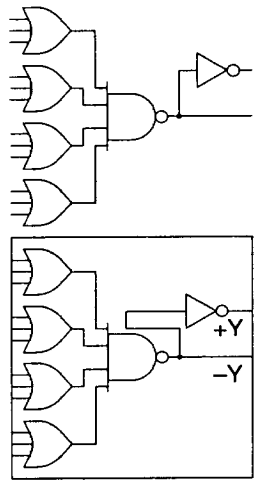
AND-NOR, OR-NAND Gates (Normal) (cont)

Macro						Delay					
								t_{plh} (ns)		t_{phl} (ns)	
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Input Name	Output Name	t_{olh}	K_{lh}	t_{ohl}	K_{hl}
3-wide, 2-input OR-NAND NA3R2		3	1	# # # # # #	A3			0.32	0.92	0.50	1.08
2-wide, 3-input OR-NAND NA2R3N		4	1	# # # # # #	A2		+Y	0.62	0.50	0.87	0.50
							–Y	0.67	1.34	0.47	0.76
2-wide, 4-input OR-NAND NA2R4N		5	1	# # # # # # # # #	A4		+Y	0.62	0.50	0.90	0.50
							–Y	0.70	1.80	0.47	0.76

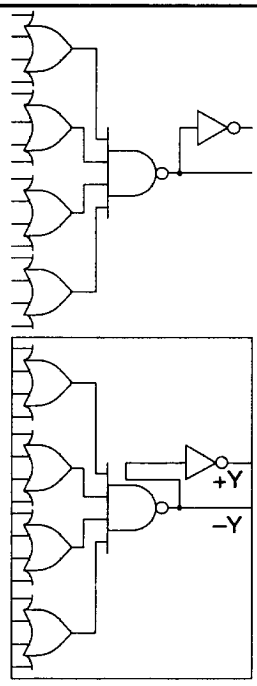
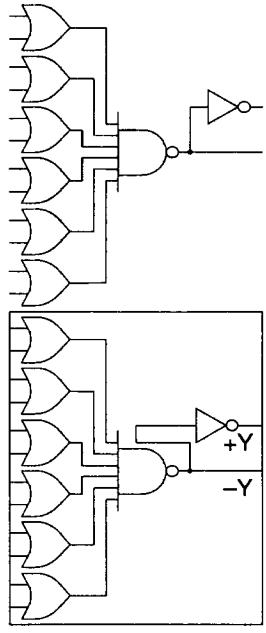
AND-NOR, OR-NAND Gates (Normal) (cont)

Macro						Delay					
								t_{plh} (ns)		t_{phl} (ns)	
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Sym-bol No.	In-put Name	Out-put Name	t_{olh}	K_{lh}	t_{ohl}	K_{hl}
3-wide, 3-input OR-NAND NA3R3N		5	1	# # # # # # # # # #			+Y	0.69	0.50	0.90	0.50
							–Y	0.70	1.34	0.54	1.08
3-wide, 4-input OR-NAND NA3R4N		7	1	# # # # # # # # # # # #			+Y	0.69	0.50	1.18	0.50
							–Y	0.98	1.80	0.54	1.08

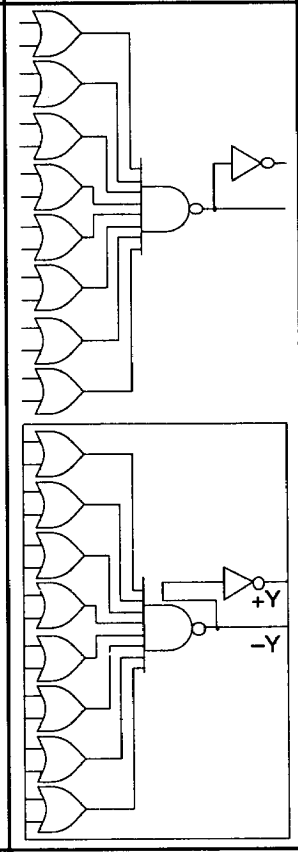
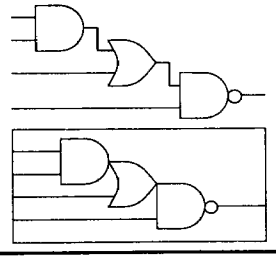
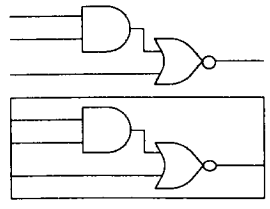
AND-NOR, OR-NAND Gates (Normal) (cont)

Macro						Delay					
								t_{plh} (ns)		t_{phl} (ns)	
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Sym-bol No.	In-put Name	Out-put Name	t_{olh}	K_{lh}	t_{ohl}	K_{hl}
4-wide, 2-input OR-NAND NA4R2N		5	1	@ @ @ @ @ @ @ @	A4		+Y	0.65	0.50	0.67	0.50
							–Y	0.47	0.92	0.50	1.36
4-wide, 3-input OR-NAND NA4R3N		7	1	# # # # # # # # # # # #			+Y	0.85	0.50	1.18	0.50
							–Y	0.98	1.34	0.70	1.36

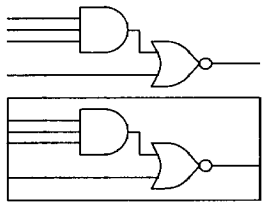
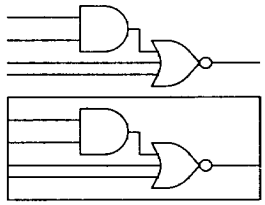
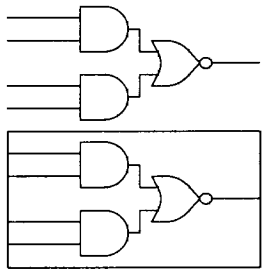
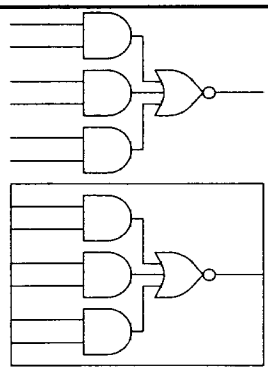
AND-NOR, OR-NAND Gates (Normal) (cont)

Macro						Delay					
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Sym-bol No.	In-put Name	Out-put Name	t_{plh} (ns)		t_{phl} (ns)	
								t_{olh}	K_{lh}	t_{ohl}	K_{hl}
4-wide, 4-input OR-NAND NA4R4N		9	1	# # # # # # # # # # # # # # # # #	A5		+Y	0.92	0.50	1.47	0.50
							–Y	1.27	1.80	0.77	1.36
6-wide, 2-input OR-NAND NA6R2N		8	1	@ @ @ @ @ @ @ @ @ @ @ @			+Y	0.60	0.92	0.57	0.50
							–Y	0.72	0.50	0.80	0.50

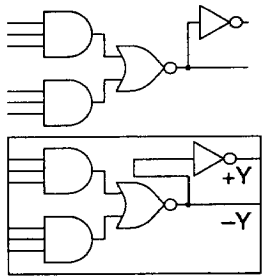
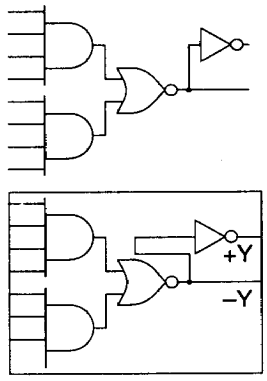
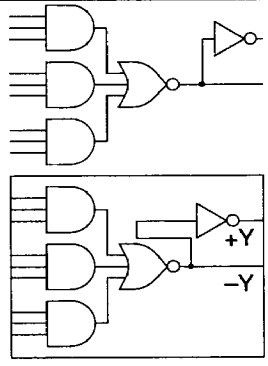
AND-NOR, OR-NAND Gates (Normal) (cont)

Macro						Delay					
								t_{plh} (ns)		t_{phl} (ns)	
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Sym-bol No.	In-put Name	Out-put Name	t_{olh}	K_{lh}	t_{ohl}	K_{hl}
8-wide, 2-input OR-NAND NA8R2N		10	1	@ @ @ @ @ @ @ @ @ @ @ @ @ @ @	A5		+Y	0.63	1.34	0.57	0.50
							–Y	0.72	0.50	0.83	0.50
2-AND-OR-NAND NARA24		2	1	@ @ # @	A1	AND		0.23	0.92	0.43	1.08
						OR		0.23		0.43	
						NAND		0.23		0.30	
2-AND-NOR NRA23		2	1	@ @ #	A1	AND		0.27	0.92	0.40	0.76
						NOR		0.26		0.40	

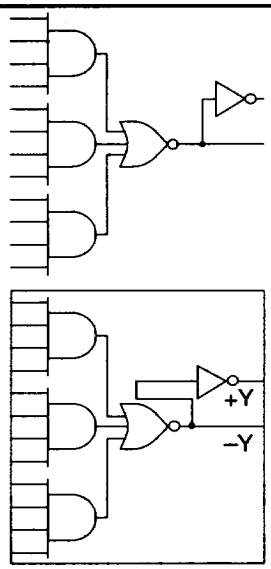
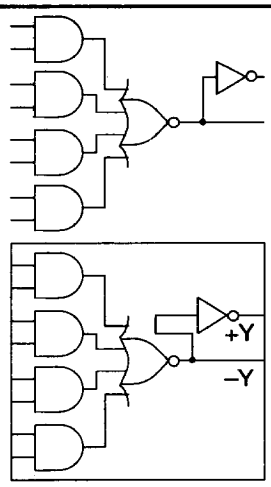
AND-NOR, OR-NAND Gates (Normal) (cont)

Macro						Delay					
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Sym-bol No.	In-put Name	Out-put Name	t_{plh} (ns)		t_{phl} (ns)	
								t_{olh}	K_{lh}	t_{ohl}	K_{hl}
3-AND-NOR NRA34		2	1	@ @ @ #	A2	AND NOR		0.27 0.26	0.92	0.40 0.40	1.08
2-AND-3-NOR NRA24		2	1	@ @ # #	A2	AND NOR		0.28 0.28	1.34	0.40 0.40	0.76
2-wide, 2-input AND-NOR NR2A2		2	1	@ @ @ @	A1			0.30	0.92	0.43	0.76
3-wide, 2-input AND-NOR NR3A2		3	1	@ @ @ @ @ @	A3			0.36	1.34	0.50	0.76

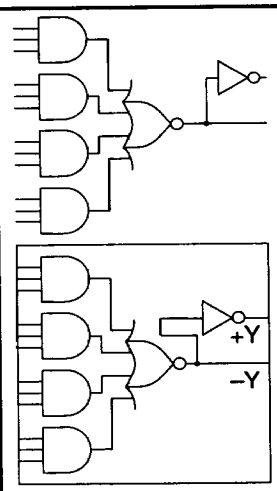
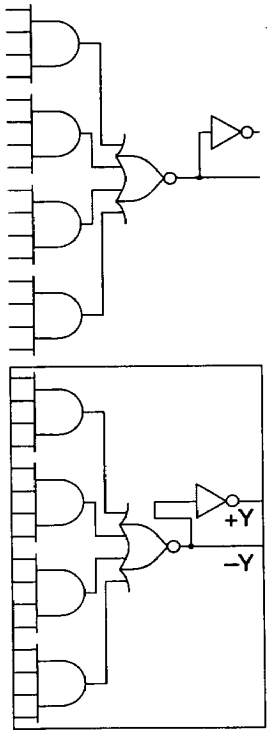
AND-NOR, OR-NAND Gates (Normal) (cont)

Macro						Delay					
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Sym-bol No.	In-put Name	Out-put Name	t_{plh} (ns)		t_{phl} (ns)	
								t_{olh}	K_{lh}	t_{ohl}	K_{hl}
2-wide, 3-input AND-NOR NR2A3N		4	1	@ @ @ @ @ @	A2		+Y	0.95	0.50	0.50	0.50
							–Y	0.30	0.92	0.80	1.08
2-wide, 4-input AND-NOR NR2A4N		5	1	@ @ @ @ @ @ @ @	A4		+Y	0.98	0.50	0.60	0.50
							–Y	0.40	0.92	0.83	1.36
3-wide, 3-input AND-NOR NR3A3N		5	1	@ @ @ @ @ @ @ @ @			+Y	0.98	0.50	0.67	0.50
							–Y	0.50	1.34	0.83	1.08

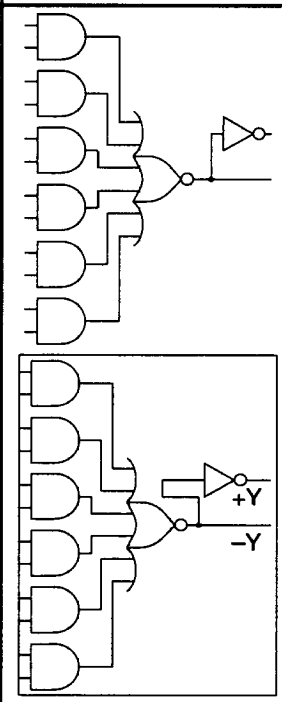
AND-NOR, OR-NAND Gates (Normal) (cont)

Macro						Delay					
								t_{plh} (ns)		t_{phl} (ns)	
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Input Name	Output Name	t_{olh}	K_{lh}	t_{ohl}	K_{hl}
3-wide 4-input AND-NOR NR3A4N		7	1	@ @ @ @ @ @ @ @ @ @ @ @			+Y	1.05	0.50	0.90	0.50
							–Y	0.70	1.34	0.90	1.36
4-wide 2-input AND-NOR NR4A2N		5	1	# # # # # # # # #	A4		+Y	0.72	0.50	0.67	0.50
							–Y	0.47	1.80	0.57	0.76

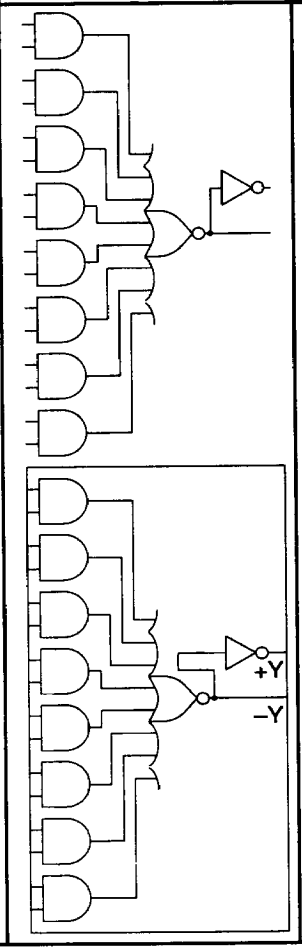
AND-NOR, OR-NAND Gates (Normal) (cont)

Macro						Delay					
								t_{plh} (ns)		t_{phl} (ns)	
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Sym-bol No.	In-put Name	Out-put Name	t_{olh}	K_{lh}	t_{ohl}	K_{hl}
4-wide 3-input AND-NOR NR4A3N		7	1	@ @ @ @ @ @ @ @ @ @ @ @			+Y	0.75	0.50	0.70	0.50
							–Y	0.50	1.80	0.60	1.34
4-wide 4-input AND-NOR NR4A4N		9	1	@ @ @ @ @ @ @ @ @ @ @ @ @ @ @ @	A5		+Y	1.15	0.50	0.92	0.50
							–Y	0.72	1.80	1.00	1.36

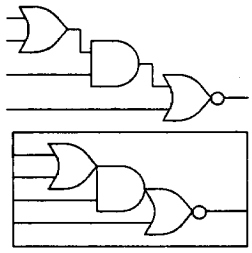
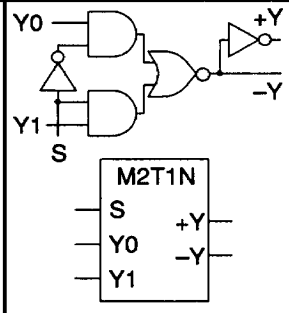
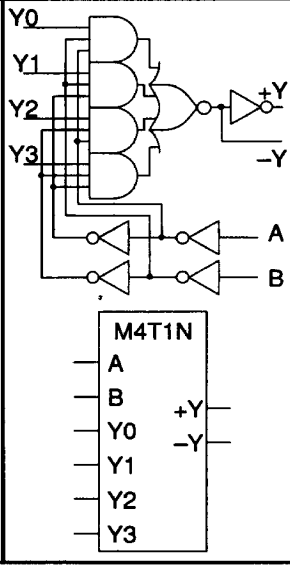
AND-NOR, OR-NAND Gates (Normal) (cont)

Macro						Delay					
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Sym-bol No.	In-put Name	Out-put Name	t_{plh} (ns)		t_{phl} (ns)	
								t_{olh}	K_{lh}	t_{ohl}	K_{hl}
6-wide 2-input AND-NOR NR6A2N		8	1	# # # # # # # # # # # #			+Y	0.80	0.50	0.90	0.50
							–Y	0.70	0.50	0.65	0.50

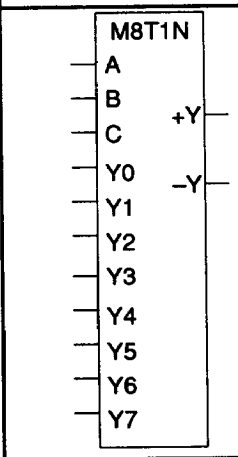
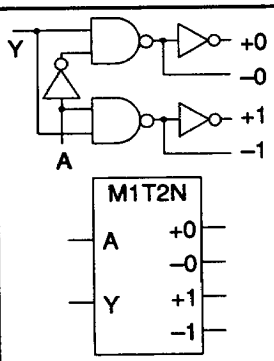
AND-NOR, OR-NAND Gates (Normal) (cont)

Macro						Delay					
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Sym-bol No.	In-put Name	Out-put Name	t_{plh} (ns)		t_{phl} (ns)	
								t_{olh}	K_{lh}	t_{ohl}	K_{hl}
8-wide 2-input AND-NOR NR8A2N		10	1	# # # # # # # # # # # # # # # # # #	A5		+Y	0.80	0.50	0.98	0.50
							–Y	0.78	0.50	0.65	0.50

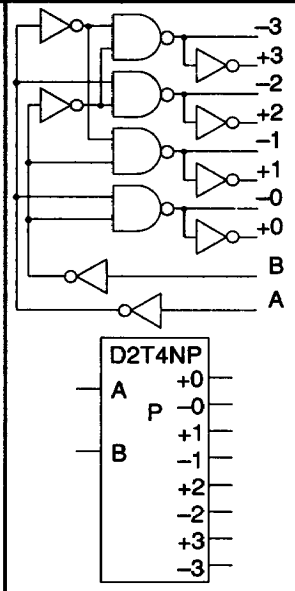
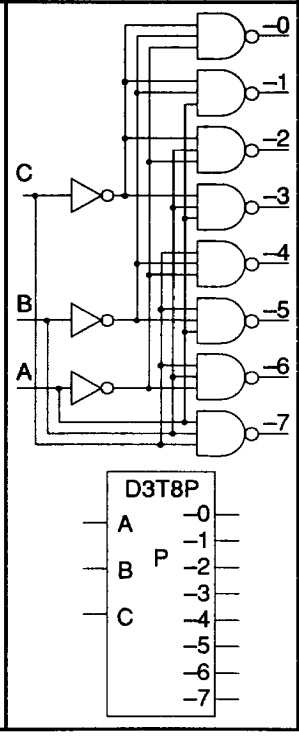
AND-NOR, OR-NAND Gates (Normal) (cont)

Macro					Sym-bol No.	Delay					
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open		In-put Name	Out-put Name	t_{plh} (ns)		t_{phl} (ns)	
								t_{olh}	K_{lh}	t_{ohl}	K_{hl}
2-OR-AND-NOR NRAR24		2	1	# # @ #	A1	OR		0.46	1.34	0.44	0.76
						AND		0.40		0.38	
						NOR		0.30		0.32	
2-to-1 multi-plexer M2T1N		3	2 1 1	# # #	B2	Y0	+Y	0.73	0.50	0.45	0.50
						Y1		0.73		0.45	
						S		0.88		0.78	
						Y0	–Y	0.30	0.92	0.53	0.76
						Y1		0.30		0.53	
						S		0.63		0.68	
4-to-1 multi-plexer M4T1N		9	1	# # # # # #	B4	Y0	+Y	1.10	0.50	0.72	0.50
						Y1		1.10		0.72	
						Y2		1.10		0.72	
						Y3		1.10		0.72	
						A		1.30		1.15	
						B		1.30		1.15	
						Y0	–Y	0.57	1.80	0.90	1.08
						Y1		0.57		0.90	
						Y2		0.57		0.90	
						Y3		0.57		0.90	
						A		1.00		1.10	
						B		1.00		1.10	

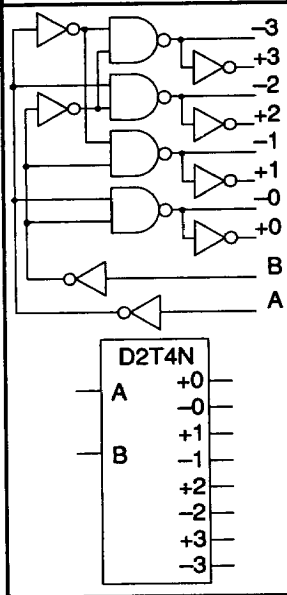
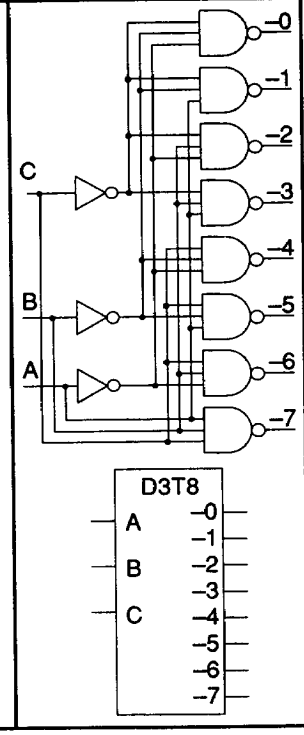
AND-NOR, OR-NAND Gates (Normal) (cont)

Macro						Delay					
								t_{plh} (ns)		t_{phl} (ns)	
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Input Name	Output Name	t_{olh}	K_{lh}	t_{ohl}	K_{hl}
8-to-1 multiplexer M8T1N		21	1	# # # # # # # # # # #	B6	Y0–Y7	+Y	1.27	0.50	1.20	1.08
						A		2.00		1.73	
						B					
						C					
						Y0–Y7	–Y	1.35	0.50	1.47	0.50
						A		1.88		2.20	
						B					
						C					
1-to-2 demultiplexer M1T2N		4	2	# @	B3	Y	+0	0.52	0.50	0.53	0.50
						A		0.59		0.60	
						Y	+1	0.52	0.50	0.53	0.50
						A		0.52		0.53	
						Y	–0	0.33	0.50	0.37	0.76
						A		0.40		0.44	
						Y	–1	0.33	0.50	0.37	0.76
						A		0.33		0.37	

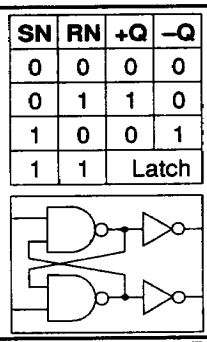
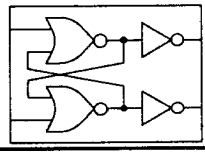
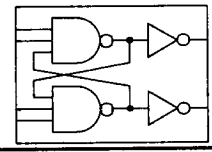
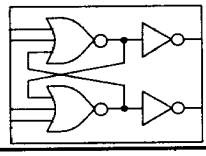
Power Decoders

Macro						Delay					
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Input Name	Output Name	t_{plh} (ns)		t_{phl} (ns)	
								t_{olh}	K_{lh}	t_{ohl}	K_{hl}
2-bit decoder D2T4NP		14	1	# #	B5	A	–0	0.58	0.30	0.62	0.42
						B		0.58		0.62	
						A	–1	0.70	0.30	0.80	0.42
						B		0.58		0.62	
						A	–2	0.58	0.30	0.62	0.42
						B		0.70		0.80	
						A	–3	0.70	0.30	0.80	0.42
						B		0.70		0.80	
						A	+0	0.77	0.30	0.78	0.30
						B		0.77		0.78	
						A	+1	0.95	0.30	0.90	0.30
						B		0.77		0.78	
						A	+2	0.77	0.30	0.78	0.30
						B		0.95		0.90	
						A	+3	0.95	0.30	0.90	0.30
						B		0.95		0.90	
3-bit decoder D3T8P		26	9	# # #	B5	A, B, C	–0 to –7	0.68	0.30	0.62	0.58

Decoders (Normal)

Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Input Name	Output Name	t_{plh} (ns) t_{olh}	t_{plh} (ns) K_{lh}	t_{phl} (ns) t_{ohl}	t_{phl} (ns) K_{hl}
2-bit decoder D2T4N		8	1	# #	B5	A	–0	0.48	0.50	0.52	0.76
						B		0.48		0.52	
						A	–1	0.60	0.50	0.70	0.76
						B		0.48		0.52	
						A	–2	0.48	0.50	0.52	0.76
						B		0.60		0.70	
						A	–3	0.60	0.50	0.70	0.76
						B		0.60		0.70	
						A	+0	0.67	0.50	0.68	0.50
						B		0.67		0.68	
						A	+1	0.85	0.50	0.80	0.50
						B		0.67		0.68	
						A	+2	0.67	0.50	0.68	0.50
						B		0.85		0.80	
						A	+3	0.85	0.50	0.80	0.50
						B		0.85		0.80	
3-bit decoder D3T8		14	5	# # #	B5	A, B, C	–0 to –7	0.58	0.50	0.52	1.08

Latches (with Scan Function)

Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{plh} (ns) t_{olh}	Delay: t_{plh} (ns) K_{lh}	Delay: t_{phl} (ns) t_{ohl}	Delay: t_{phl} (ns) K_{hl}
$\overline{RS}$ latch TLRS0		9	1	@ @	A3	$\overline{S}$	+Q	1.30	0.50	—	0.42
						$\overline{R}$		1.16		1.00	
						$\overline{S}$	–Q	1.16	0.50	1.00	0.42
						$\overline{R}$		1.30		—	
RS latch TLRS3		9	1	# #	A3	S	+Q	1.00	0.50	1.30	0.42
						R		—		1.37	
						S	–Q	—	0.50	1.37	0.42
						R		1.00		1.30	
2-input $\overline{RS}$ latch TLR2S20		10	1	@ @ @ @	A4	$\overline{S}$	+Q	1.37	0.50	—	0.42
						$\overline{R}$		1.30		1.05	
						$\overline{S}$	–Q	1.30	0.50	1.05	0.42
						$\overline{R}$		1.37		—	
2-input RS latch TLR2S23		10	1	# #	A4	S	+Q	1.05	0.50	1.37	0.42
						R		—		1.51	
						S	–Q	—	0.50	1.51	0.42
						R		1.05		1.37	

SN	RN	+Q	–Q
0	0	0	0
0	1	1	0
1	0	0	1
1	1	Latch	

S	R	+Q	–Q
0	0	Latch	
0	1	0	1
1	0	1	0
1	1	1	1

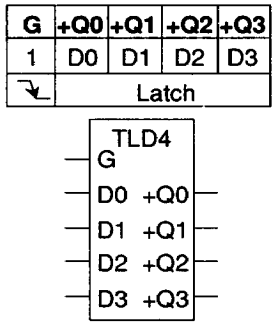
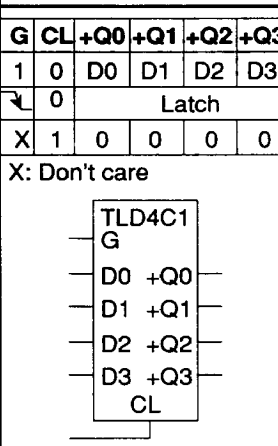
SN	RN	+Q	–Q
0	0	0	0
0	1	1	0
1	0	0	1
1	1	Latch	

S	R	+Q	–Q
0	0	Latch	
0	1	0	1
1	0	1	0
1	1	1	1

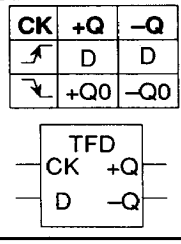
Latches (with Scan Function) (cont)

Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{plh} (ns) t_{olh}	Delay: t_{plh} (ns) K_{lh}	Delay: t_{phl} (ns) t_{ohl}	Delay: t_{phl} (ns) K_{hl}
D Latch TLD	G | +Q | –Q 1 | D | $\bar{D}$ ↘ | Latch TLD: G, D → +Q, –Q	6	1 1	@ @	C	G D	+Q	1.20 1.20	0.30	1.20 1.20	0.30
						G D	–Q	1.00 1.00	0.30	1.05 1.05	0.30
D Latch with CLR TLDC1	G | CL | +Q | –Q 1 | 0 | D | $\bar{D}$ ↘ | 0 | Latch X | 1 | 0 | 1 X: Don't care TLDC1: G, D, CL → +Q, –Q	7	1 1 1	@ @ #	C	G D CL	+Q	1.30 1.30 0.85	0.30	1.20 1.20 0.80	0.30
						G D CL	–Q	1.00 1.00 0.60	0.30	1.15 1.15 0.70	0.30
D Latch with PRE TLDP1	G | PR | +Q | –Q 1 | 0 | D | $\bar{D}$ ↘ | 0 | Latch X | 1 | 1 | 0 X: Don't care TLDP1: G, D, PR → +Q, –Q	7	1 1 1	@ @ #	C	G D PR	+Q	1.20 1.20 0.95	0.30	1.30 1.30 1.05	0.30
						G D PR	–Q	1.10 1.10 0.85	0.30	1.05 1.05 0.80	0.30
D Latch with CLR/PRE TLDPC3	G | PR | CL | +Q | –Q 1 | 0 | 0 | D | $\bar{D}$ ↘ | 0 | 0 | Latch X | 1 | 0 | 1 | 0 X | 0 | 1 | 0 | 1 X | 1 | 1 | 0 | 1 X: Don't care TLDPC3: G, D, PR, CL → +Q, –Q	8	1 1 1 1	@ @ # #	C	G D PR CL	+Q	1.40 1.40 1.10 0.85	0.30	1.40 1.40 0.95 0.80	0.30
						G D PR CL	–Q	1.20 1.20 0.75 0.60	0.30	1.25 1.25 0.95 0.70	0.30

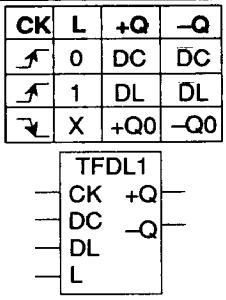
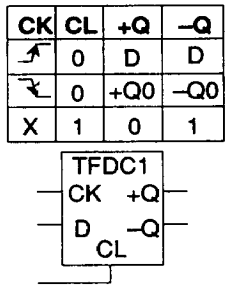
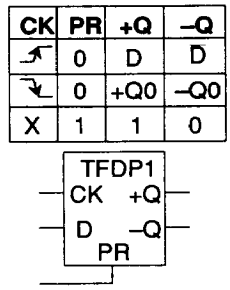
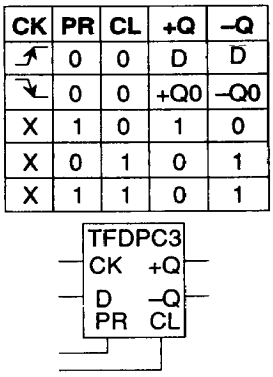
Latches (with Scan Function) (cont)

Function and Macro Name	Macro: Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Delay: Input Name	Output Name	t_{plh} (ns) t_{olh}	t_{plh} (ns) K_{lh}	t_{phl} (ns) t_{ohl}	t_{phl} (ns) K_{hl}
4-bit latch TLD4		21	1 1 1 1 1	@ @ @ @ @	B4	G D0–D3	+Q0–+Q3	1.12 1.02	0.30	1.28 1.07	0.30
4-bit latch with CLR TLD4C1		27	1 1 1 1 1 1	@ @ @ @ @ #	B4	G D0–D3 CL	+Q0–+Q3	1.12 1.12 1.00	0.30	1.28 1.07 1.05	0.30

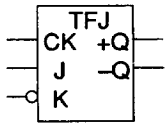
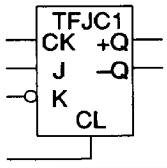
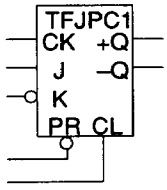
Flip-Flops (with Scan Function)

Function and Macro Name	Macro: Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Delay: Input Name	Output Name	t_{plh} (ns) t_{olh}	t_{plh} (ns) K_{lh}	t_{phl} (ns) t_{ohl}	t_{phl} (ns) K_{hl}
D flip-flop TFD		8	1	@ @	C	CK	+Q –Q	1.24 1.10	0.30 0.30	1.30 1.09	0.30 0.30

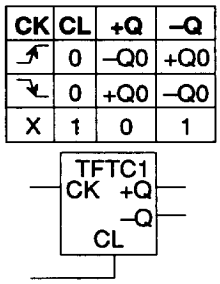
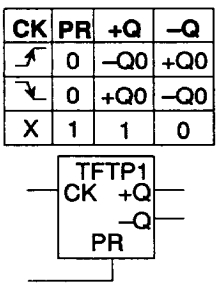
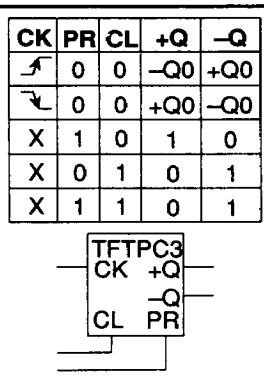
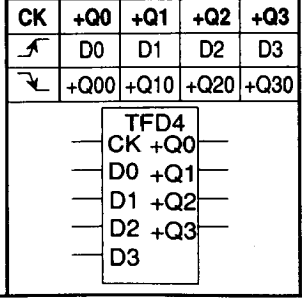
Flip-Flops (with Scan Function) (cont)

Function and Macro Name	Macro: Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Sym-bol No.	Delay: In-put Name	Out-put Name	t_{plh} (ns)	K_{lh}	t_{phl} (ns)	K_{hl}
D flip-flop with Load TFDL1		10	1 1 1 2	@ @ @ #	C	CK	+Q	1.24	0.30	1.30	0.30
							–Q	1.10	0.30	1.09	0.30
D flip-flop with CLR TFDC1		9	1 1 2	@ @ #	C	CK	+Q	1.34	0.30	1.30	0.30
						CL		—		0.87	
						CK	–Q	1.10	0.30	1.19	0.30
						CL		0.67		—	
D flip-flop with PRE TFDP1		9	1 1 2	@ @ #	C	CK	+Q	1.26	0.30	1.35	0.30
						PR		1.02		—	
						CK	–Q	1.15	0.30	1.11	0.30
						PR		—		0.87	
D flip-flop with CLR/PRE TFDPC3		10	1 1 2 2	@ @ # #	C	CK	+Q	1.26	0.30	1.35	0.30
						CL		0.94		0.87	
						PR		1.16		—	
						CK	–Q	1.15	0.30	1.11	0.30
						CL		0.67		0.79	
						PR		—		1.01	

Flip-Flops (with Scan Function) (cont)

Macro						Delay					
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Sym-bol No.	In-put Name	Out-put Name	t_{plh} (ns)		t_{phl} (ns)	
								t_{olh}	K_{lh}	t_{ohl}	K_{hl}
JK flip-flop TFJ	CK J K +Q –Q ↓ 0 0 0 1 ↓ 1 1 1 0 ↓ 0 1 +Q0 –Q0 ↓ 1 0 –Q0 +Q0 ↘ X X +Q0 –Q0 	11	2 1 1	@ @ #	C	CK	+Q	1.96	0.30	1.72	0.30
							–Q	1.96	0.30	1.72	0.30
JK flip-flop with CLR TFJC1	CK J K CL +Q –Q ↓ 0 0 0 0 1 ↓ 1 1 0 1 0 ↓ 0 1 0 +Q0 –Q0 ↓ 1 0 0 –Q0 +Q0 ↘ X X 0 +Q0 –Q0 X X X 1 0 1 	14	2 1 1 1	@ @ # #	C	CK	+Q	2.16	0.30	1.92	0.30
						CL		—		1.72	
						CK	–Q	2.00	0.30	1.94	0.30
						CL		2.08		—	
JK flip-flop with PRE/CLR TFJPC1	CK J K PR CL +Q –Q ↓ 0 0 1 0 0 1 ↓ 1 1 1 0 1 0 ↓ 0 1 1 0 +Q0 –Q0 ↓ 1 0 1 0 –Q0 +Q0 ↘ X X 1 0 +Q0 –Q0 X X X 0 0 1 0 X X X 1 1 0 1 X X X 0 1 1 1 	15	2 1 1 2 1	@ @ # @ #	C	CK	+Q	1.94	0.30	2.10	0.30
						PR		1.32		1.30	
						CL		—		2.10	
						CK	–Q	2.01	0.30	2.16	0.30
						PR		—		2.06	
						CL		1.72		1.34	

Flip-Flops (with Scan Function) (cont)

Function and Macro Name	Macro: Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Sym-bol No.	Delay: In-put Name	Out-put Name	t_{plh} (ns) t_{olh}	t_{plh} (ns) K_{lh}	t_{phl} (ns) t_{ohl}	t_{phl} (ns) K_{hl}
T flip-flop with CLR TFTC1		10	1 2	@ #	C	CK CL CK CL	+Q –Q 	2.01 — 1.10 1.72	0.30 0.30 	1.30 0.87 1.19 —	0.30 0.30
T flip-flop with PRE TFTP1		10	1 2	@ #	C	CK PR CK PR	+Q –Q 	1.26 1.02 1.15 —	0.30 0.30 	1.35 — 1.11 0.87	0.30 0.30
T flip-flop with PRE/CLR TFTPC3		11	1 2 2	@ # #	C	CK PR CL CK PR CL	+Q –Q 	1.36 1.26 1.04 1.25 — 0.77	0.30 0.30 	1.45 — 0.97 1.21 1.11 0.89	0.30 0.30
4-bit D flip-flop TFD4		29	1 1 1 1 1	@ @ @ @ @	B4	CK	+Q0– +Q3	1.40	0.30	1.85	0.30

Flip-Flops (with Scan Function) (cont)

Function and Macro Name	Macro: Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Sym-bol No.	Delay: In-put Name	Out-put Name	t_{plh} (ns) t_{olh}	t_{plh} (ns) K_{lh}	t_{phl} (ns) t_{ohl}	t_{phl} (ns) K_{hl}
4-bit D flip-flop with CLR TFD4C1	CK CL +Q0 +Q1 +Q2 +Q3 ↑ 0 D0 D1 D2 D3 ↓ 0 +Q00 +Q10 +Q20 +Q30 X 1 0 0 0 0 TFD4C1: CK +Q0, D0 +Q1, D1 +Q2, D2 +Q3, D3, CL	34	1 1 1 1 1 1	@ @ @ @ @ #	B4	CK CL	+Q0–+Q3	1.60 —	0.30	1.85 1.60	0.30

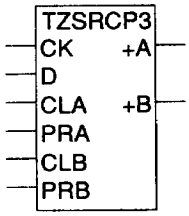
Shift Registers (with Scan Function)

Function and Macro Name	Macro: Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Sym-bol No.	Delay: In-put Name	Out-put Name	t_{plh} (ns) t_{olh}	t_{plh} (ns) K_{lh}	t_{phl} (ns) t_{ohl}	t_{phl} (ns) K_{hl}
2-bit shift register TZSR	CK +A +B ↑ D +A0 ↓ +A0 +B0 TZSR: CK +A, D +B	13	1 1	@ @	B	CK	+A +B	1.16 1.16	0.30 0.30	1.33 1.33	0.30 0.30
2-bit shift register with CLR TZSRC1	CK CLA CLB +A +B ↑ 0 0 D +A0 ↓ 0 0 +A0 +B0 X 1 X 0 X X X 1 X 0 TZSRC1: CK +A, D, CLA +B, CLB	16	1 1 2 2	@ @ # #	C	CK CLA CK CLB	+A +B 	1.26 — 1.26 —	0.30 0.30 	1.43 1.35 1.43 1.35	0.30 0.30

Shift Registers (with Scan Function) (cont)

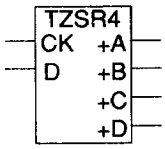
2-bit shift register with CLR/PRE — TZSRCP3

CK	CLA	CLB	PRA	PRB	+A	+B
↑	0	0	0	0	D	+A0
↓	0	0	0	0	+A0	+B0
X	1	X	X	X	0	X
X	X	1	X	X	X	0
X	X	X	1	X	1	X
X	X	X	X	1	X	1
X	1	X	1	X	0	X
X	X	1	X	1	X	0



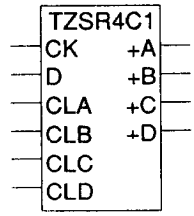
4-bit shift register — TZSR4

CK	+A	+B	+C	+D
↑	D	+A0	+B0	+C0
↓	+A0	+B0	+C0	+D0



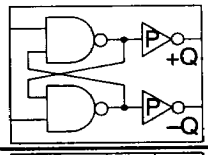
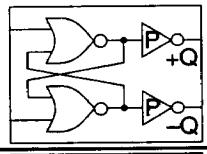
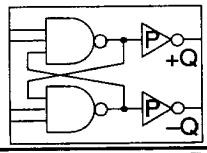
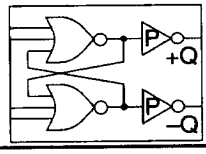
4-bit shift register with CLR — TZSR4C1

CK	CLA	CLB	CLC	CLD	+A	+B	+C	+D
↑	0	0	0	0	D	+A0	+B0	+C0
↓	0	0	0	0	+A0	+B0	+C0	+D0
X	1	X	X	X	0	X	X	X
X	X	1	X	X	X	0	X	X
X	X	X	1	X	X	X	0	X
X	X	X	X	1	X	X	X	0



Function and Macro Name	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Input Name	Output Name	t_{plh} (ns)		t_{phl} (ns)	
							t_{olh}	K_{lh}	t_{ohl}	K_{hl}
2-bit shift register with CLR/PRE TZSRCP3	18	1	@	B4	CK	+A	1.46	0.30	1.63	0.30
		1	@		CLA		0.75		1.55	
		2	#		PRA		0.82		—	
		2	#		CK	+B	1.46	0.30	1.63	0.30
		2	#		CLB		0.75		1.55	
		2	#		PRB		0.82		—	
4-bit shift register TZSR4	29	1	@	C	CK	+A	1.38	0.30	1.55	0.30
		1	@			+B	1.38	0.30	1.55	0.30
						+C	1.38	0.30	1.55	0.30
						+D	1.38	0.30	1.55	0.30
4-bit shift register with CLR TZSR4C1	37	1	@	B4	CK	+A	1.58	0.30	1.75	0.30
		1	@		CLA		—		1.35	
		2	#		CK	+B	1.58	0.30	1.75	0.30
		2	#		CLB		—		1.35	
		2	#		CK	+C	1.58	0.30	1.75	0.30
		2	#		CLC		—		1.35	
					CK	+D	1.58	0.30	1.75	0.30
					CLD		—		1.35	

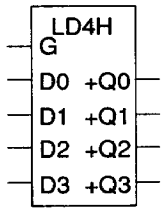
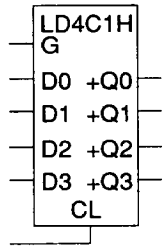
Power Latches

Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{plh} (ns)	Delay: K_{lh}	Delay: t_{phl} (ns)	Delay: K_{hl}
RS latch LRS0H	SN RN +Q –Q 0 0 0 0 0 1 1 0 1 0 0 1 1 1 Latch 	4	1	@ @	A3	$\overline{S}$ $\overline{R}$	+Q	0.75 0.61	0.30	— 0.45	0.30
						$\overline{S}$ $\overline{R}$	–Q	0.61 0.75	0.30	0.45 —	0.30
RS latch LRS3H	S R +Q –Q 0 0 Latch 0 1 0 1 1 0 1 0 1 1 1 1 	4	1	# #	A3	S R	+Q	0.45 —	0.30	0.75 0.82	0.30
						S R	–Q	— 0.45	0.30	0.82 0.75	0.30
2-input RS latch LR2S20H	SN RN +Q –Q 0 0 0 0 0 1 1 0 1 0 0 1 1 1 Latch 	5	1	@ @ @ @	A4	$\overline{S}$ $\overline{R}$	+Q	0.82 0.75	0.30	— 0.50	0.30
						$\overline{S}$ $\overline{R}$	–Q	0.75 0.82	0.30	0.50 —	0.30
2-input RS latch LR2S23H	S R +Q –Q 0 0 Latch 0 1 0 1 1 0 1 0 1 1 1 1 	5	1	# # # #	A4	S R	+Q	0.50 —	0.30	0.82 0.96	0.30
						S R	–Q	— 0.50	0.30	0.96 0.82	0.30

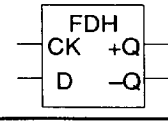
Power Latches (cont)

Function and Macro Name	Macro: Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Sym-bol No.	Delay: In-put Name	Out-put Name	t_{plh} (ns) t_{olh}	t_{plh} (ns) K_{lh}	t_{phl} (ns) t_{ohl}	t_{phl} (ns) K_{hl}
D Latch LDH	G +Q –Q 1 D D Latch LDH G +Q D –Q	5	2 1	@ @	C	G D	+Q	0.80 0.80	0.30	0.80 0.80	0.30
						G D	–Q	0.95 0.95	0.30	1.00 1.00	0.30
D Latch with CLR LDC1H	G CL +Q –Q 1 0 D D 0 Latch X 1 0 1 X: Don't care LDC1H G +Q D –Q CL	6	2 1 1	@ @ #	C	G D CL	+Q	1.25 1.25 0.80	0.30	1.15 1.15 0.75	0.30
						G D CL	–Q	0.95 0.95 0.55	0.30	1.10 1.10 0.65	0.30
D Latch with PRE LDP1H	G PR +Q –Q 1 0 D D 0 Latch X 1 1 0 X: Don't care LDP1H G +Q D –Q PR	6	2 1 1	@ @ #	C	G D PR	+Q	0.80 0.80 0.55	0.30	0.90 0.90 0.65	0.30
						G D PR	–Q	1.05 1.05 0.80	0.30	1.00 1.00 0.75	0.30
D Latch with CLR/PRE LDPC3H	G PR CL +Q –Q 1 0 0 D D 0 0 Latch X 1 0 1 0 X 0 1 0 1 X 1 1 0 1 X: Don't care LDPC3H G +Q D –Q PR CL	7	2 1 1 1	@ @ # #	C	G D PR CL	+Q	1.35 1.35 1.05 0.80	0.30	1.35 1.35 0.90 0.75	0.30
						G D PR CL	–Q	1.15 1.15 0.70 0.55	0.30	1.20 1.20 0.90 0.65	0.30

Power Latches (cont)

Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{plh} (ns) t_{olh}	Delay: t_{plh} (ns) K_{lh}	Delay: t_{phl} (ns) t_{ohl}	Delay: t_{phl} (ns) K_{hl}
4-bit latch LD4H	G | +Q0 | +Q1 | +Q2 | +Q3 1 | D0 | D1 | D2 | D3 ↘ | Latch 	14	1 1 1 1 1	@ @ @ @ @	B4	G D0–D3	+Q0–+Q3	0.92 0.82	0.30	1.03 0.82	0.30
4-bit latch with CLR LD4C1H	G | CL | +Q0 | +Q1 | +Q2 | +Q3 1 | 0 | D0 | D1 | D2 | D3 ↘ | 0 | Latch X | 1 | 0 | 0 | 0 | 0 X: Don't care 	15	1 1 1 1 1 1	@ @ @ @ @ #	B4	G D0–D3 CL	+Q0–+Q3	0.92 0.92 0.80	0.30	1.03 0.82 0.80	0.30

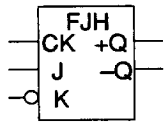
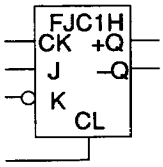
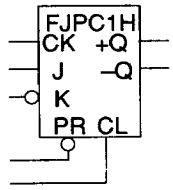
Power Flip-Flops

Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{plh} (ns) t_{olh}	Delay: t_{plh} (ns) K_{lh}	Delay: t_{phl} (ns) t_{ohl}	Delay: t_{phl} (ns) K_{hl}
D flip-flop FDH	CK | +Q | –Q ↗ | D | D ↘ | +Q0 | –Q0 	7	1 1	@ @	C	CK	+Q –Q	0.84 1.05	0.30 0.30	0.90 1.04	0.30 0.30

Power Flip-Flops (cont)

Macro						Delay					
								t_{plh} (ns)		t_{phl} (ns)	
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Sym-bol No.	In-put Name	Out-put Name	t_{olh}	K_{lh}	t_{ohl}	K_{hl}
D flip-flop with load FDL1H	CK L +Q –Q ↑ 0 DC $\overline{DC}$ ↑ 1 DL $\overline{DL}$ ↓ X +Q0 –Q0 FDL1H: CK +Q, DC –Q, DL, L	9	1 1 1 2	@ @ @ #	C	CK	+Q	0.84	0.30	0.90	0.30
							–Q	1.05	0.30	1.04	0.30
D flip-flop with CLR FDC1H	CK CL +Q –Q ↑ 0 D $\overline{D}$ ↓ 0 +Q0 –Q0 X 1 0 1 FDC1H: CK +Q, D –Q, CL	8	1 1 2	@ @ #	C	CK	+Q	0.84	0.30	0.90	0.30
						CL		—		1.06	
						CK	–Q	1.05	0.30	1.14	0.30
						CL		0.62		—	
D flip-flop with PRE FDP1H	CK PR +Q –Q ↑ 0 D $\overline{D}$ ↓ 0 +Q0 –Q0 X 1 1 0 FDP1H: CK +Q, D –Q, PR	8	1 1 2	@ @ #	C	CK	+Q	0.86	0.30	0.94	0.30
						PR		0.62		—	
						CK	–Q	1.10	0.30	1.06	0.30
						PR		—		0.82	
D flip-flop with CLR/PRE FDPC3H	CK PR CL +Q –Q ↑ 0 0 D $\overline{D}$ ↓ 0 0 +Q0 –Q0 X 1 0 1 0 X 0 1 0 1 X 1 1 1 1 FDPC3H: CK +Q, D –Q, PR CL	9	1 1 2 2	@ @ # #	C	CK	+Q	0.86	0.30	0.94	0.30
						CL		—		0.96	
						PR		0.62		0.70	
						CK	–Q	1.10	0.30	1.06	0.30
						CL		0.62		0.74	
						PR		—		0.82	

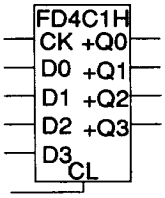
Power Flip-Flops (cont)

Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{plh} (ns) t_{olh}	Delay: t_{plh} (ns) K_{lh}	Delay: t_{phl} (ns) t_{ohl}	Delay: t_{phl} (ns) K_{hl}
JK flip-flop FJH	CK J K +Q –Q ↑ 0 0 0 1 ↑ 1 1 1 0 ↑ 0 1 +Q0 –Q0 ↑ 1 0 –Q0 +Q0 ↓ X X +Q0 –Q0 	10	2 1 1	@ @ #	C	CK	+Q	1.16	0.30	0.92	0.30
							–Q	1.16	0.30	0.92	0.30
JK flip-flop with CLR FJC1H	CK J K CL +Q –Q ↑ 0 0 0 0 1 ↑ 1 1 0 1 0 ↑ 0 1 0 +Q0 –Q0 ↑ 1 0 0 –Q0 +Q0 ↓ X X 0 +Q0 –Q0 X X X 1 0 1 	13	2 1 1 1	@ @ # #	C	CK CL	+Q	1.36 —	0.30	1.12 0.92	0.30
						CK CL	–Q	1.20 1.28	0.30	1.14 —	0.30
JK flip-flop with PRE/CLR FJPC1H	CK J K PR CL +Q –Q ↑ 0 0 1 0 0 1 ↑ 1 1 1 0 1 0 ↑ 0 1 1 0 +Q0 –Q0 ↑ 1 0 1 0 –Q0 +Q0 ↓ X X 1 0 +Q0 –Q0 X X X 0 0 1 0 X X X 1 1 0 1 X X X 0 1 0 0 	14	2 1 1 2 1	@ @ # @ #	C	CK PR CL	+Q	1.36 1.26 0.54	0.30	1.21 — 0.92	0.30
						CK PR CL	–Q	1.30 0.50 1.30	0.30	1.14 0.52 —	0.30

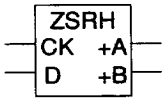
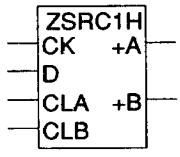
Power Flip-Flops (cont)

Function and Macro Name	Macro: Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Delay: Input Name	Output Name	t_{plh} (ns) t_{olh}	t_{plh} (ns) K_{lh}	t_{phl} (ns) t_{ohl}	t_{phl} (ns) K_{hl}
T flip-flop with CLR FTC1H	CK CL +Q –Q ↑ 0 –Q0 +Q0 ↓ 0 +Q0 –Q0 X 1 0 1 FTC1H: CK, CL; +Q, –Q	9	1 2	@ #	C	CK CL CK CL	+Q –Q 	0.84 — 1.05 0.62	0.30 0.30 	0.90 1.06 1.14 —	0.30 0.30
T flip-flop with PRE FTP1H	CK PR +Q –Q ↑ 0 –Q0 +Q0 ↓ 0 +Q0 –Q0 X 1 1 0 FTP1H: CK, PR; +Q, –Q	9	1 2	@ #	C	CK PR CK PR	+Q –Q 	0.86 0.62 1.10 —	0.30 0.30 	0.94 — 1.06 0.82	0.30 0.30
T flip-flop with PRE/CLR FTPC3H	CK PR CL +Q –Q ↑ 0 0 –Q0 +Q0 ↓ 0 0 +Q0 –Q0 X 1 0 1 0 X 0 1 0 1 X 1 1 1 1 FTPC3H: CK; +Q, –Q; PR, CL	10	1 2 2	@ # #	C	CK PR CL CK PR CL	+Q –Q 	0.86 0.62 — 1.20 — 0.72	0.30 0.30 	0.94 0.70 0.96 1.16 0.92 0.84	0.30 0.30
4-bit D flip-flop FD4H	CK +Q0 +Q1 +Q2 +Q3 ↑ D0 D1 D2 D3 ↓ +Q00 +Q10 +Q20 +Q30 FD4H: CK; D0, D1, D2, D3; +Q0, +Q1, +Q2, +Q3	22	1 1 1 1 1	@ @ @ @ @	B4	CK	+Q0– +Q3	1.20	0.30	1.60	0.30

Power Flip-Flops (cont)

Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Input Name	Output Name	Delay t_{plh} (ns)		Delay t_{phl} (ns)	
								t_{olh}	K_{lh}	t_{ohl}	K_{hl}
4-bit D flip-flop with CLR FD4C1H	CK CL +Q0 +Q1 +Q2 +Q3 ↑ 0 D0 D1 D2 D3 ↓ 0 +Q00 +Q10 +Q20 +Q30 X 1 0 0 0 0 	26	1 1 1 1 1 1	@ @ @ @ @ #	B4	CK CL	+Q0– +Q3	1.40 —	0.30	1.60 1.35	0.30

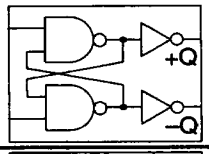
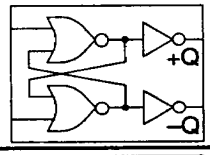
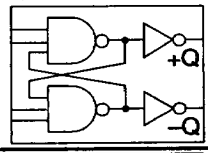
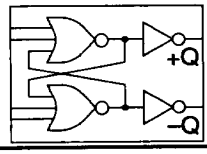
Power Shift Registers

Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Input Name	Output Name	Delay t_{plh} (ns)		Delay t_{phl} (ns)	
								t_{olh}	K_{lh}	t_{ohl}	K_{hl}
2-bit shift register ZSRH	CK +A +B ↑ D +A0 ↓ +A0 +B0 	11	1 1	@ @	B1	CK	+A +B	0.96 0.96	0.30 0.30	1.08 1.08	0.30 0.30
2-bit shift register with CLR ZSRC1H	CK CLA CLB +A +B ↑ 0 0 D +A0 ↓ 0 0 +A0 +B0 X 1 X 0 X X X 1 X 0 	13	1 1 2 2	@ @ # #	C	CK CLA CK CLB	+A +B 	1.06 — 1.06 —	0.30 0.30 	1.18 1.10 1.18 1.10	0.30 0.30

Power Shift Registers (cont)

Macro: Function and Macro Name	Macro: Equiv. Circuit and Symbol	Macro: Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{plh} (ns)		Delay: t_{phl} (ns)	
								t_{olh}	K_{lh}	t_{ohl}	K_{hl}
2-bit shift register with CLR/PRE ZSRCP3H	CK CLA CLB PRA PRB +A +B ↑ 0 0 0 0 D +A0 ↓ 0 0 0 0 +A0 +B0 X 1 X X X 0 X X X 1 X X X 0 X X X 1 X 1 X X X X X 1 X 1 X 1 X 1 X 1 X X X 1 X 1 X 1 ZSRCP3H: CK, D, CLA, PRA, CLB, PRB → +A, +B	15	1 1 2 2 2 2	@ @ # # # #	B4	CK CLA PRA CK CLB PRB	+A +B 	1.26 — 0.62 1.26 — 0.62	0.30 0.30 	1.38 1.30 0.70 1.38 1.30 0.70	0.30 0.30
4-bit shift register ZSR4H	CK +A +B +C +D ↑ D +A0 +B0 +C0 ↓ +A0 +B0 +C0 +D0 ZSR4H: CK, D → +A, +B, +C, +D	20	1 1	@ @	C	CK	+A +B +C +D	1.18 1.18 1.18 1.18	0.30 0.30 0.30 0.30	1.30 1.30 1.30 1.30	0.30 0.30 0.30 0.30
4-bit shift register with CLR ZSR4C1H	CK CLA CLB CLC CLD +A +B +C +D ↑ 0 0 0 0 D +A0 +B0 +C0 ↓ 0 0 0 0 +A0 +B0 +C0 +D0 X 1 X X X 0 X X X X X 1 X X X 0 X X X X X 1 X X X 0 X X X X X 1 X X X 0 ZSR4C1H: CK, D, CLA, CLB, CLC, CLD → +A, +B, +C, +D	24	1 1 2 2 2 2	@ @ # # # #	B4	CK CLA CK CLB CK CLC CK CLD	+A +B +C +D 	1.38 — 1.38 — 1.38 — 1.38 —	0.30 0.30 0.30 0.30 	1.50 1.10 1.50 1.10 1.50 1.10 1.50 1.10	0.30 0.30 0.30 0.30

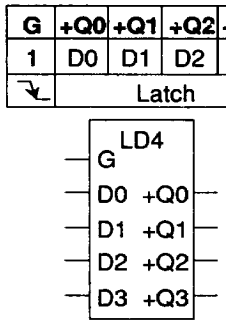
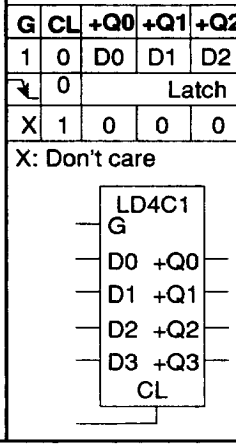
Latches (Normal)

Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Sym-bol No.	Input Name	Output Name	t_{plh} (ns) t_{olh}	K_{lh}	t_{phl} (ns) t_{ohl}	K_{hl}
RS latch LRS0	SN RN +Q –Q 0 0 0 0 0 1 1 0 1 0 0 1 1 1 Latch 	3	1	@ @	A3	$\overline{S}$ $\overline{R}$	+Q	0.65 0.51	0.50	— 0.35	0.50
						$\overline{S}$ $\overline{R}$	–Q	0.51 0.65	0.50	0.35 —	0.50
RS latch LRS3	S R +Q –Q 0 0 Latch 0 1 0 1 1 0 1 0 1 1 1 1 	3	1	# #	A3	S R	+Q	0.35 —	0.50	0.65 0.72	0.50
						S R	–Q	— 0.35	0.50	0.72 0.65	0.50
2-input RS latch LR2S20	SN RN +Q –Q 0 0 0 0 0 1 1 0 1 0 0 1 1 1 Latch 	4	1	@ @ @ @	A4	$\overline{S}$ $\overline{R}$	+Q	0.72 0.65	0.50	— 0.40	0.50
						$\overline{S}$ $\overline{R}$	–Q	0.65 0.72	0.50	0.40 —	0.50
2-input RS latch LR2S23	S R +Q –Q 0 0 Latch 0 1 0 1 1 0 1 0 1 1 1 1 	4	1	# # # #	A4	S R	+Q	0.40 —	0.50	0.72 0.86	0.50
						S R	–Q	— 0.40	0.50	0.86 0.72	0.50

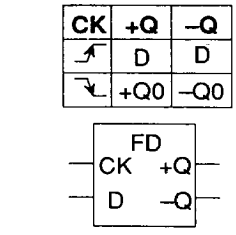
Latches (Normal) (cont)

Macro						Delay					
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	In-put Name	Out-put Name	t_{plh} (ns)		t_{phl} (ns)	
								t_{olh}	K_{lh}	t_{ohl}	K_{hl}
D Latch LD	G | +Q | –Q 1 | D | $\overline{D}$ ↘ | Latch LD: G, D → +Q, –Q	4	2 1	@ @	C	G D	+Q	0.70 0.70	0.50	0.70 0.70	0.50
						G D	–Q	0.85 0.85	0.50	0.90 0.90	0.50
D Latch with CLR LDC1	G | CL | +Q | –Q 1 | 0 | D | $\overline{D}$ ↘ | 0 | Latch X | 1 | 0 | 1 X: Don't care LDC1: G, D, CL → +Q, –Q	5	2 1 1	@ @ #	C	G D CL	+Q	1.15 1.15 0.70	0.50	1.05 1.05 0.65	0.50
						G D CL	–Q	0.85 0.85 0.45	0.50	1.00 1.00 0.55	0.50
D Latch with PRE LDP1	G | PR | +Q | –Q 1 | 0 | D | $\overline{D}$ ↘ | 0 | Latch X | 1 | 1 | 0 X: Don't care LDP1: G, D, PR → +Q, –Q	5	2 1 1	@ @ #	C	G D PR	+Q	0.70 0.70 0.45	0.50	0.80 0.80 0.55	0.50
						G D PR	–Q	0.95 0.95 0.70	0.50	0.90 0.90 0.65	0.50
D Latch with CLR/PRE LDPC3	G | PR | CL | +Q | –Q 1 | 0 | 0 | D | $\overline{D}$ ↘ | 0 | 0 | Latch X | 1 | 0 | 1 | 0 X | 0 | 1 | 0 | 1 X | 1 | 1 | 0 | 1 X: Don't care LDPC3: G, D, PR, CL → +Q, –Q	6	2 1 1 1	@ @ # #	C	G D PR CL	+Q	1.25 1.25 0.95 0.70	0.50	1.25 1.25 0.80 0.65	0.50
						G D PR CL	–Q	1.05 1.05 0.60 0.45	0.50	1.10 1.10 0.80 0.55	0.50

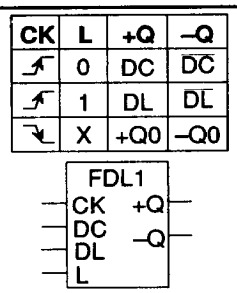
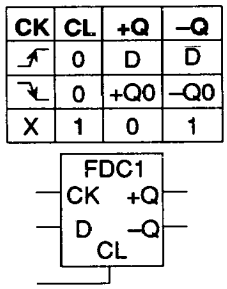
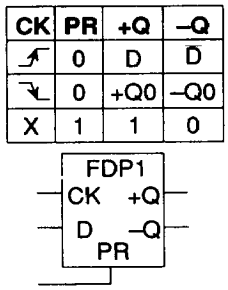
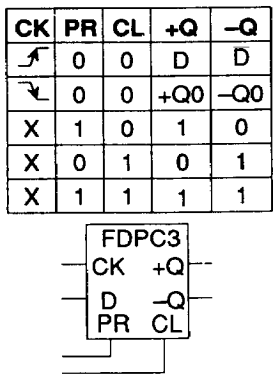
Latches (Normal) (cont)

Function and Macro Name	Macro: Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Sym-bol No.	Delay: In-put Name	Out-put Name	t_{plh} (ns) t_{olh}	t_{plh} (ns) K_{lh}	t_{phl} (ns) t_{ohl}	t_{phl} (ns) K_{hl}
4-bit latch LD4		13	1 1 1 1 1	@ @ @ @ @	B4	G D0–D3	+Q0–+Q3	0.82 0.72	0.50	0.93 0.72	0.50
4-bit latch with CLR LD4C1		14	1 1 1 1 1 1	@ @ @ @ @ #	B4	G D0–D3 CL	+Q0–+Q3	0.82 0.82 0.70	0.50	0.93 0.72 0.70	0.50

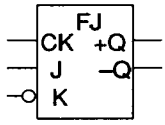
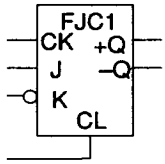
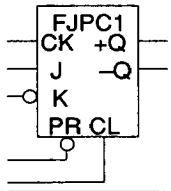
Flip-Flops (Normal)

Function and Macro Name	Macro: Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Sym-bol No.	Delay: In-put Name	Out-put Name	t_{plh} (ns) t_{olh}	t_{plh} (ns) K_{lh}	t_{phl} (ns) t_{ohl}	t_{phl} (ns) K_{hl}
D flip-flop FD		6	1	@ @	C	CK	+Q –Q	0.74 0.95	0.50 0.50	0.80 0.94	0.50 0.50

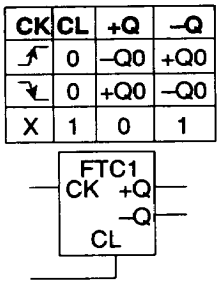
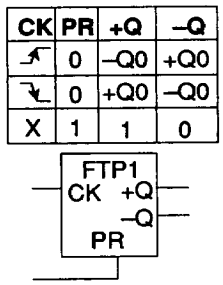
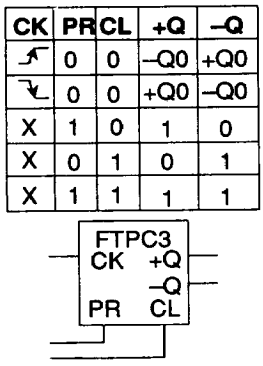
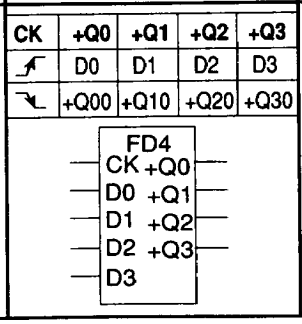
Flip-Flops (Normal) (cont)

Macro						Delay					
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	In-put Name	Out-put Name	t_{plh} (ns)		t_{phl} (ns)	
								t_{olh}	K_{lh}	t_{ohl}	K_{hl}
D flip-flop with load FDL1		8	1 1 1 2	@ @ @ #	C	CK	+Q	0.74	0.50	0.80	0.50
							–Q	0.95	0.50	0.94	0.50
D flip-flop with CLR FDC1		7	1 1 2	@ @ #	C	CK	+Q	0.74	0.50	0.80	0.50
						CL		—		0.96	
						CK	–Q	0.95	0.50	1.04	0.50
						CL		0.52		—	
D flip-flop with PRE FDP1		7	1 1 2	@ @ #	C	CK	+Q	0.76	0.50	0.84	0.50
						PR		0.52		—	
						CK	–Q	1.00	0.50	0.96	0.50
						PR		—		0.72	
D flip-flop with PRE/CLR FDPC3		8	1 1 2 2	@ @ # #	C	CK	+Q	0.76	0.50	0.84	0.50
						CL		—		0.86	
						PR		0.52		0.60	
						CK	–Q	1.00	0.50	0.96	0.50
						CL		0.52		0.64	
						PR		—		0.72	

Flip-Flops (Normal) (cont)

Function and Macro Name	Macro: Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Sym-bol No.	Delay: In-put Name	Out-put Name	t_{plh} (ns) t_{olh}	t_{plh} (ns) K_{lh}	t_{phl} (ns) t_{ohl}	t_{phl} (ns) K_{hl}
JK flip-flop FJ	CK J K +Q –Q ↑ 0 0 0 1 ↑ 1 1 1 0 ↑ 0 1 +Q0 –Q0 ↑ 1 0 –Q0 +Q0 ↓ X X +Q0 –Q0 	9	2 1 1	@ @ #	C	CK	+Q	1.06	0.50	0.82	0.50
							–Q	1.06	0.50	0.82	0.50
JK flip-flop with CLR FJC1	CK J K CL +Q –Q ↑ 0 0 0 0 1 ↑ 1 1 0 1 0 ↑ 0 1 0 +Q0 –Q0 ↑ 1 0 0 –Q0 +Q0 ↓ X X 0 +Q0 –Q0 X X X 1 0 1 	12	2 1 1 1	@ @ # #	C	CK CL	+Q	1.26 —	0.50	1.02 0.82	0.50
						CK CL	–Q	1.10 1.18	0.50	1.04 —	0.50
JK flip-flop with PRE/CLR FJPC1	CK J K PR CL +Q –Q ↑ 0 0 1 0 0 1 ↑ 1 1 1 0 1 0 ↑ 0 1 1 0 +Q0 –Q0 ↑ 1 0 1 0 –Q0 +Q0 ↓ X X 1 0 +Q0 –Q0 X X X 0 0 1 0 X X X 1 1 0 1 X X X 0 1 0 0 	13	2 1 1 2 1	@ @ # @ #	C	CK PR CL	+Q	1.26 1.16 0.44	0.50	1.11 — 0.82	0.50
						CK PR CL	–Q	1.20 0.40 1.20	0.50	1.04 0.42 —	0.50

Flip-Flops (Normal) (cont)

Function and Macro Name	Macro: Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Delay: Input Name	Output Name	t_{plh} (ns) t_{olh}	K_{lh}	t_{phl} (ns) t_{ohl}	K_{hl}
T flip-flop with CLR FTC1		8	1 2	@ #	C	CK CL CK CL	+Q –Q 	0.74 — 0.95 0.52	0.50 0.50 	0.80 0.96 1.04 —	0.50 0.50
T flip-flop with PRE FTP1		8	1 2	@ #	C	CK PR CK PR	+Q –Q 	0.76 0.52 1.00 —	0.50 0.50 	0.84 — 0.96 0.72	0.50 0.50
T flip-flop with PRE/CLR FTPC3		9	1 2 2	@ # #	C	CK PR CL CK PR CL	+Q –Q 	0.76 0.52 — 1.10 — 0.62	0.50 0.50 	0.84 0.60 0.86 1.06 0.82 0.74	0.50 0.50
4-bit D flip-flop FD4		21	1 1 1 1 1	@ @ @ @ @	B4	CK	+Q0– +Q3	1.10	0.50	1.50	0.50

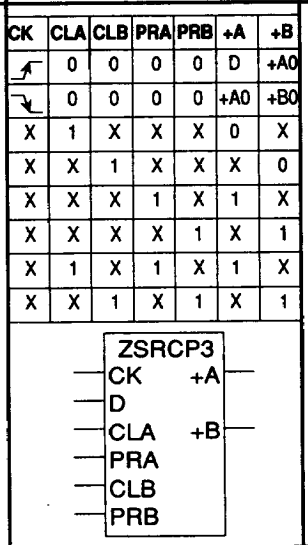
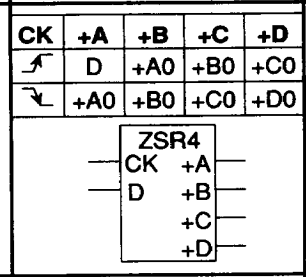
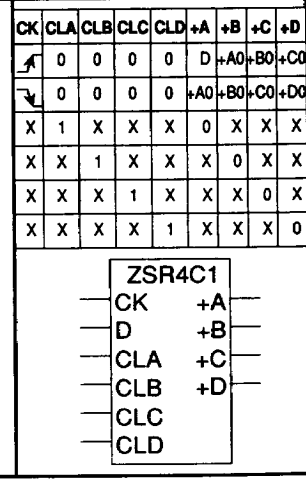
Flip-Flops (Normal) (cont)

Function and Macro Name	Macro: Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Delay: Input Name	Output Name	t_{plh} (ns) t_{olh}	K_{lh}	t_{phl} (ns) t_{ohl}	K_{hl}
4-bit D flip-flop with CLR FD4C1	CK CL +Q0 +Q1 +Q2 +Q3 ↑ 0 D0 D1 D2 D3 ↓ 0 +Q00 +Q10 +Q20 +Q30 X 1 0 0 0 0 FD4C1: CK +Q0, D0 +Q1, D1 +Q2, D2 +Q3, D3, CL	25	1 1 1 1 1 1	@ @ @ @ @ #	B4	CK CL	+Q0–+Q3	1.30 —	0.50	1.50 1.25	0.50

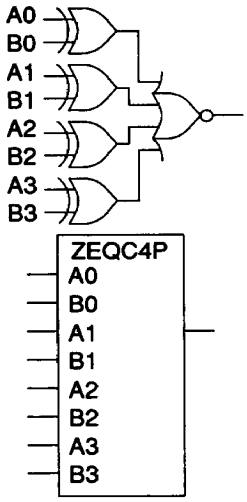
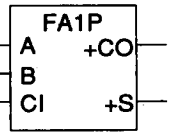
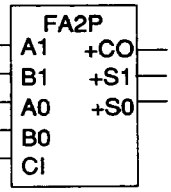
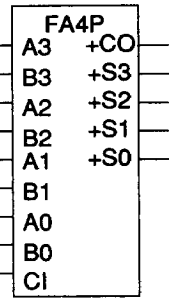
Shift Registers (Normal)

Function and Macro Name	Macro: Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Delay: Input Name	Output Name	t_{plh} (ns) t_{olh}	K_{lh}	t_{phl} (ns) t_{ohl}	K_{hl}
2-bit shift register ZSR	CK +A +B ↑ D +A0 ↓ +A0 +B0 ZSR: CK +A, D +B	10	1 1	@ @	B1	CK	+A +B	0.86 0.86	0.50 0.50	0.98 0.98	0.50 0.50
2-bit shift register with CLR ZSRC1	CK CLA CLB +A +B ↑ 0 0 D +A0 ↓ 0 0 +A0 +B0 X 1 X 0 X X X 1 X 0 ZSRC1: CK +A, D, CLA +B, CLB	12	1 1 2 2	@ @ # #	C	CK CLA CK CLB	+A +B 	0.96 — 0.96 —	0.50 0.50 	1.08 1.00 1.08 1.00	0.50 0.50

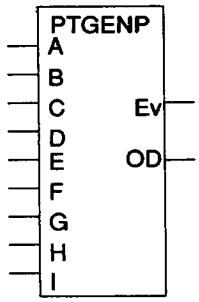
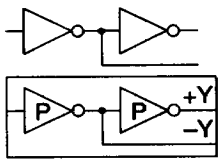
Shift Registers (Normal)

Function and Macro Name	Macro: Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Delay: Input Name	Output Name	t_{plh} (ns) t_{olh}	t_{plh} (ns) K_{lh}	t_{phl} (ns) t_{ohl}	t_{phl} (ns) K_{hl}
2-bit shift register with CLR/PRE ZSRCP3		14	1 1 2 2 2 2	@ @ # # # #	B4	CK CLA PRA CK CLB PRB	+A +B 	1.16 — 0.52 1.16 — 0.52	0.50 0.50 	1.28 1.20 0.60 1.28 1.20 0.60	0.50 0.50
4-bit shift register ZSR4		19	1 1	@ @	C	CK	+A +B +C +D	1.08 1.08 1.08 1.08	0.50 0.50 0.50 0.50	1.20 1.20 1.20 1.20	0.50 0.50 0.50 0.50
4-bit shift register with CLR ZSR4C1		23	1 1 2 2 2 2	@ @ # # # #	B4	CK CLA CK CLB CK CLC CK CLD	+A +B +C +D 	1.28 — 1.28 — 1.28 — 1.28 —	0.50 0.50 0.50 0.50 	1.40 1.00 1.40 1.00 1.40 1.00 1.40 1.00	0.50 0.50 0.50 0.50

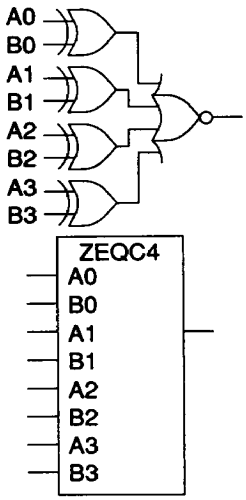
Others (Power)

Macro						Delay					
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Input Name	Output Name	t_{plh} (ns)		t_{phl} (ns)	
								t_{olh}	K_{lh}	t_{ohl}	K_{hl}
4-bit comparator ZEQC4P		14	2	# # # # # # # #	B5	A0–A3, B0–B3		0.78	0.98	0.70	0.30
1-bit full adder FA1P		9	2 2 2	# # #	B2	A, B CI	+CO	1.02 0.70	0.30	0.80 0.42	0.42
						A, B CI	+S	1.06 0.74	0.30	1.08 0.70	0.30
2-bit full adder FA2P		16	2 2 2 2 2	# # # # #	C	An, Bn CI	+CO	1.48 1.30	0.30	1.32 0.74	0.42
						An, Bn CI	+Sn	1.72 1.14	0.30	1.44 0.86	0.30
4-bit full adder FA4P		46	2 2 2 2 2 2 2 2 4	# # # # # # # # #	B5	An, Bn CI	+CO	1.30 1.10	0.30	1.22 1.06	0.30
						An, Bn CI	+Sn	2.68 2.26	0.50	2.74 2.32	0.42

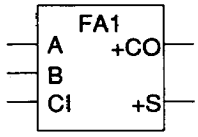
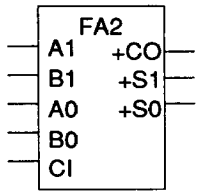
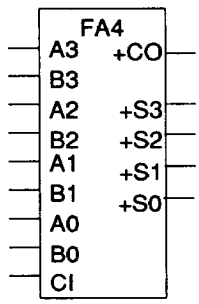
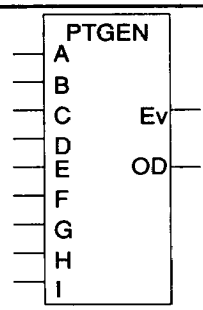
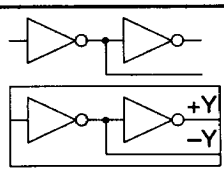
Others (Power) (cont)

Macro						Delay					
								t_{plh} (ns)		t_{phl} (ns)	
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Input Name	Output Name	t_{olh}	K_{lh}	t_{ohl}	K_{hl}
4-bit parity generator/ checker PTGENP		42	1 1 1 1 1 1 1 1 1	# # # # # # # # #	B5	A–I	Ev	2.50	0.98	2.50	0.58
							OD	2.65	0.30	2.70	0.30
Power buffer BUFP		2	2	@	A1		+Y	0.51	0.30	0.44	0.30
							–Y	0.24	0.30	0.36	0.30

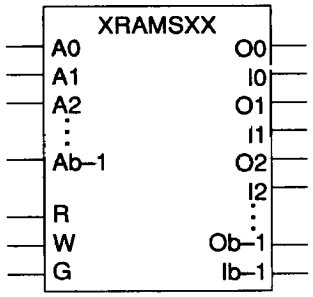
Other (Normal)

Macro						Delay					
								t_{plh} (ns)		t_{phl} (ns)	
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	Input Name	Output Name	t_{olh}	K_{lh}	t_{ohl}	K_{hl}
4-bit comparator ZEQC4		12	2	# # # # # # # #	B5	A0–A3, B0–B3		0.68	1.80	0.60	0.50

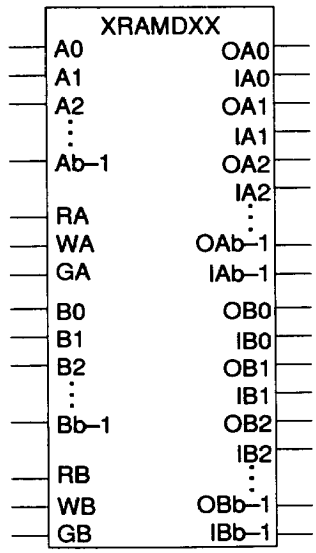
Other (Normal) (cont)

Macro						Delay					
								t_{plh} (ns)		t_{phl} (ns)	
Function and Macro Name	Equiv. Circuit and Symbol	Equiv. Gate Count	LV	Clamp Level when Open	Symbol No.	In-put Name	Out-put Name	t_{olh}	K_{lh}	t_{ohl}	K_{hl}
1-bit full adder FA1		7	2 2 2	# # #	B2	A, B CI A, B CI	+CO +S 	0.92 0.60 0.96 0.64	0.50 0.50 	0.70 0.32 0.98 0.60	0.76 0.50
2-bit full adder FA2		14	2 2 2 2 2	# # # # #	C	An, Bn CI An, Bn CI	+CO +Sn 	1.38 1.20 1.62 1.04	0.50 0.50 	1.22 0.64 1.34 0.76	0.76 0.50
4-bit full adder FA4		43	2 2 2 2 2 2 2 2 3	# # # # # # # # #	B5	An, Bn CI An, Bn CI	+CO +Sn 	1.20 1.00 2.58 2.16	0.50 0.92 	1.12 0.96 2.64 2.22	0.50 0.76
9-bit parity generator/ checker PTGEN		37	1 1 1 1 1 1 1 1 1	# # # # # # # # #	B5	A–I	Ev OD	2.40 2.55	1.80 0.50	2.40 2.60	1.08 0.50
Power buffer BUF		1	1	@	A1		+Y –Y	0.60 0.30	0.50 0.50	0.50 0.45	0.50 0.50

RAM

Macro				Delay					
						t_{plh} (ns)		t_{phl} (ns)	
Function and Macro Name	Equiv. Circuit and Symbol	LV	Clamp Level when Open	Input Name	Output Name	t_{olh}	K_{lh}	t_{ohl}	K_{hl}
Single-port RAM		1	#	A0 to Ab–1	O0 to Ob–1	12	0.24	12	0.24
		1	#	R		6		6	
		1	#	W		—		—	
		1	@	G		12		12	
		1	#	I0 to Ib–1		—		—	

Cell Name	Function	Equivalent Gate Count
TRAMS1A	256 W × 9 b (scan func.)	10000
TRAMS2A	128 W × 18 b (scan func.)	10000
TRAMS3A	64 W × 36 b (scan func.)	10000
RAMS1A	256 W × 9 b	10000
RAMS2A	128 W × 18 b	10000
RAMS3A	64 W × 36 b	10000

Dual-port RAM		1	#	A0 to Ab–1, B0 to Bb–1	OA0 to OAb–1, OB0 to OBb-1	12	0.24	12	0.24
		1	#	R,A, RB		6		6	
		1	#	WA, WB		—		—	
		1	@	GA, GB		12		12	
		1	#	IA0 to IAb–1, IB0 to IBb–1		—		—	

Cell Name	Function	Equivalent Gate Count
TRAMD1A	128 W × 9 b (scan func.)	10000
TRAMD2A	64 W × 18 b (scan func.)	10000
TRAMD3A	32 W × 36 b (scan func.)	10000
RAMD1A	128 W × 9 b	10000
RAMD2A	64 W × 18 b	10000
RAMD3A	32 W × 36 b	10000

Single-Port RAM

Features

- One address, one R/W port
- Asynchronous
- Autodiagnosis
- 256 word × 9 bit
  128 word × 18 bit
  64 word × 36 bit

Notes

- Since the address latch (ADD-L, figure 2) is built in, G must be open (automatically pulled high) when it is not used.
- Outputs (O_0–O_{b-1}) are high impedance when read enable (R) is low.
- Change the address while write enable (W) is low only.

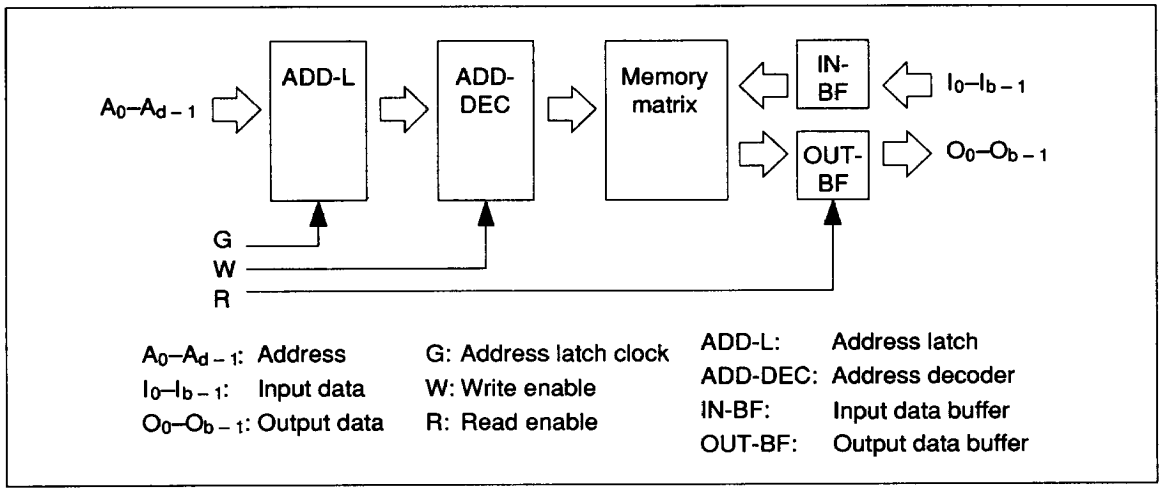


Figure 2 Single-Port RAM Block Diagram

Timing

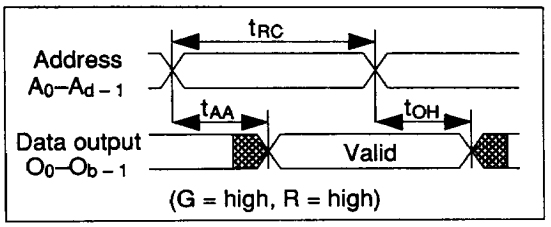


Figure 3 Single-Port Read Cycle Timing

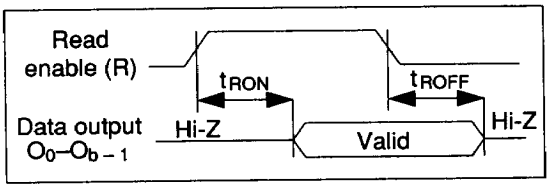


Figure 4 Single-Port Data Output Timing

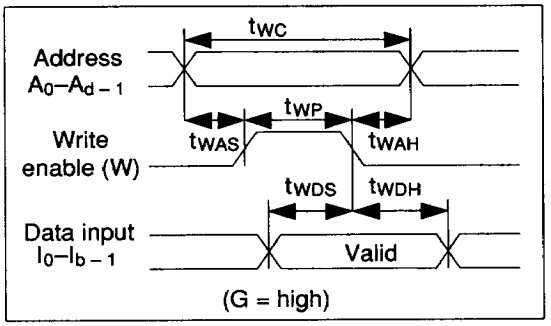


Figure 5 Single-Port Write Cycle Timing

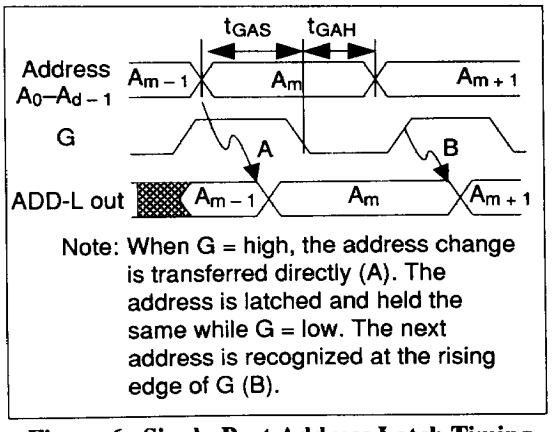


Figure 6 Single-Port Address Latch Timing

Table 6 Single-Port RAM Timing

Item	Symbol	Min	Typ	Max
Read cycle time	t_{RC}	24	—	—
Address access time	t_{AA}	—	12	20
Output data hold time	t_{OH}	1	—	—
Read enable time	t_{RON}	—	6	10
Read disable time	t_{ROFF}	0.8	—	—
Write cycle	t_{WC}	24	—	—
Write pulse width	t_{WP}	10	—	—
Address setup time	t_{WAS}	6	—	—
Address hold time	t_{WAH}	8	—	—
Data setup time	t_{WDS}	10	—	—
Data hold time	t_{WDH}	8	—	—
Address latch setup time	t_{GAS}	4	—	—
Address latch hold time	t_{GAH}	2	—	—

Dual-Port RAM

Features

- Two addresses, two R/W ports
- Asynchronous
- Autodiagnosis
- 128 word × 9 bit
  64 word × 18 bit
  32 word × 36 bit

Notes

- Since the address latch (ADD-L, figure 7) is built in, GA and GB must be open (automatically pulled high) when it is not used.
- Outputs (OA_0–OA_{b-1}/OB_0–OB_{b-1}) are high impedance when read enable (RA/RB) is low.
- You cannot write to the same address from both the A and B ports simultaneously.
- Change the address while write enable (WA/WB) is low only.

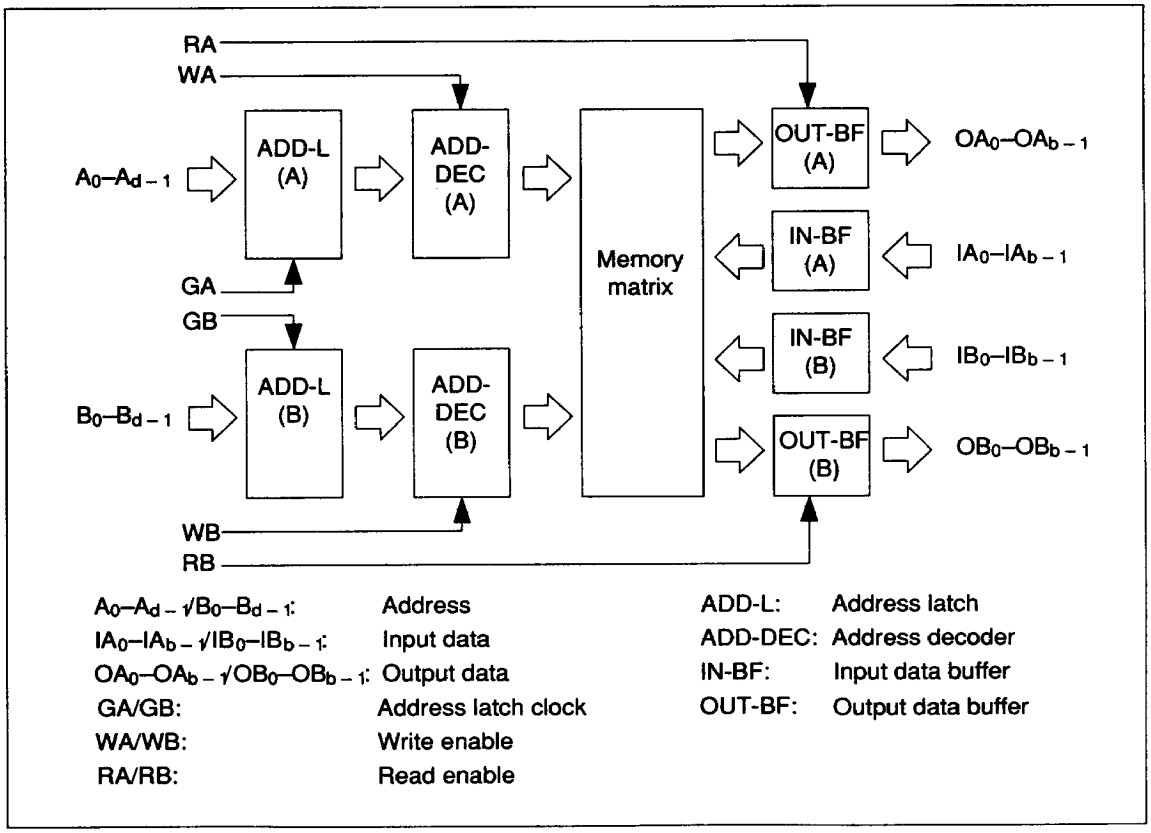


Figure 7 Dual-Port RAM Block Diagram

Timing

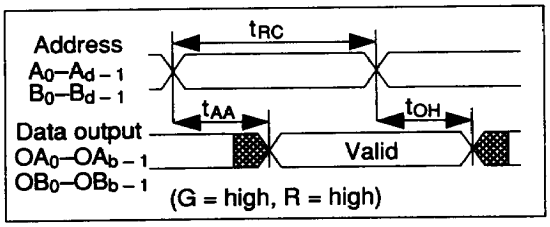


Figure 8 Dual-Port Read Cycle Timing

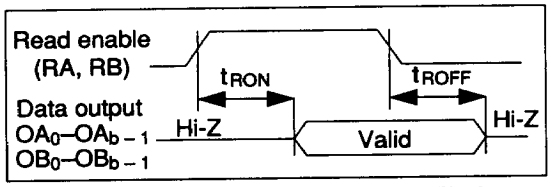


Figure 9 Dual-Port Data Output Timing

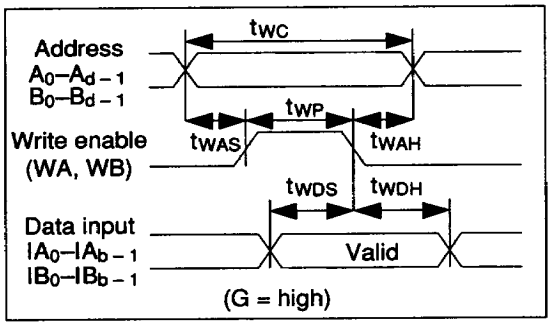


Figure 10 Dual-Port Write Cycle Timing

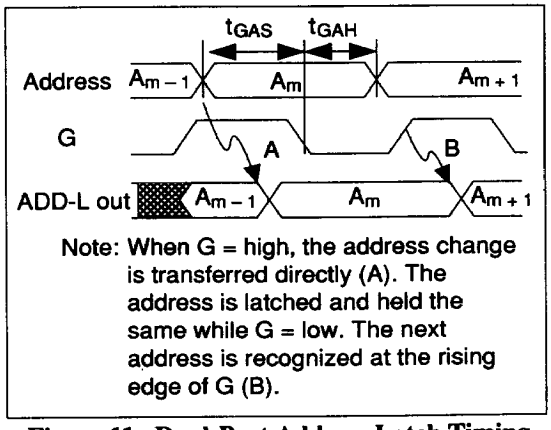


Figure 11 Dual-Port Address Latch Timing

Table 7 Dual-Port RAM Timing

Item	Symbol	Min	Typ	Max
Read cycle time	t_{RC}	24	—	—
Address access time	t_{AA}	—	12	20
Output data hold time	t_{OH}	1	—	—
Read enable time	t_{RON}	—	6	10
Read disable time	t_{ROFF}	0.8	—	—
Write cycle	t_{WC}	24	—	—
Write pulse width	t_{WP}	10	—	—
Address setup time	t_{WAS}	6	—	—
Address hold time	t_{WAH}	8	—	—
Data setup time	t_{WDS}	10	—	—
Data hold time	t_{WDH}	8	—	—
Address latch setup time	t_{GAS}	4	—	—
Address latch hold time	t_{GAH}	2	—	—

Absolute Maximum Ratings

Item		Symbol	Rating	Unit
Supply voltage		V_{CC}	–0.3 to +6.7	V
Terminal voltage	Input	V_{TI}	–0.3 to V_{CC} + 0.3	V
	Output	V_{TO}	–0.3 to V_{CC} + 0.3	V
Output current	Per output	I_O	–32 to +32	mA
	Per V_{CC}/GND	I_{OT}	–70 to +70	mA
Operating temperature		T_{opr}	–20 to +75	°C
Storage temperature	With bias	T_{bias}	–20 to +85	°C
	Without bias	T_{stg}	–55 to +125	°C

Electrical Characteristics

Terminal Capacitance (Ta = 25°C, f = 1 MHz)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Terminal capacitance	C_T	—	—	12.5	pF	V_{IN} = 0 V

Note: Terminal capacitance is sampled and not 100% tested.

Normal Temperature Range (V_{CC} = 5 V ± 5%, Ta = 0°C to +70°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Input voltage (TTL level)	V_{IHT}	2.2	—	V_{CC} + 0.3	V	
	V_{ILT}	–0.3	—	0.8	V	
Input voltage (CMOS level)	V_{IHC}	0.7 × V_{CC}	—	V_{CC} + 0.3	V	
	V_{ILC}	–0.3	—	0.3 × V_{CC}	V	
Schmitt trigger (TTL level)	V_{TT+}	1.5	—	2.5	V	V_{CC} = 5 V
	V_{TT-}	0.5	—	1.5	V	V_{CC} = 5 V
	ΔV_{TT}	0.3	—	—	V	V_{CC} = 5 V
Schmitt trigger (CMOS level)	V_{TC+}	2.8	—	4.0	V	V_{CC} = 5 V
	V_{TC-}	1.2	—	2.4	V	V_{CC} = 5 V
	ΔV_{TC}	0.3	—	—	V	V_{CC} = 5 V
Output voltage (I_{OL} = 2 mA)	V_{OH}	3.5	—	—	V	I_{OH} = –1 mA
	V_{OL}	—	—	0.4	V	I_{OL} = 2 mA
Output voltage (I_{OL} = 8 mA)	V_{OH}	3.5	—	—	V	I_{OH} = –2 mA
	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output voltage (I_{OL} = 12 mA)	V_{OH}		—	—	V	TBD
	V_{OL}	—	—		V	TBD

Normal Temperature Range (cont) (V_{CC} = 5 V ± 5%, Ta = 0°C to +70°C)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Output voltage (I_{OL} = 16 mA)		V_{OH}	3.5	—	—	V	I_{OH} = –8 mA
		V_{OL}	—	—	0.4	V	I_{OL} = 16 mA
Input leakage current		I_{LI}	—	—	1	µA	
Output leakage current		I_{LO}	—	—	1	µA	At high impedance
Pull-up current		I_{PU}	80	220	550	µA	V_{IN} = GND
Pull-down current		I_{PD}	80	220	550	µA	V_{IN} = V_{CC}
Gate delay	Internal	t_{pd}	—	0.3	—	ns	2-input power NAND, FO = 2, Al = 2mm
	Input buffer	t_{pd}	—	1.2	—	ns	FO = 2, Al = 2 mm
	Output buffer	t_{pd}	—	3.5	—	ns	High-speed buffer (OT6), C_L = 50 pF
Power dissipation		I_{CC}	—	40	—	µA/ gate	Internal 2-input power NAND at 10 MHz

Note: Input voltage may change according to the number of synchronously changing output lines or the types of output buffers.

Extended Temperature Range (V_{CC} = 5 V ± 5%, Ta = –20°C to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Input voltage (TTL level)	V_{IHT}	2.4	—	V_{CC} + 0.3	V	
	V_{ILT}	–0.3	—	0.8	V	
Input voltage (CMOS level)	V_{IHC}	0.7 × V_{CC}	—	V_{CC} + 0.3	V	
	V_{ILC}	–0.3	—	0.3 × V_{CC}	V	
Schmitt trigger (TTL level)	V_{TT+}	1.5	—	2.5	V	V_{CC} = 5 V
	V_{TT-}	0.5	—	1.5	V	V_{CC} = 5 V
	ΔV_{TT}	0.3	—	—	V	V_{CC} = 5 V
Schmitt trigger (CMOS level)	V_{TC+}	2.8	—	4.0	V	V_{CC} = 5 V
	V_{TC-}	1.2	—	2.4	V	V_{CC} = 5 V
	ΔV_{TC}	0.3	—	—	V	V_{CC} = 5 V
Output voltage (I_{OL} = 2 mA)	V_{OH}	3.5	—	—	V	I_{OH} = –1 mA
	V_{OL}	—	—	0.4	V	I_{OL} = 2 mA
Output voltage (I_{OL} = 8 mA)	V_{OH}	3.5	—	—	V	I_{OH} = –2 mA
	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA

Extended Temperature Range (V_{CC} = 5 V ± 5%, Ta = –20°C to +75°C) (cont)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Output voltage (I_{OL} = 12 mA)		V_{OH}		—	—	V	TBD
		V_{OL}	—	—		V	TBD
Output voltage (I_{OL} = 16 mA)		V_{OH}	3.5	—	—	V	I_{OH} = –8 mA
		V_{OL}	—	—	0.4	V	I_{OL} = 16 mA
Input leakage current		I_{LI}	—	—	1	µA	
Output leakage current		I_{LO}	—	—	1	µA	At high impedance
Pull-up current		I_{PU}	80	220	550	µA	V_{IN} = GND
Pull-down current		I_{PD}	80	220	550	µA	V_{IN} = V_{CC}
Gate delay	Internal	t_{pd}	—	0.3	—	ns	2-input power NAND, FO = 2, Al = 2 mm
	Input buffer	t_{pd}	—	1.2	—	ns	FO = 2, Al = 2 mm
	Output buffer	t_{pd}	—	3.5	—	ns	High-speed buffer (OT6), C_L = 50 pF
Power dissipation		I_{CC}	—	40	—	µA/ gate	Internal 2-input power NAND at 10 MHz

Note: Input voltage may change according to the number of synchronously changing output lines or the types of output buffers.

Characteristic Curves

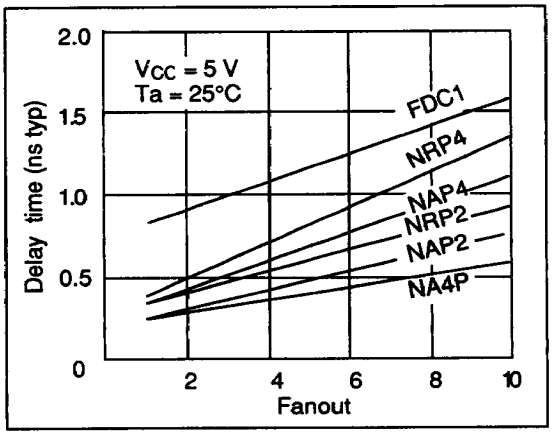


Figure 12 Internal Gate Delay Time

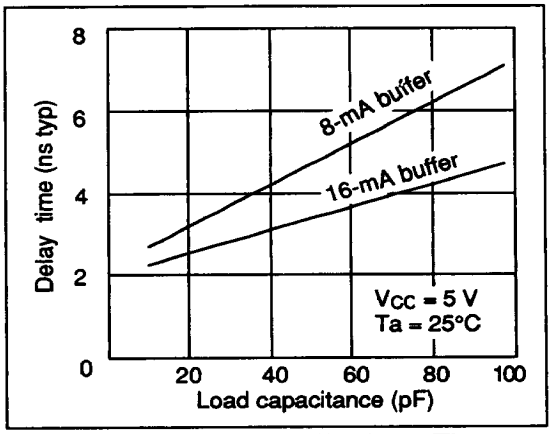


Figure 13 Output Buffer Delay Time

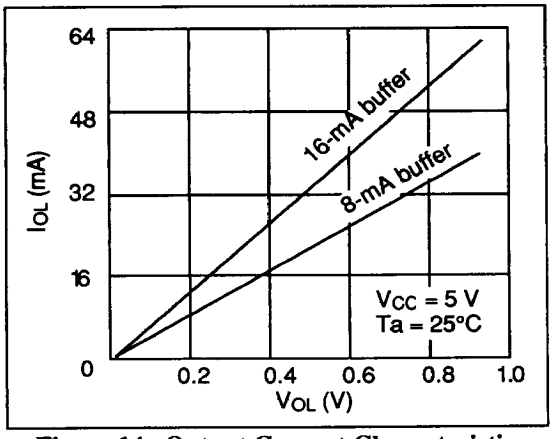


Figure 14 Output Current Characteristics (V_{OL}—I_{OL})

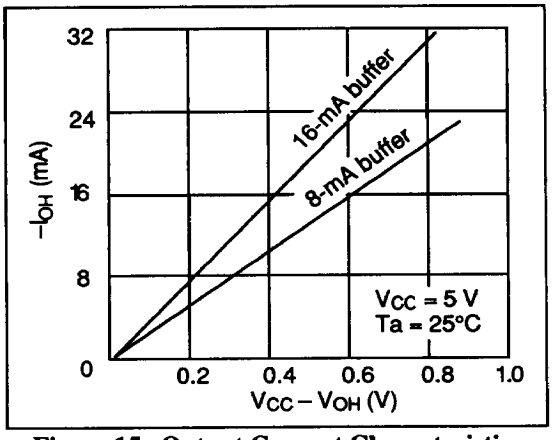
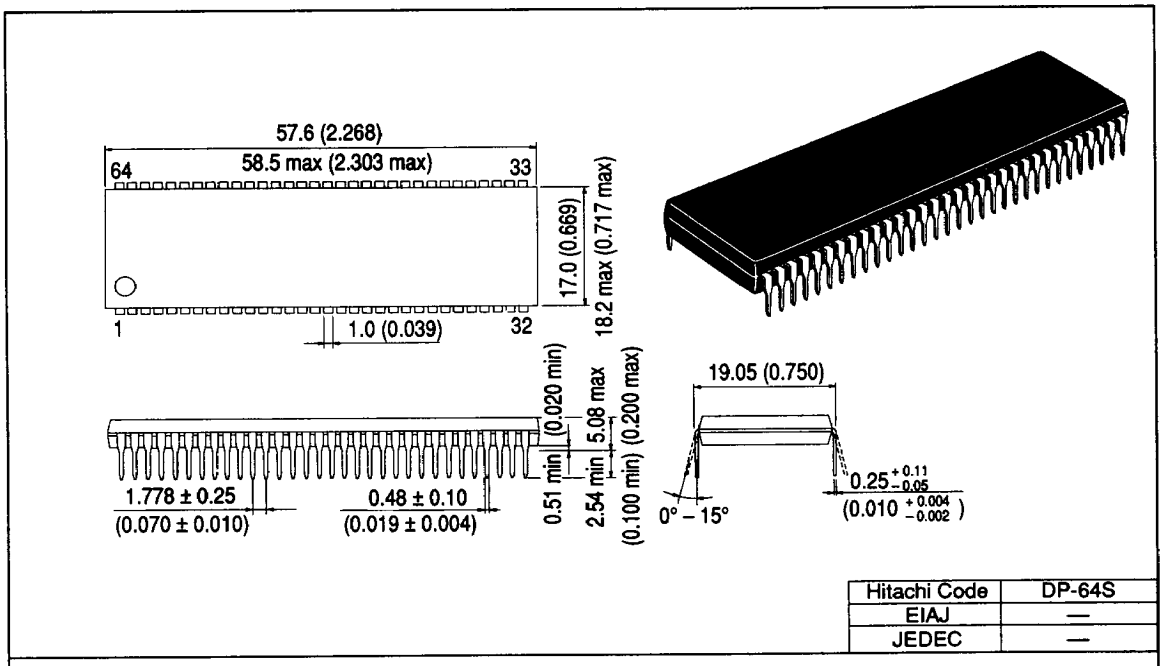


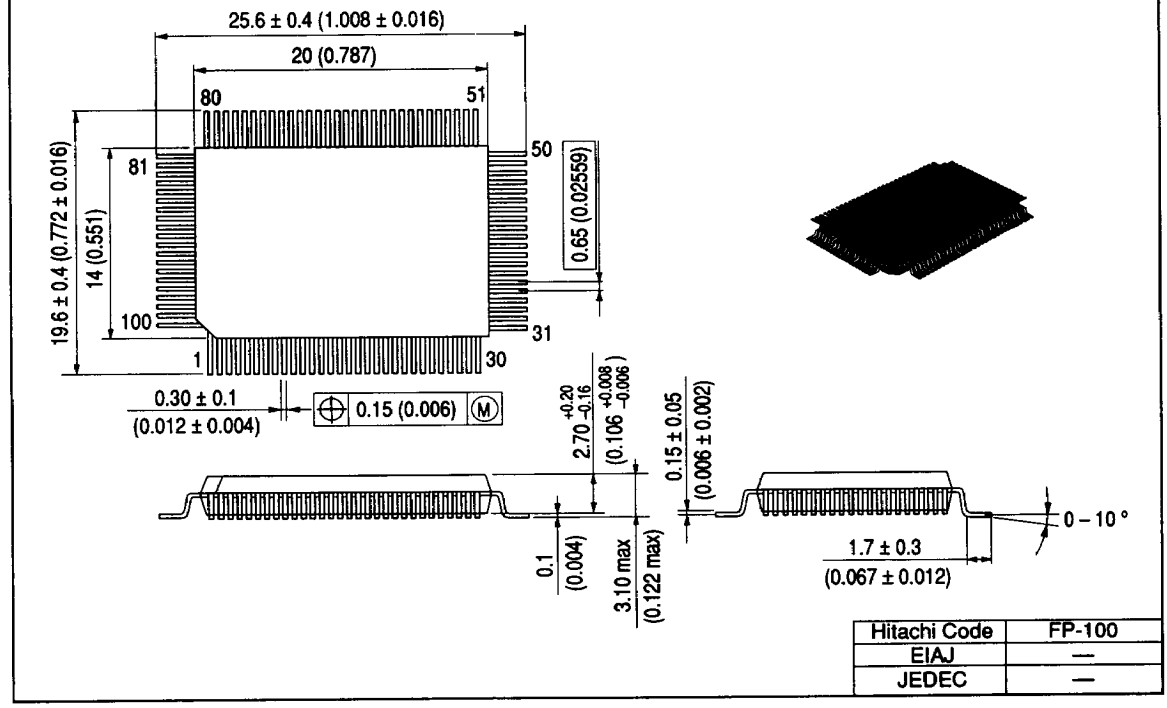
Figure 15 Output Current Characteristics (V_{OH}—I_{OH})

Package Dimensions

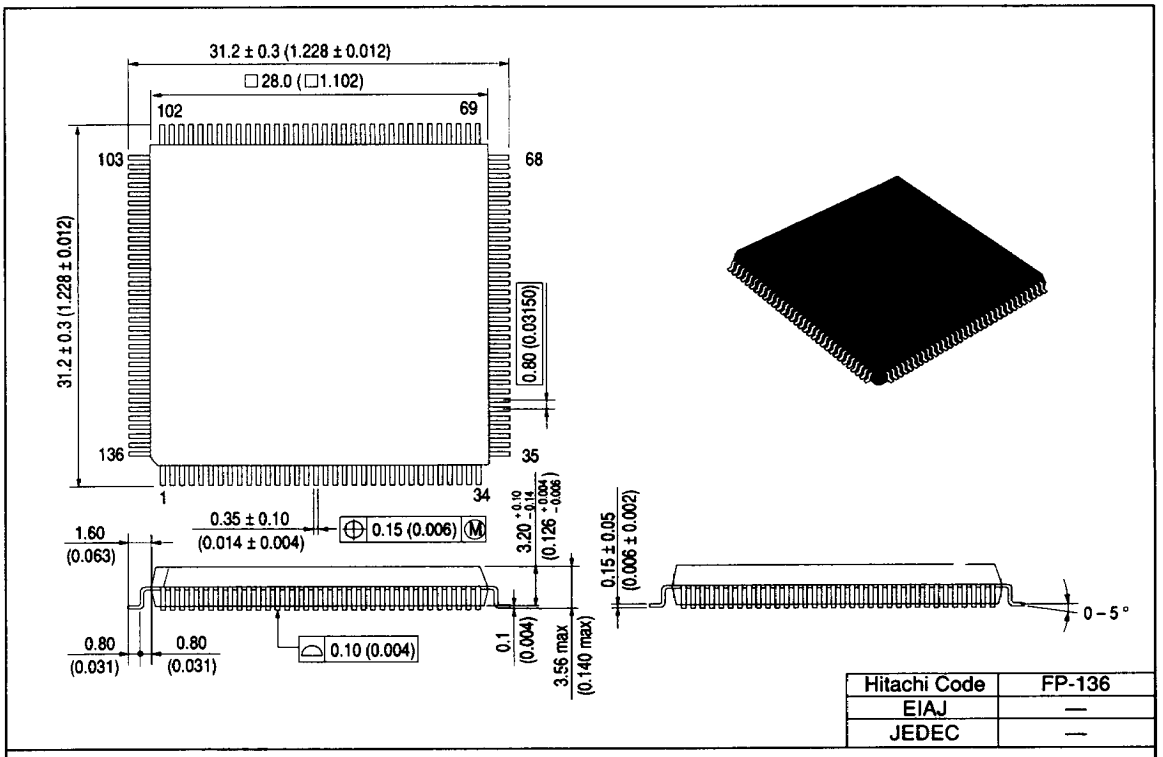
Unit: mm (inch)



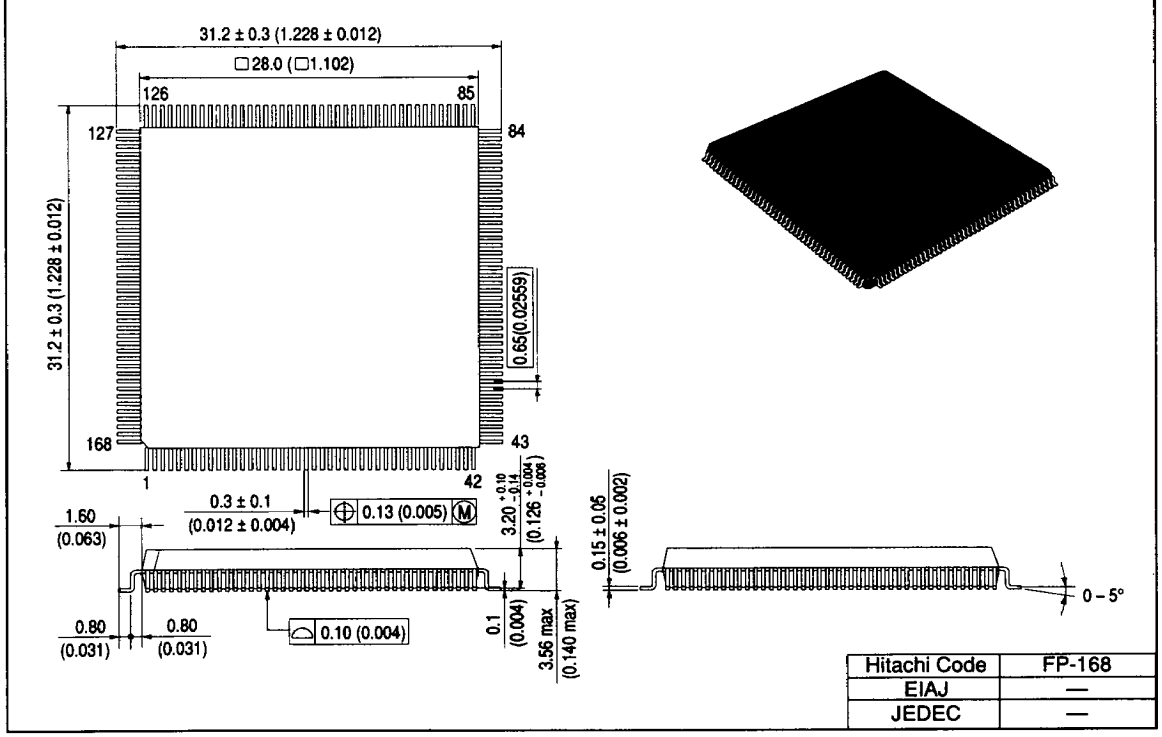
Hitachi Code	DP-64S
EIAJ	—
JEDEC	—



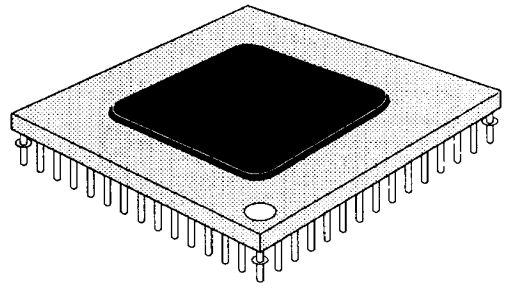
Hitachi Code	FP-100
EIAJ	—
JEDEC	—

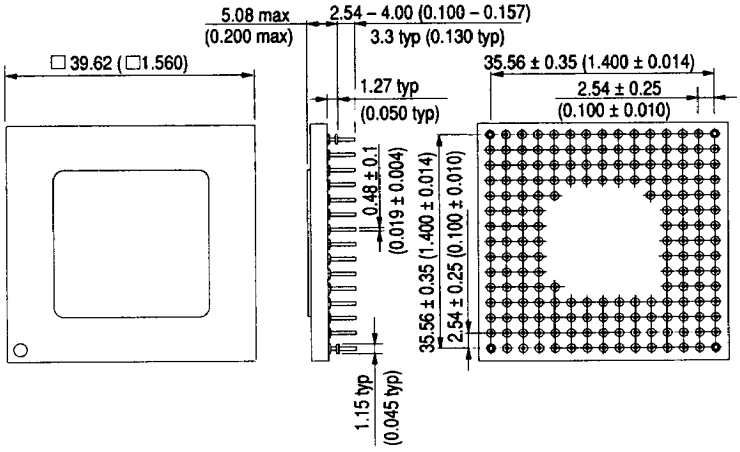


Hitachi Code	FP-136
EIAJ	—
JEDEC	—

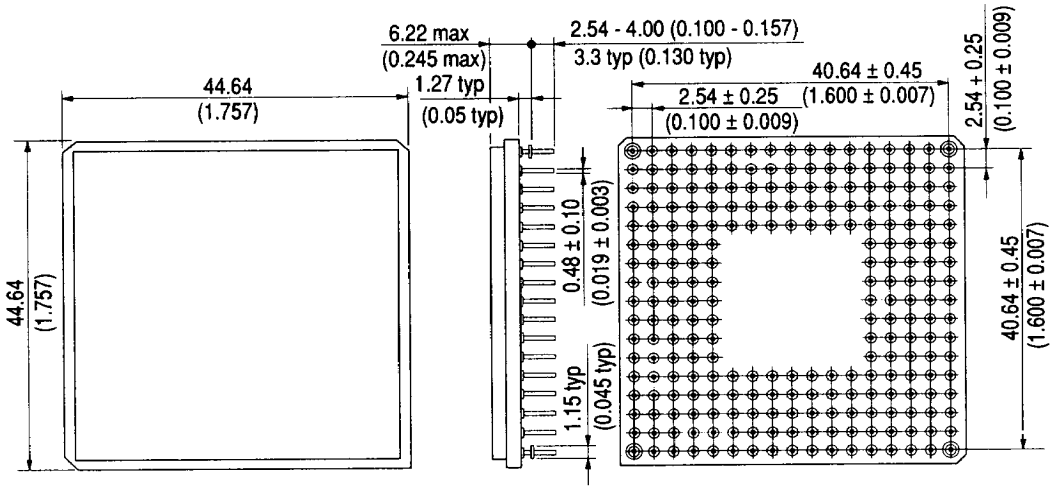


Hitachi Code	FP-168
EIAJ	—
JEDEC	—

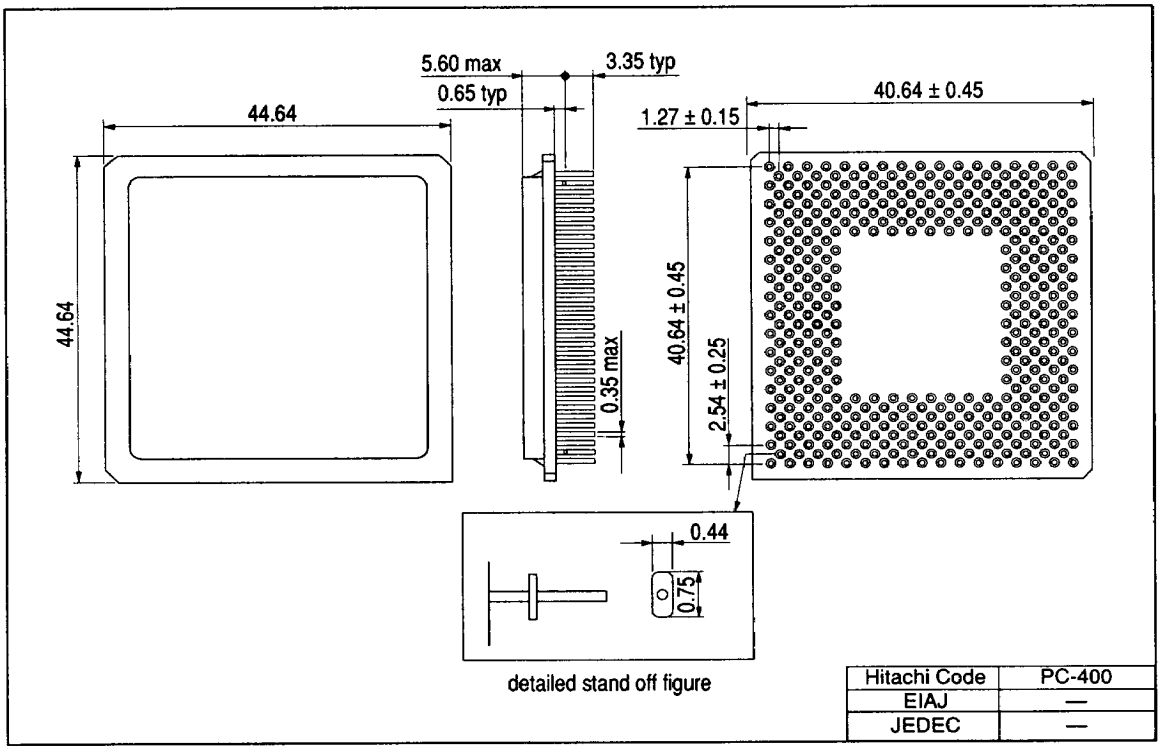




Hitachi Code	PC-179
EIAJ	—
JEDEC	—



Hitachi Code	PC-240
EIAJ	—
JEDEC	—



Hitachi Code	PC-400
EIAJ	—
JEDEC	—