Extended data rate adaptor PCB2325

1. Introduction

The Extended Data Rate Adapter (EDRA) is a CMOS integrated circuit for ISDN applications developed to adapt synchonous and asynchronous user data rates on the CCITT R-interface to a 64 kbit/s data stream and vice versa.

1.1. Features

* Data rate adaption to 64 kbit/s according CCITT V.110/X.30 and ECMA-102 recommendations.

* Synchronous data rates supported:

600, 1200, 2400, 4800, 9600, 19200, 38400, 48000, 56000 and 64000 bit/s.

* Asynchronous data rates supported (using RA0 asynchronous-synchronous conversion):

full duplex with the same rates:

300, 600, 1200, 2400, 4800, 9600, 19200

or full duplex with:

1200/75 and 75/1200 bit/s.

* Asynchronous automatic data rate adaption from 0 upto 19.2 kbit/s using a multiple sampling method with additional transition coding (based on CCITT rec. R.111), for compatibility with its predecessor the PCB2320 DRA. Useful for data rates as:

50, 75, 110, 134.5, 150, 200, 3600, 7200, 12000, 14400 and 19200 bit/s.

* Flexible synchronous data interface, which supports both long and short frame synchronisation, i.e. connectable to:

  -2.048 Mbit/s Terminal highway;
  -SLD interface;
  -IOM interface (not in MPX mode);

* Submultiplexing, according to CCITT rec. I.460, permits upto 8 EDRAs to share one 64 kbit/s channel on the synchronous data interface.

* Serial interface for the DTE/DCE. A complete set of V- or X-series interchange circuits is supported.

* Microcontroller interface with multiplexed data/address lines.

* Built in UART for microcontroller access to both local and remote side of the data channel.

* Local flowcontrol by control of lead 106 or X-ON/X-OFF.

* End to end flowcontrol.

* Inband Parameter Exchange (IPE), according to ECMA-102 recommendation:
  - -unrestricted 64 kbit/s;
  - -restricted 56 kbit/s;
  - -asynchronous RA0;
  - -asynchronous multiple-sampling.

* Network Independent Clocking (NIC) (for synchronous data rates), according to CCITT rec. V.110 and ECMA-102, for the data rates of:

4800, 9600 and 19200 bit/s.

* Automatic speed recognition with aid of the microcontroller for data rates upto 19.2 kbit/s.

* EDRA is usable in an interrupt driven environment (open drain interrupt output).

* Monitoring and clamping of the interchange circuits (by microcontroller).

* Low power (power consumption < 40 mW).

* Powerdown mode (power consumption in powerdown mode < 0.2 mW).

* Maintenance loops.

* Boundary scan test.

* Single 5V supply power.

1.2. Ordering information

TYPE NUMBER	TEMPERATURE RANGE ^{0}C	PACKAGE
PCB2325	-10 .. 75°C	PLCC 44
PCB2325	-10 .. 75°C	DIL 40

1.3. Signal description

1.3.1. PLCC 44 package

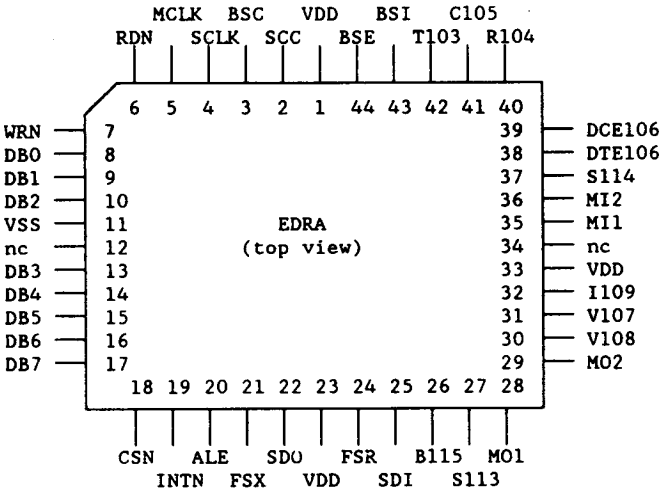


Figure 1.3-1 Pinning diagram (PLCC 44)

1.3.2. DIL 40 package

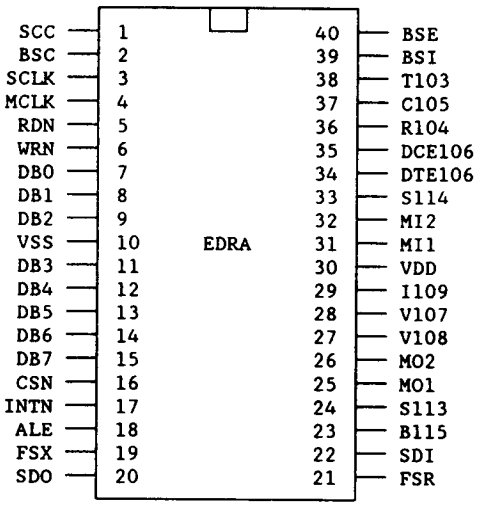


Figure 1.3-2 Pinning diagram (DIL 40)

The signals names which are illustrated in figure 1.3-1 and figure 1.3-2 are now described. The pin numbers refer to the PLCC 44 package (figure 1.3-1) and the pin numbers between brackets refer to the DIL 40 package (figure 1.3-2).

1		VDD	Power supply connection +5V.
2	(1)	SCC	Scan Control input. Together with BSI (pin 43 (39)) and BSE (pin 44 (40)) the test-mode of the EDRA is determined.
3	(2)	BSC	Boundary scan clock input.
4	(3)	SCLK	Synchronous interface clock input (64 kHz - 2.048 MHz). SCLK determines the data rate on the synchronous data interface.
5	(4)	MCLK	Master clock input (2.048 MHz).
6	(5)	RDN	Read Not input (active low). Data is set on the μC-bus by EDRA (if selected by CSN), after the trailing edge of RDN.
7	(6)	WRN	Write Not input (active low). The μC writes data into the EDRA (if selected by CSN). Data is latched on the leading edge of WRN.
8	(7)	DB0	Data/address line 0 (LSB).
9	(8)	DB1	Data/address line 1.
10	(9)	DB2	Data/address line 2.
11	(10)	VSS	Ground
12		n.c.	Not connected
13	(11)	DB3	Data/address line 3.
14	(12)	DB4	Data/address line 4.
15	(13)	DB5	Data/address line 5.
16	(14)	DB6	Data/address line 6.
17	(15)	DB7	Data/address line 7 (MSB).
18	(16)	CSN	Chip Select input (active low).
19	(17)	INTN	Interrupt output (active low, open drain).
20	(18)	ALE	Address Latch Enable input. Indicates that the combined data/address bus contains an address.

21 (19)	FSX	Transmit Frame Select input. FSX aligns every 125 μs the 8 data bits on SDO (pin 22 (20)).
22 (20)	SDO	Synchronous Data output. Data output of the synchronous data interface.
23	VDD	Power supply connection +5V.
24 (21)	FSR	Receive Frame Select input. FSR aligns every 125 μs the 8 data bits for the EDRA on SDI (pin 25 (22)).
25 (22)	SDI	Synchronous data input. Serial data input of the synchronous data interface.
26 (23)	B115	Byte timing (B) or receiver element timing output. Signal B is a CCITT X-series defined control signal. This circuit provides the DTE the byte timing signal. The output pin B indicates the last bit of a data-byte. It will be HIGH during one period of S114 (pin 37 (33)) and will be LOW within the byte-period. Receiver element timing output. Circuit 115 (V-series) generates the data element clock for circuit R104 (pin 40 (36)).
27 (24)	S113	Transmitter element timing input (provided by the DTE). S113 provides the data element timing for T103 (pin 42 (38)).
28 (25)	MO1	Multifunctional output 1.
29 (26)	MO2	Multifunctional output 2.
30 (27)	V108	Data Terminal Ready input. Indicates that the associated terminal is ready to receive and transmit data.
31 (28)	V107	Data Set Ready output. Indicates that to the terminal that the EDRA is ready to receive data. Output V107 indicates the state of the remote subscribers V108 circuit.
32 (29)	I109	Data channel received line signal detector/indication. Output which indicates the state of the remote subscribers C105 circuit. Under control of the μC, I109 can be made byte-timing synchronous. This pin is in boundary test mode boundary scan output.
33 (30)	VDD	Power supply connection +5V.
34	n.c.	Not connected.
35 (31)	MI1	Multifunctional input 1.
36 (32)	MI2	Multifunctional input 2.

37 (33) S114 Transmitter element timing output. In synchronous mode S114 generates the data element clock for circuit T103 (pin 42 (38)).

38 (34) DTE106 Request To Send input (EDRA=DTE).

39 (35) DCE106 Request To Send output. Output which indicates the state of the remote subscribers DTE106 circuit.

40 (36) R104 Received data output. R104 provides circuit 104 for V- and R for X-series of interfaces. Circuit R104 will be shifted out every trailing edge of S114 (pin 37 (33)).

41 (37) C105 For V-series, C105 performs as circuit 105, for X-series as circuit C. C105 is a signalling channel which corresponds with I109 of the remote subscriber.

42 (38) T103 Transmit data input. Transmit input has to be connected to the transmit (T for X-, circuit 103 for V-series) output of the DTE equipment. For synchronous speeds T103 will be sampled at every leading edge of B115 (pin 26 (23)).

43 (39) BSI Boundary scan input.

44 (40) BSE Boundary scan enable.

2. Functional description

2.1. General description

The EDRA adapts synchronous and asynchronous user data rates on the so called R-interface fully in accordance to CCITT rec. X.30/V.110 and ECMA-102 recommendations to a 64 kbit/s channel (ISDN B-channel) and vice versa.

To be compatible with the EDRAs predecessor, the PCB2320 Data Rate Adapter (DRA) also multiple sampling is used. Asynchronous user data rates from 0 upto 19.2 kbit/s on the R-interface are also supported using the multiple sampling method with additional transition coding based on CCITT rec. R.111. With this multiple sampling method it is possible to convert every asynchronous user data rate to a 64 kbit/s data stream without the need of programming the EDRA for the specific user data rate of the DTE.

Network independent clocking is supported by the EDRA. It allows the EDRA to be connected to a synchronous modem with a data rate upto 19.2 kbit/s not locked to the user data rate of the EDRA without loss of data.

In order to provide a means to transfer data by μC to the remote EDRA, an IPE exchange mode is implemented. In this mode the μC can access the 64 kbit/s channel to transmit data to and receive data from the remote EDRA.

To be able to communicate with the DTE the μC connected to the EDRA can be connected to the R-interface. In this way the μC can demand the DTE for call setup information.

The conversion between user data rates and the 64 kbit/s data rate takes place RA0, RA1 and RA2 adaption stages as decribed in the CCITT X.30 and V.110 and ECMA-102 recommendations. The RA0 adaption stage performs the asynchronous-synchronous conversion, while the RA1 and RA2 adaption stage perform the conversion between a synchronous data rate (or synchronous data from the RA0 stage) to 64 kbit/s. In figure 2.1-1 a survey is given of the different data paths within the EDRA.

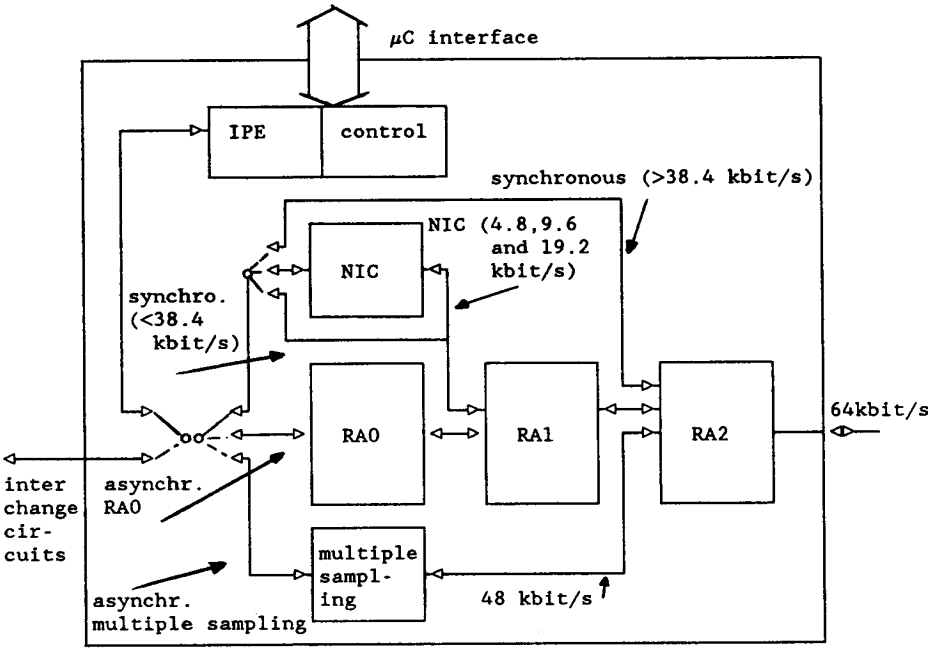


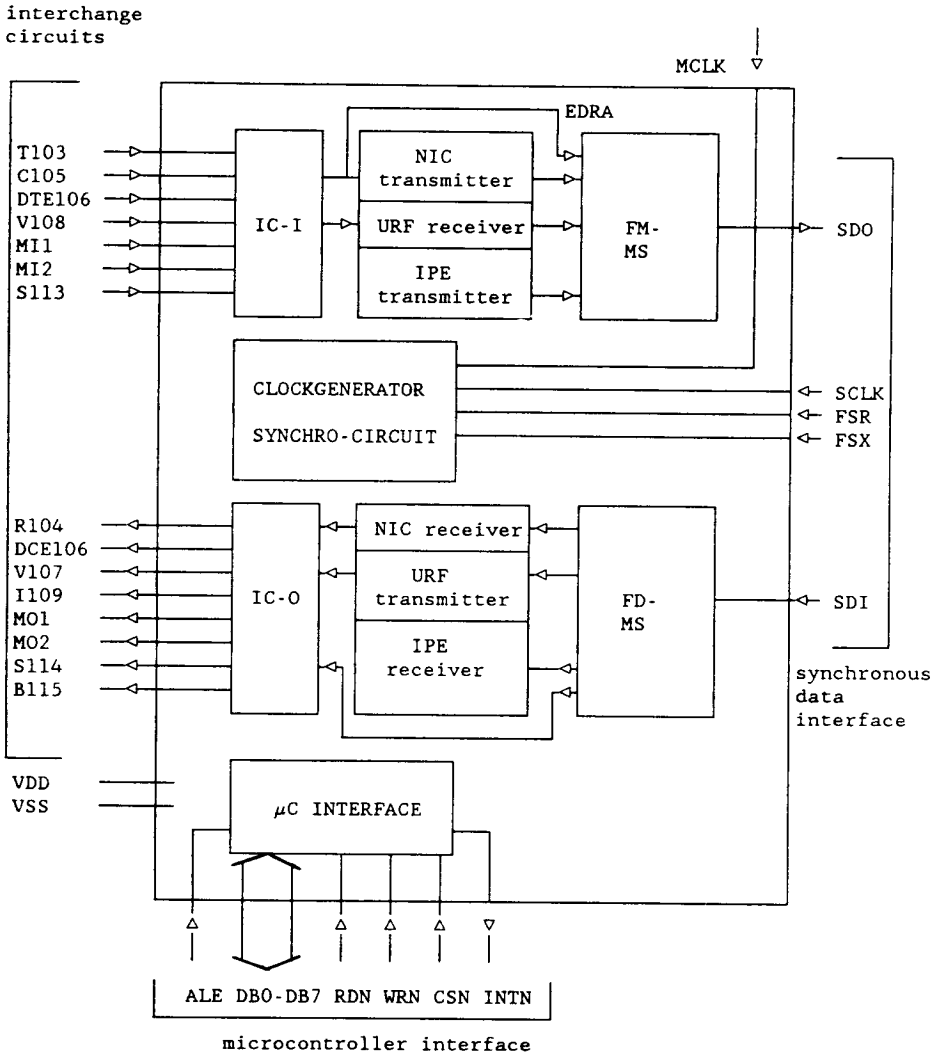
Figure 2.1-1 Data paths within the EDRA

In the EDRA different functional blocks can be distinghuised. These blocks are illustrated in blockdiagram 2.1-2.

A brief description of the interfaces of the EDRA is given before the functional blocks are described. In blockdiagram 2.1-2 three interfaces can be destinguished:

*The interchange interface. A set of V-type interchange circuits: 103, 104, 105, 106, 107, 108, 109, 113, 114, 115 and two multifunctional input and two multifunctional outputs or X-type data interface interchange circuits: T, R, C, I, S and B can be connected to the EDRA via level converters. This interchange interface is described in section 2.3.

*The synchronous data interface can have a transmission rate between 64 kbit/s and 2.048 Mbit/s. The interface consists of two unidirectional data lines (SDI and SDO), a clock line (SCLK) determining the transmission rate on this interface, a frame select transmit signal (FSX) and frame select receive signal (FSR) which indicate the transmit and receive timeslot on the synchronous data interface. The synchronous data interface is described in section 2.4.



All the blocks in the EDRA are controlled via the µC interface and receive their timing from the clock generator/synchronisation circuit.

Figure 2.1-2 Block diagram of the EDRA.

*The 8 bit microcontroller interface is a data/address multiplexed microcontroller interface. The microcontroller interface performs the interface for the control stages of the EDRA. The EDRA can be programmed and monitored via the microcontroller interface. The settings of the EDRA can be programmed in a set of write registers. The following settings can be programmed:

- selection of functional mode
- data rate setting
- the mapping scheme (interchange circuits to S- and X-bits)
- clamping of interchange circuits
- testloop selection
- communications control via UART
- interrupt masking
- 64 kbit/s channel framing and synchronisation control
- setting UART/flow control parameters

The EDRA can be monitored by reading out the read registers. The following functions can be read out:

- in/out synchronisation-indication
- activity check on interchange circuits
- readout logic state of interchange circuits.
- readout of the interrupt source.
- readout the UART

The microcontroller interface description and the detailed description of the registers is provided in section 2.9.

*Clock generator and synchronisation circuit

The clock generator and synchronisation circuit provides all internal clocks of the EDRA. It generates i.e. the baud rates on circuits S114 and 115 and provides byte timing on circuit B. (B and 115 are physically one circuit, but can be switched by the microcontroller). The baudrate on the interchange interface can be selected with register W01, see section 2.9.1.2.

*Interchange circuits (inputs/outputs) (IC-I/IC-O)

The interchange circuit (input and output) blocks (IC-I and IC-O) interface with the connected data equipment. All interchange circuits can be monitored via the μC-interface. Via this block, the mapping of the interchange circuits to the S- and X-bits in the frame on the synchronous data interface can be chosen. A detailed desciption of these blocks is given in section 2.3.

*Frame mapping and demapping block and multiple-sampling coding/decoding (FM-MS/FD-MS)

The translation between synchronous user data rates and the 64 kbit/s channel takes place in the frame mapping block (FM in figure 2.1-2) while the reverse action is performed by the frame demapping block (FD). These blocks perform the RA1 and RA2 stages as described in CCITT rec. X.30/V.110 and ECMA-102. The asynchronous to synchronous conversion according to the multiple sampling method with additional transition coding is also performed in the frame mapping/demapping block. A detailed description of the frame mapping/demapping block is given in section 2.8.

*URF transmitter/receiver

URF transmitter/receiver block is a combination of three functions, UART, RA0 adaption stage (according ECMA-102 and CCITT rec. V.22), flow-control (FLC). A detailed description of the URF transmitter/receiver is given in section 2.5.

*IPE transmitter/receiver

The Inband Parameter Exchange (IPE) function is discussed in 2.6.

*Network independent clocking transmitter/receiver

The NIC block allows the EDRA to be connected to a synchronous modem with a data rate of 4800, 9600 or 19.2 kbit/s. A detailed description of the NIC function is given in section 2.7.

2.2. Modes of operation

The EDRA can be used in three different modes of operation (illustrated in figure 2.2-1) which can be programmed by the microcontroller:

* Transmission-mode 1: Local DTE to remote DTE.

  - -1A: synchronous, data rate adaption according to CCITT rec. V.110 or X.30 (V.110 (asynchronous or bit synchronous) or X.30 mode (byte-synchronous) can be selected);
  - -1B: asynchronous with the RA0 coding;
  - -1C: asynchronous with flow control;
  - -1D: asynchronous with multiple sampling and additional transition coding. In this mode the break character can be filtered out by microcontroller and user data can be read out via the microcontroller interface.

* Transmission-mode 2: Local DTE to local microcontroller.

  In this mode, the microcontroller can communicate to the DTE/DCE via the UART. Only asynchronous transmission is possible. the URF will be used as asynchronous receiver transmitter (the UART function).

* Transmission-mode 3: Local microcontroller to 64 kbit/s channel.

-3A: asynchronous, the 64 kbit/s channel data will be coded according the multiple sampling method. the URF will be used as asynchronous receiver transmitter (the UART function);
-3B: asynchronous, IPE mode with RA0 coded data in 64 kbit/s channel. the URF will be used as asynchronous receiver transmitter (the UART function);
-3C: synchronous, IPE mode with 64 or 56 kbit/s data rate in the 64 kbit/s channel, The microcontroller uses the UART for parallel-serial conversion and the data in the 64 kbit/s channel will be coded according to the selected mode (56 or 64 kbit/s).

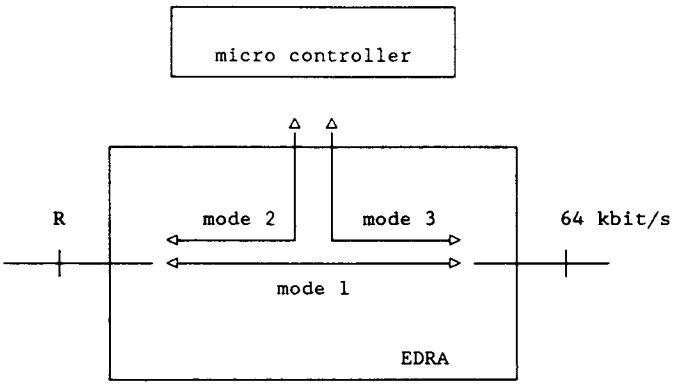


Figure 2.2-1 The three transmission modes of the EDRA

2.3. Interchange circuits

The interchange interface of the EDRA connects to level converters which then connect to the DTE (or DCE) (see figure 2.3-1). The interchange interface consists of:

*T103 :Circuit 103 (V-series), Transmitted Data.
T (X-series), Transmit.

*R104 :Circuit 104 (V-series), Received Data.
R (X-series), Receive.

*C105 :Circuit 105 (V-series), Request To Send.
C (X-series), Control.

*DTE106 :Circuit 106 (V-series), Clear To Send (the EDRA is DTE).

*DCE106 :Circuit 106 (V-series), Clear To Send (the EDRA is DCE).

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*V107       :Circuit 107 (V-series), Data Set Ready.

*V108       :Circuit 108 (V-series), Data Terminal Ready.

*I109       :Circuit 109 (V-series), Data channel received line signal
             detector.
             I (X-series), Indication.

*S113       :Circuit 113 (V-series), Transmit signal element timing (from
             DTE).
             S (X-series), Signal element timing.

*S114       :Circuit 114 (V-series), Transmit signal element timing (from
             DCE).
             S (x-series), Signal element timing.

*B115       :Circuit 115 (V-series), Receiver signal element timing.
             B (X-series), Byte timing.

*MO1        :Multifunctional output 1.

*MO2        :Multifunctional output 2.

*MI1        :Multifunctional input 1.

*MI2        :Multifunctional input 2.
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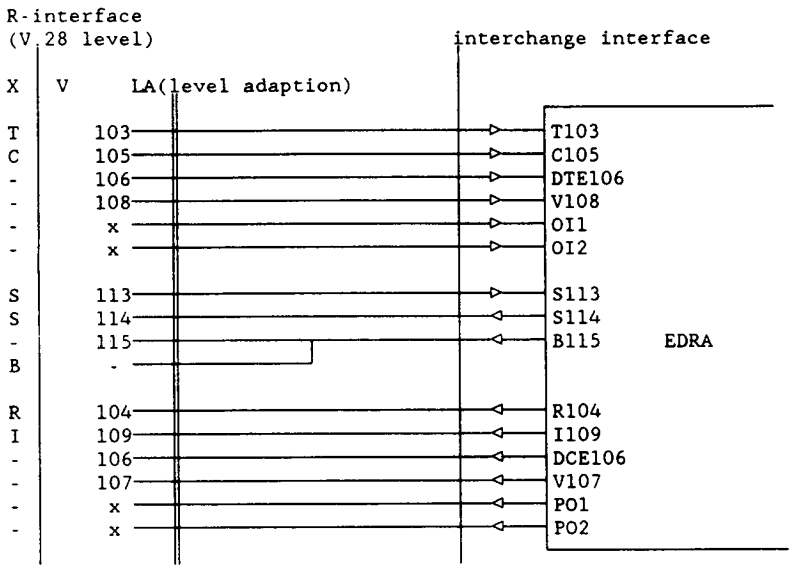


Figure 2.3-1 The interchange interface.

2.3.1. Mapping of the interchange circuits in Data, S- and X-bits

ECMA and CCITT specify the interchange circuits that should be mapped into the frame used in the 64 kbit/s channel. In the EDRA the mapping of interchange circuits into the 64 kbit/s channel can be performed in three ways (see register W00, section 2.9.1.1):

-V.110 mode: in this mode the EDRA is asynchronous or bit synchronous but not byte synchronous (see section 2.3.3).
-X.30 mode: in this mode the EDRA is byte synchronous (see section 2.3.3).

-μC mode: in this mode the S- and X-bits in the frame can be set and read by μC.

For user data rates $\leq$ 38.4 kbit/s a 10 bytes multiframe is used (see section 2.8.2 and appendix B for the description of this frame). Table 2.3.1-1 shows the mapping of interchange circuits in the bits of the 10-bytes multiframe.

	local subscriber	frame bits	remote subscriber
V.110 mode	V108 C105 frame sync/DTE106 T103	S1,S3,S6,S8 S4,S9 X2,X7 D1 - D48	V107 I109 DCE106 R104
X.30 mode	C105 frame sync/DTE106 T103	SP, SQ, SR X2, X7 P1 - R8	I109 DCE106 R104
μC-mode	register W07	S1,X2,S3,S4,S6,X7, S8,S9	register R24 (bit 0-7)

Table 2.3.1-1 Mapping of interchange circuits for user data rates ≤ 38.4 kbit/s.

For the user data rate of 48 kbit/s a four bytes frame is used (see section 2.8.2 and appendix B for the description of this frame). In table 2.3.1-2 the mapping of the interchange circuits in the bits of the 4 bytes frame is illustrated.

For a user data rate of 56 kbit/s only one S-bit is available (in the 4 bytes frame) to transmit one interchange circuit. The mapping of the interchange circuits for the user data rate of 56 kbit/s is illustrated in table 2.3.1-3 (see section 2.8.2 and appendix B for a description of this frame).

	local subscriber	frame bits	remote subscriber
V.110 mode	V108 C105 frame sync/DTE106 T103	S1,S3 S4 X2 D1 - D24	V107 I109 DCE106 R104
X.30 mode	C105 frame sync/DTE106 T103	SP, SQ, SR X2 P1 - R8	I109 DCE106 R104
μC-mode	register W07 (S6-S9 not relevant)	S1,X2,S3,S4	register R24 (bit 0-3)

Table 2.3.1-2 Mapping of interchange circuits for a user data rate of 48 kbit/s.

	local subscriber	frame bits	remote subscriber
X.30 mode	C105 T103	S D1 - D28	I109 R104
µC-mode	the S bit wil not be influenced by W07 in the µC-mode, the S bit is directly coupled to lead C105.		
	clamping of C105	S	register R24, bit 0

Table 2.3.1-3 Mapping of interchange circuits for a user data rate of 56 kbit/s.

2.3.2. Relation between ON/OFF and their binary values

In the december '84 ECMA specification, the binary values of S- and X-bits in the data stream on the synchronous data interface are given related to ON or OFF conditions of the interchange circuits:

For the S- and X-bits, a zero corresponds with the ON condition, a one with the OFF condition.

In the september '84 ECMA report this definition was reverse: zero corresponds with OFF, a one with ON.

To meet both definitions (and so to be upwards compatible with the DRA), both definitions can be selected in registers W5/W10 (section 2.9.1). When the EDRA is connected to a DRA, the EDRA must code the S- and X-bits according the september ECMA definition. When other networks are involved, the EDRA must be V.110 compatible (december '84 ECMA definition) and can not cooperate with the DRA anymore. In figure 2.3.2-1 the relation between the signals on the interchange circuits and the signals on the EDRA pins are depicted.

Signal	V.28 level <= -3V	V.28 level >= 3V	comment
T103	1	0	Condition 0 on V.28 level = condition 0 in the data bits on the SD interface.
R104	1	0	Condition 1 on V.28 level = condition 1 in the data bits on the SD interface.
C105	OFF	ON	Condition ON on V.28 level = condition 0 in the S- and X-bits on the SD interface (V.110 mode).
DTE106	OFF	ON	Condition OFF on V.28 level = condition 1 in the S- and X-bits on the SD interface (V.110 mode).
DCE106	OFF	ON	
V107	OFF	ON	
V108	OFF	ON	Condition ON on V.28 level = condition 1 in the S- and X-bits on the SD interface (DRA-mode).
I109	OFF	ON	
S113	OFF	ON	
S114	OFF	ON	Condition OFF on V.28 level = condition 0 in the S- and X-bits on the SD interface (DRA-mode)
B115	OFF	ON	

Table 2.3.2-1 Relation between the signals on the interchange circuits and the signals on the EDRA.

2.3.3. Functional timing relations

In X.30 mode, the byte timing interchange circuit B is provided for character alignment (pin B115). Circuit C (pin C105) is sampled together with bit 8 of the preceeding character (on T103). The timing of the outgoing interchange circuits is related to this byte timing signal. Circuit I (pin I109) is changing its state at the boundaried between old and new character at circuit R (pin R104). In figure 2.3.3-1 the relation in timing between the interchange circuits is depicted. The receiver block provides byte- and bit-synchronisation, and delaying of circuits I and R, to fit the byte-timing for X.21 interfaces.

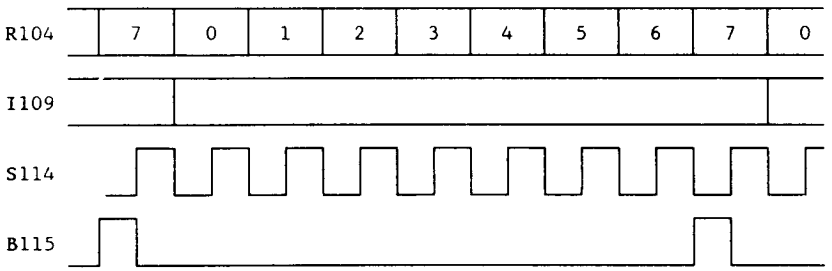


Figure 2.3.3-1 Byte timing relation between data and S bits.

In appendix A the sampling moments and the moment of state changes of the interchange circuits in X.30 mode are depicted for the 4 bytes frame and the 10 bytes multiframe (see also section 2.8.2).

In V.110 mode the receiver data (on pin R104) is not byte synchronous with the transmitter data (T103). The received S-bits are related to databits as follows depicted in table 2.3.3-2.

S-bit	D-bit
S1	D8
S3	D16
S4	D24
S6	D32
S8	D40
S9	D48

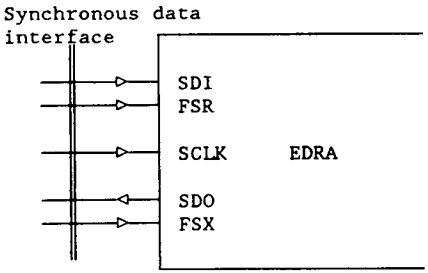
Table 2.3.3-2 Coordination of S-bits to D-bits.

In appendix A the sampling moments and the moment of state changes of the interchange circuits in V.110 mode are illustrated for the 4 bytes frame and the 10 bytes multiframe (see also section 2.8.2).

2.4. Synchronous data interface

The synchronous data interface (illustrated in figure 2.4-1) consists of :

- SDI: Synchronous data input;
- SDO: Synchronous data output;
- SCLK: Data element clock (64 kHz - 2.048 MHz);
- FSR: Receive frame select;
- FSX: Transmit frame select.



2.4-1 Synchronous data interface.

The synchronous data interface can operate between at a data rate between 64 kbit/s and 2.048 Mbit/s. The synchronous data interface operates in short synchronisation mode. However, a long synchronisation signal may be used if a minimal off-time Tw is taken into account (see figure 2.4.1-1 and section 3.3).

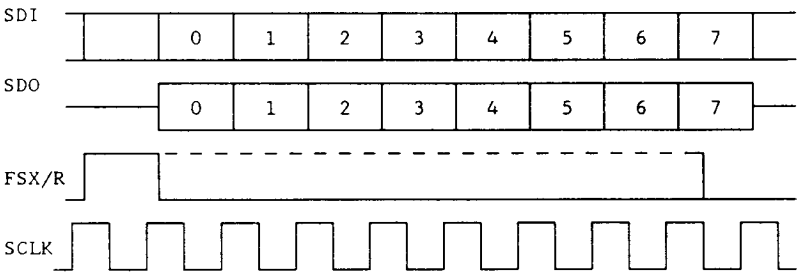


Figure 2.4.1-1 Synchronous data interface functional timing.

The last data rate adaption stage, RA2, converts intermediate rates from the RA1 adaption stage to the 64 kbit/s data rate (see section 2.8.2). Instead of the adaption from the intermediate rate to the 64 kbit/s data rate, the intermediate data rate can be placed in a part of the 64 kbit/s channel of the synchronous data interface. This means that for an intermediate rate of 8 kbit/s (user data upto 4.8 kbit/s) only the one of the eight bits of the timeslot is used and eight EDRAs can be (time division) multiplexed in one 64 kbit/s channel. For an intermediate rate of 16 kbit/s, four EDRAs can share the same 64 kbit/s channel and for an intermediate rate of 32 kbit/s two EDRAs.

Via the microcontroller interface the selection of the bit position that will be occupied in the 64 kbit/s bitstream can be chosen: an 8 kbit/s intermediate bitstream may occupy any bit position, a 16 kbit/s intermediate stream occupies bit positions (0,1) or (2,3) or (4,5) or (6,7), a 32 kbit/s intermediate stream occupies bit positions (0,1,2,3) or (4,5,6,7); the bit position selections can be made in register W03 (section 2.9.1.4).
The order of transmission of the bits at each intermediate rate will be identical at transmitter and receiver. The highway output will 3-state all unused bits, this to enable another EDRA to transmit data in the same timeslot on the synchronous data interface.

2.5. URF transmitter/receiver

URF transmitter/receiver performs three functions, UART, RA0, flow-control (FLC). In figure 2.5-1 the URF transmitter/receiver block is illustrated. In this figure the data streams for the different operational modes of the EDRA (as discussed in section 2.2) are shown. In addition to figure 2.5-1 the URF transmitter and receiver are shown in more detail in figure 2.5-2 and figure 2.5-3. The different functions of the URF transmitter/receiver are discussed in the following sections.

Extended data rate adaptor PCB2325

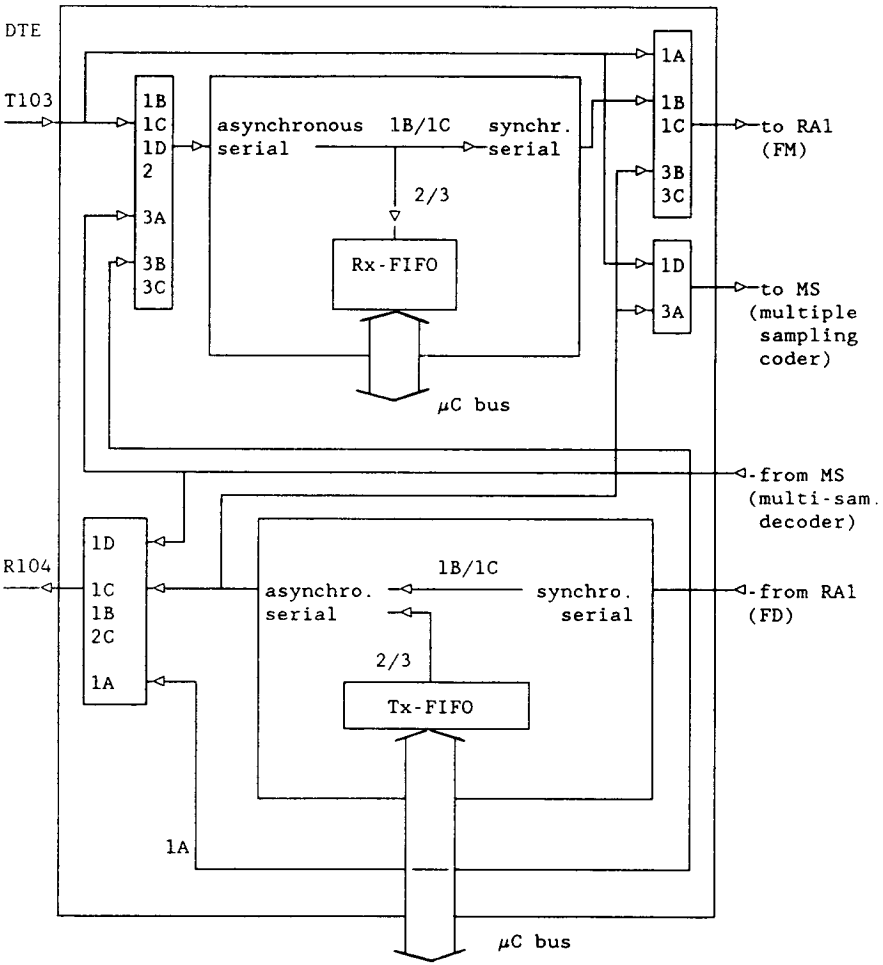


Figure 2.5-1 The URF transmitter/receiver.

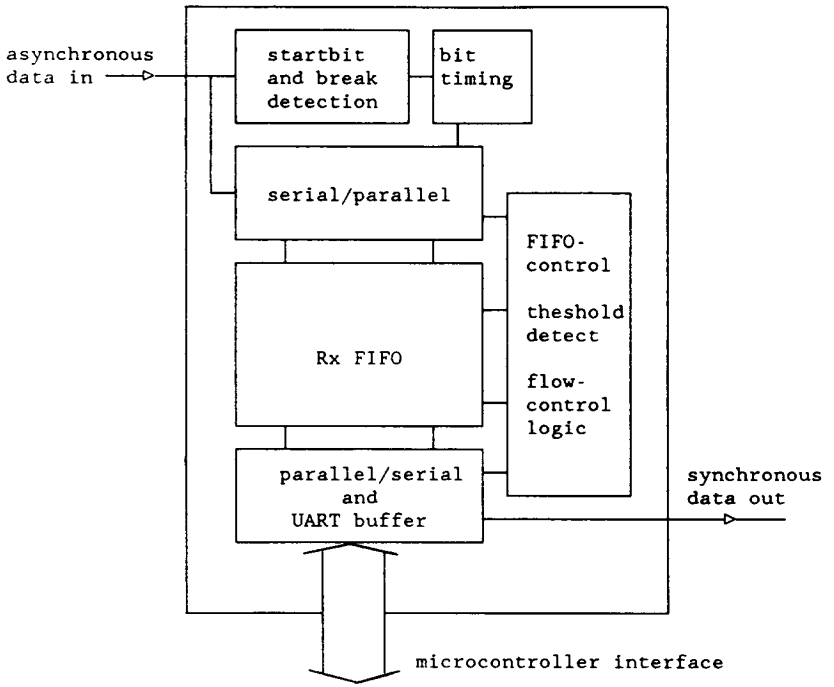


Figure 2.5-2 URF receiver

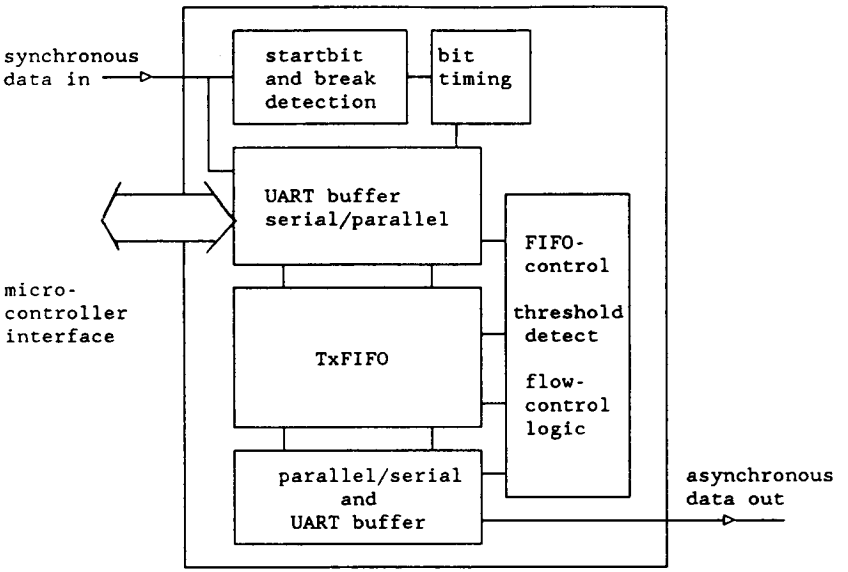


Figure 2.5-3 URF transmitter

2.5.1. RA0 converter

In transmission mode 1B, 1C and 3B the RA0 function is used. Function RA0 is an asynchronous to synchronous conversion stage (and vice versa), using the technique of ECMA-102/CCITT V.22. RA0 converts asynchronous user data to synchronous data of 2**n * 600 bit/s, where n=[0,1,2,3,4,5] (speed setting by μC is needed). This will be done by adding stopbits to fit the nearest synchronous channel. In table 2.5.1-1 the supported speeds and their relations to synchronous- and intermediate rate are depicted.

URF data-rate bps	rate tol-erance % *	data bits	added parity	stop bits	possible FRAME speed selections
300	+4.8/ -4.8	5/7/8	odd/even/	1 or 2	600 - 38400
600	+1 / -4.8	5/7/8	none/	1 or 2	600 - 38400
1200	+1 / -4.8	5/7/8	mark/spac	1 or 2	1200 - 38400
2400	+1 / -4.8	5/7/8	,,	1 or 2	2400 - 38400
4800	+1 / -4.8	5/7/8	,,	1 or 2	4800 - 38400
9600	+1 / -4.8	5/7/8	,,	1 or 2	9600 - 38400
19200	+1 / -4.8	5/7/8	,,	1 or 2	19200 - 38400
1200/75	+1 / -4.8	5/7/8	,,	1 or 2	fixed 1200 bps
75/1200	+1 / -4.8	5/7/8	,,	1 or 2	fixed 1200 bps

* tolerances without Flowcontrol-setting. With FLC all tolerances are +/- 4.8 %

Table 2.5.1-1 Asynchronous data rates.

2.5.1.1. RA0 asynchronous to synchronous conversion

In this section the asynchronous to synchronous conversion algorithm performed by the RA0-function is discussed. The asynchronous to synchronous conversion takes place in two stages. In the first stage an asynchronous data byte is received and placed in the Rx-FIFO (illustrated in figure 2.5-2). In the second stage the data byte is taken out of the Rx-FIFO and transmitted synchronously.

The following actions are performed by the URF receiver for the conversion of asynchronous data (on pin T103) to the Rx-FIFO:

I1. detects a period of n stopbits. This is needed for character synchronisation.
I2. detects the trailing edge of the startbit.
I3. and starts counting to the middle of this bit (at frequency 16*baudrate), checks state zero. If not back to I1.
I4. starts latching incoming bitstream in a shift-in register
I5. increment bitcounter.
I6. at expected stopbit, checks of state one. If so, loads contents of shift-in register into the Rx-FIFO and goto I2.
I6a. If not and a null character has been shifted in, it loads a null character and gives a breaksignal. It waits until a rising edge of a stopbit, goto I2.
I6b. If no stopbit is present at the expected moment and no null character is received, it loads the shift in character into the Rx-FIFO and gives the frame-error signal and continues counting to the next expected middle of a databit, checks if this bit is a start- or a stopbit. If it is a stopbit goto I2. Otherwise goto I4.

The following actions are performed to convert the data from the Rx-FIFO to the synchronous data stream:

01. When a character is available in the Rx-FIFO, data is loaded into a shift-out register (parallel/serial and UART buffer block in figure 2.5-2).
02. The shift-out register is clocked continuously with the used synchronous clock. After shifting out the parallel loaded Rx-FIFO information, the shift-out register continues sending ones (stopbits) until a character is available in the Rx-FIFO.

In figure 2.5.1.1-1 this procedure is illustrated for asynchronous user data of 300 baud with 7 data bits, 1 start bit and 1 stopbit.

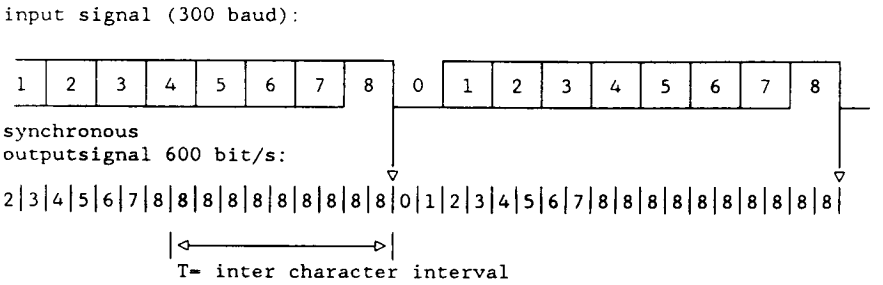


Figure 2.5.1.1-1 RA0 adaption of a 300 baud asynchronous user data rate.

In case the asynchronous user data has a baud rate that is a fraction higher than the nominal baud rate (overspeed), the intervaltime T (figure 2.5.1.1-1) will become smaller because of the insertion of less stopbits. This implies that at a certain user data rate the RA0-transmitter may sometimes delete the only stopbit there is. This causes problems at the remote DEDRA when the transmitted characters are sent with minimal spacing.

This problem is due to the RA0 method. In CCITT rec. V.110 and ECMA-102 the following solution recommended: Because of the overspeed, the contents of the Tx-FIFO (at the remote EDRA) is increasing. To prevent the FIFO to overflow, the EDRA detects a fixed threshold level of the FIFO at two characters. Now the stopbits of the asynchronous to be sent characters are shortened to 7/8 of the normal length. In the case that two stopbits per character are selected, only one stopbit is shortened.

If the baud rate of the user data is somewhat less than the nominal rate (underspeed), the interval T may be longer than nominal because of an extra insertion of a stopbit. This extra stopbit does not affect the transmission.

2.5.1.2. RA0 synchronous to asynchronous conversion

In this section the synchronous to asynchronous conversion by the RA0-function is discussed. The synchronous to asynchronous conversion takes place in two stages. In the first stage a synchronous data byte is received and placed in the Tx-FIFO. In the second stage the data byte is taken out of the Tx-FIFO and transmitted asynchronously (see figure 2.5-3).

The following actions are performed by the URF transmitter to convert synchronous data to the Tx-FIFO:

I1. It starts up with a longer period of stopelements.
I2. searches for the startbit; samples the received synchronous bitstream on the S114 falling edge. The first detected zero is the startbit.
I3. shifts the following characterbits in a shiftin register.
I4. when the whole character is shifted in, the character wil be loaded into the Tx-FIFO, and goto I2.

The following actions are performed to transfer data from from Tx-FIFO to the asynchronous user data stream (R104 output):

O1. until a character is available in the Tx-FIFO, it will transmit stopbits.
O2. loads the character into the shift-out register including a startbit and the selected number of stopbits. In case that the fixed threshold is reached, one stopbit is shortened to 7/8. After this go back to O1.

For 1% overspeed, maximum once per eight characters, a stop-element will be deleted.

2.5.1.3. Break signal detection

RA0 asynchronous to synchronous converter is able to detect a break signal (continuous zeros on input T103) of the DTE connected to the EDRA. If the RA0 converter detects M to 2M+3 bits, all of start polarity (zero), where M is the number of bits per character in the selected format including start-, parity- and stopbits, RA0 transmits 2M+3 bits of start polarity (at the synchronous speed). If RA0 detects more than 2M+3 bits of start polarity, it transmits all these bits as start polarity.

M = nr. of databits + paritybit + startbit + stopbits.

Note:

The DTE must transmit on circuit 103 at least 2M bits of stop polarity after the start polarity break signal, before sending further data characters. The RA0 converter will then be able to regain character synchronisation from the following stop/start transition, else character synchronisation may be lost. This fully in accordance to CCITT rec. V.110.

If 2M+3 or more bits of start polarity are received from the remote EDRA these bits are output to the DTE connected to the EDRA.

In figure 2.5.1.3-1 the transmission of the break signal is illustrated:

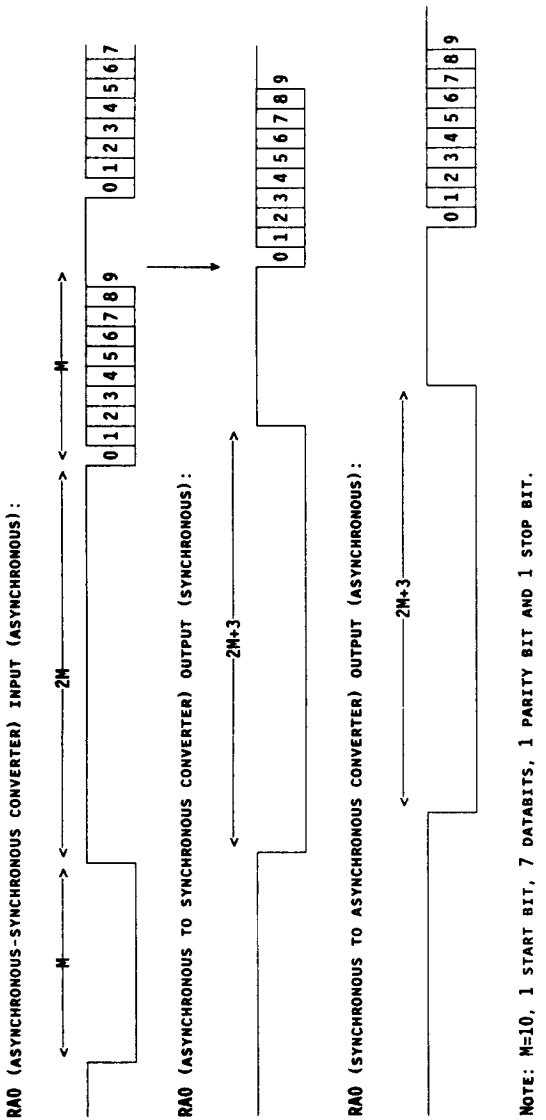


Figure 2.5.1.3-1 the transmission of the break signal

2.5.2. UART

The UART is used in transmission mode 2 of the EDRA. It is also used in transmission mode 1B, 1C, 3A, 3B, 3C to do the serial parallel conversion (and vice versa) as was discussed in section 2.5.1. In mode 1D the UART can be used to monitor the data from the DTE.

The UART that is part of the URF transmitter/receiver has the following capabilities:

- Receive buffer: 32 bytes FIFO.
- Transmit buffer: 32 bytes FIFO.
- Threshold levels for FIFO guarding are programmable (for different flow control situations).
- Split speeds 1200/75 only.
- All registers directly addressable.
- Receiver and transmit interrupt indication in general interrupt status register.
- 5/7/8 bits/char excluding parity.
- number of stop bits: one or two.
- odd, even ,mark ,space or no parity.
- break generation and detection.
- parity, overrun and framing error detection.
- Two basic I/O modes are supported: polling and interrupt driven.

2.5.2.1. Asynchronous receive

The number of bits per character is controlled by the command-code register W11. Five, seven or eight bits per character may be selected also by this register. Data is right-justified (to the least significant bits) with the unused bits set to 1's. The parity of the transmitted character, and the parity check of a received character can be set to Even, Odd, Mark, Space and None. The parity bit is transferred to the receive FIFO with the data if the character length selected, including parity, is 8 bits or less and can be read out of register R27.

The receiver always checks for a stop bit. If after character assembly the stop is found to be '0', the framing error bit is set. This error bit is coupled to the data and can be read in register R27 before the data is read out.

The Break condition is continuous 0's, as opposed to the usual continuous ones during idle. The EDRA recognizes the Break condition upon seeing a null character plus a framing error (see register R27). Upon recognizing this sequence the break bit will be set (register R27) and will remain set until a one is received. At this point the Break condition is no longer present. At the termination of a break the receive data FIFO contains a single null character which should be read and discarded. The Framing Error bit nor the Parity Error bit will be set for this character.

2.5.2.2. Receive interrupts

The receive interrupts of the UART are enabled/disabled as a group by the Receive Interrupt Enable bit (register W4 RxGIE). If the interrupt capabilities are not needed, polling may be used. This is selected by disabling the receiver interrupts and polling the receiver status register (register R27). If receiver status is to be checked, it must be done before the data is read because reading the data pops both the data and error conditions belonging to that data.

The Group Interrupt Pending bit will always be set if one of the receiver activity detectors are set, but an interrupt will only be given if the source is enabled and the RxGIE is set.

2.5.2.3. Asynchronous transmit

The number of stopbits that will be transmitted can be selected in command-code register W11. The setting of character length and parity are common to both the receiver and the transmitter. In all cases the data is in the least significant bits of the data word written by the processor.

The transmitter may be programmed to send a Break. To do this the Send Break bit (register W10) may be written by the processor. Setting of this bit causes the transmitter to transmit continuous 0's from the first transmit clock edge after the bit is set, until the first clock edge after this bit is reset. When this bit is set, the character that's currently beeing sent shall be corrupted and internally the Tx-FIFO is stopped to prevent lost of more characters. An additional status bit for use in asynchronous mode is the All Sent bit. This bit is set when the transmit shift register is empty and all previous data or stop bits have been shifted out. This bit can be used by the processor as an indication that the transmitter may be safely disabled.

2.5.2.4. Transmit interrupts

Transmit interrupts are controlled by the Transmit Group Interrupt Enable bit. There are a number of transmit interrupt sources: Tx-buffer empty, Tx-shift register all sent, overflow and, when enabled, the threshold interrupts.

If the interrupt capabilities are not required polling may be used. This is selected by a reset of the register W04 TxGIE bit and polling the Tx status and activity bits in register R20.

2.5.3. Flow control

The flow control function is used in transmission mode 1C of the EDRA.

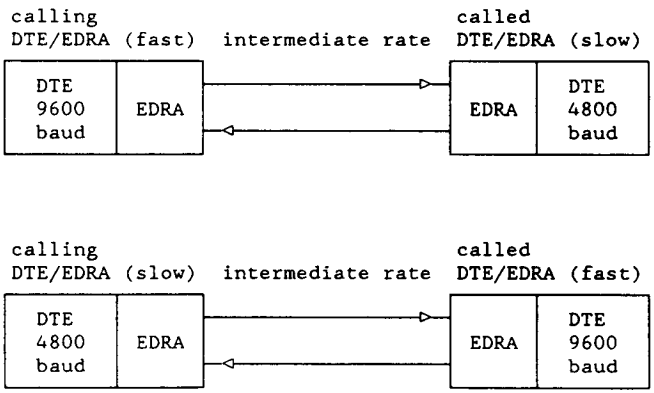
Flow control allows the connection of two EDRAs with asynchronous terminals operating at different user data rates, by reducing the character output of the faster to that of the slower terminal. Each EDRA has a data rate setting that is equal to the data rate of the DTE that it is connected to. Between the two EDRA/DTE combinations a rate difference may be present.

Data rate differences between the two EDRAs is taken care of by the end to end flowcontrol mechanism (manipulation of the X-bit in the data stream on the synchronous data interface). While the data transfer between EDRA and DTE is handled with local flow control. This local flow control can be performed by X-ON/X-OFF or by control of lead 106.

According to ECMA, the intermediate rate between the two EDRAs is determined by the calling EDRA. And so two situations be distinguished:

- A fast EDRA/DTE combination calls a slow EDRA/DTE combination;
- A slow EDRA/DTE combination calls a fast EDRA/DTE combination.

These two situations are illustrated in figure 2.5.3-1.



2.5.3-1 Examples of the two flow-control situations.

When a faster EDRA/DTE calls a slower EDRA/DTE, the situation is illustrated in figure 2.5.3-2:

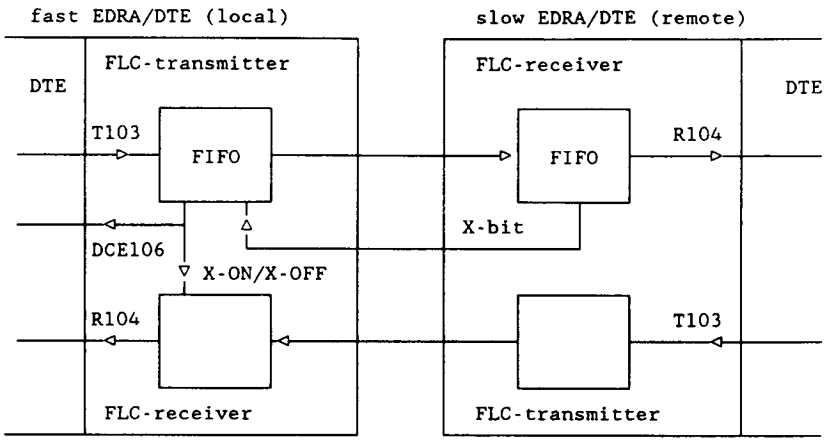


Figure 2.5.3-2 Fast EDRA/DTE calls a slow EDRA/DTE.

In the FLC-receiver of the EDRA at the remote side, data on the synchronous data interface is coming in faster than it is going out to the DTE. The FIFO gets filled. When threshold level 1 is reached (see section 2.5.3.1) the X-bit is turned off ('1'). When the FLC-receiver of the local EDRA detects the X-bit to be turned off, transmission of data over the synchronous data interface is blocked. While data is still coming from the local DTE, the data in the FIFO at the local EDRA reaches the threshold level 1. (This threshold level is also reached is the local DTE transmits with overspeed.) At this point an interrupt (EDRA transmitter TH1) is generated (if enabled). When the command 'AUTO 106' has been given, the DTE will be stopped with lead DCE106. If the connected DTE can only handle XON/XOFF, also 'AUTO XON/XOFF' can be selected. After the local DTE has stopped transmitting data, and the remote EDRAs FIFO level has decreased below threshold level 2, the X-bit will be turned on. The FIFO level from the local EDRA will decrease and lead DCE106 becomes high or a X-ON character will be generated by the EDRA.

The remote control with the X-bit is called end-to-end flow control. The situation at the calling DTE/EDRA, caused by the end-to-end flow control and the overspeed of the DTE, is handled as local flow control.

The second situation the calling DTE/EDRA (local) is slower as the called DTE/EDRA (remote). This situation is illustrated in figure 2.5.3-3.

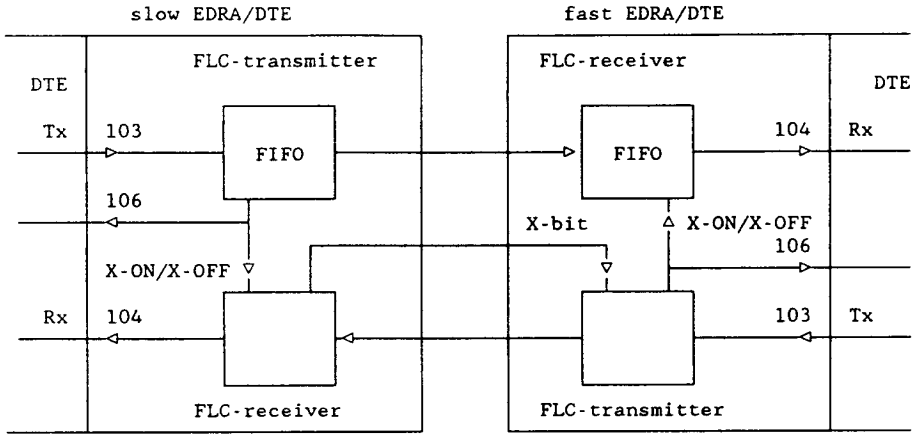


Figure 2.5.3-3 Slow EDRA/DTE calls fast EDRA/DTE.

At the local side, the DTE can cause overspeed due to the fact that the intermediate is determined by the local EDRA. This overspeed is handled with local flow control.

The remote DTE transmits its data faster than the synchronous data interface can handle. Also this situation is solved with the local flow control procedure.

The X-bit in the data stream from local to remote DTE/EDRA is still used, but is continu ON ('0'), unless overspeed occurs because of insertion X-ON/X-OFF characters in the receiver at the local side.

2.5.3.1. Flow control FIFOs

The FIFOs, which are used for flow control, have a capacity of 32 bytes. They are equiped with two threshold level detectors, which can be programmed in registers W12 and W14 (section 2.9.1). The threshold detectors give an indication if the contents of the FIFO is higher than level 1 or lower than level 2. An illustration of the FIFOs is given in figure 2.5.3.1-1.

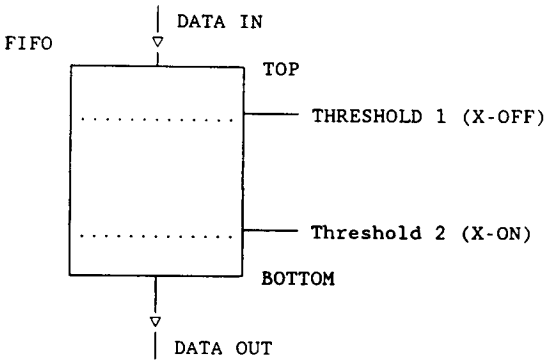


Figure 2.5.3.1-1. Flow control FIFO.

For both receiver- and transmitter FIFO a threshold register is available to be able to program both threshold levels. The register is divided into two parts. The first part contains threshold level TH1 (4 bits), the second part contains threshold level TH2 (4 bits) (see section 2.9.1.13). Both thresholds can only have an odd values. With the four bits in the threshold register only the four most significant bits can be programmed. The least significant bit is always 1. So all odd threshold levels between 1 and 31 can be programmed.

2.5.3.2. FIFO threshold levels

The setting of the FIFO threshold levels concerning flow-control, depends on the type of data connection. Determining factors are whether the EDRA is on the calling or called side of a data connection, and if its DTE data rate is faster or slower than the data rate of the DTE at the remote EDRA.

Resuming, there are 4 different situations:

1. The EDRA is at the calling side of the connection, local DTE is faster than remote.
2. The EDRA is at the calling side of the connection, local DTE is slower than remote.
3. The EDRA is at the called side of the connection, local DTE is slower than remote.
4. The EDRA is at the called side of the connection, local DTE is faster than remote.

Each situation requires it specific setting of the threshold levels of the FIFOs. The settings are determined by the following characteristics:

-Overspeed of the DTE;
-DTE responce on lead 106 or X-OFF, the number of characters transmitted by the DTE after "X-OFF" or DCE106 LOW;
-Local/remote DTE data rate difference;
-Delay of the network.

Flow control can be used in different ways, automatically or microprocessor controlled. The flowcontrol mode can be set in write register W00 (section 2.9.1.1). The specific flowcontrol features can be selected in write register W11 (section 2.9.1.12). The monitoring of flowcontrol is performed by the FIFO threshold levels 1 and 2. When threshold level TH1 is reached, the incoming data must be stopped as soon as possible. When the level drops below threshold level TH2, the FIFO can accept data again.

2.5.3.3. End to end flowcontrol

For end to end flowcontrol, the X-bit in the synchronous data interface frame controls the transfer of data via that interface. The end to end flow control can be automatically performed by the EDRA or can be managed by the microcontroller.

If the EDRA is in the automatic flow control mode the X-bit is switched ON and OFF according the values of the threshold levels TH1 and TH2 of the FLC-receiver. In figure 2.5.3.3-1 the switching of the X-bit is illustrated.

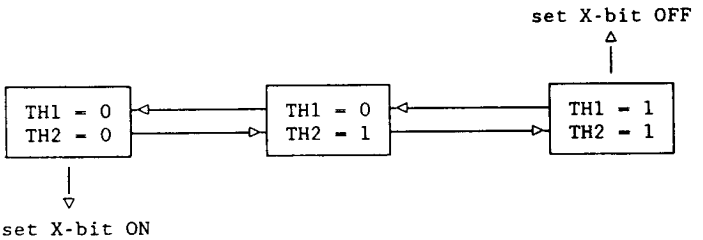


Figure 2.5.3.3-1 X-bit control by the threshold levels.

When the EDRA is not in automatic mode, the microcontroller must know the state of the FIFO thresholds of the FLC-receiver to be able to perform flowcontrol.

The threshold levels can be monitored by polling read register R20 (section 2.9.2.1) or if bit THD GIE of write register W04 is enabled and (TH1=0 and TH2=0) or (TH1=1 and TH2=1) an interrupt will be generated.

The microcontroller has to perform the following actions:

If an interrupt was generated and the interrupt source was the FLC-receiver TH1 or (in polling mode) TH1 = 0, the X-bit must be clamped '1' (OFF)

In an interrupt was generated and the interrupt source was the FLC-receiver TH2 or (in polling mode) TH2 = 1, the X-bit must be clamped '0' (ON)

The remote EDRA will stop the transmission of data on the synchronous data interface when the received X-bit is ON. When the received X-bit is OFF, it can restart transmission.

2.5.3.4. Local flowcontrol

If local flow control is performed in automatic mode the EDRA performs the folling actions:

When threshold level TH1 is reached at the FLC transmitter, the transmission of data from DTE to the EDRA must be stopped. If the FIFO level of the FLC transmitter drops below threshold level TH2, the DTE can start the data transmission again.

The EDRA can start and stop the transmission of the DTE data in two ways:

-In the 'AUTO 106' mode lead DCE106 will be controlled by the flow control logic.
-If the EDRA is in 'AUTO XON/XOFF' mode, character 'X-OFF' (DC3 ASCII) or 'X-ON' (DC1 ASCII) are inserted in the data, and transmitted via lead T104 to the DTE. The ASCII code for XON/XOFF can be downloaded in write registers W16 and W17).

If the local flowcontrol is performed by the microcontroller, the threshold levels TH1 and TH2 can be monitored by polling read register R20 (section 2.9.2.1) or if bit THD GIE of write register W04 is enabled and (TH1=0 and TH2=0) or (TH1=1 and TH2=1) an interrupt will be generated. The actions that must performed on the interrupt from TH1 and TH2 of the URF-transmitter are illustrated in figure 2.5.3.4-1.

interrupt-source	DTE reacts on lead DCE106	DTE reacts on XON/XOFF character
TH1 = 1	clamp DCE106 to 1 (OFF)	EDRA sends one X-OFF character
TH2 = 0	clamp DCE106 to 0 (ON)	EDRA sends one X-ON character

Figure 2.5.3.4-1 Local flowcontrol procedure by μC.

2.5.3.5. X-ON/X-OFF

The X-ON and X-OFF characters can be downloaded by the microcontroller into register W16 and W17 (section 2.9.1). Only the data must be written, parity, start and stop bits will be auto generated by the EDRA according the settings in register W11 (section 2.9.1.12).

The X-ON/X-OFF characters are generated by the EDRA in the AUTO X-ON/X-OFF mode. However the X-ON/X-OFF characters can be inserted in the data stream on lead T104 by microcontroller (see register W11).

It is possible to filter the X-ON/X-OFF characters that are received on lead T103. This can only be done if they do not contain any parity and/or frame errors. This feature is needed when local flow-control is used with X-ON/X-OFF because if a X-ON/X-OFF character is transmitted to the remote EDRA/DTE, the local flow-control at this remote EDRA/DTE can be disturbed. These filter can prevent the transfer of X-ON/X-OFF characters in the data stream to the remote EDRA. The filters can be enabled/disabled by μC in write register W11.

The default setting of the filters (when a transmission mode is selected in write register W00) is 'OFF' (no filtering). When in transmission mode 1C (flow-control) the AUTO X-ON/X-OFF mode will be selected, both filters will be active.

Two data switches are implemented in URF. One in the data path from T103 to SDO (just after the Rx-FIFO), and one in the data-flow from SDI to R104 (just after the Tx-FIFO). By switching the data switches the data flow inbvolved can be stopped.

Both switches can be independently enabled/disabled by the microcontroller, or be controlled by the X-bit from SDI for the Rx data switch and controlled by the X-ON/X-OFF character-detection (T103) for the Tx data switch.

The settings for control of the data switches are written in register W11 by microcontroller.

By selection of any transmission mode, both the Tx and Rx data switches will be enabled, except for transmission mode 1C. In this case the data switches will be controlled by the X-bit from the remote EDRA. When in transmission mode 1C 'AUTO X-ON/X-OFF' mode is selected, the Tx data switch will be default controlled by the X-ON/X-OFF character recognition.

In figure 2.5.3.5-1 the data paths of the EDRA in flowcontrol mode are illustrated.

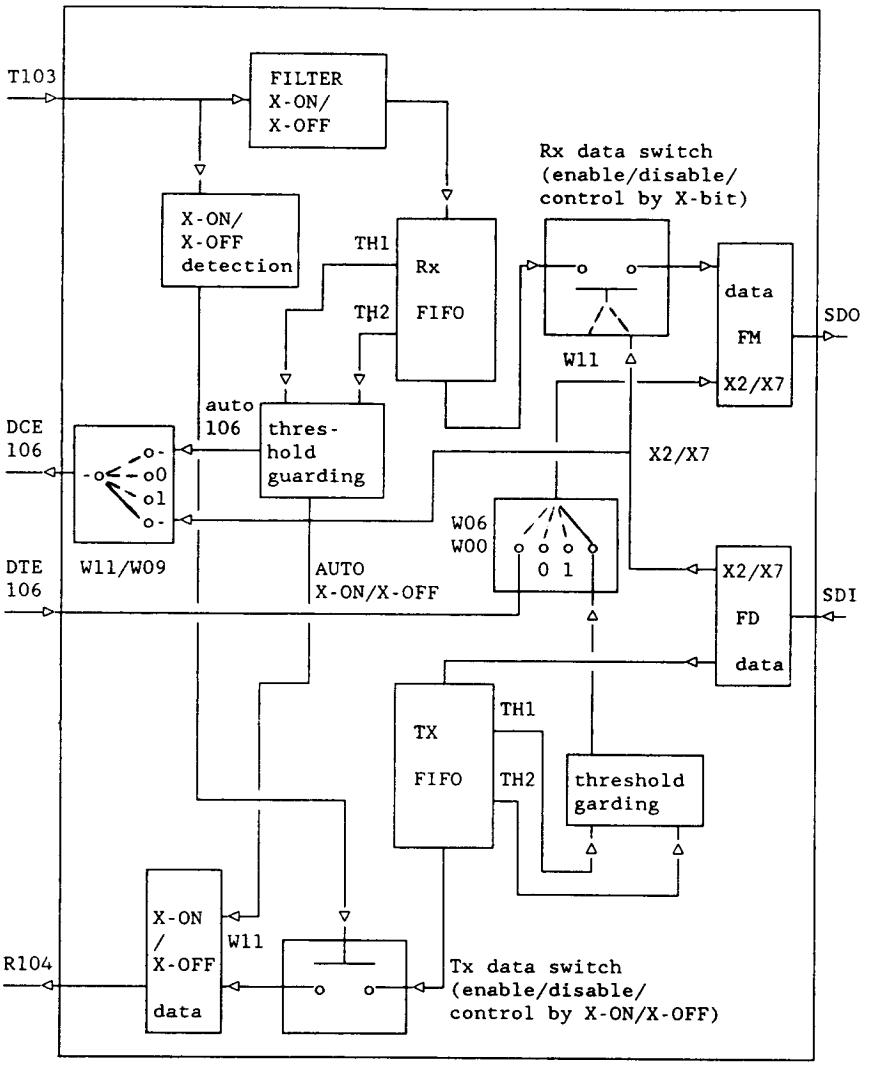


Figure 2.5.3.5-1 Flow control in the EDRA.

2.6. Inband Parameter Exchange

The EDRA allows transfer of parameter information within the user data stream of an established connection. This transfer of parameter information is called Inband Parameter Exchange (IPE). The EDRA supports the three different types of IPE that are recommended by ECMA-102:

- asynchronous IPE mode with RA0 coded data in the 64 kbit/s channel (EDRAs transmission mode 3B).
- unrestricted synchronous IPE mode at 64kbit/s rate in the 64 kbit/s channel (EDRAs transmission mode 3C).
- restricted synchronous IPE mode at 56kbit/s rate in the 64 kbit/s channel (EDRAs transmission mode 3C).

and also is supported:

- multiple sampling coded data in the 64 kbit/s channel (EDRAs transmission mode 3A).

In all four modes the transmit data is to be written into write register W15 while the received data must be read from read register R26.

2.6.1. Asynchronous IPE mode

In the asynchronous IPE mode, the data is RA0 coded on an intermediate rate or 64 kbit/s channel. The number of data bits in a data byte, the number of stopbits and the parity bit should be programmed in the UART (see section 2.5.2).

In the ECMA recommendations IPE is specified for three speeds: 19200, 9600 and 4800 bit/s. The EDRA supports IPE for all RA0 speeds. The interchange circuits can be used as in all other modes.

Data written to register W15 and is placed in the Tx-FIFO. Then it is shifted out on the synchronous data interface. When all data is transmitted, the transmitter starts sending 1's until a new character is available for transmission.

The received data can be readout of the Rx-FIFO (read register R26).

2.6.2. Synchronous IPE mode at 64 kbit/s

The synchronous IPE function for unrestricted transfer. For this mode only one additional setting must be done in write register W11: the character length should be set on 8 bits/char. Data written to register W15, will be placed in the Tx-FIFO and is shifted out on the synchronous data interface, without additions. When the Tx-FIFO is empty, the last byte that was transmitted, will be repeated until a new character is available.

The received data can be readout of the Rx-FIFO (read register R26).

2.6.3. Restricted synchronous IPE mode at 56 kbit/s

The synchronous IPE function for restricted transfer. For the EDRA this mode is equal to unrestricted 64 kbit/s IPE mode.
For this mode only one additional setting must be done in write register W11: the character length should be set on 8 bits/char. Only the lowest 7 bits can be used in write register W15. The MSB should be set '1'. The data written to register W15, will be placed in the Tx-FIFO and is shifted out on the synchronous data interface, without additions. When the Tx-FIFO is empty, the last byte that was transmitted, will be repeated until a new character is available.

The received data can be readout of the Rx-FIFO (read register R26).

2.6.4. Multiple sampling IPE mode

In the multiple sampling IPE mode, the data is coded according the multiple sampling method and placed in the 64 kbit/s channel. The number of data bits in a data byte, the number of stopbits and the parity bit should be programmed in the UART (see section 2.5.2).

The data that is written in register W15, will be placed in the Tx-FIFO and is shifted out to the multiple sampling coder. When all data is transmitted, the transmitter starts sending 1's until a new character is available for transmission.

The received data can be readout of the Rx-FIFO (read register R26).

2.7. Network independent clocking

When the EDRA must adapt synchronous data of which the timing is not synchronised to the EDRA timing, a method, called bit-stuffing is used to enable transfer of those data signals (for V-series only). The EDRA supports the NIC function as it is decribed in the ECMA-102/CCITT V.110 recommendations.

In this section the term modem-clock (on lead S113) will be used when the independent clock is meant and EDRA-clock (on lead S114) for the system locked clock.

The NIC function consists of the following parts:

- a phase comparator that measures the phase difference between the EDRA- and modem-timing and a buffer for transmit data.
- a coder that provides the E-bits in the synchronous data interface bitstream with compensation information.
- and a decoder to translate the incoming E-bits of the synchronous data interface to data and clock correction.

In figure 2.7-1 a blockdiagam is illustrated of the NIC transmitter while in figure 2.7-2 the NIC receiver is illustrated.

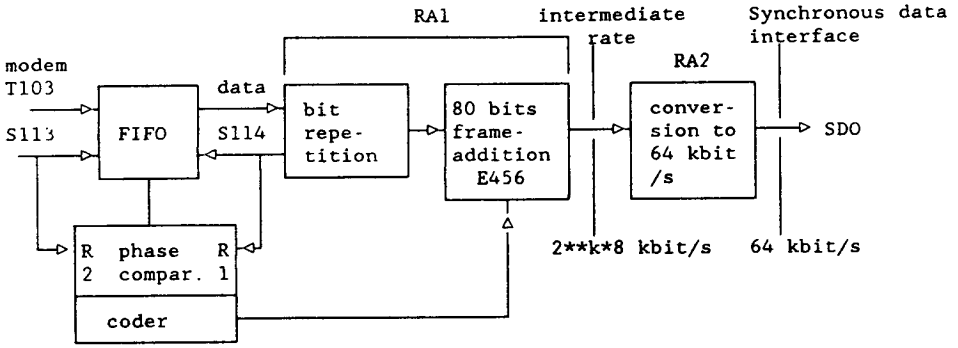


Figure 2.7-1 Block diagram of the NIC transmitter.

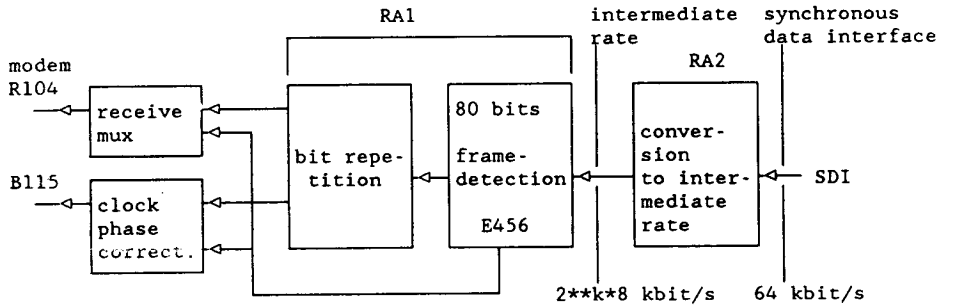


Figure 2.7.2 Block diagram of the receiver.

2.7.1. NIC transmitter

The measurement of the phase difference:

The phase difference between the following two frequencies is measured (according to ECMA-102 recommendation):

R1 = 0.6 * intermediate rate of the EDRA (synchronised to EDRA)
R2 = 0.6 * intermediate rate of the modem, derived from and synchronised to the modem signal element timing

The relation between R1, R2 and their intermediate rate is depicted in table 2.7.1-1.

intermediate rate	R1,R2
8000	4800
16000	9600
32000	19200

Table 2.7.1-1 Nominal R1/R2 frequencies for given intermediate.

Phase measurements are given relative to R1 by the formula below:

PD (phase difference) = phase(R2) - phase(R1)

The system will know the next five phases: 0%, 20%, 40%, -40%, -20%. These phases will be coded and transmitted to the receiving EDRA in the E-field (of the 10 bytes frame).

Compensation:

The next drawing shows the states of the phase of R2 relative to R1.

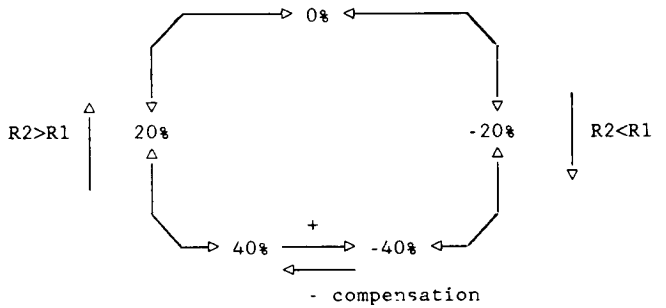


Figure 2.7.1-2 Network independent clocking state diagram.

Every 10 bytes frame the EDRA connected to the modem codes the phase difference state into the E4, E5 and E6 positions of the E-field. To avoid continuous jitter in the transmitted code, it will be changed after an increased phase difference of 15% (of the R1 clock period). So, a code 000 (20%) will be changed in 001 (40%), when the measured phase difference is 35% or more, and changed in 111 (0%) when 5% or less.

In the case the data rate of the modem is higher than the rate of the EDRA the situation occurs that the phase difference is 40%. When the phase difference is 40%, the modem nearly transmits more information than the EDRA can handle. At a certain moment the phase difference will be 55%. This means that the EDRA will miss one data bit received from the modem. With the compensation method this bit will be transmitted in the E-bits. This is called positive stuffing and the transmitted code will indicate compensation of a binary 1 or 0.

In the case the data rate of the modem is lower than the rate of the EDRA the situation occurs that the phase difference is -40%. When the phase difference is -40%, the EDRA is nearly transmitting more information than the modem offers. At -40% to 40% transition the code indicates the receiving EDRA to 'stuff' a bit (negative compensation). In table 2.7.1-3 the coding of the E-bits used for network independent clocking is illustrated.

Displacement (in % of nominal R1 clock period at n * 4800 bps, n=1, 2 or 4)		Coding in the 80-bits frame		
		E4	E5	E6
nominally	0	1	1	1
	+20	0	0	0
	+40	0	0	1
	-40	0	1	0
	-20	0	1	1
Compensation control		E4	E5	E6
Positive compensation of binary 1		1	0	1
Positive compensation of binary 0		1	0	0
Negative compensation		1	1	0

Table 2.7.1-3 Coding of the E bits.

2.7.2. NIC receiver

The NIC receiver contains a decoder/phase shifter and a receiver data-mux. By means of the received frame, the phase of the receiver-clock (to DTE) must be changed in steps of 20%, as described in chapter 2.7.1.

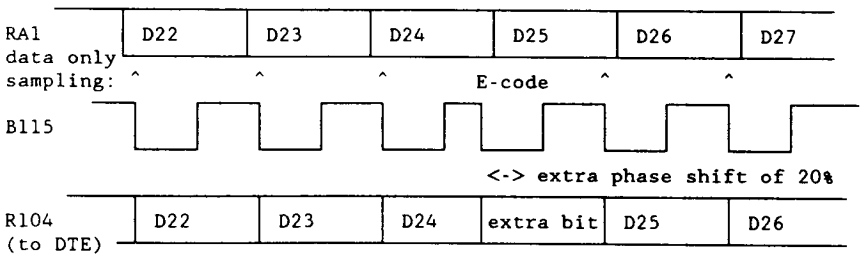


Figure 2.7.2-1 Positive compensation.

Figure 2.7.2-1 shows the received data (from the RA1) and the EDRA clock. In the previous frames the E4, E5 and E6 bits indicated a phase shift that resulted in a +40% clock. After bit D24 a new E-Field is received indicating positive-compensating of a bit. This results in new phase shift of the clock of 20% to +60% (-40%).The received data-mux now selects the extra bit coming from the E-Field. The next clock-edge will be just in time to sample bit D25. The achieved clock-delay will now be -40%.

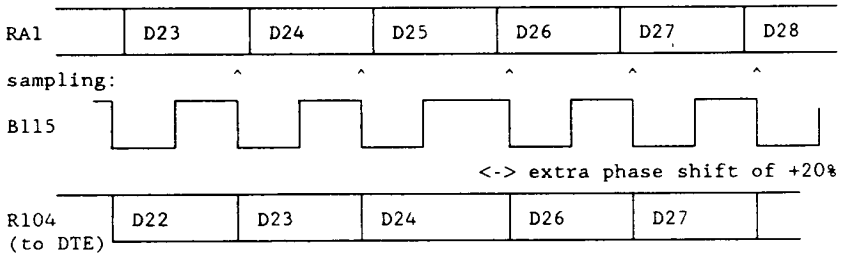


Figure 2.7.2-2 Negative compensation.

Figure 2.7.2-2 shows a -40% clock. The next received E-field indicate a negative compensation. This will result in an extra clock-delay of 20% to -60% (+40%). After this clock shift, bit D25 will be skipped.

The place in the framing where compensation takes place is bit D25. Positive compensation inserts a bit between D24 and D25, negative compensation deletes bit D25.

Max frequency deviation modem clock for 4800, 9600 and 19200 bit/s = +/- 0.347 % while the allowed jitter on modem clock for 4800, 9600 and 19200 bit/s is 1 bit jitter on 48 bits interval. This is a 1.97 % modem clock deviation, provided that the mean deviation over 48 bits is zero.

2.8. Frame mapping/demapping and multiple sampling

2.8.1. Multiple sampling method

For asynchonous user data to synchronous 64 kbit/s conversion, the EDRA has the multiple sampling method available as it is implemented in its predecessor the PCB2320 DRA. Every asynchronous data rate lower than or equal to 19200 bit/s can be adapted without a specific speed setting on the EDRA (the local and remote DTE however should have the same data rate setting).

Concerning the interchange circuits, two points must be taken into account: The EDRA must be in X30-mode (see register W00, section 2.9.1.1). The relation between ON/OFF of the interchange circuits and the binary values of the S- and X-bits on the synchronous data interface should be according the ECMA-102 september definition (see section 2.3.2).

This coding/sampling method is based on the technique of multiple sampling with additional transition coding as depicted in CCITT recommendation R.111.

This method doesn't recognise character lenght or start-stop bits. It samples the incoming data with 96 kHz. Only transitions are coded in two bits: a transition bit T and coding bit C.

The transition bit T is used to indicate the polarity after a transition, and the second bit C (coding) defines in which half A or B of a 48 kbit/s clock period the transition has occurred. Transitions of data rates upto 24 kbit/s can be coded by the 48 kbit/s. Because one bit can discriminate two phases (A or B), the sampling frequency has to be 96 kHz.

In the lower data-rates, more than two 48 kHz pulses will fall between two signal element transitions. In this case the resulting 48 kbit databits P (polarity) will repeat the polarity and are therefore equal to the previous bit T.

The phase jitter on the received data stream varies for the different bit rates from 20 % for 19.2 kbit/s down to 2.5 % for 2400 bit/s or even lower for slow data.

The 48 kbit/s data stream is further handled as 48 kbit/s synchronous data stream.

In appendix C the multiple sampling method is illustrated.

2.8.2. Frame mapping/demapping

For synchronous data rates of 600, 1200, 2400, 4800, 9600, 19200 and 38400 bit/s, a X.30/V.110 defined multiframe of 10 bytes bits is used (see appendix B). It consists of two 5 bytes frames, using subrates of 8, 16 and 32 kHz. An incoming data rate will be first translated to the next higher rate expressed by 2**k * 8 kHz where k=[0,1,2,3] (see table 2.8.2-1). For speeds 600, 1200, 2400 a first rate adaption to 4800 bit/s is done by bit repetition. This first stage of rate adaption is called the RA1 function and is illustrated in figure 2.8.2-2.

Data rate (bit/s)	framespeed (Hz)
600, 1200, 2400, 4800	8000
9600	16000
19200	32000
38400	64000

Table 2.8.2-1 First step in data rate adaption.

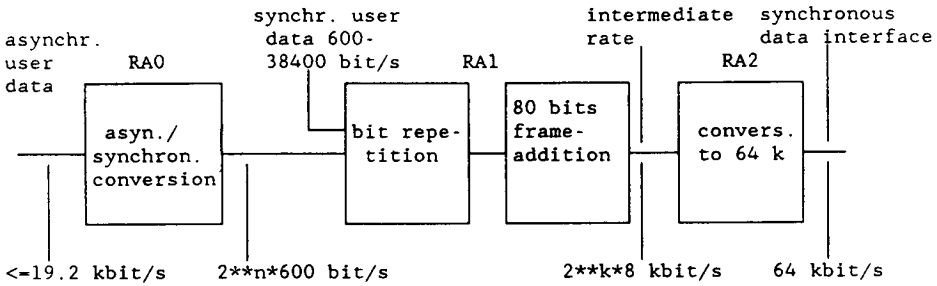


Figure 2.8.2-2 Bit rate adaption of synchronous data received from the RA0 blocks and synchronous user data <=38400 bit/s.

The multiframe consists of 10 bytes containing 8*6 data bits, 8 S-bits, two X-bits, 17 bits for the frame synchronisation pattern and 7 E-bits used for the following purposes:

E1	E2	E3	E4	E5	E6	E7
speed indication for remote EDRA			network independ. clocking code-bits			600 and 1200 bit/s multiframe syncbits

The three speed indication bits can be filled in via the μC-interface and are transmitted to the remote EDRA transparently. The E4 to E6 bits are used to transmit the positive or negative bit-stuffing coding. Bit E7 is used for slow-data synchronisation purposes (see section 2.9.1.4).

The data rate conversion is completed after the conversion of the intermediate rate to 64 kbit/s by block RA2 as illustrated in figure 2.8.2-2.

The 48, 56 and 64 kbit/s synchronous user data are adapted to 64 kbit/s in one step using a 32 bit frame. Asynchronous user data ≤ 19200 bit/s, that is coded with the multiple sampling method, is also inserted at this level as a 48000 bit/s data stream. In figure 2.8.2-3 this rate adaption stage is illustrated.

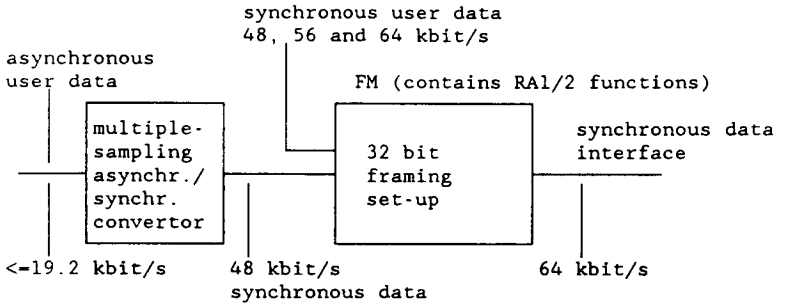


Figure 2.8.2-3 Bit rate adaption of synchronous user data >=48000 bps and asynchronous user data (multiple sampling).

For the data rate of 48000 bit/s a 32 bits frame is used (see appendix B). This frame consists of 4 bytes containing 4*6 data bits, 3 S-bits, one X-bit and 4 frame synchronisation bits.

For the data rate of 56000 bit/s the 32 bits frame structure is used (see appendix B). Only now 4*7 bits consist for data and four S-bits. No frame bits for synchronisation can be used.

For the data rate of 64000 bit/s no rate adaption is needed and the DRA is transparent for this speed (see appendix B).

2.9. Microcontroller interface

The EDRA is controllable by the 8-bit INTEL compatible microcontroller bus.

The bus consists of:

* 8 data/address multiplexed I/O lines (DB7 to DB0)
* A read not input (RDN)
* A write not input (WRN)
* An address latch enable input (ALE)
* A chip select not input (CSN)
* An interrupt not open drain output (INTN)

When ALE is HIGH and the EDRA is selected, the address on the DB7-DB0 I/O port is latched into the address latch. One of the eightteen write registers or one of the nine read registers may be selected (see table 2.9-1). This selection is made by the five least significant data/address lines (DB0-DB4) and the CSN signal whereby the EDRA is selected by CSN and register is selected by the address lines.

When RDN is LOW the EDRA writes the data byte from the selected read register to the data-bus I/O port. On the leading edge of WRN, the data-byte from the data-bus I/O port is written into the addressed write register.

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	address	write reg	read reg
X	X	X	0	0	0	0	0	0	W0	-
X	X	X	0	0	0	0	1	1	W1	-
X	X	X	0	0	0	1	0	2	W2	-
X	X	X	0	0	0	1	1	3	W3	-
X	X	X	0	0	1	0	0	4	W4	-
X	X	X	0	0	1	0	1	5	W5	-
X	X	X	0	0	1	1	0	6	W6	-
X	X	X	0	0	1	1	1	7	W7	-
X	X	X	0	1	0	0	0	8	W8	-
X	X	X	0	1	0	0	1	9	W9	-
X	X	X	0	1	0	1	0	10	W10	-
X	X	X	0	1	0	1	1	11	W11	-
X	X	X	0	1	1	0	0	12	W12	-
X	X	X	0	1	1	0	1	13	W13	-
X	X	X	0	1	1	1	0	14	W14	-
X	X	X	0	1	1	1	1	15	W15	-
X	X	X	1	0	0	0	0	16	W16	-
X	X	X	1	0	0	1	0	17	W17	-
X	X	X	1	0	1	0	0	20	-	R20
X	X	X	1	0	1	0	1	21	-	R21
X	X	X	1	0	1	1	0	22	-	R22
X	X	X	1	0	1	1	1	23	-	R23
X	X	X	1	1	0	0	0	24	-	R24
X	X	X	1	1	0	0	1	25	-	R25
X	X	X	1	1	0	1	0	26	-	R26
X	X	X	1	1	0	1	1	27	-	R27
X	X	X	1	1	1	0	0	28	-	R28

Table 2.9-1 Register addresses.

2.9.1. Registers W0-W17

In this section the bit assignment of the write registers is illustrated.

EDRA-mode control:

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W0	-	-	FSINV	TRM2	TRM1	TRM0	ICM1	ICM0
W1	V7	V6	V5	V4	V3	V2	V1	V0
W2	LLP1	LLPCI	LLP3	RLP4	RLP2	E3	E2	E1
W3	SDO=1	SG2	SG1	SG0	FM1	FM0	E7	NoCCITT

Table 2.9.1-1 Bit assignment;register W0, W1, W2, W3.

General interrupt control:

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W4	MIE	-	-	ICGIE	THGIE	OOSIE	TxGIE	RxGIE

Table 2.9.1-2 Bit assignment;register W4.

Input interchange circuits:

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W5	R104IE	T103IE	C105IE	V108IE	MI2IE	MI1IE	DTE106 IE	SXI
W6	T103=1	T103=0	C105=1	C105=0	V108=1	V108=0	DTE106 =1	DTE106 =0
W7	S9	S8	X7	S6	S4	S3	X2	S1

Table 2.9.1-3 Bit assignment;register W5, W6, W7.

Output interchange circuits:

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W8	S9IE	S8IE	X7IE	S6IE	S4IE	S3IE	X2IE	S1IE
W9	R104=1	R104=0	DCE106 =1	DCE106 =0	107=1	107=0	I109=1	I109=0
W10	TXsebr	MO1	B115=1	S114=1	-	MO2	-	SXO

Table 2.9.1-4 Bit assignment;register W8, W9, W10.

Selections for URF (UART/RAO/Flowcontrol):

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W11	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0

Table 2.9.1-5 Bit assignment;register W11.

URF receiver FIFO thresholds:

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W12	TH2A4	TH2A3	TH2A2	TH2A1	TH1A4	TH1A3	TH1A2	TH1A1

Table 2.9.1-6 Bit assignment;register W12.

URF mode bits:

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W13	RxFrEr IE	RxPar IE	RxBreak IE	Rx/TxOf IE	RxChAv IE	TxFIFOe IE	TxAllSe IE	XonXoff IE

Table 2.9.1-7 Bit assignment;register W13.

URF transmitter FIFO thresholds:

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W14	TH2A4	TH2A3	TH2A2	TH2A1	TH1A4	TH1A3	TH1A2	TH1A1

Table 2.9.1-8 Bit assignment;register W14.

UART Transmit buffer:

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W15	TX7	TX6	TX5	TX4	TX3	TX2	TX1	TX0

Table 2.9.1-9 Bit assignment;register W15.

(Flow control) XON/XOFF code:

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W16	XON 7	XON 6	XON 5	XON 4	XON 3	XON 2	XON 1	XON 0
W17	XOFF 7	XOFF 6	XOFF 5	XOFF 4	XOFF 3	XOFF 2	XOFF 1	XOFF 0

Table 2.9.1-10 Bit assignment;register W16, W17.

2.9.1.1. Register W00

Bit ICM0 and ICM1: Bit ICM0 and bit ICM1 are used to select the mode of the interchange circuits as the are described in section 2.3. The modes are illustrated in table 2.9.1.1-1.

IC0	IC1	mode
0	0	V.110
0	1	μC
1	0	X.30
1	1	not used

Table 2.9.1.1-1. interchange circuit modes.

Bit TRM0 to TRM2: Bit TRM0 to TRM2 are used to select the transmission mode of the EDRA. The transmission modes of the EDRA are described in section 2.2. The relation between bits TRM0 to TRM2 and the transmission mode of the EDRA are depicted in table 2.9.1.1-2.

TR2	TR1	TR0	Transmission mode		
0	0	0	1A	synchronous	(DTE-DTE)
0	1	0	1B	asynchronous RA0	(DTE-DTE)
0	1	1	1C	asynchronous FLC	(DTE-DTE)
0	0	1	1D	asynchronous MS	(DTE-DTE)
1	0	0	2	asynchronous	(DTE- µC)
1	1	0	3A	asynchronous MS	(µC - 64kbit/s)
1	0	1	3B	asyn. RA0 (IPE-RA0)	(µC - 64kbit/s)
1	1	1	3C	IPE-64/56kbit/s	(µC - 64kbit/s)

Table 2.9.1.1-2 Transmission mode of the EDRA.

Note 1: when mode 1D (asynchronous multiple sampling) is selected, the speed selection in W01 must be set to 48 kbit/s.

Note 2: If no flow control is selected (any other mode than mode 1B) the next actions must be taken to disable the flowcontrol-auto modes:

*For mode 1A: Write to register W11: 24H.
*For mode 1B: Write to register W11: 24H and
to register W12: FFH.
*For mode 1C: Write to register W12: 24H.
*For mode 3 : No special actions, interchange interface leads should be clamped.

Bit FSINV: Frame select inversion. When FSINV is set to '0': FSX/R leading edge triggers frame select. This situation is described in section 2.4 and illustrated in figure 2.4.1-1. When FSINV is set to '1': FSX/R trailing edge triggers frame select (the inverse frame select signals can be provided to the EDRA).

2.9.1.2. Register W01

Bits V0 - V4: bits V0 - V4 determine the synchronous data rate at the interchange interface for the adaption of synchronous user data. They also determine the synchronous data rate in which the output data of the RA0 block is placed (in case of RA0 asynchronous user data rate adaption). The NIC data rates can also be selected by V0 - V4. The settings of V0 - V4 are illustrated in table 2.9.1.2-1.

V4	V3	V2	V1	V0	Frame speed	Intermediate	remarks
0	0	0	0	1	600	8000	
0	0	0	1	0	1200	8000	
0	0	0	1	1	2400	8000	
0	0	1	0	0	4800	8000	
0	0	1	0	1	9600	16000	
0	0	1	1	0	19200	32000	
0	0	1	1	1	38400	64000	
0	1	0	0	0	48000 *)	64000	
0	1	0	0	1	56000	64000	
0	1	0	1	0	64000	64000	
0	1	1	0	0	1200/75	8000	Split
0	1	1	0	1	75/1200	8000	speeds
1	0	1	0	0	4800	8000	NIC
1	0	1	0	1	9600	16000	speeds
1	0	1	1	0	19200	32000	

*) In transmission mode 1D, Multiple sampling mode (see register W00), 48000 bps must be selected.

Note: for split speed interchange connections to the DTE see appendix D.

Table 2.9.1.2-1 Synchronous data rate selection.

Bit V5 - V7: bit V5 - V7 determine the asynchronous data rate of the URF receiver/transmitter. These settings are used in transmission mode 1B, 1C, 1D, 2, 3A and 3B. In table 2.9.1.2-2 the settings of V5 - V7 are illustrated.

V7	V6	V5	URF rate (baud)
0	0	0	300
0	0	1	600
0	1	0	1200
0	1	1	2400
1	0	0	4800
1	0	1	9600
1	1	X	19200

Table 2.9.1.2-2 URF rate selection.

2.9.1.3. Register W02

Bits E1, E2 and E3: In every 10 bytes multiframe (for user data rates not exceeding 38400 bit/s), E1 to E3 are available to transmit information about the data rate setting to the remote subscriber. The information to be filled in, is illustrated in table 2.9.1.3-1.

data rate (bit/s)	E1	E2	E3
600	1	0	0
1200	0	1	0
2400	1	1	0
4800	0	1	1
9600	0	1	1
19200	0	1	1

Table 2.9.1.3-1 Setting of E1 - E3.

Bit RLP2: If bit RPL2 is made '1' remote test loop 2 is set. In this testloop circuit R104 is inside the EDRA connected to circuit T103 and circuit I109 is inside the EDRA connected to circuit C105. This remote testloop is illustrated in figure 2.9.1.3-2.

Bit RLP4: If bit RLP4 is made '1' remote testloop 4 is set. In this testloop circuit T103 is inside the EDRA connected to circuit R104. The serial data input is inside the EDRA connected to the synchronous data output. The remote testloop 4 is illustrated in figure 2.9.1.3-3.

Bit LLP3: If bit LLP3 is made '1' local testloop 3 is set. In this testloop the synchronous data output is inside the EDRA connected to the synchronous data input. The local testloop 3 is illustrated in figure 2.9.1.3-4.

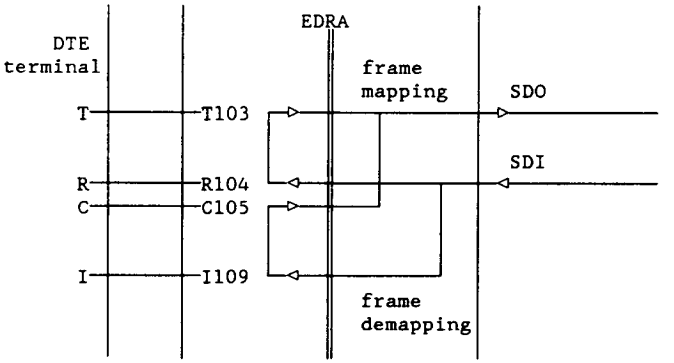


Figure 2.9.1.3-2 remote testloop 2

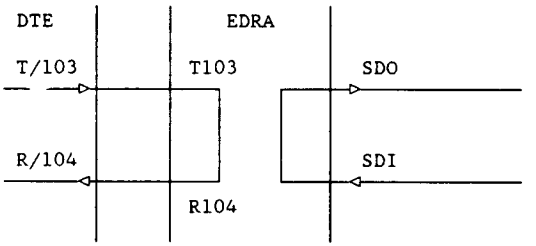


Figure 2.9.1.3-3 remote testloop 4

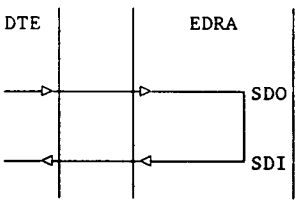


Figure 2.9.1.3-4 local testloop 3

Bit LLPCI: If bit LLPCI is made '1' local testloop C⟶I is set. In this testloop the input C105 is inside the EDRA connected to the I109 output. The local testloop C⟶I is illustrated in figure 2.9.1.3-5.

note: this loop can only be used when the V.110 mode is selected in register W00.

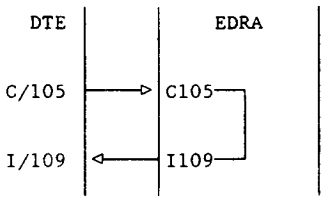


Figure 2.9.1.3-5 local testloop C⟶I

Bit LLP1: If bit LLP1 is made '1' local testloop 1 is set. In this testloop the input T103 is inside the EDRA connected to the R104 output. The local testloop 1 is illustrated in figure 2.9.1.3-6.

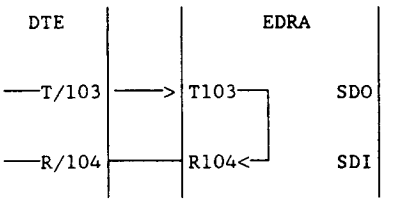


Figure 2.9.1.3-6 local testloop 1

2.9.1.4. Register W03

Bit NoCCITT: When the EDRA is in X.30 mode and bit NoCCITT is '0', circuit I109 is byte timing synchronous according to CCITT recommendation X.30. The circuit I109 will be delayed to have a change at the first 1 to 0 transition of S114 after the 1 to 0 transition of circuit B (B115). The timing relation between B115, S114 and I109 is depicted in figure 2.9.1.4-1.

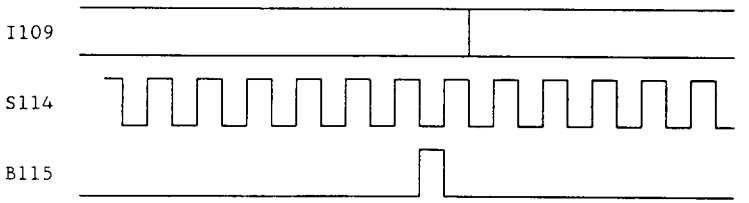


Figure 2.9.1.4-1 the timing relation between the outgoing interchange circuits when NoCCITT is set to '0'.

When the EDRA is in X.30 mode and bit NoCCITT is '1', the NOT CCITT compatible mode is selected: I109 will be changed at the 1 to 0 transition of S114 when B is 1, at this same moment the 8th databit will be clocked out on circuit R104; so I109 is one bit earlier as defined in CCITT's X.30. The timing relations when the outgoing interchange circuits are not in the CCITT compatible mode are depicted in figure 2.9.1.4-2.

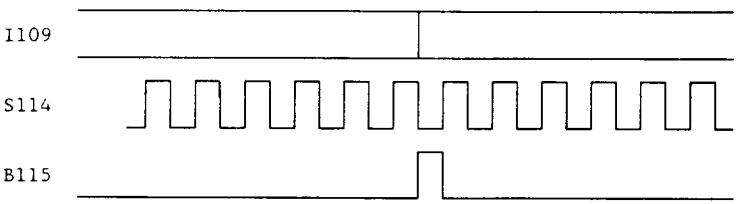


Figure 2.9.1.4-2 the timing relation between the outgoing interchange circuits when NoCCITT is set to '1'.

Bit E7: The E7 bit is used for the data rate setting in the 10 bytes frame for user data rates > 1200 bit/s. For lower speeds this bit is internally used for multiframe synchronisation and is coded as is illustrated in table 2.9.1.4-3.

Bit FM0 and FM1: With bit FM0 and FM1 the intermediate frame speed can be selected when submultiplexing on the synchronous data interface is needed. When no submultiplexing is used, 64 kbit/s should be selected. The coding of the bits FM0 and FM1 is illustrated in table 2.9.1.4-4.

FM1	FM0	intermediate data rate
0	0	8000
0	1	16000
1	0	32000
1	1	64000

Table 2.9.1.4-4 Intermediate data rate selection

Data rate 600 bit/s:

multiframe 1	00000000	1PPPPPPS 111111	1PPPPPPX 112222	1PPPPPPS 222233	1PPPPPPS 333333
	1EEEEEE1 123456	1PPPPPPS 444444	1PPPPPPX 445555	1PPPPPPS 555566	1PPPPPPS 666666
multiframe 2	00000000	1PPPPPPS 777777	1PPPPPPX 778888	1PPPPQQS 888811	1QQQQQQS 111111
	1EEEEEE1 123456	1QQQQQQS 222222	1QQQQQQX 223333	1QQQQQQS 333344	1QQQQQQS 444444
multiframe 3	00000000	1QQQQQQS 555555	1QQQQQQX 556666	1QQQQQQS 666677	1QQQQQQS 777777
	1EEEEEE1 123456	1QQQQQQS 888888	1QQRRRRX 881111	1RRRRRRS 111122	1RRRRRRS 222222
multiframe 4	00000000	1RRRRRRS 333333	1RRRRRRX 334444	1RRRRRRS 444455	1RRRRRRS 555555
	1EEEEEE0	1RRRRRRS 666666	1RRRRRRX 667777	1RRRRRRS 777788	1RRRRRRS 888888

After four multiframes, the E7 bit changes from 1 to 0, which indicates that three complete data bytes have been transmitted.

Data rate 1200 bit/s:

multiframe 1	00000000	1PPPPPPS 111122	1PPPPPPX 223333	1PPPPPPS 444455	1PPPPPPS 556666
	1EEEEEE1 123456	1PPPPPPS 777788	1PPQQQQX 881111	1QQQQQQS 222233	1QQQQQQS 334444
multiframe 2	00000000	1QQQQQQS 555566	1QQQQQQX 667777	1QQQQRRS 888811	1RRRRRRS 112222
	1EEEEEE0 123456	1RRRRRRS 333344	1RRRRRRX 445555	1RRRRRRS 666677	1RRRRRRS 778888

After two multiframes, the E7 bit changes from 1 to 0, which indicates that three complete data bytes have been transmitted.

Table 2.9.1.4-3 Multiframe synchronisation.

Bits SG2,SG1 and SG0. These bits are the submultiplex code bits. They determine the bit position in the SDO timeslot where the EDRA will insert data (see section 2.4).

SG2	SG1	SG0	bitpositions for intermediate: 8000	16000	32000	64000
0	0	0	0	0 1	0 1 2 3	-
0	0	1	1	2 3	4 5 6 7	-
0	1	0	2	4 5	-	-
0	1	1	3	6 7	-	-
1	0	0	4	-	-	-
1	0	1	5	-	-	-
1	1	0	6	-	-	-
1	1	1	7	-	-	-

Table 2.9.1.4-5 Submultiplex code bits

Bit SDO=1. When bit SDO=1 is set to '1', the EDRA will clamp the outgoing data on the ssynchronous data interface to '1'.

2.9.1.5. Register W04

Bit RxGIE: Bit RxGIE bit (when set to '1') enables the URF-receiver activity checkers (register R27) to generate interrupts. These activity checkers can be individually enabled in register W13.

Bit TxGIE: Bit TxGIE (when set to '1') enables the URF-transmitter activity checkers to give interrupts. These activity checkers (register R20) can be individually enabled in register W13.

Bit OOSIE, when set to '1', enables the activity checker OOSact (register R20) to give interrupts. The OOSstate can be read in register R22.

Bit THGIE, when set to '1', enables the URF-FIFO threshold activity checkers to give interrupts. The activity and status of the FIFO thresholds can be read in register R28.

Bit ICGIE (when set to '1') enables the interchange circuits activity checkers to give interrupts. The activity checkers can be individually enabled in registers W05 and W08. The status and activity bits of the interchange circuits can be read in registers R21, R22, R23 and R24.

Bit MIE. When bit MIE is set to '0', all EDRA interrupts are disabled.

2.9.1.6. Register WO5

Bit SXI controls the programmable inverters on the interchange input circuits. This control is necessary to define the binary state of ON and OFF according CCITT definition or to be compatible with the DRA (PCB2320).

If SXI is made '0', the inputs have no inversion and the S- and X-bits in the synchronous data interface stream are CCITT compatible (ON=0, OFF=1). When SXI is made '1', the inputs are inverting and the EDRA is DRA compatible (ON=1, OFF=0). Bit SXI influences only the S- and X-bit definition in the 64 kbit/s data stream. The readouts and clampings of the input interchange circuits remain as in CCITT compatible mode.

Bit DTE106IE: when bit DTE106IE is set to '1', the EDRA generates an interrupt on the setting of DTE106 activity bit (register R21).

Bit M01IE: when bit M01E is set to '1', the EDRA generates an interrupt on the setting of M01 activity bit (register R21).

Bit M02IE: when bit M02IE is set to '1', the EDRA generates an interrupt on the setting of M02 activity bit (register R21).

Bit V108IE: when bit V108IE is set to '1', the EDRA generates an interrupt on the setting of V108 activity bit (register R21).

Bit C105IE: when bit C105IE is set to '1', the EDRA generates an interrupt on the setting of C105 activity bit (register R21).

Bit T103IE: when bit T103IE is set to '1', the EDRA generates an interrupt on the setting of T103 activity bit (register R21).

Bit R104IE: when bit R104IE is set to '1', the EDRA generates an interrupt on the setting of R104 activity bit (register R21).

2.9.1.7. Register W06

Bit T103/1 and T103/0: With T103/0 and T103/1 it is possible to control input T103. The input can be clamped (internally) to '0' or '1' or the EDRA accepts input on lead T103. For the settings of T103/0 and T103/1 is referred to table 2.9.1.7-1.

T103/1	T103/0	T103
0	0	EDRA accepts data on T103
0	1	T103 is internally clamped to 0
1	X	T103 is internally clamped to 1

Table 2.9.1.7-1 Settings of T103/0 and T103/1.

Bit C105/1 and C105/0: With C105/0 and C105/1 it is possible to control input C105. The input can be clamped (internally) to '0' or '1' or the EDRA accepts input on lead C105. For the settings of C105/0 and C105/1 is referred to table 2.9.1.7-2.

C105/1	C105/0	C105
0	0	EDRA accepts data on C105
0	1	C105 is internally clamped to 0
1	X	C105 is internally clamped to 1

Table 2.9.1.7-2 Settings of C105/0 and C105/1.

Bit V108/1 and V108/0: With V108/0 and V108/1 it is possible to control input V108. The input can be clamped (internally) to '0' or '1' or the EDRA accepts input on lead V108. For the settings of V108/0 and V108/1 is referred to table 2.9.1.7-3.

V108/1	V108/0	V108
0	0	EDRA accepts data on V108
0	1	V108 is internally clamped to 0
1	X	V108 is internally clamped to 1

Table 2.9.1.7-3 Settings of V108/0 and V108/1.

Bit DTE106/1 and DTE106/0: With DTE106/0 and DTE106/1 it is possible to control input DTE106. The input can be clamped (internally) to '0' or '1' or the EDRA accepts input on lead DTE106. For the settings of DTE106/0 and DTE106/1 is referred to table 2.9.1.7-4.

DTE106/1	DTE106/0	DTE106
0	0	EDRA accepts data on DTE106
0	1	DTE106 is internally clamped to 0
1	X	DTE106 is internally clamped to 1

Table 2.9.1.7-4 Settings of DTE106/0 and DTE106/1.

2.9.1.8. Register W07

Bits S1, X2, S3, S4, S6, X7, S8, S9: In μC mode these bits that are transferred in the frame over the synchronous data interface, can be programmed by the microcontroller. Setting these bits is only useful when the μC-mode is selected in register W00.

note: for speeds > 38.4 kbit/s not all bits are transferred in the 4 bytes frame (see section 2.3) (it of no use programming the bits that are not transferred).

2.9.1.9. Register W08

Bits S1IE, X2IE, S3IE, S4IE, S6IE, X7IE, S8IE, S9IE. If one of these bits is set to '1' the interrupt is enabled on the related activity bit (register R23). If the related activity bit is set an interrupt is generated by the EDRA.

2.9.1.10. Register W09

Bits R104/0 and R104/1: With R104/0 and R104/1 it is possible to control output R104. The output can be clamped to '0' or '1' or is indicating the received data bits. For the settings of R104/0 and R104/1 is referred to table 2.9.1.10-1.

R104/1	R104/0	R104
0	0	EDRA indicates on R104 the received D bits
0	1	R104 is internally clamped to 0
1	X	R104 is internally clamped to 1

Table 2.9.1.10-1 Settings of R104/0 and R104/1.

Bits DCE106/1 and DCE106/0: With DCE106/1 and DCE106/0 it is possible to control output DCE106. The output can be clamped to '0' or '1' or is indicating the X7- and/or X2-bits (see section 2.3). For the settings of DCE106/1 and DCE106/0 is referred to table 2.9.1.10-2.

DCE106/1	DCE106/0	DCE106
0	0	EDRA indicates on DCE106 the received X bits
0	1	DCE106 is internally clamped to 0
1	X	DCE106 is internally clamped to 1

Table 2.9.1.10-2 Settings of R104/0 and R104/1.

Bit V107/0 and V107/1: With V107/0 and V107/1 it is possible to control output V107. The output can be clamped to '0' or '1' or is indicating the received S1-, S3-, S6- and S8-bits (see section 2.3). For the settings of V107/0 and V107/1 is referred to table 2.9.1.10-3.

V107/1	V107/0	V107
0	0	EDRA indicates on V107 the received S bits
0	1	V107 is internally clamped to 0
1	X	V107 is internally clamped to 1

Table 2.9.1.10-3 Settings of V107/0 and V107/1.

Bits I109/1 and I109/0: With I109/1 and I109/0 it is possible to control output I109. The output can be clamped to logic '0' or '1' or is indicating the received S9- and/or S4-bits (see section 2.3). For the settings of I109/1 and I109/0 is referred to table 2.9.1.10-4.

I109/1	I109/0	I109
0	0	EDRA indicates on I109 the received S bits
0	1	I109 is internally clamped to 0
1	X	I109 is internally clamped to 1

Table 2.9.1.10-4 Settings of I109/1 and I109/0.

2.9.1.11. Register W10

Bit SXO: Bit SXO controls the programmable inverters on the interchange output circuits. This control is necessary to program the relation between the binary values of S- and X-bits and the states (ON and OFF) of the interchange circuits. This relation can be according CCITT definition or ECMA-102 september '84 (to be compatible with the DRA (PCB2320)).

If SXO is made '0', the outputs have no inversion and the S- and X-bits in the synchronous data interface stream are interpreted according CCITT standard (ON=0, OFF=1). When SXO is made '1', the outputs are inverting and the EDRA is DRA compatible (ON=1, OFF=0). Bit SXO influences only the interpretation of the S- and X-bits in the 64 kbit/s data stream. The readouts and clampings of the input interchange circuits remain as in CCITT compatible mode.

Bit MO2: With this bit, the state of output pin MO2 can be set or reset by the micro controller. When MO2 is made '1' the output is '1' (5V), a '0' results in 0V at the MO2 output.

Bit S114=1. When this bit is set to '0', the output S114 delivers the timing signals S114 as described in section 2.3.3. When S114=1 is set to '1', the output is clamped to '1' (5V). See figure 2.9.1.11-1.

Bit B115=1. When this bit is set to '0', the output S114 delivers the timing signals B115 as described in section 2.3.3. When B115=1 is set to '1', the output is clamped to '1' (5V). See figure 2.9.1.11-1.

Bit MO1: With this bit, the state of output pin MO1 can be set or reset by the micro controller. When MO1 is made '1' the output is '1' (5V), a '0' results in 0V at the MO1 output.

Bit TXsBr: When this bit is set '1' the EDRA generates a break condition on circuit R104 (as long as this bit is '1'). The current character that is transmitted will be corrupted while the next characters will be stored in the Tx-FIFO.

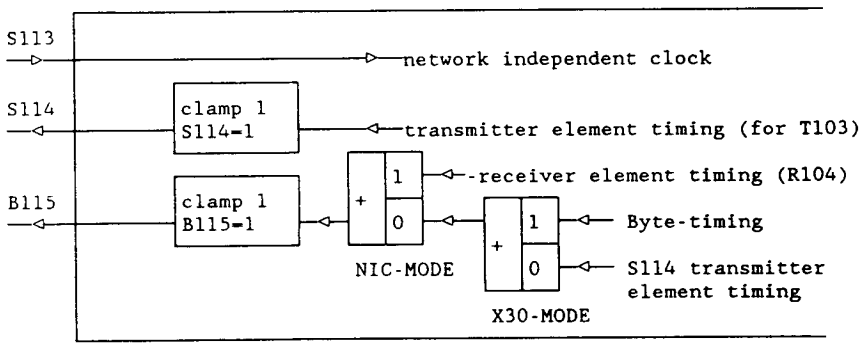


Figure 2.9.1.11-1 Interchange circuits B115 and S114.

2.9.1.12. Register W11

Bit CC0 - CC7: Bit CC0 - CC7 are the command code bits. With these bits data settings of the URF transmitter/receiver blocks can be set. In table 2.9.1.12-1 the settings of CC0 - CC7 are illustrated.

CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0	action
1	-	-	-	-	0	-	1	reset FIFOs
0	-	0	-	0	-	0	1	5 bits/character
0	-	0	-	0	-	1	0	7 bits/character
0	-	0	-	0	-	1	1	8 bits/character
0	-	0	0	1	0	0	-	none parity
0	-	0	0	1	1	0	0	odd parity
0	-	0	0	1	1	0	1	even parity
0	-	0	0	1	1	1	0	space parity
0	-	0	0	1	1	1	1	mark parity
0	-	0	1	1	0	1	0	1 stopbit
0	-	0	1	1	0	1	1	2 stopbits *4)
1	-	-	-	-	1	-	0	Tx sends one X-ON (on lead R104)
1	-	-	-	-	1	-	1	Tx sends one X-OFF (on lead R104)
0	-	1	0	-	0	0	0	Rx X-ON filter OFF (on lead T103) *0)
0	-	1	0	-	0	0	1	Rx X-ON filter ON (on lead T103) *1)
0	-	1	0	-	0	1	0	Rx X-OFF filter OFF (on lead T103) *0)
0	-	1	0	-	0	1	1	Rx X-OFF filter ON (on lead T103) *1)
0	-	1	0	-	1	-	0	auto XON/XOFF (on lead T103 and R104)
0	-	1	0	-	1	-	1	auto circuit 106 *3)
0	-	1	1	-	0	0	1	Tx transmit enabled (lead R104) *0)
0	-	1	1	-	0	0	0	Tx transmit disabled (lead R104)
0	-	1	1	-	0	1	1	Tx transmit enabled, controlled by the local DTEs lead T103 X-ON/X-OFF *1)
0	-	1	1	-	1	0	1	Rx transmit enabled (synchronous data interface) *0)
0	-	1	1	-	1	0	0	Rx transmit disabled (synchronous data interface)
0	-	1	1	-	1	1	-	Rx transmit enabled, controlled by the remote EDRAs X-bit *2)

Figure 2.9.1.12-1 Selections for URF (UART/RA0/Flowcontrol).

*0) automatic selected at any write action in register W00.
*1) automatic selected in auto X-ON/X-OFF mode if flowcontrol is selected in register W00.
*2) automatic selected at selection of flowcontrol in register W00.

*3) there is always an automode selected. This means that for other modes than the flowcontrol mode, lead DCE106 should be coupled directly to the incoming X-bits, the auto X-ON/X-OFF must be selected, in combination with Rx-threshold level setting at FF-Hex, unless auto X-ON/X-OFF is wanted for local flowcontrol purposes.
*4) in two stopbit mode, the receiver checks on two stop-elements

Note 1: bits/char, partity and number of stopbit: no default setting, must all be set when using URF (mode 1B, 1C and 1D), For mode 2, 3A, 3B and 3C (only 8 bits character has to be programmed).

Note 2: Tx send one X-ON/X-OFF: after the current character is transmitted, a X-ON or X-OFF will be transmitted to the local DTE. This can be usefull when in using RA0. When this feature is used in flowcontrol mode (mode 1C), one should realise that this manual X-ON/X-OFF will disturb the auto generated X-ON/X-OFF or DTE106.

Note 3: Rx X-ON/X-OFF filters, AUTO X-ON/X-OFF/ AUTO DCE106: one of these modes must be set. See chapter 2.5.3.

Note 4: Tx and Rx transmit enabled/disabled: see chapter 2.5.3.

2.9.1.13. Register W12

Bits TH1A1 - TH1A4: bits TH1A1 - TH1A4 contain the threshold level 1 of the receiver FIFO (see section 2.5.3.1). It indicates an odd addresses (with TH1A1 -TH1A4 address 1 upto 31 can be selected the least significant bit is always 1).

Bits TH2A1 - TH2A4: bits TH2A1 - TH2A4 contain the threshold level 2 of the receiver FIFO (see section 2.5.3.1). It indicates an odd addresses (with TH2A1 -TH2A4 address 1 upto 31 can be selected the least significant bit is always 1).

2.9.1.14. Register W13

Bit XonXoffIE: This bit enables the URF receiver X-ON and X-OFF activity bits (see register R26) to generate interrupts.

Bit TxAllSeIE: This bit enables the EDRA to generate an interrupt when activity bit Txallsent (register R20) becomes '1'.

Bit TxFIFOeIE: This bit enables the EDRA to generate an interrupt when the bit TxFIFOempty state (register R20) becomes '1'.

Bit RXChAvIE: This bit enables the EDRA to generate an interrupt if the char.av activity (register R27) becomes '1'.

Bit Rx/TxOfIE: This bit enables the EDRA to generate an interrupt at the moment the overflw act. bit (register R27) or the Tx FIFO overfl. activity bit (register R20) become '1'.

Bit RxBreakIE: When this bit is made '1' the EDRA generates an interrupt when the break state bit (register R27) becomes '1'.

Bit RxParIE: When this bit is made '1' it enables the EDRA to generate an interrupt at the moment the frmerr activity bit (register R27) is '1'.

Bit RxFrEr: When this bit is set ('1') the EDRA genrates an interrupt at the moment the frmerr activity bit (register R27) is set (has become '1').

2.9.1.15. Register W14

Bits TH1A1 - TH1A4: bits TH1A1 - TH1A4 contain the threshold level 1 of the transmitter FIFO (see section 2.5.3.1). It indicates an odd addresses (with TH1A1 -TH1A4 address 1 upto 31 can be selected the least significant bit is always 1).

Bits TH2A1 - TH2A4: bits TH2A1 - TH2A4 contain the threshold level 2 of the transmitter FIFO (see section 2.5.3.1). It indicates an odd addresses (with TH2A1 -TH2A4 address 1 upto 31 can be selected the least significant bit is always 1).

2.9.1.16. Register W15

The data can be written by microcontroller to the UART, via this write register. Before a byte can be written, the TxFIFOoverfl activity bit in register R20 must be '0'.

2.9.1.17. Register W16

In this register the flowcontrol X-ON character code can be downloaded.

2.9.1.18. Register W17

In this register the flowcontrol X-OFF character code can be downloaded.

2.9.2. Registers R20-R28

General activity/state register:

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R20	Tx FIFO overfl. act.	Tx FIFO empty state	Tx all sent act.	-	IC group act.	TH group act.	OOS act.	Rx group act.

Table 2.9.2-1 Bit assignment;register R20.

Input interchange circuits activity indications:

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R21	R104ACT 0-1/1-0	T103ACT 0-1/1-0	C105ACT 1-0	C105ACT 0-1	V108ACT 1-0	V108ACT 0-1	MI1/MI2 0-1/1-0	DTE106 0-1/1-0

Table 2.9.2-2 Bit assignment;register R21.

Input interchange circuits status indications:

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R22	-	OOS state	C105	-	V108	MI2	MI1	DTE106

Table 2.9.2-3 Bit assignment;register R22.

Output interchange circuits activity indications:

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R23	S9 ACT 0-1/1-0	S8 ACT 0-1/1-0	X7 ACT 0-1/1-0	S6 ACT 0-1/1-0	S4 ACT 0-1/1-0	S3 ACT 0-1/1-0	X2 ACT 0-1/1-0	S1 ACT 0-1/1-0

Table 2.9.2-4 Bit assignment;register R23.

Output interchange circuits status indications:

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R24	S9	S8	X7	S6	S4	S3	X2	S1
R25	E7	E6	E5	E4	E3	E2	E1	-

Table 2.9.2-5 Bit assignment;register R24 and R25.

UART receive buffer:

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R26	RX7	RX6	RX5	RX4	RX3	RX2	RX1	RX0

Table 2.9.2-6 Bit assignment;register R26.

URF receiver state/activity register:

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R27	Xon det act.	Xoff act.	FIFOemp state	frm.err act.	par.err act.	break state	overflw act.	char.av act

Table 2.9.2-7 Bit assignment;register R27.

FIFO threshold status and activity register:

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R28	Tx TH1 state	Tx TH2 state	Tx TH1 act.	Tx TH2 act.	Rx TH1 state	Rx TH2 state	Rx TH1 act.	Rx TH2 act.

Table 2.9.2-8 Bit assignment;register R28.

2.9.2.1. Register R20

Bit Rx group act.: Receiver Group activity (URF-bit). This bit indicates that one of more receiver activity bits have become '1'. This activity-bits can not be read but the status bits that caused the activity can be read in register R27. After this read cycle the activity bits will be reset and the INTN lead goes HIGH (non active).

OOSact.: 64 kbit/s channel Out Of Synchronisation. This activity bit indicates the in-synchronisation to out-synchronisation transition of the synchronisation mechanism in the CS. This for all speed-setting in W01, exept for synchronous 56 and 64 kbit/s. For these speeds, this bit will always be '0' (in synchronisation). After readout the activity bit will be reset. The status bit OOS state in register R22 indicates the real time state of synchronisation.

While synchronising, the incoming datastream on SDI is checked for frame synchronisation bits. If they don't appear on the expected position in the frame, this can have two causes: The clockunit must be presetted to the right value or one of more frame synchronisation bits have been distorted.

For the ten bytes frame:

The EDRA gives out of synchronisation after three consecutive incorrect multiframes (with one or more errors per multiframe) and starts searching for the right timing:
-After receiving the eight zero frame bits the clockunit is preset to the right value,
-If the following frame-bits in that multiframe are received correctly, the EDRA is in synchronisation and OOS state in register R22 will be reset.
-If they are not all correct the OOS bit remains '1' and the EDRA will search for the next 8 zero frame-bits.

For the four bytes frame:

The EDRA gives out of synchronisation after three consecutive incorrect frames of 4-bytes (with one or more errors per frame) and starts searching for the right timing:

-The incoming data on the synchronous data interface have correct octet-orientation.
-After receiving the 1011-pattern in the frame synchronisation bits, the EDRA is in synchronisation and the OOS state bit will be reset.
-If they are not all correct the OOS state bit remains '1' and the EDRA will continue searching for the synchronisation pattern.

Bit TH group act.: Threshold group activity bit. This bit indicates that one of the receiver or transmitter threshold activity checkers is active ('1').

Bit IC group act.: Interchange circuits group activity. This bit indicates that one or more of the IC activity checkers are active ('1').

Bit Tx all sent act.: Tx all sent activity bit. This bit becomes '1' when all characters have completely cleared the transmitter. It will be reset after reading register R20.

Bit Tx FIFO empty state: Tx FIFO empty state bit. When this bit is '1', the Tx FIFO contains no more data.

Bit Tx FIFO overfl. act.: When this bit becomes '1', it indicates that a Tx FIFO overflow has occurred. This bit is reset after reading register R20.

2.9.2.2. Register R21

Bit DTE1060-1/1-0: Activity check bit on input DTE106. If any signal changes on this input pin occur, this bit is set '1'.

MI1/MI20-1/1-0: Activity check bit on inputs MI1 and MI2. If any signal changes on one of these input pins occur, this bit is set '1'.

Bit V108act0-1: Activity check bit on input V108. If any signal changes from 0 to 1 occur on this input pin, this bit is set '1'.

Bit V108act1-0: Activity check bit on input V108. If any signal changes from 1 to 0 occur on this input pin, this bit is set '1'.
Bit C105act0-1: Activity check bit on input C105. If any signal changes from 0 to 1 occur on this input pin, this bit is set '1'.

Bit C105act1-0: Activity check bit on input C105. If any signal changes from 1 to 0 occur on this input pin, this bit is set '1'.

Bit T103ACT0-1/1-0: Activity check bit on input T103. If any signal changes on this input pin occur, this bit is set '1'.

Bit R104ACT0-1/1-0: Activity check bit on output R104. If any signal changes on this input pin occur, this bit is set '1'.

2.9.2.3. Register R22

Bit DTE106, MI1, MI2, V108, C105: These bits indicate the actual state of the input they are named after. If the input is HIGH (5V) the bit is '1'. If the inupt is LOW (0V) the bit is '0'.

Bit OOS state: It gives the actual state of the synchronisation system of the EDRA. This for all user data rates, exept for synchronous 56 and 64 kbit/s. For these speeds, this bit is always '0' (in synchronisation).

2.9.2.4. Register R23

Bit S9 ACT 0-1/1-0, S8 ACT 0-1/1-0, X7 ACT 0-1/1-0, S6 ACT 0-1/1-0, S4 ACT 0-1/1-0, S3 ACT 0-1/1-0, X2 ACT 0-1/1-0, S1 ACT 0-1/1-0: These bit are activity bits and are set to '1' is any signal changes occur in the S and X-bits of the incoming frame on pin SDI (synchronous data input).

In case of a 4 bytes frame only S1/X2/S3/S4 contain valid information.

2.9.2.5. Register R24

Bits S1, X2, S3, S4, S6, X7, S8, S9: contain the actual state of the bits they are named after. The information in these bits is filled in by the remote EDRA.

In case of a 4 bytes frame only S1/X2/S3/S4 contain valid information.

2.9.2.6. Register R25

Bits E1, E2, E3, E4, E5, E6, E7: In every 10 bytes multi-frame (for speeds not exeeding 38400 bit/s), 7 E-bits are available. The information filled in by the remote subscriber is received in these bits.

These bits are only applicable in a 10 bytes frame.

2.9.2.7. Register R26

Bits RX0 - RX7: Data bytes of the UART receive buffer can be read out of this register.

2.9.2.8. Register R27

Bit char.av.act.: The character available activity bit indicates that a character can be read out of the UART Rx buffer. An interrupt will be given, if the interrupt source in the EDRA is enabled in register W13. Character available is an activity bit, and will be reset after reading register R27.

Bit overflw act.: Receive FIFO overflow error activity bit. This bit indicates that the receive FIFO has an overflow. This bit is an activity bit, and will be reset after reading register R27. If enabled in W13, an interrupt will be given by the EDRA when this bit is set (become '1').

Bit break state. This bit is set ('1') when a break sequence has been detected, and will last as long as this condition is present, If enabled, in register W13 an interrupt will be given by the EDRA at the moment this bit is set.

Bit par.err.act.: Parity Error activity bit. When parity is enabled, this bit is set for the characters whose parity do not match the programmed sense. It is an activity bit, and will be reset after reading register R27. It pops with the data, so must be read before reading the UART receive buffer (register R26). When the parity error bit is set, and the interrupt is enabled in register W13, an interrupt will be given.

Bit frm.err act. This bit is set ('1') when the stop bit is not found. It is an activity bit, and will be reset after reading register R27. It pops with the data. When enabled in register W13 the EDRA generates an interrupt when this bit is set.

Bit FIFOemp state: Rx FIFO empty. This is a state bit and is set when no characters are left in the 32 bytes Rx-FIFO.

Bit Xoff act.: Rx X-OFF detection. This activity bit is set when an incoming character on lead T103 is equal to the character written in register W17. This bit is reset after reading register W27.

Note: The incoming character may not contain frame or parity error.

Bit Xon det act.: Rx X-ON detection. This activity bit is set when an incoming character on lead T103 is equal to the character written in register W16. The bit is reset after reading register W27.

Note: The incoming character may not contain frame or parity error.

2.9.2.9. Register R28

Bit Rx TH2 act.: It indicates the 0/1 transition of the receiver TH2 state. If enabled in register W04, the EDRA generates an interrupt on the setting of this bit.

Bit Rx TH1 act.: It indicates the 0/1 transition of the receiver TH1 state. If enabled in register W04, the EDRA generates an interrupt on the setting of this bit.

Bit Rx TH2 state: When this bit is '1', the contents of this FIFO is equal or passed the receiver FIFO TH2 (lower) threshold.

Bit Rx TH1 state: This bit indicates the state of the receiver FIFO. When this bit is '1', the contents of this FIFO is equal or passed the TH1 (upper) threshold.

Bit Tx TH2 act.: It indicates the 0/1 transition of the transmitter TH2 state. If enabled in register W04, the EDRA generates an interrupt on the setting of this bit.

Bit Tx TH1 act.: It indicates the 0/1 transition of the transmitter TH1 state. If enabled in register W04, the EDRA generates an interrupt on the setting of this bit.

Bit Tx TH2 state: When this bit is '1', the contents of this FIFO is equal or passed the transmitter FIFO TH2 (lower) threshold.

Bit Tx TH1 state: This bit indicates the state of the transmitter FIFO. When this bit is '1', the contents of this FIFO is equal or passed the TH1 (upper) threshold.

3. Testability

The EDRA has two test modes on board: A boudary scan test and a possiblity to make all output pins high-Z. These test modes can be set by three control pins: SCC, BSE and BSI. With these pins the next modes are selectable:

BSI	BSE	SCC	MODE
x	0	0	normal
0	1	1	high-Z
x	1	0	boundary shift

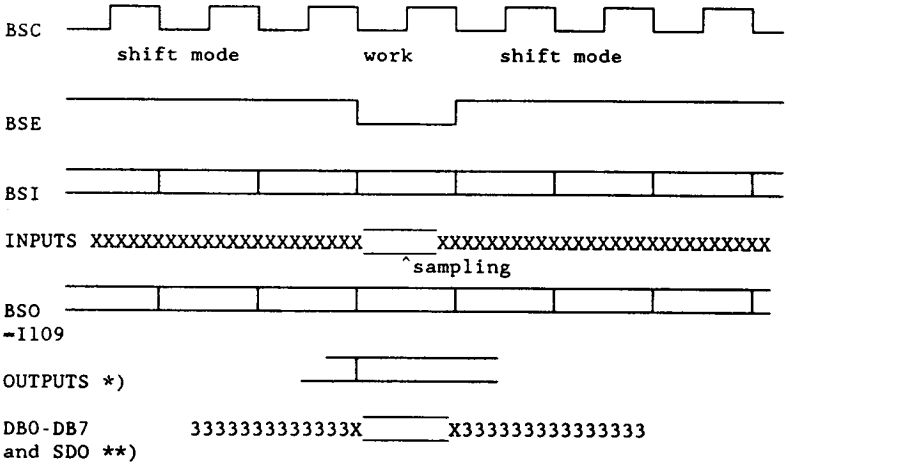
Table 3-1 Testmode setting

For testing after PCB assembly two features are interesting: the high-Z mode and the boundary scantest. In the high-Z mode, all chip outputs are high impedance, which will make testing of other devices mounted on the PCB easier.

The boundary scantest enables to check the connections between the chippads and the PCB. The boundary test is a method to check the connections of the chip-pads to the PCB. In the boundary scan mode, all output pins can be set, and all input pins can be sensed, via the boundary scanline.

Testvalues should be driven from electrical specification.

In the following figure the functional timing is illustrated in the boudary scan testmode:



*) except DB0 - DB7 and SDO
**) High-Z during shift, in workmode dependent of B20/B21 see table 3.3

Figure 3.2 Functional timing in boundary-scan mode.

In the shift mode, BSE=1, the databus and the SDO pin are high-Z. In the work cycle, where inputs are sampled in the scanline, and outputs are forced, the direction of the databus and the mode of the SDO pin is determined by two boundary chain elements: B01 and B02;

control	behaviour in workcycle
B01 = 0 = 1	DB0 - DB7 are high-Z, databus in inputmode DB0 - DB7 in output mode from chain elements B09- B16
B02 = 0 = 1	HWO is high-Z HWO is in output mode, from chain element B19

Boundaryscan chainorder:

NR.	NAME	SHIFT FROM	WORK DATA IN	WORK DATA OUT	
1	B01	BSI-pin	T103	PQ01 (data bus)	*
2	B02	B01	SCC	PQ02 (synchr. data interface)	*
3	B03	B02	internal CQ11		
4	B04	B03	internal CQ13		
5	B05	B04	SCLK		
6	B06	B05	MCLK		
7	B07	B06	RDN		
8	B08	B07	WRN		
9	B09	B08	DB0	DB0	
10	B10	B09	DB1	DB1	
11	B11	B10	DB2	DB2	
12	B12	B11	DB3	DB3	
13	B13	B12	DB4	DB4	
14	B14	B13	DB5	DB5	
15	B15	B14	DB6	DB6	
16	B16	B15	DB7	DB7	
17	B17	B16	CSN	INTN	
18	B18	B17	ALE		
19	B19	B18	FSX	SDO	
20	B20	B19	FSR		
21	B21	B20	SDI	B115	
22	B22	B21	S113	MI2	
23	B23	B22	V108	MO2	
24	B24	B23	MI1	V107	
25	B25	B24	MI2	S114	
26	B26	B25	DTE106	DCE106	
27	B27	B26	C105	R104	
28	B28	B27		I109 - BSO	

4. DC characteristics

4.1. Ratings

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
DC supply voltage		V_{DD}	-0.5	7.0	V
DC input diode current	V_I< -0.5 or V_I> Vdd+0.5	$\pm I_{IK}$	-	tbf	mA
DC output diode current	V_O< -0.5 or V_O> Vdd+0.5	$\pm I_{OK}$	-	tbf	mA
DC output sink current	-0.5 <V_O< Vdd + 0.5	$\pm I_O$	-	tbf	mA
DC output source current	-0.5 <VO< Vdd + 0.5	±IO	-	tbf	mA
DC V_{DD} current		$\pm I_{DD}$	-	tbf	mA
DC ground current		$\pm I_{GND}$	-	tbf	mA
Voltage on any pin		V_n	tbf	tbf	V
Storage temperature range		T_{stg}	tbf	tbf	^0C
Operating ambient temperature range		T_{amb}	-10	+75	^0C
Total power dissipation		P_{tot}	-	40	mW

4.2. DC characteristics

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
DC supply voltage		V_{DD}	4.5	5.5	V
Inputs					
Threshold voltage positive-going	$4.5 < V_{DD} < 5.5$ V	V_{T+}	-	2.0	V
negative-going	$4.5 < V_{DD} < 5.5$ V	V_{T-}	0.8	-	V
Input leakage current	$0 < V_I < Vdd$	I_{IL}	-	1.0	uA
Outputs (except SDO & DB0..7, INTN)					
Output voltage LOW	V_{DD} = 5 V I_{OL} = 2.0 mA	V_{OL}	-	0.4	V
Output voltage HIGH	VDD = 5 V -IOH = 2.0 mA	V_{OH}	4.0	-	V
3-state OFF current	$0 < V_O < V_{DD}$ I_O = 0	$\pm I_{OZ}$	-	10	µA
Outputs (SDO,DB0..7)					
Output voltage LOW	V_{DD} = 5 V I_{OL} = 4.0 mA	V_{OL}	-	0.4	V
Output voltage HIGH	VDD = 4.5 V -IOH = 4.0 mA	V_{OH}	4.0	-	V
3-state OFF current	$0 < V_O < V_{DD}$ I_O = 0	$\pm I_{OZ}$	-	10	µA
Outputs (INTN)					
Output voltage LOW	V_{DD} = 5 V I_{OL} = 2.0 mA	V_{OL}	-	0.4	V

5. AC Characteristics

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Input capacitance		C_I	-	tbf	pF
Input/ Output capacitance		$C_{I/O}$	-	tbf	pF
Output capacitance		C_O	-	tbf	pF

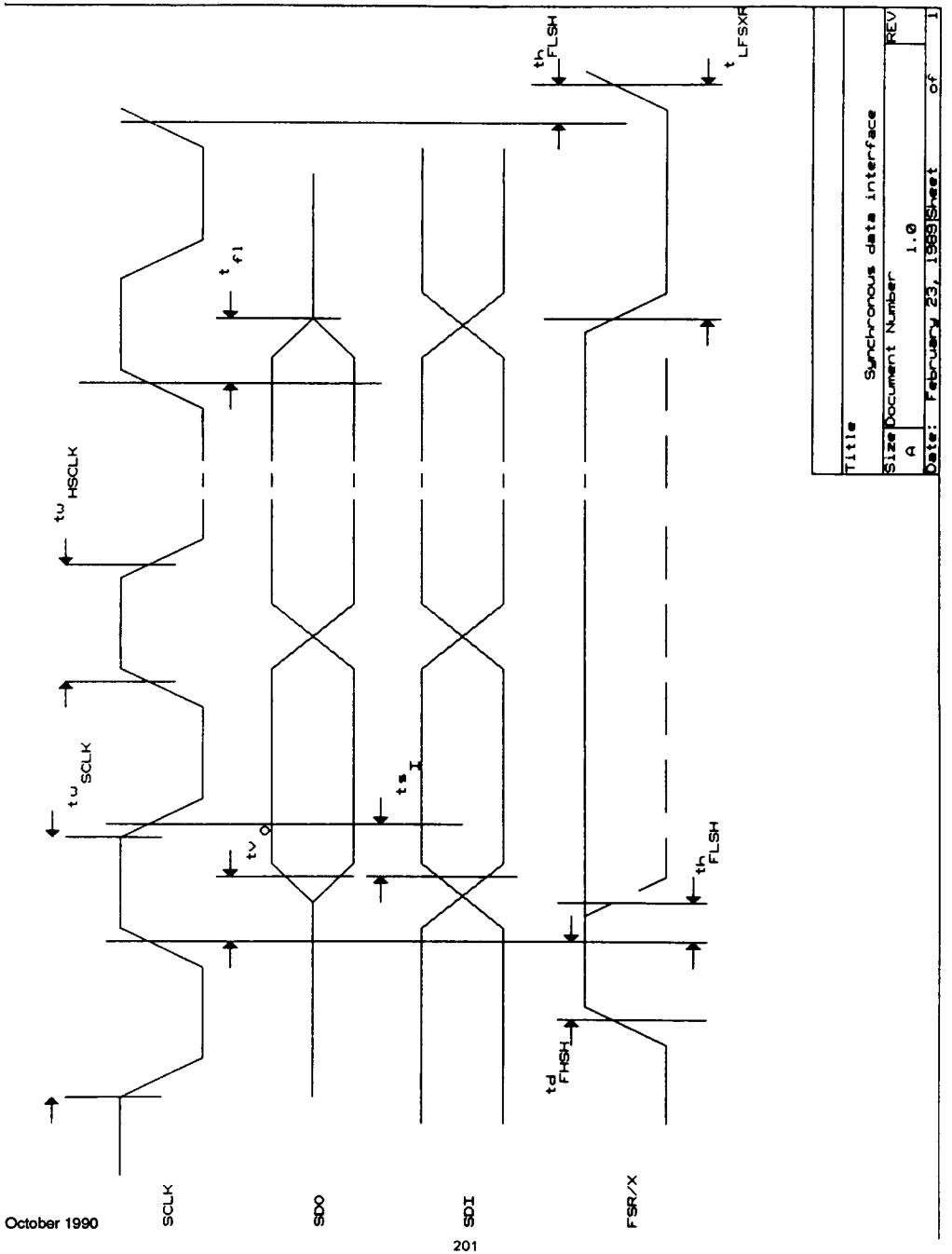
Timing measurements are specified for V_{il} at 0.4 and V_{ih} at 4.0 V, V_{ol} at 20% and V_{oh} at 80% of V_{DD}.

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Synchronous data interface					
FSX/R HIGH to SCLK HIGH		td_{FHSH}	100	-	ns
hold time FSX/R LOW after SCLK HIGH		th_{FLSH}	0	-	ns
hold time FSX/R HIGH after SCLK HIGH		th_{FHSH}	0	-	ns
FSX/R LOW time		t_{LFSXR}	tw_{SCLK}	-	
SDI data set up time		ts_I	100	-	ns
SDO valid after SCLK HIGH		tv_O	-	50	ns

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Synchronous data interface					
SDO floating after SCLK		t_{fl}	-	20	ns
SCLK period		tw_{SCLK}	488 (ns)	15.6	µs
SCLK HIGH time		t_{HSCLK}	50	-	ns

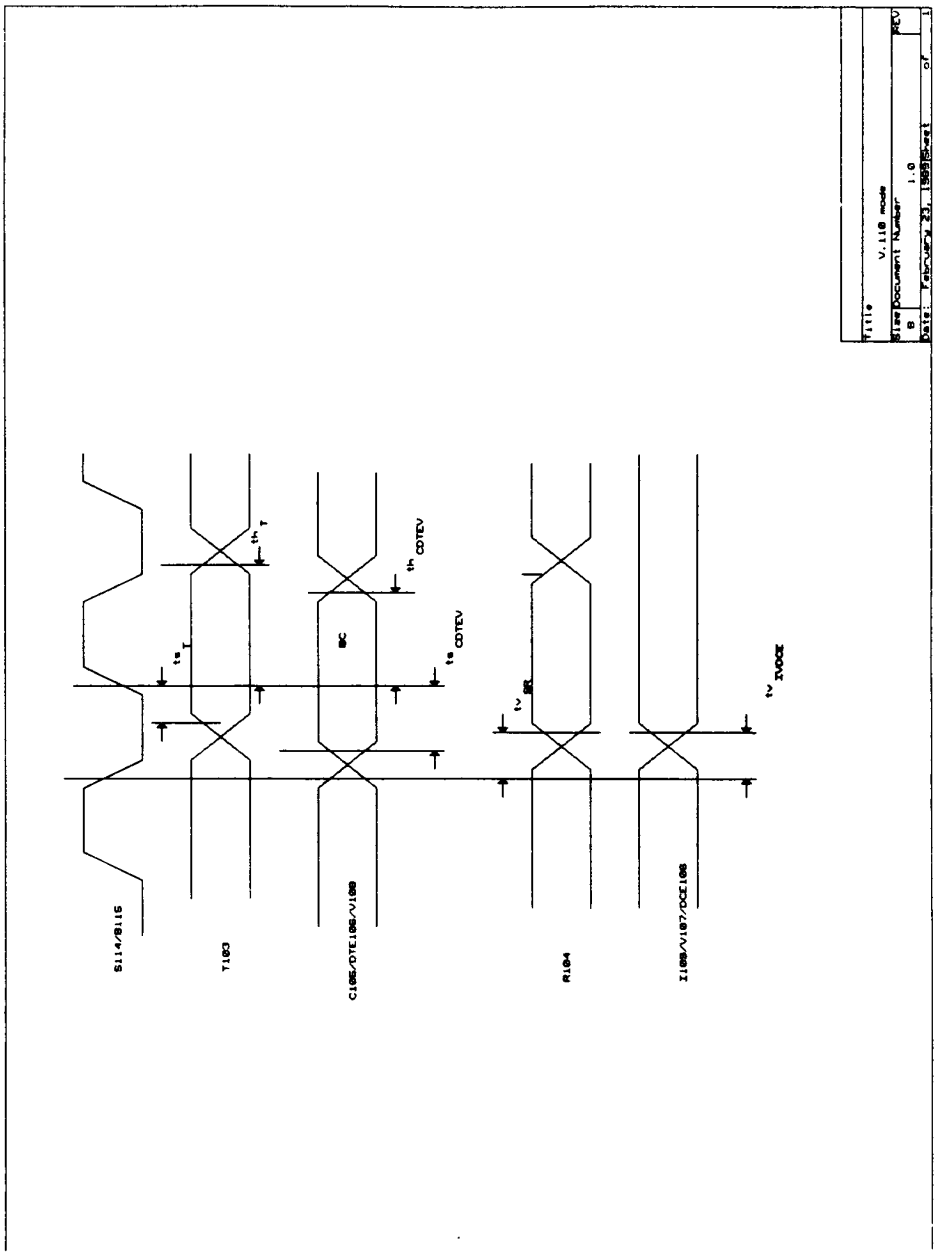
Extended data rate adaptor

PCB2325



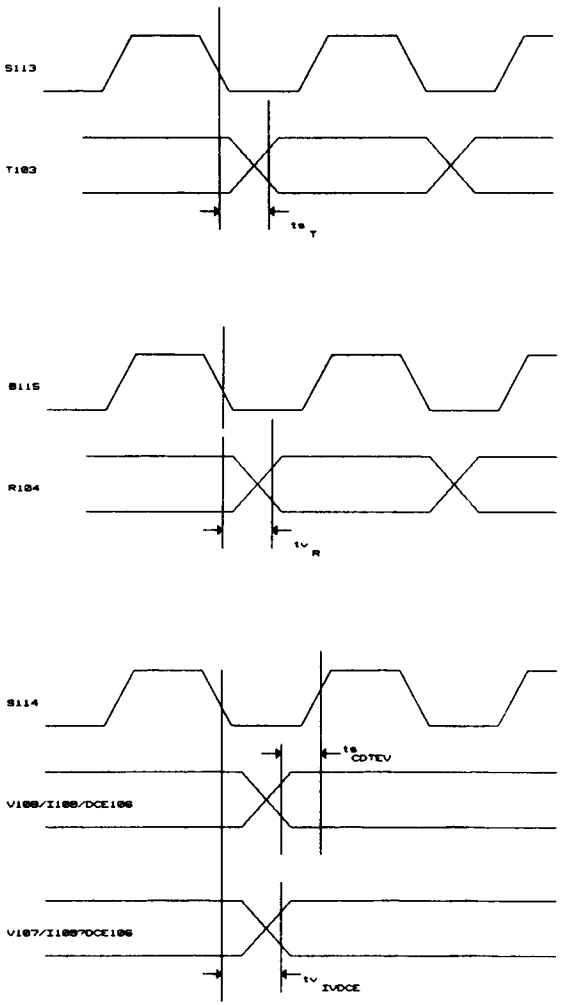
PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Interchange Interface					
V.110 mode without NIC					
T103					
data set up time		ts_T	100	-	ns
data hold time		th_T	0	-	ns
C105/V108 DTE106					
data set up time		ts_{CDTEV}	100	-	ns
data hold time		th_{CDTEV}	0	-	ns
R104					
data valid after S114 LOW		tv_R	100	-	ns
I109/V107 DCE106					
data valid after S114 LOW		tv_{IVDCE}	100	-	ns

Extended data rate adaptor PCB2325

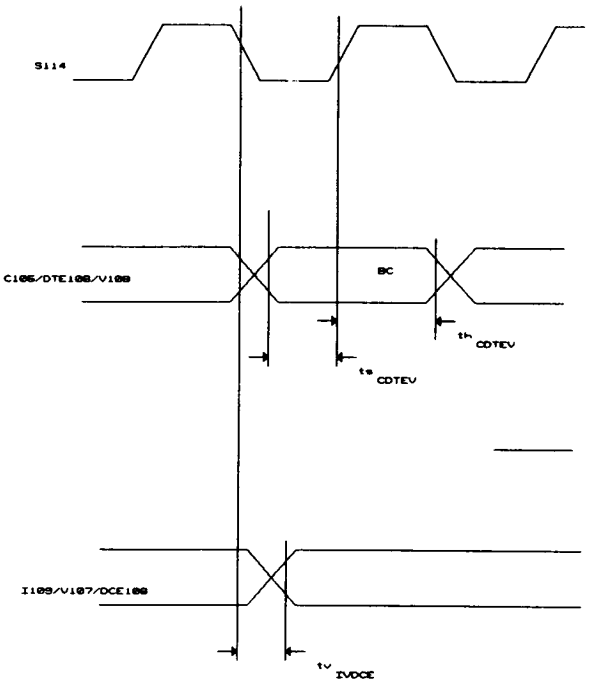


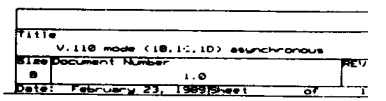
PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Interchange Interface V.110 mode with NIC					
T103 data valid after S113 LOW		tv_T	100	-	ns
C105/V108 DTE106 data set up time		ts_{CDTEV}	100	-	ns
R104 data valid after B115 LOW		tv_R	100	-	ns
I109/V107 DCE106 data valid after S114 LOW		tv_{IVDCE}	100	-	ns

Extended data rate adaptor PCB2325

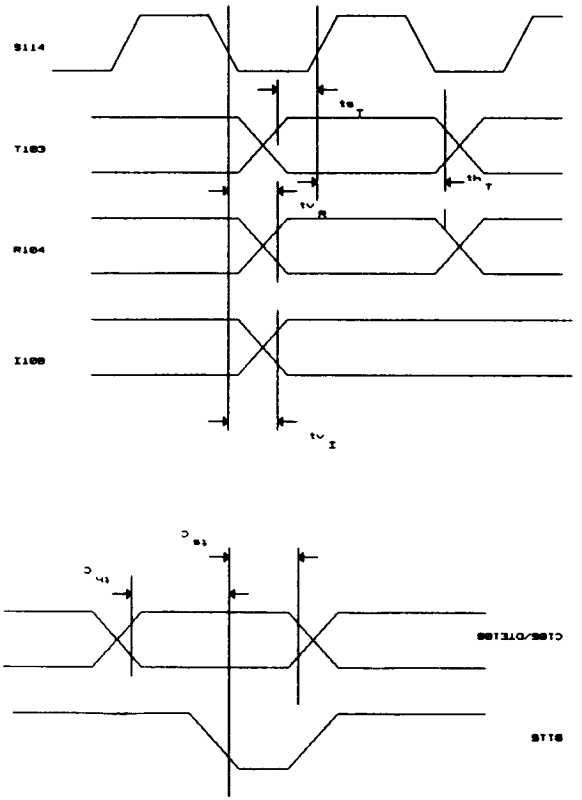


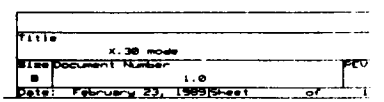
PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Interchange Interface					
V.110 mode asynchr.					
C105/V108 DTE106					
data set up time		ts_{CDTEV}	100	-	ns
data hold time		th_{CDTEV}	0	-	ns
I109/V107 DCE106					
data valid after S114 LOW		tv_{IVDCE}	100	-	ns



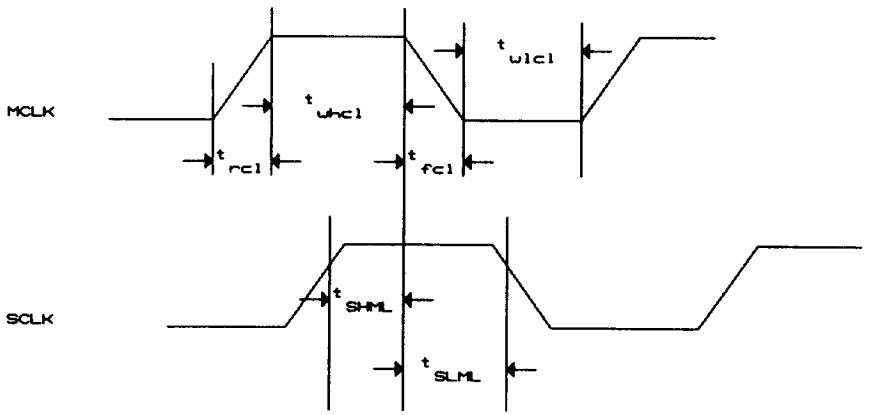


PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Interchange Interface					
X.30 mode					
T103					
data set up time		ts_T	100	-	ns
data hold time		th_T	0	-	ns
C105 DTE106					
data set up time		ts_C	100	-	ns
data hold time		th_C	0	-	ns
R104					
data valid after S114 LOW		tv_R	100	-	ns
I109					
data valid after S114 LOW		tv_I	100	-	ns





PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Clock circuit					
MCLK LOW time		t_{whcl}	190	290	ns
MCLK HIGH time		t_{wlcl}	190	290	ns
SCLK transition after MCLK LOW		t_{SLML}	20		ns
SCLK transition before MCLK LOW		t_{SHML}	20		ns



Title: MCLK and SCLK		
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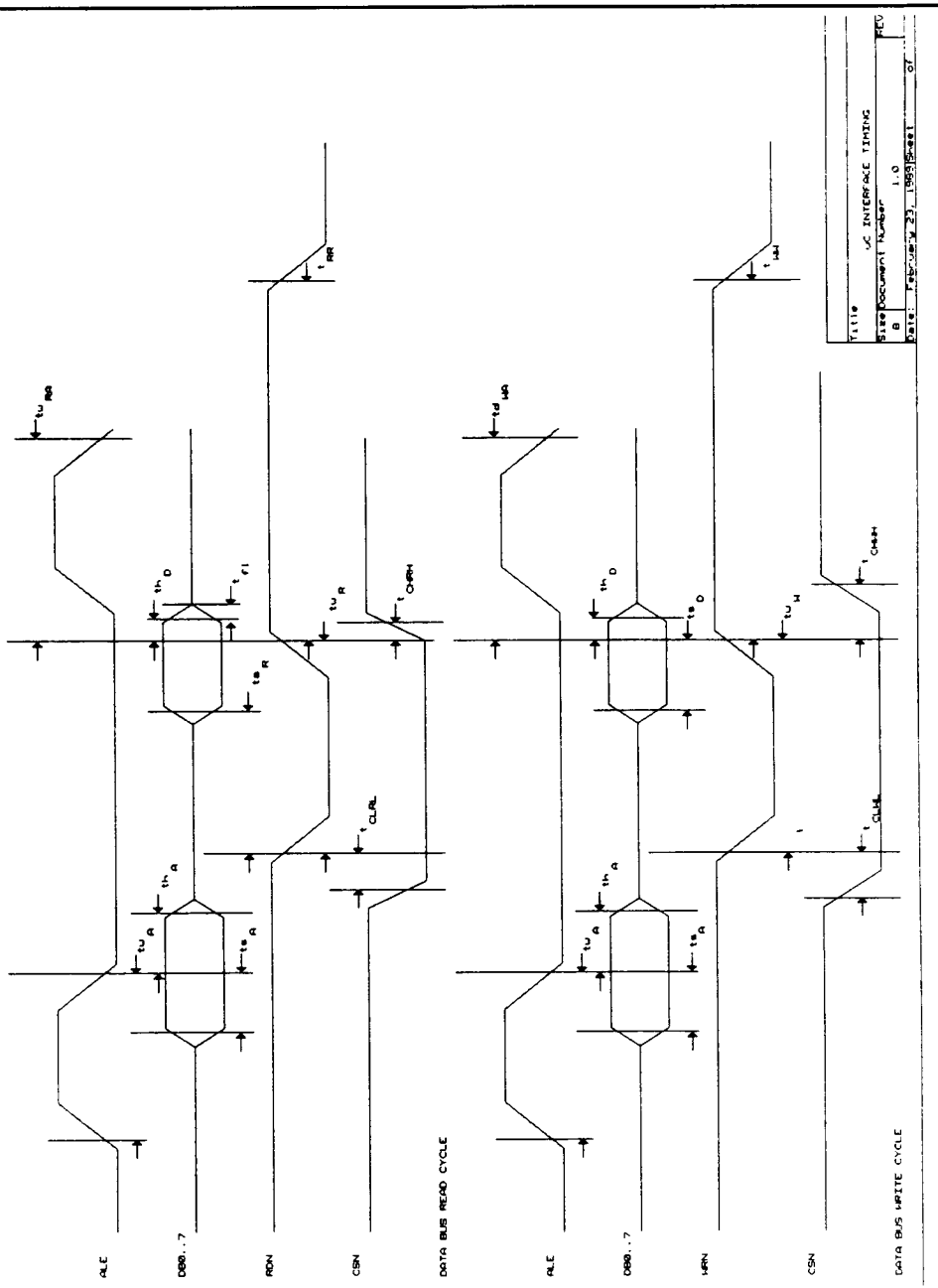
PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Microcontroller bus					
ALE pulse width		tw_A	100	-	ns
Data bus read cycle					
Address set up time		ts_A	55	-	ns
Address hold time		th_A	10	-	ns
RDN pulse width		tw_R	200	-	ns
Read access time	Cl = 200pF	ta_R	-	200	ns
Data hold time		th_D	10	-	ns
Time from RDN HIGH to ALE LOW		td_{RA}	1	-	µs
CSN LOW before RDN LOW		t_{CLRL}	50	-	ns
CSN HIGH before RDN HIGH		t_{CHRH}	0	-	ns
Bus floating after read		t_{fl}	-	75	ns
Time between two RDN (R 26 access)		t_{RR}	2	-	µs

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Microcontroller bus					
ALE pulse width		tw_A	100	-	ns
Data bus write cycle					
Address set up time		ts_A	55	-	ns
Address hold time		th_A	10	-	ns
WRN pulse width		tw_W	100	-	ns
Data set up time		ts_D	155	-	ns
Data hold time		th_D	0	-	ns
Time from WRCEN HIGH to ALE LOW		td_{WA}	10	-	ns
CSN LOW before WRN LOW		t_{CLWL}	50	-	ns
CSN HIGH after WRN HIGH		t_{CHWH}	0	-	ns
Time between two WRN (W 15 access)		t_{WW}	2	-	μs

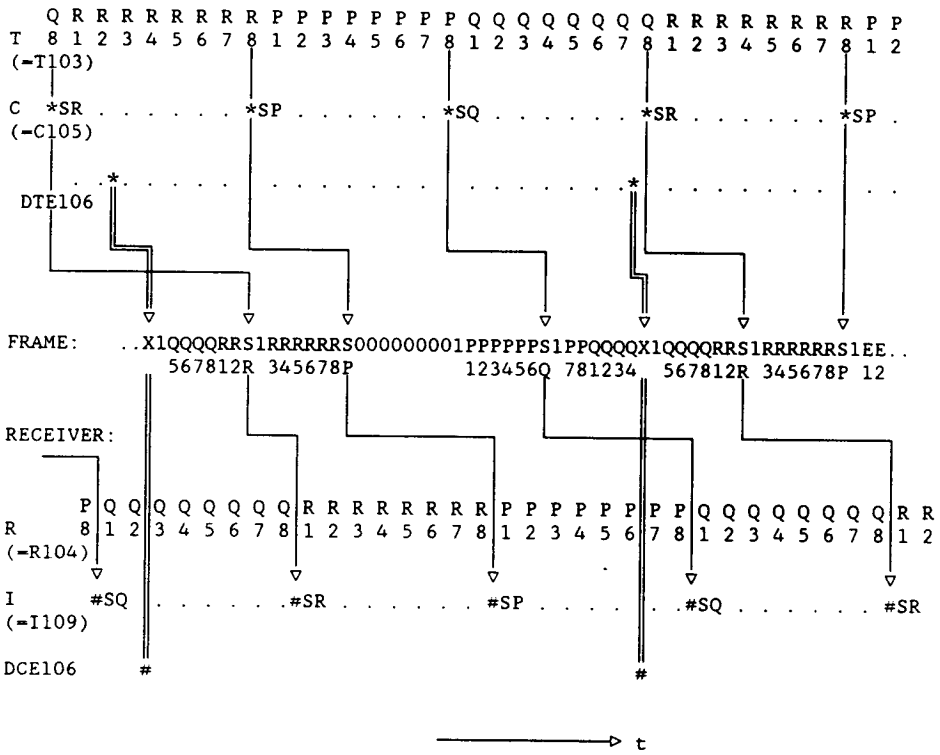
Extended data rate adaptor

PCB2325



Appendix A sample moments and state changes of the interchange circuits

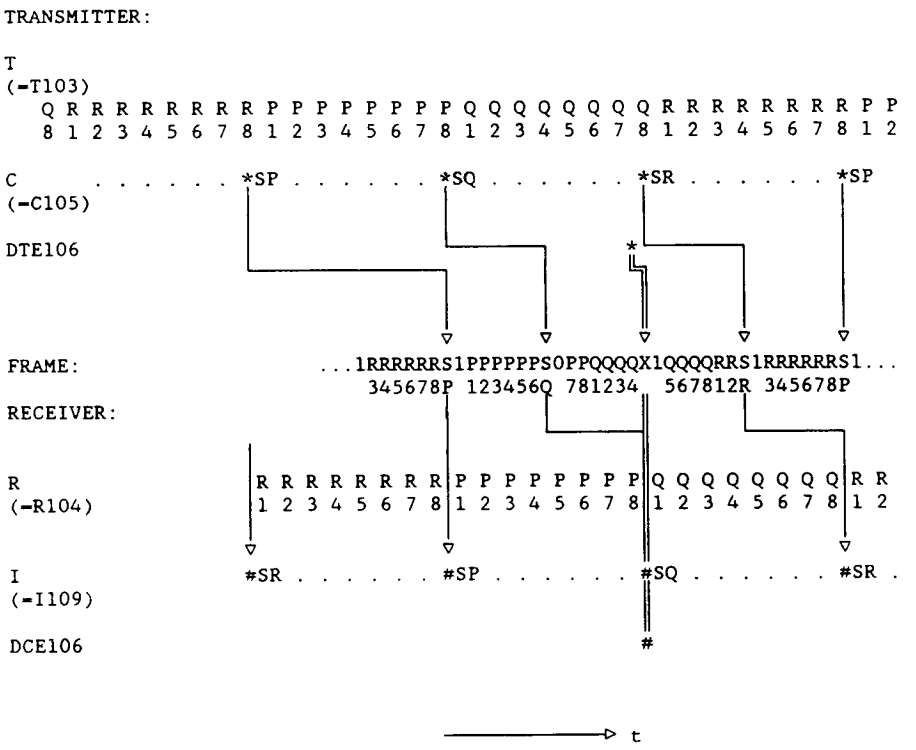
TRANSMITTER:



* sample moment of the interchange circuit
\# change point of the interchange circuit

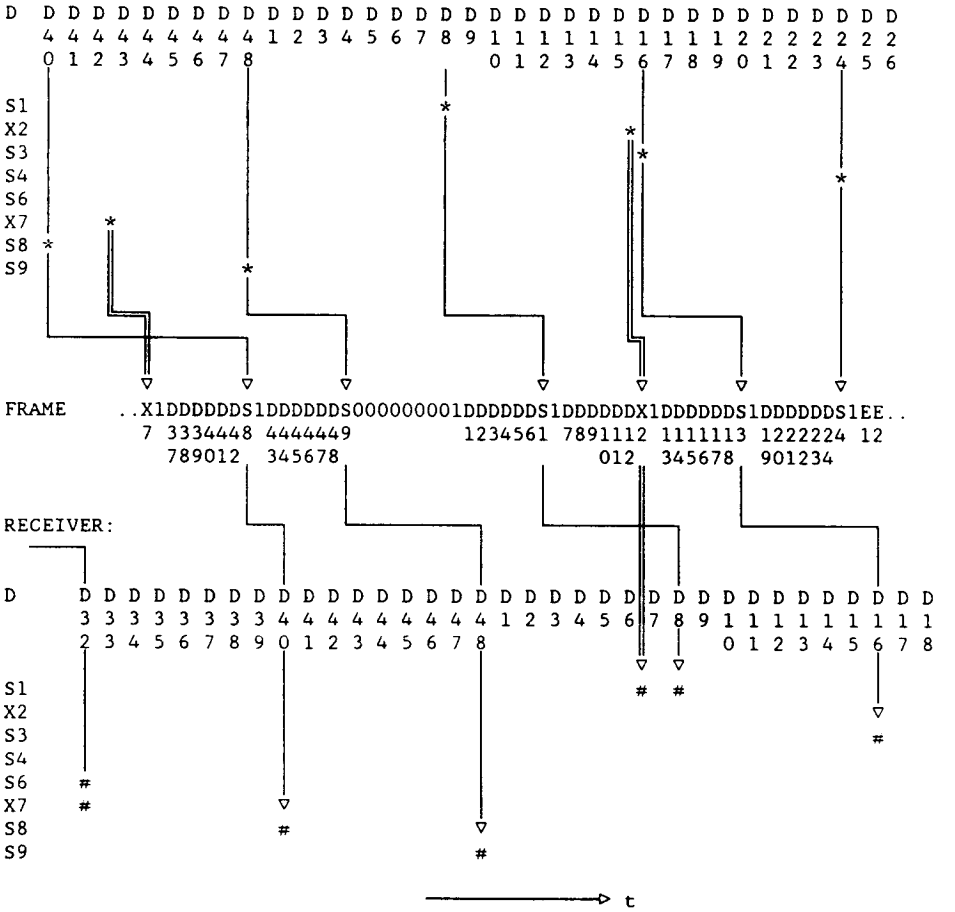
note1: When bit repetition is used (600 and 2400 bit/s) the value of last sample of the interchange circuits is repeated in the data bits, the S- and X-bits till a new sample is made (see appendix A, figure A-1.b and figure A-1.d).

Figure B-1 Sample moments and change points of the interchange circuit C, DTE106, DCE106 and I using a 10-bytes frame (rec. X.30)



* sample moment of the interchange circuit
\# change point of the interchange circuit

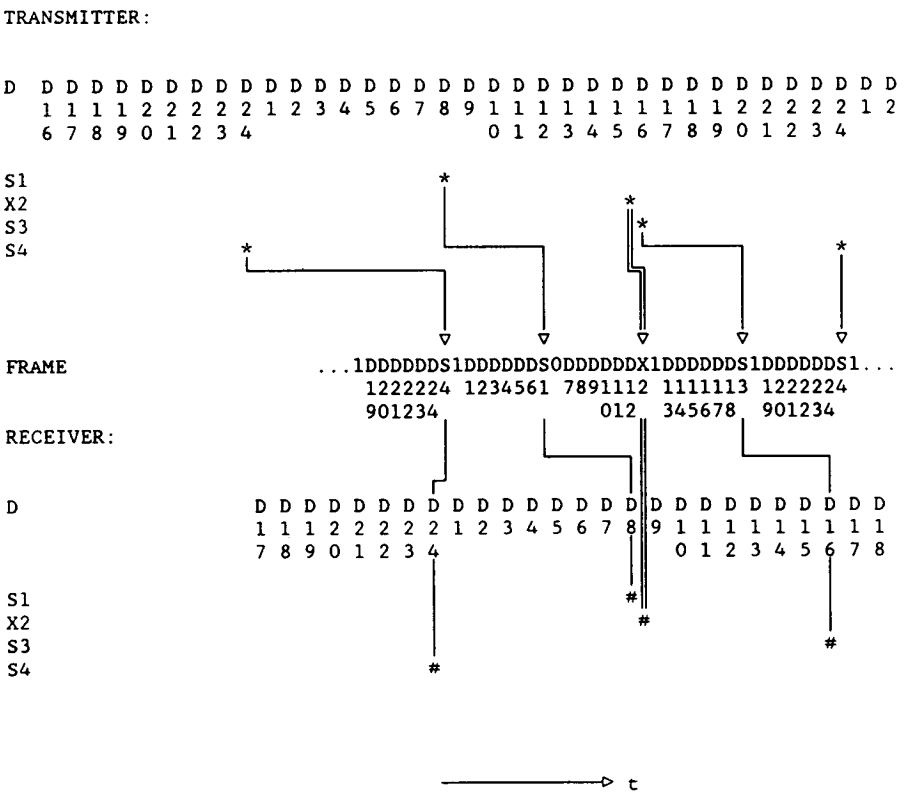
Figure B-2 Sample moments and change points of the interchange circuit C, DTE106, DCE106, IA and I using a 4-bytes frame (rec. X.30)



* sample moment of the interchange circuit
\# change point of the interchange circuit

notel: When bit repetition is used (600, 1200 and 2400 bit/s) the value of last sample of the interchange circuits is repeated in the data bits, the S- and X-bits till a new sample is made (see appendix A, figure A-1.b, A-1.c, A-1.d).

Figure B-3 Sample moments and change points of the interchange circuit 105, DTE106, 108 using a 10-bytes frame (rec. V.110)



* sample moment of the interchange circuit
\# change point of the interchange circuit

Figure B-4 Sample moments and change points of the interchange circuit 105, 108, DTE106 using a 4-bytes frame (rec. V.110)

Appendix B frame formats

OCTET	BIT NUMBER one	two	three	four	five	six	seven	eight
zero	0	0	0	0	0	0	0	0
one	1	D1 /P1	D2 /P2	D3 /P3	D4 /P4	D5 /P5	D6 /P6	S1/SQ
two	1	D7 /P7	D8 /P8	D9 /Q1	D10/Q2	D11/Q3	D12/Q4	X
three	1	D13/Q5	D14/Q6	D15/Q7	D16/Q8	D17/R1	D18/R2	S3/SR
four	1	D19/R3	D20/R4	D21/R5	D22/R6	D23/R7	D24/R8	S4/SP
five	1	E1	E2	E3	E4	E5	E6	E7
six	1	D25/P1	D26/P2	D27/P3	D28/P4	D29/P5	D30/P6	S6/SQ
seven	1	D31/P7	D32/P8	D33/Q1	D34/Q2	D35/Q3	D36/Q4	X
eight	1	D37/Q5	D38/Q6	D39/Q7	D40/Q8	D41/R1	D42/R2	S8/SR
nine	1	D43/R3	D44/R4	D45/R5	D46/R6	D47/R7	D48/R8	S9/SP

Figure B-1.a Frame format of the intermediate datastream for synchronous user data rates when no bit repetition is used (4800, 9600, 19200 bit/s) and frame format on the terminal highway for the synchronous user data rate of 38400 bit/s (V.110/X.30).

OCTET	BIT NUMBER one	two	three	four	five	six	seven	eight
zero	0	0	0	0	0	0	0	0
one	1	D1 /P1	D1 /P1	D2 /P2	D2 /P2	D3 /P3	D3 /P3	S1/SP
two	1	D4 /P4	D4 /P4	D5 /P5	D5 /P5	D6 /P6	D6 /P6	X
three	1	D7 /P7	D7 /P7	D8 /P8	D8 /P8	D9 /Q1	D9 /Q1	S3/SQ
four	1	D10/Q2	D10/Q2	D11/Q3	D11/Q3	D12/Q4	D12/Q4	S4/SQ
five	1	E1	E2	E3	E4	E5	E6	E7
six	1	D13/Q5	D13/Q5	D14/Q6	D14/Q6	D15/Q7	D15/Q7	S6/SR
seven	1	D16/Q8	D16/Q8	D17/R1	D17/R1	D18/R2	D18/R2	X
eight	1	D19/R3	D19/R3	D20/R4	D20/R4	D21/R5	D21/R5	S8/SR
nine	1	D22/R6	D22/R6	D23/R7	D23/R7	D24/R8	D24/R8	S9/SP

Figure B-1.b Frame format of the intermediate data stream (8 kbit/s) with a synchronous user data rate of 2400 bit/s (V.110/X.30)

OCTET	BIT NUMBER one	two	three	four	five	six	seven	eight
zero	0	0	0	0	0	0	0	0
one	1	D1	D1	D1	D1	D2	D2	S1
two	1	D2	D2	D3	D3	D3	D3	X
three	1	D4	D4	D4	D4	D5	D5	S3
four	1	D5	D5	D6	D6	D6	D6	S4
five	1	E1	E2	E3	E4	E5	E6	E7
six	1	D7	D7	D7	D7	D8	D8	S6
seven	1	D8	D8	D9	D9	D9	D9	X
eight	1	D10	D10	D10	D10	D11	D11	S8
nine	1	D11	D11	D12	D12	D12	D12	S9

Figure B-1.c Frame format of the intermediate data stream (8 kbit/s) for a synchronous user data rate of 1200 bit/s (V.110).

OCTET	BIT NUMBER one	two	three	four	five	six	seven	eight
zero	0	0	0	0	0	0	0	0
one	1	D1 /P1	D1 /P1	D1 /P1	D1 /P1	D1 /P1	D1 /P1	S1/SP
two	1	D1 /P1	D1 /P1	D2 /P2	D2 /P2	D2 /P2	D2 /P2	X
three	1	D2 /P2	D2 /P2	D2 /P2	D2 /P2	D3 /P3	D3 /P3	S3/SP
four	1	D3 /P3	D3 /P3	D3 /P3	D3 /P3	D3 /P3	D3 /P3	S4/SP
five	1	E1	E2	E3	E4	E5	E6	E7
six	1	D4 /P4	D4 /P4	D4 /P4	D4 /P4	D4 /P4	D4 /P4	S6/SP
seven	1	D4 /P4	D4 /P4	D5 /P5	D5 /P5	D5 /P5	D5 /P5	X
eight	1	D5 /P5	D5 /P5	D5 /P5	D5 /P5	D6 /P6	D6 /P6	S8/SP
nine	1	D6 /P6	D6 /P6	D6 /P6	D6 /P6	D6 /P6	D6 /P6	S9/SP
zero	0	0	0	0	0	0	0	0
one	1	D7 /P7	D7 /P7	D7 /P7	D7 /P7	D7 /P7	D7 /P7	S1/SP
two	1	D7 /P7	D7 /P7	D8 /P8	D8 /P8	D8 /P8	D8 /P8	X
three	1	D8 /P8	D8 /P8	D8 /P8	D8 /P8	D9 /Q1	D9 /Q1	S3/SP
four	1	D9 /Q1	D9 /Q1	D9 /Q1	D9 /Q1	D9 /Q1	D9 /Q1	S4/SP
five	1	E1	E2	E3	E4	E5	E6	E7
six	1	D10/Q2	D10/Q2	D10/Q2	D10/Q2	D10/Q2	D10/Q2	S6/SQ
seven	1	D10/Q2	D10/Q2	D11/Q3	D11/Q3	D11/Q3	D11/Q3	X
eight	1	D11/Q3	D11/Q3	D11/Q3	D11/Q3	D12/Q4	D12/Q4	S8/SQ
nine	1	D12/Q4	D12/Q4	D12/Q4	D12/Q4	D12/Q4	D12/Q4	S9/SP
zero	0	0	0	0	0	0	0	0
one	1	D13/Q5	D13/Q5	D13/Q5	D13/Q5	D13/Q5	D13/Q5	S1/SP
two	1	D13/Q5	D13/Q5	D14/Q6	D14/Q6	D14/Q6	D14/Q6	X
three	1	D14/Q6	D14/Q6	D14/Q6	D14/Q6	D15/Q7	D15/Q7	S3/SP
four	1	D15/Q7	D15/Q7	D15/Q7	D15/Q7	D15/Q7	D15/Q7	S4/SP
five	1	E1	E2	E3	E4	E5	E6	E7
six	1	D16/Q8	D16/Q8	D16/Q8	D16/Q8	D16/Q8	D16/Q8	S6/SP
seven	1	D16/Q8	D16/Q8	D17/R1	D17/R1	D17/R1	D17/R1	X
eight	1	D17/R1	D17/R1	D17/R1	D17/R1	D18/R2	D18/R2	S8/SP
nine	1	D18/R2	D18/R2	D18/R2	D18/R2	D18/R2	D18/R2	S9/SP
zero	0	0	0	0	0	0	0	0
one	1	D19/R3	D19/R3	D19/R3	D19/R3	D19/R3	D19/R3	S1/SP
two	1	D19/R3	D19/R3	D20/R4	D20/R4	D20/R4	D20/R4	X
three	1	D20/R4	D20/R4	D20/R4	D20/R4	D21/R5	D21/R5	S3/SP
four	1	D21/R5	D21/R5	D21/R5	D21/R5	D21/R5	D21/R5	S4/SP
five	1	E1	E2	E3	E4	E5	E6	E7
six	1	D22/R6	D22/R6	D22/R6	D22/R6	D22/R6	D22/R6	S6/SP
seven	1	D22/R6	D22/R6	D23/R7	D23/R7	D23/R7	D23/R7	X
eight	1	D23/R7	D23/R7	D23/R7	D23/R7	D24/R8	D24/R8	S8/SP
nine	1	D24/R8	D24/R8	D24/R8	D24/R8	D24/R8	D24/R8	S9/SP

Figure B-1.d Frame format of the intermediate datastream (8 kbit/s) for the user data rate speeds of 600 bit/s (V.110/X.30)

OCTET	BIT NUMBER one	two	three	four	five	six	seven	eight
one	1	D1 /P1	D2 /P2	D3 /P3	D4 /P4	D5 /P5	D6 /P6	S1/SQ
two	0	D7 /P7	D8 /P8	D9 /Q1	D10/Q2	D11/Q3	D12/Q4	X
three	1	D13/Q5	D14/Q6	D15/Q7	D16/Q8	D17/R1	D18/R2	S3/SR
four	1	D19/R3	D20/R4	D21/R5	D22/R6	D23/R7	D24/R8	S4/SP

Figure B-2 Frame format on the terminal highway for synchronous user data of 48 kbit/s and asynchronous user data upto 19.2 kbit/s (V-series only).

OCTET	BIT NUMBER one	two	three	four	five	six	seven	eight
one	D1	D2	D3	D4	D5	D6	D7	S
two	D8	D9	D10	D11	D12	D13	D14	S
three	D15	D16	D17	D18	D19	D20	D21	S
four	D22	D23	D24	D25	D26	D27	D28	S

Figure B-3 Frame format on the terminal highway for synchronous speed 56 kbit/s. When S is set '1', the framing fits to rec. V.110.

OCTET	BIT NUMBER one	two	three	four	five	six	seven	eight
one	D1	D2	D3	D4	D5	D6	D7	D8
two	D9	D10	D11	D12	D13	D14	D15	D16
three	D17	D18	D19	D20	D21	D22	D23	D24
four	D25	D26	D27	D28	D29	D30	D31	D32

Figure B-4 Frame format on the terminal highway for synchronous speed of 64 kbit/s.

Appendix C multiple sampling method

asynchronous signal

A | B | A | B | A | B | A | B | A | B | A | B | A | B | A | B | A |

96 KHz

48 KHz

T C P T C T C P

bit identity

1 0 1 0 0 1 0 1

bit sequence (48 kbit/s)

code character for a transition (C)				position of the transition in a group of two sampling pulses
from 1⟶ 0		from 0⟶ 1		
T	C	T	C	
0	0	1	1	in first half (A)
0	1	1	0	in second half (B)

Figure C-5 Additional transition coding (based on R.111).

Additional transition coding is based on R.111. In R.111 however two transition code characters (C1 and C2) are used for each signal transition instead of one (C).

Appendix D connection of the interchange circuits at 1200/75 bit/s

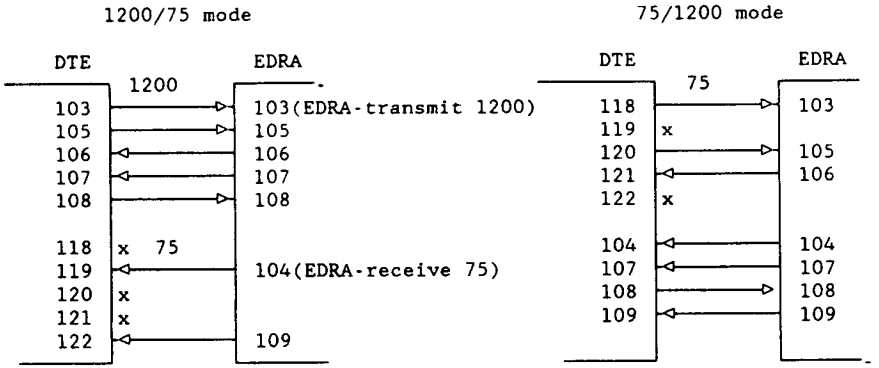


Figure D-1 Split speed (1200/75).

For the signal names of figure D-1 is referred to CCITT rec. V23.