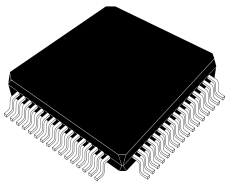
TDA7580

FM/AM DIGITAL IF SAMPLING PROCESSOR

PRODUCT PREVIEW

- FM/AM IF SAMPLING DSP
- ON-CHIP ANALOGUE TO DIGITAL CONVERTER FOR 10.7MHz IF SIGNAL CONVERSION
- SOFTWARE BASED CHANNEL EQUALIZATION
- FM ADJACENT CHANNEL SUPPRESSION
- RECEPTION ENHANCEMENT IN MULTIPATH CONDITION
- STEREO DECODER AND WEAK SIGNAL PROCESSING
- 2 CHANNELS SERIAL AUDIO INTERFACE (SAI) WITH SAMPLE RATE CONVERTER
- I^2C AND BUFFER-SPI CONTROL INTERFACES
- RDS FILTER, DEMODULATOR & DECODER
- INTER PROCESSOR TRANSPORT INTERFACE FOR ANTENNA AND TUNER DIVERSITY
- FRONT-END AGC FEEDBACK

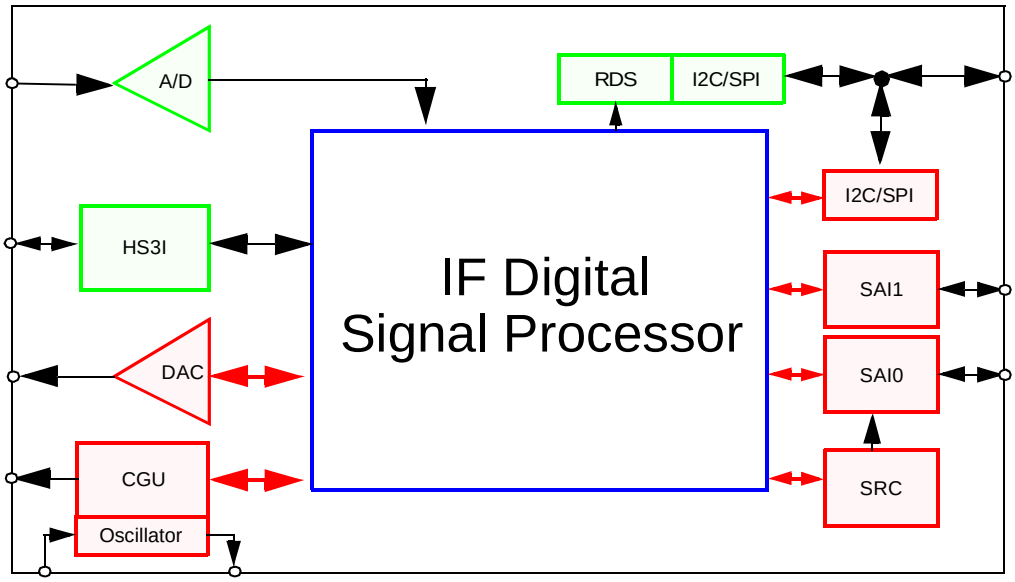


TQFP64
ORDERING NUMBER: TDA7580

DESCRIPTION

The TDA7580 is an integrated circuit implementing an advanced mixed analogue and digital solution to perform the signal processing of a AM/FM channel. The HW&SW architecture has been devised so to have a digital equalization of the FM/AM channel; hence a real rejection of adjacent channels and any other signals interfering with the listening of the desired station. In severe Multiple Paths conditions, the reception is improved to get the audio with high quality.

BLOCK DIAGRAM



DESCRIPTION (continued)

The algorithm is self-adaptive, thus it requires no “on-the-field” adjustments after the parameters optimization.

The chip embeds a *Band Pass Sigma Delta Analogue to Digital Converter* for 10.7MHz IF conversion from a “tuner device” (it is highly recommended the TDA7515).

The internal 24bit-DSP allows some flexibility in the algorithm implementation, thus giving some freedom for customer required features. The total processing power offers a significant headroom for customer’s software requirement, even when the channel equalization and the decoding software is running. The Program and Data Memory space can be loaded from an external non volatile memory via I^2C or SPI.

The oscillator module works with an external 74.1MHz quartz crystal. It has very low Electro Magnetic Interference, as it introduces very low distortion, and in any case any harmonics fall outside the Radio bandwidth.

The companion tuner device receives the reference clock through a differential ended interface, which works off the Oscillator module by properly dividing down the master clock frequency. That allows the overall system saving an additional crystal for the tuner.

After the IF conversion, the digitized baseband signal passes through the Base Band processing section, either FM or AM, depending on the listener selection. The FM Base Band processing comprises of Stereo Decoder, Spike Detection and Noise Blanking. The AM Noise Blanking is fully software implemented.

The internal RDS filter, demodulator and decoder features complete functions to have the output data available through either I^2C or SPI interface. No DSP support is needed but at start-up, so that RDS can work in background and in parallel with other DSP processing. This mode (RDS-only) allows current consumption saving for low power application modes.

An I^2C/SPI interface is available for any control and communication with the main micro, as well as RDS data interface. The DSP SPI block embeds a 10 words FIFO for both transmit and receive channels, to lighten the DSP task and frequently respond to the interrupt from the control interface.

Serial Audio Interface (SAI) is the ideal solution for the audio data transfer, both transmit and receive: either master or slave. The flexibility of this module gives a wide choice of different protocols, including I^2S. Two fully independent bidirectional data channels, with separate clocks allows the use of TDA7580 as general purpose digital audio processor.

A fully Asynchronous Sample Rate Converter (ASRC) is available as a peripheral prior to sending audio data out via the SAI, so that internal audio sampling rate (~36kHz and FM/AM mode) can be adapted by upconversion to any external rate.

An Inter Processor Transport Interface (HS^3I, High Speed Synchronous Serial Interface) is also available for a modular system which implements *Dual Tuner Diversity*, thus enhancing the overall system performance. It is about a Synchronous Serial Interface which exchanges data up to the MPX rate. It has been designed to reduce the Electro Magnetic Interference toward the sensitive analogue signal from the Tuner.

General Purpose I/O registers are connected to and controlled by the DSP, by means of memory map.

A Debug and Test Interface is available for on-chip software debug as well as for internal registers read/write operation.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
VDD VDD3	Power supplies (1)	Nom. 1.8V Nom. 3.3V	-0.5 to 2.5 -0.5 to 4.0	V V
	Analog Input or Output Voltage belonging to 3.3V IO ring (V_{DDSD}, V_{DDOSC})		-0.5 to 4.0	V
	Digital Input or Output Voltage, 5V tolerant	Normal(2) Fail-safe(3)	-0.5 to 6.50 -0.5 to 3.80	V V
	All remaining Digital Input or Output Voltage	Nom. 1.8V Nom. 3.3V	-0.5 to (VDD+0.5) -0.5 to (VDD3+0.5)	V
T_j	Operating Junction Temperature Range		-40 to 125	°C
T_{stg}	Storage Temperature		-55 to 150	°C

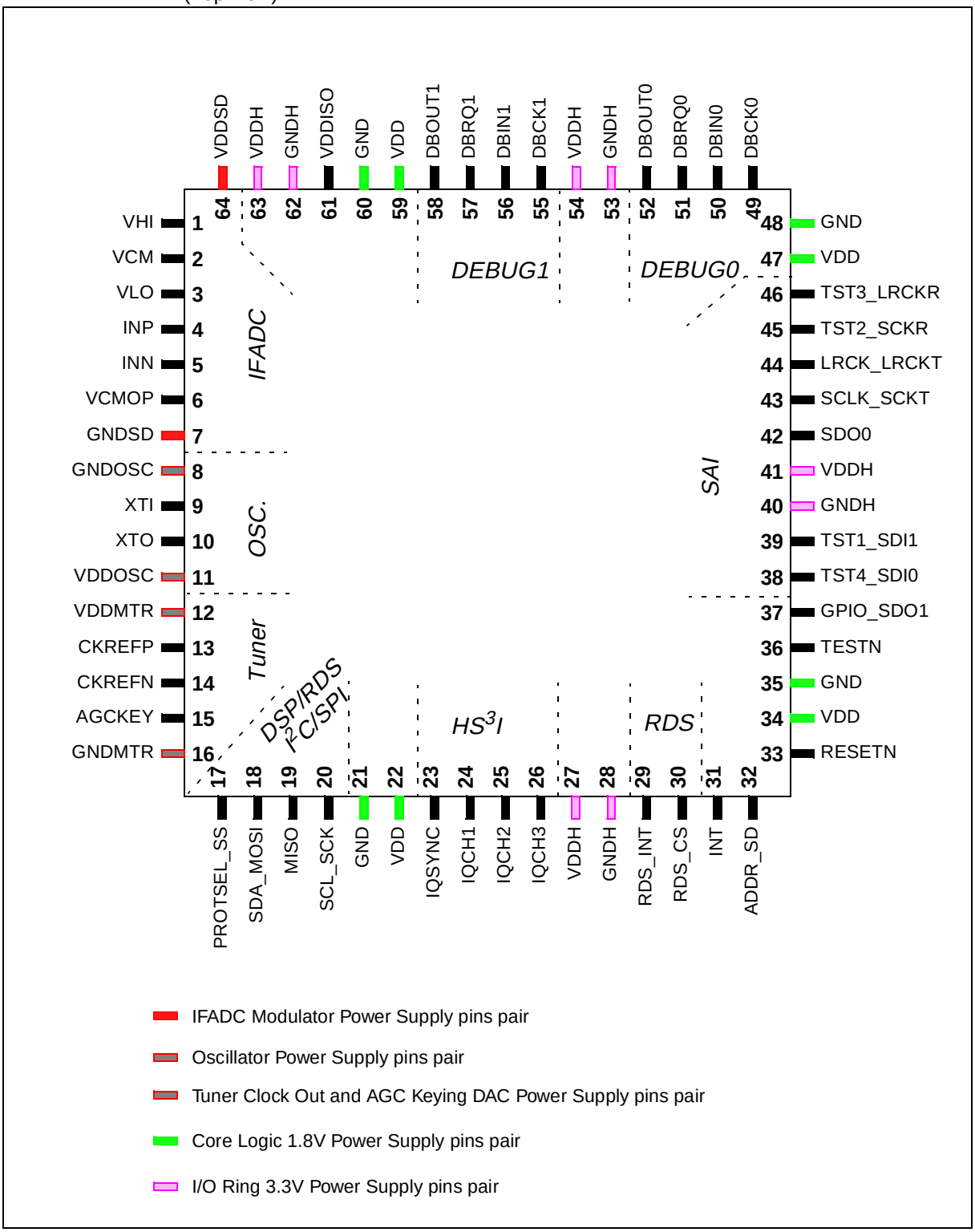
Warning: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Note: 1. V_{DD3} refers to all of the nominal 3.3V power supplies (V_{DDH}, V_{OSC}, V_{DDSD}). V_{DD} refers to all of the nominal 1.8V power supplies (V_{DD}, V_{MTR}).
2. During Normal Mode operation VDD3 is always available as specified
3. During Fail-safe Mode operation VDD3 may be not available.

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal resistance junction to ambient	68	°C/W

PIN CONNECTION (Top view)



PIN DESCRIPTION

N°	Name	Type	Description	Notes	After Reset
1	VHI	A	Internally generated IFADC Opamps 2.65V (@VDD=3.3V) Reference Voltage Pin for external filtering	It needs external 22µF and 220nF ceramic capacitors	
2	VCM	A	Internally generated Common Mode 1.65V (@VDD=3.3V) Reference Voltage Pin for external filtering	It needs external 22µF and 220nF ceramic capacitors	
3	VLO	A	Internally generated IFADC Opamps 0.65V (@VDD=3.3V) Reference Voltage Pin for external filtering	It needs external 22µF and 220nF ceramic capacitors	
4	INP	A	Positive IF signal input from Tuner	2.0Vpp @VDD=3.3V	
5	INN	A	Negative IF signal input from Tuner	2.0Vpp @VDD=3.3V	
6	VCMOP	A	Internally generated Modulator Opamps Common Mode 2.65V (@VDD=3.3V) Reference Voltage Pin for external filtering	It needs external 22µF and 220nF ceramic capacitors	
7	GNDSD	G	IFADC Modulator Analogue Ground	Clean Ground, to be star-connected to voltage regulator ground	
8	GNDOSC	G	Oscillator Ground	Clean Ground, to be star-connected to voltage regulator ground	
9	XTI	I	High impedance oscillator input (quartz connection) or clock input when in Antenna Diversity slave mode	Maximum voltage swing is VDD	
10	XTO	O	Low impedance oscillator output (quartz connection)		
11	VDDOSC	P	Oscillator Power Supply	3.3V	
12	VDDMTR	P	Tuner reference clock and AGCKeying DAC Power Supply	1.8V	
13	CKREFP	B	Tuner reference clock positive output.	FM 100kHz AM_{EU} 18kHz With internal pull_up, on at reset	Output
14	CKREFN	B	Tuner reference clock negative output.	FM 100kHz AM_{EU} 18kHz With internal pull_up, on at reset	Output
15	AGCKEY	A	DAC output for Tuner AGCKeying	1.5kohm ±30% output impedance. 1Vpp ±1% output dynamic range	
16	GNDMTR	G	Tuner reference clock and AGC keying DAC Ground		

PIN DESCRIPTION (continued)

N°	Name	Type	Description	Notes	After Reset
17	PROTSEL_SS	B	DSP0 GPIO for Control Serial Interface (Low: SPI or High: I^2C) selection at device Bootstrap. In SPI protocol mode, after Boot procedure, SPI Slave Select, otherwise DSP0 GPIO0	DSP0 GPIO0 5V tolerant With internal pull_up, on at reset	Input
18	SDA_MOSI	B	Control Serial Interface and RDS IO: - SPI mode: slave data in or master data out for main SPI and RDS SPI data in - I^2C mode: data for main I^2C or RDS I^2C	5V tolerant With internal pull_up, on at reset	Input
19	MISO	B	SPI slave data out or master data in for main SPI and RDS SPI data out	DSP0 GPIO1 5V tolerant With internal pull_up, on at reset	Input
20	SCL_SCK	B	Bit clock for Control Serial Interface and RDS	5V tolerant With internal pull_up, on at reset	Input
21	GND	G	Digital Core Power Ground		
22	VDD	P	Digital Core Power Supply	1.8V	
23	IQSYNC	B	High Speed Synchronous Serial Interface (HS^3I) clock if HS^3I master mode, else DSP1 GPIO or DSP1 Debug Port Clock (DBOUT1)	DSP1 GPIO0 5V tolerant With internal pull_up, on at reset	Input
24	IQCH1	B	High Speed Synchronous Serial Interface (HS^3I) Channel 1 Data if HS^3I master mode, else DSP1 GPIO or DSP1 Debug Port Request (DBRQ1)	DSP1 GPIO1 5V tolerant With internal pull_up, on at reset	Input
25	IQCH2	B	High Speed Synchronous Serial Interface (HS^3I) Channel 2 Data if HS^3I master mode, else DSP1 GPIO or DSP1 Debug Port Data In (DBIN1)	DSP1 GPIO2 5V tolerant With internal pull_down, on at reset	Input
26	IQCH3	B	High Speed Synchronous Serial Interface (HS^3I) Channel 3 Data if HS^3I master mode, else DSP1 GPIO or DSP1 Debug Port Data Out (DBCK1)	DSP1 GPIO3 5V tolerant With internal pull_down, on at reset	Input
27	VDDH	P	3.3V IO Ring Power Supply (HS^3I, I^2C/ SPI, RDS, INT)		
28	GNDH	G	3.3V IO Ring Power Ground (HS^3I, I^2C/ SPI, RDS, INT)		
29	RDS_INT	B	RDS interrupt to external main microprocessor in case of traffic information	DSP1 GPIO4 5V tolerant With internal pull_up, on at reset	Input

PIN DESCRIPTION (continued)

N°	Name	Type	Description	Notes	After Reset
30	RDS_CS	B	RDS chip select. When RESETN rising, If RDS_CS 0, the RDS's SPI is selected; else RDS's I^2C	DSP1 GPIO5 5V tolerant With internal pull_up, on at reset	Input
31	INT	I	DSP0 External Interrupt	5V tolerantWith internal pull_up, on at reset	
32	ADDR_SD	B	IFS chip master (Low) or slave (High) mode selection, latched in upon RESETN release. It selects the LSB of the I^2C addresses. Station Detector output	DSP0 GPIO2 5V tolerantWith internal pull_down, on at reset	Input
33	RESETN	I	Chip Hardware reset, active Low	5V tolerant With internal pull_up	
34	VDD	P	Digital Power Supply	1.8V	
35	GND	G	Digital Power Ground		
36	TESTN	I	Test Enable pin, active Low	With internal pull_up	
37	GPIO_SDO1	B	DSP0 GPIO for Boot selection or Audio SAI0 output.	5V tolerant DSP0 GPIO3 With internal pull_up, on at reset	Input
38	TST4_SDI0	B	Audio SAI0 Data input or test selection pin in Test Mode	5V tolerant DSP0 GPIO5With internal pull_up, on at reset	Input
39	TST1_SDI1	B	DSP0 GPIO for Boot selection or Audio SAI1 input. Test selection pin in Test Mode.	5V tolerant DSP0 GPIO4With internal pull_up, on at reset	Input
40	GNDH	G	3.3V IO Ring Power Ground (Audio SAI, ResetN, Test Pins)		
41	VDDH	P	3.3V IO Ring Power Supply (Audio SAI, ResetN, Test Pins)		
42	SDO0	B	Radio or Audio SAI0 data output	5V tolerant With internal pull_up, on at reset	Output
43	SCLK_SCKT	B	SAI0 Receive and Transmit bit clock (master or slave with ASRC); SAI1 Transmit bit clock	5V tolerant With internal pull_up, on at reset	Input
44	LRCK_LRCKT	B	SAI0 Receive and Transmit LeftRight clock (master or slave with ASRC); SAI1 Transmit LeftRight clock	5V tolerant With internal pull_up, on at reset	Input

PIN DESCRIPTION (continued)

N°	Name	Type	Description	Notes	After Reset
45	TST2_SCKR	B	SAI0 Transmit bit clock; SAI1 Receive and Transmit bit clock. Or Test selection pin in Test Mode	5V tolerant DSP0 GPIO6 With internal pull_up, on at reset	Input
46	TST3_LRCKR	B	SAI0 Transmit LeftRight clock; SAI1 Receive and Transmit bit clock. Or Test selection pin in Test Mode	DSP0 GPIO7 5V tolerant With internal pull_up, on at reset	Input
47	VDD	P	Digital Core Power Supply	1.8V	
48	GND	G	Digital Core Power Ground		
49	DBCK0	B	Debug Port Clock of DSP0 (DBCK0)	DSP0 GPIO9 5V tolerant With internal pull_down, on at reset	Input
50	DBIN0	B	Debug Port Data Input of DSP0 (DBIN0)	DSP0 GPIO11 5V tolerant With internal pull_down, on at reset	Input
51	DBRQ0	B	Debug Port Request of DSP0 (DBRQ0)	DSP0 GPIO 5V tolerant With internal pull_up, on at reset	Input
52	DBOUT0	B	Debug Port Data Output of DSP0 (DBOUT0)	DSP0 GPIO10 5V tolerant With internal pull_up, on at reset	Input
53	GNDH	G	3.3V IO Ring Power Ground (Debug Interface, GPIO)		
54	VDDH	P	3.3V IO Ring Power Supply (Debug Interface, GPIO)		
55	DBCK1	B	DSP1 Debug Port Clock (DBCK1) if HS^3I master mode, else High Speed Synchronous Serial Interface (HS^3I) Channel3 Data	DSP1 GPIO9 5V tolerant With internal pull_down, on at reset	Input
56	DBIN1	B	DSP1 GPIO or DSP1 Debug Port Data In (DBIN1) if HS^3I master mode, else High Speed Synchronous Serial Interface (HS^3I) Channel2 Data i	DSP1 GPIO11 5V tolerant With internal pull_down, on at reset	Input
57	DBRQ1	B	DSP1 GPIO or DSP1 Debug Port Request (DBRQ1) if HS^3I master mode, else High Speed Synchronous Serial Interface (HS^3I) Channel1 Data	5V tolerant With internal pull_up, on at reset	Input

PIN DESCRIPTION (continued)

N°	Name	Type	Description	Notes	After Reset
58	DBOUT1	B	DSP1 GPIO or DSP1 Debug Port Data Out (DBOUT1) if HS^{3}I master mode, else High Speed Synchronous Serial Interface (HS^{3}I) clock	DSP1 GPIO10 5V tolerant With internal pull_up, on at reset	Input
59	VDD	P	Digital Core Power Supply	1.8V	
60	GND	G	Digital Core Power Ground		
61	VDDISO	P	3.3V N-isolation biasing supply	Clean 3.3V supply to be star-connected to voltage regulator	
62	GNDH	G	3.3V IO Ring Power Ground (Modulator digital section)		
63	VDDH	P	3.3V IO Ring Power Supply (Modulator digital section)		
64	VDDSD	P	3.3V IFADC Modulator Analogue Power Supply	Clean Power Supply, to be star-connected to 3.3V voltage regulator	

I/O TYPE

P: Power Supply from Voltage regulator
G: Power Ground from Voltage regulator
A: Analogue I/O
I: Digital Input
O: Digital Output
B: Bidirectional I/O

I/O DEFINITION AND STATUS

Z: high impedance (input)
O: logic low output
X: undefined output
1: logic high output
Output **PP**: Push-Pull/ **OD**: Open-Drain

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Comment	Min.	Typ.	Max.	Unit
V_{DD}	1.8V Power Supply Voltage	Core Power Supply	1.7	1.80	1.9	V
V_{DDH}	3.3V Power Supply Voltage (1)	IO Rings Power Supply (with G_{NDH})	3.15	3.30	3.45	V
V_{OSC}	3.3V Power Supply Voltage (1)	Oscillator Power Supply (GND_{OSC})	3.15	3.30	3.45	V
V_{DDSD}	3.3V Power Supply Voltage (1)	IF ADC Power Supply (with G_{NDSD})	3.15	3.30	3.45	V
V_{MTR}	1.8V Power Supply Voltage	DAC-Keying and Tuner clock Power Supply (with GND_{MTR})	1.7	1.80	1.9	V

Note: 1. V_{DDH}, V_{OSC}, V_{DDSD} are also indicated in this document as V_{DD3}. All others as V_{DD}.

GENERAL INTERFACE ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{ilh}	Low Level Input Current I/Os@V_{DD3} (absolute value)	V_i = 0V (notes 1, 2) without pull-up-down device			1	µA
I_{ihh}	High Level Input Current I/Os@V_{DD3} (absolute value)	$V_i = V_{DD3}$ (notes 1, 2) without pull-up-down device			1	µA
I_{il}	Low Level Input Current I/Os@V_{DD} (absolute value)	V_i = 0V (notes 1, 3, 4) without pull-up-down device			1	µA
I_{ih}	High Level Input Current I/Os@V_{DD} (absolute value)	$V_i = V_{DD}$ (notes 1, 3, 4) without pull-up device			1	µA
I_{ipdh}	Pull-down current I/Os @ V_{DD3}	$V_i = V_{DD3}$ (note 5) with pull-down device	3.2	6.6	10.0	µA
I_{opuh}	Pull-up current I/Os @ V_{DD3}	V_i = 0V(note 6) with pull-up device	-10.0	-6.6	-3.2	µA
I_{opul}	Pull-up current I/Os @ V_{DD}	V_i = 0V (note 3) with pull-up device	-5.4	-3.6	-1.8	µA
I_{aihop}	Analogue pin sunk/drawn current on pin1 and pin 6	$V_i = V_{DD3}$	0.95	1.25	1.55	mA
		V_i = 0V	-6.25	-5.0	-3.75	mA
I_{acm}	Analogue pin sunk/drawn current on pin 2	$V_i = V_{DD3}$	1.5	2.0	2.5	mA
		V_i = 0V	-2.5	-2.0	-1.5	mA
I_{ail}	Analogue pin sunk/drawn current on pin 3	$V_i = V_{DD3}$	3.75	5.0	6.25	mA
		V_i = 0V	-1.55	-1.25	-0.95	mA
I_{ain}	Analogue pin sunk/drawn current on pin 4 and pin 5	$V_i = V_{DD3}$	24	32	40	µA
		V_i = 0V	-40	-32	-24	µA
I_{aik}	Analogue pin sunk/drawn current on pin 15	$V_i = V_{DD}$	0.8	1.2	1.6	mA
		V_i = 0V (spec absolute value)			1	µA
I_{oz}	Tri-state Output leakage	V_o = 0V or V_{DD3} (note 1) without pull up/down device			1	µA

GENERAL INTERFACE ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{ozFT}	5V Tolerant Tri-state Output leakage (without pull up/down device)	V_o = 0V or V_{dd} (note 1)			1	µA
		V_o = 5.5V		1	3	µA
$I_{latchup}$	I/O latch-up current	V < 0V, V > V_{dd}	200			mA
V_{esd}	Electrostatic Protection	Leakage, 1µA	2000			V

Note: 1. The leakage currents are generally very small, <1nA. The value given here, 1µA, is the maximum that can occur after an Electrostatic Stress on the pin.
2. On pins:17 to 20,23 to 26,29 to 33,36 to 39,42 to 46,49 to 52,55 to 58.
3. On pins: 13 and 14.
4. Same check on the analogue pin 15 (phisically without pull-up-down)
5. On pins:25, 26,32,49,50,55,56
6. On pins:17 to 20,23 to 24,29 to 31,33,36 to 39,42 to 46,51, 52,57, 58

LOW VOLTAGE CMOS INTERFACE DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{il}	Low Level Input Voltage	1.70V<=VDD<=1.90V			0.3*V_{DD3}	V
V_{ih}	High Level Input Voltage	1.70V<=VDD<=1.90V	0.8*V_{DD3}			V
V_{ol}	Low level output Voltage	I_{ol} = 4mA (notes 1)			0.15	V
V_{oh}	High level output Voltage	I_{ol} = -4mA (notes 1)	V_{DD}-0,15			V

Note: 1. It is the source/sink current under worst case conditions and reflects the name of the I/O cell according to the drive capability.

HIGH VOLTAGE CMOS INTERFACE DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{il}	Low Level Input Voltage	3.15V<=VDD3<=3.45V			0.8	V
V_{ih}	High Level Input Voltage	3.15V<=VDD3<=3.45V	2.0			V
V_{ol}	Low level output Voltage	I_{ol} = XmA (notes 1 and 2)			0.15	V
V_{oh}	High level output Voltage	I_{ol} = -XmA (notes 1 and 2)	V_{DD3}-0.15			V

Note: 1. It is the source/sink current under worst case conditions and reflects the name of the I/O cell according to the drive capability
2. X=4mA for pins 17 to 20,29,30,32,36 to 39,42 to 46; X=8mA for pins 23 to 26,49 to 52,55 to 58.

CURRENT CONSUMPTION

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{DD}	Current through V_{DD} Power Supply	V_{DD}=1.8V,VDD3=3.3V All digital blocks working		120	200	mA
I_{DDH}	Current through V_{DDH} Power Supply	V_{DD}=1.8V,VDD3=3.3V All I/Os working with 5pF load		3	5	mA
I_{SD}	Current through V_{SD} Power Supply	V_{DD}=1.8V,VDD3=3.3V	36	45	54	mA
I_{OSCdc}	Current through V_{OSC} Power Supply	V_{DD}=1.8V,VDD3=3.3V without quartz	5.5	8	10.5	mA

CURRENT CONSUMPTION (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{OSCac}	Current through V_{OSC} Power Supply	V_{DD}=1.8V,VDD3=3.3V with quartz in FM mode	11	14	17	mA
I_{MTR}	Current through V_{MTR} Power Supply	V_{DD}=1.8V,VDD3=3.3V		5		mA

Note: 74.1MHz internal DSP clock, at T_{amb} = 25°C. Current due to external loads not included.

OSCILLATOR CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
F_{OSCFM}	Oscillator Frequency (XTI/XTO)	V_{OSC} @ 3.3V		74.1		MHz
F_{OSCAM}	Oscillator Frequency (XTI/XTO)	V_{OSC} @ 3.3V		74.106		MHz

Notes: 1. The accuracy of this figure only depends on the quartz frequency precision: high stability oscillator

QUARTZ CHARACTERISTICS

Parameter Name	Parameter Value
Temperature range	-55°C ÷ +125°C
Adjustment tolerance (@ 25°C ± 3°C)	+/-20ppm
Frequency stability (-20°C ÷ +70°C)	+/-50ppm
Aging @ 25°C	5ppm/year
Shunt (static) capacitance (Co)	<6pF
Packages (holders)	UM-1; HC-52U; HC-35; HC-48U; HC-49U; HC-50U; HC-51U
Mode of oscillation	AT-3rd
Resonance resistance (ESR)	<35ohm
Oscillation Frequency (without external load)	≥74108000 Hz
Oscillation Frequency (12pF parallel load)	target 74.1MHz

DSP CORE

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
F_{dspMax}	Maximum DSP clock frequency	At 1.7V Core Power Supply and 125°C junction temperature	81.5			MHz

FM STEREO DECODER CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
a_ch	Channel Separation		50			dB
THD	Total Harmonic Distortion			0.02		%
(S+N)/N	Signal plus Noise to Noise ratio			80		dB

SAMPLE RATE CONVERTER

MCK = 18.525MHz, F_{sin}/F_{sout} = 0.820445366

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
THD+N	Total Harmonic Distortion + Noise	20Hz to 20kHz, Full Scale, 16 bit inp.		-95		dB
		20Hz to 20kHz, Full Scale, 20 bit inp.		-98		dB
		1 kHz Full Scale, 16 bit inp.		-95		dB
		10 kHz Full Scale, 16 bit inp.		-95		dB
		1 kHz Full Scale, 20 bit inp.		-105		dB
		10 kHz Full Scale, 20 bit inp		-98		dB
DR	Dynamic Range	1 kHz -60 dB - 16 bit inp.,A-Weighted		98		dB
		1 kHz -60 dB - 20 bit inp.,A-Weighted		120		dB
IPD	Interchannel Phase Deviation				0	Degree
f_c	Cutoff Frequency	@ -3 dB				Hz
R_p	Pass Band Ripple	from 0 to 20kHz	-0.01		0.01	dB
R_s	Stopband Attenuation	@24.1kHz		-120		dB
T_g	Group Delay	Fsout = 44.1 kHz		540		µs
F_{ratio}	Sampling Frequency In/Out Ratio	Fsout = 44.1 kHz	0.7		1.05	

POWER ON TIMING

Figure 1. Power on and boot sequence using I^2C

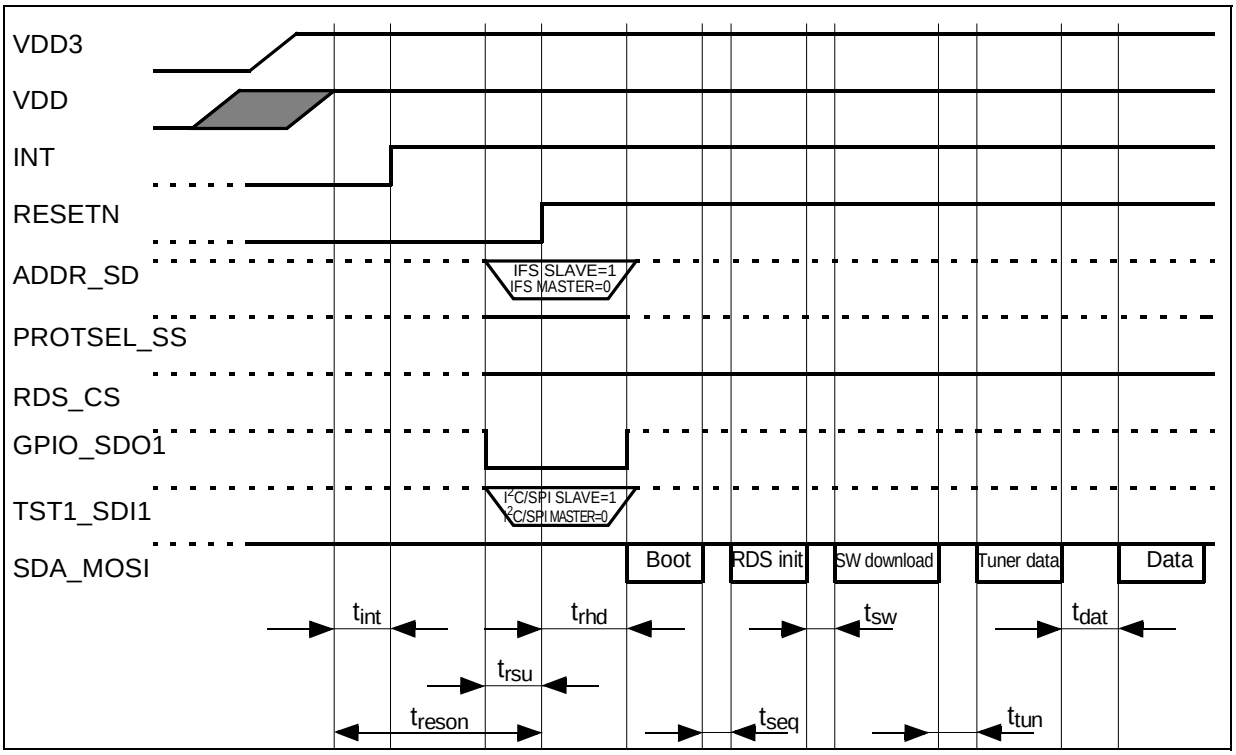
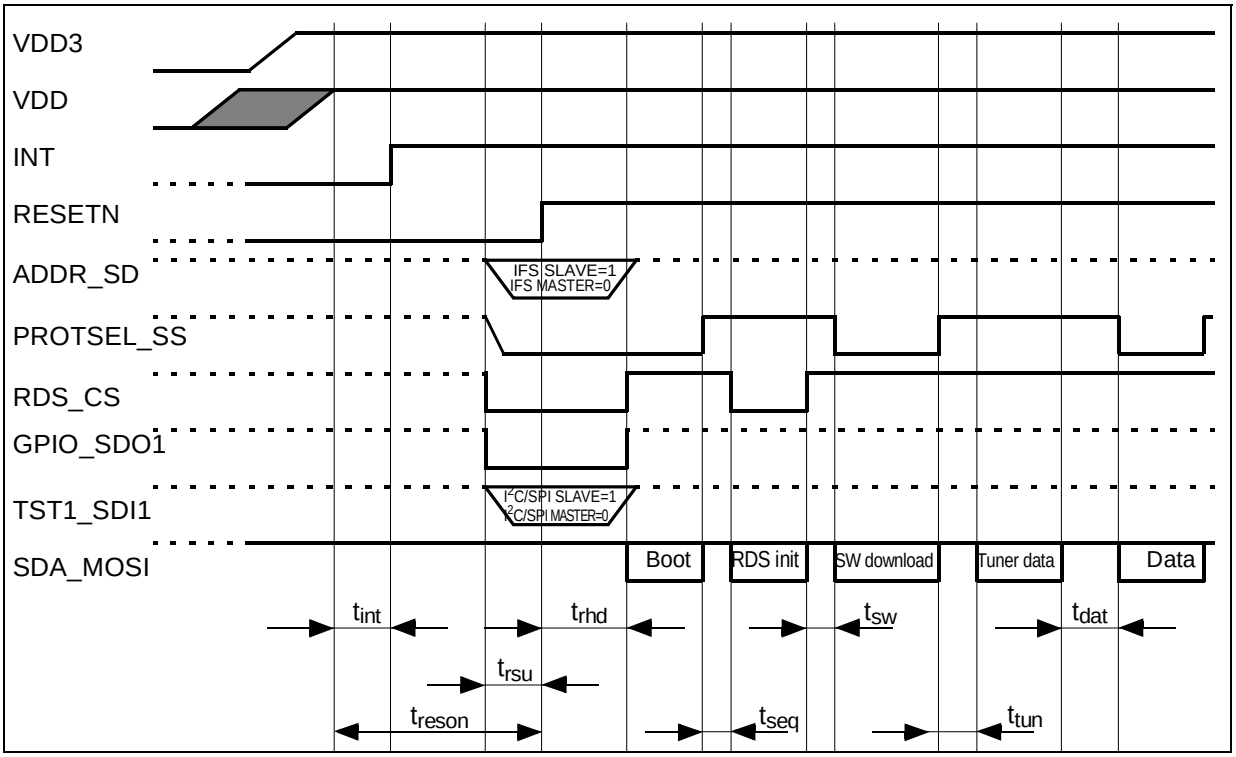


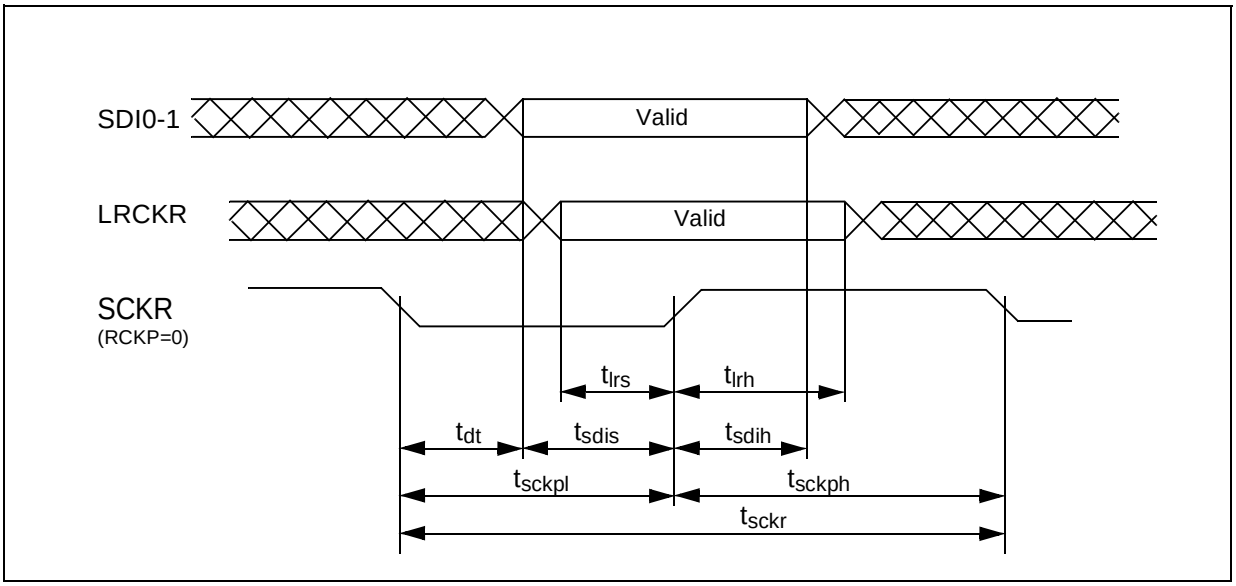
Figure 2. Power on and boot sequence using SPI



Timing	Description	Value	Unit
t_{int}	Maximux delay for INT signal	1	ms
t_{reson}	Minimum RESETN hold time at 0 after the start-up	22	ms
t_{rsu}	Minimum data set-up time	1	µs
t_{rhd}	Minimum data hold time	1	µs
t_{seq}	Minimum wait time after boot	4	ms
t_{sw}	Minimum wait time before downloading the Program Software	1	µs
t_{tun}	Minimum wait time before downloading the software to the FE	1	µs
t_{dat}	Minimum wait time before using interface protocols	1	µs

SAI INTERFACE

Figure 3. SAI Timings



Timing	Description	Value	Unit
T_{DSP}	Internal DSP Clock Period (Typical 1/74.1MHz)	13.495	ns
t_{sckr}	Minimum Clock Cycle	$32*T_{DSP}$	ns
t_{dt}	SCKR active edge to data out valid	40	ns
t_{lrs}	LRCK setup time	16	ns
t_{lrh}	LRCK hold time	9	ns
t_{sdid}	SDI setup time	16	ns
t_{sdih}	SDI hold time	9	ns
t_{sckph}	Minimum SCK high time	$0.5*t_{sckr}$	ns
t_{sckpl}	Minimum SCK low time	$0.5*t_{sckr}$	ns

Note T_{DSP} = DSP master clock cycle time = $1/F_{DSP}$

Figure 4. SAI protocol when RLRS=0; RREL=0; RCKP=1; RDIR=0

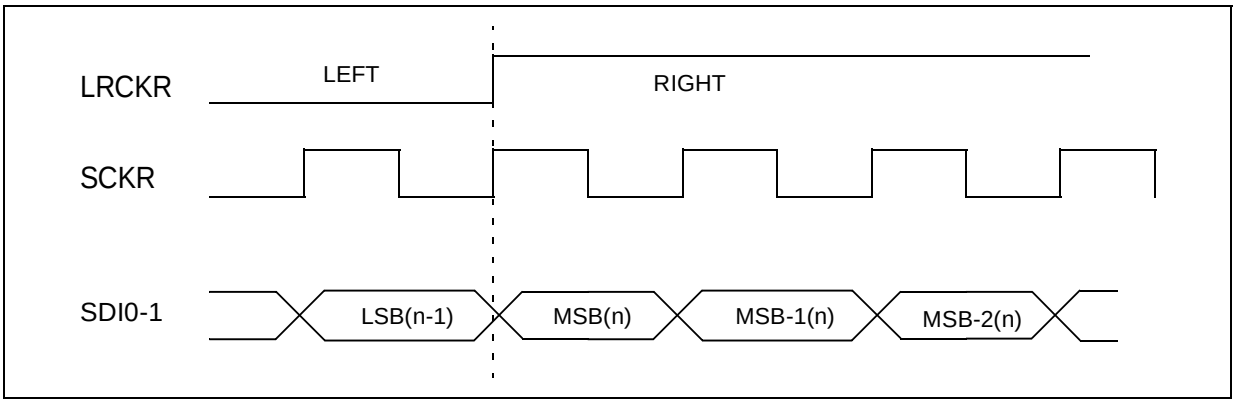


Figure 5. SAI protocol when RLRS=1; RREL=0; RCKP=1; RDIR=1.

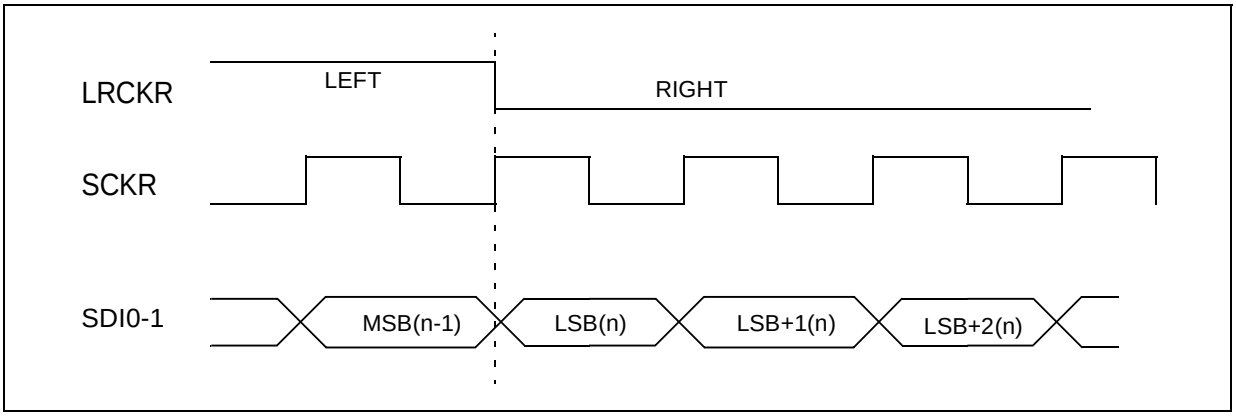


Figure 6. SAI protocol when RLRS=0; RREL=0; RCKP=0; RDIR=0.

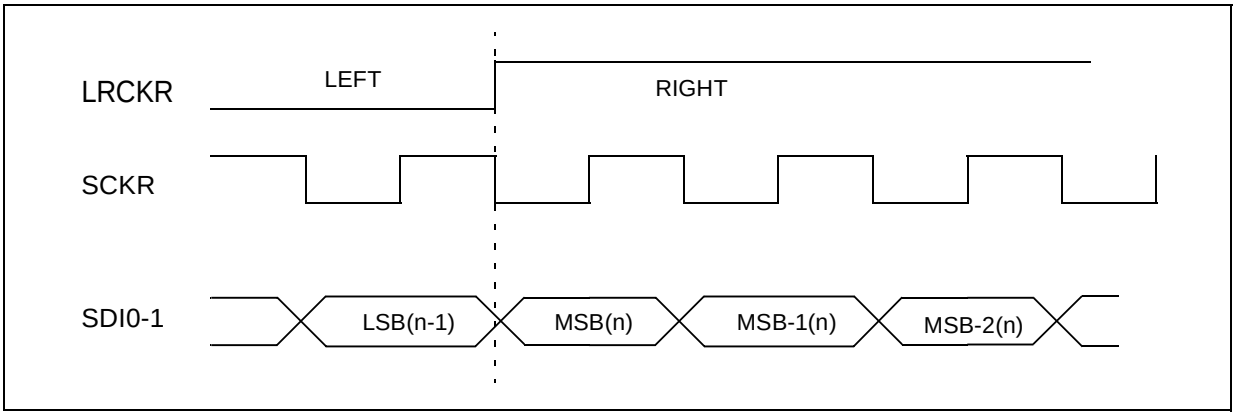
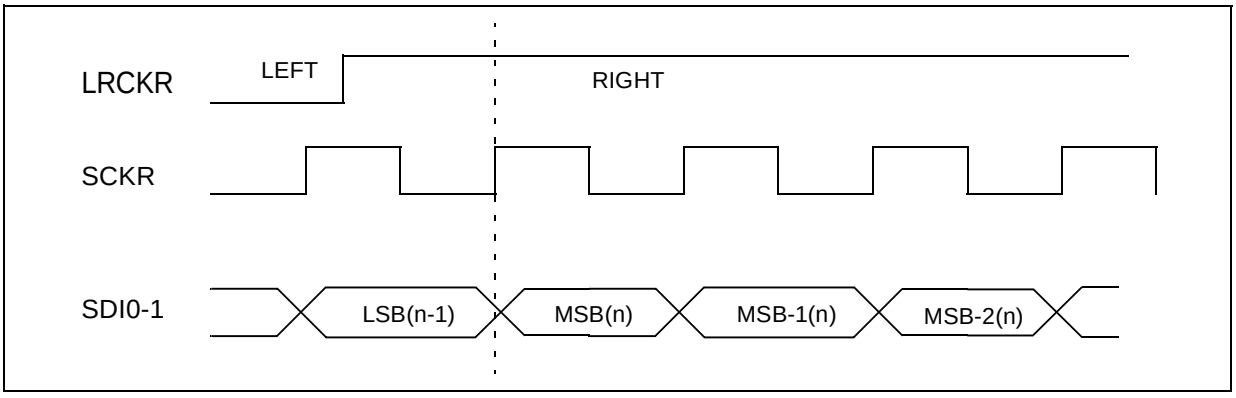
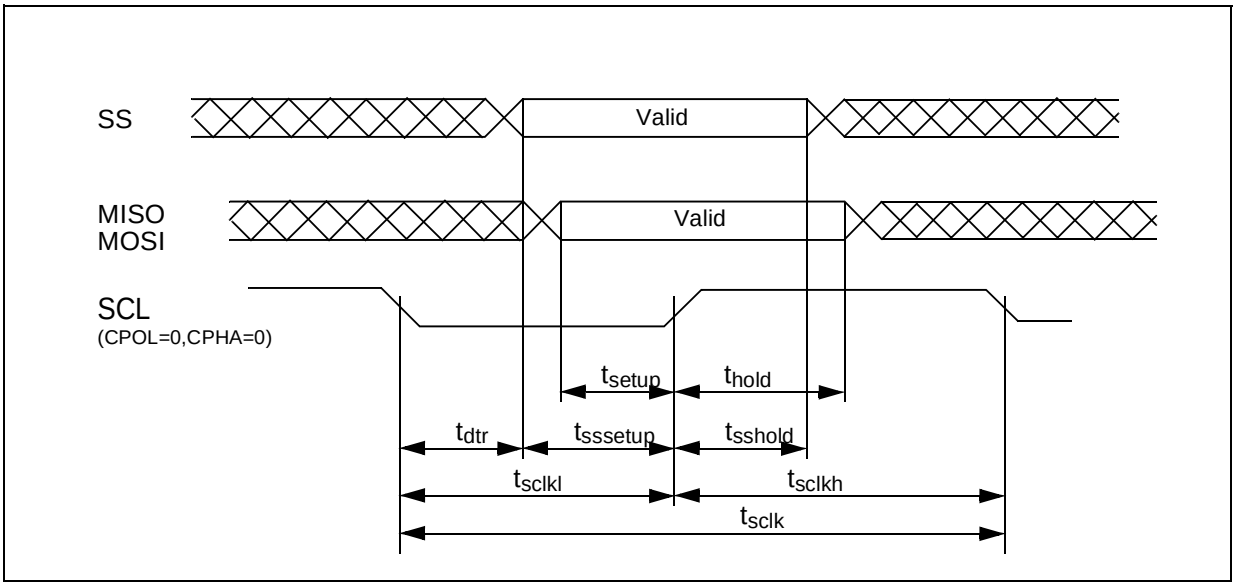


Figure 7. SAI protocol when RLRS=0; RREL=1; RCKP=1; RDIR=0.



SPI INTERFACE

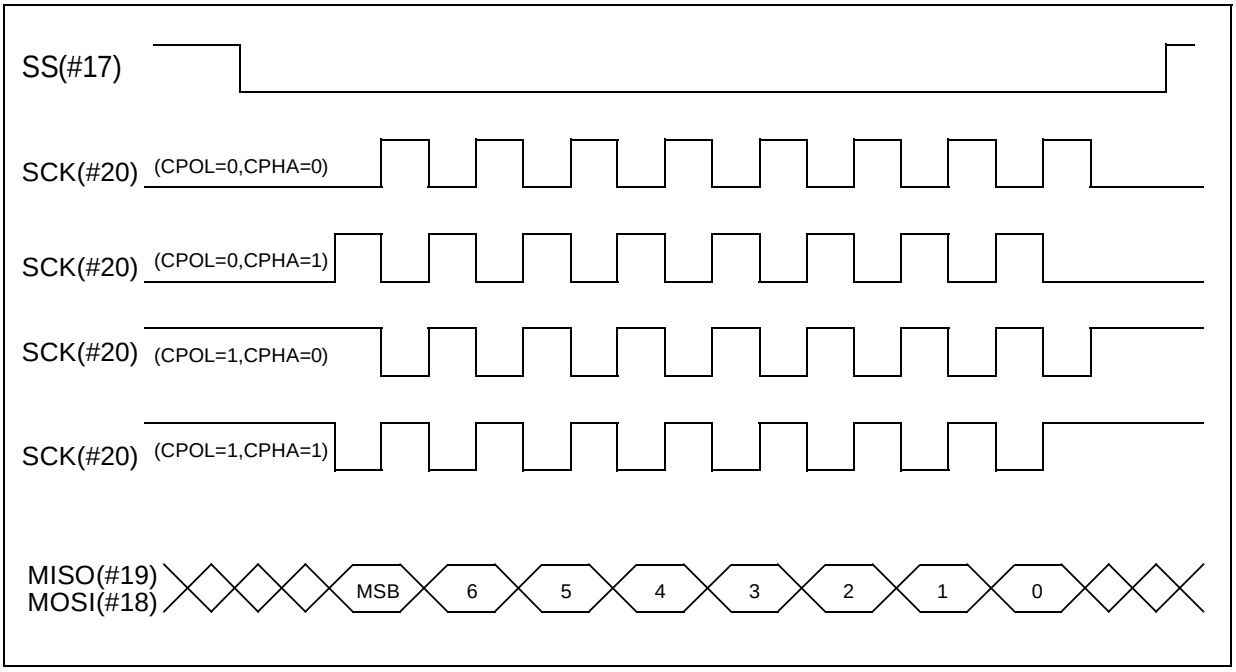
Figure 8. SPI Timings



Symbol	Description	Value	Unit
T_{DSP}	Internal DSP Clock Period (Typical 1/74.1MHz)	13.495	ns
	MASTER		
t_{sclk}	Minimum Clock Cycle	$12*T_{DSP}$	ns
t_{dtr}	Minimum Sclk edge to MOSI valid	40	ns
t_{setup}	Minimum MISO setup time	16	ns
t_{hold}	Minimum MISO hold time	9	ns
t_{sclkh}	Minimum SCK high time	$0.5*t_{sclk}$	ns
t_{sclkl}	Minimum SCK low time	$0.5*t_{sclk}$	ns
$t_{sssetup}$	Minimum SS setup time	40	ns
t_{sshold}	Minimum SS hold time	25	ns
	SLAVE		
t_{sclk}	Minimum Clock Cycle	$12*T_{DSP}$	ns
t_{dtr}	Minimum Sclk edge to MOSI valid	40	ns
t_{setup}	Minimum MOSI setup time	16	ns
t_{hold}	Minimum MOSI hold time	9	ns
t_{sclkh}	Minimum SCK high time	$0.5*t_{sclk}$	ns

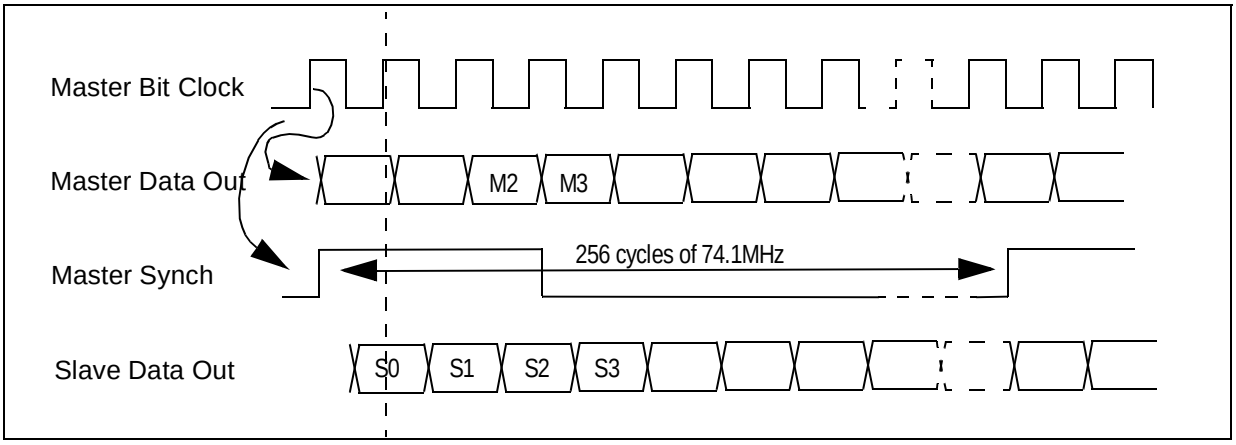
Symbol	Description	Value	Unit
t_{sclkl}	Minimum SCK high low	$0.5*t_{sclk}$	ns
$t_{sssetup}$	Minimum SS setup time	40	ns
t_{sshold}	Minimum SS hold time	20	ns

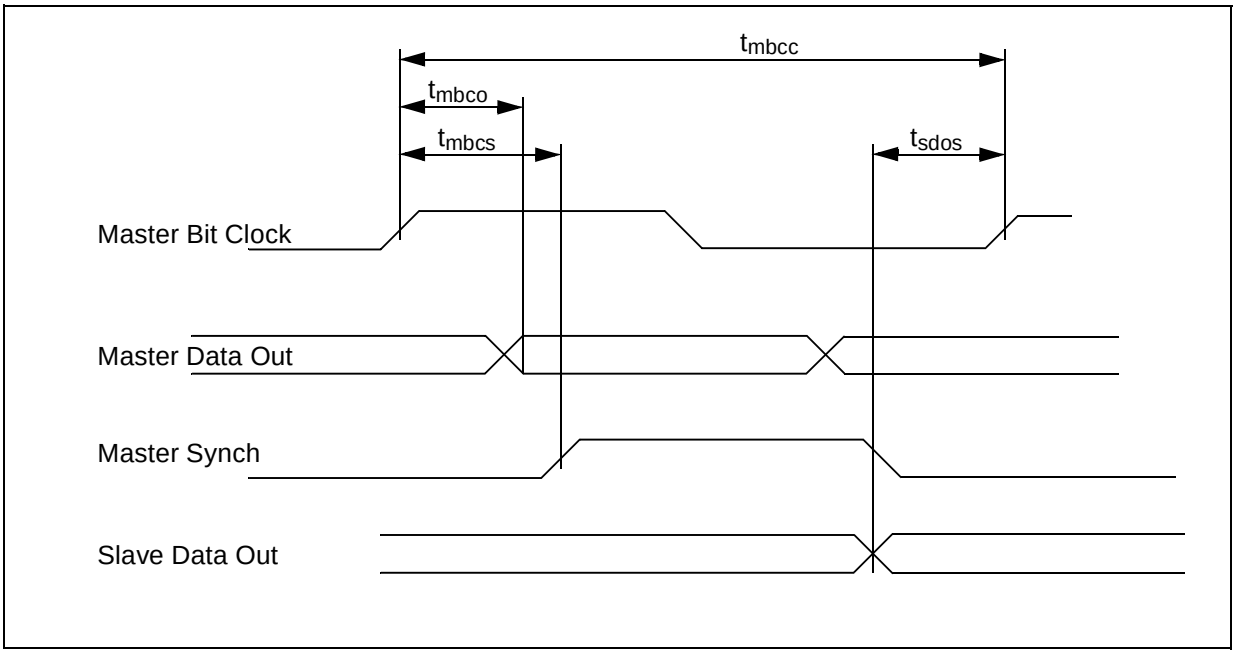
Figure 9. SPI Clocking Scheme



INTER PROCESSOR TRANSPORT INTERFACE FOR ANTENNA DIVERSITY

Figure 10. High Speed Synchronous Serial Interface - HS^{3}I



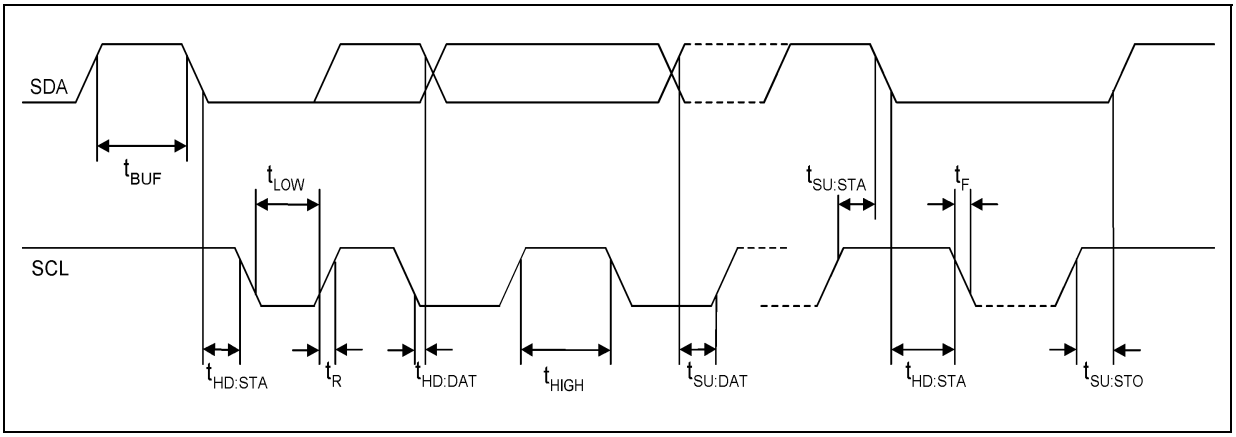


Timing	Description	Value	Unit
T_{DSP}	Internal DSP Clock Period (Typical 1/74.1MHz)		
t_{mbcc}	MBC minimum Clock Cycle	$32*T_{DSP}$	ns
t_{mbco}	MBC active edge to master data out valid	4	ns
t_{mbcs}	MBC active edge to master synch valid	4	ns
t_{sdos}	Slave Data Out setup time	6	ns

Note T_{DSP} = DSP master clock cycle time = $1/F_{DSP}$

I²C TIMING

Figure 11. DSP and RDS I²C BUS Timings.



Symbol	Parameter	Test Condition	Standard Mode I²C BUS		Fast Mode I²C BUS		Unit
			Min.	Max.	Min.	Max.	
F_{SCL}	SCLl clock frequency		0	100	0	400	kHz
t_{BUF}	Bus free between a STOP and Start Condition		4.7	–	1.3	–	µs
$t_{HD:STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated		4.0	–	0.6	–	µs
t_{LOW}	LOW period of the SCL clock		4.7	–	1.3	–	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	–	0.6	–	µs
$t_{SU:STA}$	Set-up time for a repeated start condition		4.7	–	0.6	–	µs
$t_{HD:DAT}$	DATA hold time		0	–	0	0.9	µs
t_R	Rise time of both SDA and SCL signals	Cb in pF	–	1000	20+ $0.1C_b$	300	ns
t_F	Fall time of both SDA and SCL signals	Cb in pF	–	300	20+ $0.1C_b$	300	ns
$t_{SU;STO}$	Set-up time for STOP condition		4	–	0.6	–	µs
$t_{SU:DAT}$	Data set-up time		250	--	--	100	ns
C_b	Capacitive load for each bus line		–	400	–	400	pF

FUNCTIONAL DESCRIPTION

The TDA7580 IC is a complete solution for high performance FM/AM Car Radio receivers, and has high processing power to allow Audio processing of both internal and external Audio source.

The processing engine is made of programmable DSP, with separate banks of Program and Data RAMs. In addition a number of hardware modules (peripherals) which help in the algorithm implementation of channel equalization, and FM/AM Baseband post-processing.

The HW architecture allows to perform Dual Tuner Diversity. In this case two TDA7580 are needed: one device must be configurated as Master, generates the clock and controls the main data interfaces. The second device becomes Slave and converts the second IF path, as well as helps the first chip as co-processor.

24-BIT DSP CORE

Some capabilities of the DSP are listed below:

- Single cycle multiply and accumulate with convergent rounding and condition code generation
- 24 x 24 to 56-bit MAC Unit
- Double precision multiply
- Scaling and saturation arithmetic
- 48-bit or 2 x 24-bit parallel moves
- 64 interrupt vector locations
- Fast or long interrupts possible
- Programmable interrupt priorities and masking
- Repeat instruction and zero overhead DO loops
- Hardware stack capable of nesting combinations of 7 DO loops or 15 interrupts/subroutines
- Bit manipulation instructions possible on all registers and memory locations, also Jump on bit test
- 4 pin serial debug interface
- Debug access to all internal registers, buses and memory locations
- 5 word deep program address history FIFO
- Hardware and software breakpoints for both program and data memory accesses
- Debug Single stepping, Instruction injection and Disassembly of program memory

DSP PERIPHERALS

- Clock Generation Unit (CGU)
- Stereo Decoder (HWSTER)
- Serial Audio Interface (SAI)
- Tuner AGC Keying DAC (KEYDAC)
- Programmable I/O Interface (I2C/BSPI)
- Asynchronous Sample Rate Converter (ASRC)
- IF Band Pass Sigma Delta Modulator (IFADC)
- Digital Down Converter (DDC)
- Discriminator (CORDIC)
- RDS
- Tuner Diversity HS^3I

DSP PERIPHERALS

The peripherals are mapped in the X-memory space.

Most of them can be handled by interrupt, with software programmable priority.

Peripherals running at very high rate have direct access to X and Y Data Bus for very fast movement from or to the core, by mean of single cycle instruction.

CLOCK GENERATION UNIT (CGU) and OSCILLATOR

This unit is responsible for supplying all necessary clocks and synchronization signals to the whole chip.

The control status register of this unit contains information about the current working mode (FM,AM,oscillator [master mode] or clock buffer [slave mode]), the tuner clock frequency setting, the general setup of the oscillator. This last function is performed inside the CGU, that establishes -using a self-trimming algorithm- which is the current that can bias the oscillator: this feature let the oscillator be independent from process parameters variation. The values of bias current are stored in the control status register of the CGU: 4 bit for the coarse current steps and 6 bit for the fine current steps. The bits relative to the fine current steps can be anyway corrected (written) by the DSP to perform the SW frequency trimming (+/-80Hz per step in FM; +/-250Hz in AM).

It sets up the oscillator which works off a quartz crystal of nominally 74.1MHz, generating very low distortion, thus improving the Electro Magnetic Interference. In FM mode the oscillator generates 74.1MHz, meanwhile in AM mode this frequency is shifted to 74.106MHz. The quartz characteristics are defined earlier in this document.

In Slave mode the oscillator behaves as a buffer: the chip can be then driven using an external clock. The clock divider, placed in this unit, gives the tuner the reference clock (100KHz in FM and AM_{US}, 18KHz in AM_{EU}).

STEREO DECODER (HWSTER)

The fully digital hardware stereo decoder does all the signal processing necessary to demodulate an FM MPX signal which is prepared by the channel equalization algorithm in the digital IF sampling device.

It makes up of pilot tone dependent Mono/Stereo switching as well as stereoblend and highcut.

Selectable deemphasis time constant allow the use of this module for different FM radio receiver standards.

There are built-in filters for field strength processing. In order to obtain the maximum flexibility the field strength processing and noise cancellation, however, are implemented as software inside the programming DSP, which has to provide control signals for the stages softmute, stereoblend, and highcut.

SERIAL AUDIO INTERFACE (SAI)

The two SAI modules have been embedded in such a way great flexibility is available in their use.

The two modules are fully separate and they each have a Receive and a Transmit channel, as well as they can be selected as either master or slave.

The bit clocks and Left&Right clocks are routed through the pins, so the audio interface can be chosen to be adapted to a large variety of application.

One SAI transmit channel can have the Asynchronous Sample Rate Converter in front, thus separate different audio rate domains.

Additional feature are:

- support of 16/24/32 bit word length
- programmable left/right clock polarity
- programmable rising/falling edge of the bit clock for data valid
- programmable data shift direction, MSB or LSB received/transmitted first

I²C INTERFACES

The inter Integrated Circuit bus is a single bidirectional two-wire bus used for efficient inter IC control. All I²C bus compatible devices incorporate an on-chip interface which allows them communicate directly with each other via the I²C bus.

Every component hooked up to the I²C bus has its own unique address whether it is a CPU, memory or some other complex function chip. Each of these chips can act as a receiver and /or transmitter on its functionality.

Two pins are used to interface both I²C of the DSP and RDS, which have different internal I²C address, thus reducing the on-board pin interconnections.

SERIAL PERIPHERAL INTERFACES

The DSP and RDS can have this serial interface, alternative to the I²C one. DSP and RDS SPI modules have separate pin for chip select.

The DSP SPI has a ten 24bit-words deep FIFO for both receive and transmit sections, which reduces DSP processing overhead even at high data rate.

The serial interface is needed to exchange commands and data over the LAN. During an SPI transfer, data is transmitted and received simultaneously. A serial clock line synchronizes shifting and sampling of the information on the two serial data lines. A slave select line allows individual selection of a slave SPI device.

When an SPI transfer occurs an 8-bit word is shifted out one data pin while another 8-bit character is simultaneously shifted in a second data pin.The central element in the SPI system is the shift register and the read data buffer. The system is single buffered in the transfer direction and double buffered in the receive direction.

HIGH SPEED SERIAL SYNCHRONOUS INTERFACE (HS³I)

The High Speed Serial Synchronous Interface is a module to send and receive data at high rate (up to 9.25Mbit/s per channel) in order to exchange data between 2 separate TDA7580 chip.

The exchanged data are related to signals that are used to increase reception quality in Car Radio systems, which make use of Antenna Diversity based upon two separate antenna and tuner sections.

The channel synchronization clock has a programmable duty cycle, so to reduce in-band harmonics noise.

TUNER AGC KEYING DAC (KEYDAC)

This DAC provides the front-end tuner with an analogue signal to be used to control the Automatic Gain Controlled stage, thus giving all time the best voltage dynamic range at the IFADC input.

ASYNCHRONOUS SAMPLE RATE CONVERTER (ASRC)

This hardware module provides a very flexible way to adapt the internal audio rate, to the one of an external source. It does not require further work off the DSP.

There is no need to explicitly configure the input and the output sample rates, as the ASRC solves this problem with an automatic Digital Ratio Locked Loop.

Main features are:

- Automatic Tracking of Sample Frequency
- Fully Digital Ratio Locked Loop
- Sampling Clock Jitter Rejection
- Up-conversion up to 1:2 Ratio
- Linear Phase

IF BAND PASS SIGMA DELTA ANALOGUE TO DIGITAL CONVERTER (IFADC)

The IFADC is a Band Pass Sigma Delta A to D converter with sampling rate of 37.05MHz (nominal) and notch frequency of 10.7MHz. The structure is a second order switched capacitor multi bit modulator with self calibration algorithm to adjust the notch frequency.
The differential ended input allows 4.0Vpp voltage dynamic range, and reduces the inferred noise back to the previous stage (tuner), and in turn gives high rejection to common mode noises.
The high linearity (very high IMD) is needed to fulfill good response of the channel equalization algorithm.
Low thermal and 1/f noise assures high dynamic range.

DIGITAL DOWN CONVERTER (DDC)

The DDC module allows to evaluate the in-phase and quadrature components of the incoming digital IF signal.

The I and Q computation is performed by the DDC block, which at the same time shifts down to 0-IF frequency the incoming digital signal.

After the down conversion the rate is still very high (at the 37.05MHz rate); a SincK filter samples data down by a factor of 32, decreasing it to 1.1578MHz. An additional decimation is performed by the subsequent FIR filters, thus lowering the data rate at the final 289.45kHz, being the MPX data rate.

RDS

The RDS block is an hardware cell able to process RDS/RBDS signal, intended for recovering the inaudible RDS/RBDS information which are transmitted by most of FM radio broadcasting stations.

It comprises of the following:

- Demodulation of the European Radio Data System (RDS)
- Demodulation of the US Radio Broadcast Data System (RDBS)
- Automatic Group and Block synchronisation with flywheel mechanism
- Error Detection and Correction
- RAM buffer with a storage capacity of 24 RDS blocks and related status information
- I^2C and SPI interface, with pins shared with the DSP I^2C/SPI

After filtering the oversampled MPX signal, the RDS/RDBS demodulator extracts the RDS Data Clock, RDS Data signal and the Quality information.

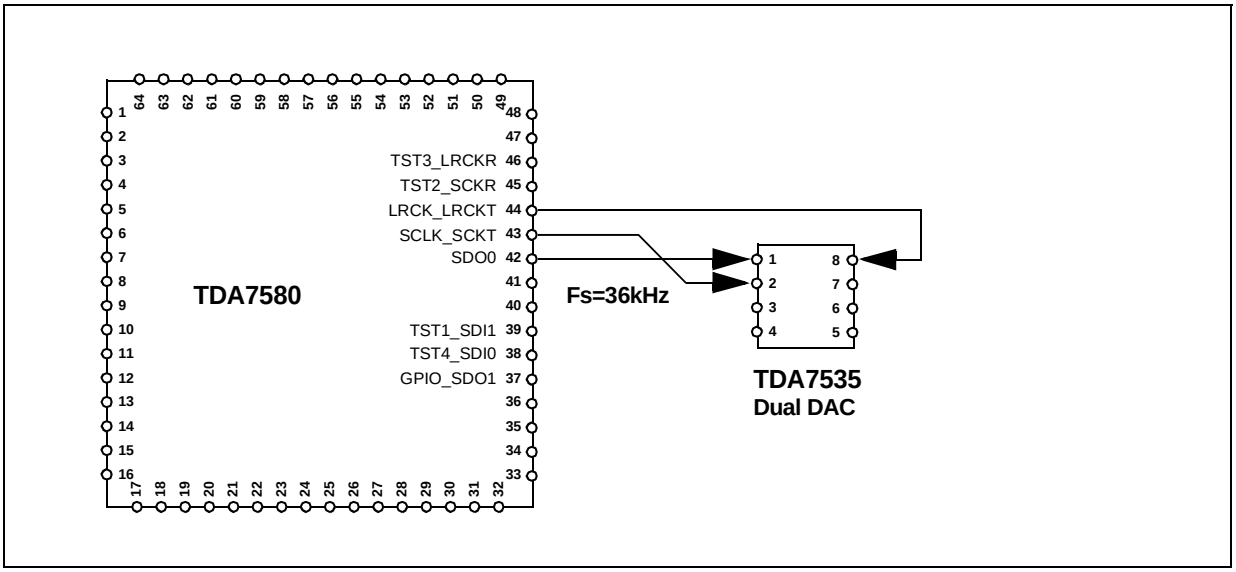
The following RDS/RBDS decoder synchronizes the bitwise RDS stream to a group and block wise information. This processing also includes error detection and error correction algorithms.

In addition, an automatic flywheel control avoids exhausting data exchange between RDS/RDBS processor and the host.

APPLICATION DIAGRAM

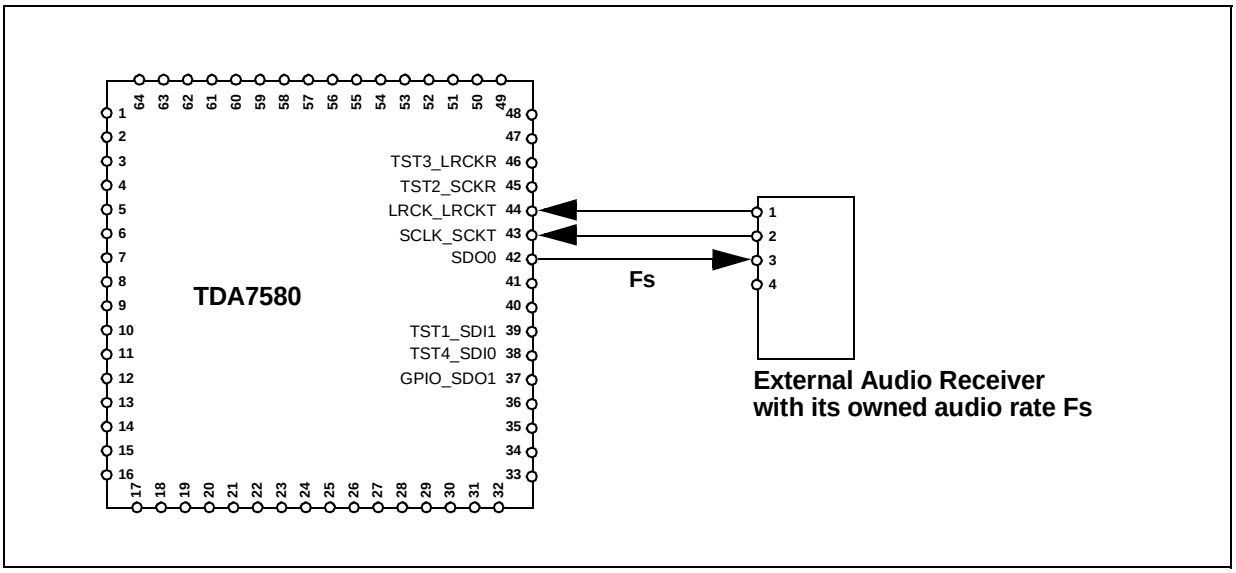
Hereafter are some examples of Applications in which the TDA7580 can be used. They are just basic references as the device can operate.

Figure 12. Radio Mode with external Slave Audio DAC



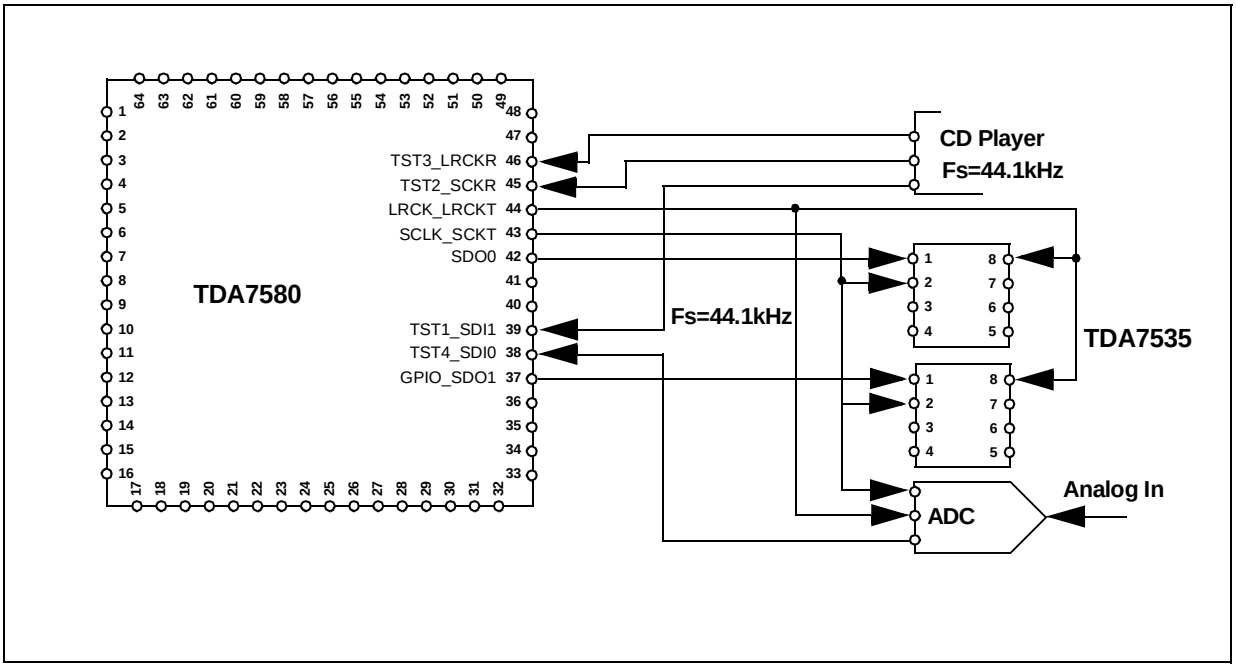
In this mode an external Slave Stereo DAC, like the ST TDA7535, can be easily connected and the TDA7580 outputs the Audio from Radio station at 36kHz rate.

Figure 13. Radio Mode with external Master Audio Device



An external digital Audio device is connected externally as a digital audio master, and the internal TDA7580 Sample Rate Converter is responsible for the conversion from internal 36kHz to the external Audio Rate.

Figure 14. Audio Mode with external Slave Audio Device



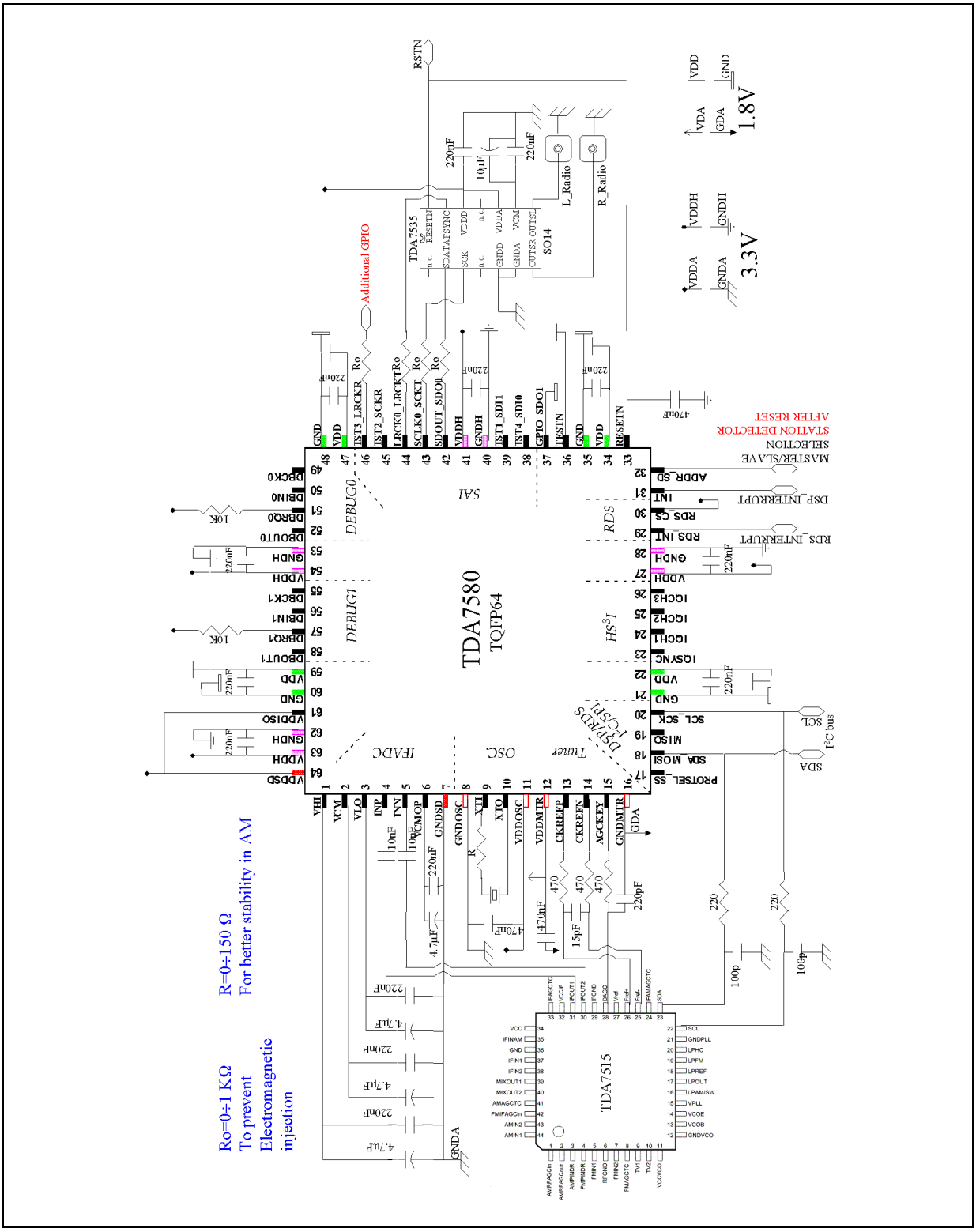
The 2 stereo channel Serial Audio Interface of the TDA7580 chip allows a very flexible application in which external Audio Source/Sinks can be connected.

The example shows an external CD player digital output giving the main Fs audio rate of the whole system. This rate is also the one of the external DACs and an ADC, being configured as slave.

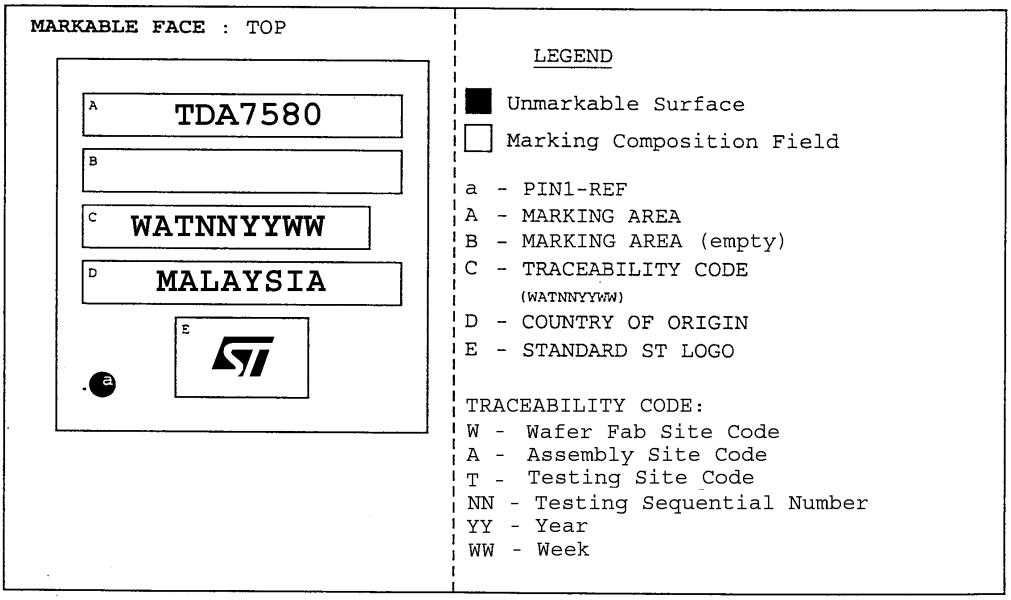
ELECTRICAL APPLICATION SCHEME

The following application diagram must be considered an example. For the real application set-up refers the application notes are necessary

.

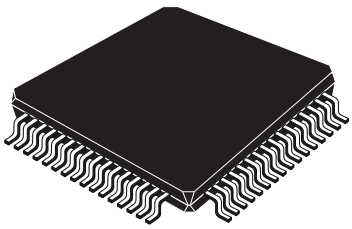


PACKAGE MARKING



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.18	0.23	0.28	0.007	0.009	0.011
C	0.12	0.16	0.20	0.0047	0.0063	0.0079
D		12.00			0.472	
D1		10.00			0.394	
D3		7.50			0.295	
e		0.50			0.0197	
E		12.00			0.472	
E1		10.00			0.394	
E3		7.50			0.295	
L	0.40	0.60	0.75	0.0157	0.0236	0.0295
L1		1.00			0.0393	
K	0°(min.), 7°(max.)					

OUTLINE AND MECHANICAL DATA



TQFP64