

October 1994

DESCRIPTION

The SSI 32F8003 Programmable Electronic Filter provides an electronically controlled low-pass filter with a separate differentiated low-pass output. A seven-pole, low-pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed equalization or bandwidth. This programmability combined with low group delay variation makes the SSI 32F8003 ideal for use in constant density recording applications. Pulse slimming equalization is accomplished by a two-pole, low-pass with a two-pole, high-pass feed forward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations.

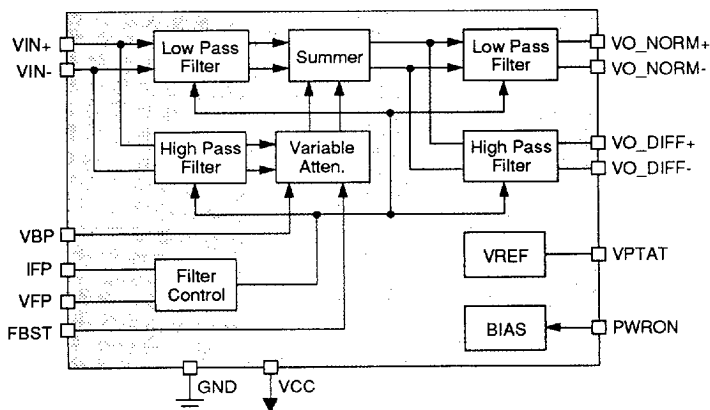
The SSI 32F8003 programmable equalization and bandwidth characteristics can be controlled by external DACs. Fixed characteristics are easily accomplished with three external resistors, in addition equalization can be switched in or out by a logic signal. The SSI 32F8003 requires only a +5V supply and is available in 16-lead SON and SOL packages.

FEATURES

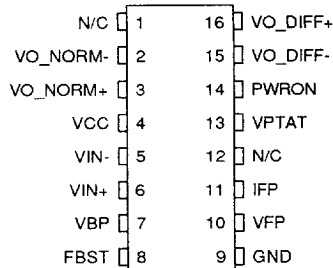
- Ideal for multi-rate systems applications
- Programmable filter cutoff frequency $f_c = 4$ to 13 MHz
- Programmable pulse slimming equalization (0 to 13.5 dB boost at the filter cutoff frequency)
- Matched normal and differentiated low-pass outputs
- Differential filter inputs and outputs
- $\pm 13\%$ cutoff frequency accuracy
- $\pm 2\%$ maximum group delay variation from $0.2 f_c$ to f_c
- Total harmonic distortion less than 1%
- No external filter components required
- +5V only operation
- 16-lead SON and SOL package
- Pin compatible with SSI 32F8011

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BLOCK DIAGRAM



PIN DIAGRAM



16-Lead SOL, SON

CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32F8003

Low-Power Programmable Electronic Filter

FUNCTIONAL DESCRIPTION

The SSI 32F8003 is a high performance programmable electronic filter. It features a 7-pole 0.05° equiripple linear phase filter with matched normal and differentiated outputs.

CUTOFF FREQUENCY PROGRAMMING

The SSI 32F8003 programmable electronic filter can be set to a filter cutoff frequency from 4 to 13 MHz with no boost.

Cutoff frequency programming can be established using either a current source fed into pin IFP whose output current is proportional to the SSI 32F8003 output reference voltage VPTAT, or by means of an external resistor tied from the output voltage reference pin VPTAT to pin VFP. The former method is optimized using the SSI 32D4661 Time Base Generator, since the current source into pin IFP is available at the DAC F output of the SSI 32D4661. Furthermore, the voltage reference input is supplied to pin VR3 of the SSI 32D4661 by the reference voltage from the VPTAT pin of the SSI 32F8003. This reference voltage is internally generated by a band-gap circuit in conjunction with a temperature varying reference to create a voltage which is proportional to absolute temperature.

The VPTAT voltage will compensate for internal temperature variation of the f_c and boost circuits.

The cutoff frequency, determined by the -3dB point relative to a very low frequency value (< 10 kHz), is related to the current IVFP injected into pin IFP by the following formulas.

$$f_c \text{ (ideal, in MHz)} = 21.67 \cdot \text{IFP} = 21.67 \cdot \text{IVFP} \cdot 1.8 / \text{VPTAT}$$

where IFP and IVFP are in mA, VPTAT is in volts, $T_a = 25^\circ\text{C}$ and $0.185 \leq \text{IFP} \leq 0.6$ mA for F8003.

If a current source is used to inject current into pin IFP, pin VFP should be left open.

If the SSI 32F8003 cutoff frequency is set using voltage VPTAT to bias up a resistor tied to pin VFP, the cutoff frequency is related to the resistor value by the following formulas.

$$f_c \text{ (ideal, in MHz)} = 21.67 \cdot \text{IFP} = 21.67 \cdot 1.8 / (3 \cdot R_x)$$

R_x in $k\Omega$

If pin VFP is used to program cutoff frequency, pin IFP should be left open.

MAGNITUDE EQUALIZATION PROGRAMMING

The magnitude equalization, measured in dB, is the amount of high frequency peaking at the cutoff frequency relative to the original -3 dB point. For example, when 12 dB boost is applied, the magnitude response peaks up 9 dB at f_c above the DC gain.

The amplitude of the input signal at frequencies near the cutoff frequency can be increased using this feature. Applying an external voltage to pin VBP which is proportional to reference output voltage VPTAT (provided by the VPTAT pin) will set the amount of boost. A fixed amount of boost can be set by an external resistor divider network connected from pin VBP to pins VPTAT and GND. No boost is applied if pin FBST, frequency boost enable, is at a low logic level.

The amount of boost FB at the cutoff frequency f_c is related to the voltage VBP by the formula

$$\text{FB (ideal, in dB)} = 20 \log_{10} [3.73(\text{VBP}/\text{VPTAT}) + 1],$$

where $0 < \text{VBP} < \text{VPTAT}$.

POWER ON / OFF

The SSI 32F8003 supports a power down mode for minimal idle mode power dissipation. When PWRON is pulled up to TTL logic high, the device is in normal operation mode. When PWRON is pulled down to TTL logic low, or left open, the device is in the power down mode.

SSI 32F8003

Low-Power Programmable Electronic Filter

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VIN+, VIN-	I	Differential Signal Inputs. The input signals must be AC coupled to these pins.
VO_NORM+, VO_NORM-	O	Differential Normal Outputs. The output signals must be AC coupled.
VO_DIFF+, VO_DIFF-	O	Differential Differentiated Outputs. For minimum time skew, these outputs should be AC coupled.
IFP	I	Frequency Program Input. The filter cutoff frequency f_c , is set by an external current IFP, injected into this pin. IFP must be proportional to voltage VPTAT. This current can be set with an external current generator such as a DAC. VFP should be left open when using this pin.
VFP	I	Frequency Program Input. The filter cutoff frequency can be set by programming a current through a resistor from VPTAT to this pin. IFP should be left open when using this pin.
VBP	I	Frequency Boost Program Input. The high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to voltage VPTAT. A fixed amount of boost can be set by an external resistor divider network connected from VBP to VPTAT and GND. No boost is applied if the FBST pin is grounded, or at logic low.
FBST	I	Frequency Boost. A high logic level or open enables the frequency boost circuitry. A low input disables this function.
PWRON	I	Power On. A high logic level enables the chip. A low level or open pin puts the chip in a low power state.
VPTAT	O	PTAT Reference Voltage. This pin outputs a reference voltage which is proportional to absolute temperature (PTAT). VBP, VFP or IFP must be referenced to this pin for proper operation.
VCC	O	+5 Volt Supply.
GND	I	Ground

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ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATINGS
Storage Temperature	-65°C to +150°C
Junction Operating Temperature, T_j	+130°C
Supply Voltage, VCC	-0.5V to 7V
Voltage Applied to Inputs	-0.5V to VCC

SSI 32F8003

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ELECTRICAL SPECIFICATIONS (continued)

RECOMMENDED OPERATING CONDITIONS

PARAMETER		RATINGS
Supply voltage	VCC	4.50V < VCC < 5.50V
Ambient Temperature	Ta	0°C < Ta < 70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified recommended operating conditions apply.

Power Supply Characteristics

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Power Supply Current	ICC	PWRON ≤ 0.8V		0.1	0.5	mA
Power Supply Current	ICC	PWRON ≥ 2.0V		46	60	mA
Power Dissipation	PD	PWRON ≥ 2.0V, VCC = 5.0V		230	300	mW
		PWRON ≥ 2.0V, VCC = 5.5V		275	330	mW
		PWRON ≤ 0.8V		0.5	2.5	mW

DC Characteristics

High Level Input Voltage	VIH	TTL input	2			V
Low Level Input Voltage	VIL				0.8	V
High Level Input Current	IIH	VIH = 2.7V			20	μA
Low Level Input Current	IIL	VIL = 0.4V	-1.5			mA

Filter Characteristics

Filter Cutoff Frequency	*fc	$fc = \frac{21.67 \text{ MHz}}{\text{mA}} (\text{IVFP})$	4		13	MHz
Filter fc Accuracy	FCA	fc = max.	-13		+13	%
VO_NORM Diff Gain	AO	F = 0.67 fc, FB = 0 dB	0.8		1.2	V/V
VO_DIFF Diff Gain	AD	F = 0.67 fc, FB = 0 dB	0.8AO		1.2AO	V/V
Frequency Boost at fc	FB	VBP = VPTAT fc = max.	12	13.5	15	dB
		fc = min.	11.5	13	14.5	dB
Frequency Boost Accuracy	FBA	VBP/VPTAT = 1.0 fc = max.	-1.5		1.5	dB

SSI 32F8003

Low-Power Programmable Electronic Filter

FILTER CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Group Delay Variation Without Boost (continued) TGDO	$f_c = \max$, $\frac{V_{BP}}{V_{PTAT}} = 0$ $F = 0.2 f_c \text{ to } f_c$	-1		+1	ns
	$f_c = \min$, $\frac{V_{BP}}{V_{PTAT}} = 0$ $F = 0.2 f_c \text{ to } f_c$	-3		+3	ns
	$F = 0.2 f_c \text{ to } f_c$, $\frac{V_{BP}}{V_{PTAT}} = 0$	-2		+2	%
	$F = f_c \text{ to } 1.75 f_c$, $\frac{V_{BP}}{V_{PTAT}} = 0$	-3		+3	%
Group Delay Variation With Boost TGDB	$f_c = \max$, $V_{BP} = V_{PTAT}$ $F = 0.2 f_c \text{ to } f_c$	-1		+1	ns
	$f_c = \min$, $V_{BP} = V_{PTAT}$ $F = 0.2 \text{ to } f_c$	-3		+3	ns
	$F = 0.2 f_c \text{ to } f_c$, $V_{BP} = V_{PTAT}$	-2		+2	%
	$F = f_c \text{ to } 1.75 f_c$, $V_{BP} = V_{PTAT}$	-3		+3	%
Filter Input Dynamic Range VIF	THD = 1% max, $F = 0.67 f_c$, $V_{BP} = 0V$ (1000 pF across Rx)	1			Vp-p
	THD = 1.5% max, $F = 0.67 f_c$, $V_{BP} = 0V$, Normal output (1000 pF across Rx)	1.5			Vp-p
Filter Input Dynamic Range VIF	THD = 2.0% max, $F = 0.67 f_c$, $V_{BP} = 0V$, Differentiated output (1000 pF across Rx)	1.5			Vp-p
Filter Diff Input Resistance RIN		3	4.3		k Ω
Filter Input Capacitance CIN				7	pF
Output Noise Voltage Differentiated Output EOOUT	BW = 100 MHz, $R_s = 50\Omega$ $f_c = \max$, $V_{BP} = 0V$		3		mV rms

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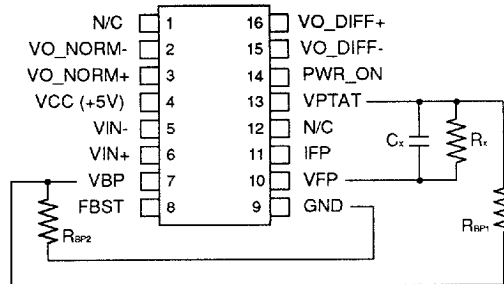
ELECTRICAL SPECIFICATIONS (continued)

FILTER CONTROL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Output Noise Voltage Normal Output	EOUT BW = 100 MHz, $R_s = 50\Omega$ $f_c = \text{max}$, VBP = 0V		1.8		mV rms
Output Noise Voltage Differentiated Output	EOUT BW = 100 MHz, $R_s = 50\Omega$ $f_c = \text{max}$, VBP = VPTAT		4.3		mV rms
Output Noise Voltage Normal Output	EOUT BW = 100 MHz, $R_s = 50\Omega$ $f_c = \text{max}$, VBP = VPTAT		2.2		mV rms
Filter Output Sink Current	IO –	1			mA
Filter Output Source Current	IO +	2			mA
Filter Output Resistance (Single ended)	RO IO+ = 1.0 mA			60	Ω
Reference Voltage	VPTAT Tj = 25°C		1.8		V
PTAT Voltage Input	VFP		2/3 VPTAT		V
Programming Current Range	IVFP Ta = 25°C	0.185		0.6	mA
Programming Voltage Range	V _{VBP}	0		VPTAT	V
Voltage at pin IFP	V _{IFP} I _{VFP} = 0 mA		2/3 VPTAT		V
Power Up Time	$f_c = \text{min}$			1.5	μs
	$f_c = \text{max}$			1	μs
Power Down Time				1	μs

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Low-Power Programmable Electronic Filter



$$VPTAT = 1.8V \text{ (25°C)}$$

$$VVFP = 2/3 \text{ (VPTAT)}$$

$$IVFP \text{ range: } 0.185 \text{ mA to } 0.6 \text{ mA @25°C}$$

Fixed frequency programming is accomplished as shown in the drawing above.

In this case IVFP (programming current) is equivalent to $\frac{VPTAT}{3} \cdot \frac{1}{R_x}$

i.e., $f_c = 13 \text{ MHz}$ then

$$IVFP = 0.6 \text{ mA @25°C} \quad R_x = 1 \text{ k}\Omega$$

Fixed boost programming is also accomplished as shown above. In this case VVBP is set by a voltage divider, where VVBP is a fraction of VPTAT.

i.e., boost = 9 dB then,

$$VBP/VPTAT = 0.488 \quad 9 \text{ dB} = 20 \log [3.73 (0.488) + 1]$$

$$\frac{R_{BP2}}{R_{BP1}} = \frac{1}{\left(\frac{VPTAT}{VBP} - 1\right)} = 0.953$$

$C_x = 1000 \text{ pF}$ - C_x is needed for lower THD at lower f_c .

FIGURE 4: 32F8003 Applications Setup

SSI 32F8003

Low-Power Programmable Electronic Filter

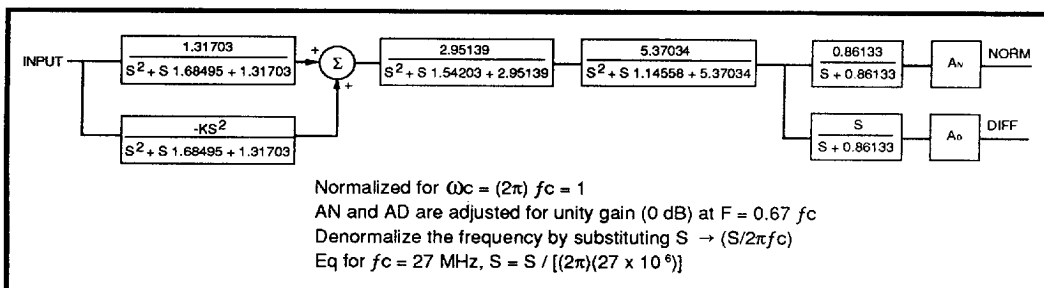


FIGURE 5: 32F8003 Normalized Block Diagram

TABLE 1: 32F8003 Frequency Boost Calculations, $K = 1.31703 (10^{\text{BOOST (dB)/20}} - 1)$

Assuming 13.5 dB boost for VBP = VPTAT	Boost	K	$\frac{\text{VBP}}{\text{VPTAT}}$	Boost	K	$\frac{\text{VBP}}{\text{VPTAT}}$
	1 dB	0.16	0.033	6 dB	1.31	0.267
	2 dB	0.34	0.069	7 dB	1.63	0.332
	3 dB	0.54	0.110	8 dB	1.99	0.405
	4 dB	0.77	0.157	9 dB	2.40	0.488
	5 dB	1.03	0.209	10 dB	2.85	0.580
or, boost in dB = $20 \log \left[3.73 \left(\frac{\text{VBP}}{\text{VPTAT}} \right) + 1 \right]$				11 dB	3.36	0.683
				12 dB	3.43	0.799
				13 dB	4.57	0.929
		$\frac{\text{VBP}}{\text{VPTAT}}$	Boost	$\frac{\text{VBP}}{\text{VPTAT}}$	Boost	
		0.1	2.753 dB	0.6	10.206 dB	
		0.2	4.841 dB	0.7	11.153 dB	
		0.3	6.523 dB	0.8	12.006 dB	
		0.4	7.391 dB	0.9	12.784 dB	
		0.5	9.142 dB	1.0	13.5 dB	

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Low-Power Programmable

Electronic Filter

TABLE 2: Calculations

Typical change in f -3 dB point with boost

Boost (dB)	Gain@ f_c (dB)	Gain@ peak (dB)	f_{peak}/f_c	f -3dB/ f_c
0	-3	0.00	no peak	1.00
1	-2	0.00	no peak	1.21
2	-1	0.00	no peak	1.51
3	0	0.15	0.70	1.80
4	1	0.99	1.05	2.04
5	2	2.15	1.23	2.20
6	3	3.41	1.33	2.33
7	4	4.68	1.38	2.43
8	5	5.94	1.43	2.51
9	6	7.18	1.46	2.59
10	7	8.40	1.48	2.66
11	8	9.59	1.51	2.73
12	9	10.77	1.51	2.80
13	10	11.92	1.53	2.87
14	11	13.06	1.53	2.93

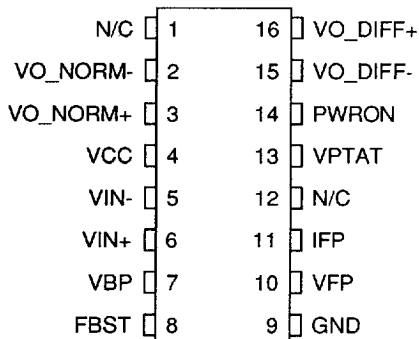
Notes: 1. f_c is the original programmed cutoff frequency with no boost
 2. f -3 dB is the new -3 dB value with boost implemented
 3. f_{peak} is the frequency where the amplitude reaches its maximum value with boost implemented
 i.e., $f_c = 9$ MHz when boost = 0 dB
 if boost is programmed to 5 dB then f -3 dB = 19.8 MHz
 $f_{peak} = 11.07$ MHz

SSI 32F8003

Low-Power Programmable Electronic Filter

PACKAGE PIN DESIGNATIONS

(Top View)



16-Lead SON, SOL

CAUTION: Use handling procedures necessary
for a static sensitive component.

THERMAL CHARACTERISTICS: θ_{ja}

16-lead SON (150 mil)	105°C/W
16-lead SOL (300 mil)	100°C/W

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 32F8003 16-Lead SOL	32F8003-CL	32F8003-CL
16-Lead SON	32F8003-CN	32F8003-CN

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