MICROCHIP

28C16A

16K (2K x 8) CMOS EEPROM

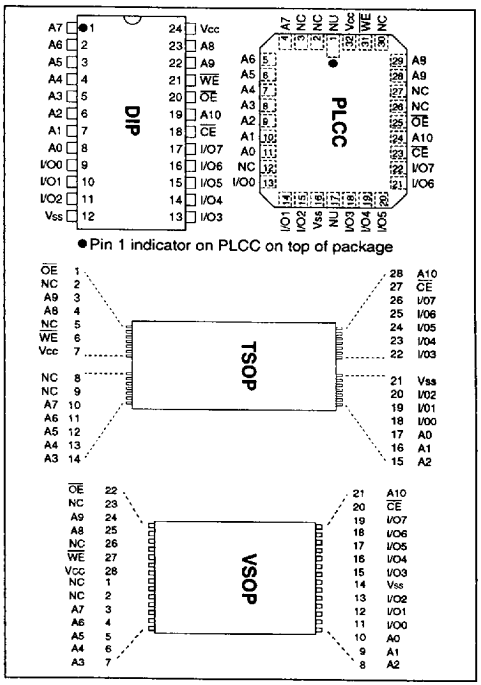
FEATURES

- Fast Read Access Time—150 ns
- CMOS Technology for Low Power Dissipation
  - 30 mA Active
  - 100 µA Standby
- Fast Byte Write Time—200 µs or 1 ms
- Data Retention >200 years
- High Endurance - Minimum 10^4 Erase/Write Cycles
- Automatic Write Operation
  - Internal Control Timer
  - Auto-Clear Before Write Operation
  - On-Chip Address and Data Latches
- $\overline{\text{Data}}$ polling
- Chip Clear Operation
- Enhanced Data Protection
  - Vcc Detector
  - Pulse Filter
  - Write Inhibit
- Electronic Signature for Device Identification
- 5-Volt-Only Operation
- Organized 2Kx8 JEDEC Standard Pinout
- 24-pin Dual-In-Line Package
- 32-pin PLCC Package
- 28-pin Thin Small Outline Package (TSOP) 8x20mm
- 28-pin Very Small Outline Package (VSOP) 8x13.4mm
- Available for Extended Temperature Ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

DESCRIPTION

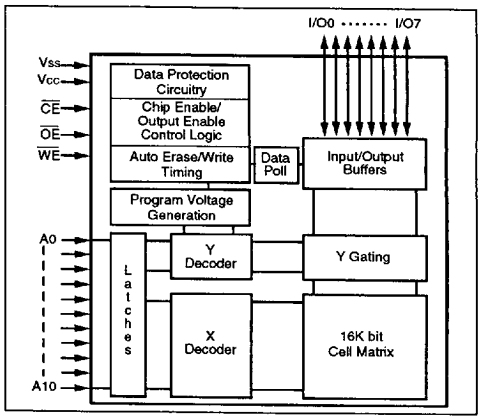
The Microchip Technology Inc. 28C16A is a CMOS 16K non-volatile electrically Erasable PROM. The 28C16A is accessed like a static RAM for the read or write cycles without the need of external components. During a "byte write", the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. To determine when a write cycle is complete, the 28C16A uses $\overline{\text{Data}}$ polling. $\overline{\text{Data}}$ polling allows the user to read the location last written to when the write operation is complete. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are required. A complete family of packages is offered to provide the utmost flexibility in applications.

PACKAGE TYPES



●Pin 1 indicator on PLCC on top of package

BLOCK DIAGRAM



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1.0 ELECTRICAL CHARACTERISTICS

1.1 MAXIMUM RATINGS*

Vcc and input voltages w.r.t. Vss ..... -0.6V to + 6.25V

Voltage on $\overline{OE}$ w.r.t. Vss ..... -0.6V to +13.5V

Voltage on A9 w.r.t. Vss ..... -0.6V to +13.5V

Output Voltage w.r.t. Vss ..... -0.6V to Vcc+0.6V

Storage temperature ..... -65°C to +125°C

Ambient temp. with power applied ..... -50°C to +95°C

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0 - A10	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
Vcc	+5V Power Supply
Vss	Ground
NC	No Connect; No Internal Connection
NU	Not Used; No External Connection is Allowed

TABLE 1-2: READ/WRITE OPERATION DC CHARACTERISTICS

Vcc = +5V ±10%
Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb = -40°C to +85°C

Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic '1' Logic '0;	VIH VIL	2.0 -0.1	Vcc+1 0.8	V V	
Input Leakage	—	ILI	-10	10	µA	VIN = -0.1V to Vcc+1
Input Capacitance	—	CIN	—	10	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Output Voltages	Logic '1' Logic '0'	VOH VOL	2.4	 0.45	V V	IOH = -400µA IOL = 2.1 mA
Output Leakage	—	ILO	-10	10	µA	VOUT = -0.1V to Vcc+0.1V
Output Capacitance	—	COUT	—	12	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Power Supply Current, Active	TTL input	ICC	—	30	mA	f = 5 MHz (Note 1) Vcc = 5.5V;
Power Supply Current, Standby	TTL input TTL input CMOS input	ICC(S)TTL ICC(S)TTL ICC(S)CMOS	—	2 3 100	mA mA µA	$\overline{CE}$ = VIH (0°C to +70°C) $\overline{CE}$ = VIH (-40°C to +85°C) $\overline{CE}$ = Vcc-0.3 to Vcc+1

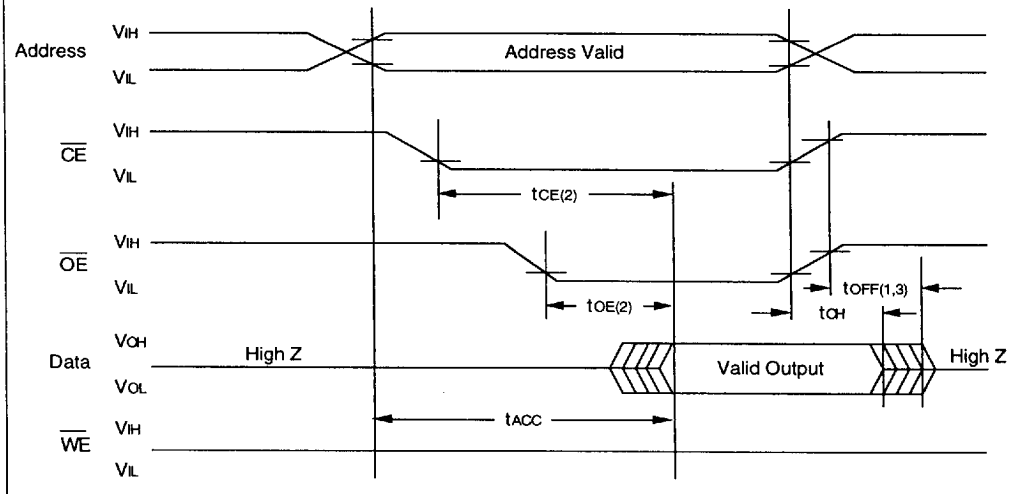
Note 1: AC power supply current above 5 MHz; 1 mA/MHz.

TABLE 1-3: READ OPERATION AC CHARACTERISTICS

AC Testing Waveform: V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; Vol = 0.8V Output Load: 1 TTL Load + 100pF Input Rise and Fall Times: 20 ns Ambient Temperature: Commercial (C): Tamb = 0°C to +70°0°C Industrial (I): Tamb = -40°C to +85°C									
Parameter	**Sym**	**28C16A-15**		**28C16A-20**		**28C16A-25**		**Units**	**Conditions**
		Min	**Max**	**Min**	**Max**	**Min**	**Max**		
Address to Output Delay	tACC	—	150	—	200	—	250	ns	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
$\overline{CE}$ to Output Delay	tCE	—	150	—	200	—	250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	tOE	—	70	—	80	—	100	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ High to Output Float	tOFF	0	50	0	55	0	70	ns	
Output Hold from $\overline{CE}$ or $\overline{OE}$, whichever occurs first	tOH	0	—	0	—	0	—	ns	
Endurance	—	1M	—	1M	—	1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note)

Note: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our BBS or website.

FIGURE 1-1: READ WAVEFORMS



Notes: (1) tOFF is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to tCE - tOE after the falling edge of $\overline{CE}$ without impact on tCE
(3) This parameter is sampled and is not 100% tested

TABLE 1-4: BYTE WRITE AC CHARACTERISTICS

	AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V Output Load: 1 TTL Load + 100 pF Input Rise/Fall Times: 20 ns Ambient Temperature: Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Remarks**
Address Set-Up Time	t_{AS}	10	—	ns	
Address Hold Time	t_{AH}	50	—	ns	
Data Set-Up Time	t_{DS}	50	—	ns	
Data Hold Time	t_{DH}	10	—	ns	
Write Pulse Width	t_{WPL}	100	—	ns	Note 1
Write Pulse High Time	t_{WPH}	50	—	ns	
$\overline{OE}$ Hold Time	t_{OEH}	10	—	ns	
$\overline{OE}$ Set-Up Time	t_{OES}	10	—	ns	
Data Valid Time	t_{DV}	—	1000	ns	Note 2
Write Cycle Time (28C16A)	t_{WC}	—	1	ms	0.5 ms typical
Write Cycle Time (28C16AF)	t_{WC}	—	200	µs	100 µs typical

Note 1: A write cycle can be initiated be $\overline{CE}$ or $\overline{WE}$ going low, whichever occurs last. The data is latched on the positive edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs first.

2: Data must be valid within 1000ns max. after a write cycle is initiated and must be stable at least until t_{DH} after the positive edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first.

FIGURE 1-2: PROGRAMMING WAVEFORMS

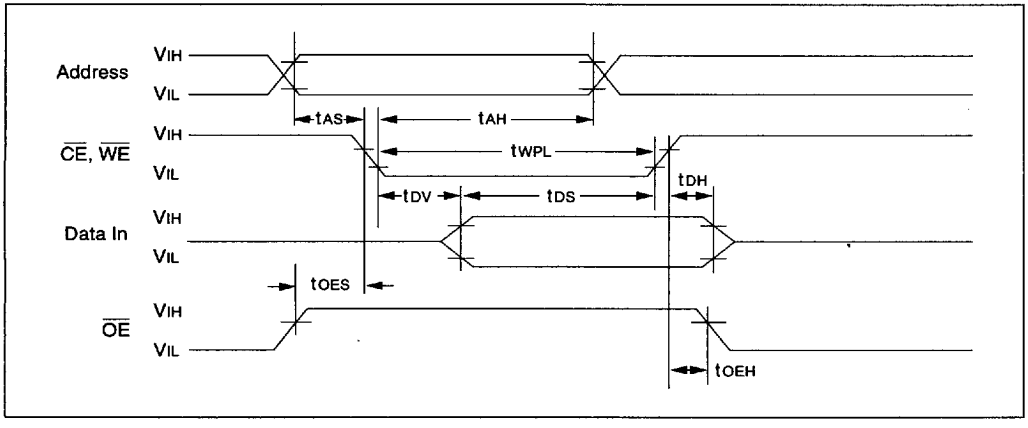


FIGURE 1-3: $\overline{\text{DATA}}$ POLLING WAVEFORMS

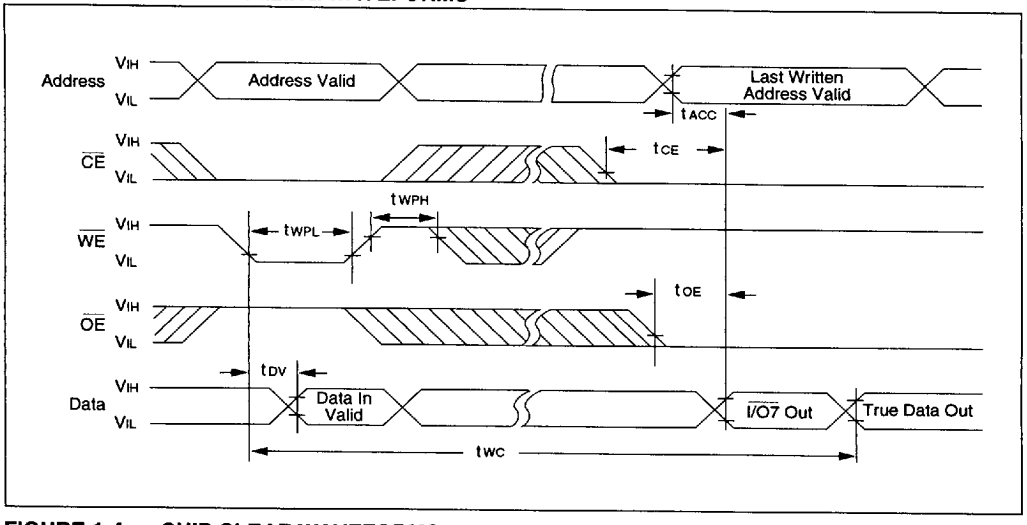


FIGURE 1-4: CHIP CLEAR WAVEFORMS

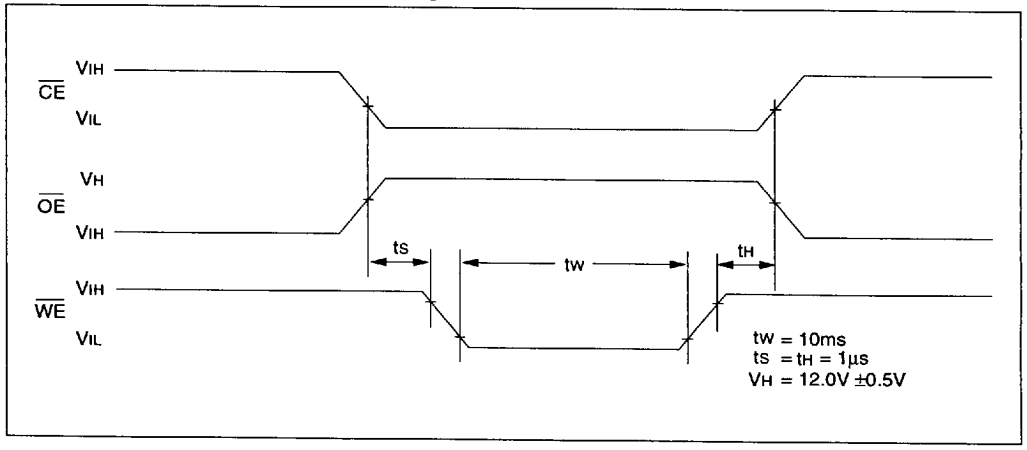


TABLE 1-5: SUPPLEMENTARY CONTROL

Mode	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	A9	Vcc	I/Oi
Chip Clear	VIL	VH	VIL	X	Vcc	
Extra Row Read	VIL	VIL	VIH	A9 = VH	Vcc	Data Out
Extra Row Write	*	VIH	*	A9 = VH	Vcc	Data In
Note 1: VH = 12.0V±0.5V		* Pulsed per programming waveforms.				

2.0 DEVICE OPERATION

The Microchip Technology Inc. 28C16A has four basic modes of operation—read, standby, write inhibit, and byte write—as outlined in the following table.

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	L	L	H	DOUT
Standby	H	X	X	High Z
Write Inhibit	H	X	X	High Z
Write Inhibit	X	L	X	High Z
Write Inhibit	X	X	H	High Z
Byte Write	L	H	L	DIN
Byte Clear	Automatic Before Each "Write"			

X = Any TTL level.

2.1 Read Mode

The 28C16A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and is used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the output t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

2.2 Standby Mode

The 28C16A is placed in the standby mode by applying a high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

2.3 Data Protection

In order to ensure data integrity, especially during critical power-up and power-down transitions, the following enhanced data protection circuits are incorporated:

First, an internal V_{CC} detect (3.3 volts typical) will inhibit the initiation of non-volatile programming operation when V_{CC} is less than the V_{CC} detect circuit trip.

Second, there is a $\overline{WE}$ filtering circuit that prevents $\overline{WE}$ pulses of less than 10 ns duration from initiating a write cycle.

Third, holding $\overline{WE}$ or $\overline{CE}$ high or $\overline{OE}$ low, inhibits a write cycle during power-on and power-off (V_{CC}).

2.4 Write Mode

The 28C16A has a write cycle similar to that of a Static RAM. The write cycle is completely self-timed and initiated by a low going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$, the address information is latched. On rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched.

2.5 Data Polling

The 28C16A features Data polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of I/O7 (I/O0 to I/O6 are indeterminable). After completion of the write cycle, true data is available. Data polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

2.6 Electronic Signature for Device Identification

An extra row of 32 bytes of EEPROM memory is available to the user for device identification. By raising A9 to 12V ±0.5V and using address locations 7EO to 7FF, the additional bytes can be written to or read from in the same manner as the regular memory array.

2.7 Chip Clear

All data may be cleared to 1's in a chip clear cycle by raising $\overline{OE}$ to 12 volts and bringing the $\overline{WE}$ and $\overline{CE}$ low. This procedure clears all data, except for the extra row.

NOTES:

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28C16A Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.