REVISIONS

SYM	DATE	CN	SHT	DESCRIPTION	BY	CH	APP

June 24, 1985

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PRELIMINARY CUSTOMER PROCUREMENT SPECIFICATION

28CP64 997719

(PAGE MODE)

64K

CMOS Memory, 8K x (8Kx8) EEPROM, 3-State

SHEET	1-11													
LAST REV														

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DISTRIBUTION LIST

SUPERSEDES

SUPERSEDED BY

GENERAL INSTRUMENT MICROELECTRONICS GROUP

TITLE CPS for (8Kx8) CMOS EEPROM (28CP64) With Page Mode

PLANT

MODULE

OPERATION

	WRITTEN	APPROVED					
BY	R. Herber						
DATE	7-2-85						

SHEET 1 OF 11

SPEC. NO. 10167

REV A

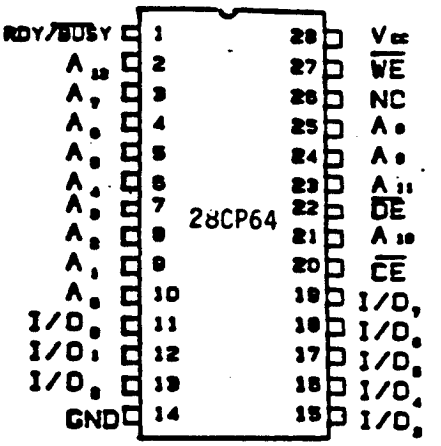
7-2

FORM 1E104 (3/81)

28CP64
64K (8Kx8) CMOS ELECTRICALLY ERASABLE PROM

Features

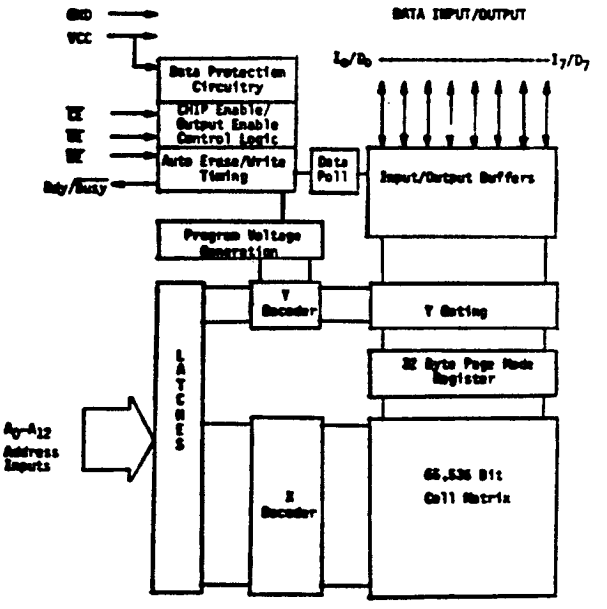
- 5 Volt Only Operation
- High Performance/Reliability Double Metal CMOS Technology
- Automatic Write Operation
  - Internal Control Timer
  - Auto-Clear Before Write Operation
- Ready/$\overline{\text{BUSY}}$ (Open Drain)
- $\overline{\text{Data}}$ Polling
- Electronic Signature
  - Device Identification
  - Tracking
- On-Chip Address and Data Latches
- 32 Byte Auto Page Mode
  - 1 to 32 Byte Page Load
  - Self-Timed Page Store
  - Auto-Clear before Write
- Low Power
  - 100uA Standby
  - 30mA Active
- Enhanced/Timed Data Protection Circuitry
- Data Retention > 10 years
- Full Military & Extended Temperature Ranges
  - 0° to 70°C Commercial
  - -40° to 85°C Industrial
  - -55° to 125°C Military
- High Endurance 10^5 Erase/Write Cycles per Byte
- Extremely Fast 1mSec Byte Write Time
- Fast Read Access Time
  - 28CP64 - 05 50nS max
  - 28CP64 - 10 100nS max
  - 28CP64 - 15 150nS max
- Chip Clear Operation
- JEDEC Approved Byte-Wide Pin Out



PIN CONFIGURATION

A_0 - A_{12}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O_0 - I/O_7	DATA INPUTS/OUTPUTS
RDY/$\overline{BUSY}$	READY/$\overline{BUSY}$

PIN NAMES



FUNCTIONAL BLOCK DIAGRAM
28CP64

Description

The General Instrument 28CP64 is a low-power, high-performance 8,192x8 bit non-volatile Electrically Erasable and Programmable Read Only Memory with popular, easy to use features. The device is manufactured with General Instrument's advanced and reliable non-volatile CMOS technology.

The 28CP64 is accessed like a static RAM for the read or write cycles without the need of external components. During a "byte write," the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer within 100uSec (<.05sec required for entire chip). A new access for a read or write cycle can begin when the RDY signal is asserted. This condition can also be tested by $\overline{\text{DATA}}$ polling of output O_7.

A page-mode, write feature allows 1 to 32 bytes of data to be written in an single-write cycle.

The 28CP64 operates from a single 5V supply and is packaged in a standard JEDEC-approved 28-pin package. All necessary programming voltages are internally generated and timed.

The CMOS technology offers fast access times of 50nS (28CP64-05) at low power dissipation of 50mA. When the chip is deselected, the standby current is less than 100uA.

The 28CP64's fast memory access time allows for direct polling with microprocessors without waiting. This feature enables the EEPROM to act as a ROM.

DEVICE OPERATION

The General Instrument 28CP64 has four basic modes of operation as outlined in the following table.

MODE	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{WE}$ (27)	I/O (11-13,15-19)	Rdy/Busy (1) Note 1
READ	L	L	H	Dout	H
STANDBY	H	X	X	High Z	H
WRITE INHIBIT	H	X	X	High Z	H
WRITE INHIBIT	X	H	X	-	H
WRITE INHIBIT	X	X	H	-	H
BYTE WRITE	L	H	L	Din	L
BYTE ERASE	Automatic Before Each "Write"				

Note 1: Open Drain Output

READ MODE

The 28CP64 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and is used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is available at the outputs tOE after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least tACC-tOE.

STANDBY MODE

The 28CP64 has a standby mode which reduces the active power dissipation by 300 percent, from 150mW to 1/2mW (values for 0 to 70°C). The 28CP64 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

DATA PROTECTION

In order to insure data integrity, especially during critical power up and power down transitions, the following enhanced data protection circuits are incorporated.

An internal VCC detect (3.8 volts typical) will inhibit the initiation of a non-volatile programming operation when VCC is less than the VCC detect circuit trip. In addition, on power up an internal timer (1mSec) will inhibit the recognition of any program operation. During this period, all normal read functions will be operational. After both the VCC detection and the internal timer have expired, normal programming operation may be exercised.

There is a $\overline{WE}$ lockout circuit that prevents $\overline{WE}$ pulses of less that 20nS duration from initiating a write cycle.

Holding $\overline{WE}$ or $\overline{CE}$ high, or $\overline{OE}$ low, inhibits a write cycle during power-on and power-off (VCC).

WRITE MODE

The 28CP64 has a write cycle that is similar to that of a Static RAM. The write cycle is completely self-timed and initiated by a low going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$, the address information is latched. On the rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched. The Ready/$\overline{Busy}$ pin (pin 1) goes to a logic low level indicating that the 28CP64 is in a write cycle which signals the microprocessor host that the system bus is free for other activity. When Ready/$\overline{Busy}$ goes back to a high, the 28CP64 has completed writing and is ready to accept another cycle.

AUTOMATIC PAGE WRITE

The Page Write feature of the 28CP64 allows 1 to 32 bytes of data to be written into the E^2Prom in a single write cycle. Following a byte write signal to the E^2Prom, the user has 100uSec to write 0 to 31 additional bytes of data into the E^2Prom providing that the byte addresses are on the same 32 byte page in memory. A page is defined by address A5 thru A12 (held constant). The 1 to 32 bytes to be written must be loaded within the first 100uSec after initiating the write of the first byte. All subsequent writes during the page load cycle must go into the same page (Address A5 thru A12) as the first byte. The bytes may be written in any order.

$\overline{DATA}$ POLLING

The 28CP64 features $\overline{Data}$ Polling to signal the completion of a byte or page write cycle. During a write cycle, an attempted read of the last byte written results in the data compliment of that byte at I/O_7. After completion of the write cycle, true data is available. $\overline{Data}$ polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

OPTIONAL CHIP ERASE (Write)

All data may be written to "1"'s (erased) in a chip erase cycle by raising $\overline{OE}$ to 12 volts and bringing the $\overline{WE}$ low.

All "0"'s condition may be obtained by raising both $\overline{CE}$ and $\overline{OE}$ to 12 volts and then bringing $\overline{WE}$ low.

RETENTION/ENDURANCE

Read retention for data written into the 28CP64 is greater than 10 years, with up to 10^5 write cycles. There is no limit to the number of times data may be read.

PRODUCT AVAILABILITY BY TEMPERATURE RANGE

Temperature Range	28CP64-05	28CP64-10	28CP64-15
0°C - +70°C	✓	✓	✓
-40°C - +85°C	Note 1	✓	✓
-55°C - +125°C		✓	✓

Note 1: Tacc max 75nS

Absolute Maximum Ratings*

Temperature Under Bias	-10°C to +80°C
Storage Temperature	-65°C to +125°C
All Input Voltages with Respect to Ground	+6.25V to -0.6V
All Output Voltages with Respect to Ground	VCC+.6V to -.6V
Voltage on Pin 22 with Respect to Ground	+13.5V to -0.6V

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

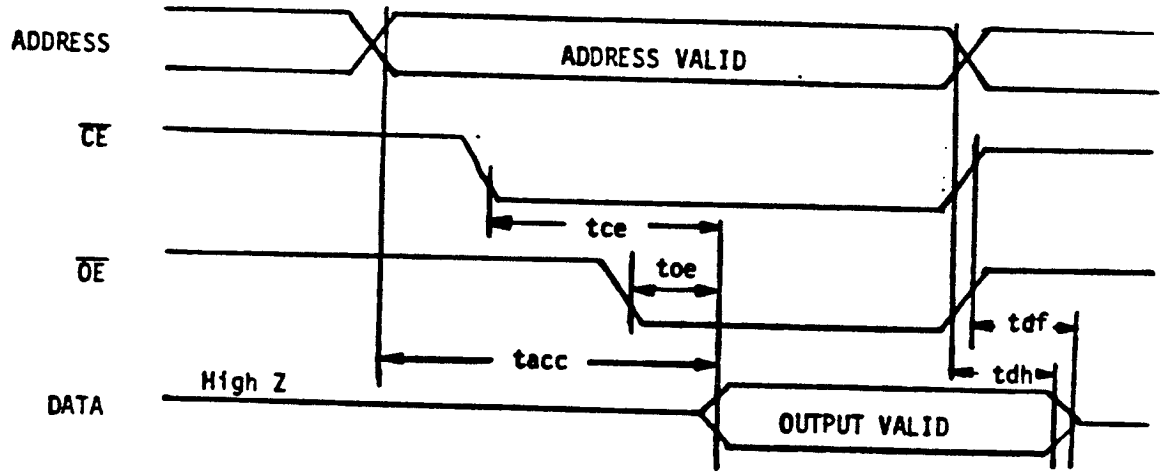
TA = 0°C to 70°C, VCC = 5V±10%, unless otherwise specified.

Symbol	Parameter	Min	Max	Units	Conditions
ILI	Input Leakage Current		10	uA	-.1 to VCC + 1
ILO	Output Leakage Current		10	uA	-.1 to VCC + .1
ICC1	VCC Current Standby		100	uA	$\overline{CE}$=VCC+1 to VCC-.3
			1	mA	$\overline{CE}$=VIH
ICC2	VCC Current Active		50	mA	T=200nS
VIL	Input Low Voltge	-.1	+.8	V	
VIH	Input High Voltage	2.0	VCC+1V		
VOL	Output Low Voltage		.40	V	IOL=2.1mA
VOH	Output High Voltage	2.4		V	IOH=-400uA
VLKO	VCC Lockout Level for Data Protection	3.5	4.25	V	

AC ELECTRICAL CHARACTERISTICS

Read Cycle 28CP64

Symbol	Parameter	28CP64-05 Min	28CP64-05 Max	28CP64-10 Min	28CP64-10 Max	28CP64-15 Min	28CP64-15 Max	Units	Test Conditions
tACC	Address to Output Delay		50		100		150	nS	$\overline{CE}=\overline{OE}=VIL$
tCE	$\overline{CE}$ to Output Delay	50		100		150		nS	$\overline{OE}=VIL$
tAA	Address Access		50		100		150	nS	$\overline{CE}=\overline{OE}=VIL$
tOE	$\overline{OE}$ to Output Delay	10	35	10	50	10	70	nS	$\overline{CE}=VIL$
tDF	$\overline{OE}$ High to Output Float	0	35	0	45	0	50	nS	$\overline{CE}=VIL$
tDH	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first	0		0		0		nS	$\overline{CE}=\overline{OE}=VIL$

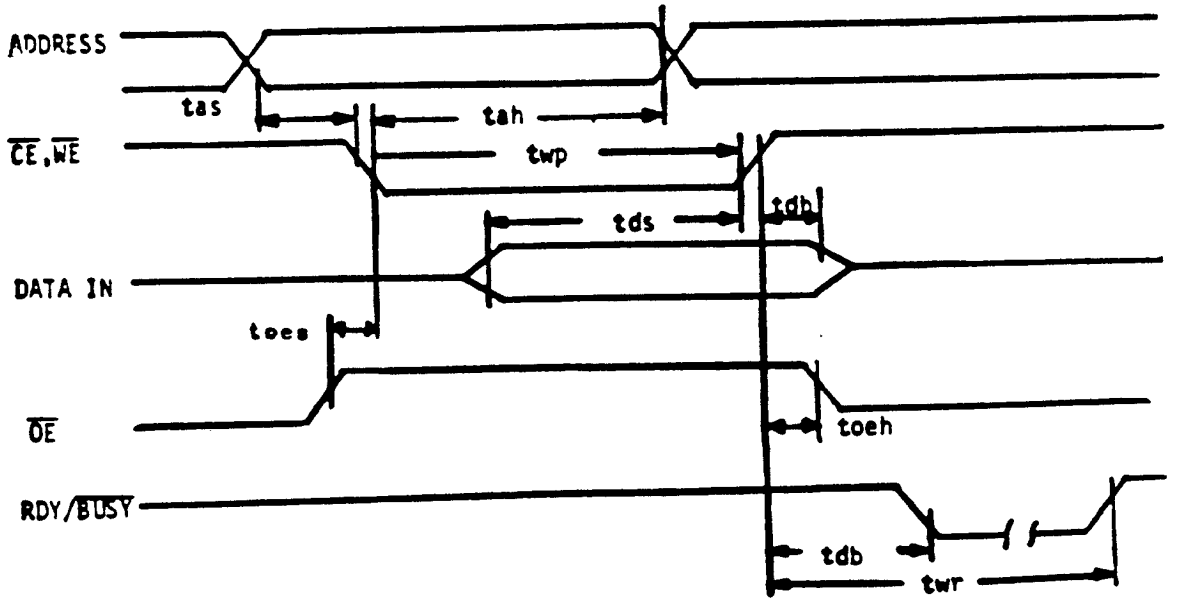


NOTES:
1. This parameter is only sampled and is not 100% tested.
2. $\overline{OE}$ may be delayed up to tACC-tOE after the falling edge of $\overline{CE}$ without impact on tACC.
3. tDF is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

AC ELECTRICAL CHARACTERISTICS -Continued

BYTE Write Cycle 28CP64

Symbol	Parameter	Min	Typ	Max	Units	Notes
tAS	Address, Setup Time	0			nS	
tAH	Address, OE Hold	50			nS	
tWP	Write Pulse Width	100			nS	
tDS	Data Setup Time	50			nS	
tDH	Data Hold Time	0			nS	
tDB	Time to Device Busy			50	nS	
tWR	Write Cycle Time			1	mSec	
tOEH	$\overline{OE}$ Hold Time	20			nS	
tOES	$\overline{OE}$ Setup Time	20			nS	

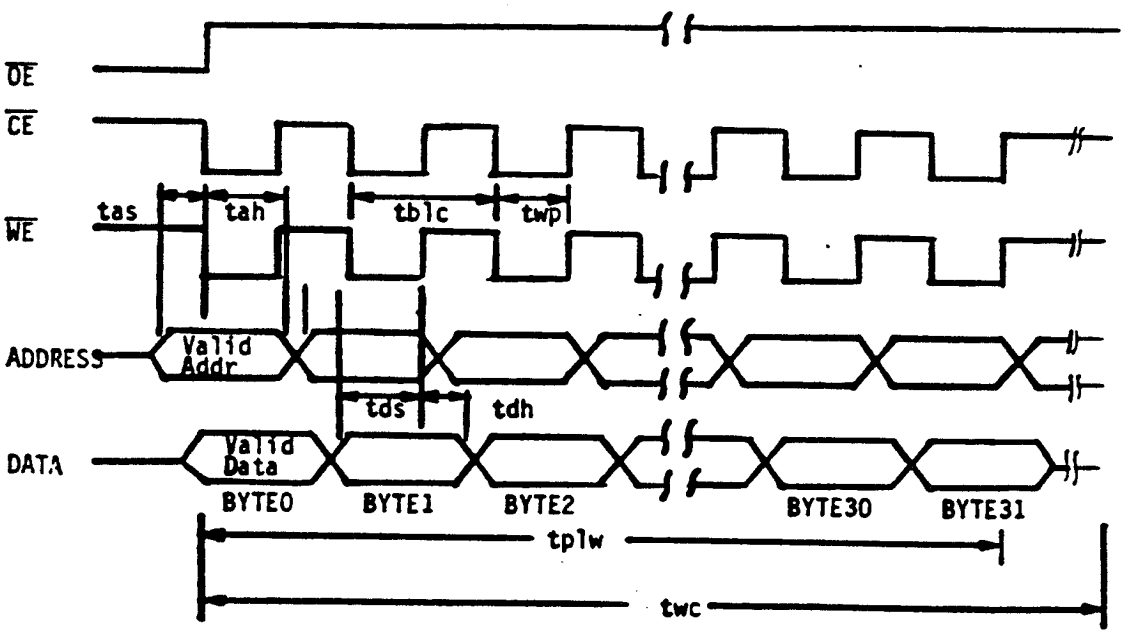


AC ELECTRICAL CHARACTERISTICS - Continued

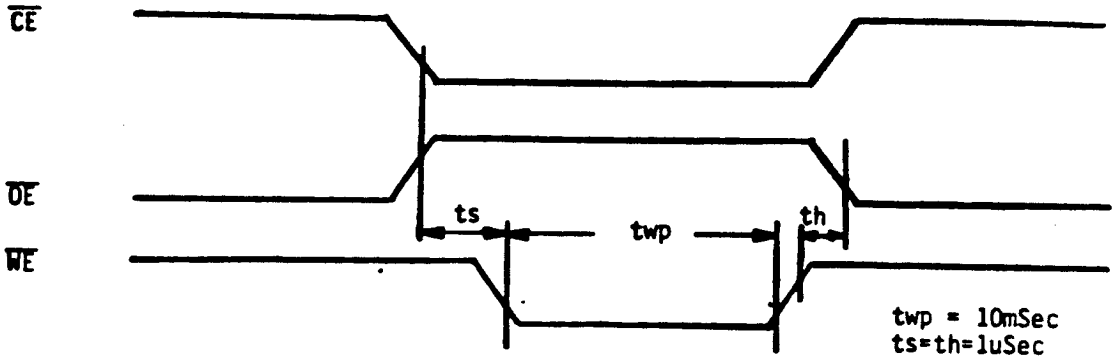
Page Mode Write

TA = 0°C to 70°C, VCC = +5V ± 10% (unless otherwise specified)

Symbol	Parameter	Min	Max	Units
tWC	Write Cycle Time		2.0	mS
tAS	Address Setup	10		nS
tAH	Address Hold	50		nS
tDS	Data Setup	50		nS
tDH	Data Hold	0		nS
tWP	Write Pulse Width	100		nS
tWH	$\overline{WE}$ Hold	100		nS
tBLC	Byte Load Cycle			
tPLW	Page Load Width		100	



CHIP ERASE (WRITE)



SUPPLEMENTARY CONTROL FUNCTIONS

Mode	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{WE}$ (27)	Ai	VCC	Di - Oi (11-13,15-19)
Chip Erase	VIL	VH		X	VCC	
Extra Row Read	VIL	VIL	VIH	A9=VH	VCC	DOUT
Extra Row Write		VIH		A9=VH	VCC	DIN

VH = 12.0 ± .5 volts