Am79486

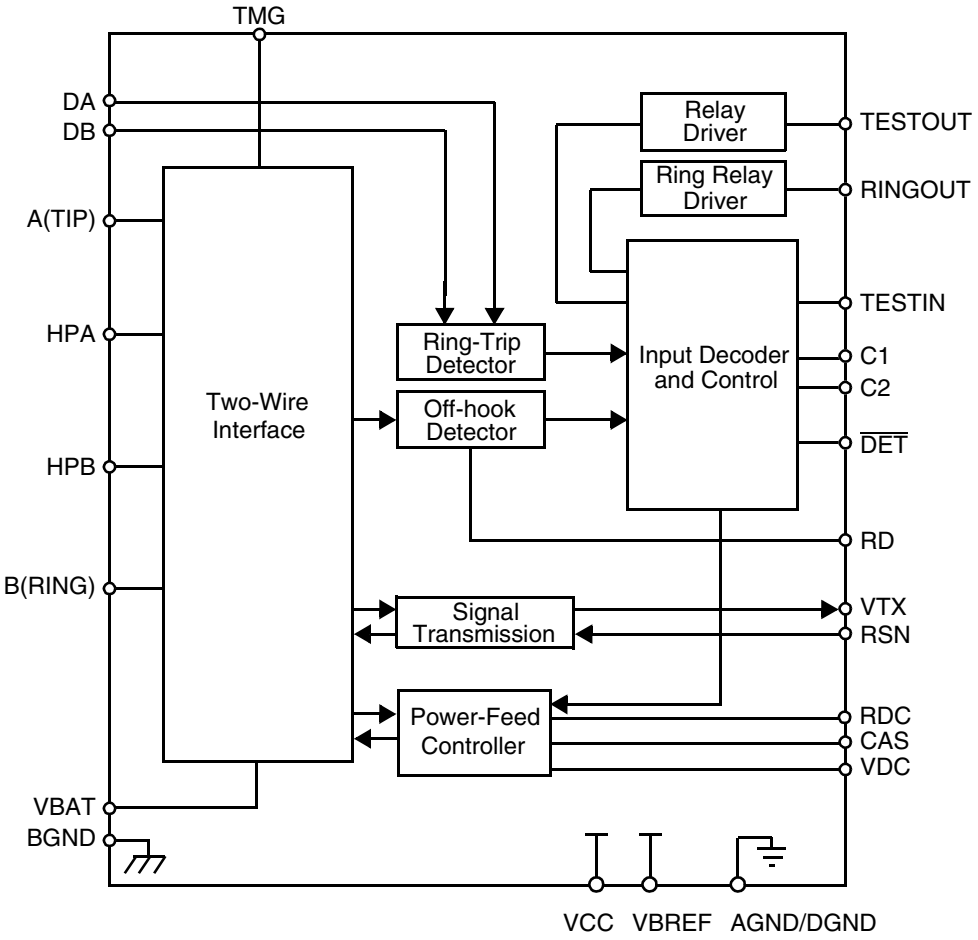
Subscriber Line Interface Circuit

The Am79486 Subscriber Line Interface Circuit implements the basic telephone line interface functions and enables the design of low cost, high performance POTS line interface cards.

DISTINCTIVE CHARACTERISTICS

- **Control states: Active, Ringing, Standby and Disconnect**
- **Low standby power**
- **–19 V to –58 V battery operation**
- **On-hook transmission**
- **Two-wire impedance set by single external impedance**
- **Programmable constant-current feed**
- **Programmable loop-detect threshold**
- **Programmable ring-trip detect threshold**
- **No –5 V supply required**
- **Current Gain = 500**
- **On-chip Thermal Management (TMG) feature**
- **Two on-chip relay drivers with relay snubbers**

BLOCK DIAGRAM



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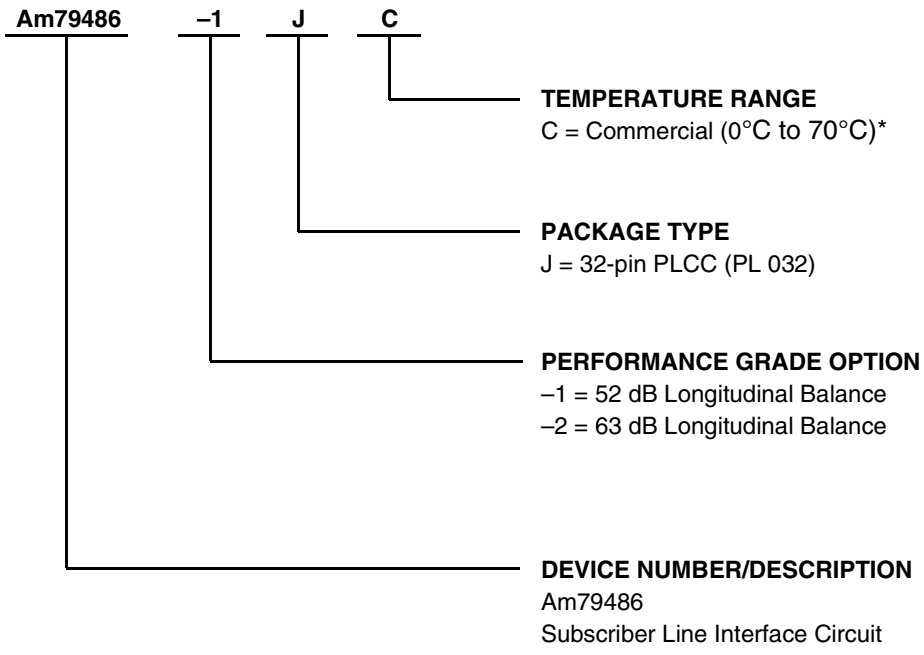
ORDERING INFORMATION

Standard Products

Legerity standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations		
Am79486	–1 –2	JC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Legerity sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on Legerity's standard military grade products.

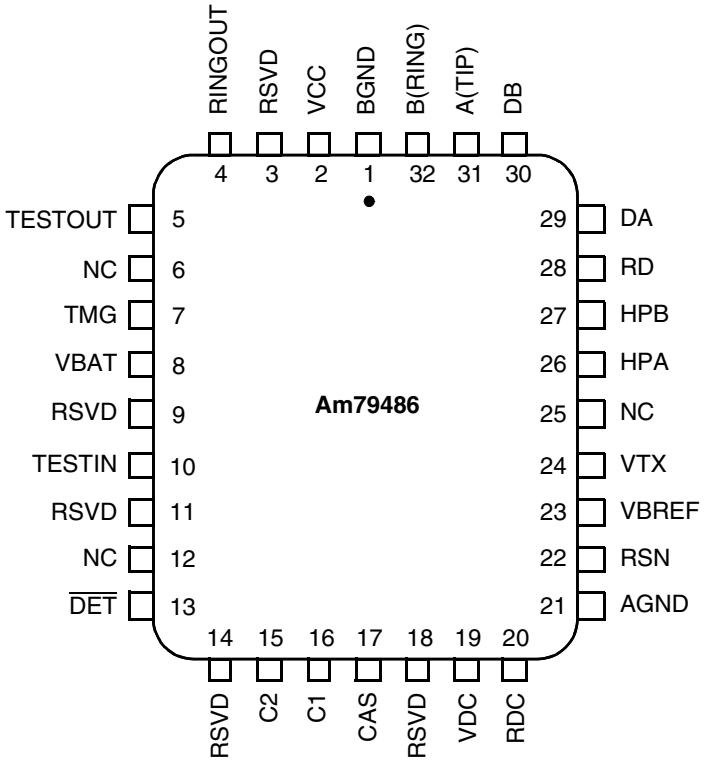
Note:

** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –25°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

CONNECTION DIAGRAM

Top View

32-Pin PLCC



Notes:

1. *Pin 1 is marked for orientation.*
2. *NC = No Connect*
3. *RSVD = Reserved. Do not connect to these pins.*

PIN DESCRIPTIONS

Pin Names	Type	Description
AGND/DGND	Gnd	Analog and Digital ground.
A(TIP)	Output	Output of A(TIP) power amplifier.
BGND	Gnd	Battery (power) ground.
B(RING)	Output	Output of B(RING) power amplifier.
C2–C1	Inputs	Decoder. SLIC control pins. C2 is MSB and C1 is LSB. TTL compatible with internal current source pullups.
CAS	Capacitor	Anti-Saturation pin for capacitor to filter reference voltage when operating in anti-saturation region.
DA	Input	Ring-Trip negative. Negative input to ring-trip comparator.
DB	Input	Ring-Trip positive. Positive input to ring-trip comparator.
DET	Output	Switchhook Detector. A logic Low indicates that selected condition is detected. The detect condition is selected by the logic inputs (C1 and C2). The output is open-collector with a built-in 15 kΩ pull-up resistor.
HPA	Capacitor	High-Pass Filter Capacitor. A(TIP) side of high-pass filter capacitor.
HPB	Capacitor	High-Pass Filter Capacitor. B(RING) side of high-pass filter capacitor.
NC	—	No connect. Pin not internally connected.
RD	Resistor	Detect resistor. Detector threshold set and filter pin.
RDC	Resistor	DC feed resistor. Connection point for the DC feed current programming network. The other end of the network connects to the receiver summing node (RSN).
RINGOUT	Output	Ring Relay Driver. Open collector driver with emitter internally connected to BGND.
RSN	Input	Receive Summing Node. The metallic current (both AC and DC) between A(TIP) and B(RING) is equal to 500 times the current into this pin. The networks which program receive gain, two-wire impedance and feed resistance all connect to this node.
RSVD	—	These pins are reserved for Legerity use. No connection should be made to these pins.
TESTIN	Input	Relay driver control. A logic low at TESTIN forces TESTOUT low. TTL compatible with internal current source pullups.
TESTOUT	Output	Relay driver. Open collector driver with emitter internally connected to BGND.
TMG	—	Thermal management. External resistor connects between this pin and VBAT to offload power from SLIC.
VBAT	Battery	Battery supply and connection to substrate.
VBREF	—	This is a Legerity reserved pin and always must be connected to the VBAT pin.
VCC	Power	+5 V power supply.
VDC	Output	Voltage output at this pin is proportional to the voltage across pins A and B (V_{AB}).
VTX	Output	Transmit audio. This output is a 0.50 gain version of the A(TIP) and B(RING) metallic voltage. VTX also sources the two-wire input impedance programming network.

ABSOLUTE MAXIMUM RATINGS

Storage temperature . . . . . –55°C to +150°C

V_{CC} with respect to AGND/DGND . . . . –0.4 V to +7 V

V_{BAT} with respect to AGND/DGND:

Continuous . . . . . +0.4 V to –70 V
10 ms . . . . . +0.4 V to –75 V

BGND with respect to AGND/DGND . . . .+3 V to –3 V

A(TIP) or B(RING) to BGND:

Continuous . . . . . V_{BAT} to +1 V
10 ms (f = 0.1 Hz) . . . . . –70 V to +5 V
1 µs (f = 0.1 Hz) . . . . . –80 V to +8 V
250 ns (f = 0.1 Hz) . . . . . –90 V to +12 V

Current from A(TIP) or B(RING). . . . . ±150 mA

RINGOUT current . . . . . 50 mA

TESTOUT current . . . . . 100 mA

RINGOUT/TESTOUT voltage . . . . . BGND to +7 V

RINGOUT/TESTOUT transient . . . . . BGND to +10 V

DA and DB inputs

Voltage on ring-trip inputs . . . . . V_{BAT} to 0 V
Current into ring-trip inputs . . . . . ±10 mA

C2–C1, TESTIN

Input voltage . . . . . –0.4 V to V_{CC} + 0.4 V

Maximum power dissipation, continuous,

T_A = 70°C, No heat sink (See note):

In 32-pin PLCC package. . . . . 1.7 W

Thermal Data: . . . . . θ_{JA}

In 32-pin PLCC package. . . . . .43°C/W typ

ESD immunity/pin (HBM) . . . . . 1500 V

Note: *Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never see this temperature and operation above 145°C junction temperature may degrade device reliability. See the SLIC Packaging Considerations for more information.*

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient temperature . . . . . 0°C to +70°C*

V_{CC} . . . . . 4.75 V to 5.25 V

V_{BAT} . . . . . –19 V to –58 V

AGND/DGND . . . . . 0 V

BGND with respect to
AGND/DGND. . . . . –100 mV to +100 mV

Load resistance on VTX to ground . . . . . 20 kΩ min

The operating ranges define those limits between which the functionality of the device is guaranteed.

** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –25°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

ELECTRICAL CHARACTERISTICS

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Transmission Performance						
2-wire return loss	200 Hz to 3.4 kHz	18	36		dB	1, 4
Analog output (V_{TX}) impedance			3	20	Ω	4
Analog (V_{TX}) output offset voltage	0°C to +70°C –25°C to +85°C	–40 –50		+40 +50	mV	— 4
Overload level, 2 wire and 4 wire	Active state	2.5			Vpk	2a
Overload level	On hook, R_{LAC} = 900 Ω	1.5			Vrms	2b
THD, Total Harmonic Distortion	0 dBm +7 dBm		–64 –55	–50 –40	dB	5
THD, on hook	+3 dBm, R_{LAC} = 900 Ω			–36		
Longitudinal Capability (See Test Circuit D)						
Longitudinal to metallic L-T, L-4 balance	200 Hz to 1 kHz					
	0°C to +70°C –1*	53			dB	
	0°C to +70°C –2	63				
	–25°C to +85°C –1	50				4
	–25°C to +85°C –2	58				
	1 kHz to 3.4 kHz					
	0°C to +70°C –1*	53			dB	
	0°C to +70°C –2	58				
	–25°C to +85°C –1	50				
	–25°C to +85°C –2	53				
Longitudinal current per pin (A or B)	Active state	8.5	27		mArms	7
Longitudinal impedance at A or B	0 to 100 Hz		25	35	Ω/pin	
Idle Channel Noise						
C-message weighted noise	R_L = 600 Ω 0°C to +70°C R_L = 600 Ω –25°C to +85°C		+7	+11 +13	dBrnC	4
Insertion Loss and Balance Return Signal (See Test Circuits A and B)						
Gain accuracy 4- to 2-wire	0 dBm, 1 kHz 0°C to +70°C –25°C to 85°C	–0.15 –0.20	0 0	+0.15 +0.20	dB	4
Gain accuracy 2- to 4-wire, 4- to 4-wire	0 dBm, 1 kHz 0°C to +70°C –25°C to 85°C	–6.17 –6.22	–6.02 –6.02	–5.87 –5.82		4
Gain accuracy, 4- to 2-wire	On hook, R_{LAC} = 900 Ω	–0.35		+0.35		4
Gain accuracy, 2- to 4-wire, 4- to 4-wire	On hook, R_{LAC} = 900 Ω	–6.37	–6.02	–5.67		
Gain accuracy over frequency	300 Hz to 3400 Hz 0°C to +70°C relative to 1 kHz –25°C to +85°C	–0.10 –0.15		+0.10 +0.15		4
Gain tracking	+3 dBm to –55 dBm 0°C to +70°C relative to 0 dBm –25°C to +85°C	–0.10 –0.15		+0.10 +0.15		4

Note:
** Performance Grade*

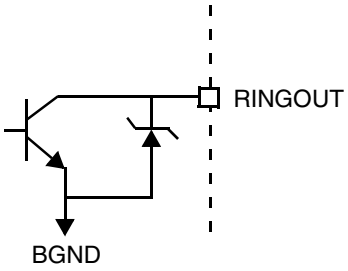
ELECTRICAL CHARACTERISTICS (continued)

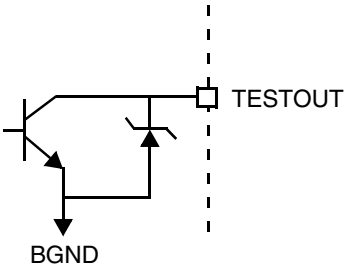
Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Gain tracking On hook, R_{LAC} = 900 Ω	0 dBm to –37 dBm 0°C to +70°C –25°C to +85°C +3 dBm to 0 dBm	–0.10 –0.15 –0.35		+0.10 +0.15 +0.35	dB	— 4 —
Group delay	0 dBm, 1 kHz		4		µs	4, 7
Line Characteristics						
I_L, short loops, Active state	R_{LDC} = 900 Ω	20	23	26	mA	
I_L, long loops, Active state	R_{LDC} = 1600 Ω, BAT = –42.75 V, T_A = 25°C	18	22			
I_L, accuracy, Standby state	$I_L = \frac{\lvert BAT\rvert - 3\ V}{R_L + 400}$ T_A = 25°C	0.7I_L	I_L	1.3I_L		
	Constant-current region	18	30			
I_L, loop current, Disconnect state	R_L = 0			100	µA	
I_LLIM	Active, A and B to GND		80	120	mA	
VDC accuracy	R_L = 300 Ω R_L = 900 Ω	0.300 0.920	0.350 1.050	0.400 1.18	V	
V_{AB}, Open Circuit voltage	V_{BAT} = –52 V	–42.75	–46			
Power Supply Rejection Ratio (V_{RIPPLE} = 100 mVrms), Active Normal State						
V_{CC}	50 Hz to 3400 Hz 500 Hz to 3000 Hz	30 35	50		dB	5
V_{BAT}	50 Hz to 3400 Hz 500 Hz to 3000 Hz	28 40	50			
V_{CC}, on hook	50 Hz to 3400 Hz	30	50			
V_{BAT}, on hook	50 Hz to 100 Hz 100 Hz to 200 Hz 200 Hz to 300 Hz 300 Hz to 500 Hz 500 Hz to 1000 Hz 1 kHz to 3400 Hz	4 9 16 24 30 34	8 14 24 28 34 40			4
Control pin feed-through (C2–C1)	50 Hz to 3400 Hz	35	50			
Effective internal resistance	CAS pin to V_{BAT}	85	170	255	kΩ	
Power Dissipation						
On hook, Disconnect state			45	70	mW	
On hook, Standby state			55	85		
On hook, Active state	R_{TMG} = 2500 Ω		150	270		
Off hook, Standby state	R_L = 600 Ω		860	1200		
Off hook, Active state	R_L = 300 Ω, R_{TMG} = 2500 Ω		700	950		
Supply Currents, Battery = –48 V						
ICC, On-hook V_{CC} supply current	Disconnect state Standby state Active state		3.0 2.8 6.3	4.0 4.0 8.5	mA	
IBAT, On-hook V_{BAT} supply current	Disconnect state Standby state Active state		0.6 0.8 2.8	1.0 1.5 4.8		
RFI Rejection						
RFI rejection	100 kHz to 30 MHz, (See Figure F)			1.0	mVrms	4

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Receive Summing Node (RSN)						
RSN DC voltage	I_{RSN} = 0 mA		0		V	4
RSN impedance	200 Hz to 3.4 kHz		10	20	Ω	
Logic Inputs (C2–C1, TESTIN)						
V_{IH}, input High voltage		2.0			V	
V_{IL}, input Low voltage				0.8		
I_{IH}, input High current		–75		40	µA	
I_{IL}, input Low current		–400		–13		
Logic Output ($\overline{DET}$)						
V_{OL}, output Low voltage	Iout = 0.3 mA, 15 kΩ to V_{CC}			0.40	V	
V_{OH}, output High voltage	Iout = –0.1 mA, 15 kΩ to V_{CC} Iout = –10 µA	2.4 0.7•V_{CC}	 0.97•V_{CC}			
Ring-Trip Detector Input (DA, DB)						
Bias current		–20	–5		nA	4
Offset voltage	Source resistance = 2 MΩ	–50	0	+50	mV	6
Offset voltage	Source resistance mismatch = 3 MΩ	–50	0	+50		4
Relay Driver Output (RINGOUT, TESTOUT)						
V_{OH}, On voltage, RINGOUT	I_{OL} = 40 mA		+0.3	+0.7	V	
V_{OH}, On voltage, TESTOUT	I_{OL} = 80 mA		+0.4	+1.0		
I_{OL}, Off leakage, RINGOUT	V_{OH} = +5 V		0	100	µA	
I_{OL}, Off leakage, TESTOUT	V_{OH} = +5 V	80	140	200		
Zener breakover	I_Z = 300 µA	5.7	7.2		V	
Zener On voltage, RINGOUT	I_Z = 30 mA		8			
Zener On voltage, TESTOUT	I_Z = 80 mA		8			
Loop Detector						
R_{LTH}, loop-detect threshold resistance	Active state, R_D = 35.4 kΩ Standby state, R_D = 35.4 kΩ	RD/11.5 RD/15	RD/10.1 RD/12.6	RD/8.8 RD/10	Ω	8

RELAY DRIVER SCHEMATICS





Notes:

1. *Unless otherwise noted, test conditions are BAT = –52 V, V_{CC} = +5 V, R_L = 900 Ω, R_T = 225 kΩ, RRX = 225 kΩ, $R_{DC1} = R_{DC2}$ = 27.17 kΩ, R_{TMG} = 2500 Ω, RD = 35.4 kΩ, no fuse resistors, CHP = 0.1 µF, C_{DC} = 0.1 µF, C_{CAS} = 0.1 µF, D1 = 1N400x, BSWEN = logic low (0), (two-wire AC input impedance is a 900 Ω).*
2. *a. Overload level is defined when THD = 1%.*
   b. Overload level is defined when THD = 1.5%.
3. *Balance return signal is the signal generated at V_{TX} by V_{RX}. This specification assumes that the two-wire AC load impedance matches the programmed impedance.*
4. *Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.*
5. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*
6. *Tested with 0 Ω source impedance. 2 MΩ is specified for system design only.*
7. *Minimum current level guaranteed not to cause a false Loop Detect.*
8. *$\overline{DET}$ goes high during loss of V_{BAT} supply.*

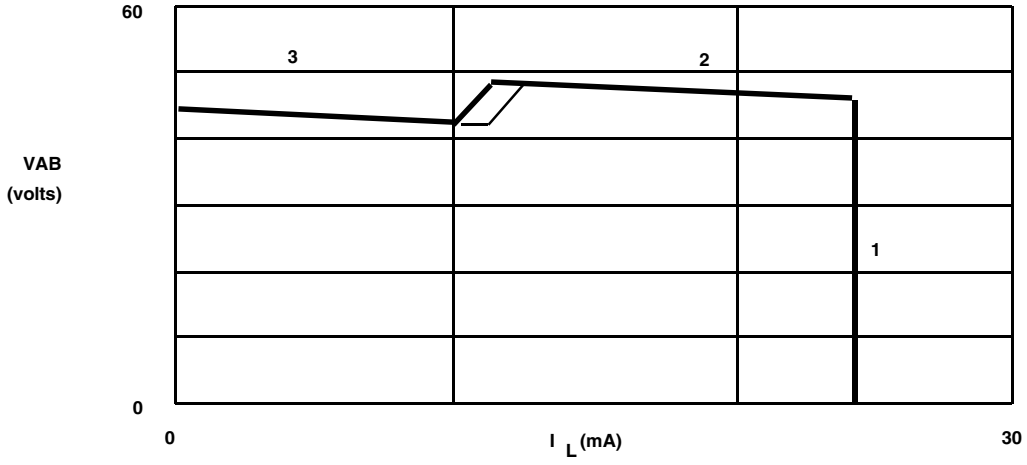
Table 1. SLIC Decoding

State	C2	C1	2-Wire Status	$\overline{DET}$ Output
0	0	0	Disconnect	Ring trip
1	0	1	Ringing	Ring trip
2	1	0	Active	Loop detector
3	1	1	Standby	Loop detector

Table 2. User-Programmable Components

$Z_T = 250(Z_{2WIN} - 2R_F)$	Z_T is connected between the VTX and RSN pins. The fuse resistors are R_F, and Z_{2WIN} is the desired 2-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.
$Z_{RX} = \frac{Z_L}{G_{42L}} \bullet \frac{500 \bullet Z_T}{Z_T + 250(Z_L + 2R_F)}$	Z_{RX} is connected from V_{RX} to R_{SN}. Z_T is defined above, and G_{42L} is the desired receive gain.
$R_{DC1} + R_{DC2} = \frac{1250}{I_{LOOP}}$ $C_{DC} = 1.5\ ms \bullet \frac{R_{DC1} + R_{DC2}}{R_{DC1} \bullet R_{DC2}}$	R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the RDC pin. R_{DC1} and R_{DC2} are approximately equal. I_{LOOP} is the desired loop current in the constant-current region.
$RD_{ACTIVE} = 10.1 \bullet R_{LTH}$ for $\lvert V_{BAT}\rvert > 40$ V $RD_{STANDBY} = 10(R_{LTH} + 400) \bullet \frac{54\ V}{BAT - 3}$ $RD_{ACTIVE} = \frac{375}{I_{DET}}$ for $\lvert V_{BAT}\rvert < 40$ V $RD_{STANDBY} = \frac{375}{I_{DET}}$	R_{LTH} is the desired loop resistance detect threshold. I_{LTH} is the loop current at R_{LTH} for a given battery.
$C_{CAS} = \frac{1}{3.4 \bullet 10^5 \pi f_c}$	C_{CAS} is the regulator filter capacitor and f_c is the desired filter cut-off frequency.
$I_{STANDBY} = \frac{V_{BAT} - 3\ V}{400\ \Omega + R_L}$	Standby loop current (resistive region).
VDC Scale Factor = $\frac{63.4 \bullet R_L}{R_{DC1} + R_{DC2}}$	VDC Scale Factor valid for constant-current region.
Thermal Management Equations (Normal Active and Tip Open States)	
$R_{TMG} \geq \frac{\lvert V_{BAT}\rvert - 6\ V}{I_{LOOP}} - 70\ \Omega$	R_{TMG} is connected from T_{MG} to V_{BAT} and is used to limit power dissipation within the SLIC in Active and Disconnect states only.
$P_{RTMG} = \frac{(\lvert V_{BAT}\rvert - 6\ V - (I_L \bullet R_L))^2}{(R_{TMG} + 70\ \Omega)^2} \bullet R_{TMG}$	Power dissipated in the thermal management resistor, R_{TMG}, during Active and Disconnect states.
$P_{SLIC} = \lvert V_{BAT}\rvert \bullet I_L - P_{RTMG} - R_L(I_L)^2 + 0.12\ W$	Power dissipated in the SLIC while in Active and Disconnect states.

DC FEED CHARACTERISTICS



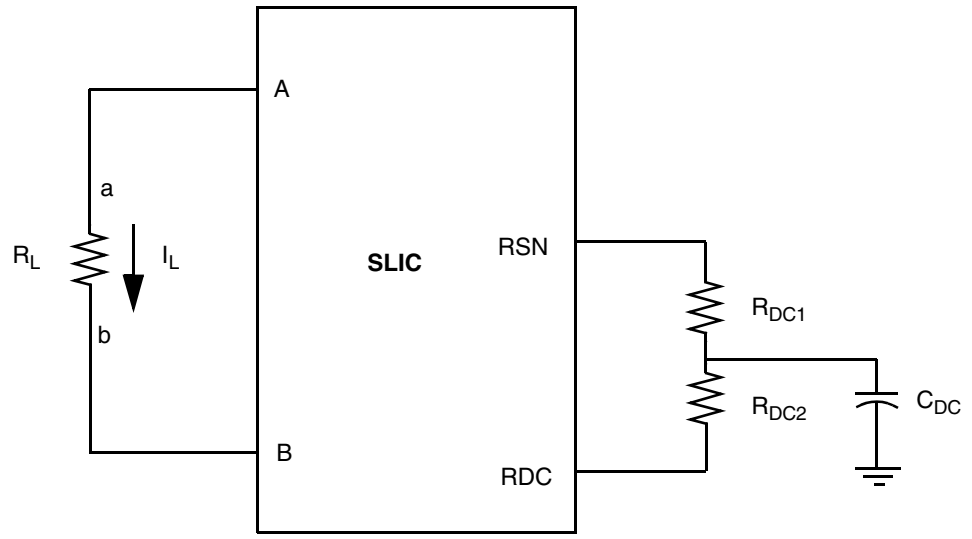
$R_{DC} = R_{DC1} + R_{DC2} = 54.34\ k\Omega$
BAT = –48 V

1. $V_{AB} = I_L R_L' = \frac{1250}{RDC} R_L'$, *where* $R_L' = R_L + 2R_F$

2. $V_{AB} = |V_{BAT}| - 3.3 - I_L \frac{RDC}{300}$

3. $V_{AB} = |V_{BAT}| - 5.5 - I_L \frac{RDC}{300}$

a. Load Line (typical)

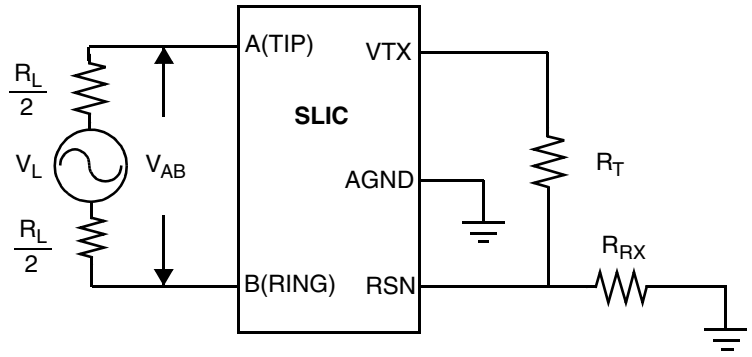


Feed current programmed by R_{DC1} and R_{DC2}

b. Feed Programming

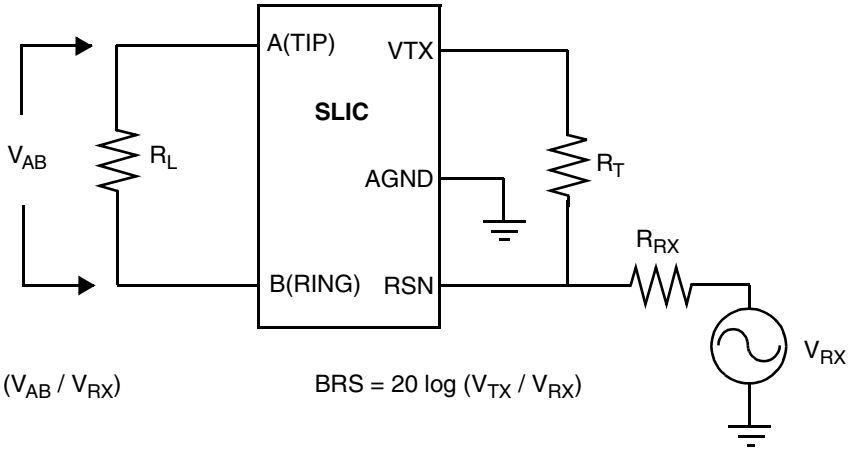
Figure 1. DC Feed Characteristics

TEST CIRCUITS



$I_{L2\text{-}4} = 20 \log (V_{TX} / V_{AB})$

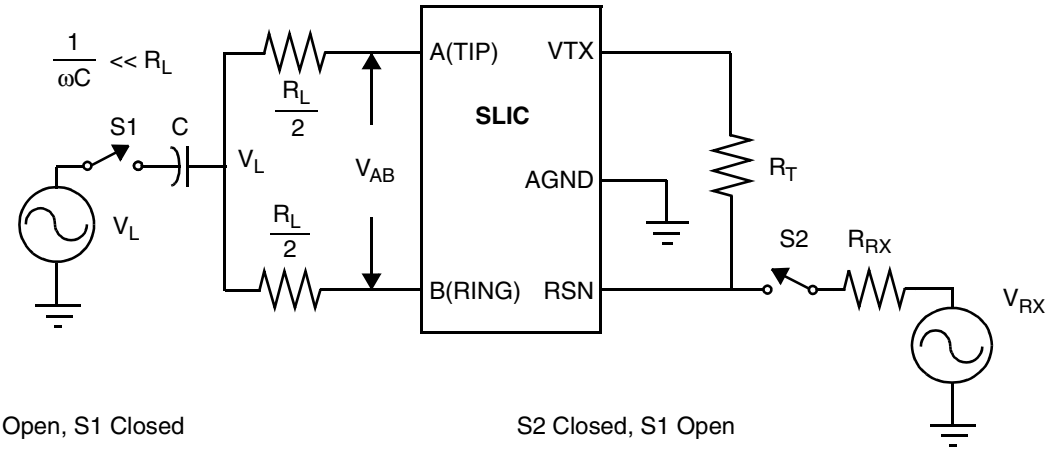
A. Two- to Four-Wire Insertion Loss



$I_{L4\text{-}2} = 20 \log (V_{AB} / V_{RX})$

$BRS = 20 \log (V_{TX} / V_{RX})$

B. Four- to Two-Wire Insertion Loss and Balance Return Signal



S2 Open, S1 Closed

L-T Long. Bal. = 20 log (V_{AB} / V_L)

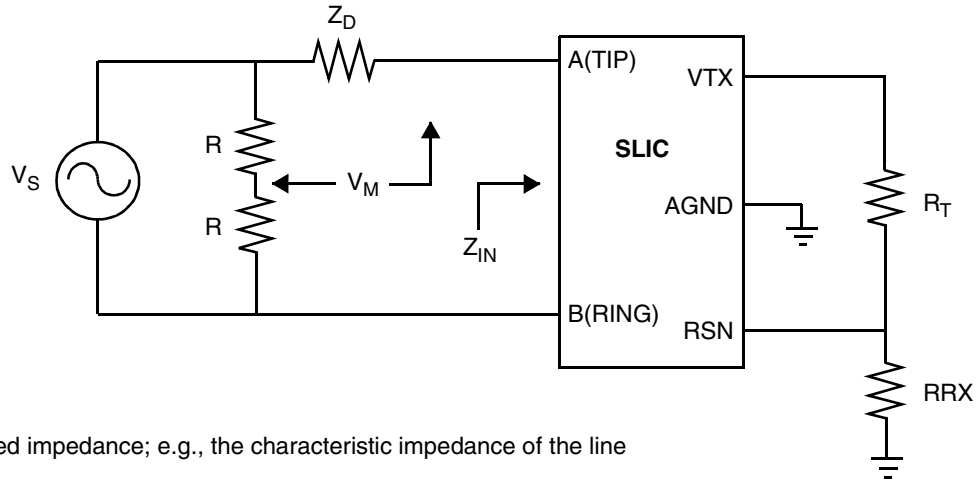
L-4 Long. Bal. = 20 log (V_{TX} / V_L)

S2 Closed, S1 Open

4-L Long. Sig. Gen. = 20 log (V_L / V_{RX})

C. Longitudinal Balance

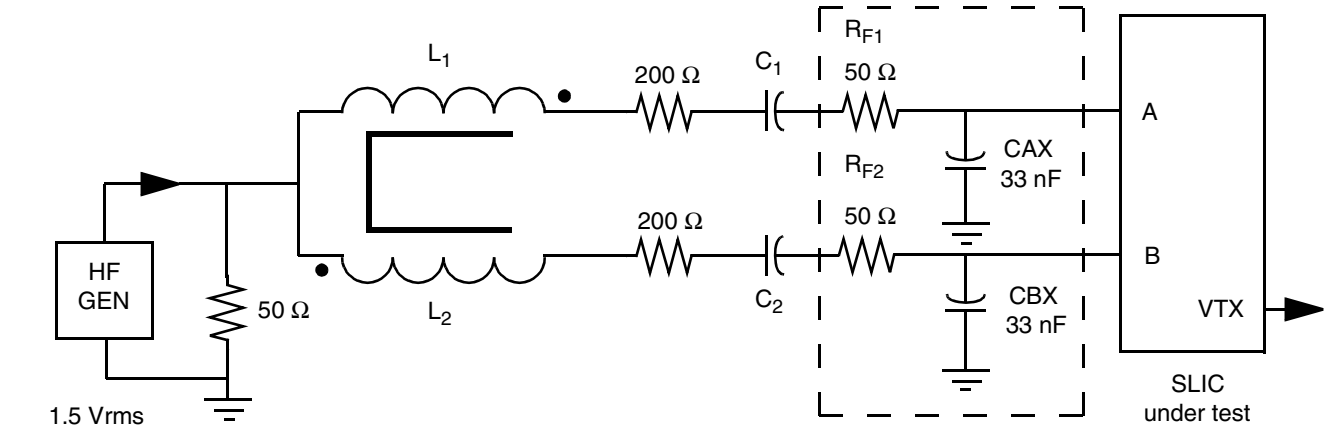
TEST CIRCUITS (continued)



Z_D: The desired impedance; e.g., the characteristic impedance of the line

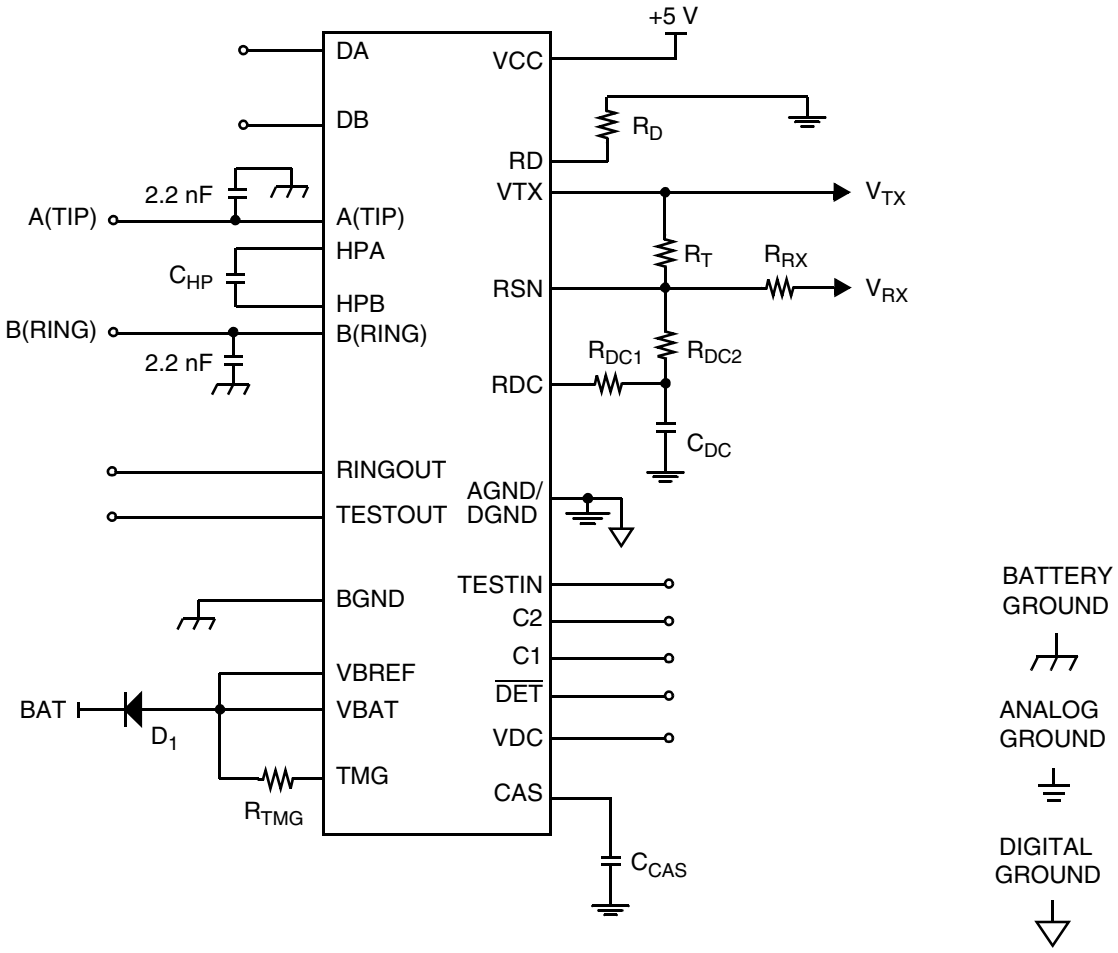
Return loss = –20 log (2 V_M / V_S)

D. Two-Wire Return Loss Test Circuit



E. RFI Test Circuit

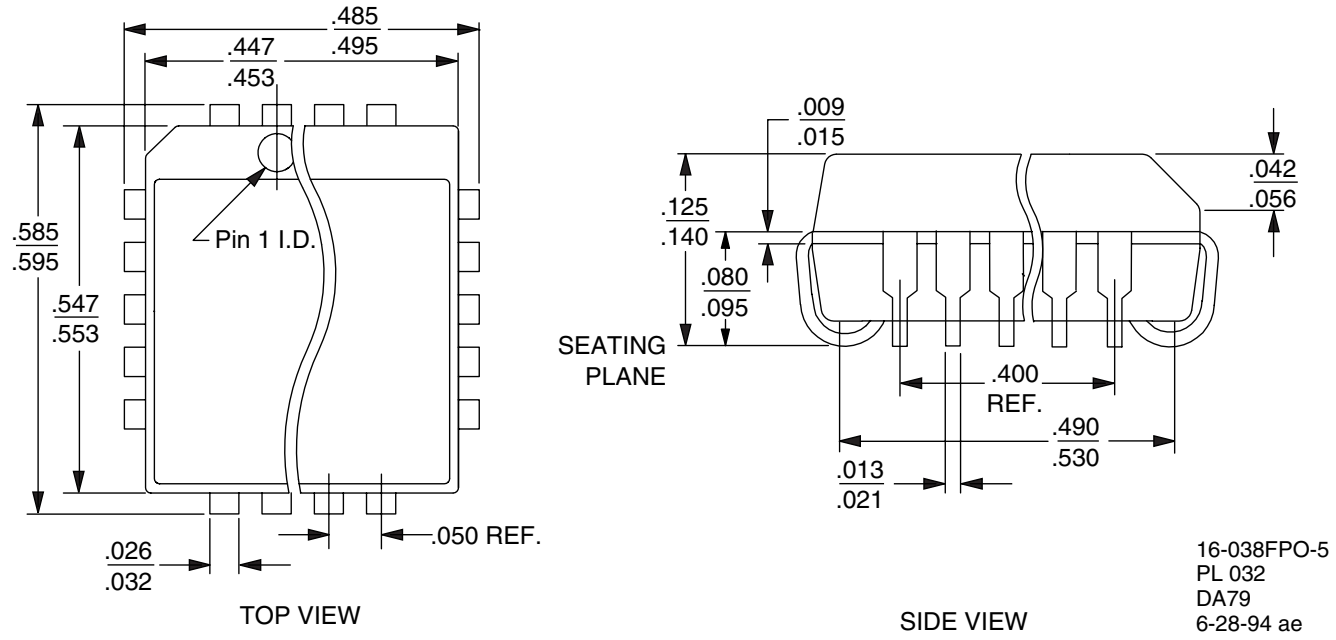
TEST CIRCUITS (continued)



F. Am79486 Test Circuit

PHYSICAL DIMENSIONS

PL032



REVISION SUMMARY

Revision A to Revision B

- Minor changes were made to the data sheet style and format to conform to Legerity standards.
- Absolute Maximum Ratings: Added ESD immunity specification

Revision B to Revision C

- The physical dimensions (PL032) were added to the Physical Dimensions section.
- Updated the Pin Description table to correct inconsistencies.

Notes:

Notes:

Legerity provides silicon solutions that enhance the performance, speeds time-to-market, and lowers the system cost of our customers' products. By combining process, design, systems architecture, and a complete set of software and hardware support tools with unparalleled factory and worldwide field applications support, Legerity ensures its customers enjoy a smoother design experience. It is this commitment to our customers that places Legerity in a class by itself.

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