CML Microcircuits
COMMUNICATION SEMICONDUCTORS

CMX624

V.23 / Bell 202 Modem

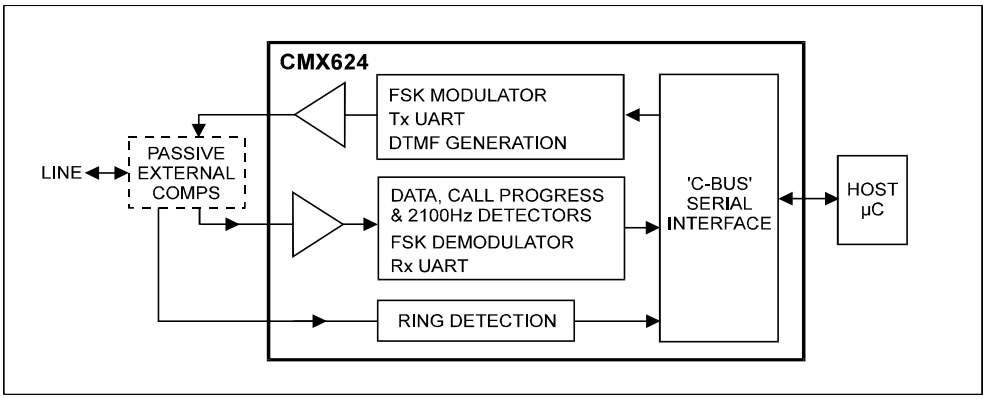
D/624/7 September 2003

Features

- **V.23 / Bell 202 Compatible Modem**
- **Integrated DTMF Encoder**
- **Call Progress Tone Detection**
- **Line Reversal and Ring Detector**
- **Low Power Operation (2.7V)**
- **Part of the CMX6x4 Modem Series**

Applications

- **Telephone Telemetry Systems**
- **Remote Utility Meter Reading**
- **Security Systems/Cash Terminals**
- **Industrial Control Systems**
- **Pay-Phones**
- **Cable TV Set-Top Boxes**



1.1 Brief Description

The CMX624 V.23 / Bell 202 modem is intended for use in any telephone based information and telemetry system with low power requirements. Using FSK signalling, fast call set-up times and robust error resistant transmission can be implemented by efficient low power circuits. The circuit can operate at 1200bps full duplex over a 4-wire circuit or 1200 bps plus low speed data over a 2-wire circuit. Flexible line driver and receive hybrid circuitry are integrated on chip requiring only passive external components to build a 2- or 4-wire interface. A low impedance pull down output is provided for a hook relay.

Control of the device is via a simple high speed serial bus; this allows easy interfacing to a host µController. The data transmitted and received by the modem is also transferred over the same high speed serial bus. On-chip programmable Tx and Rx UARTs allow asynchronous data to be simultaneously encoded and decoded. Either UART may be disabled to allow 8-bit raw data to be received or transmitted. Any repetitive 8-bit data pattern can be sent without the controller having to reload data every 8 bits. All 16 DTMF combinations are available along with a single tone 'melody' mode. The ringing, 2100Hz, call progress and data detectors included on the CMX624 make the set-up of a telephone call a simple matter for the host µController.

In many data collection and telemetry systems low power consumption is important. The CMX624 features a 'Zero Power' standby mode. Whilst in standby the ring detector continues to operate and will supply the host µController with an interrupt when line reversal or ringing is detected. The CMX624 can operate on a supply voltage between 3.0V and 5.5V across the full temperature range of -40°C to +85°C.
The CMX624 is pin compatible with the CMX644A V22 and Bell 212A modem also from CML.

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1.2 Block Diagram

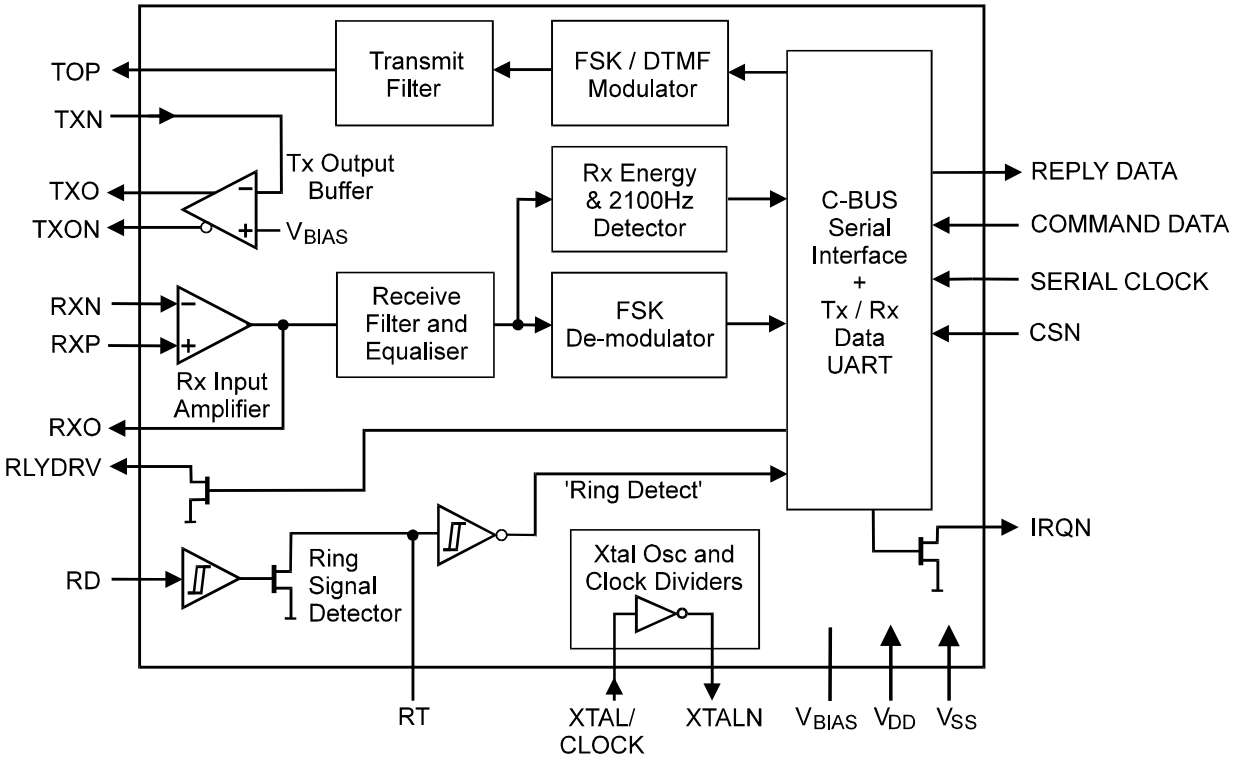


Figure 1 Block Diagram

1.3 Signal List

CMX624 D2/D5/P4	Signal		Description
Pin No.	**Name**	**Type**	
1	XTALN	O/P	The output of the on-chip Xtal oscillator inverter.
2	XTAL/CLOCK	I/P	The input to the oscillator inverter from the Xtal circuit or external clock source.
3	SERIAL CLOCK	I/P	The 'C-BUS' serial clock input from the µC. See Section 1.5.11
4	COMMAND DATA	I/P	The 'C-BUS' serial data input from the µC.
5	REPLY DATA	T/S	A 3-state 'C-BUS' serial data output to the µC. This output is high impedance when not sending data to the µC.
6	CSN	I/P	The 'C-BUS' transfer control input provided by the µC.
7	IRQN	O/P	A 'wire-ORable' output for connection to a µC Interrupt Request input. This output is pulled down to V_{SS} when active and is high impedance when inactive. An external pullup resistor is required.
8	TOP	O/P	The Tx analogue signal output.
9	TXO	O/P	The output of the line driving amplifier.
10	TXN	I/P	The inverting input to the line driver amplifier.
11	TXON	O/P	The inverted output of the line driving amplifier.
12	V_{SS}	Power	The negative supply rail (ground).
13	V_{BIAS}	O/P	Internally generated bias voltage of $V_{DD}/2$, except when the device is in 'Zero Power' mode when V_{BIAS} will discharge to V_{SS}. Should be decoupled to V_{SS} by a capacitor mounted close to the device pins.
14	RLYDRV	O/P	Relay drive open drain output. This output is pulled down to V_{SS} when active and is high impedance when inactive.
15	RXP	I/P	The non-inverting input to the Rx input amplifier.

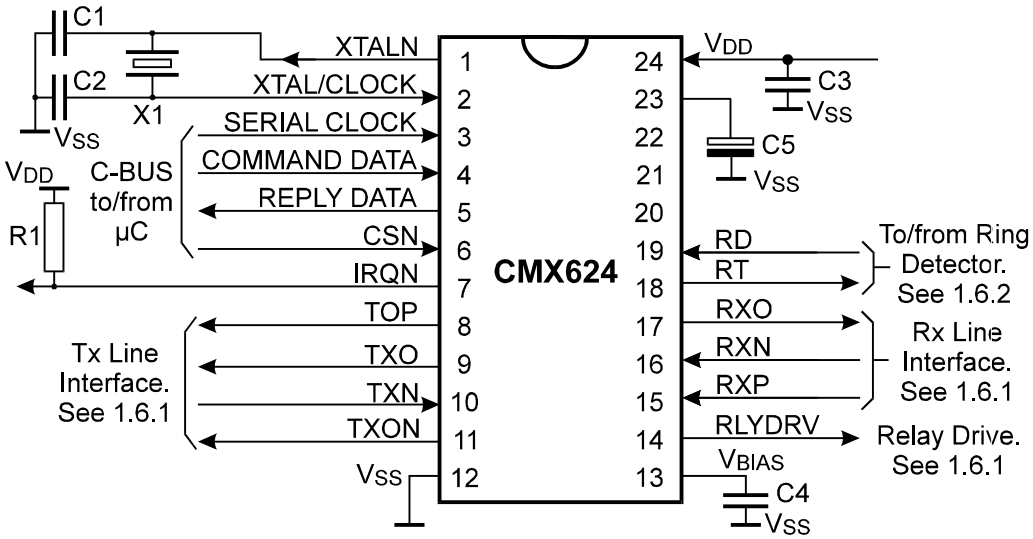
CMX624 D2/D5/P4	Signal		Description
Pin No.	**Name**	**Type**	
16	RXN	I/P	The inverting input to the Rx input amplifier.
17	RXO	O/P	The output of the Rx input amplifier.
18	RT	BI	Open drain output and Schmitt trigger input forming part of the Ring Signal detector.
19	RD	I/P	Schmitt trigger input to the Ring Signal Detector.
20	-	NC	No connection should be made to this pin.
21	-	NC	No connection should be made to this pin.
22	-	NC	No connection should be made to this pin if the printed circuit board is to be used for CMX624 only. If the board is also to be used for CMX644A, a capacitor should be connected as shown in Figure 2.
23	-	I/P	No connection should be made to this pin if the printed circuit board is to be used for CMX624 only. If the board is also to be used for CMX644A, a capacitor should be connected as shown in Figure 2.
24	V_{DD}	Power	The positive supply rail. Levels and thresholds within the device are proportional to this voltage. Should be decoupled to V_{SS} by a capacitor mounted close to the device pins.

Notes:

I/P = Input
O/P = Output
BI = Bidirectional
T/S = 3-state Output
NC = No Connection

This device is capable of detecting and decoding small amplitude signals. To achieve this V_{DD} and V_{BIAS} decoupling and protecting the receive path from extraneous in-band signals are very important. It is recommended that the printed circuit board is laid out with a ground plane in the CMX624 area to provide a low impedance connection between the V_{SS} pin and the V_{DD} and V_{BIAS} decoupling capacitors.

1.4 External Components



R1	100kΩ	C1, C2	18pF
X1	3.579545MHz	C3, C4	0.1µF
		C5	*

Resistors ±5%, capacitors ±10% unless otherwise stated.
* This component is only required for compatibility with CMX644A, see CMX644A Data Sheet for further details.

Figure 2 Recommended External Components for Typical Application

1.5 General Description

The CMX624 contains a V.23/Bell 202 compatible FSK modem capable of duplex operation at 1200/75 or 1200/150 bps over a 2-wire line or 1200/1200 bps over a 4-wire line, a flexible FSK data UART, a receive FSK or Call Progress Tone energy detector, a 2100Hz detector, a DTMF generator, a Tx line driving buffer amplifier, a telephone line Ringing Signal or Line Voltage Reversal detector and a 3.579545MHz Xtal oscillator. These functions are all controlled over a 'C-BUS' serial µC interface which also carries the transmit and receive FSK modem data.

1.5.1 Xtal Osc and Clock Dividers

Frequency and timing accuracy of the CMX624 is determined by a 3.579545MHz clock present at the XTAL/CLOCK pin. This may be generated by the on-chip oscillator inverter using the external components C1, C2 and X1 of Figure 2, or may be supplied from an external source to the XTAL/CLOCK input. If the clock is supplied from an external source, C1, C2 and X1 should not be fitted.

The on-chip oscillator is turned off in the 'Zero-Power' mode.

If the clock is provided by an external source which is not always running, then the 'Zero-Power' mode must be set when the clock is not available. Failure to observe this rule may cause a rise in the supply current drawn by CMX624.

1.5.2 Rx Input Amplifier

This amplifier, with suitable external components, is used to adjust the received signal to the correct amplitude for the FSK receiver and Energy Detect circuits and may also form part of a 2-wire or 4-wire hybrid circuit; see Section 1.6.1.

1.5.3 Receive Filter and Equaliser

This block includes a bandpass filter whose characteristics are set by bits 4 and 5 of the FSK MODE Register according to the receive operating mode (Call Progress, 75/150bps FSK or 1200bps FSK). It is used to attenuate out of band noise and interfering signals, especially the locally generated transmit FSK signal which could otherwise interfere with the received FSK signal when the modem is operating in 2-wire duplex mode. When receiving 1200bps FSK data an optional equaliser section, enabled by setting bit 6 of the FSK MODE Register, compensates for one-half of the ETS Test Line 1 characteristics shown in Figure 3b.

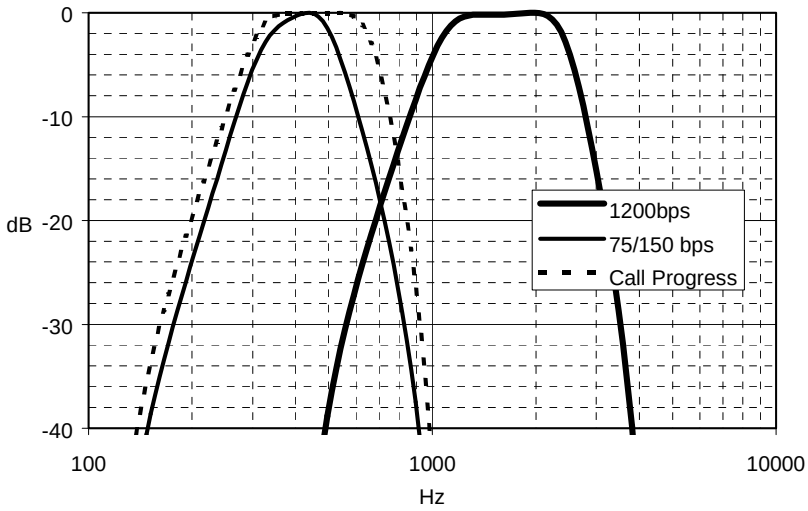


Figure 3a Rx Frequency Responses with Line Interface, see section 1.6.1 (equaliser disabled)

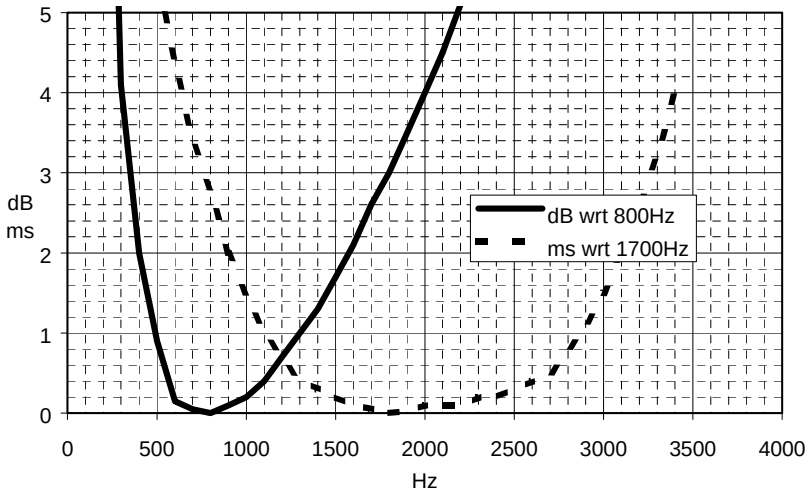


Figure 3b ETS 300 114 Test Line 1 Characteristics (Normalised)

1.5.4 FSK Demodulator

This block is enabled when bits 1 and 5 of the FSK MODE Register are set to '1', and converts the 75, 150 or 1200 bps FSK input signal to a binary received data signal which is sent to the Rx UART block.

Note that in the absence of a valid FSK signal, the demodulator may falsely interpret speech or other extraneous signals as data.

1.5.5 Rx Energy and 2100Hz Detector

The function of this block is controlled by Bits 4 and 5 of the FSK MODE Register and Bit 0 of the TX TONES Register.

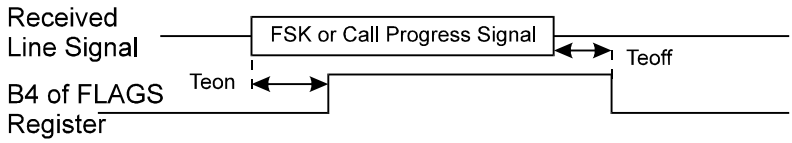
When Bit 0 of the TX TONES Register and Bits 4 and 5 of the FSK MODE Register are set to '1' this block will measure the frequency and amplitude of the incoming signal. When a signal of 2100Hz is present of sufficient amplitude and time Bit 4 of the FLAGS Register is set high. See Section 1.7.1 for amplitude, time and frequency limits.

When Bit 0 of the TX TONES Register is set to '0' this block compares the level of the signal at the output of the Receive Filter against an internal threshold and may be used as a FSK level detector or a simple Call Progress Signal detector according to the settings of bits 4 and 5 of the FSK MODE Register, which affect the Receive Filter pass band as described in Section 1.5.3.

The required register settings are summarised in the table below:

TX TONES Reg	FSK MODE Reg		
Bit 0	Bit 5	Bit 4	Detection Mode
0	0	0	Call Progress
0	1	0	75 / 150 bps FSK
0	1	1	1200 bps FSK
1	1	1	2100 Hz

Bit 4 of the FLAGS Register is set to '1' by the output of this block when the received level has exceeded the threshold for sufficient time. Amplitude and time hysteresis are used to reduce chattering in marginal conditions.



See Section 1.7.1 for definitions of Teon and Teoff

Figure 4 Rx Energy Detector Timing

1.5.6 FSK / DTMF Modulator

When bit 7 of the TX TONES Register is set to '0' then this block generates FSK signals as determined by bits 0 and 1 of the FSK MODE Register and the Tx data bits from the UART block as shown in the tables below:

V.23 mode (bit 7 of SETUP register = '0'):

FSK MODE Reg		FSK / DTMF Modulator block output	FSK Signal Frequency	
Bit 1	Bit 0	(Bit 7 of TX TONES = '0')	'0' (Space)	'1' (Mark)
0	x	Disabled (o/p held at V_{DD} / 2)	-	-
1	0	75bps FSK	450Hz	390Hz
1	1	1200bps FSK	2100Hz	1300Hz

Bell 202 mode (bit 7 of SETUP register = '1'):

FSK MODE Reg		FSK / DTMF Modulator block output	FSK Signal Frequency	
Bit 1	Bit 0	(Bit 7 of TX TONES = '0')	'0' (Space)	'1' (Mark)
0	x	Disabled (o/p held at V_{DD} / 2)	-	-
1	0	150bps FSK	487Hz	387Hz
1	1	1200bps FSK	2200Hz	1200Hz

When bit 7 of the TX TONES Register is set to '1', the block generates DTMF tone pairs or single tones from the DTMF range as shown in the table below. Bit 6 of the TX TONES Register is then used to enable or disable the block's output to the Tx filter.

TX DATA Register Bits 0 - 3				DTMF Tone Pairs (TX TONES Register Bit 4 = '0')			Single Tone (Bit 4 = '1')
D3	D2	D1	D0	Lower Frequency (Hz)	Upper Frequency (Hz)	Keypad Legend	Single Tone Frequency (Hz)
0	0	0	0	941	1633	D	1633
0	0	0	1	697	1209	1	1209
0	0	1	0	697	1336	2	1336
0	0	1	1	697	1477	3	1477
0	1	0	0	770	1209	4	1209
0	1	0	1	770	1336	5	1336
0	1	1	0	770	1477	6	1477
0	1	1	1	852	1209	7	1209
1	0	0	0	852	1336	8	852
1	0	0	1	852	1477	9	852
1	0	1	0	941	1336	0	941
1	0	1	1	941	1209	*	941
1	1	0	0	941	1477	#	941
1	1	0	1	697	1633	A	697
1	1	1	0	770	1633	B	770
1	1	1	1	852	1633	C	852

1.5.7 Transmit Filter

This stage attenuates out of band signals present at the output of the FSK/DTMF modulator and also includes a programmable 3dB level switch, selected by bit 2 of the FSK MODE Register.

The nominal output levels at the TOP pin when V_{DD} = 5.0V are as shown below.

FSK MODE Register bit 2	FSK Signal	DTMF Tone (Low group)	DTMF Tone (High group)
0 (low level)	-6dB	-5dB	-3dB
1 (high level)	-3dB	-2dB	0dB

0dB = 775mVrms

These levels are proportional to V_{DD}, and the actual transmit signal levels present on the 2- or 4-wire line will depend on the external circuitry as described in Section 1.6.1. Using the external components recommended in Section 1.6.1 for a nominal FSK transmit level of -9dBm, DTMF tone levels of -8dBm and -6dBm, then the out of band energy sent to the line will be within the limits shown in Figure 5 for both FSK and DTMF signals.

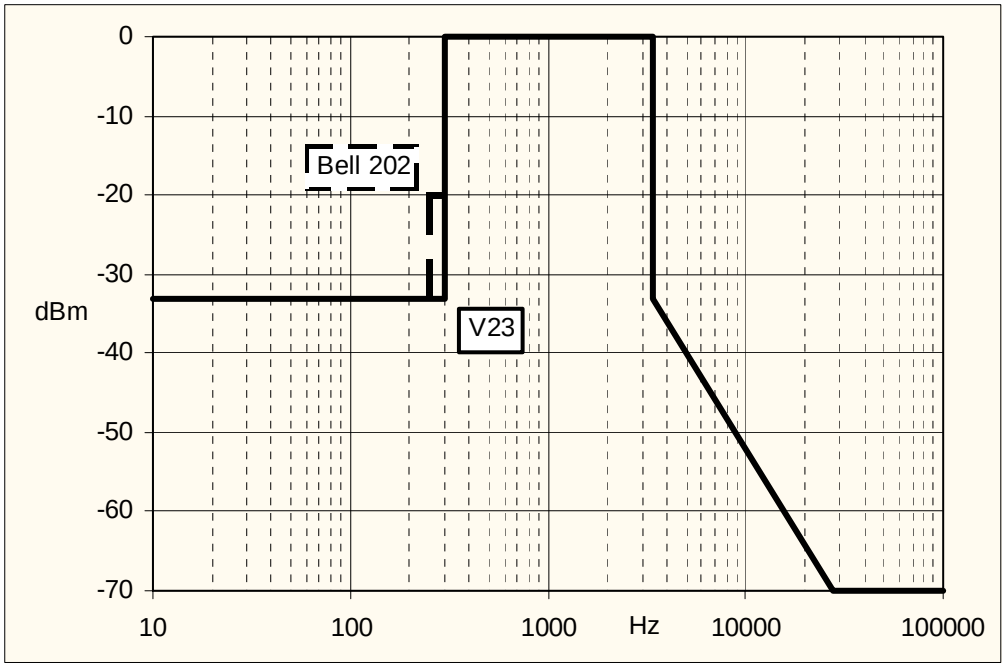


Figure 5 Maximum Out of Band Tx Line Energy Limits

1.5.8 Transmit Output Buffer

This buffer amplifier, connected to the TXN, TXO and TXON pins, is intended for use as a Tx line driver as shown in Section 1.6.1. Two symmetrical outputs are provided for use with a balanced load to give sufficient Tx line signal levels even at low V_{DD}. If this is not required the TXON output can be disabled.

If the buffer is used as a balanced line driver, then bit 6 of the SETUP Register should be set to '1' (TXON output enabled). Setting bit 6 to '0' disables the TXON output and the buffer draws less current from the supply. When bit 6 is set to '0' the TXON pin should be left open circuit. N.B. The TXO output is unaffected by this bit.

1.5.9 Ring Signal Detector

This block, which functions even in Zero Power mode, can be used to detect a telephone line Ring Signal or Line Voltage Reversal and then generate a Interrupt Request signal to wake up the µC at the start of a call. Suitable interface circuits are shown in Section 1.6.2.

The output of this block is the 'Ring Detect' line shown in Figure 1 which directly drives bit 6 of the FLAGS Register. Any '0' to '1' or '1' to '0' change on this line will also set the 'Ring Detect Change' bit (5) of the FLAGS Register.

If this block is not used, then the RD and RT pins should be connected to V_{SS} and the 'Ring Detect Change' bit (5) of the IRQ MASK Register set to '0'.

1.5.10 Tx/Rx UART

This block connects the µC, via the 'C-BUS' interface, to the received data from the FSK Demodulator and to the transmit data input to the FSK Modulator.

As part of this function, the block can be programmed to convert data to be transmitted from 7 or 8-bit bytes to asynchronous data characters, adding Start and Stop bits and - optionally - a parity bit to the data before passing it to the FSK Modulator. Similarly, in the receive direction it can extract data bits from asynchronous characters coming from the FSK Demodulator, stripping off the Start and Stop bits and performing an optional Parity check on the received data before passing the result over the 'C-BUS' to the µC. Bits 0-3 of the SETUP Register control the number of Stop and Data bits and the Parity options for both receive and transmit directions.

Data to be transmitted should be loaded by the µC into the TX DATA Register when the Tx Data Ready bit (bit 0) of the FLAGS Register goes high. It will then be treated by the Tx UART block in one of two ways, depending on the setting of bit 3 of the FSK MODE Register:

If the bit is '0' ('Tx Sync' mode) then the 8 bits from the TX DATA Register will be transmitted sequentially at 75, 150 or 1200bps, LSB (D0) first.

If bit 3 of the FSK MODE Register is '1' ('Tx Async') then bits will be transmitted as asynchronous data characters at 75, 150 or 1200 bps according to the following format:

One Start bit (Space).

7 or 8 Data bits from the TX DATA Register (D0-D6 or D0-D7) as determined by bit 0 of the SETUP Register. LSB (D0) transmitted first.

Optional Parity bit (even or odd parity) as determined by bits 1 and 2 of the SETUP Register.

One or Two Stop bits (Mark) as determined by bit 3 of the SETUP Register.

In both cases data will only be transmitted if bit 1 of the FSK MODE Register is set to '1'.

Failure to load the TX DATA Register with a new value when required will result in bit 1 (Tx Data Underflow) of the FLAGS Register being set to '1' and if the 'Tx Async' mode of operation had been selected then a continuous Mark ('1') signal will then be transmitted until a new value is loaded into TX DATA, whereas in 'Tx Sync' mode the byte already in the TX DATA Register will be re-transmitted.

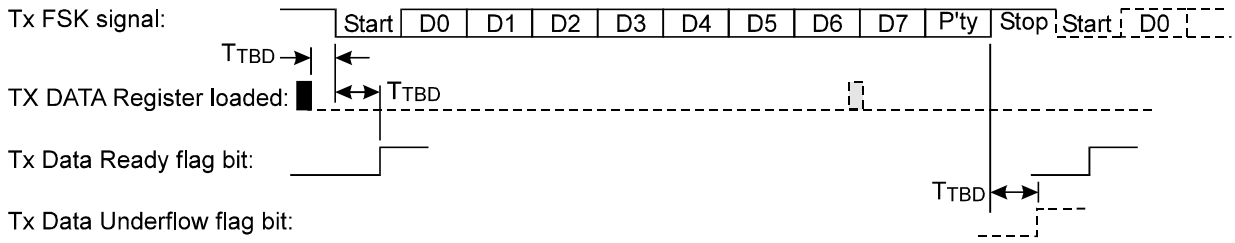


Figure 6a Transmit UART Function (Async)

Received data from the FSK Demodulator goes into the receive part of the UART block, where it is handled in one of two ways depending on the setting of bit 7 of the FSK MODE Register:

If the bit is '0' ('Rx Sync' mode) then the receive part of the UART block will simply take 8 consecutive bits from the Demodulator and transfer them to the RX DATA Register (the first bit going into the D0 position). Note that this mode is intended for detection of simple data patterns such as '1010…' or continuous Mark or Space signals, the CMX624's receive data clock extraction circuits are not adequate to support a true synchronous receive data mode of operation.

If bit 7 of the FSK MODE Register is '1' (' Rx Async') then the received data output of the FSK Demodulator is treated as 75, 150 or 1200 bps asynchronous characters each comprising:

A Start bit (Space).

7 or 8 Data bits as determined by bit 0 of the SETUP Register. These bits will be placed into the RX DATA Register with the first bit received going into the D0 position.

An optional Parity bit as determined by bits 1 and 2 of the SETUP Register. If Parity is enabled (bit 2 of the SETUP Register = '1') then bit 7 of the FLAGS Register will be set to '1' if the received parity is incorrect.

At least one Stop bit (Mark).

Bit 2 (Rx Data Ready) of the FLAGS Register will be set to '1' every time a new received value is loaded into the RX DATA Register. If the previous contents of the RX DATA Register had not been read out over the 'C-BUS' before the new value is loaded from the UART then bit 3 (Rx Data Overflow) of the FLAGS Register will also be set to '1'.

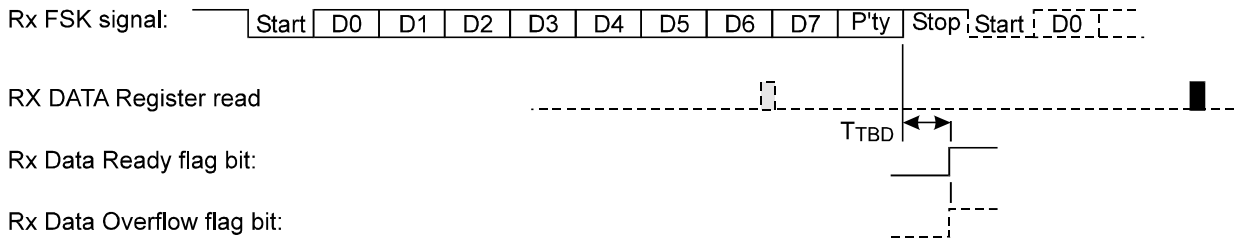


Figure 6b Receive UART Function (Async)

1.5.11 'C-BUS' Interface

This block provides for the transfer of data and control or status information between the CMX624's internal registers and the µC over the 'C-BUS' serial bus. Each transaction, see Figure 7, consists of a single Register Address byte sent from the µC which may be followed by a single data byte sent from the µC to be written into one of the CMX624's Write Only Registers, or a single byte of data read out from one of the CMX624's Read Only Registers, as illustrated in Figure 7.

Data sent from the µC on the Command Data line is clocked into the CMX624 on the rising edge of the Serial Clock input. Reply Data sent from the CMX624 to the µC is valid when the Serial Clock is high. The interface is compatible with the most common µC serial interfaces such as SCI, SPI and Microwire, and may also be easily implemented with general purpose µC I/O pins controlled by a simple software routine. See Figure 10 for detailed 'C-BUS' timing requirements.

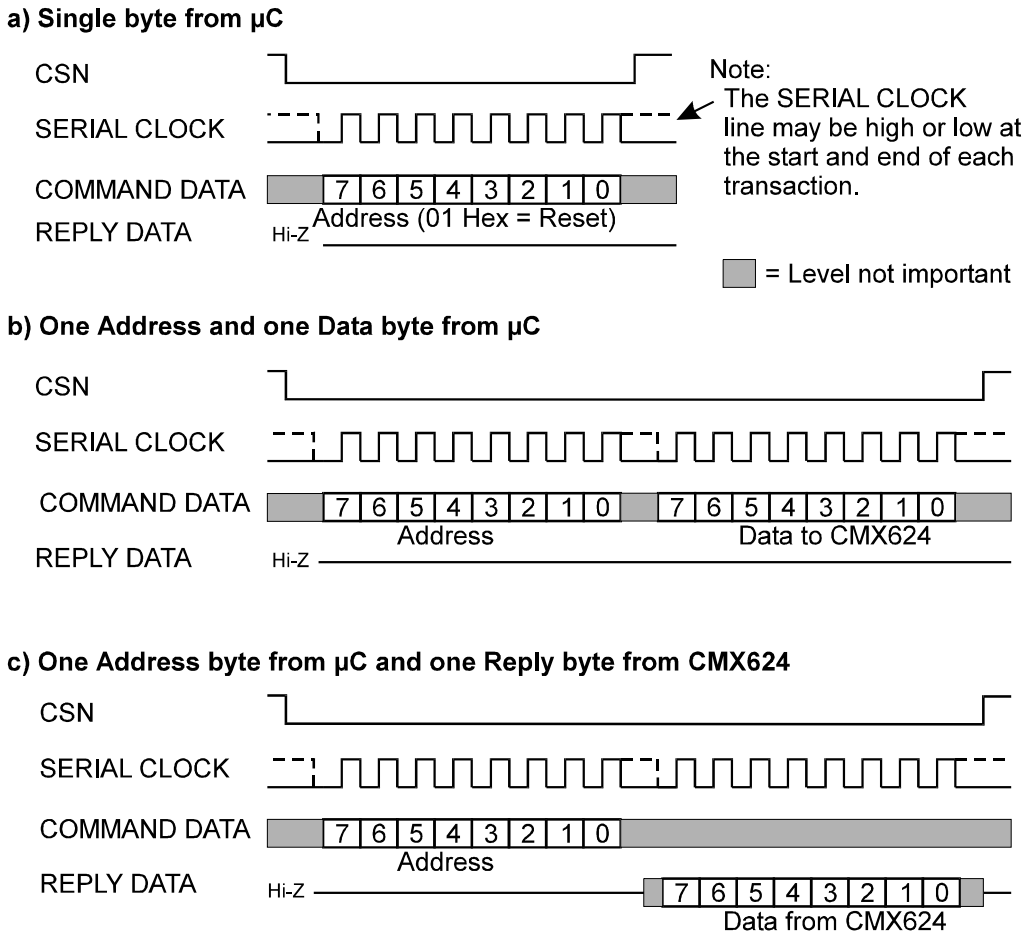


Figure 7 'C-BUS' Transactions

1.5.12 'C-BUS' Registers

Write Only 'C-BUS' Registers

		Command Data Byte Bits							
Addr	Reg.	7	6	5	4	3	2	1	0
$01	RESET	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
$E0	SETUP	FSK mode: 0 = V.23 1 = Bell 202	TXON o/p: 0 = Off 1 = On	Relay Drive: 0 = o/c 1 = Pull low	0 = Zero Power 1 = Normal	Stop bits: 0 = 1 bit 1 = 2 bits	Parity: 0 = None 1 = Parity	Parity: 0 = Odd 1 = Even	Data bits: 0 = 8 bits 1 = 7 bits
$E1	TX TONES	Tx Mode: 0 = FSK. 1 = Tones.	Tone or FSK o/p: 0 = Off. 1 = On.	Reserved, set to 0	0 = DTMF 1 = Single tone	Reserved, set to 0	Reserved, set to 0	Reserved, set to 0	Set Detect: 0 = FSK/CP 1 = 2100Hz
$E3	TX DATA	D7	D6	D5	D4	D3	D2	D1	D0
$E7	FSK MODE	0 = Rx Sync 1 = Async	Rx Equal: 0 = Off 1 = On	0 = Rx Call Progress 1 = Rx FSK	0 = Rx 75 / 150 bps 1 = 1200	0 = Tx Sync 1 = Async	Tx o/p level: 0 = Normal 1 = +3dB	FSK enable: 0 = Off 1 = On (Tx & Rx)	0 = Tx 75 / 150 bps 1 = 1200 or DTMF
$EE	IRQ MASK	Reserved, Set to 0	Reserved, Set to 0	Ring Detect Change	Reserved, Set to 0	Rx Data overflow	Rx Data ready	Tx Data underflow	Tx Data ready

Read Only 'C-BUS' Registers

		Reply Data Byte Bits							
Addr	Reg.	7	6	5	4	3	2	1	0
$EA	RX DATA	D7	D6	D5	D4	D3	D2	D1	D0
$EF	FLAGS	Bad Rx Parity	Ring Detect	Ring Detect Change **	Rx Energy or 2100Hz detect.	Rx Data overflow **	Rx Data ready **	Tx Data underflow **	Tx Data ready **

** See notes 2 and 3

Notes:

1. Accessing the RESET Register over the 'C-BUS' clears all of the bits in the SETUP, TX TONES, TX DATA, FSK MODE and IRQ MASK registers, and bits 0-3 and 5 of the FLAGS Register to '0'. This will set the device into Zero Power mode. Note that this is a single-byte 'C-BUS' transaction consisting solely of the address byte value $01.

   Note that putting the device in Zero Power mode by directly setting SETUP Bit 4 to '0' does not clear the other register bits. Care should be taken before re-enabling the device that the other bits are set so as to prevent undesired transient operation. In particular, bit 6 of the TXTONES Register should be set to '0' to prevent modulation of the transmitter output.

2. If any of bits 0, 1, 2, 3 or 5 of the FLAGS Register is '1' and the corresponding bit of the IRQ MASK Register is also '1' then the IRQN output of the CMX624 will be pulled low.

3. Bit 5 (Ring Detect Change) of the FLAGS Register is set on every '0' to '1' or '1' to '0' change of bit 6 (Ring Detect).

4. Clearing bit 4 of the SETUP Register puts the CMX624 into the Zero Power mode by turning off all blocks except for the 'C-BUS' interface and Ring Detector circuit.

5. Reading the FLAGS Register clears the IRQN output and also clears bits 0, 1, 2, 3 and 5 of the FLAGS Register.

6. FLAGS Register (bit 4) is '1' whenever the received signal being looked for is detected and '0' when both signals are absent. IRQ MASK Register (bit 4) is normally set to '0' - but can be set to '1' to enable interrupts on the IRQN output. In the latter case, IRQN will be continuously pulled to '0' whilst Rx Energy or 2100Hz are present. This may be useful for device evaluation purposes.

1.6 Application Notes

1.6.1 Line Interface

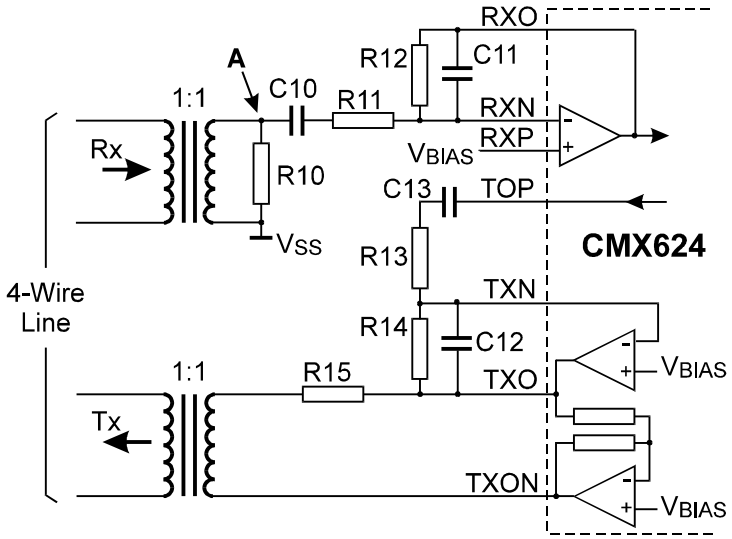
A line interface circuit is needed to provide dc isolation between the modem and the line, to perform line impedance termination, and to set the correct transmit and receive signal levels.

4-Wire Line Interface

Figure 8a shows an interface circuit for use with a 600Ω 4-wire line. The line terminations are provided by R10 and R15, while R11 and R13 should be selected to give the desired transmit and receive levels.

The gain of the receive input amplifier (R12 / R11) should be set to compensate for the loss of the input transformer and the supply voltage.

Assuming transformer loss of about 1dB, R11 should be 91kΩ at 5.0V, or 130kΩ at 3.0V.



Note relay circuit, ac and dc loads and line protection not shown for clarity.

R10	600Ω	R13	See text	C10	100nF
R11	See text	R14	100kΩ	C11	220pF
R12	100kΩ	R15	600Ω	C12	330pF
				C13	100nF

Resistors ±1%, capacitors ±20%.

Figure 8a 4-Wire Line Interface Circuit

In the transmit direction, the level on the 4-wire line is determined by the level at the TOP pin, the gain of the Output Buffer Amplifier, a loss of nominally 6dB due to the line termination resistor R15, and the loss in the transformer.
The TOP pin signal level is proportional to V_{DD} and is also affected by the setting of the Tx o/p level control bit (bit 2) of the FSK Mode Register.

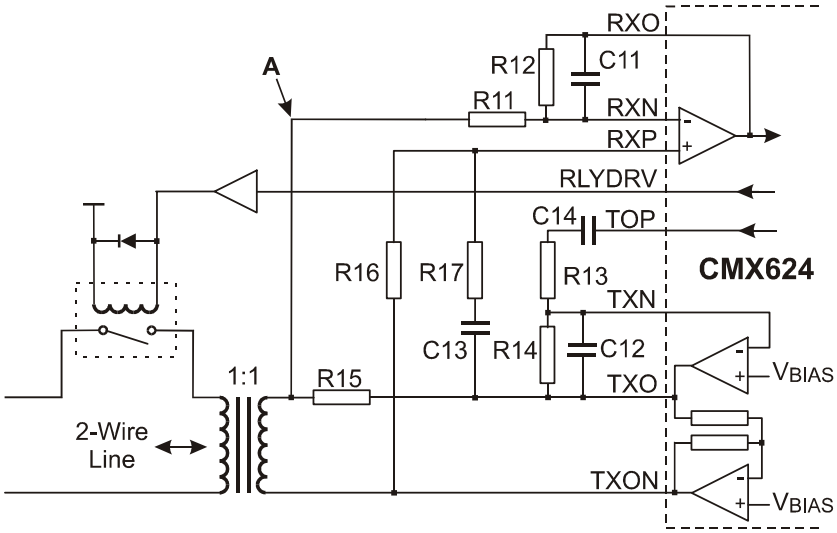
Assuming that the Tx o/p level control bit is set to '1' (giving a FSK signal level of -3dB wrt 775mVrms at the TOP pin when V_{DD} = 5.0V) and that there is 1dB loss in the transformer, then:

$$\text{Tx FSK 4-wire line level} = -(3+6+1) + 20 \times LOG_{10}(2 \times R14 / R13) + 20 \times LOG_{10}(V_{DD} / 5.0) \quad \text{dBm}$$

For example, to generate a nominal Tx FSK line level of -9dBm, R13 should be 180kΩ when V_{DD} = 5.0V, falling to 120kΩ at 3.3V.

2-Wire Line Interface

Figure 8b shows an interface circuit suitable for connection to a 600Ω 2-wire line. The circuit also shows how a relay may be driven from the RLYDRV pin. Note that when the CMX624 is powered from less than 5.0V, buffer circuitry will be required to drive a 5V relay.



Note ac and dc loads and line protection not shown for clarity.

R11	See text	R15	600Ω	C11	220pF
R12	100kΩ	R16	120kΩ	C12	330pF
R13	See text	R17	100kΩ	C13	10nF
R14	100kΩ			C14	100nF

Resistors ±1%, capacitors ±20%

Figure 8b 2-Wire Line Interface Circuit

This circuit includes a 2-wire to 4-wire hybrid circuit, formed by R11, R15, R16, R17, C13 and the impedance of the line itself, which ensures that the modem receive input and transmit output paths are both coupled efficiently to the line, while minimising coupling from the modem's transmit signal into the receive input.
The values of R11 and R13 should be calculated in the same way as for the 4-wire interface circuit of Figure 8a.

1.6.2 Ring Detector Interface

Figure 9 shows how the CMX624 may be used to detect the large amplitude Ringing signal received at the start of an incoming telephone call.

The ring signal is usually applied at the subscriber's exchange as an ac voltage inserted in series with one of the telephone wires and will pass through either C20 and R20 or C21 and R21 to appear at the top end of R22 (point X in Figure 9) in a rectified and attenuated form.

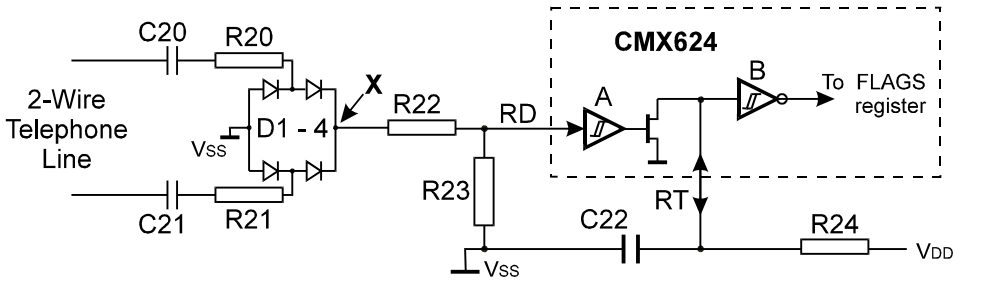
The signal at point X is further attenuated by the potential divider formed by R22 and R23 before being applied to the CMX624 RD input. If the amplitude of the signal appearing at RD is greater than the input threshold (Vthi) of Schmitt trigger 'A' then the N transistor connected to RT will be turned on, pulling the voltage at RT to V_{SS} by discharging the external capacitor C22. The output of the Schmitt trigger 'B' will then go high, setting bit 6 (Ring Detect) of the FLAGS Register.

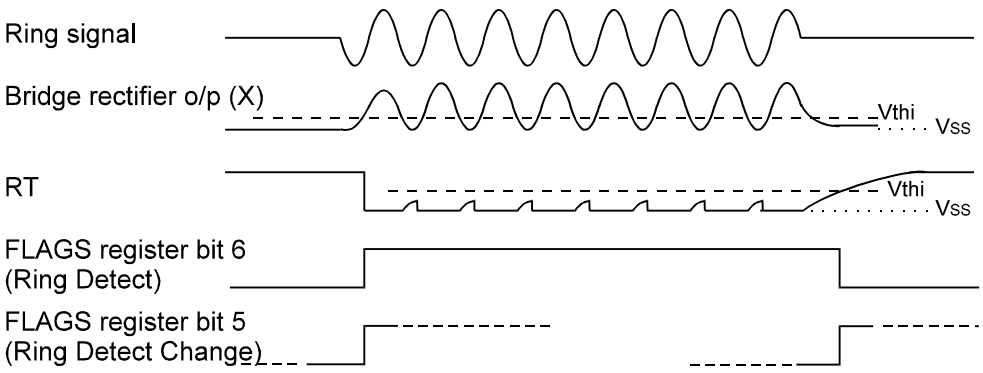
The minimum amplitude ringing signal that is certain to be detected is:

$$(0.7 + Vthi \times [R20 + R22 + R23] / R23) \times 0.707 \quad Vrms$$

where Vthi is the high-going threshold voltage of the Schmitt trigger A (see Section 1.7.1).

With R20-22 all 470kΩ as Figure 9, then setting R23 to 68kΩ will guarantee detection of ringing signals of 40Vrms and above for V_{DD} over the range 3.0 to 5.5V.





R20, 21, 22	470kΩ	C20, 21	0.1µF
R23	See text	C22	0.33µF
R24	470kΩ	D1-4	1N4004

Resistors ±1%, capacitors ±20%

Figure 9 Ring Signal Detector Interface Circuit

If the time constant of R24 and C22 is large enough then the voltage on RT will remain below the threshold of the 'B' Schmitt trigger for the duration of a ring cycle.

The time for the voltage on RT to charge from V_{SS} towards V_{DD} can be derived from the formula

$$V_{RT} = V_{DD} \times [1 - \exp(-t/(R24 \times C22))]$$

As the Schmitt trigger high-going input threshold voltage (Vthi) has a minimum value of 0.56 x V_{DD} , then the Schmitt trigger B output will remain high for a time of at least 0.821 x R24 x C22 following a pulse at RD.

The values of R24 and C22 given in Figure 9 (470kΩ and 0.33μF) give a minimum RT charge time of 100 msec, which is adequate for ring frequencies of 10Hz or above.

Note that the circuit will also respond to a telephone line voltage reversal. If necessary the μC can distinguish between a Ring signal and a line voltage reversal by measuring the time that bit 6 of the FLAGS Register (Ring Detect) is high.

1.7 Performance Specification

1.7.1 Electrical Performance

1.7.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Unit
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current into or out of V_{DD} and V_{SS} pins	-50	+50	mA
Current into RLYDRV pin		+50	mA
Current into or out of any other pin	-20	+20	mA

D2 Package	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at Tamb = 25°C		800	mW
... Derating		13	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

D5 Package	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at Tamb = 25°C		550	mW
... Derating		9	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

P4 Package	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at Tamb = 25°C		800	mW
... Derating		13	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

1.7.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Unit
Supply (V_{DD} - V_{SS})		2.7	5.5	V
Operating Temperature		-40	+85	°C
Xtal Frequency	1	3.575965	3.583125	MHz

Notes: 1. A Xtal frequency of 3.579545MHz ±0.1% is required for correct operation.

1.7.1.3 Operating Characteristics

For the following conditions unless otherwise specified:
V_{DD} = 2.7V at Tamb = 25°C and V_{DD} = 3.0V to 5.5V at Tamb = -40 to +85°C,
Xtal Frequency = 3.579545MHz ± 0.1%, 0dBm corresponds to 775mVrms.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
I_{DD} (Zero Power mode)	1, 2	-	1.0	-	µA
(Running, TXON o/p Off, V_{DD}= 5.0V)	1	-	3.4	6.0	mA
(Running, TXON o/p Off, V_{DD}= 3.3V)	1	-	1.8	3.2	mA
(Running, TXON o/p On, V_{DD}= 5.0V)	1	-	3.5	6.2	mA
(Running, TXON o/p On, V_{DD}= 3.3V)	1	-	1.9	3.4	mA
Logic '1' Input Level	3	70%	-	-	V_{DD}
Logic '0' Input Level	3	-	-	30%	V_{DD}
Logic Input Leakage Current (Vin = 0 to V_{DD}), (excluding XTAL/CLOCK input)		-1.0	-	+1.0	µA
Output Logic '1' Level (I_{OH} = 360µA)		V_{DD}-0.4	-	-	V
Output Logic '0' Level (I_{OL} = 360µA)		-	-	0.4	V
IRQN O/P 'Off' State Current (Vout = V_{DD})		-	-	1.0	µA
Schmitt trigger input high-going threshold (Vthi) (see Figure 11)		0.56V_{DD}	-	0.56V_{DD} + 0.6V	V
Schmitt trigger input low-going threshold (Vtlo) (see Figure 11)		0.44V_{DD} - 0.6V	-	0.44V_{DD}	V
RLYDRV 'ON' resistance to V_{SS} (V_{DD}= 5.0V)		-	38.0	TBD	Ω

Notes:
1. At 25°C, not including any current drawn from the CMX624 pins by external circuitry other than X1, C1 and C2.
2. All logic inputs at V_{SS} except for RT and CSN inputs which are at V_{DD}.
3. Excluding RD, RT and XTAL/CLOCK pins.

FSK Modulator and Tx UART	Notes	Min.	Typ.	Max.	Unit
Level at TOP pin.	4	-4.0	-3.0	-2.0	dBm
Twist (Mark level WRT Space level)		-2.0	0	+2.0	dB
Tx 1200bits/sec (V.23 mode)					
Baud Rate (set by UART and Xtal frequency)		1194	1200	1206	Baud
Mark (Logical 1) Frequency		1297	1300	1303	Hz
Space (Logical 0) Frequency		2097	2100	2103	Hz
Tx 75bits/sec (V.23 mode)					
Baud Rate (set by UART and Xtal frequency)		74	75	76	Baud
Mark (Logical 1) Frequency		388	390	392	Hz
Space (Logical 0) Frequency		448	450	452	Hz
Tx 1200bits/sec (Bell 202 mode)					
Baud Rate (set by UART and Xtal frequency)		1194	1200	1206	Baud
Mark (Logical 1) Frequency		1197	1200	1203	Hz
Space (Logical 0) Frequency		2197	2200	2203	Hz
Tx 150bits/sec (Bell 202 mode)					
Baud Rate (set by UART and Xtal frequency)		149	150	151	Baud
Mark (Logical 1) Frequency		385	387	389	Hz
Space (Logical 0) Frequency		485	487	489	Hz

Notes:
4. At V_{DD} = 5.0V, Tx o/p level control bit set to '1'; load resistance greater than 40kΩ.

DTMF Transmitter	Notes	Min.	Typ.	Max.	Unit
Level at TOP pin; tones in High Group	4	-1.0	0.0	+1.0	dBm
Twist (level of High Group tones WRT level of Low Group tones)		-	+2.0	-	dB
Tone frequency accuracy (worst case)		-0.5	-	+0.5	%

Tx Filter and Output Buffer	Notes	Min.	Typ.	Max.	Unit
Change in level at TOP pin caused by changing bit 2 of FSK MODE Register		2.5	3.0	3.5	dB
Buffer output signal swing; Load greater than 500Ω.	5	2.2	-	-	Vp-p

Notes: 5. For each of the TXON (if enabled) and TXO pins, load between pin and V_{DD} / 2.

FSK Demodulator and Rx UART	Notes	Min.	Typ.	Max.	Unit
Valid Input Level Range	6	-43.0	-	-9.0	dBm
Acceptable Twist (Mark level WRT Space level)		-7.0	-	+7.0	dB
Acceptable Signal to Noise Ratio	7	20.0	-	-	dB
Rx 1200bits/sec (V.23 mode)					
Acceptable Rx Data Rate	8	1188	1200	1212	Baud
Mark (Logical 1) Frequency		1280	1300	1320	Hz
Space (Logical 0) Frequency		2068	2100	2132	Hz
Rx 75bits/sec (V.23 mode)					
Acceptable Rx Data Rate	8	TBD	75	TBD	Baud
Mark (Logical 1) Frequency		TBD	390	TBD	Hz
Space (Logical 0) Frequency		TBD	450	TBD	Hz
Rx 1200bits/sec (Bell 202 mode)					
Acceptable Rx Data Rate	8	1188	1200	1212	Baud
Mark (Logical 1) Frequency		1180	1200	1220	Hz
Space (Logical 0) Frequency		2168	2200	2232	Hz
Rx 150bits/sec (Bell 202 mode)					
Acceptable Rx Data Rate	8	TBD	150	TBD	Baud
Mark (Logical 1) Frequency		TBD	387	TBD	Hz
Space (Logical 0) Frequency		TBD	487	TBD	Hz

Notes: 6. Measured at point A in Figures 8a and 8b, for V_{DD} = 5.0V. The internal threshold levels are proportional to V_{DD}. To cater for other supply voltages or different signal level ranges the voltage gain of the Rx Input Amplifier should be adjusted by selecting the appropriate external components as described in Section 1.6.1.
7. Flat noise in 300-3400 Hz band for V.23, 200-3400 Hz for Bell 202.
8. Set by Rx UART and Xtal frequency.

2100Hz Detector	Notes	Min.	Typ.	Max.	Unit
'Will Decode' Frequency Range		2040	-	2235	Hz
'Will Not Decode' Frequency Range		<2010	-	>2265	Hz
'Off' to 'On' time	9	-	-	25	ms
'On' to 'Off' time	9	4.0	-	-	ms

Notes: 9. 2100Hz detection requires a signal within the amplitude range given in the Rx Energy Detector section.

Rx Energy Detector	Notes	Min.	Typ.	Max.	Unit
'Off' to 'On' Threshold Level (FSK)	6, 10	-48.0	-	-43.0	dBm
'Off' to 'On' Threshold Level (Call Progress)	6, 10	-48.0	-	-40.0	dBm
Hysteresis (measured at V_{DD} = 3V and 5V)	6, 10	2.0	-	-	dB
'Off' to 'On' Time (Figure 4 Teon):	6, 10				
1200bps Rx mode		-	-	25	ms
75/150bps Rx mode		-	-	48	ms
Call Progress Detect mode		-	-	48	ms
'On' to 'Off' Time (Figure 4 Teoff):	6, 10				
1200bps Rx mode		8.0	-	-	ms
75/150bps Rx mode		20	-	-	ms
Call Progress Detect mode		20	-	-	ms

Notes: 10. Measured with 1300Hz signal in 1200bps mode, 390Hz for 75 or 150 bps and Call Progress mode, signal level -33dBm for time delay measurements.

XTAL/CLOCK Input	Notes	Min.	Typ.	Max.	Unit
'High' Pulse Width	11	100	-	-	ns
'Low' Pulse Width	11	100	-	-	ns

Notes: 11. Timing for an external input to the XTAL/CLOCK pin.

'C-BUS' Timings (See Figure 10)		Notes	Min.	Typ.	Max.	Unit
t_{CSE}	CSN-Enable to Clock-High time		100	-	-	ns
t_{CSH}	Last Clock-High to CSN-High time		100	-	-	ns
t_{LOZ}	Clock-Low to Reply Output enable time		0.0	-	-	ns
t_{HIZ}	CSN-High to Reply Output 3-state time		-	-	1.0	µs
t_{CSOFF}	CSN-High Time between transactions		1.0	-	-	µs
t_{NXT}	Inter-Byte Time		200	-	-	ns
t_{CK}	Clock-Cycle time		200	-	-	ns
t_{CH}	Serial Clock-High time		100	-	-	ns
t_{CL}	Serial Clock-Low time		100	-	-	ns
t_{CDS}	Command Data Set-Up time		75	-	-	ns
t_{CDH}	Command Data Hold time		25	-	-	ns
t_{RDS}	Reply Data Set-Up time		50	-	-	ns
t_{RDH}	Reply Data Hold time		0	-	-	ns

Note: These timings are for the latest version of the 'C-BUS' as embodied in the CMX624.

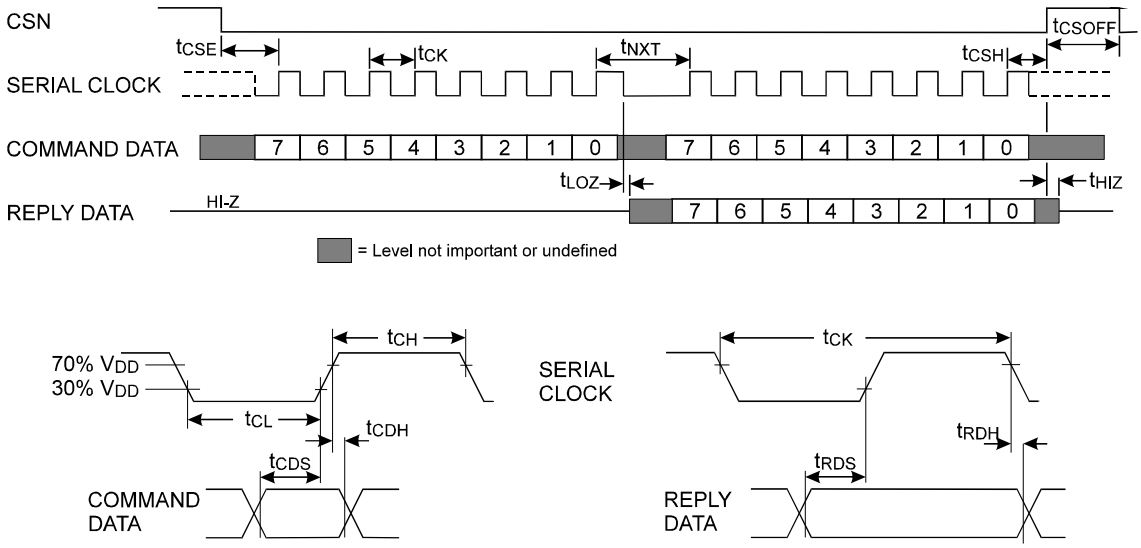


Figure 10 'C-BUS' Timing

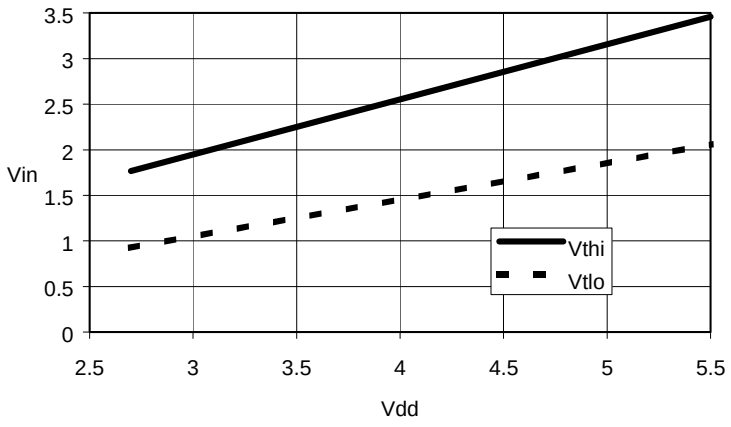
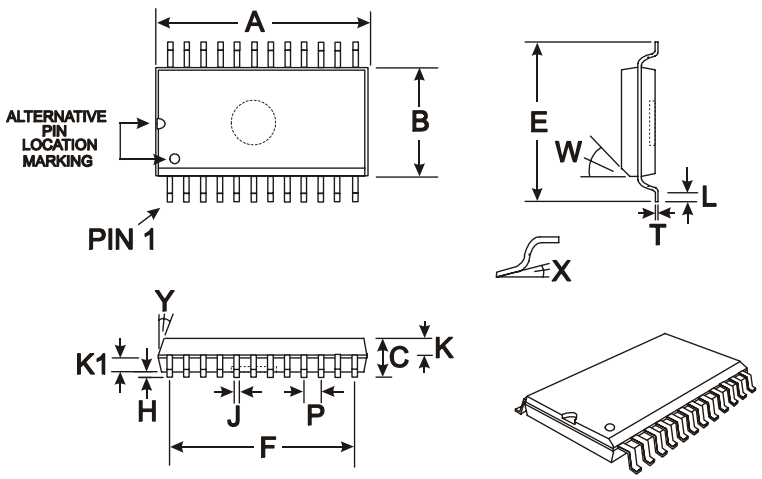


Figure 11 Typical Schmitt Trigger Input Voltage Thresholds vs. V_{DD}

1.7.2 Packaging



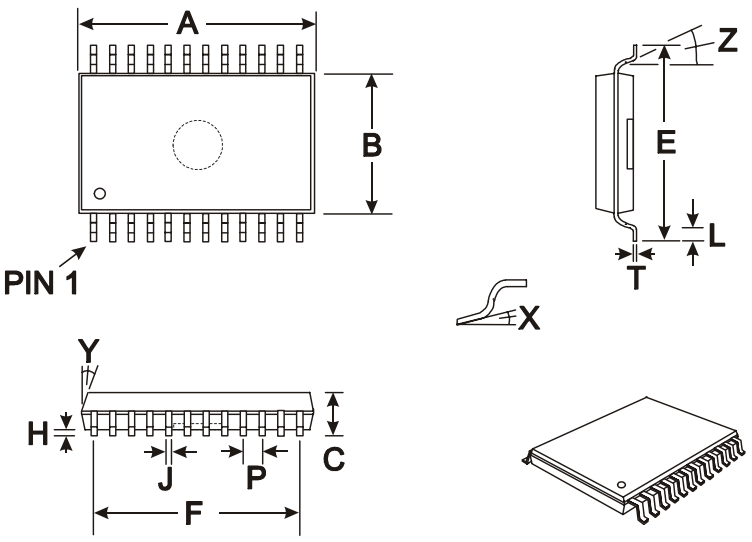
	DIM.	MIN.	TYP.	MAX.
*	A	0.597 (15.16)		0.613 (15.57)
*	B	0.286 (7.26)		0.299 (7.59)
	C	0.093 (2.36)		0.105 (2.67)
	E	0.390 (9.90)		0.419 (10.64)
	F		0.550 (14.1)	
	H	0.003 (0.08)		0.020 (0.51)
	J	0.013 (0.33)		0.020 (0.51)
	K		0.041 (1.04)	
	K1		0.041 (1.04)	
	L	0.016 (0.41)		0.050 (1.27)
	P		0.050 (1.27)	
	T	0.009 (0.23)		0.0125 (0.32)
	W		45°	
	X	0°		10°
	Y		7°	

NOTE :

* A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees
Co-Planarity of leads within 0.004" (0.1mm)

Figure 12a 24-pin SOIC (D2) Mechanical Outline: *Order as part no. CMX624D2*



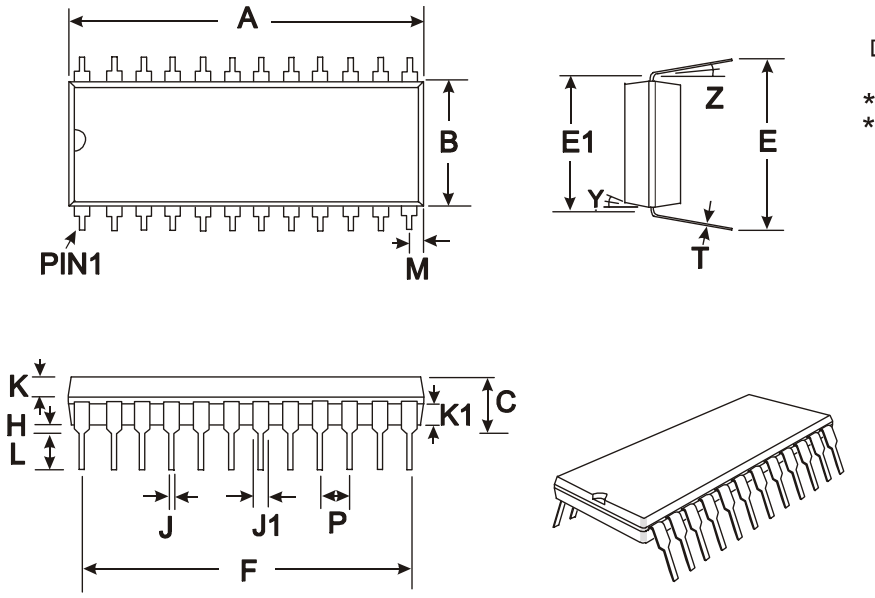
	DIM.	MIN.	TYP.	MAX.
*	A	7.90		8.50
*	B	5.00		5.60
	C	1.67		2.00
	E	7.40		8.20
	F		7.15	
	H	0.05		0.21
	J	0.22		0.38
	L	0.55		0.95
	P		0.65	
	T	0.09		0.25
	X	0°		8°
	Y	7°		9°
	Z	4°		12°

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees
Co-Planarity of leads within 0.1mm

Figure 12b 24-pin SSOP (D5) Mechanical Outline: *Order as part no. CMX624D5*



DIM.	MIN.	TYP.	MAX.
* A	1.200 (30.48)		1.270 (32.26)
* B	0.500 (12.70)		0.555 (14.10)
C	0.142(3.61)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
F		1.10 (27.94)	
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.68)		0.074 (1.88)
K1	0.060 (1.52)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.06)
M		0.180 (4.58)	
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	
Z		4°	

NOTE :

* A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees

Figure 12c 24-pin DIL (P4) Mechanical Outline: *Order as part no. CMX624P4*

Handling precautions: This product includes input protection, however, precautions should be taken to prevent device damage from electro-static discharge. CML does not assume any responsibility for the use of any circuitry described. No IPR or circuit patent licences are implied. CML reserves the right at any time without notice to change the said circuitry and this product specification. CML has a policy of testing every product shipped using calibrated test equipment to ensure compliance with this product specification. Specific testing of all circuit parameters is not necessarily performed.

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