HARRIS

HV255

PRELIMINARY

May 1991

Half Bridge Complementary MOSFET Driver

Features

- Bipolar or Unipolar Supply Operation
- Wide Supply Range ..... ±40V to ±225V
- Complete MOSFET Protection
- High Output to Logic Supply Isolation
- High Peak Output Current 2A
- Fast Switching Times 100ns
- Frequency Range .....10kHz to 100kHz

Applications

- High Switchmode Power Supplies
- PWM Servo Drives
- Stepper Motor Drives
- DC-DC Converters
- Uninterruptible Power Supplies

Ordering Information

PART NUMBER	TEMPERATURE RANGE	DESCRIPTION
HV255CP	$0^oC \leq T_A \leq +75^oC$	16 Pin Plastic DIP
HV255IP	$-40^oC \leq T_A \leq +85^oC$	16 Pin Plastic DIP
HV255MJ*	$-55^oC \leq T_A \leq +125^oC$	16 Pin Ceramic DIP

Description

The HV255 is a monolithic dielectrically isolated high voltage integrated circuit. The circuit provides an interface from digital signals to the gates of complementary power MOSFETs or IGBTs. The circuit has wide supply voltage range, from 80VDC to 450VDC in unipolar connection or +40VDC to +225VDC. In addition the logic supply can float within the high voltage rails.

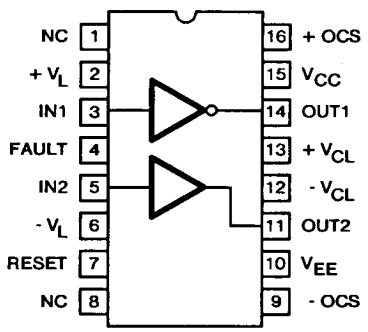
The inputs are TTL compatible when the logic supply is 5V, but will operate up to 15V logic supply.

The outputs provide up to 2A current spikes to drive the gates of power MOSFETs or IGBTs. The actual voltage that the gates are driven to is set by the user, up to 20V for V_{GS}.

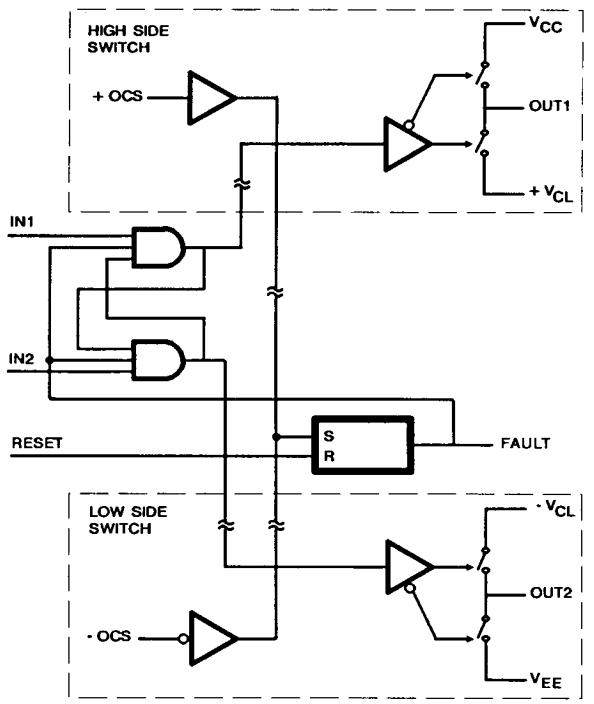
Also on board the chip is an overcurrent sense circuit, which independently sense overcurrent on the high side and the low side. An overcurrent condition sets a latch that disables both outputs. In order to enable the output the reset input must be toggled.

Pinout

HV255CP (16 PIN PLASTIC DIP)
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

 * Offered at a later date.

File Number **2847**

Absolute Maximum Ratings

Voltage Between $+V_S$ and $-V_S$ 500V
Voltage Between $+V_I$ and $-V_I$ 30V
Voltage Between $-V_S$ and $-V_I$ 250V
Peak Output Current 2A
Logic Input Voltage ..... $+V_L$
Over Current Sense to $|V_S|$ 7V
Fault Output Current 1mA

Operating Temperature Range

HV255CP ..... $0^oC \leq T_A \leq +75^oC$
HV255IP ..... $-40^oC \leq T_A \leq +85^oC$
HV255MJ* ..... $-55^oC \leq T_A \leq +125^oC$
Storage Temperature Range ..... $-65^oC \leq T_A \leq +150^oC$
Maximum Junction Temperature ..... $+175^oC$

* Offered at a Later Date

Electrical Specifications V_{CC} = +40V, V_{EE} = -40V, C_L = 10nF, V_L = 5V Unless Otherwise Specified

PARAMETER	TEMP	HV255CP, HV255IP			UNITS
		MIN	TYP	MAX	
INPUT CHARACTERISTICS					
Input Voltage, High (V_{IH})	Full	2.4	-	-	V
Input Voltage, Low (V_{IL})	Full	-	-	0.8	V
Input Current (I_{IH})	+25°C	-	-	300	µA
	Full	-	-	300	µA
Input Current, Low (I_{IL})	+25°C	150	-	-	µA
	Full	150	-	-	µA
Overcurrent Input Threshold	+25°C	80	100	120	mV
	Full	75	100	125	mV
TRANSFER CHARACTERISTICS					
Turn-On Delay (T_{D1}, T_{D3})	+25°C	-	-	1	µs
	Full	-	-	1	µs
Turn-On Delay Skew (T_{D1}, T_{D3})	+25°C	-	±300	-	ns
	Full	-	±300	-	ns
Turn-Off Delay (T_{D2}, T_{D4})	+25°C	-	-	1	µs
	Full	-	-	1	µs
Turn-Off Delay Skew (T_{D2}, T_{D4})	+25°C	-	±100	-	ns
	Full	-	±100	-	ns
Current Limit Sense to Output Turn-Off Delay	+25°C	-	500	-	ns
	Full	-	500	-	ns
Current Limit Sense to Fault Output Turn-Off Delay	+25°C	50	-	150	ns
	Full	50	-	150	ns
Reset Delay (T_{D6})	+25°C	-	500	-	ns
	Full	-	500	-	ns
OUTPUT CHARACTERISTICS					
Output Rise Time	Full	-	100	150	ns
Output Fall Time	Full	-	100	150	ns
OUT1 Voltage (High)	Full	$+V_S$ -0.2	-	-	V
OUT1 Voltage (Low)	Full	-	-	$+V_S$ -19	V
OUT2 Voltage (High)	Full	$-V_S$ +19	-	-	V
OUT2 Voltage (Low)	Full	-	-	$-V_S$ +0.2	V
Fault Output (V_{OH})	Full	4.5	-	-	V
Fault Output (V_{OL})	Full	-	-	0.8	V
POWER SUPPLY					
I_{CC}	Full	-	-	200	µA
I_{EE}	Full	-	-	200	µA
I_L	Full	-	-	4	mA

Parameter Definitions (Refer to Switching Waveforms)

SYMBOL	DEFINITIONS
T_{D2}	Delay time as measured from the logic input high to low transition (1 to 0) at the 10% point, to the 10% point of the output transition for the high side switch.
T_{D1}	Delay time as measured from the logic input low to high transition (0 to 1) at the 10% point, to the 10% point of the output transition for the high side switch.
T_{D4}	Same as T_{D0-1} for the ow side switch.
T_{D3}	Same as T_{D1-1} for the ow side switch.
T_{R1}	Output rise time from the 10% – 90% points for the high side switch.
T_{R2}	Output rise time from the 10% – 90% points for the low side switch.
T_{F1}	Output fall time from the 10% – 90% points for the high side switch.
T_{F2}	Output fall time from the 10% – 90% points for the low side switch.
T_{D5}	Delay time as measured from the overcurrent input 10% point to the fault output high to low transition at the 10% point.
T_{D6}	Delay time as measured from the reset input 10% point to the fault output low to high transition at the 90% point.
T_{D7}	Delay time as measured from the overcurrent 1 input 10% point to output 1 low to high transition at the 90% point.
T_{D8}	Delay time as measured from the overcurrent 2 input 10% point to output 2 high to low transition at the 10% point.

Switching Time Test Circuits

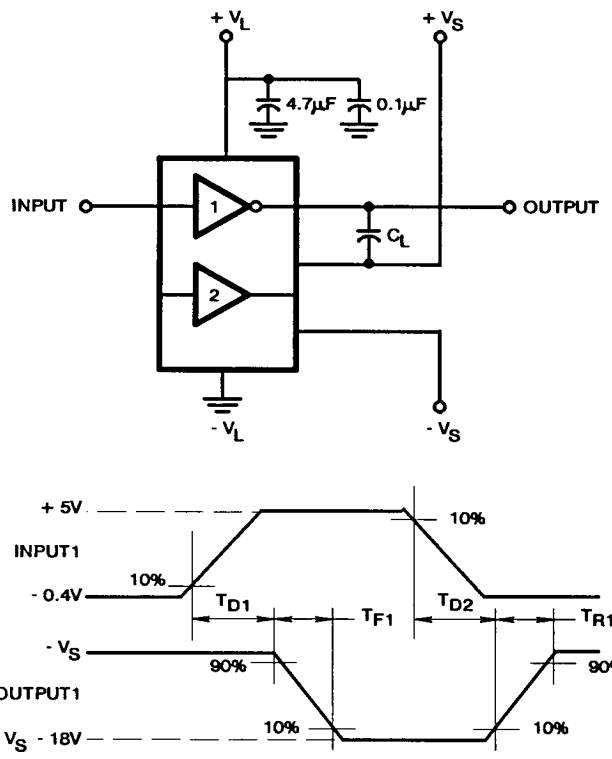


FIGURE 1. INVERTING DRIVE SWITCHING TIME (HIGH SIDE)

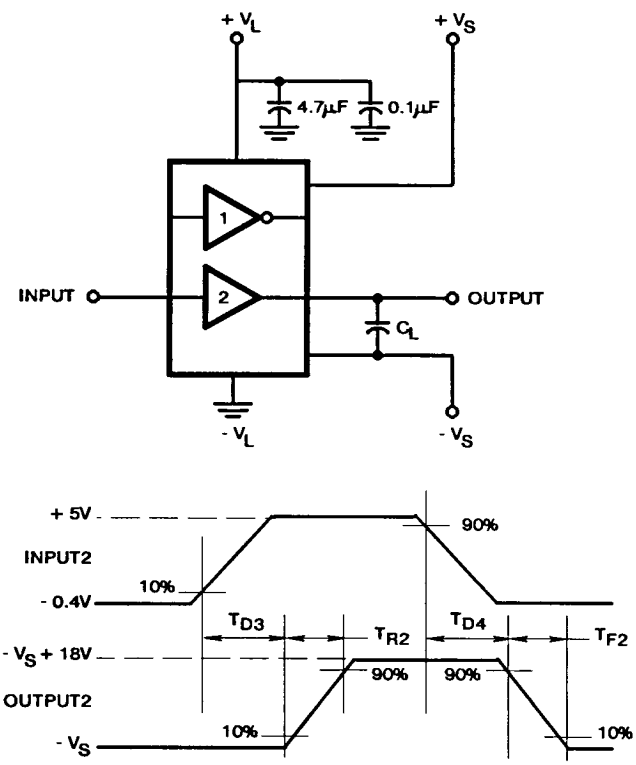
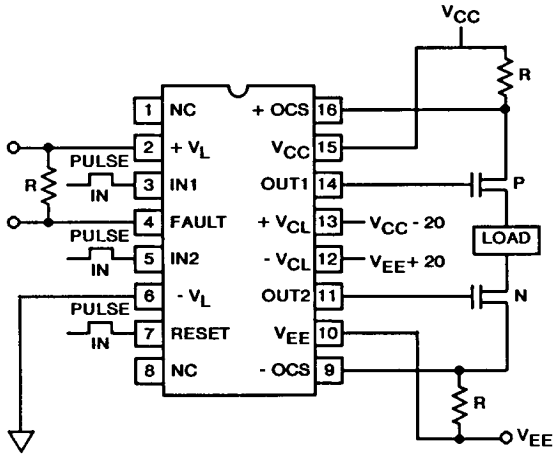
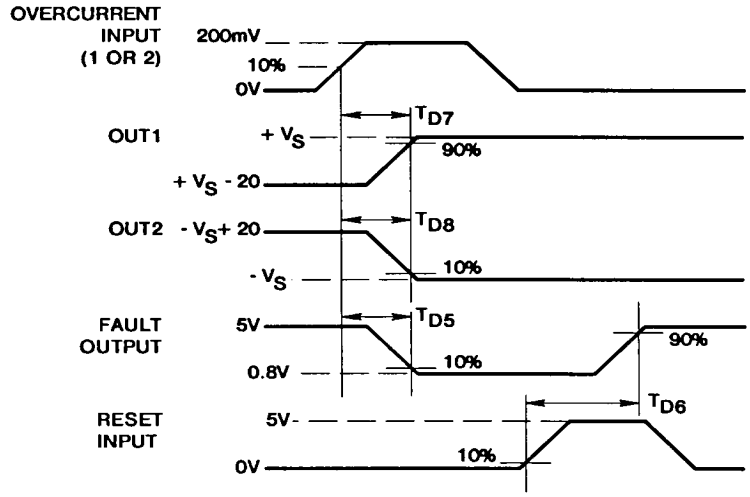


FIGURE 2. NON-INVERTING DRIVER SWITCHING TIME (LOW SIDE)

Overcurrent Test Waveforms

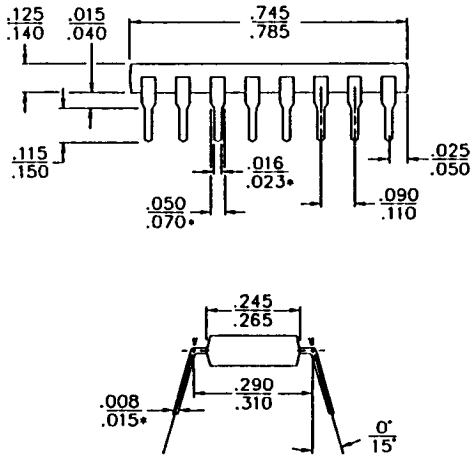
OVERCURRENT TEST CIRCUIT





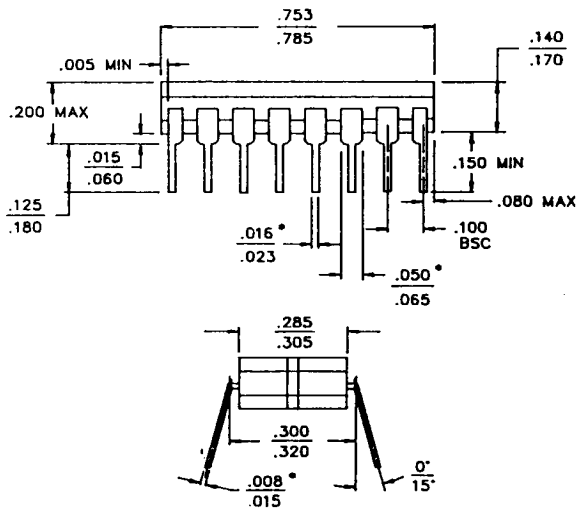
Packaging

16 PIN PLASTIC DIP



* ADD .003 INCHES TO DIM FOR SOLDER DIPPED LEADS.

16 PIN CERAMIC DIP



* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

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