T-77-07-05

LR3791X 1-Chip Microcomputer with a built-in EEPROM for TV Tuner

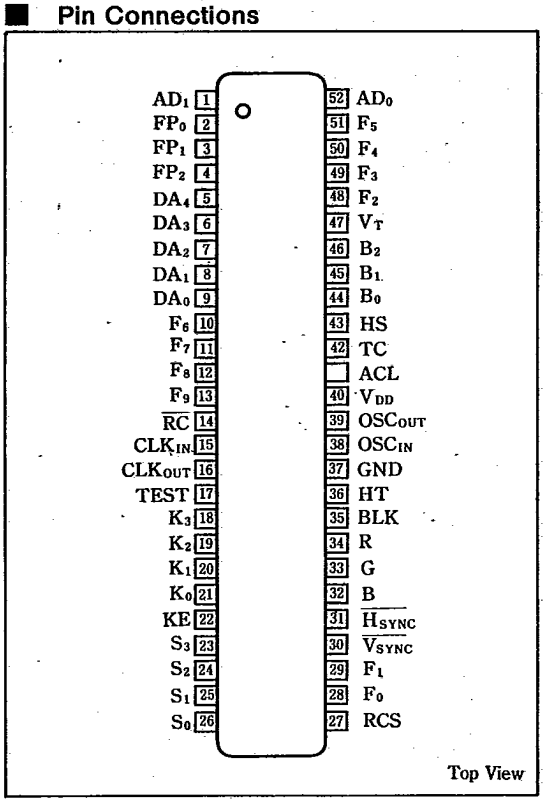
Description

The LR3791X is a 4-bit microcomputer for voltage synthesizer TV tuners. This mocrocomputer integrates an EEPROM for tuning data memory, on-screen display function, and A/D and D/A converters in a single chip.

Features

1. CMOS silicon gate process
2. ROM capacity : 8192×9 bits
3. RAM capacity : 256×4 bits
4. EEPROM capacity : 50×16 bits (for tuning data memory)
5. Instruction cycle time : 2 μs/4MHz
6. Number of instructions : 57
7. Subroutine stack : 6 levels (including data pointer stack and interrupt)
8. Interrupt : 4 kinds
9. I/O pin : 26 pins (Including 13 pins assigned for N-ch. open drain output)
10. Built-in SIO function (8-bit)
    F7, F8 and F9 ports are used as serial data-in, serial data-out and SIO clock respectively.
11. A/D converter : 4 bits×1 port (Additional two ports are mask option)
12. D/A converter : 14 bits×1 port (For tuning voltage control)
    6bits×5 ports (N-ch. open drain output or general purpose output)
13. Synchronizing signal detection counter
    5 bits×1 port (Available for general purpose input)
14. On-screen display control function
    - Display characters : 24 characters×2 lines or 12 characters×4 lines (Multiple block display is possible)
    - Number of characters : 96
    - Character composition : 12×12 dots
    - Display colors : 8 colors (R, G, B and BLK output, each output can be used as general purpose output.)
    - Background : 8 colors (with background half tone output pin)
    - Blinking : 1 sec interval (0.7 sec ON, 0.3 sec OFF)
    - Character data ROM : 12 dots×12 dots×96 characters=13824 bits
    - Display data RAM : 48 characters×(7+3+1) =528 bits
      7 : character designation
      3 : color designation
      1 : blinking designation
    - Character size : 2 kinds (H and V)
15. +5V single power supply (TYP.)
16. 52-pin shrink dual-in-line package

Pin Connections



Top View

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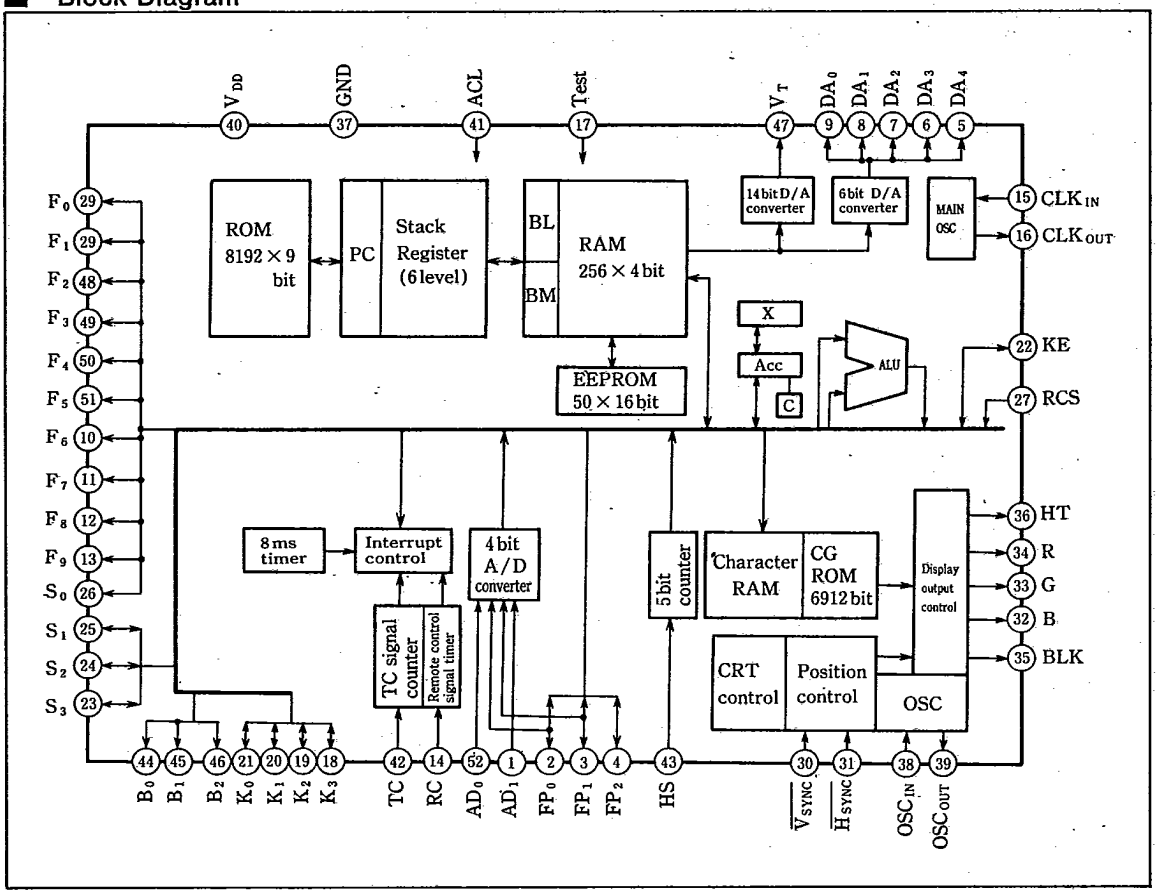
Block Diagram



Pin Description

Pin No.	Pin name	I/O	I/O type	State at ACL	termination
1	AD_1	I	PD/PU/OG	—	ADC input
2	FP_0	I/O	PU/OD/PP	H	General purpose I/O port. When OD is selected and the output is "High", ADC input is obtained
3	FP_1	I/O	PU/OD/PP	H	General purpose I/O port. When OD is selected and the output is "High", ADC input is obtained
4	FP_2	I/O	PU/OD/PP	H	General purpose I/O port
5-9	DA_4-DA_0	O	OD/PP	L	DAC output. General purpose output port
10	F_6	I/O	OD/PP	L	Medium voltage open drain
11	F_7	I/O	OD/PP	L	General purpose I/O port. Medium voltage open drain
12	F_8	I/O	OD/PP	L	General purpose I/O drain. Medium voltage open drain
13	F_9	I/O	OD/PP	L	General purpose I/O drain. Medium voltage open drain
14	$\overline{RC}$	I	PU	—	External interrupt input
15	CLK_{IN}	I	—	—	System clock generator
16	CLK_{OUT}	I/O	—	—	System clock generator
17	TEST	I	PD	—	Test pin. Normally at "Low"
18-21	K_3-K_0	I/O	PU/OD/PP	H	General purpose I/O port
22	KE	I/O	PU/OD/PP	H	General purpose I/O port
23-26	S_3-S_0	I/O	PU/OD/PP	H	General purpose I/O port
27	RCS	I/O	PU/OD/PP	H	General purpose I/O port
28, 29	F_0, F_1	I/O	OD/PP	H	General purpose I/O port. Medium voltage open drain
30	$\overline{V_{SYNC}}$	I	PU	—	Vertical synchronizing signal input
31	$\overline{H_{SYNC}}$	I	PU	—	Horizontal synchronizing signal input
32	B	O	PP	L	CRT display. Blue output. General purpose output port
33	G	O	PP	L	CRT display. Green output. General purpose output port
34	R	O	PP	L	CRT display. Red output. General purpose output port
35	BLK	O	PP	L	CRT display. Blanking output. General purpose output port
36	HT	O	PP	L	CRT display. Half tone output. General purpose output port
37	GND	—	—	—	Reference voltage
38	OSC_{IN}	I	—	—	Clock generator for CRT display
39	OSC_{OUT}	I/O	—	—	Clock generator for CRT display
40	V_{DD}	—	—	—	Supply voltage
41	ACL	I	PD	—	ACL input
42	TC	I	PD/PU/OG	—	Event counter (50/60 Hz input)
43	HS	I	PD/PU/OD	—	Event counter (Synchronizing detection input). General purpose input port
44-46	B_0-B_2	I/O	OD/PP	H	General purpose I/O port. Medium voltage open drain
47	V_T	I/O	PP	H	Tuning voltage output
48-50	F_2-F_4	I/O	OD/PP	L	General purpose I/O port. Medium voltage open drain
51	F_5	I/O	OD/PP	H	General purpose I/O port. Medium voltage open drain
52	AD_0	I	PD/PU/OG	—	ADC input

OG : Open gate, PU : Pull-up, PD : Pull-down, OD : Open drain, PP : Push-pull.

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■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Supply voltage	V_{DD}	−0.3 to +7.5	V	1
Input voltage	V_{IN}	−0.3 to V_{DD}+0.3	V	1
Output voltage 1	V_{OUT}	−0.3 to V_{DD}+0.3	V	1, 2
Output voltage 2	V_{OD}	−0.3 to +15	V	1, 3
Operating temperature	T_{opr}	−10 to +70	℃	
Storage temperature	T_{stg}	−55 to +150	℃	

Note 1 : Referenced to GND.
Note 2 : Applied to pins other than medium voltage open drain output pin.
Note 3 : Applied to medium voltage open drain output pin.

■ Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Note
Supply voltage	V_{DD}	4.5	5.0	5.5	V	1
System clock frequency	f_{SYS}		4.0		MHz	
CRT clock frequency	f_{ORT}		6.0	6.6	MHz	

Note 1 : Applied to the case where pins other than H_{SYNK}, V_{SYNK}, $\overline{INT_2}$, HS and TC are used as input.

■ Electrical Characteristics

(V_{DD}=4.5 to 5.5V, Ta=−10 to +70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH1}		0.9V_{DD}		V_{DD}	V	1
	V_{IL1}		0		0.1V_{DD}		
	V_{IH2}		0.7V_{DD}		V_{DD}	V	2
	V_{IL2}		0		0.3V_{DD}		
Input current	I_{IH1}	$V_{IH}=V_{DD}$			10	μA	3
	$-I_{IL1}$	V_{IL}=0V			100		
	I_{IH2}	$V_{IH}=V_{DD}$			100	μA	4
	$-I_{IL2}$	V_{IL}=0V			10		
	I_I	V_I=0-V_{DD}			10	μA	5
Output current	$-I_{OH1}$	$V_{OH}=V_{DD}-1.0V$	1.0			mA	6
	I_{OL1}	V_{OL}=1.0V	1.0			mA	7
	I_{OL2}	V_{OL}=2.0V	10			mA	8
	$-I_{OH3}$	V_{OH}=1.0V	10			μA	9
ACL release voltage	V_{ACL}	External 3.0V Zener diode and resistor		3.5		V	10
Horizontal synchronizing signal pulse width	t_{HSYNC}	Horizontal synchronizing signal from TV set in "Low" stage	5			μs	11
Vertical synchronizing signal pulse width	t_{VSYNC}	Vertical synchronizing signal from TV set in "Low" stage	5			μs	12
Current consumption	I_{DD}	f_{srs}=4.0MHz, f_{CRT}=6.0MHz			20	mA	13
Input current	I_{IH3}	$V_{IH}=V_{DD}$			10	μA	14
	$-I_{IL3}$	V_{IL}=0V			800		

Note 1 : Applied to pins $\overline{H_{SYNC}}$, $\overline{V_{SYNC}}$, $\overline{INT2}$, HS and TC.
Note 2 : Applied to the case where pins other than those shown in note 1 are used as input.
Note 3 : Applied to pins which pulled-up at the termination or input pin designed to pull-up by mask option.
Note 4 : Applied to pins which pulled-down at the termination or input pin designated to pull-down by mask option.
Note 5 : Applied to pins with open-gate at the termination or input pin designated to open-gate by mask option.
Note 6 : Applied to output pin of push-pull or general purpose I/O designated to push-pull by mask option.
Note 7 : Applied to general purpose I/O pin excluding medium voltage open-drain.
Note 8 : Applied to medium voltage open-drain pin.
Note 9 : Applied to general purpose I/O pin designated to pull-up by mask option.
Note 10 : Applied to $\overline{ACL}$ pin.
Note 11 : Applied to $\overline{H_{SYNC}}$ pin.
Note 12 : Applied to $\overline{V_{SYNC}}$ pin.
Note 13 : No-load condition.
Note 14 : Applied to general purpose I/O pin designated to pull-up by mask option.

■ EEPROM Memory Characteristics

Endurance of erase/write cycle : 10^5 times
Data hold time characteristics : 10 years

■ Functions

(1) Interrupt

The following four kinds of interrupt are available.

① External interrupt from $\overline{INT}$ pin

34-64 μs after the signal applied to $\overline{INT}$ pin is fallen, it is judged as the interrupt signal, and interrupt request flip-flop is set.

② Internal interrupt from 8 ms timer

An internal interrupt is generated every 8 ms all the time, and interrupt request flip-flop is set.

③ Internal interrupt from event counter

Interrupt request flip-flop is set by overflowing of 4-bit event counter (up counter) which counts the input from TC pin.

④ External interrupt from SIO

When serial from F_7 is input as much as 8 bits, interrupt request flip-flop is set.

(2) 14-bit D/A converter (V_T)

14-bit D/A converter outputs the pulse row which is pulse-width modulated (PWM) from V_T corresponding to 14-bit data stored in RAM and converts it to tuning voltage using a simple external low pass filter. Output waveform of V_T divides frequency T_O (repeated frequency 8.192ms) into 2^{14} pieces minimum pulse width "t_O" (500ns) and executes pulse width modulation according to 14-bit data at "t_O" unit.

(3) 6-bit D/A converter (DA_0-DA_4)

6-bit D/A converter outputs the pulse row which is pulse-width modulated (PWM) from DA corresponding to 6-bit data stored in RAM.

DA_0-DA_4 output waveform divides frequency T_O (repeated frequency 512 μs) into 2^6 pieces minimum pulse width "t_O" (8 μs) and executes pulse width modulation at "t_O" unit according to 6-bit data.

The DA_0-DA_4 is an Nch medium voltage (+12V) open drain output.

(4) Remote control signal timer

Pulse interval of the signal which is applied to the external interrupt circuit from $\overline{INT}$ pin can be measured in the range of 0 to 4.096ms based on the reference clock (256 μs unit×16). This counter consists of 4 bits, and counter value can be transferred to the accumulator Acc. When the interval exceeds 4.096ms, counter value remains "F" even if it is transferred to the accumulator Acc.

(5) A/D converter (AD_0, AD_1, FP_0, FP_1)

A/D converter inputs include four pins such as AD_0, AD_1 inputs and FP_0, FO_1 inputs. These are selected by the program. Analog voltage at the selected pin is compared with 16 kinds of voltages by the software one by one and can be converted into 4-bit data.

(6) 5-bit counter (HS)

The HS input consists of a 5-bit counter and latch which stores upper 4 bits. After the counter is reset for the first time, it counts the pulse being input to HS pin for 1.02ms. Following this, the content of a counter is latched by 2 μs. The counter is reset again to execute pulse counting. The content thus latched can be transferred to the accumulator Acc.

(7) K_0-K_3, S_0-S_3, FP_0-FP_2, RCS and KE pins

These are of general purpose I/O pins. Selection of output format of push-pull, open drain and pull-up is carried out at ROM masking. The relation between input/output state vs. termination is as follows :

Pin	Termination	I/O	Output data set
I/O	Push-pull	O	don't care
	Open drain, Pull-up	O	don't care
		I	Set the output state to go High

In the case output format is of push-pull, use it as an output.

(8) F_0-F_9 and B_0-B_2 pins

These pins are of Nch medium voltage (+12V) open drain I/O. The output should be "High" when input. In the case push-pull output format is selected by mask option, use it as an output.

(9) EEPROM

Built-in EEPROM is organized as 50 words×16 bits. When writing, 16-bit data stored in RAM is written. When reading, 16-bit data of EEPROM is stored in RAM at 4-bit unit through an accumulator.

(10) Serial interface

The serial interface consists of an 8-bit shift register and a 3-bit counter, and can be used for serial data input/output. When a serial interface is used, each flag of SM register should be set by programming.

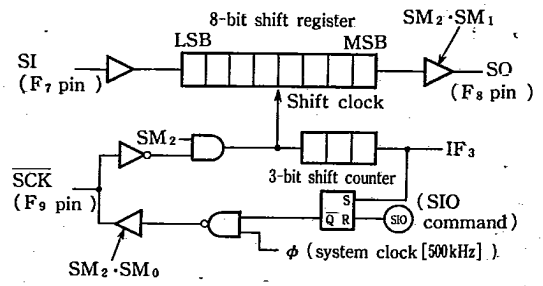


Fig. 1 Serial interface block diagram

2	1	0
SM Register		

Fig. 2

SM_2 : Operation/non-operation of serial interface is selected.
"0" : Non-operation (In this case, F_7, F_8 and F_9 pins ares used as general purpose I/O).
"1" : Operation

SM_1 : SO (F_8 pin) state is selected.
"0" : Becomes high impedance and is used exclusively for input.
"1" : Content of shift register is output.

SM_0 : Transfer clock is selected.
"0" : External clock.
(input from F_9 pin)
"1" : Internal clock (500kHz).
(also output from F_9 pin)

※ All SM flags are reset at "0" at ACL.

As for serial shift operation, the most significant bit (MSB) of a shift register is taken out at the falling edge of a serial clock and is output to F_8 pin if SM_2 and SM_1 flags are being set. In the meantime, the data input to F_7 pin while the serial clock is at "Low" is transferred to the least significant bit (LSB) at the rising edge of a serial clock, and the content of a shift register is shifted to upper location by 1-bit.

As for data setting of an 8-bit shift register, 8-bit data being stored in RAM is transferred. At data reading from an 8-bit shift register, upper 4 bits and lower 4 bits are taken into accumulator respectively.

(11) CRT display

The CRT display control circuit is controlled by setting various control registers from the accumulator and memory. 96 kinds of character patterns are displayed in the form of 24 characters×2 lines or 12 characters×4 lines. Color designation is possible for each character unit. Each display character is composed of 12×12 dots.

① **Setting of character data** The character data is stored into character RAM. Composition of one word of character RAM is as follows :

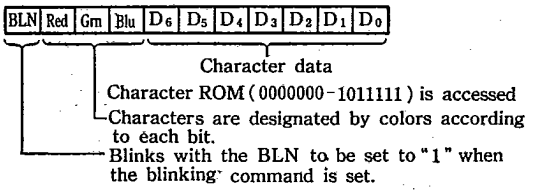


Fig. 3 Composition of display RAM data

As for character data, 11-bit data stored in the data RAM is transferred. The address of character RAM is designated by an exclusive address register. The value of address is set by transferring 6-bit data stored in the data RAM. The value of address register is automatically counted up when character data is transferred.

② **Positionning of display** The start point of character display can be set by 32 stages at 8H

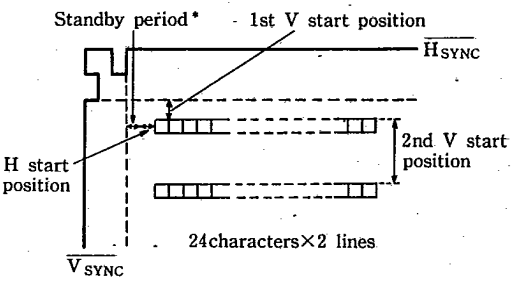
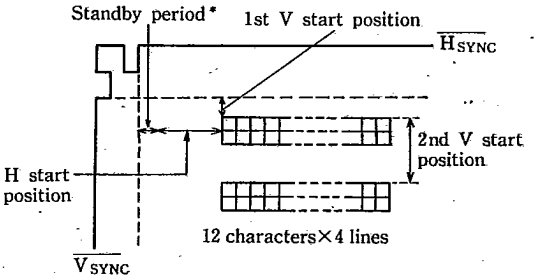


Fig. 4



* Standby period Lower case character $(1/f_{OSC} \times 25)$ ns
Upper case character $(1/f_{OSC} \times 49)$ ns

Fig. 5 Display position 1

unit to vertical direction and 16 stages at $8/f_{OSC}$ sec unit to horizontal direction. This is determined by horizontal start point register (H register) and vertical start point register (V register). As for display, 24 characters×2 lines or 12 characters×4 lines can be controlled by the most significant bit of V register. The display can be divided into two blocks. As for 24 characters×2 lines, it is divided every one line, and for 12 characters×4 lines, it is divided every two lines.

As for the value of horizontal and vertical start point registers, 4-bit value or 11-bit value stored in the data RAM is transferred.

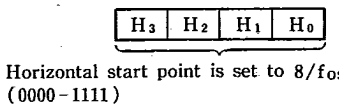


Fig. 6 H Register

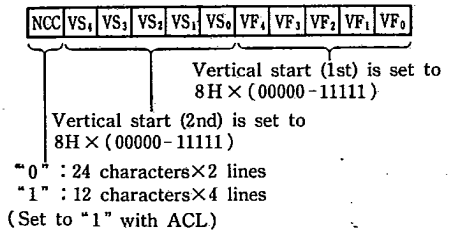


Fig. 7 V register

When the 2nd vertical start data is set at 00000, block division to vertical direction is not available.

③ Display ON/OFF and Blinking Display ON/OFF and blinking are set by setting the data to 4-bit register.

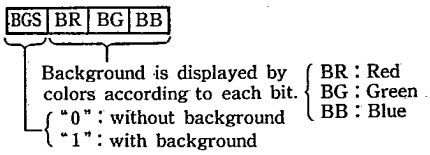
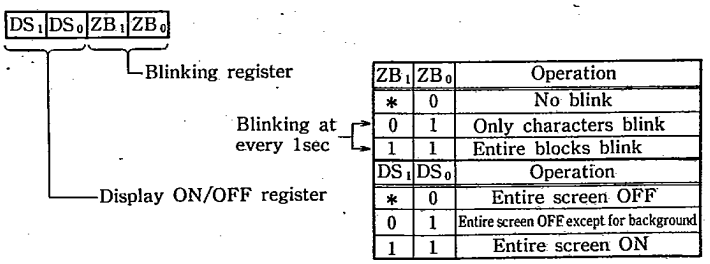


Fig. 8



ZB_1	ZB_0	Operation
*	0	No blink
0	1	Only characters blink
1	1	Entire blocks blink
DS_1	DS_0	Operation
*	0	Entire screen OFF
0	1	Entire screen OFF except for background
1	1	Entire screen ON

Fig. 9

④ Color designation of background Entire background of the block where characters are displayed can be designated by setting the data to 4-bit register.

⑤ Color designation of entire background The color of background of entire screen can be designated by setting 4-bit data to the register.

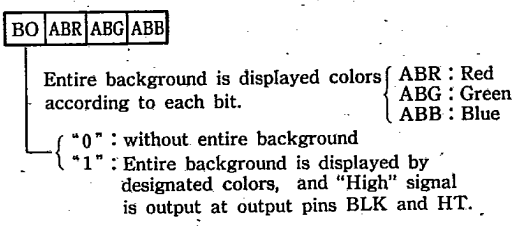
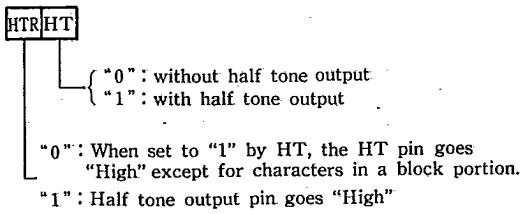


Fig. 10

⑥ Setting of halftone When characters are being displayed, it is possible to output the timing signal from HT pin in order to reduce the brightness of character background (block portion). This is done by setting the data to 2-bit register.

When HT bit is set at "1" to display the background and entire background, the background portion is displayed by the color including that of entire background.



HTR F/F	HT F/F	HT output
1	*	High
0	0	Low
0	1	Half tone output

Fig. 11

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⑦ Line background and ON/OFF of line display Line background and ON/OFF of line display can be designated by setting the character value of D_6-D_0 in one word in character RAM to the following specific value. (See Fig. 3)

i) When D_6, D_5, D_4, D_3, D_2, D_1, D_0=1, 1, 1, 1, 1, 0, 0, background of the display following to this data in the same line becomes ON. (This has nothing to do with background register BGS.)

ii) When D_6, D_5, D_4, D_3, D_2, D_1, D_0=1, 1, 1, 1, 1, 0, 1, background of the display following to this data in the same line becomes OFF. (This has nothing to do with background register BGS.)

iii) When D_6, D_5, D_4, D_3, D_2, D_1, D_0=1, 1, 1, 1, 1, 1, 0, display following to this data in the same line becomes OFF. (This has nothing to do with display ON/OFF register.)

iv) When D_6, D_5, D_4, D_3, D_2, D_1, D_0=1, 1, 1, 1, 1, 1, 1, display following to this data in the same line becomes ON. (This is applicable to the case where display ON/OFF register is ON).

After the foregoing data setting, the portion should be blank without background.

⑧ Taking-in of CRT display states

1) Of the CRT display states, the position of vertical direction dot of displaying characters can be taken into the accummulator Acc.

2) Of the CRT display states, the line number of display can be taken into the accumulator Acc.

3) Of the CRT display states, vertical synchronizing signal $\overline{V_{SYNC}}$ and display division completion signal can be taken.

By using these functions, multiple line block display is possible.

⑨ Designation of character size Four kinds of character size can be set in every line.

Character size	Horizontal	Vertical
Lower case characters	$12/f_{OSC}$	12H
Horizontally double size characters	$24/f_{OSC}$	12H
Vertically double size characters	$12/f_{OSC}$	24H
Horizontally and vertically double size characters	$24/f_{OSC}$	24H

⑩ Character ROM data 96 kinds of character ROMs can be designated. Each character is composed of 12×12 dots.

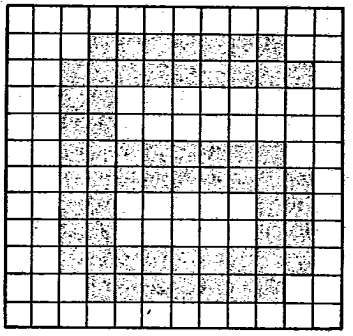


Fig. 12 Example of character

(12) CLK_{IN}, CLK_{OUT}

CLK_{IN} and CLK_{OUT} pins are used for system clock generation. A ceramic oscillator of 4.0MHz and capacitors are connected as shown in Fig. 13.

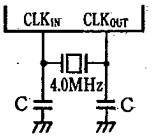


Fig. 13 System clock oscillation circuit

(13) $\overline{H_{SYNC}}$, $\overline{V_{SYNC}}$

$\overline{H_{SYNC}}$ and $\overline{V_{SYNC}}$ are input pins which receive the timing from TV set, etc. to set the position of display on the CRT. Square wave pulse with 0-5V amplitude corresponding to horizontal synchronizing signal and vertical synchronizing signal is input to $\overline{H_{SYNC}}$ and $\overline{V_{SYNC}}$ respectively. Input polarity is of Low level active.

(14) OSC_{IN}, OSC_{OUT}

OSC_{IN} and OSC_{OUT} external CR connection pins which generate clocks for CRT display.

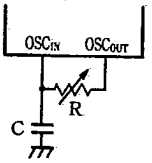


Fig. 14 CRT display oscillation circuit

(15) Standby Function

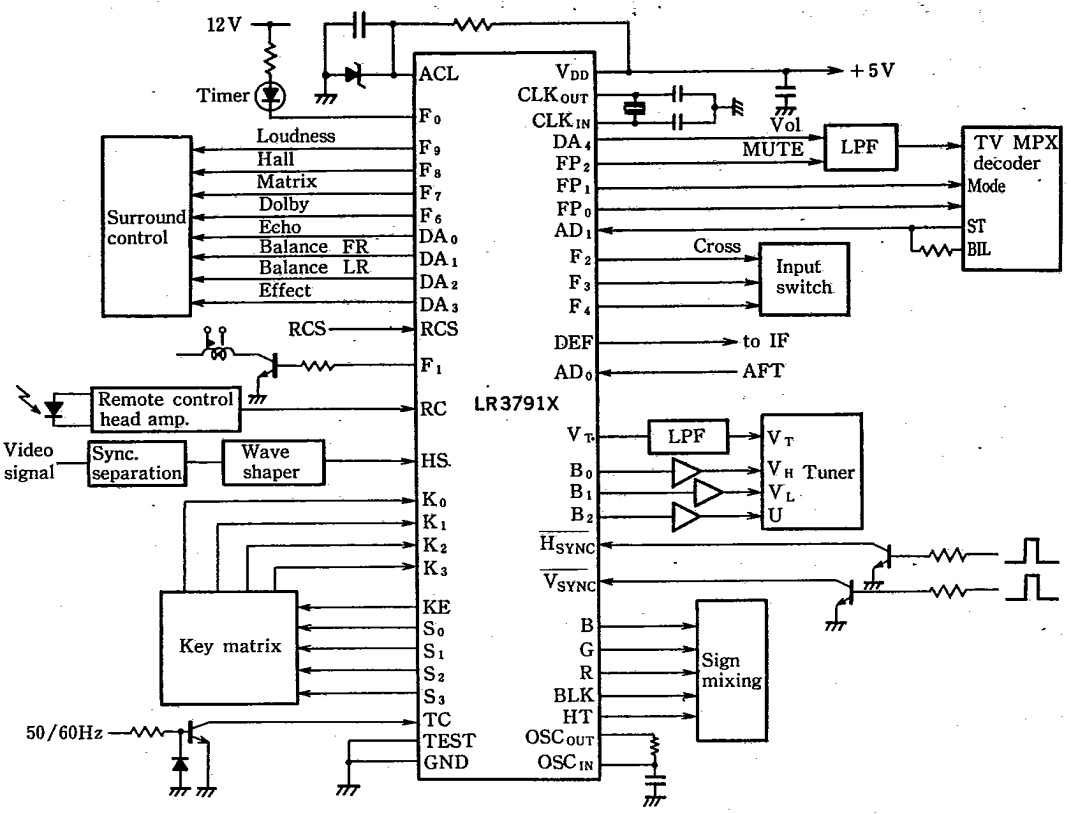
It is possible to enter into standby mode by executing an instruction in order to reduce current consumption, and then both system clock and CRT display clock are inactivated. In standby mode, control RAM, output latches the C flag and CRT display RAM remain operative.

Standby mode may be cleared with the F_I pin to go "Low" externally and in approximately 4ms after the system clock started oscillation. At this moment, the program counter is set at address 4 where the program restarts.

Note : That S_I pin can not be used as the output pin in the system where standby mode is used.

T-77-07-05

System Configuration Example



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