PUMA 68F64006X - 90/12/15

Issue 5.0 December 1999

Description

The PUMA 68F64006X is a 2M x 32 Flash Module housed in a 68 'J' Leaded Surface mount package with access times of 90, 120 and 150ns.

The Output width is user configurable as 8, 16 or 32 bits wide using 4 Chip Selects (/CS1~4) for optimum application flexibility.

The module incorporates Embedded Algorithms for Program and Erase with sector architecture and supports full chip erase.

The device also features hardware sector protection, which disables both program and erase operations in any of the 32 sectors on the module.

The device is available to commercial and industrial temperature grades.

Features

• Access times of 90, 120 and 150ns.

• 5V $\pm$ 10%.

• Commercial and Industrial temperature grades

• 68 'J' Leaded JEDEC surface mount package.

• Industry standard pinout.

• User configurable as 8/16/32 bits wide

• 64K Byte sector size.

• Operating Power   (32 Bit)   1.32W   (max)

• Low power standby.   (TTL)   22mW   (max)

• Completely Static Operation.

• 10,000 Write and Erase (W/E) Cycles.

• 10 Year Data Retention.

Package Details

Plastic 'J' Leaded JEDEC PLCC

Max. Dimensions (mm) - 25.27 x 25.27 x 5.08

Block Diagram
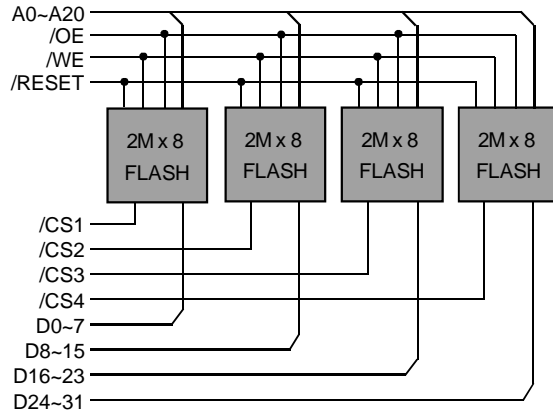
Pin Definition

See page 2.

Pin Functions

Description	Signal
Address Input	A0~A20
Data Input/Output	D0~D31
Chip Select	/CS1~4
Write Enable	/WE
Output Enable	/OE
Hardware Reset	/RESET
No Connect	NC
Power	V_{CC}
Ground	V_{SS}

Pin Definition - PUMA68F64006X

Pin	Signal	Pin	Signal
1	V_{CC}	35	V_{CC}
2	A19	36	A13
3	/CS1	37	A12
4	/CS2	38	A11
5	/CS3	39	A10
6	/CS4	40	A9
7	A17	41	A8
8	A18	42	A7
9	D16	43	D0
10	D17	44	D1
11	D18	45	D2
12	D19	46	D3
13	V_{SS}	47	V_{SS}
14	D20	48	D4
15	D21	49	D5
16	D22	50	D6
17	D23	51	D7
18	V_{CC}	52	V_{CC}
19	D24	53	D8
20	D25	54	D9
21	D26	55	D10
22	D27	56	D11
23	V_{SS}	57	V_{SS}
24	D28	58	D12
25	D29	59	D13
26	D30	60	D14
27	D31	61	D15
28	A6	62	A14
29	A5	63	A15
30	A4	64	A16
31	A3	65	/WE
32	A2	66	/OE
33	A1	67	/RESET
34	A0	68	A20

Absolute Maximum Ratings[(1)]

Parameter	Symbol	Min	Typ	Max	Unit
Voltage on any pin relative to V_{SS}	V_T	-2.0	-	+7.0	V
Supply Voltage[(2)]		-2.0	-	+7.0	V
Voltage on A9 relative to V_{SS}	V_{A9}	-2.0	-	+12.5	V
Storage Temperature	T_{STG}	-65	-	+125	^{O}C

Notes : (1) *Minimum DC Voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may overshoot V_{SS} to -2.0V for periods of up to 20ns . See Maximum DC Voltage on output and I/O pins is V_{cc}+0.5V. During Voltage transitions, outputs may overshoot to V_{cc}+2.0V for periods up to 20ns.*

(2) *Minimum DC input voltage on A9, OE#, RESET# pins is -0.5V. During voltage transitions, A9 ,OE# and RESET# pins may overshoot V_{ss} to -2.0V for periods of up to 20ns. Maximum DC Input voltage on A9, OE# and RESET# is 12.5V which may overshoot to 13.5V fo periods up to 20ns.*

(3) *No more than one output shorted at a time. Duration of a short circuit should not be greater than one second. Stresses Greater than those listed in this section may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

Parameter		Symbol	Min	Typ	Max	Unit	
Supply Voltage		V_{CC}	4.5	5.0	5.5	V	
Input High Voltage		V_{IH}	2.0	-	V_{CC}+0.5	V	
Input Low Voltage		V_{IL}	-0.5	-	0.8	V	
Operating Temperature	(Commercial)	T_A	0	-	70	^{O}C	
	(Industrial)	T_{AI}	-40	-	85	^{O}C	(I Suffix)

DC Electrical Characteristics

(V_{CC}=5V$\pm$10%, T_A=-40°C to 85°C)

Parameter		Symbol	Test Condition	Min	Typ	Max	Unit
Input Leakage Current Address, /OE		I_{LI1}	V_{CC}=V_{CC}max, V_{IN}=0V or V_{CC}	-	-	±4	μA
A9 Input Leakage Current		I_{LI2}	V_{CC}=V_{CC}max, A9=12.5V	-	-	200	μA
Other Pins		I_{LI3}	V_{CC}=V_{CC}max, V_{IN}=0V or V_{CC}	-	-	±4	μA
Output Leakage Current		I_{LO}	V_{CC}=V_{CC}max, V_{OUT}=0V or V_{CC}	-	-	±4	μA
V_{CC} Operating Current	32 Bit	I_{CCO32}	/CS[(1)]=V_{IL},/OE=V_{IH},I_{OUT}=0mA, f=6MHz	-	-	160	mA
	16 Bit	I_{CCO16}	As Above	-	-	82	mA
	8 Bit	I_{CCO8}	As Above	-	-	43	mA
V_{CC} Program Erase Current	32 Bit	I_{CCP32}	Programming In Progress	-	-	240	mA
	16 Bit	I_{CCP16}	As Above	-	-	122	mA
	8 Bit	I_{CCP8}	As Above	-	-	63	mA
Standby Supply Current	TTL	I_{SB1}	V_{CC}=V_{CC}max,/CS=V_{IH}[(1)] /OE=V_{IH}	-	-	4	mA
Autoselect/Sector Protect Voltage		V_{ID}	V_{CC}=5.0V	11.5	-	12.5	V
Output Voltage Low		V_{OL}	I_{OL}=12mA, V_{CC} = V_{CC} Min	-	-	0.45	V
Output Voltage High		V_{OH1}	I_{OH}=-2.5mA, V_{CC} = V_{CC} Min	2.4	-	-	V
Low V_{CC} Lock-Out Voltage		V_{LKO}		3.2	-	4.2	V

Notes (1) */CS1~4 inputs operate simultaneously for 32 bit mode, in pairs for 16 bit mode and singly for 8 bit mode.*

Capacitance

$(V_{CC} = 5.0V, T_A = 25^{O}C, F=1MHz.)$

Parameter		Symbol	Test Condition	Min	Typ	Max	Unit
Input Capacitance	(Address, /OE, /WE)	C_{IN1}	$V_{IN}=0V$	-	-	35	pF
	Other Pins	C_{IN2}	$V_{IN}=0V$	-	-	17	pF
Output Capacitance	32 bit mode	C_{OUT}	$V_{OUT}=0V$	-	-	40	pF

Note : These Parameters are calculated not measured.

Test Conditions

- Input pulse levels : 0.45V to 2.40V
- Input rise and fall times : 20ns
- Input and Output timing reference levels : 1.5V
- Output Load : See Load Diagram.
- Module tested in 32 bit mode.
- $V_{CC} = 5V\pm10\%$

Output Load

I/O Pin 166Ω

1.76V

30pF
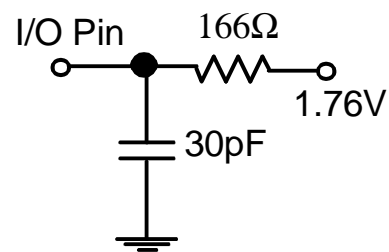
Read Cycle

Parameter	Symbol	90		120		150		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	90	-	120	-	150	-	ns
Address to Output Delay	t_{ACC}	-	90	-	120	-	150	ns
Chip Select to Output	t_{CS}	-	90	-	120	-	150	ns
Output Enable to Output	t_{OE}	-	40	-	50	-	55	ns
Output Enable to Output High Z	t_{DF}	-	20	-	30	-	35	ns
Output Hold From Address /CS or /OE whichever occurs first	t_{OH}	0	-	0	-	0	-	ns
/RESET Pin Low to Read	t_{READY}	-	20	-	20	-	20	μs

Erase/Program

Parameter	Symbol	90			120			150			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ.	Max	
Write Cycle Time	t_{WC}	90	-	-	120	-	-	150	-	-	ns
Address Setup Time	t_{AS}	0	-	-	0	-	-	0	-	-	ns
Address Hold Time	t_{AH}	45	-	-	50	-	-	50	-	-	ns
Data Setup Time	t_{DS}	45	-	-	50	-	-	50	-	-	ns
Data Hold Time	t_{DH}	0	-	-	0	-	-	0	-	-	ns
Read Recover before Write	t_{GHWL}	0	-	-	0	-	-	0	-	-	ns
/CS Setup Time	t_{CS}	0	-	-	0	-	-	0	-	-	ns
/CS Hold Time	t_{CH}	0	-	-	0	-	-	0	-	-	ns
/WE Pulse Width	t_{WP}	45	-	-	50	-	-	50	-	-	ns
/WE Pulse Width High	t_{WPH}	20	-	-	20	-	-	20	-	-	ns
Programming Operation[2]	t_{WHWH1}	-	7	-	-	7	-	-	7	-	μs
Sector Erase Operation[2]	t_{WHWH2}	-	-	8	-	-	8	-	-	8	s
V_{CC} Setup Time	t_{VCS}	50	-	-	50	-	-	50	-	-	μs

Notes : (1) This does not include the preprogramming time.
(2) Not 100% tested.

Erase/Program Alternate /CS controlled Writes

| Parameter	Symbol	90 Min	90 Typ	90 Max	120 Min	120 Typ	120 Max	150 Min	150 Typ.	150 Max	Units
Write Cycle Time	t_{WC}	90	-	-	120	-	-	150	-	-	ns
Address Setup Time	t_{AS}	0	-	-	0	-	-	0	-	-	ns
Address Hold Time	t_{AH}	45	-	-	50	-	-	50	-	-	ns
Data Setup Time	t_{DS}	45	-	-	50	-	-	50	-	-	ns
Data Hold Time	t_{DH}	0	-	-	0	-	-	0	-	-	ns
Read Recover before Write	t_{GHEL}	0	-	-	0	-	-	0	-	-	ns
/CS Setup Time	t_{WS}	0	-	-	0	-	-	0	-	-	ns
/CS Hold Time	t_{WH}	0	-	-	0	-	-	0	-	-	ns
/WE Pulse Width	t_{CP}	45	-	-	50	-	-	50	-	-	ns
/WE Pulse Width High	t_{CPH}	20	-	-	20	-	-	20	-	-	ns
Programming Operation[2]	t_{WHWH1}	-	7	-	-	7	-	-	7	-	µs
Sector Erase Operation[2]	t_{WHWH2}	-	-	8	-	-	8	-	-	8	s

Notes : (1) *This does not include the preprogramming time.*
(2) *Not 100% tested.*

Hardware Reset (/RESET)

Parameter JEDEC	Parameter Std	Description	Test Setup	All Speed Options	Unit
	t_{READY}	/RESET Pin Low (NOT During Embedded Algorithms) to Read or Write*	Max	20	µs
	t_{RP}	/RESET# Pulse Width	Min	500	ns
	t_{RH}	/RESET# High Time before Read*	Min	50	ns

Note : Not 100% tested
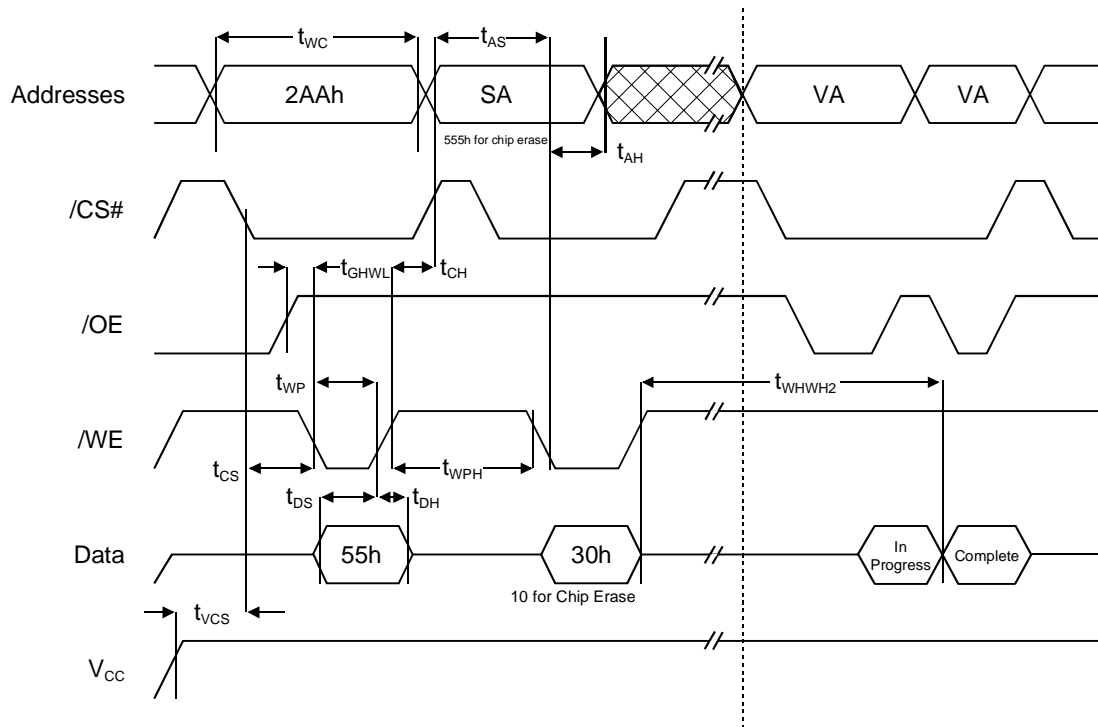
Read Operation Timings
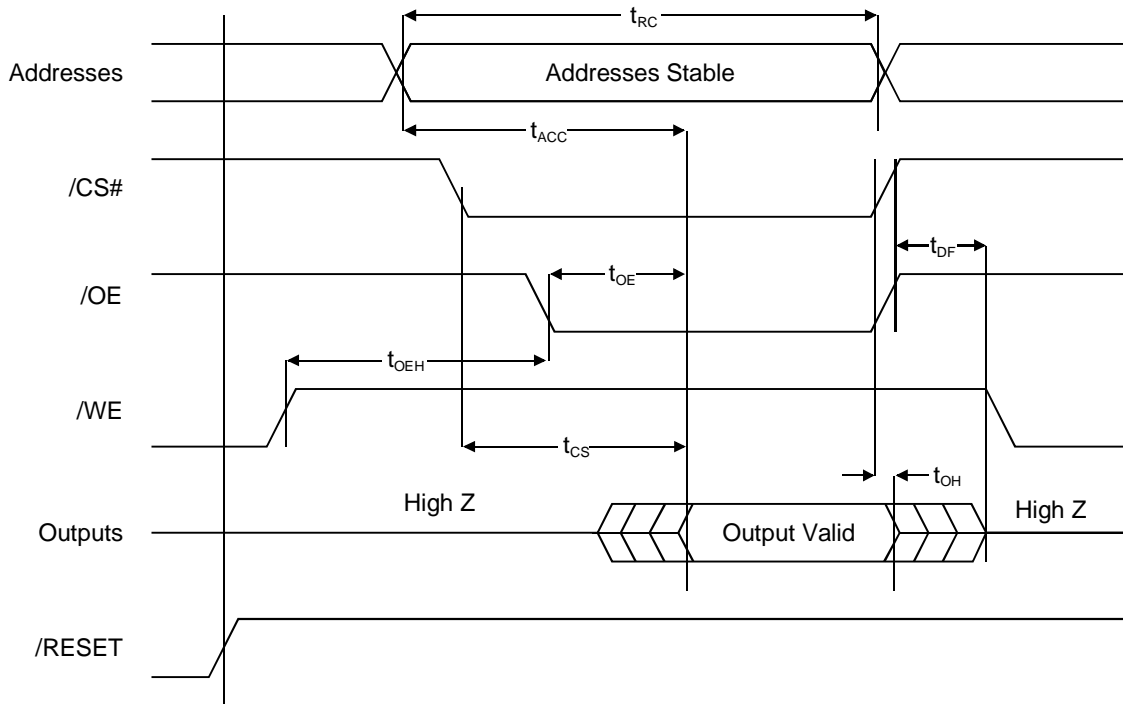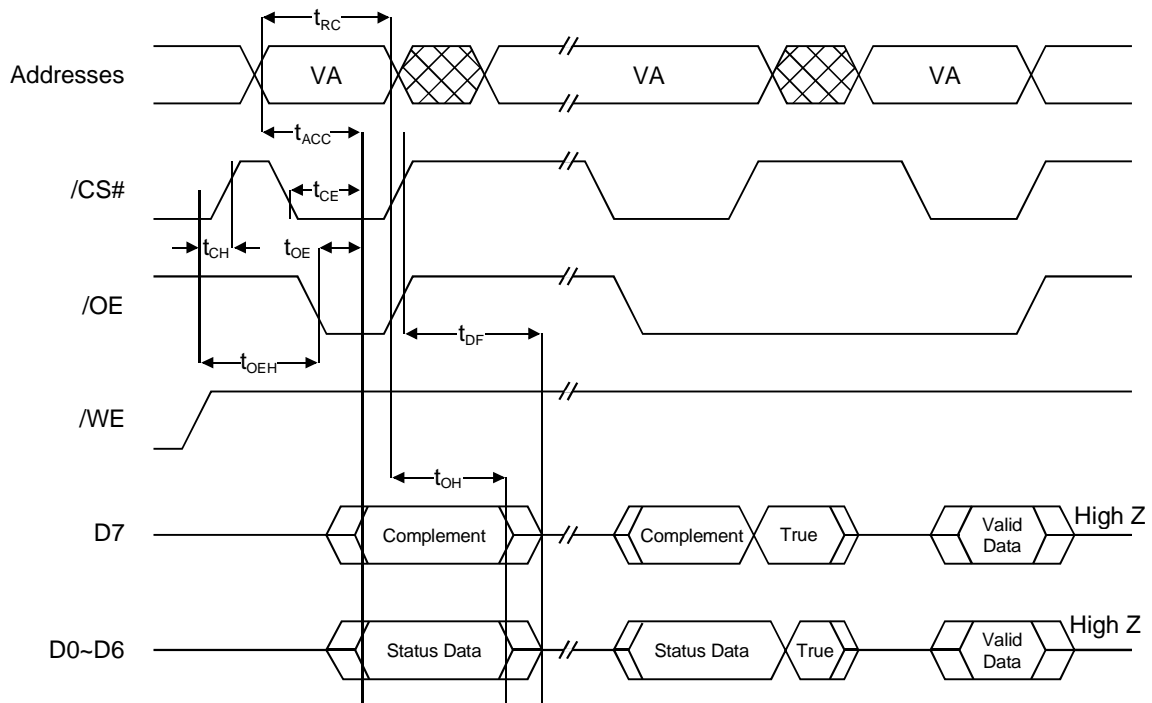

Program Operation Timings
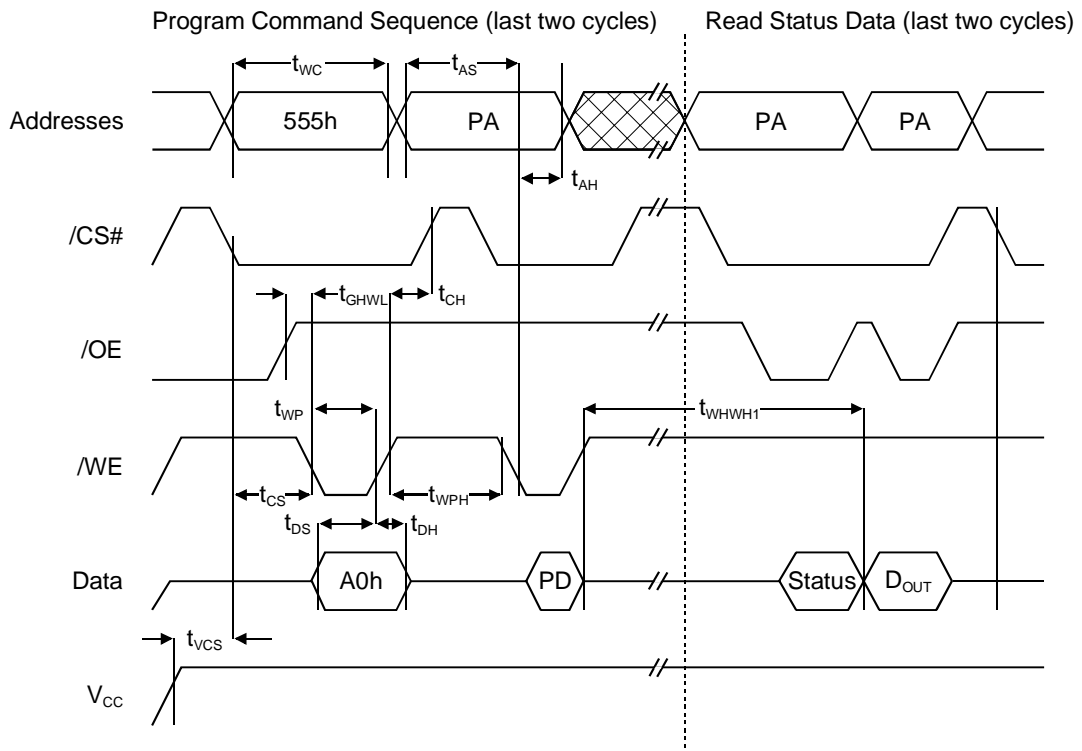
Note : PA = program address, PD = Program data, D_{OUT} is the true data at the program address

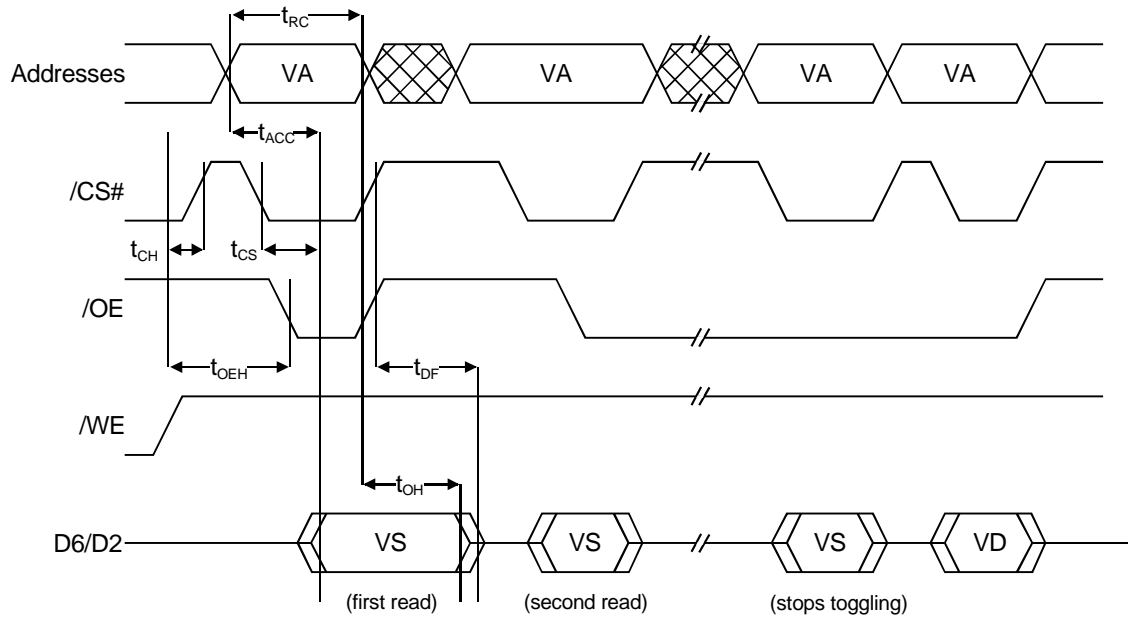## Chip/Sector Erase Operation Timings.

Note : SA=Sector Address. VA=Valid Address for reading status data.

Data# Polling Timings (During Embedded Algorithms)

Note :
VA = Valid Address. Illustration shows first status cycle after command sequence,
last status read cycle, and array data read cycle.

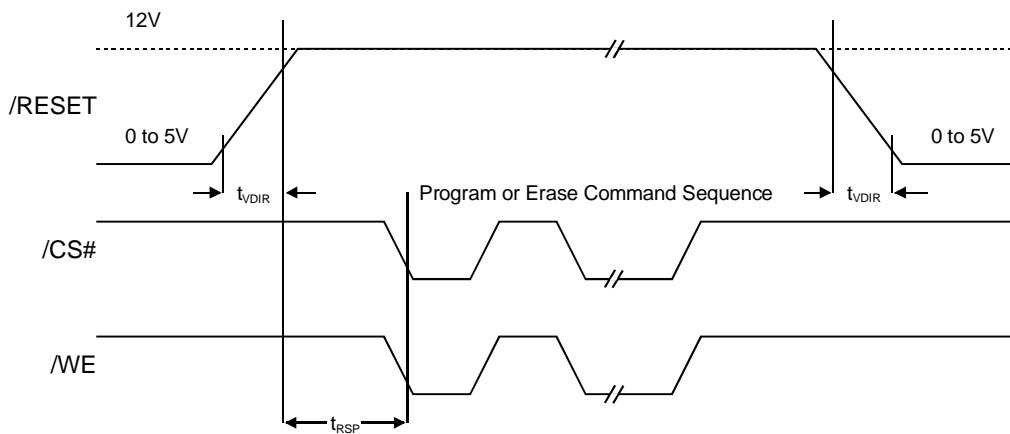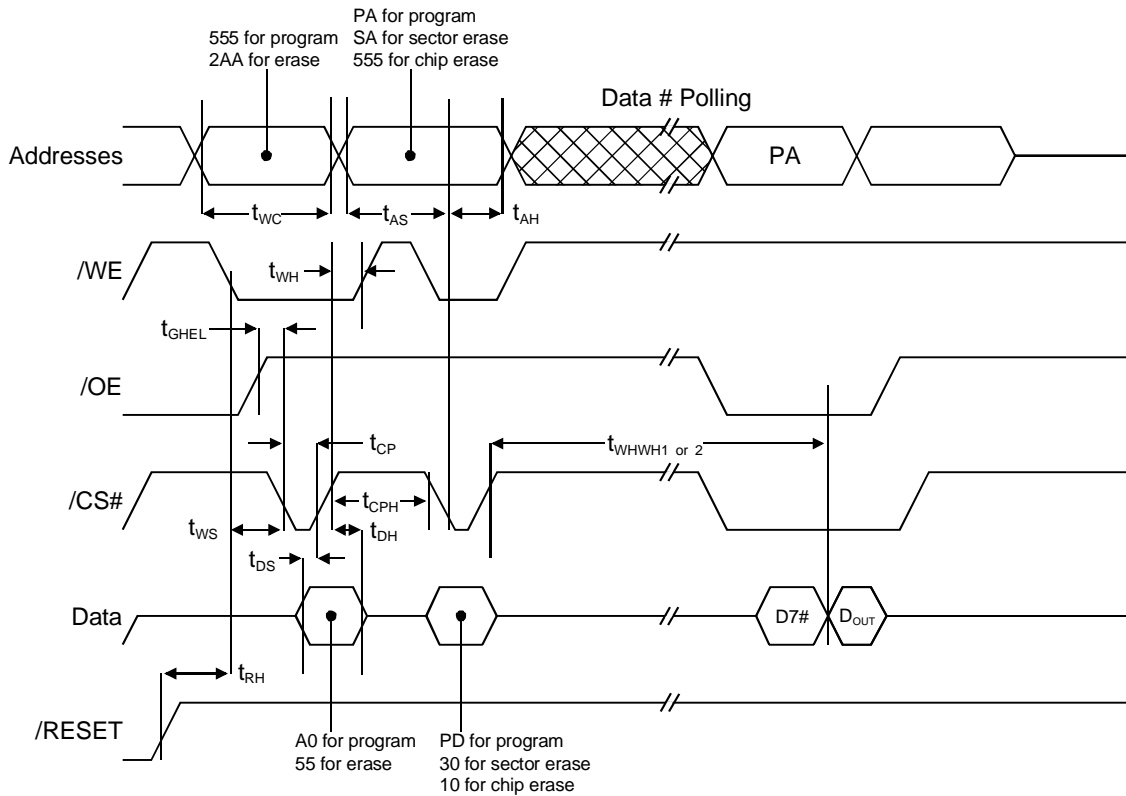## Toggle Bit Timings (During Embedded Algorithms)

Note :
VA=Valid Address; not required for D6. Illustration shows first two status cycle after
command sequence, last status read cycle, and array data read cycle.
VS=Valid Status, VD=Valid Data.
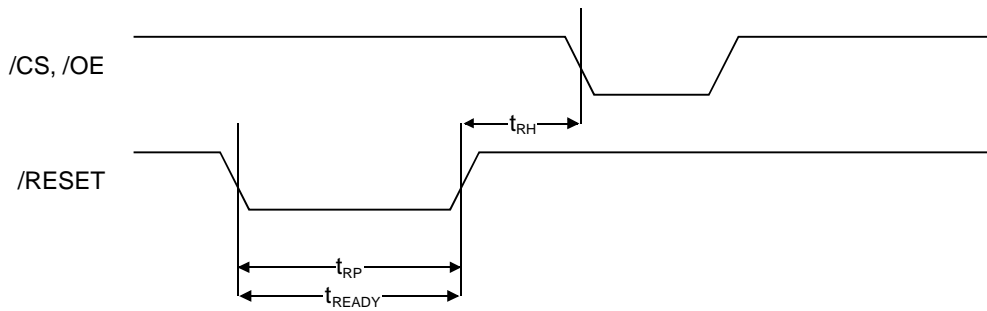
Temporary Sector Group Timings

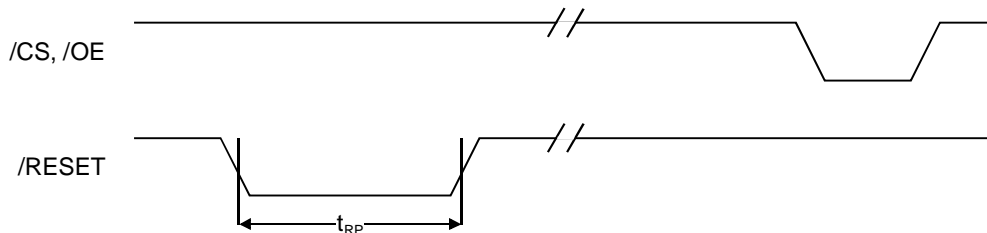## Alternate /CS# Controlled Write Operation Timings

Notes:
1. PA =Program Address, PD=Program Data, SA=Sector Address,
   D7#=Compliment of Data Input, D_{OUT}=Array Data.
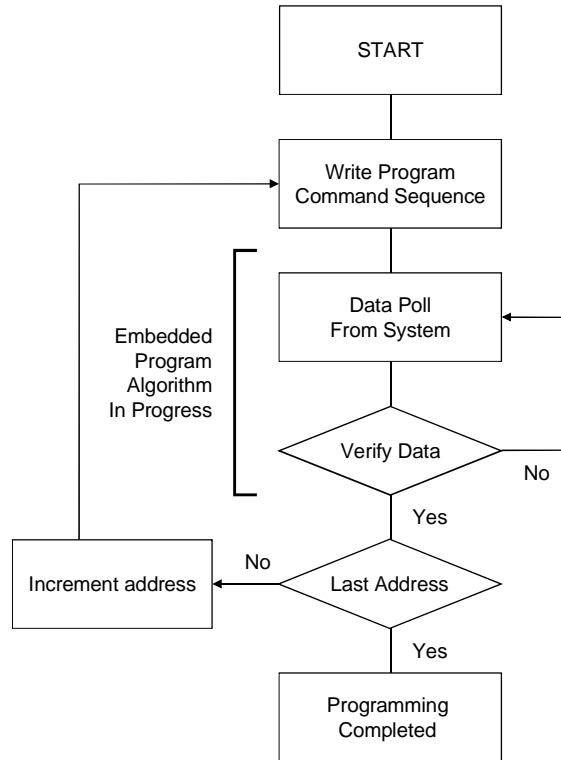2. Figure indicates the last two bus cycles of the command sequence.

/RESET Timings

Reset Timings NOT during Embedded Algorithms

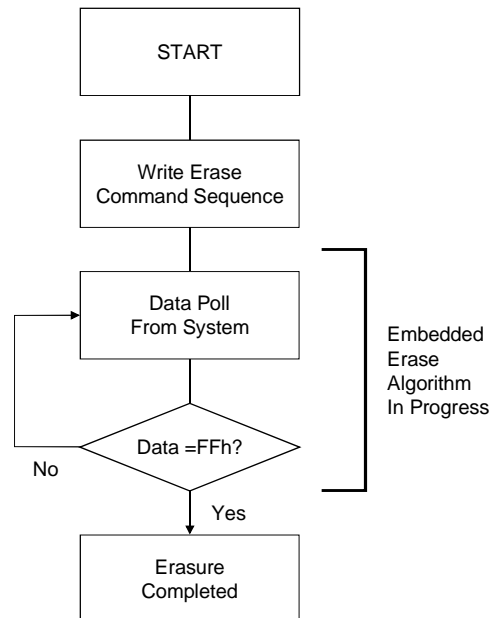*Reset Timings during Embedded Algorithms*

Program Operation

```
                    ┌─────────────┐
                    │    START    │
                    └─────────────┘
                           │
                           ▼
                 ┌───────────────────┐
                 │   Write Program   │◄──────┐
                 │ Command Sequence  │       │
                 └───────────────────┘       │
                           │                 │
    Embedded               ▼                 │
    Program          ┌─────────────┐         │
    Algorithm        │  Data Poll  │◄──┐     │
    In Progress      │ From System │   │     │
                     └─────────────┘   │     │
                           │           │     │
                           ▼           │     │
                     ◇─────────────◇   │     │
                     ◇ Verify Data ◇───┘     │
                     ◇─────────────◇  No     │
                           │ Yes             │
                           ▼                 │
  ┌──────────────┐  No  ◇─────────────◇      │
  │  Increment   │◄─────◇ Last Address◇      │
  │   address    │      ◇─────────────◇      │
  └──────────────┘            │ Yes          │
         └───────────────────────────────────┘
                              ▼
                      ┌───────────────┐
                      │  Programming  │
                      │   Completed   │
                      └───────────────┘
```

Note :
See the appropriate Command definitions table for program command sequence

Erase Operation

```
                    ┌─────────────┐
                    │    START    │
                    └─────────────┘
                           │
                           ▼
                 ┌───────────────────┐
                 │   Write Erase     │
                 │ Command Sequence  │
                 └───────────────────┘
                           │
                           ▼
                 ┌─────────────┐            Embedded
            ┌───►│  Data Poll  │            Erase
            │    │ From System │            Algorithm
            │    └─────────────┘            In Progress
            │          │
            │          ▼
            │    ◇─────────────◇
            └────◇  Data =FFh? ◇
            No   ◇─────────────◇
                       │ Yes
                       ▼
                ┌─────────────┐
                │   Erasure   │
                │  Completed  │
                └─────────────┘
```

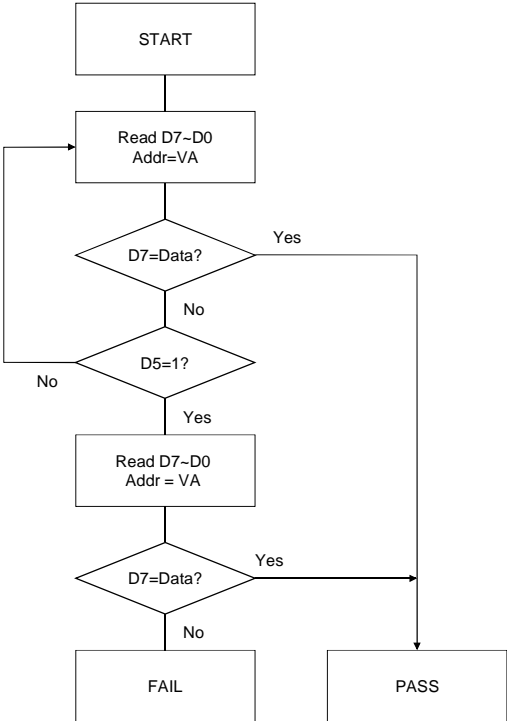Note :
1. See the appropriate Command definitions table for erase command sequence.
2. See 'D3 : Sector Erase Timer' For more information.

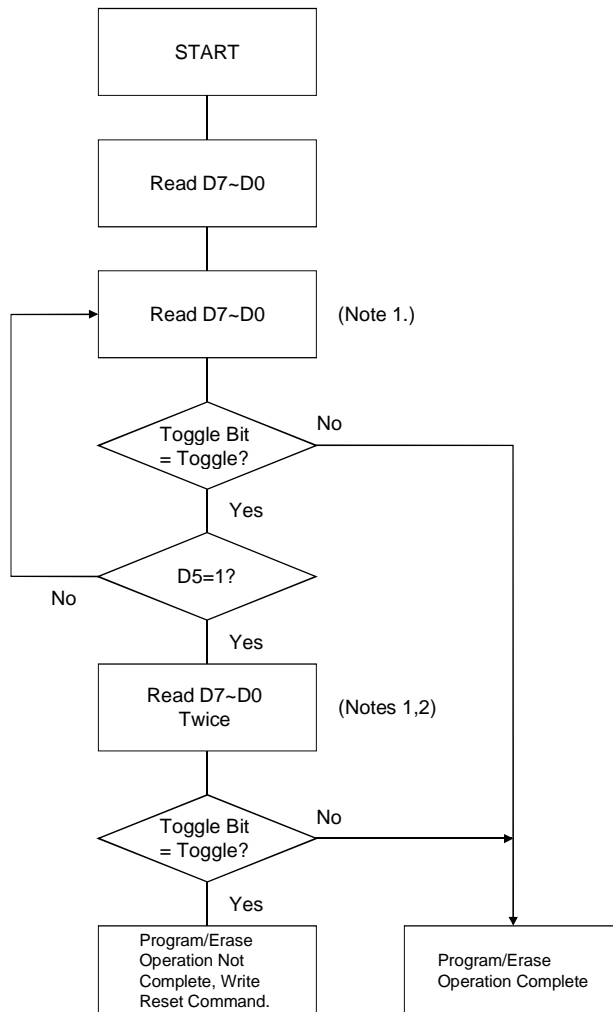## Temporary Sector Group Unprotect Operation

```
                    ┌─────────────────┐
                    │      START      │
                    └────────┬────────┘
                             │
                    ┌────────▼────────┐
                    │   /RESET=V_ID   │
                    │    (Note 1)     │
                    └────────┬────────┘
                             │
                    ┌────────▼────────┐
                    │ Perform Erase or│
                    │Program Operations│
                    └────────┬────────┘
                             │
                    ┌────────▼────────┐
                    │   /RESET=V_IH   │
                    └────────┬────────┘
                             │
                    ┌────────▼────────┐
                    │    Temporary    │
                    │Sector Group Unprotect│
                    │ Completed (Note 2)│
                    └─────────────────┘
```
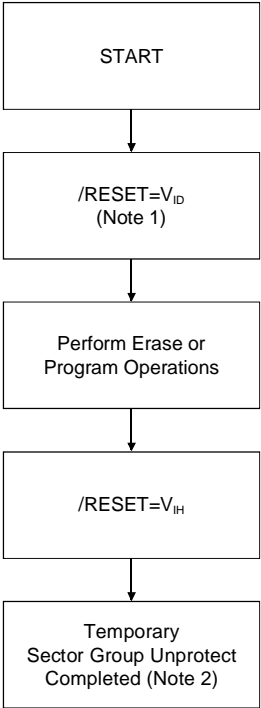
Notes:
1. All protected sector groups unprotected.
2. All previously protected sector groups are protected once again.

Data# Polling Operation

```
                    ┌─────────────────┐
                    │      START      │
                    └────────┬────────┘
                             │
                    ┌────────▼────────┐
              ┌────►│   Read D7~D0    │
              │     │    Addr=VA      │
              │     └────────┬────────┘
              │              │
              │          ◄ D7=Data? ►──── Yes ────┐
              │              │ No                  │
              │              │                     │
              │ No       ◄ D5=1? ►                 │
              └──────────────┤ Yes                 │
                             │                     │
                    ┌────────▼────────┐            │
                    │   Read D7~D0    │            │
                    │    Addr = VA    │            │
                    └────────┬────────┘            │
                             │                     │
                         ◄ D7=Data? ►── Yes ───────┤
                             │ No                  │
                    ┌────────▼────────┐   ┌────────▼────────┐
                    │      FAIL       │   │      PASS       │
                    └─────────────────┘   └─────────────────┘
```

Note :
1. VA = Valid Address for programming. During a sector erase operartion, a valid adddress
   is an address within any sector selected for erasure. During chip erase, a valid address is
   any non-protected sector address.
2. D7 should be rechecked even if D5 = '1' beceause D7 may change simultaneously
   with D5.

Toggle Bit Algorithm

```
                    ┌─────────────┐
                    │    START    │
                    └──────┬──────┘
                           │
                    ┌──────┴──────┐
                    │  Read D7~D0 │
                    └──────┬──────┘
                           │
                    ┌──────┴──────┐
         ┌─────────▶│  Read D7~D0 │  (Note 1.)
         │          └──────┬──────┘
         │                 │
         │            ╱────┴────╲        No
         │          ╱ Toggle Bit  ╲──────────────┐
         │          ╲ = Toggle?   ╱               │
         │            ╲────┬────╱                 │
         │                 │ Yes                  │
         │            ╱────┴────╲                 │
         │      No  ╱           ╲                 │
         └─────────╱   D5=1?     ╲                │
                    ╲           ╱                 │
                     ╲────┬────╱                  │
                          │ Yes                   │
                   ┌──────┴──────┐                │
                   │  Read D7~D0 │  (Notes 1,2)   │
                   │    Twice    │                │
                   └──────┬──────┘                │
                          │                       │
                     ╱────┴────╲        No        │
                   ╱ Toggle Bit  ╲─────────────▶  │
                   ╲ = Toggle?   ╱                │
                     ╲────┬────╱                  │
                          │ Yes                   │
                   ┌──────┴──────┐         ┌───────┴──────┐
                   │Program/Erase│         │Program/Erase │
                   │Operation Not│         │  Operation   │
                   │Complete,Write│        │  Complete    │
                   │Reset Command.│        └──────────────┘
                   └──────────────┘
```

Note :
1. Read Toggle bit twice to determine whether or not it is toggling. See text.
2. Recheck toggle bit because it may stop toggling as D5 changes to '1' . See text.

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register it self does not occupy any addressable memory location.The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. The appropriate device bus operations table lists the inputs and control levels required, and the resulting output. The following subsections describe each of these operations in further detail.

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the /CS# and /OE pins to V_{IL}. /CS# is the power control and selects the device. /OE is the output control and gates array data to the output pins. /WE should remain at V_{IH}.

The internal state machine is set for reading array data upon device power up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See "Reading Array Data" for more information. Refer to the AC Read Operations table for timing specifications and to the Read Operations Timings diagram for the timing waveforms. I_{CCO32}, I_{CCO16} and I_{CCO8} in the DC Characteristics table represents the active current specification for reading array data.

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive /WE and /CS# to V_{IL}, and /OE to V_{IH}. An erase operation can erase one sector, multiple sectors, or the entire device. The Sector Address Tables indicate the address space that each sector occupies. A "sector address" consists of the address bits required to uniquely select a sector. See the "Command Definitions" section for details on erasing a sector or the entire chip, or suspending/resuming the erase operation. After the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on D7~D0. Standard read cycle timings apply in this mode. Refer to the "Autoselect Mode" and "Autoselect Command Sequence" sections for more information. I_{CCP32}, I_{CCP16} and I_{CCP8} in the DC Characteristics table represents the active current specification for the write mode. The "AC Characteristics" section contains timing specification tables and timing diagrams for write operations.

Program and Erase Operation Status

During an erase or program operation, the system may check the status of the operation by reading the status bits on D7~D0. Standard read cycle timings and I_{CCO32}, I_{CCO16} and I_{CCO8} read specifications apply. Refer to "Write Operation Status" for more information, and to each AC Characteristics section for timing diagrams.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the /OE input.

The device enters the CMOS standby mode when /CS and /RESET pins are both held at $V_{CC} \pm 0.5$ V. (Note that this is a more restricted voltage range than V_{IH}.) The device enters the TTL standby mode when /CS# and /RESET pins are both held at V_{IH}. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

The device also enters the standby mode when the /RESET pin is driven low. Refer to the next section, "/RESET: Hardware Reset Pin".

If the device is deselected during erasure or program-ming, the device draws active current until the operation is completed.

In the DC Characteristics tables, I_{SB} represents the standby current specification.

/RESET: Hardware Reset Pin

The /RESET pin provides a hardware method of resetting the device to reading array data. When the system drives the /RESET pin low for at least a period of t_{RP}, the device **immediately terminates** any operation in progress, tristates all data output pins, and ignores all read/write attempts for the duration of the /RESET pulse. The device also resets the internal state ma-chine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When /RESET is held at V_{IL}, the device enters the TTL standby mode; if /RESET is held at $V_{SS} \pm 0.5$ V, the device enters the CMOS standby mode.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firm-ware from the Flash memory. The system can read data t_{RH} after the /RESET pin returns to V_{IH}.

Refer to the AC Characteristics tables for /RESET parameters and timing diagram.

Output Disable Mode

When the /OE input is at V_{IH} , output from the device is disabled. The output pins are placed in the high impedance state.

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on D7~D0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} (11.5 V to 12.5 V) on address pin A9. Address pins A6, A1, and A0 must be as shown in Autoselect Codes (High Voltage Method) table. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits. Refer to the corresponding Sector Address Tables. The Command Definitions table shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on D7~D0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in the Command Definitions table. This method does not require V_{ID} . See "Command Definitions" for details on using the autoselect mode.

Sector Group Protection/Unprotection

The hardware sector group protection feature disables both program and erase operations in any sector group. Each sector group consists of four adjacent sectors. Table 4 shows how the sectors are grouped, and the address range that each sector group contains. The hardware sector group unprotection feature re-enables both program and erase operations in previously protected sector groups. Sector group protection/unprotection must be implemented using programming equipment. The procedure requires a high voltage (V_{ID}) on address pin A9 and the control pins. The device is shipped with all sector groups unprotected. See "Autoselect Mode" for details.

Temporary Sector Group Unprotect

This feature allows temporary unprotection of previously protected sector groups to change data in-system. The Sector Group Unprotect mode is activated by setting the /RESET pin to V_{ID} . During this mode, formerly protected sector groups can be programmed or erased by selecting the sector group addresses. Once V_{ID} is removed from the /RESET pin, all the previously protected sector groups are protected again. Figure 1 shows the algorithm, and the Temporary Sector Group Unprotect diagram shows the timing waveforms, for this feature.

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to the Command Definitions table). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on /OE, /CS# or /WE do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of /OE = V_{IL}, /CS# = V_{IH} or /WE = V_{IH}. To initiate a write cycle, /CS# and /WE must be a logical zero while /OE is a logical one.

Power-Up Write Inhibit

If /WE = /CS# = V_{IL} and /OE = V_{IH} during power up, the device does not accept commands on the rising edge of /WE. The internal state machine is automatically reset to reading array data on power-up.

Writing specific address and data commands or sequences into the command register initiates device operations. The Command Definitions table defines the valid register command sequences. Writing **incorrect address and data values** or writing them in the **improper sequence** resets the device to reading array data.

All addresses are latched on the falling edge of /WE or /CS#, whichever happens later. All data is latched on the rising edge of /WE or /CS#, whichever happens first. Refer to the appropriate timing diagrams in the "AC Characteristics" section.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See "Erase Suspend/Erase Resume Commands" for more information on this mode.

The system *must* issue the reset command to re-enable the device for reading array data if D5 goes high, or while in the autoselect mode. See the "Reset Command" section, next.

See also "Requirements for Reading Array Data" in the "Device Bus Operations" section for more information. The Read Operations table provides the read parame-ters, and Read Operation Timings diagram shows the timing diagram.

Reset Command

Writing the reset command to the device resets the device to reading array data. Address bits are don't care for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command *must* be written to return to reading array data (also applies to autoselect during Erase Suspend).

If D5 goes high during a program or erase operation, writing the reset command returns the device to read-ing array data (also applies during Erase Suspend).

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and devices codes, and determine whether or not a sector is protected. The Command Definitions table shows the address and data requirements. This method is an alternative to that shown in the Autoselect Codes (High Voltage Method) table, which is intended for PROM programmers and requires V_{ID} on address bit A9.

The autoselect command sequence is initiated by writing two unlock cycles, followed by the autoselect command. The device then enters the autoselect mode, and the system may read at any address any number of times, without initiating another command sequence.

A read cycle at address XX00h retrieves the manufacturer code. A read cycle at address XX01h returns the device code. A read cycle containing a sector address (SA) and the address 02h in returns 01h if that sector is protected, or 00h if it is unprotected. Refer to the Sector Address tables for valid sector addresses.

The system must write the reset command to exit the autoselect mode and return to reading array data.

Byte Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically provides internally generated program pulses and verify the programmed cell margin. The Command Definitions take shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using D7 or D6. See "Write Operation Status" for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the programming operation. The program command sequence should be reinitiated once the device has reset to reading array data, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from a "0" back to a "1".** Attempting to do so may halt the operation and set D5 to "1", or cause the Data# Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still "0". Only erase operations can convert a "0" to a "1".

Chip Erase Command Sequence

Chip erase is a six-bus-cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. The Command Definitions table shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Embedded Erase algorithm are ignored. Note that a **hardware reset** during the chip erase operation immediately terminates the operation. The Chip Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

The system can determine the status of the erase operation by using D7, D6 or D2. See "Write Operation Status" for information on these status bits. When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Figure 3 illustrates the algorithm for the erase operation. See the Erase/Program Operations tables in "AC Characteristics" for parameters, and to the Chip/Sector Erase Operation Timings for timing waveforms.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two un-lock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the

address of the sector to be erased, and the sector erase command. The Command Definitions table shows the address and data requirements for the sector erase command sequence. The device does not require the system to preprogram the memory prior to erase. The Embedded Erase algorithm automatically programs and verifies the sector for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. After the command sequence is written, a sector erase time-out of 50 μs begins. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 μs, otherwise the last address and command might not be accepted, and erasure may begin. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. If the time between additional sector erase commands can be assumed to be less than 50 μs, the system need not monitor D3.

Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to reading array data. The system must rewrite the command sequence and any additional sector addresses and commands.

The system can monitor D3 to determine if the sector erase timer has timed out. (See the "D3: Sector Erase Timer" section.) The time-out begins from the rising edge of the final /WE pulse in the command sequence.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. Note that a **hardware reset** during the sector erase operation immediately terminates the operation. The Sector Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using D7, D6 or D2. Refer to "Write Operation Status" for information on these status bits.

Figure 3 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations tables in the "AC Characteristics" section for parameters, and to the Sector Erase Operations Timing diagram for timing waveforms.

Erase Suspend/Erase Resume Commands

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. Writing the Erase Suspend command during the Sector Erase time-out immediately terminates the time-out period and suspends the erase operation. Addresses are "don't-cares" when writing the Erase Suspend command.

When the Erase Suspend command is written during a sector erase operation, the device requires a maximum of 20 µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the system can read array data from or program data to any sector not selected for erasure. (The device "erase suspends" all sectors selected for erasure.) Normal read and write timings and command definitions apply. Reading at any address within erase-suspended sectors produces status data on D7~D0. The system can use D7, or D6 and D2 together, to determine if a sector is actively erasing or is erase-suspended. See "Write Operation Status" for information on these status bits.

After an erase-suspended program operation is complete, the system can once again read array data within non-suspended sectors. The system can determine the status of the program operation using the D7 or D6 status bits, just as in the standard program operation. See "Write Operation Status" for more information.

The system may also write the autoselect command sequence when the device is in the Erase Suspend mode. The device allows reading autoselect codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation. See "Autoselect Command Sequence" for more information.

The system must write the Erase Resume command (address bits are "don't care") to exit the erase suspend mode and continue the sector erase operation. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the device has resumed erasing.

The device provides several bits to determine the status of a write operation: D2, D3, D5, D6 and D7. Table 6 and the following subsections describe the functions of these bits. D7 and D6 each offer a method for determining whether a program or erase operation is complete or in progress.

These three bits are discussed first.

D7: /Data Polling

The /Data Polling bit, D7, indicates to the host syst em whether an Embedded Algorithm is in progress or completed, or whether the device is in Erase Suspend. /Data Polling is valid after the rising edge of the final /WE pulse in the program or erase command sequence.

During the Embedded Program algorithm, the device outputs on D7 the complement of the datum programmed to D7. This D7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to D7. The system must provide the program address to read valid status information on D7. If a program address falls within a protected sector, /Data Polling on D7 is active for approximately 2 µs, then the device returns to reading array data.

During the Embedded Erase algorithm, /Data Polling produces a "0" on D7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, /Data Polling produces a "1" on D7. This is analogous to the complement/true datum output described for the Embedded Program algorithm: the erase function changes all the bits in a sector to "1"; prior to this, the device outputs the "complement," or "0." The system must provide an address within any of the sectors selected for erasure to read valid status information on D7.

After an erase command sequence is written, if all sectors selected for erasing are protected, /Data Polling on D7 is active for approximately 100 µs, then the device returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

When the system detects D7 has changed from the complement to true data, it can read valid data at D7~D0 on the following read cycles. This is because D7 may change asynchronously with D0~D6 while Output Enable (/OE) is asserted low. The /Data Polling Timings (During Embedded Algorithms) figure in the "AC Characteristics" section illustrates this. Table 6 shows the outputs for /Data Polling on D7. Figure 4 shows the /Data Polling algorithm.

D6: Toggle Bit I

Toggle Bit I on D6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final /WE pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause D6 to toggle. (The system may use either /OE or /CS to control the read cycles.) When the operation is complete, D6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, D6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use D6 and D2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), D6 toggles. When the device enters the Erase Suspend mode, D6 stops toggling. However, the system must also use D2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use D7 (see the subsection on "D7: /Data Polling").

If a program address falls within a protected sector, D6 toggles for approximately 2 µs after the program command sequence is written, then returns to reading array data.

D6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

The Write Operation Status table shows the outputs for Toggle Bit I on D6. Refer to Figure 5 for the toggle bit algorithm, and to the Toggle Bit Timings figure in the "AC Characteristics" section for the timing diagram. The D2 vs. D6 figure shows the differences between D2 and D6 in graphical form. See also the subsection on "D2: Toggle Bit II"

D2: Toggle Bit II

The "Toggle Bit II" on D2, when used with D6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit

II is valid after the rising edge of the final /WE pulse in the command sequence. D2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either /OE or /CS to control the read cycles.) But D2 cannot distinguish whether the sector is actively erasing or is erase-suspended. D6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information.

Refer to Table 6 to compare outputs for D2 and D6. Figure 5 shows the toggle bit algorithm in flowchart form, and the section "D2: Toggle Bit II" explains the algorithm. See also the "D6: Toggle Bit I" subsection. Refer to the Toggle Bit Timings figure for the toggle bit timing diagram. The D2 vs. D6 figure shows the differences between D2 and D6 in graphical form.

Reading Toggle Bits D6/D2

Refer to Figure 5 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read D7~D0 at least twice in a row to determine whether a toggle bit is toggling. Typically, a system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on D7~D0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of D5 is high (see the section on D5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped tog-gling just as D5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and D5 has not gone high. The system may continue to monitor the toggle bit and D5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 5).

D5: Exceeded Timing Limits

D5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions D5 produces a "1." This is a failure condition that indicates the program or erase cycle was not successfully completed.

The D5 failure condition may appear if the system tries to program a "1" to a location that is previously programmed to "0." **Only an erase operation can change a "0" back to a "1."** Under this condition, the device halts the operation, and when the operation has exceeded the timing limits, D5 produces a "1."

Under both these conditions, the system must issue the reset command to return the device to reading array data.

D3: Sector Erase Timer

After writing a sector erase command sequence, the system may read D3 to determine whether or not an erase operation has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the ti me-out is complete, D3 switches from "0" to "1." The system may ignore D3 if the system can guarantee that the time between additional sector erase commands will always be less than 50 µs. See also the "Sector Erase Command Sequence" section.

After the sector erase command sequence is written, the system should read the status on D7 (/Data Polling) or D6 (Toggle Bit I) to ensure the device has accepted the command sequence, and then read D3. If D3 is "1", the internally controlled erase cycle has begun; all further commands (other than Erase Suspend) are ignored until the erase operation is complete. If D3 is "0", the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of D3 prior to and following each subsequent sector erase command. If D3 is high on the second status check, the last command might not have been accepted. Table 6 shows the outputs for D3.

Table 1 : Device Bus Operations

Device Bus Operation						
Operation	CS#	OE#	WE#	RESET#	A0~A20	D0~D7
Read	L	L	H	H	A_{IN}	D_{OUT}
Write	L	H	L	H	A_{IN}	D_{IN}
CMOS Standby	$V_{CC}\pm0.5V$	X	X	$V_{CC}\pm0.5V$	X	High Z
TTL Standby	H	X	X	H	X	High Z
Output Disable	L	H	H	H	X	High Z
Hardware Reset	X	X	X	L	X	High Z
Temporary Sector Unprotect. [1]	X	X	X	V_{ID}	A_{IN}	D_{IN}

Legend : $L = Logic\ Low= V_{IL}$, $H = Logic\ High = V_{IH}$, $V_{ID} = 12.0\pm0.5V$, $X = Don't\ Care$, $D_{IN} = Data\ In$, $D_{OUT} = Data\ Out$, $A_{IN} = Address\ In$

Notes : See the sections on the Sector Group Protection and Temporary Sector Unprotect, for more information

Table 3 : Autoselect Codes

Autoselect Codes (High Voltage Method)											
Description	/CS#	/OE	/WE	A20 ~ A18	A17 ~ A10	A9	A8 ~ A7	A6	A5 ~ A2	A1	A0	D7~D0
Sector Group Protection Verification	L	L	H	Sector Group Address	X	V_{ID}	X	V_{IL}	X	V_{IH}	V_{IL}	01h (Protected)
												00h (Unprotected)

Legend : $L = Logic\ Low= V_{IL}$, $H = Logic\ High = V_{IH}$, $SA = Sector\ Address$, $X = Don't\ Care$.

Table 4 : Sector Group Addresses

Sector Group Addresses				
Sector Group	A20	A19	A18	Sectors
SGA0	0	0	0	SA0~SA3
SGA1	0	0	1	SA4~SA7
SGA2	0	1	0	SA8~SA11
SGA3	0	1	1	SA12~SA15
SGA4	1	0	0	SA16~SA19
SGA5	1	0	1	SA20~SA23
SGA6	1	1	0	SA24~SA27
SGA7	1	1	1	SA28~SA31

Table 2 : Sector Address Table

Sector	A20	A19	A18	A17	A16	Address Range
SA0	0	0	0	0	0	000000h~00FFFFh
SA1	0	0	0	0	1	010000h~01FFFFh
SA2	0	0	0	1	0	020000h~02FFFFh
SA3	0	0	0	1	1	030000h~03FFFFh
SA4	0	0	1	0	0	040000h~04FFFFh
SA5	0	0	1	0	1	050000h~05FFFFh
SA6	0	0	1	1	0	060000h~06FFFFh
SA7	0	0	1	1	1	070000h~07FFFFh
SA8	0	1	0	0	0	080000h~08FFFFh
SA9	0	1	0	0	1	090000h~09FFFFh
SA10	0	1	0	1	0	0A0000h~0AFFFFh
SA11	0	1	0	1	1	0B0000h~0BFFFFh
SA12	0	1	1	0	0	0C0000h~0CFFFFh
SA13	0	1	1	0	1	0D0000h~0DFFFFh
SA14	0	1	1	1	0	0E0000h~0EFFFFh
SA15	0	1	1	1	1	0F0000h~0FFFFFh
SA16	1	0	0	0	0	100000h~10FFFFh
SA17	1	0	0	0	1	110000h~11FFFFh
SA18	1	0	0	1	0	120000h~12FFFFh
SA19	1	0	0	1	1	130000h~13FFFFh
SA20	1	0	1	0	0	140000h~14FFFFh
SA21	1	0	1	0	1	150000h~15FFFFh
SA22	1	0	1	1	0	160000h~16FFFFh
SA23	1	0	1	1	1	170000h~17FFFFh
SA24	1	1	0	0	0	180000h~18FFFFh
SA25	1	1	0	0	1	190000h~19FFFFh
SA26	1	1	0	1	0	1A0000h~1AFFFFh
SA27	1	1	0	1	1	1B0000h~1BFFFFh
SA28	1	1	1	0	0	1C0000h~1CFFFFh
SA29	1	1	1	0	1	1D0000h~1DFFFFh
SA30	1	1	1	1	0	1E0000h~1EFFFFh
SA31	1	1	1	1	1	1F0000h~1FFFFFh

Note : All sectors are 64Kbyte in size.

Table 5 : Command Definitions

Command Sequence[1]		Cycles	Bus Cycles [2~4]											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read[5]		1	RA	RD										
Reset[6]		1	XXX	F0										
Autoselect[7]	SGP Verify[8]	4	555	AA	2AA	55	555	90	SGA X02	XX00				
										XX01				
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Erase Suspend[9]		1	XXX	B0										
Erase Resume[10]		1	XXX	30										

Legend:

  X = *Don't care*
 RA = *Address of the memory location to be read.*
 RD = *Data read from location RA during read operation.*
 PA = *Address of the memory location to be programmed. Addresses latch on the falling edge of the /WE or /CS# pulse, whichever happens later.*
 PD = *Data to be programmed at location PA. Data latches on the rising edge of /WE or /CS# pulse, whichever happens first.*
 SA = *Address of the sector to be verified (in autoselect mode) or erased. Address bits A20–A16 select a unique sector.*
SGA = *Address of the sector group to be verified. Address bits A20–A18 select a unique sector group.*
SGP = *Sector Group Protect.*

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except when reading array or autoselect data, all bus cycles are write operations.*
4. *Address bits A20–A11 are don't cares for unlock and command cycles, unless SA or PA required.*
5. *No unlock or command cycles required when reading array data.*
6. *The Reset command is required to return to reading array data when device is in the autoselect mode, or if D5 goes high (while the device is providing status data).*
7. *The fourth cycle of the autoselect command sequence is a read cycle.*
8. *The data is 00h for an unprotected sector group and 01h for a protected sector group. See "Autoselect Command Sequence" for more information.*
9. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.*
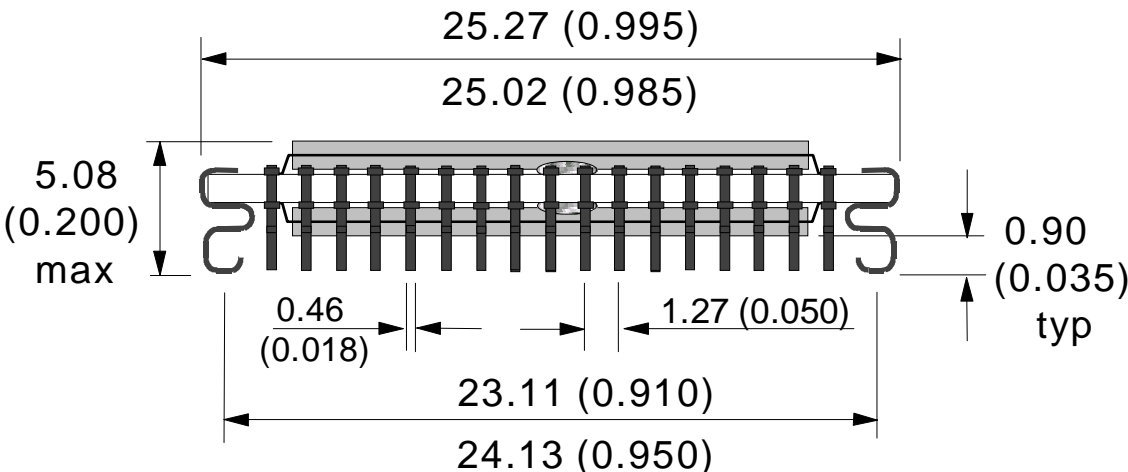10. *The Erase Resume command is valid only during the Erase Suspend mode.*
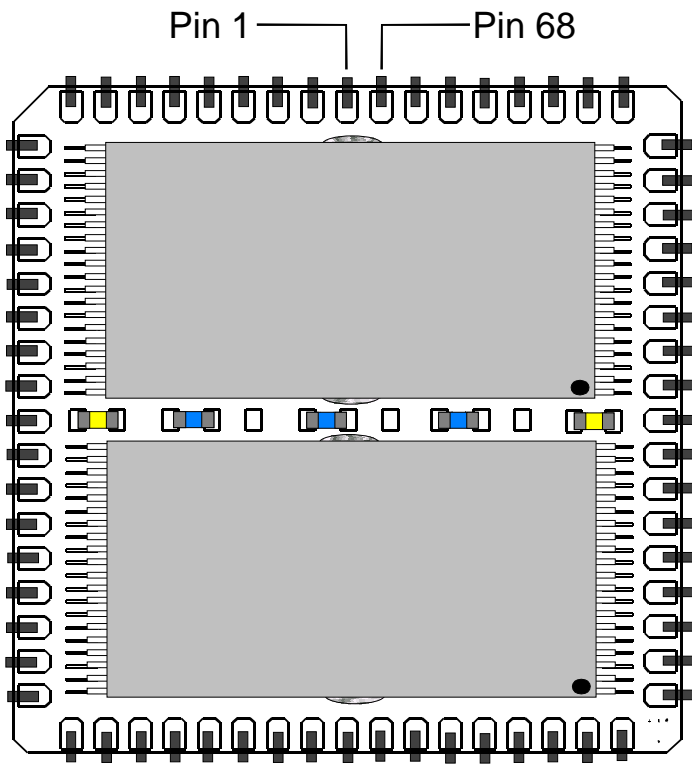
Table 6 : Write Operation Status

	Operation	D7[1]	D6	D5[2]	D3	D2[1]	RY/BY#
Standard Mode	Embedded Program Algorithm	D7#	Toggle	0	N/A	No Toggle	0
	Embedded Erase Algorithm	0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Reading Within Erase Suspended Sector	1	No Toggle	0	N/A	Toggle	1
	Reading Within Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
	Erase-Suspend-Program	D7#	Toggle	0	N/A	N/A	0

Notes:

1. *D7 and D2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*
2. *D5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. See "D5: Exceeded Timing Limits" for more information.*

PUMA 68 pin JEDEC Surface Mounted PLCC

Pin 1 ——————— Pin 68

25.27 (0.995)
25.02 (0.985)

5.08
(0.200)
max

0.90
(0.035)
typ

0.46
(0.018)

1.27 (0.050)

23.11 (0.910)
24.13 (0.950)

Co Planarity

Specified as +/- 2 thou max.

Visual Inspection Standard

All devices inspected to ANSI 2 standard

Moisture Sensitivity

Devices are **moisture sensitive.**

Shelf Life in Sealed Bag 12 months at <40°C and <90% relative humidity (RH).

After this bag has been opened, devices that will be subjected to infrared reflow, vapour phase reflow, or equivalent processing (peak package body temp 220°C) **must be** :

A : Mounted within 72 Hours at factory conditions of <30°C/60% RH

OR

B : Stored at <20% RH

If these conditions are not met or indicator card is >20% when read at 23°C +/-5% devices **require baking** as specified below.

If baking is required, devices may be baked for :-

A : 24 hours at 125°C +/-5% for high temperature device containers

OR

B : 192 hours at 40°C +5°C/-0°C and <5% RH for low temperature device containers**.**

Packaging Standard

Devices packaged in dry nitrogen, JED-STD-020.

Packaged in trays as standard.

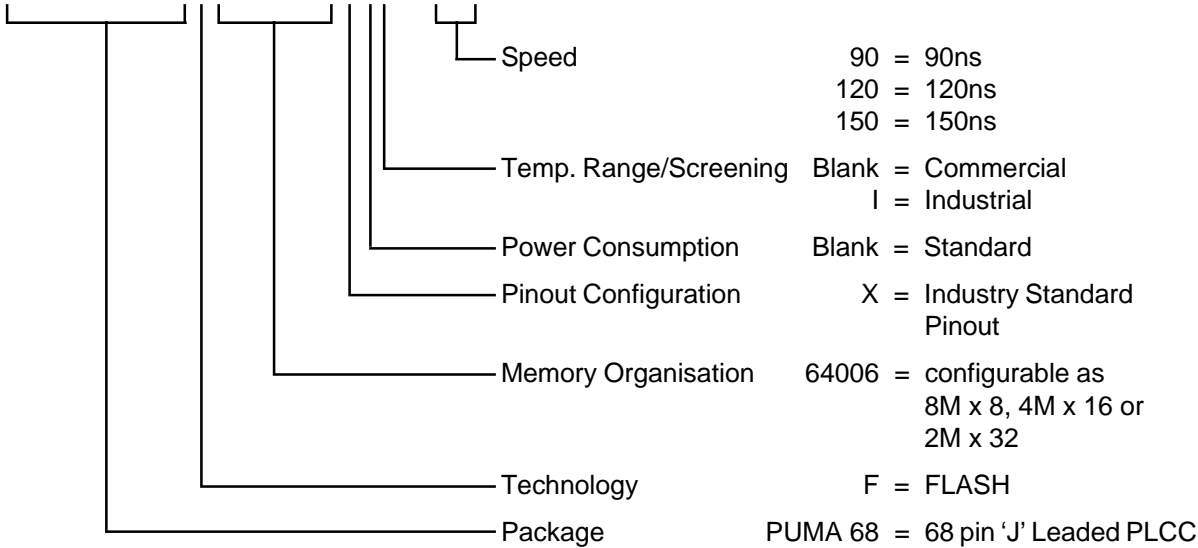Tape and reel available for shipment quantities exceeding 200pcs upon request.

Soldering Recomendations

IR/Convection -	Ramp Rate	6°C/sec max.
	Temp. exceeding 183°C	150 secs. max.
	Peak Temperature	225°C
	Time within 5°C of peak	20 secs max.
	Ramp down	6°C/sec max.
Vapour Phase -	Ramp up rate	6°C/sec max.
	Peak Temperature	215 - 219°C
	Time within 5°C of peak	60 secs max.
	Ramp down	6°C/sec max.

Note :   The above recomendations are based on standard industry practice. Failiure to comply with the above recomendations invalidates product warranty.

Ordering Information

PUMA 68F64006X I - 90

Speed	90 =	90ns
	120 =	120ns
	150 =	150ns
Temp. Range/Screening	Blank =	Commercial
	I =	Industrial
Power Consumption	Blank =	Standard
Pinout Configuration	X =	Industry Standard Pinout
Memory Organisation	64006 =	configurable as 8M x 8, 4M x 16 or 2M x 32
Technology	F =	FLASH
Package	PUMA 68 =	68 pin 'J' Leaded PLCC

Note :

Although this data is believed to be accurate the information contained herein is not intended to and does not create any warranty of merchantibility or fitness for a particular purpose.

Our products are subject to a constant process of development. Data may be changed without notice.

Products are not authorised for use as critical components in life support devices without the express written approval of a company director.