# SYVANTEK

# SYC16C450
## ASYNCHRONOUS COMMUNICATIONS ELEMENT

## FEATURES

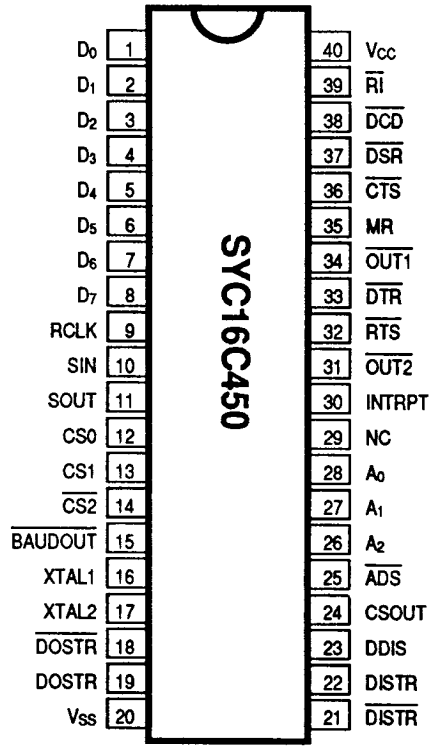
- High performance CMOS.
- Single +5 volt power supply.
- Adds or deletes standard asynchronous communication bits (start, stop, and parity) to or from serial data stream.
- Independently controlled transmit, receive, line status, and data set interrupts.
- Programmable baud generator allows division of any input clock by 1 to $(2^{16}-1)$ and generates the internal 16 x clock.
- Full double buffering eliminates need for precise synchronization.
- Independent receiver clock input.
- Complete status reporting capabilities.
- False start bit detection.
- MODEM control functions ($\overline{CTS}$, $\overline{RTS}$, $\overline{DSR}$, $\overline{DTR}$, $\overline{RI}$, and $\overline{DCD}$).
- Fully programmable serial-interface characteristics:
  —5-, 6-, 7-, or 8-bit characters.
  —Even, odd, or no-parity bit generation and detection.
  —1-, 1½-, or 2-stop bit generation.
  —Baud generation (DC to 56k baud).
- Line break generation and detection.
- Internal diagnostic capabilities:
  —Loopback controls for communications link fault isolation.
  —Break, parity, overrun, framing error simulation.
- Full prioritized interrupt system controls.
- All inputs and outputs are TTL compatible.
- Easily interface to most popular microprocessors.

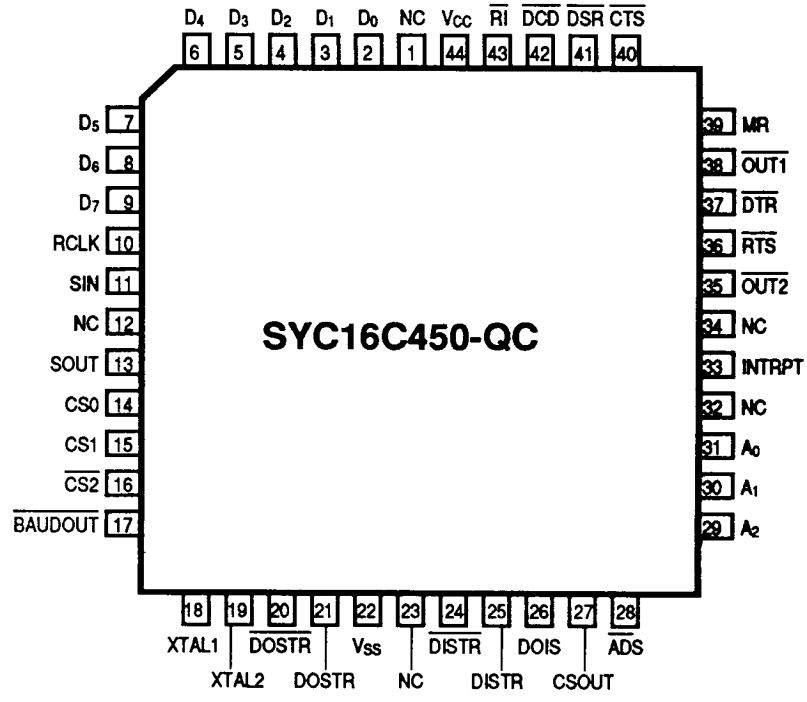
## GENERAL DESCRIPTION

The SYC16C450 is a programmable Asynchronous Communication Element (ACE) chip fabricated using high performance CMOS process. The SYC16C450 performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received from CPU. The complete status of the SYC16C450 can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the transfer operations being performed, and error conditions involving parity, overrun, framing or break interrupt.

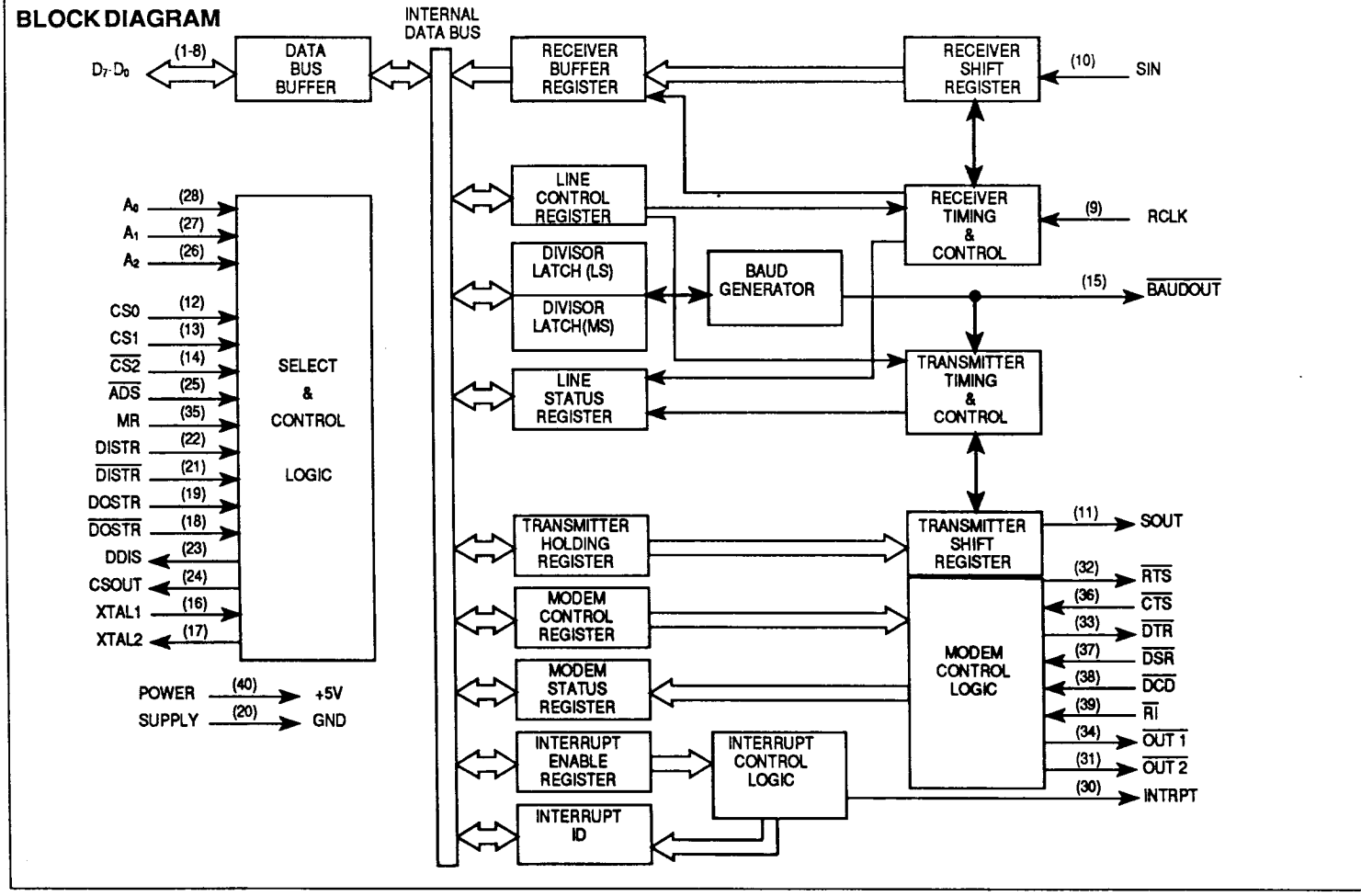
A programmable baud rate generator is included that can divide the timing reference clock input by a divisor between 1 and $(2^{16}-1)$. Also included in the SYC16C450 is a complete MODEM-control capability, and a processor-interrupt system that may be software tailored to the user's requirement to minimize the computing required to handle the communications link.

### PIN DIAGRAMS



## BLOCK DIAGRAM




### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Ambient Temperature under Bias | $0^0$ C to $+70^0$ C |
| Storage Temperature | $-65^0$C to $+150^0$ C |
| Voltage on any I/O pin with Respect to Ground | -0.5V to +7.0V |
| Power Dissipation | 700mW |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated on the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**DC CHARACTERISTICS** TA = $0^0$C to + $70^0$C, VCC = 5 V ± 5%, VSS = O V, unless otherwise specified

| | | SYC16C450 | | | |
|---|---|---|---|---|---|
| Symbol | Parameter | Min | Max | Units | Conditions |
| VILX | Clock input LOW Voltage | -0.5 | 0.8 | V | |
| VIHX | Clock input HIGH Voltage | 2.0 | VCC | V | |
| VIL | Input LOW Voltage | -0.5 | 0.8 | V | |
| VIH | Input HIGH Voltage | 2.0 | VCC | V | |
| VOL | Output LOW Voltage | | 0.4 | V | IOL= 1.6 mA on all Note 1 |
| VOH | Output HIGH Voltage | 2.4 | | V | IOH = -1.0 mA Note 1 |
| ICC (Avg) | Average Power Supply Current (VCC) | | 20 | mA | VCC = 5.25 V, No loads on SIN, DSR, RLSD, CTS, DCD. RI = 2.0 V. All other inputs = 0.8 V. Baud rate generator at 4 MHz. Baud rate at 56K. |
| IIL | Input Leakage | | ± 10 | U A | VCC = 5.25 V, VSS = 0 V. All other pins floating. |
| ICL | Clock Leakage | | ± 10 | U A | VIN = 0 V, 5.25 V |
| IOZ | 3-state Leakage | | ± 20 | U A | VCC = 5.25 V, VSS = 0 V. VOUT = 0 V, 5.25 V 1) Chip deselected 2) Chip and write mode selected |
| VILMR | MR Schmitt VIL | | 0.8 | V | |
| VIHMR | MR Schmitt VIH | 2.0 | | V | |

## CAPACITANCE TA = 25$^0$C, f = 1.0 MHz, VCC = VSS = O V

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| CXTAL2 | Clock Input Capacitance | | 15 | 20 | pF | |
| CXTAL1 | Clock Output Capacitance | | 20 | 30 | pF | fc =1 MHz |
| CI | Input Capacitance | | 6 | 10 | pF | Unmeasured pins returned to VSS |
| CO | Output Capacitance | | 10 | 20 | pF | |

## AC CHARACTERISTICS TA = 0$^0$C to +70$^0$C, VCC = 5 V ± 5%, Note 5

| Symbol | Parameter | SYC16C450 Min | SYC16C450 Max | Units | Conditions |
|---|---|---|---|---|---|
| $t_{AW}$ | Address Strobe Width | 60 | | ns | |
| $t_{AS}$ | Address Setup Time | 60 | | ns | |
| $t_{AH}$ | Address Hold Time | 0 | | ns | |
| $t_{CS}$ | Chip Select Setup Time | 60 | | ns | |
| $t_{CH}$ | Chip Select Hold Time | 0 | | ns | |
| $t_{CSS}$ | Chip Select Output Delay From $\overline{ADS}$ | | | ns | |
| $t_{DID}$ | $\overline{DISTR}$/DISTR Delay From $\overline{ADS}$ | | | ns | |
| $t_{DIW}$ | $\overline{DISTR}$/DISTR Strobe Width | 125 | | ns | |
| $t_{RC}$ | Ready Cycle Delay | 175 | | ns | |
| RC | Ready Cycle = $t_{AR}(1) + t_{DIW} + t_{RC}$ | 360 | | ns | |
| $t_{DD}$ | $\overline{DISTR}$/DISTR to Driver Disable Delay | | 60 | ns | 100 pF load, Note 4 |
| $t_{DDD}$ | Delay from $\overline{DISTR}$/DISTR to Data | | 125 | ns | 100 pF load |
| $t_{HZ}$ | $\overline{DISTR}$/DISTR to Floating Data Delay | 0 | 100 | ns | 100 pF load, Note 4 |
| $t_{DOD}$ | $\overline{DOSTR}$/DOSTR delay from ADS | | | ns | |
| $t_{DOW}$ | $\overline{DOSTR}$/DOSTR Storbe Width | 100 | | ns | |
| $t_{WC}$ | Write Cycle Delay | 200 | | ns | |
| WC | Write Cycle = $t_{AW}$* + $t_{DOW}$ +$t_{WC}$ | 360 | | ns | |
| $t_{DS}$ | Data Setup Time | 40 | | ns | |
| $t_{DH}$ | Data Hold Time | 40 | | ns | |
| $t_{CSC}$* | Chip Select Output Delay from Select | | 100 | ns | 100 pF load |
| $t_{RA}$* | Address Hold Time from $\overline{DISTR}$/DISTR | 20 | | ns | Note 2 |
| $t_{RCS}$* | Chip Select Hold Time from $\overline{DISTR}$/DISTR | 20 | | ns | Note 2 |
| $t_{AR}$* | $\overline{DISTR}$/DISTR Delay from Address | 60 | | ns | Note 2 |
| $t_{CSR}$* | $\overline{DISTR}$/DISTR Delay from Chip Select | 50 | | ns | Note 2 |
| $t_{WA}$* | Address Hold Time from $\overline{DOSTR}$/DOSTR | 20 | | ns | Note 2 |
| $t_{WCS}$* | Chip Select Hold Time from $\overline{DOSTR}$/DOSTR | 20 | | ns | Note 2 |
| $t_{AW}$* | $\overline{DOSTR}$/DOSTR Delay from Address | 60 | | ns | Note 2 |
| $t_{CSW}$* | $\overline{DOSTR}$/DOSTR Delay from Select | 50 | | ns | Note 2 |
| $t_{MRW}$ | Master Reset Pulse Width | 5 | | µs | |
| $t_{XH}$ | Duration of Clock HIGH Pulse | 140 | | ns | |
| tXL | Duration of Clock LOW Pulse | 140 | | ns | External Clock (3.1 MHz Max.) |

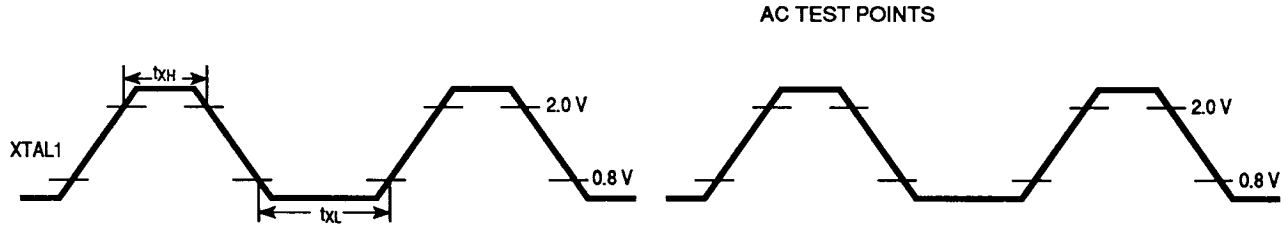
## AC CHARACTERISTICS (Cont.) TA = $0^0$C to + $70^0$ C, VCC = 5 V ± 5%

| Symbol | Parameter | SYC16C450 Min | SYC16C450 Max | Units | Conditions |
|---|---|---|---|---|---|
| **Transmitter** | | | | | |
| $t_{HR1}$ | Delay from rising edge of $\overline{DOSTR}$/DOSTR (WR THR)to Reset Interrupt | | 175 | ns | 100 pF load |
| $t_{HR2}$ | Delay from falling edge of $\overline{DOSTR}$/DOSTR (WR THR) to Reset Interrupt | | n/a | ns | 100 pF load |
| $t_{IRS}$ | Delay from initial INTR Reset to Transmit Start | 8 | 24 | RCLK Cycles | Note 3 |
| $t_{SI}$ | Delay from Initial Write to Interrupt | 16 | 32 | RCLK Cycles | Note 3 |
| $t_{SS}$ | Delay from Stop to Next Start | | | ns | |
| $t_{STI}$ | Delay from Stop to Interrupt (THRE) | 8 | 8 | RCLK Cycles | Note 3 |
| $t_{IR}$ | Delay from $\overline{DISTR}$/DISTR (RD IIR) to Reset Interrupt (THRE) | | 250 | ns | 100 pF load |
| **Modem Control** | | | | | |
| $t_{MDO}$ | Delay from $\overline{DOSTR}$/DOSTR (WR MCR) to Output | | 200 | ns | 100 pF load |
| $t_{SIM}$ | Delay to Set Interrupt from MODEM Input | | | ns | 100 pF load |
| $t_{RIM}$ | Delay to Reset Interrupt from $\overline{DISTR}$/DISTR (RS MSR) | | 250 | ns | 100 pF load |
| **Baud Generator** | | | | | |
| N | Baud Divisor | 1 | $2^{16}$-1 | | |
| $t_{BLD}$ | Baud Output Negative Edge Delay | | 125 | ns | 100 pF load |
| $t_{BHD}$ | Baud Output Positive Edge Delay | | 125 | ns | 100 pF load |
| $t_{LW}$ | Baud Output Down Time | 425 | | ns | fx = 2 MHz, + 2,100 pF load |
| $t_{HW}$ | Baud Output Up Time | 330 | | ns | fx = 3 MHz , +3, 100 pF load |
| **Reciever** | | | | | |
| $t_{SCD}$ | Delay from RCLK to Sample Time | | 2 | µs | |
| $t_{SINT}$ | Delay from Stop to Set Interrupt | 1 | 1 | RCLK Cycles | Note 3 |
| $t_{RINT}$ | Delay from $\overline{DISTR}$/DISTR (RD RBR/RDLSR) to Reset Interrupt | | 1 | µs | 100 pF load |

Notes:
1. Does not apply to XTAL2.
2. Applicable only when ADS is tied LOW.
3. RCLK=tXH and tXL.
4. Charge and discharge time is determined by VOL, VOH and the external loading.
5. All timings are referenced to valid 0 and valid 1 (see AC TEST POINTS).

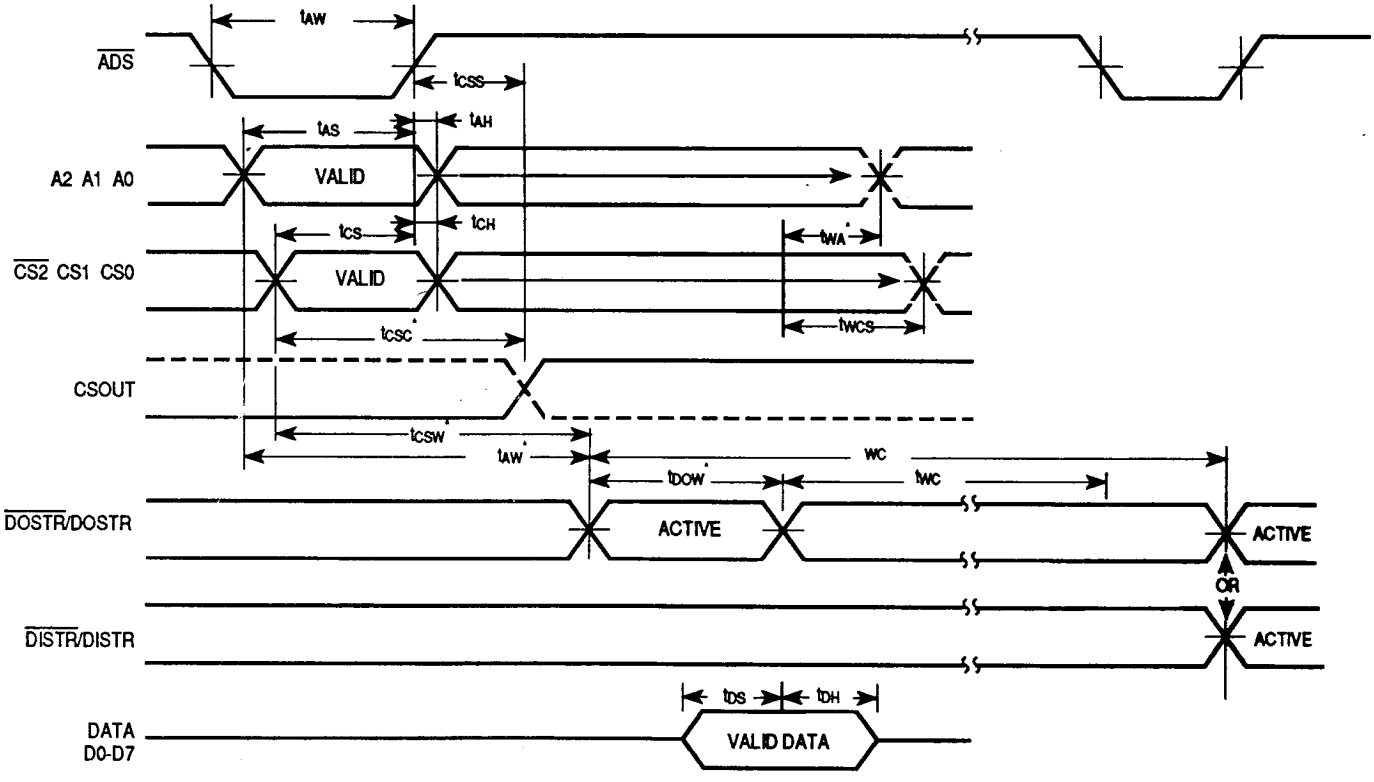
## AC TESTING INPUT/OUTPUT WAVE FORM

EXTERNAL CLOCK INPUT (3.1 MHz MAXIMUM)




## TIMING DIAGRAM

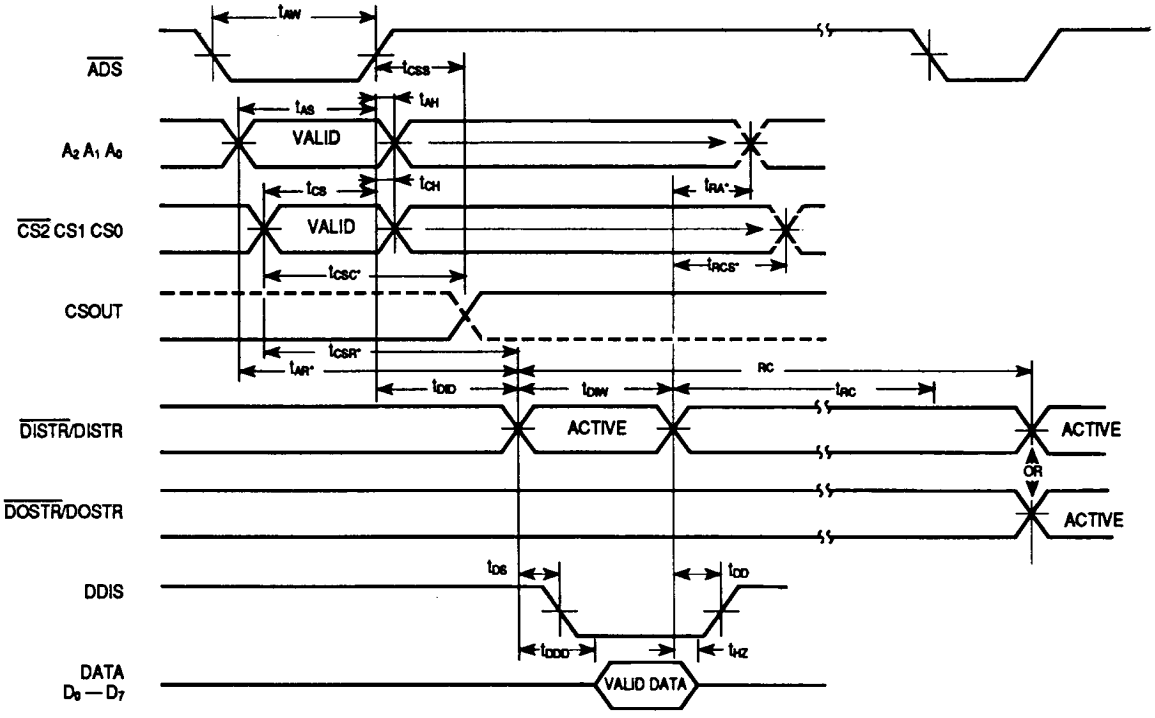
WRITE CYCLE




* Applicable only when $\overline{ADS}$ is tied low.

## TIMING DIAGRAM

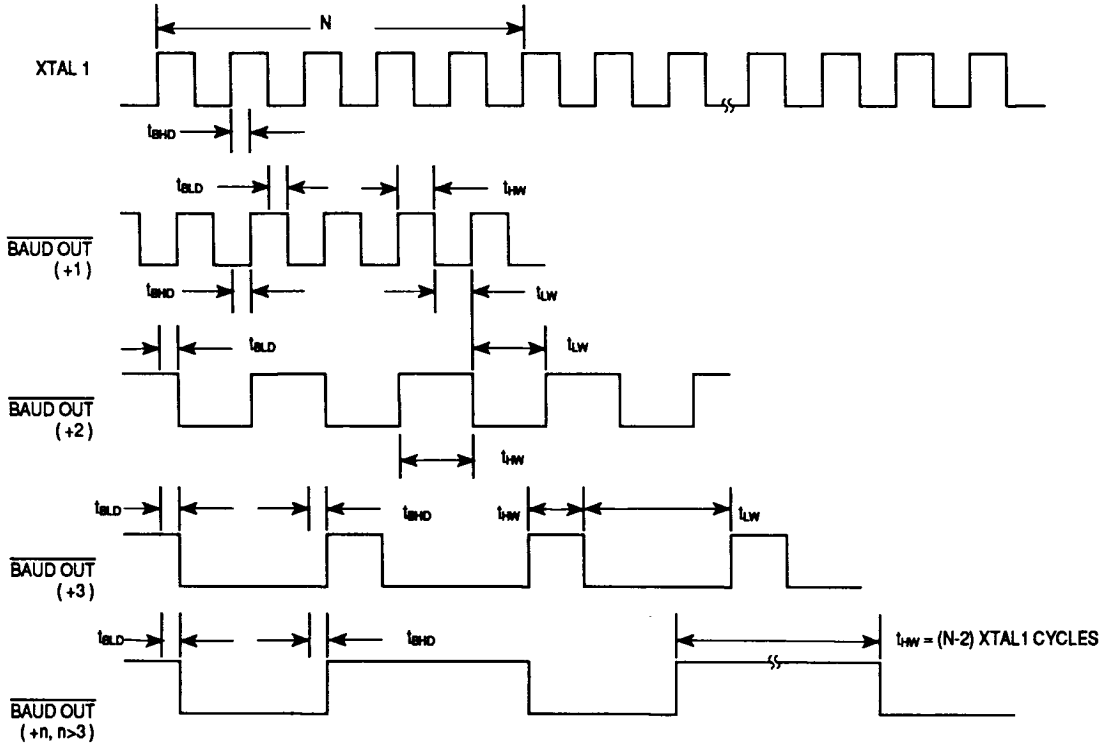
READ CYCLE



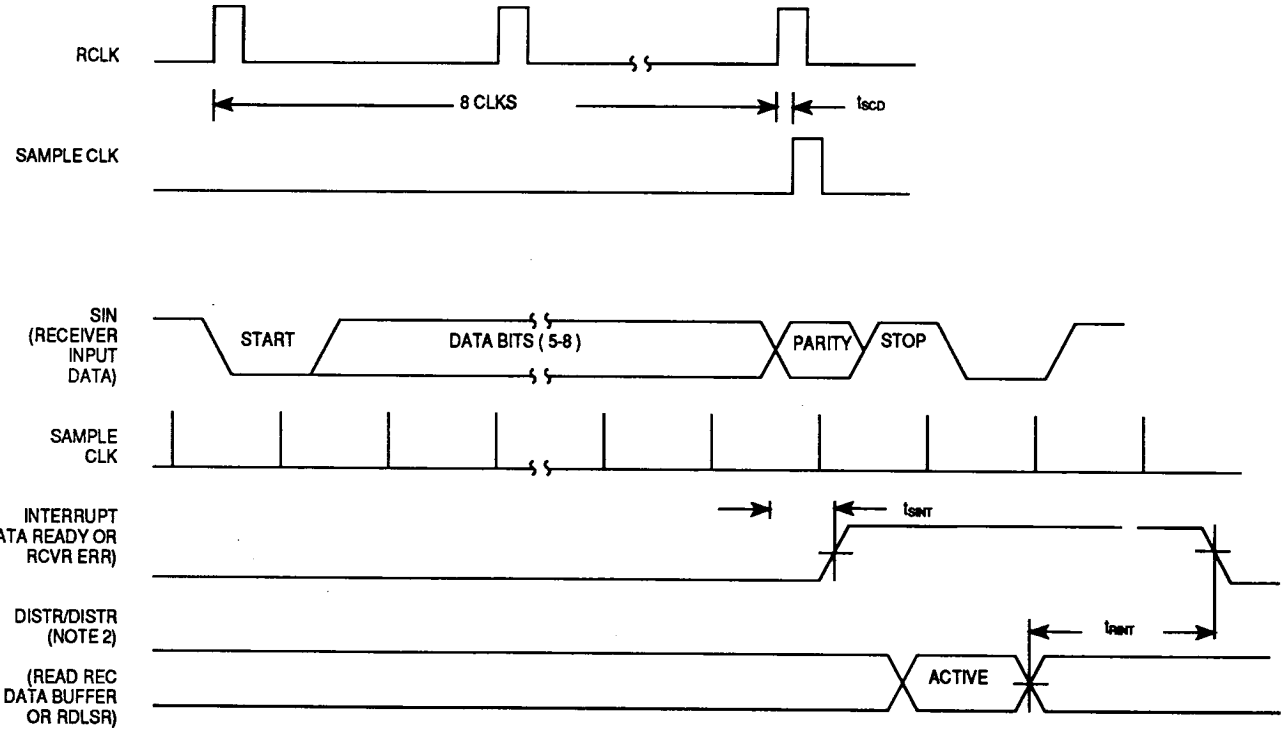

* Applicable only when $\overline{ADS}$ is tied low.

## TIMING DIAGRAM

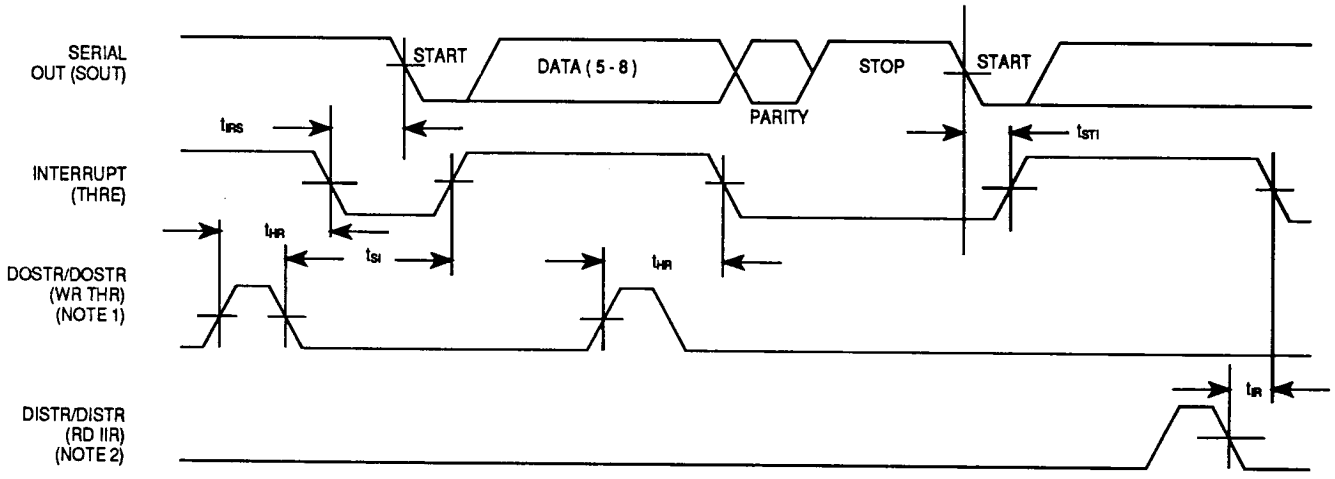
BAUDOUT



## TIMING DIAGRAM
RECEIVER

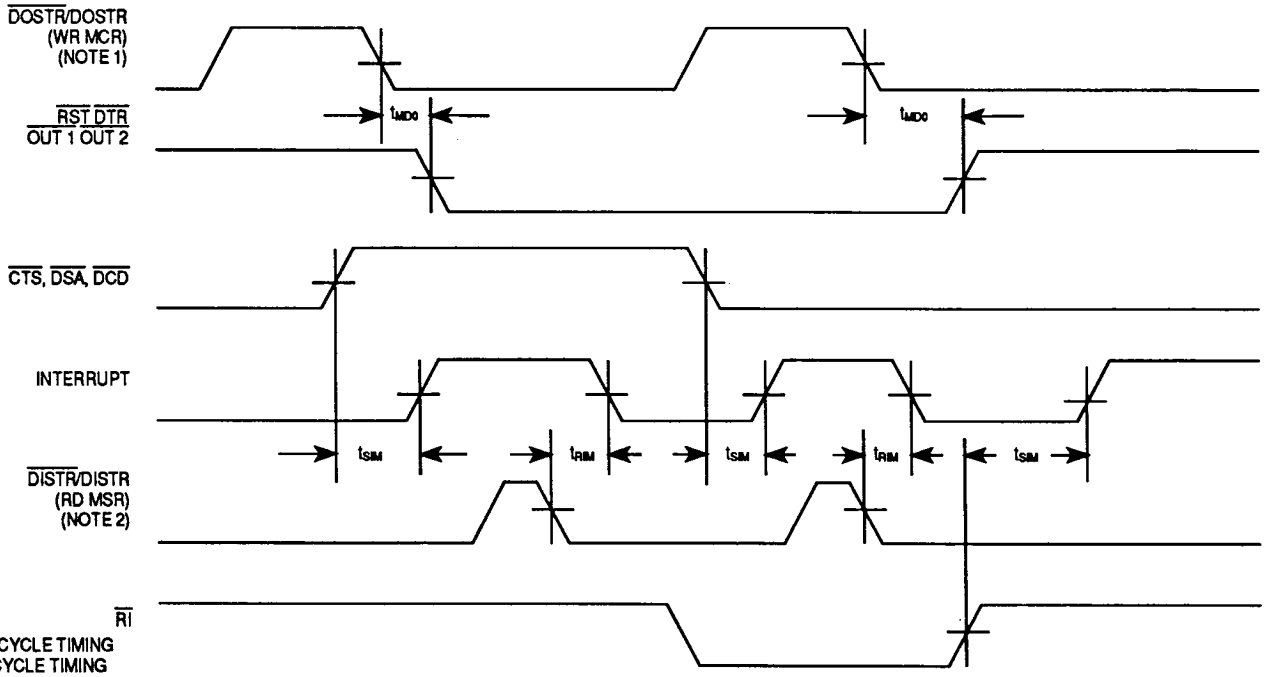



## TIMING DIAGRAM
TRANSMITTER



## TIMING DIAGRAM

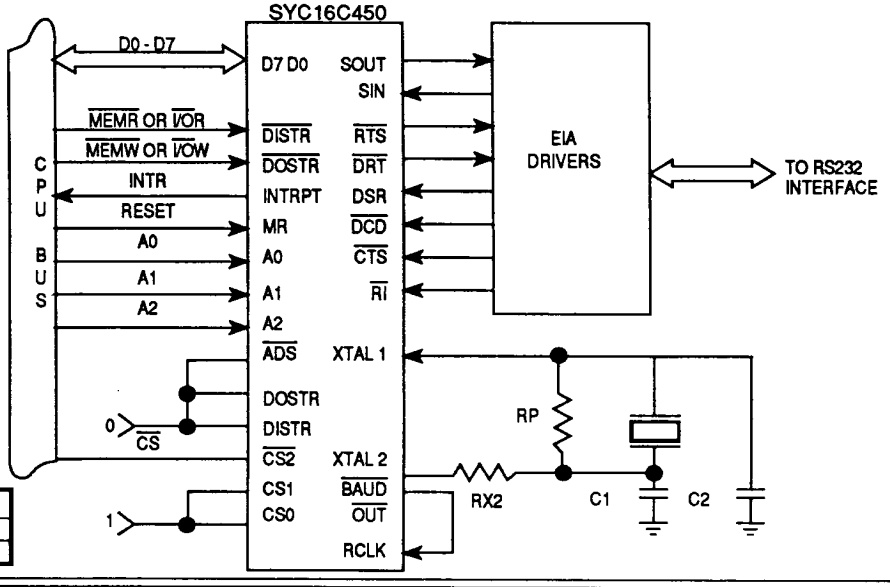
MODEM CONTROLS




NOTES:
1. SEE WRITE CYCLE TIMING
2. SEE READ CYCLE TIMING

## BASIC CONFIGURATION

SYC16C450




| TYPICAL COMPONENT VALUES | | | | |
|---|---|---|---|---|
| Crystal | RP | RX2 | C1 | C2 |
| 3.072 MHz | 1 MΩ | 1.5 Ω | 10-30 pF | 40-90 pF |

## ORDER INFORMATION

| Part Number | Maximum External Clock Frequency | Package |
|---|---|---|
| SYC16C450 | 3.1 MHz | Plastic DIP |
| SYC16C450-QC | 3.1 MHz | Plastic Leaded Chip Carrier (PLCC) |

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