YAMAHA LSI

YSS240

KP2S

Karaoke Processor 2 for SRAM

■OUTLINE

YSS240(KP2S) is an LSI used to carry out digital signal processor for "Karaoke" systems.
With a 256K bit pseudo SRAM or SRAM connected externally, it executes signal processing such as Key Control, Voice cancel, Microphone echo and Surround with easy control.
With A/D and D/A converters integrated, it can handle input and output of analog audio signals in addition to digital audio signal.

■FEATURES

- Built in 3-channel 15-bit floating A/D converters and 1-channel D/A converter handle audio signal from L, R, Microphone channels.
- Digital signal can be input directly, and it is possible to output digital signals to oversampling digital filter or DACs.
- It is necessary to connect 256K bit (32K* 8) pseudo SRAM or SRAM for external memory.
- De-emphasis processing for digital audio input signal.
- Mixing, fade-in and fade-out processing for digital/analog signals.
- Voice cancel processing for attenuating center-positioned voice.
- Key control processing up to a maximum +-600 cent by 50 cent.
  (200 cent = 1 whole tone, 1200 cent = 1 octave)
- Microphone echo processing up to a maximum 200ms.
- Surround signal processing with 4 preset patterns.
- Easy control by setting register through the microprocessor serial interface.
- The register controlled by microprocessor is compatible with YSS216B(KP2)'s method.
- Master clock is 16.9344MHz and sampling frequency is 44.1kHz.
- 5V single power supply, Si-gate CMOS process.
- 64-pin plastic QFP (YSS240-F).

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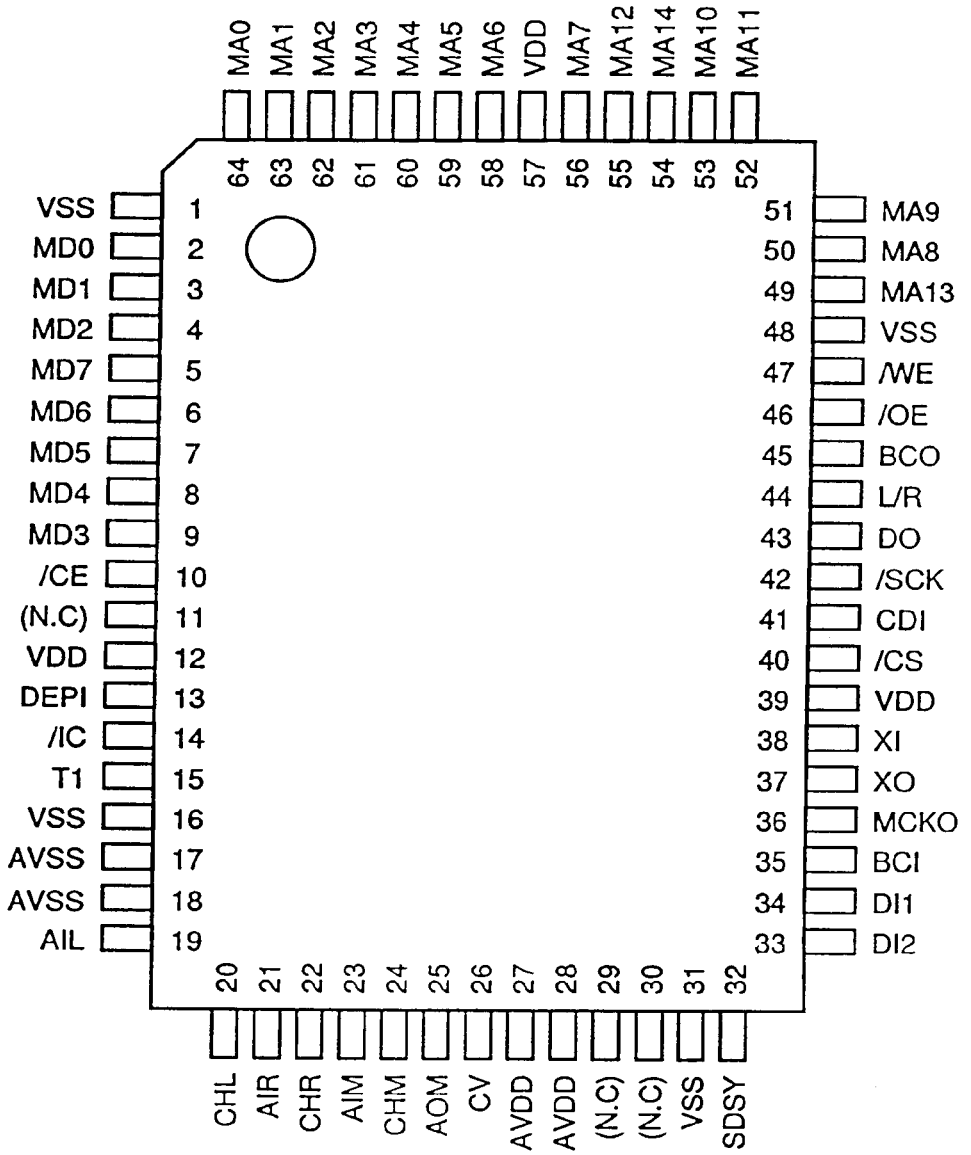
YSS240 CATALOG
CATALOG No. : LSI-4SS240A2
1996. 5

■PIN CONFIGURATION



<64pin QFP Top View>

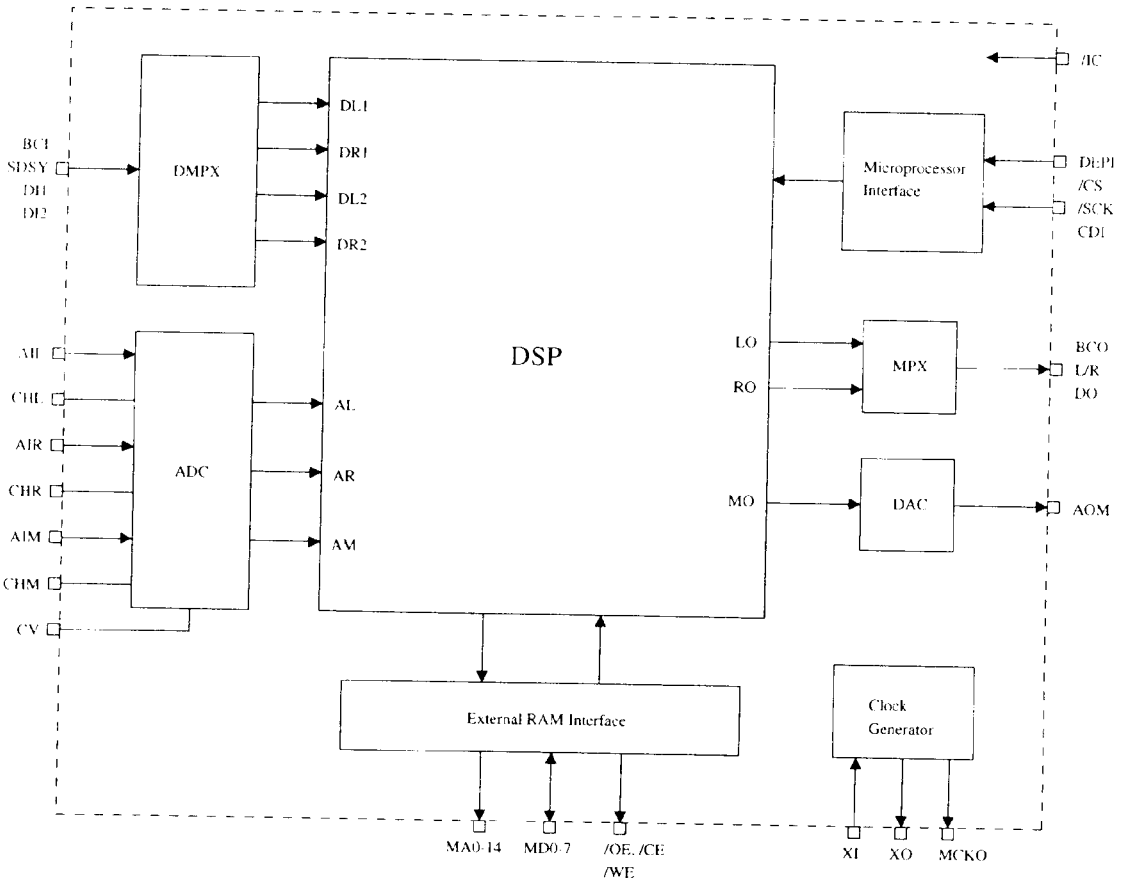
■PIN DESCRIPTION

No.	Name	I/O	Function
1	VSS	-	Ground (digital block)
2	MD0	I/O	External RAM interface data
3	MD1	I/O	External RAM interface data
4	MD2	I/O	External RAM interface data
5	MD7	I/O	External RAM interface data
6	MD6	I/O	External RAM interface data
7	MD5	I/O	External RAM interface data
8	MD4	I/O	External RAM interface data
9	MD3	I/O	External RAM interface data
10	/CE	O	External RAM interface CE
11	(N.C)	-	
12	VDD	-	+5V power supply (digital block)
13	DEPI	I	De-emphasis control input (H : ON, L : by FCR register)
14	/IC	I	Initial clear input (low active)
15	T1	I+	LSI test terminal (Do not connect.)
16	VSS	-	Ground (digital block)
17	AVSS	-A	Ground (ADC, DAC block, connect to VSS externally)
18	AVSS	-A	Ground (ADC, DAC block, connect to VSS externally)
19	AIL	IA	Analog audio signal L channel ADC input
20	CHL	-A	Sample/hold capacitor connecting terminal of AIL input
21	AIR	IA	Analog audio signal R channel ADC input
22	CHR	-A	Sample/hold capacitor connecting terminal of AIR input
23	AIM	IA	Analog audio signal Microphone channel ADC input
24	CHM	-A	Sample/hold capacitor connecting terminal of AIM input
25	AOM	OA	Analog audio signal Microphone channel DAC output
26	CV	-A	Center voltage of ADC
27	AVDD	-A	+5V power supply (ADC, DAC block, connect to VDD externally)
28	AVDD	-A	+5V power supply (ADC, DAC block, connect to VDD externally)
29	(N.C)	-	
30	(N.C)	-	
31	VSS	-	Ground (digital block)
32	SDSY	I+	Digital audio signal input word clock
33	DI2	I+	Digital audio signal input serial data 2
34	DI1	I+	Digital audio signal input serial data 1
35	BCI	I+	Digital audio signal input bit clock
36	MCKO	O	Master clock output (16.9344MHz)
37	XO	O	X'tal oscillator connecting terminal
38	XI	I	X'tal oscillator connecting terminal, or clock input (16.9344MHz)
39	VDD	-	+5V power supply (digital block)
40	/CS	I	Microprocessor interface chip select
41	CDI	I	Microprocessor interface serial data
42	/SCK	I	Microprocessor interface serial clock
43	DO	O	Digital audio signal output serial data
44	L/R	O	Digital audio signal output word clock
45	BCO	O	Digital audio signal output bit clock
46	/OE	O	External RAM interface OE
47	/WE	O	External RAM interface WE
48	VSS	-	Ground (digital block)

No.	Name	I/O	Function
49	MA13	O	External RAM interface address
50	MA8	O	External RAM interface address
51	MA9	O	External RAM interface address
52	MA11	O	External RAM interface address
53	MA10	O	External RAM interface address
54	MA14	O	External RAM interface address
55	MA12	O	External RAM interface address
56	MA7	O	External RAM interface address
57	VDD	-	+5V power supply (digital block)
58	MA6	O	External RAM interface address
59	MA5	O	External RAM interface address
60	MA4	O	External RAM interface address
61	MA3	O	External RAM interface address
62	MA2	O	External RAM interface address
63	MA1	O	External RAM interface address
64	MA0	O	External RAM interface address

NOTE) I+ ; Pulled-up input, A ; Analog terminal

■BLOCK DIAGRAM



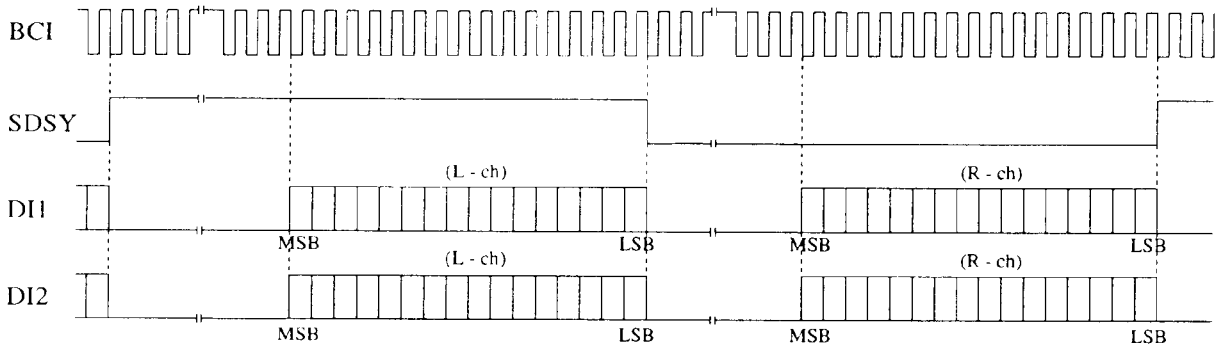
■FUNCTION DESCRIPTION

1. Clocks XI, XO, MCKO

Using XI, XO terminals, X'tal oscillator circuit is constructed.
Oscillating frequency is 16.9344MHz.
Also, external clock can be input to XI terminal.
XI clock is output through MCKO terminal.

2. Digital inputs BCI, SDSY, DI1, DI2

Digital audio data is input to BCI, SDSY, DI1 and DI2 terminal as following format.



Digital inputs have two stereo inputs. BCI, SDSY and DI1 or DI2 must be synchronized to XI clock.

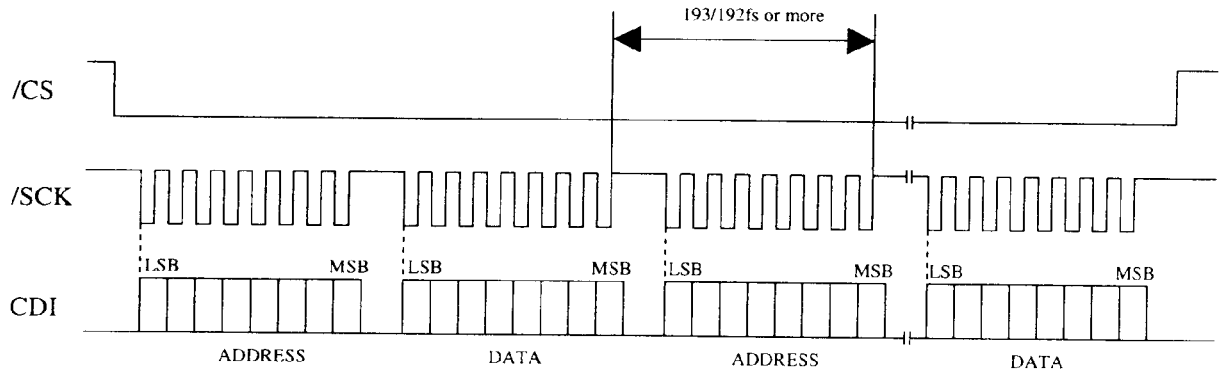
3. Analog inputs AIL, AIR, AIM, CHL, CHR, CHM, CV

L, R and Microphone analog signal are input to AIL, AIR and AIM terminals respectively. Sampling frequency of A/D converter is 44.1kHz.
Connect sample/hold capacitors for A/D conversion to CHL, CHR and CHM terminals.
CV terminal indicates center voltage of A/D converter. Connect a capacitor for stabilizing. Each analog input signal must be biased by this voltage.

4. Microprocessor interface /CS, /SCK, CDI, DEPI

To write data to internal register, this LSI has 8-bit serial interface.

Write register address and data together as following format.

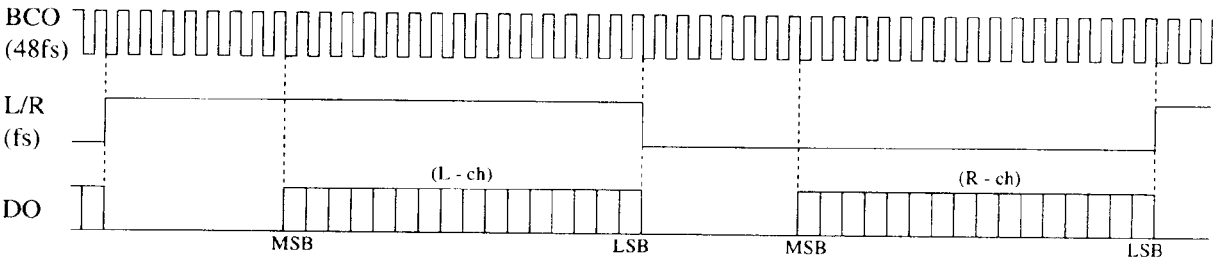


After initial clear, input "H" to "L" signal at /CS terminal. As soon as the MSB bit of register data is taken by "L" to "H" signal of /SCK terminal, the setting register is written to internal register.

The digital data input to DI1 terminal can be undergone de-emphasis processing. The DEPI signal, logical-summed by bit 1(de-emphasis ON/OFF) of FCR register, controls de-emphasis processing. When DEPI is set to "H", de-emphasis processing is ON. And when DEPI is set to "L", de-emphasis processing depends on FCR register.

5. Digital outputs BCO, L/R, DO

After each sound processing, data is output through BCO, L/R and DO terminals as following.



6. Analog output AOM

AOM is a DAC output of microphone echo signal.

Sampling frequency of D/A converter is 44.1kHz.

It outputs voltage output. Connect sample/hold capacitor and execute buffering by using Op-Amp. with high impedance input.

7. External RAM interface MA0-14, MD0-7, /OE, /WE, /CE

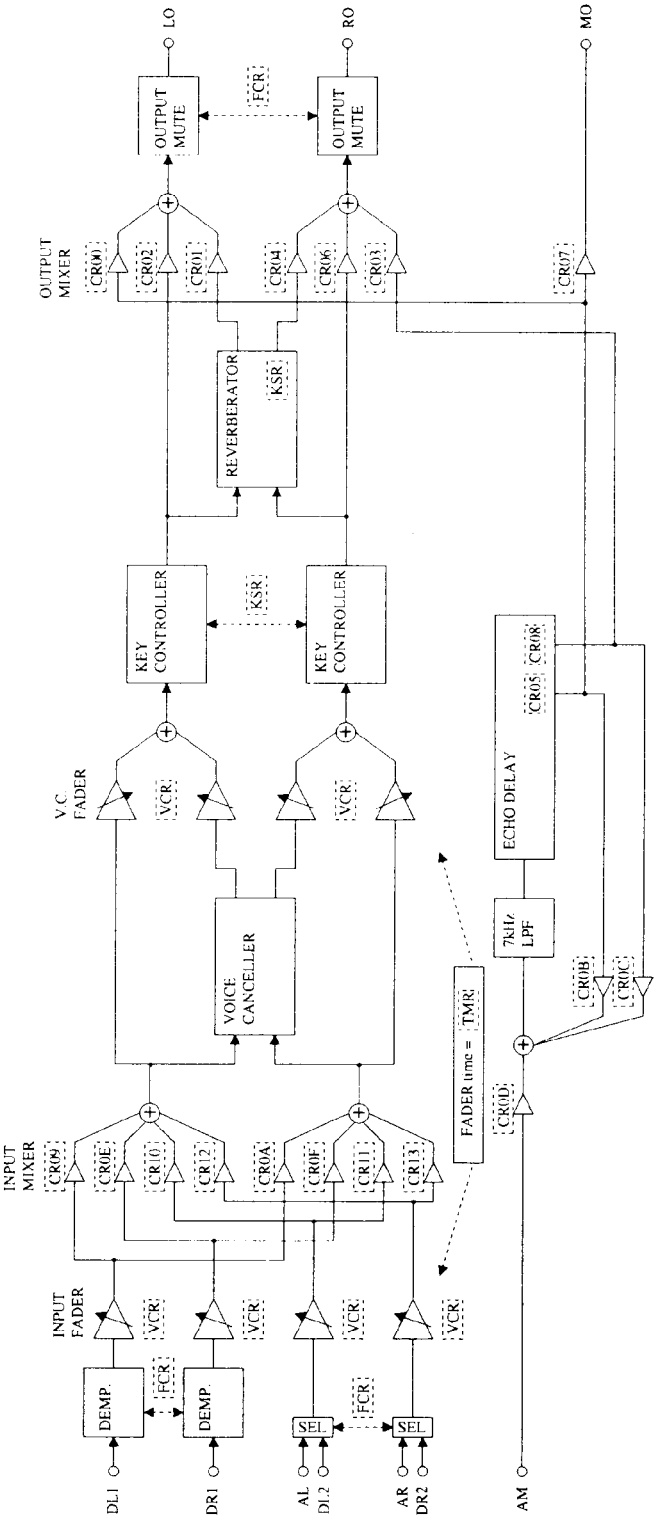
This LSI requires a 256K bit (32K*8-bit) pseudo SRAM or SRAM that access time is 200ns or less.

8. Initial clear /IC

This LSI requires initial clear when turning on the power.

■CONTROL DESCRIPTION

1. Signal flow



2. Register description

Each part of this LSI is controlled by setting data to 24 byte register as follows.

ADDR	NAME	FUNCTION
$00	FCR	Function control register
$01	KSR	Key, surround control register
$02	VCR	Multi-sound, voice cancel register
$03	TMR	Time constant register
$20 ↓ $33	CR00 ↓ CR13	Coefficient register (effective only when FCR bit 2 = 0)

Each block of the signal flow is controlled by the register marked in dotted frame in that block.

● Function control register (FCR)

This register is for hardware setting.

bit 0 (LSB)	Select ADC data input (AIL, AIR)/digital data input (DI2) "1" = ADC data input (AIL, AIR) "0" = digital data input (DI2) ※This bit is not concerned in DI1 terminal input.
bit 1	Digital input (DI1) de-emphasis processing ON/OFF "1" = OFF "0" = ON ※This bit is not concerned in DI2 terminal input.
bit 2	Select coefficients "1" = preset data used "0" = data set to coefficient register CR00 ~ CR13 used.
bit 3	Output muting ON/OFF "1" = muting OFF (fade-in within 23.2ms) "0" = muting ON (fade-out within 23.2ms)
bit 4	Internal accumulator clear "1" = zero clear "0" = normal
bit 5	Digital audio input synchronizing setting "1" = internal synchronization (when BCI, SDSY, DI1, DI2 is not used) "0" = external synchronization (when BCI, SDSY, DI1, DI2 is used)
bit 6	Select de-emphasis coefficient "1" = normal (fs=44.1kHz) "0" = CD-I (fs=37.8kHz)
bit 7 (MSB)	Don't care.

Note) bit 0 ~ bit 6 are set to "1" when initial clear.

● Key, surround control register (KSR)

Specify key shift rate of key controller by using lower 5 bits.
Select surround pattern of reverberator by using upper 2 bits.
Bit 7 (MSB) is "don't care".

bit 4	3	2	1	0	key shift rate
0	1	1	1	1	1900 cent up
0	1	1	1	0	1200 cent up
0	1	1	0	1	700 cent up
0	1	1	0	0	600 cent up
0	1	0	1	1	550 cent up
0	1	0	1	0	500 cent up
0	1	0	0	1	450 cent up
0	1	0	0	0	400 cent up
0	0	1	1	1	350 cent up
0	0	1	1	0	300 cent up
0	0	1	0	1	250 cent up
0	0	1	0	0	200 cent up
0	0	0	1	1	150 cent up
0	0	0	1	0	100 cent up
0	0	0	0	1	50 cent up
0	0	0	0	0	no effect

bit 4	3	2	1	0	key shift rate
1	1	1	1	1	50 cent down
1	1	1	1	0	100 cent down
1	1	1	0	1	150 cent down
1	1	1	0	0	200 cent down
1	1	0	1	1	250 cent down
1	1	0	1	0	300 cent down
1	1	0	0	1	350 cent down
1	1	0	0	0	400 cent down
1	0	1	1	1	450 cent down
1	0	1	1	0	500 cent down
1	0	1	0	1	550 cent down
1	0	1	0	0	600 cent down
1	0	0	1	1	700 cent down
1	0	0	1	0	1200 cent down
1	0	0	0	1	1400 cent down
1	0	0	0	0	1900 cent down

Note) 1200 cent = 1 octave, 200 cent = 1 whole tone

This LSI has 4 types of surround patterns.
Each surround effect varies depending on mixing ratio to direct sound, input sources and so on.

bit 6	5	Surround Pattern	Description
0	0	Simulation stereo	Monaural source (L channel) is made pseudo stereophonic.
0	1	Live	Using (L - R) signal, presence is added.
1	0	Movie	Using (L - R) signal, surround effect is emphasized.
1	1	Karaoke	Reverberation is added to (L + R) signal as well

Note) Each pattern name and its description are tentative. All of these patterns use about 50ms delay.

Bit 0 ~ bit 6 are set to "0" when initial clear.

● Multi sound, voice cancel control register (VCR)

Input fader is started by setting lower 4 bits. bit 5 ~ bit 7(MSB) is "don't care".

bit 3	bit 2	bit 1	bit 0
AIR/DI2 R	AIL/DI2 L	DI1 R	DI1 L

"1" = fade-in start
"0" = fade-out start

bit 4	Voice cancel fader start setting "1" = cross fade to voice canceler output side "0" = cross fade to bypass side

Bit 0 ~ bit 4 are set to "0" when initial clear. (then input fader is in fade-out state.)

● Time constant register (TMR)

Fade in/out time is set for input fader and voice cancel fader.

bit 7	6	5	4	3	2	1	0	HEX	fading time
1	1	1	1	1	1	1	1	FF	0.09s
1	1	1	0	1	1	1	0	EE	0.10s
0	0	1	1	0	0	0	0	30	0.50s
0	0	0	1	1	0	0	0	18	0.99s
0	0	0	1	0	0	0	0	10	1.49s
0	0	0	0	1	1	0	0	0C	1.98s
0	0	0	0	1	0	0	0	08	2.97s
0	0	0	0	0	1	1	0	06	3.96s
0	0	0	0	0	1	0	0	04	5.94s
0	0	0	0	0	0	1	1	03	7.92s
0	0	0	0	0	0	0	0	00	23.2ms

As bit 0 ~ bit 7 are set to "0" when initial clear, be sure to set fading time.

● Coefficient registers (CR00~CR13)

CR05, CR08 are for setting delay time of microphone echo. Other registers than these are for setting attenuation value which determines mixing ratio of input, output and feed-back gain of microphone echo.

(1) Delay time setting (CR05, CR08)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
C7	C6	C5	C4	C3	C2	C1	0

Note) bit 0 must be set to "0".

$$\text{Delay time} = \left(\sum_{N=1}^{7} C_N \times 2^N\right) \times \frac{64}{44.1} \text{ [ms]}$$

Where $0 \leqq \sum_{N=1}^{7} C_N \times 2^N \leqq 138$

(2) Attenuation value setting (CR00~CR04, CR06, CR07, CR09~CR13)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
C7	C6	C5	C4	C3	C2	C1	C0

$$\text{Coefficient value} = (-1)\times C_7 + \sum_{N=0}^{6} C_N \times 2^{N-7}$$

When $C_7 \sim C_0 = 01111111$, however, the coefficient value becomes $0.99976\left(\sum_{N=0}^{11} 2^{N-12}\right)$

(3) Coefficient preset value

This LSI has a set of preset values corresponding to each coefficient register.

When using it, data does not need to send to the coefficient register. Control is possible only with 4 registers.

Use bit 2 of FCR register to select these preset values or values set in coefficient registers for actual signal processing.

As the state at initial clear is for using preset values (FCR bit 2 = "1"), when using coefficient register values, set the data for coefficient registers and then set FCR bit 2 to "0".

● Coefficient preset values

Coef.	Value	Coef.	Value	Coef.	Value
CR00	00H	CR07	7FH	CR0E	00H
CR01	00H	CR08	00H	CR0F	00H
CR02	7FH	CR09	00H	CR10	7FH
CR03	00H	CR0A	00H	CR11	00H
CR04	00H	CR0B	32H	CR12	00H
CR05	68H	CR0C	00H	CR13	7FH
CR06	7FH	CR0D	40H		

■ ELECTRIC CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	-0.3～7.0	V
Input voltage	V_I	-0.3～V_{DD}+0.3	V
Operating temperature	T_{OP}	0～70	℃
Storage temperature	T_{stg}	-50～125	℃

2. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	4.75	5.00	5.25	V
Operating temperature	T_{OP}	0	25	70	℃

3. DC Characteristics (Condition : Ta = 0～70℃, V_{DD} = 5.0 ±0.25V)

Parameter	Symbol	Condition	Min	Typ.	Max.	Unit
Power supply current	I_{DD}	I_{DD} = 5.0V			80	mA
Input voltage H level	V_{IH1}	(*1)	2.0			V
Input voltage H level	V_{IH2}	(*2)	3.5			V
Input voltage L level	V_{IL}				0.8	V
Input leakage current	V_{LK}		-10		10	μA
Output voltage H level	V_{OH1}	I_{OH} = -0.4mA (*3)	V_{DD}-1.0			V
Output voltage H level	V_{OH2}	I_{OH} = -0.4mA (*4)	2.8			V
Output voltage L level	V_{OL}	I_{OL} = 1.6mA			0.4	pF

*1) Applicable to input terminals except XI, /IC, T1.

*2) Applicable to XI, /IC, T1 terminals.

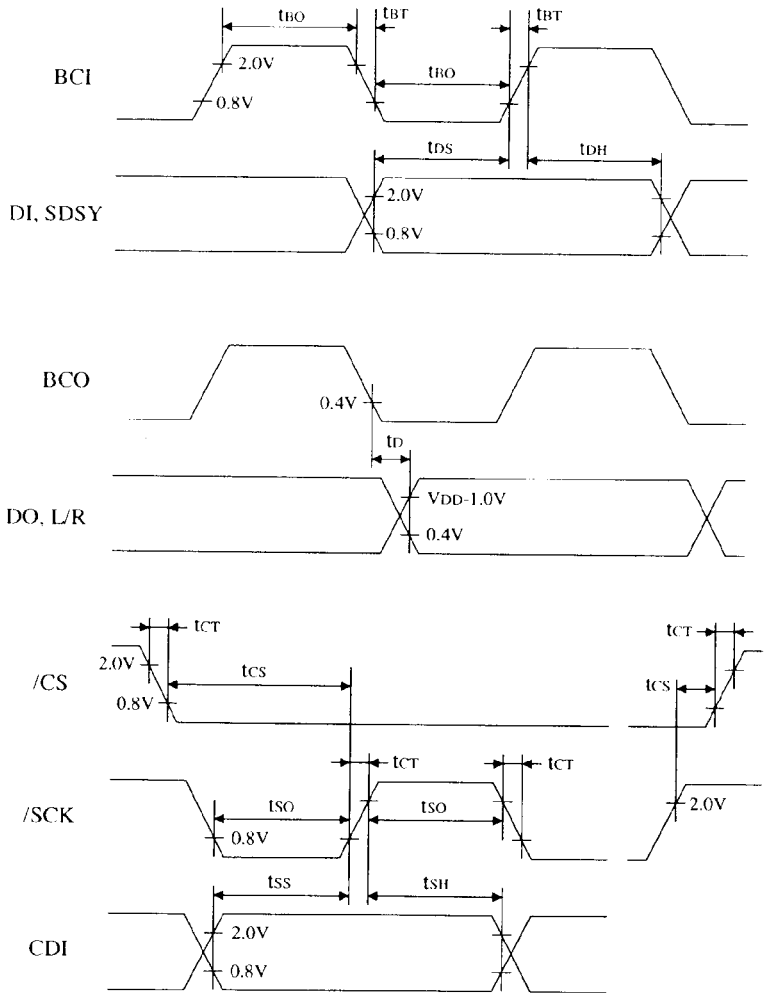
*3) Applicable to output terminals except MA0-14, MD0-7, /CE, /OE, /WE.

*4) Applicable to MA0-14, MD0-7, /CE, /WE terminals.

4. AC Characteristics (Condition : Ta = 0~70℃, V_{DD} = 5.0±0.25V)

Parameter		Symbol	Min	Typ.	Max.	Unit
XI	Input frequency	f_C	12.0	16.9344	17.0	MHz
XI	Duty	R_C		50		%
BCI	Frequency	f_{BC}	1.0		4.3	MHz
BCI	ON/OFF time	t_{BO}	100			ns
	Transition time	t_{BT}			20	ns
DI, SDSY	Setup time	t_{DS}	100			ns
	Hold time	t_{DH}	100		20	ns
DO, L/R	Access time	t_D	-20		20	ns
/CS	Setup time	t_{CS}	1/50fs			s
/SCK	ON/OFF time	t_{SO}	1/50fs			s
/CS, /SCK	Transition time	t_{CT}			1/150fs	s
CDI	Setup time	t_{SS}	1/100fs			s
	Hold time	t_{SH}	1/100fs			s

(Note) fs = fc/384



5. Analog Characteristics (Condition : Ta = 25℃, V_{DD} = 5.0V)

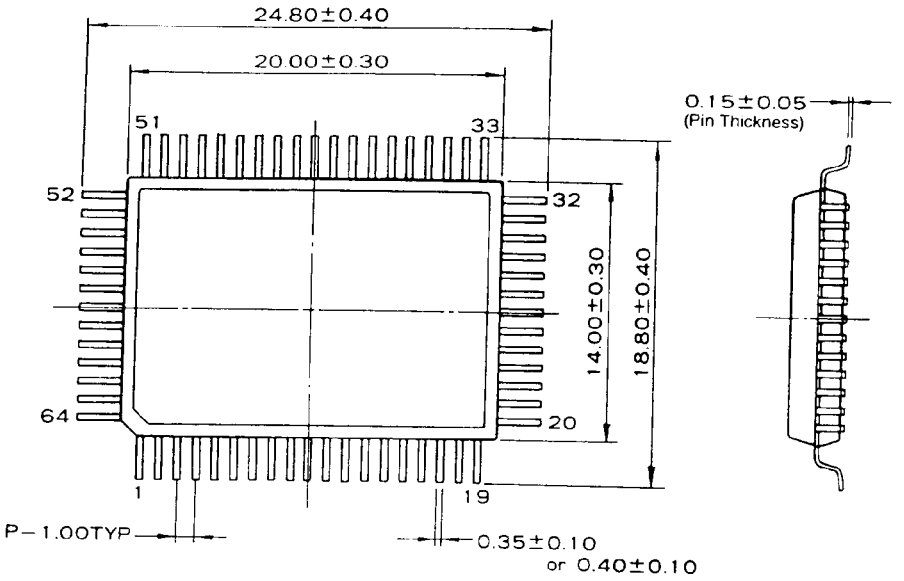
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Analog input voltage	V_{IA}	(*1)		4.75		V
Analog output voltage	V_{OA}	(*2)		4.75		V
CV terminal voltage	V_C			2.5		V
Total harmonic distortion	THD+N	1kHz, 0dB (*3)		0.5	1.0	%
		1kHz, -30dB (*3)		0.8	1.5	%
Signal to noise ratio	S/N	S = 0dB (*3)	73	80		dB

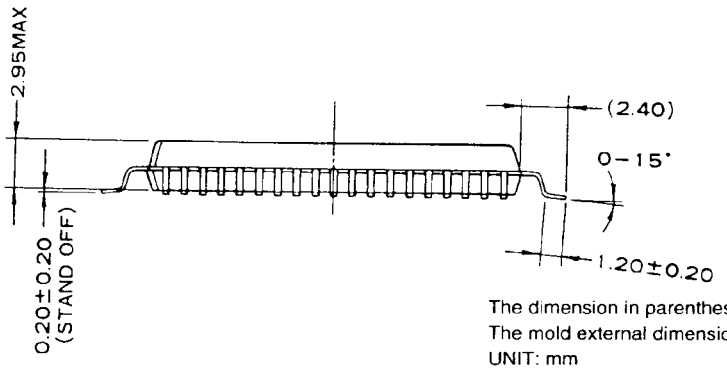
*1) peak to peak, applicable to AIL, AIR, AIM terminals.

*2) peak to peak, appicable to AOM terminal.

*3) when 0dB = 4.75Vpp and each A/D input→AOM D/A output through.

■EXTERNAL DIMENSIONS





The dimension in parentheses is for reference only.
The mold external dimensions do not include flash.
UNIT: mm

NOTE: The LSIs for surface mount need especial consideration on storage and soldering conditions. For detailed information, please contact your nearest agent of yamaha.

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