Utilizing 3 V Flash in 5 V Flash Systems

Application Note

July 2003

The following document refers to Spansion memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this document as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal documentation improvements and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about Spansion memory solutions.

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This document is intended to assist hardware designers in adapting 5 V embedded systems for use with low voltage Flash devices. Systems can benefit from advanced architectures such as Simultaneous Read/Write (AMD DL family), as well as decreased system power requirements. Since many new high-density Flash devices are being introduced in low voltage applications, systems employing 5 V power planes and signals can benefit from these breakthrough devices.

Benefits of Low Voltage Flash Devices

In order to facilitate low power designs, most new Flash devices are designed to operate in lower voltage systems (primarily systems using a 2.7 V to 3.6 V voltage source). Low voltage systems are often battery powered, needing components designed to draw low active current, with standby current requirements of less than 1 µA per device. The latest generation of low voltage Flash devices are manufactured using revolutionary 0.32 and 0.25 µm process technologies, which provide for faster access times and lower power consumption. On average, 3 V Am29LVxxx devices consume about 50% less current than the equivalent 5 V Am29Fxxx devices, in terms of active reads and writes. This correlates to an average sixty percent decrease in power consumption during active reads and writes. For systems designed for reduced power requirements, migrating from 5 V memory subsystems to 3 V can reduce overall power dissipation and parasitic heat generation.

Perhaps the greatest benefit is the inclusion of the advanced architectural features, available in newer generation devices, into designs that previously could not support these low voltage family devices. AMD's true Simultaneous Read/Write architecture (DL family) is available in 2.7 V technology devices, not 5 V. The simultaneous read/write architecture allows code to be executed from the same physical memory as data, while being programmed or erased. This allows system designers to reduce or eliminate separate memory components like EPROM, SRAM, or EPROM, which would have been needed to separate programming code or data storage from the traditional Flash memory system. Now a single Flash memory can serve both code and data storage needs. Other enhancements available newer 2.7 V Flash devices (but not in the 5.0 V flash devices) include 1 million erase cycle endurance, enhanced control over sector protection, high security sectors, faster programming modes, and higher density with x8/x16 bus width.

In addition to new architectures, a myriad of new packaging possibilities exist in low voltage devices. For systems that place a premium on system board space, the new generation of chip scale packaging offer greatly reduced package area requirements. This includes fine-pitch ball grid array (FBGA) and micro ball grid array (µBGA™) packages. However, most 5 V Flash devices are not supported in these new "small form factor" device packages.

Migration Factors

There are two main areas of concern when designing low voltage Flash into 5 V systems. First, the 5 V power plane must be regulated down to the lower voltage supply requirements of the Flash device. Second, the 5 V signals that control the Flash device (including data, address, and control signals, all at TTL levels) must be limited so as not to exceed the supply voltage provided to the Flash memory, without altering the function of the system. Ideally, this voltage translation interface should be inexpensive, and require as little board area as possible.

Signal Voltage Level Isolation/Translation

Since AMD low voltage flash is not 5V I/O tolerant (the only exception to this rule is the Burst Mode (BL) and Page Mode (PL) families), there must exist an interface that translates incoming control, data, and address signals from 5 V I/O voltage levels down to 3 V. (AMD low voltage Flash devices are not 5 V I/O tolerant in order to minimize die size as well as to decrease leakage current).

A common way of accomplishing this is through the use of a voltage level translator IC. The devices in the 74LCX244 and 74LCX245 low power, low voltage CMOS families are ideal for this purpose. The 244 devices are unidirectional buffers/line drivers with 5 V tolerant I/O pins, suitable for address and control signal translation. The 245 family devices are bi-directional bus transceivers used for input/output data pins. Thus through use of both these ICs, all signal, address, and data lines can be level translated, with the additional benefit of a buffering layer to the rest of the system.

The first step is to determine the total number of unidirectional buffer pins required by the system. There are 4 signal control pins (WE#, OE#, CE# and RESET#), and depending on the device density, between 17 and 23 address lines. Figure 1 illustrates the connection of the first 16 address lines from the 5 V-address bus to the 3 V Flash address pins.

Since the Flash address and control pins are input only, the Output Enable lines of the buffer can be tied to ground, simplifying the control circuitry.

Figures 1 and 2 outline the connections for 20 address lines, along with the 4 required control signal lines. For systems employing multiple flash devices, it will be necessary to substitute the 16 bit version (74LCX16244) for the second buffer (74LCX244) in order to accommodate additional Chip Select Signals.

The address and control signal system will require at maximum 27 translation lines, with 1 additional line for each device added to the system.

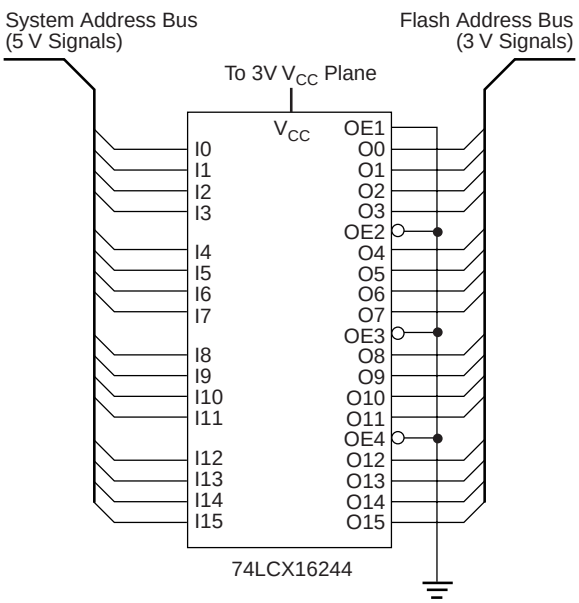

Figure 1. Address Translation Circuitry (First 16 Address Lines)

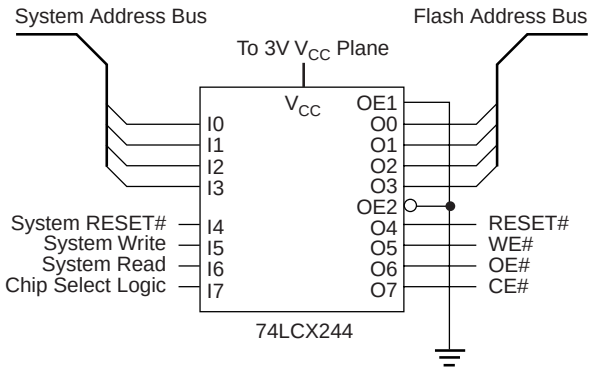

Figure 2. Address and Control Signal Connections

Note: *the A9, OE#, and RESET# pins on AMD Flash devices are used in high voltage programming and autoselect modes, and are 12 V tolerant. If the system design requires additional translation pins, these three pins can be directly connected to 5 V signals, thereby freeing three translation lines for use by additional address/control signals. This can save expense by preventing the requirement of additional buffer ICs.*

On the data side, the system requires a low voltage, 5 V tolerant transceiver/buffer, to allow for bi-directional data travel. The LCX family contains the 74LCX245 and 74LCX16245 for this purpose. In most ways, they function in the same way as the address buffers above, but they contain additional switch logic to distinguish between reads and writes from/to the Flash device. See Figure 3.

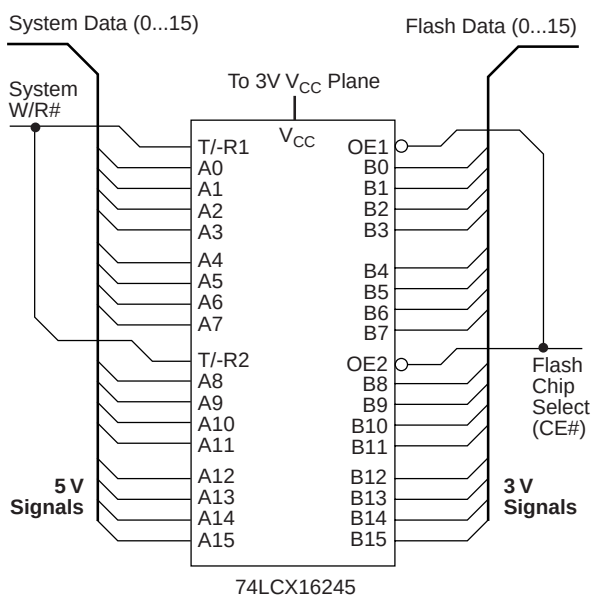

Figure 3. Data Bus Transceiver

Note: *Certain systems do not have a direct implementation of the W/R# signal. This signal distinguishes between a bus read and a bus write cycle. This signal can be synthesized from the System READ and System WRITE signals outlined in Figure 2 with the circuit (assumes System READ and System WRITE are active low) in Figure 4.*

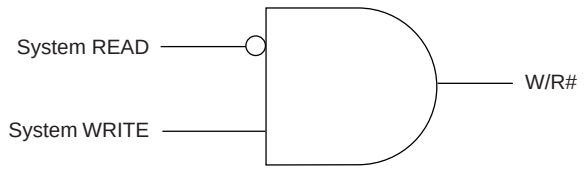

Figure 4. W/R# Control Circuitry

It may also be possible to use the System READ signal directly, so long as the system cannot assert both the READ and WRITE signals simultaneously.

V_{CC} Power Plane Isolation

To supply the correct operating voltage to the Flash device and the voltage translation buffers, the 5 V power plane must be regulated to 2.7-3.6 V nominal. This can be accomplished in several ways, depending on system board space and cost requirements.

The simplest method of accomplishing this is to use three silicon diodes to provide an approximate 2.1 V drop from 5 V (yielding a V_{CC} voltage of around 3 V). However, the nominal 5 V supply must be regulated to within 5% to ensure that the diode reduced voltage remains within the 2.7 V to 3.6 V range. Capacitors C1 and C2 provide voltage conditioning, and keep the diodes properly biased in case of V_{CC} power glitches. See Figure 5.

Virtually any silicon diode will function properly in this circuit: form factor or cost per unit will be the main driving factors in selecting an appropriate diode. Suggested parts are 1N4148 or 1N914.

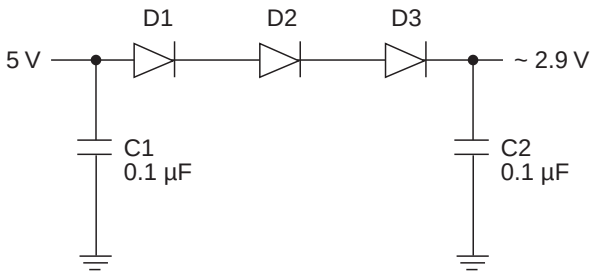

Figure 5. Voltage Regulation Using Silicon Diodes

Regulation can also be accomplished through use of a dedicated voltage regulator IC. Fixed linear regulators from Linear Technologies, such as the LT1117CST-3.3, produce excellent results due to low load regulation.

C1 and C2 provide transient stability to filter voltage fluctuations, as are taken from recommended values. Resistor R1 provides a minimum load current of 1 mA, which is the minimum current draw at which the device guarantees regulation. See Figure 6.

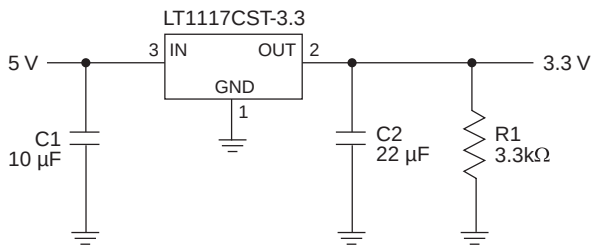

Figure 6. Voltage Regulation Using Fixed Regulator IC

Of particular note is the current limiting protection of the regulators versus the diodes only solution. The LT1117 has internal over-current protection circuitry that will protect system components in case of power surges on the 5 V V_{CC} power plane. This protection may justify the additional cost of the regulators over the diode solution, in systems that have strict power protection requirements. Most regulators also have thermal shutdown benefits to prevent system damage due to excessive currents. The regulator may also be necessary in systems that cannot regulate the 5 V supply to within 5% tolerance.