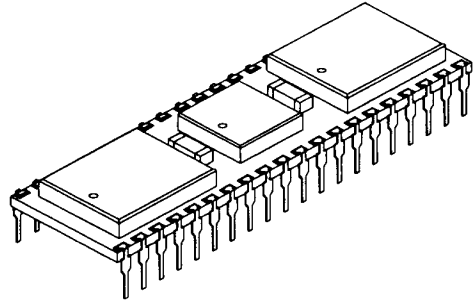


DESCRIPTION:

The DPS8M612 is a one megabit Static Random Access Memory (SRAM), complete with memory interface logic and on-board capacitors, organized as 32K X 16 bits.

The DPS8M612 is ideally suited for high performance applications where word wide data bus and ease of use is required.

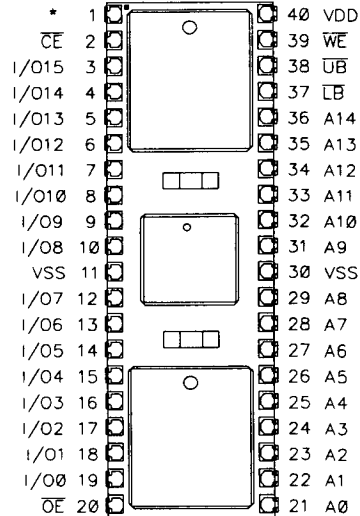


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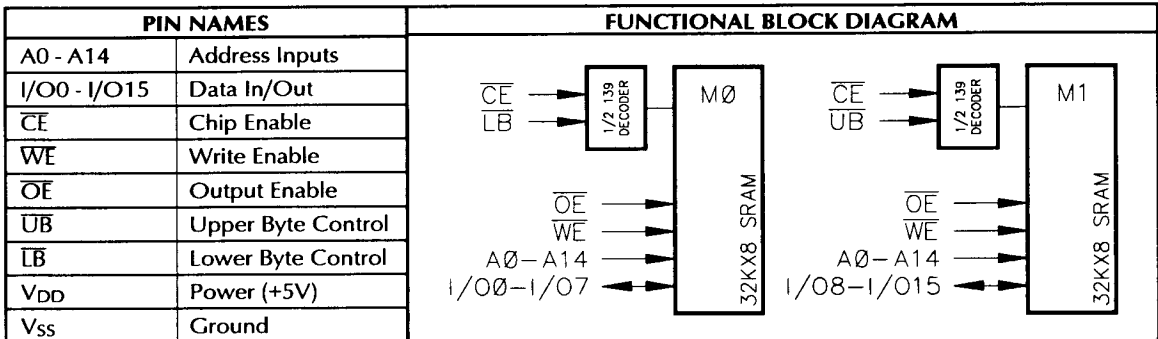
FEATURES:

- Fast Access Times:
35, 45, 55, 70, 85, 100, 120, 150ns (max.)
- Fully Static Operation; No Clock or Refresh Required
- Single +5V Power Supply, $\pm 10\%$ Tolerance
- TTL Compatible
- Common Data Input and Output
- Low Data Retention Voltage: 2.0V min.
- JEDEC Standard 40-Pin DIP Package
- Military Version Available with Devices Fully Compliant to MIL -STD-883C

PIN-OUT DIAGRAMS



* This pin must be connected to a Logic-LOW for proper operation.



TRUTH TABLE									
Mode	Pin 1	CE	LB	UB	WE	OE	I/O0 - I/O7	I/O8 - I/O15	Supply Current
Not Selected	X	H	X	X	X	X	HIGH-Z	HIGH-Z	Standby
Not Selected	X	X	H	H	X	X	HIGH-Z	HIGH-Z	Standby
DOUT Disable	L	L	L	L	H	H	HIGH-Z	HIGH-Z	Active
Read Lower Block	L	L	L	H	H	L	DOUT	HIGH-Z	Active
Read Upper Block	L	L	H	L	H	L	HIGH-Z	DOUT	Active
Read All	L	L	L	L	H	L	DOUT	DOUT	Active
Write Lower Block	L	L	L	H	L	X	DIN	HIGH-Z	Active
Write Upper Block	L	L	H	L	L	X	HIGH-Z	DIN	Active
Write All	L	L	L	L	L	X	DIN	DIN	Active

H = HIGH, L = LOW and is X = Don't Care.

DPS8M612-35, -45, -55, -70, -85, -100 DC OPERATING CHARACTERISTICS: Over operating ranges									
Symbol	Characteristics	Test Conditions	C		I		M/B		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I _{IN}	Input Leakage Current	V _{IN} = 0V to V _{DD}	-10	+10	-10	+10	-10	+10	μA
I _{OUT}	Output Leakage Current	V _{I/O} = 0V to V _{DD} , CE or OE = V _{IH} , or WE = V _{IL}	-10	+10	-10	+10	-10	+10	μA
I _{CC1}	Active Supply Current	CE = V _{IL} , V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA Cycle = 0		210		240		250	mA
I _{CC2}	Operating Supply Current	Cycle = min., Duty = 100% I _{OUT} = 0mA,		290		330		330	mA
I _{SB1}	Full Standby Supply Current (CMOS)	CE = V _{DD} -0.2V, Cycle = 0, V _{IN} ≥ V _{DD} -0.2V or V _{IN} ≤ 0.2V		4		4		4	mA
I _{SB2}	Standby Current (TTL)	CE = V _{IH} , Cycle = min.		60		70		70	mA
I _{CCDR2}	Data Retention Supply Current	CE ≥ V _{DR} -0.2V, V _{DR} = 2V		0.6		0.7		1.2	mA
I _{CCDR3}	Data Retention Supply Current	CE ≥ V _{DR} -0.2V, V _{DR} = 3V		0.7		0.8		1.6	mA
V _{OL}	Output Low Voltage	I _{OUT} = 2.1mA		0.4		0.4		0.4	V
V _{OH}	Output High Voltage	I _{OUT} = -1.0mA	2.4		2.4		2.4		V

DPS8M612-120, -150 DC OPERATING CHARACTERISTICS: Over operating ranges									
Symbol	Characteristics	Test Conditions	C		I		M/B		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I _{IN}	Input Leakage Current	V _{IN} = 0V to V _{DD}	-10	+10	-10	+10	-10	+10	μA
I _{OUT}	Output Leakage Current	V _{I/O} = 0V to V _{DD} , CE or OE = V _{IH} , or WE = V _{IL}	-10	+10	-10	+10	-10	+10	μA
I _{CC1}	Active Supply Current	CE = V _{IL} , V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA, Cycle = 0		100		100		100	mA
I _{CC2}	Operating Supply Current	Cycle = min., Duty = 100% I _{OUT} = 0mA		130		140		150	mA
I _{SB1}	Full Standby Supply Current (CMOS)	CE = V _{DD} -0.2V, Cycle = 0, V _{IN} ≥ V _{DD} -0.2V or V _{IN} ≤ 0.2V		200		400		600	μA
I _{SB2}	Standby Current (TTL)	CE = V _{IH} , Cycle = min.		4		4		4	mA
I _{CCDR2}	Data Retention Supply Current	CE ≥ V _{DR} -0.2V, V _{DR} = 2V		30		80		400	μA
I _{CCDR3}	Data Retention Supply Current	CE ≥ V _{DR} -0.2V, V _{DR} = 3V		80		100		480	μA
V _{OL}	Output Low Voltage	I _{OUT} = 2.1mA		0.4		0.4		0.4	V
V _{OH}	Output High Voltage	I _{OUT} = -1.0mA	2.4		2.4		2.4		V

RECOMMENDED OPERATING RANGE ¹					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
VDD	Supply Voltage	4.5	5.0	5.5	V
VIH	Input HIGH Voltage	2.2		VDD+0.3	V
VIL	Input LOW Voltage	-0.5 ²		0.8	V

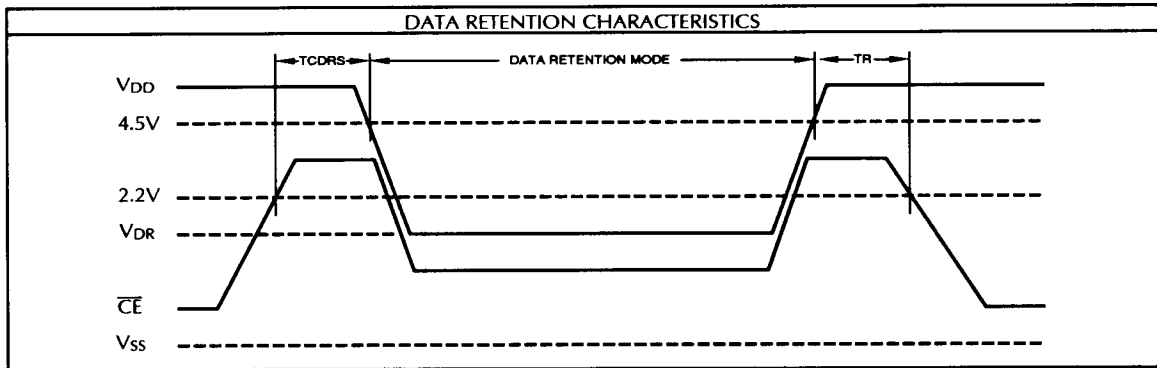
ABSOLUTE MAXIMUM RATINGS ³			
Symbol	Parameter	Value	Unit
TSTC	Storage Temperature	-65 to +150	°C
TBIAS	Temperature Under Bias	-55 to +125	°C
VDD	Supply Voltage ¹	-0.5 to +7.0	V
VI/O	Input/Output Voltage ¹	-0.5 to VDD + 0.5	V

CAPACITANCE ⁴ : TA = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
CADR	Address Input	30	pF	VIN = 0V
CCE	Chip Enable	20		
CWE	Write Enable	30		
COE	Output Enable	30		
CIO	Data Input/Output	25		

DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
VOH	HIGH Voltage	IOH = -1.0mA	2.4	-	V
VOL	LOW Voltage	IOL = 2.1mA	-	0.4	V

4

DATA RETENTION CHARACTERISTICS						
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
VDR	Data Retention Voltage	CE ≥ VDR - 0.2V	2.0	5.0	5.5	V
tCDR	Chip Disable to Data Retention Time		0			ns
tR	Recovery Time	tRC = Read Cycle Timing	tRC			ns



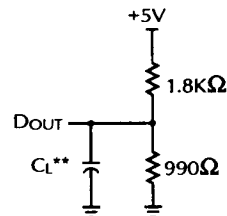
AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns*
Input Timing Reference Levels	1.5V

* Transition measured from 0.8V and 2.2V.

AC TEST CONDITIONS		
Load	CL	Parameters Measured
1	100pF	except tCLZ, tCHZ, tWHZ, tWLZ, tOLZ and tOHZ
2	5pF	tCLZ, tCHZ, tWHZ, tWLZ, tOLZ and tOHZ

Figure 1. Output Load

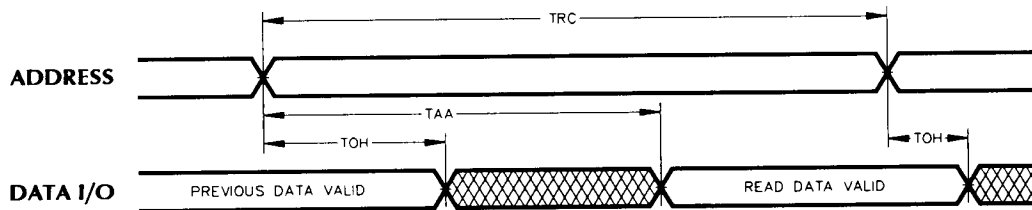
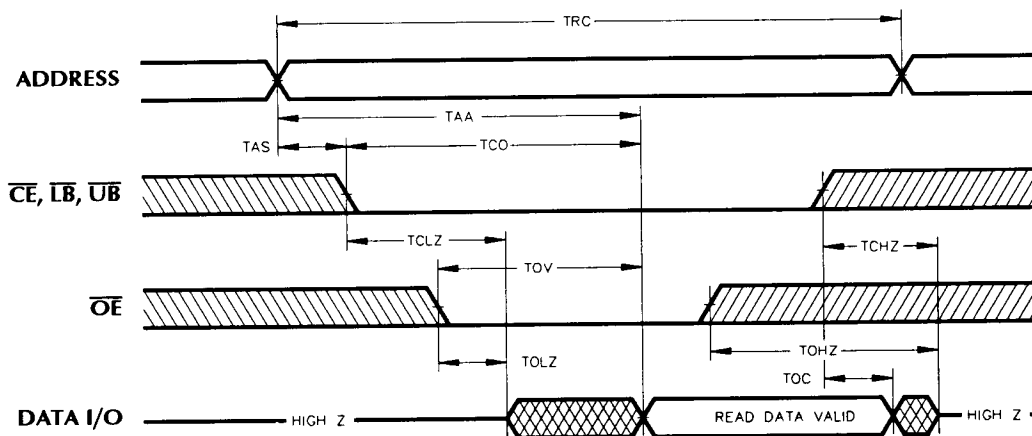
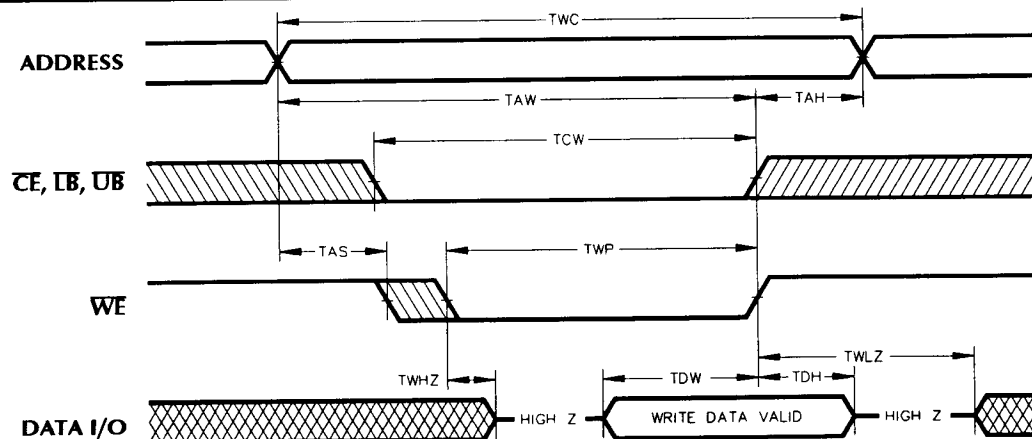
** Including Probe and Jig Capacitance.

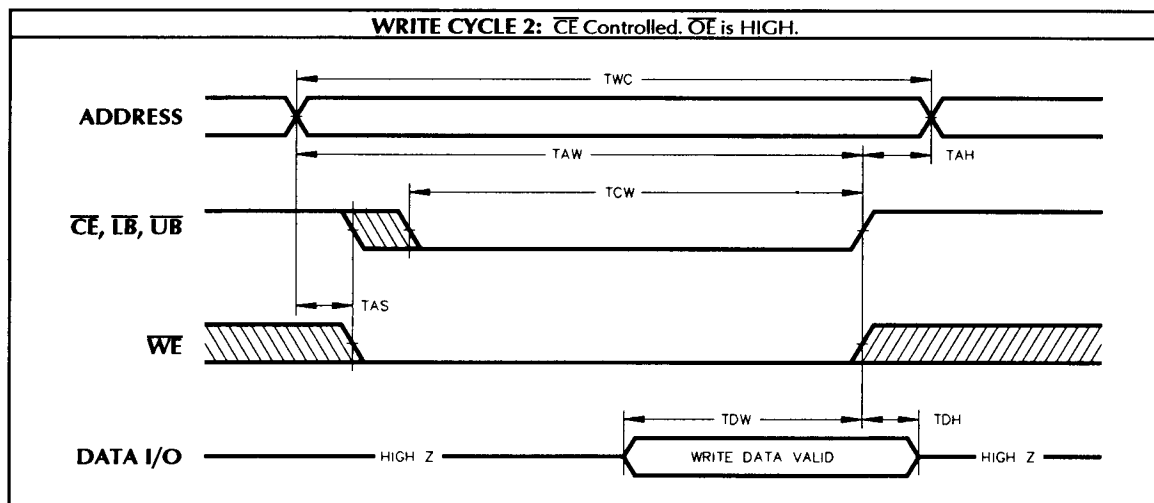


AC OPERATING CONDITIONS AND CHARACTERISTICS													
READ CYCLE: Over operating ranges													
No.	Symbol	Parameter	-35		-45		-55		-70		-85		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t _{RC}	Read Cycle Time	35		45		55		70		85		ns
2	t _{AA}	Address Access Time		35		45		55		70		85	ns
3	t _{CO}	Chip Enable to Output Valid		35		45		55		70		85	ns
4	t _{OV}	Output Enable to Output Valid		20		25		35		40		50	ns
5	t _{OH}	Output Hold from Address Change	3		3		3		3		5		ns
6	t _{CLZ}	Chip Enable to Output in LOW-Z ^{4, 6}	5		5		5		5		5		ns
7	t _{OLZ}	Output Enable to Output in LOW-Z ^{4, 6}	0		5		5		5		5		ns
8	t _{CHZ}	Chip Enable to Output in HIGH-Z ^{4, 6}		15		20		25		30		35	ns
9	t _{OHZ}	Output Enable to Output in HIGH-Z ^{4, 6}		15		20		25		30		35	ns
10	t _{OC}	Output Hold from Chip Enable		10		10		10		10		10	ns
WRITE CYCLE: Over operating ranges ⁷													
11	t _{WC}	Write Cycle Time	35		45		55		70		85		ns
12	t _{AW}	Address Valid to End of Write	30		40		50		65		75		ns
13	t _{CW}	Chip Enable to End of Write	30		40		50		65		75		ns
14	t _{DW}	Data Valid to End of Write	20		20		20		25		30		ns
15	t _{DH}	Data Hold Time	3		0		0		0		0		ns
16	t _{WP}	Write Pulse Width	30		30		35		40		45		ns
17	t _{AS}	Address Set-up Time**	0		0		0		0		0		ns
18	t _{AH}	Address Hold Time	0		5		5		5		5		ns
19	t _{WHZ}	Write Enable to Output in HIGH-Z ^{4, 6}		15		15		20		25		30	ns
20	t _{WLZ}	Write Enable to Output in LOW-Z ^{4, 6}	5		5		5		5		5		ns

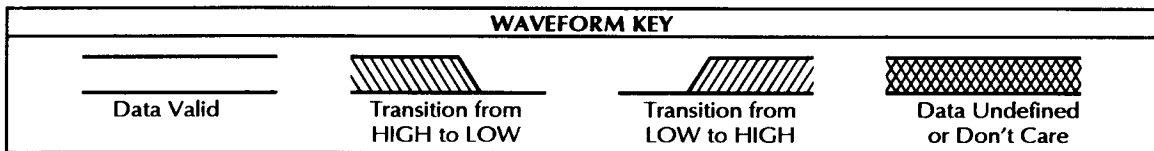
AC OPERATING CONDITIONS AND CHARACTERISTICS												
READ CYCLE: Over operating ranges												
No.	Symbol	Parameter	-100		-120		-150		Unit			
			Min.	Max.	Min.	Max.	Min.	Max.				
1	t _{RC}	Read Cycle Time	100		120		150		ns			
2	t _{AA}	Address Access Time		100		120		150	ns			
3	t _{CO}	Chip Enable to Output Valid		100		120		150	ns			
4	t _{OV}	Output Enable to Output Valid		60		60		70	ns			
5	t _{OH}	Output Hold from Address Change	10		10		10		ns			
6	t _{CLZ}	Chip Enable to Output in LOW-Z ^{4, 6}	10		10		10		ns			
7	t _{OLZ}	Output Enable to Output in LOW-Z ^{4, 6}	5		5		5		ns			
8	t _{CHZ}	Chip Enable to Output in HIGH-Z ^{4, 6}		40		45		55	ns			
9	t _{OHZ}	Output Enable to Output in HIGH-Z ^{4, 6}		35		40		50	ns			
10	t _{OC}	Output Hold from Chip Enable	0		0		0		ns			
WRITE CYCLE: Over operating ranges ⁷												
11	t _{WC}	Write Cycle Time	100		120		150		ns			
12	t _{AW}	Address Valid to End of Write	90		100		120		ns			
13	t _{CW}	Chip Enable to End of Write	90		100		120		ns			
14	t _{DW}	Data Valid to End of Write	40		50		60		ns			
15	t _{DH}	Data Hold Time	0		0		0		ns			
16	t _{WP}	Write Pulse Width	65		75		80		ns			
17	t _{AS}	Address Set-up Time**	0		0		0		ns			
18	t _{AH}	Address Hold Time	5		5		5		ns			
19	t _{WHZ}	Write Enable to Output in HIGH-Z ^{4, 6}		30		35		40	ns			
20	t _{WLZ}	Write Enable to Output in LOW-Z ^{4, 6}	5		5		5		ns			

** Valid for both Read and Write Cycles.

READ CYCLE 1: Address Controlled. $\overline{WE}$ is HIGH. $\overline{CE}$ and $\overline{OE}$ are LOW.**READ CYCLE 2: $\overline{CE}$ Controlled. $\overline{WE}$ is HIGH.****WRITE CYCLE 1: $\overline{WE}$ Controlled. $\overline{OE}$ is LOW.**

**NOTES:**

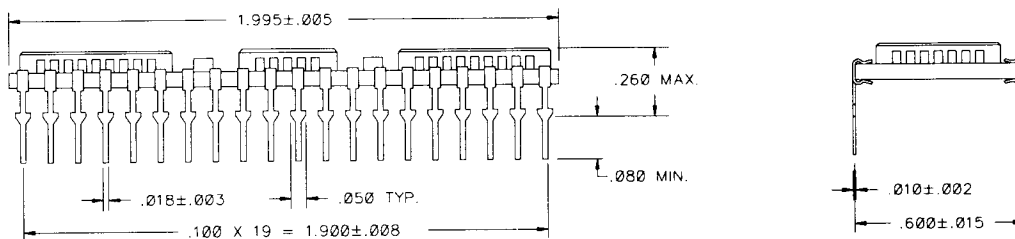
1. All voltages are with respect to V_{SS} .
2. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of $\pm 500\text{mV}$ from steady state voltage.
6. When $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH, I/O pins are in the output state, and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when $\overline{WE}$ is LOW.



ORDERING INFORMATION

DP PREFIX	S8M612 - DEVICE TYPE	XXX SPEED	X GRADE			
				C	COMMERCIAL	0°C to +70°C
				I	INDUSTRIAL	-40°C to +85°C
				M	MILITARY	-55°C to +125°C
				B *	MIL-PROCESSED	-55°C to +125°C
				35	35ns	
				45	45ns	
				55	55ns	
				70	70ns	
				85	85ns	
				100	100ns	
				120	120ns	
				150	150ns	
					32KX16 CMOS SRAM	

* B grade modules can be constructed with 883 devices.

MECHANICAL DRAWING**Dense-Pac Microsystems, Inc.**

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