



21-Bit Deserializers with Programmable Spread Spectrum and DC Balance

General Description

The MAX9242/MAX9244/MAX9246/MAX9254 deserialize three LVDS serial-data inputs into 21 single-ended LVC-MOS/ LVTTTL outputs. A separate parallel-rate LVDS clock provides the timing for deserialization. The MAX9242/MAX9244/MAX9246/MAX9254 feature spread-spectrum capability, allowing the output data and clock frequency to spread over a specified range to reduce EMI. The single-ended data and clock outputs are programmable for a frequency spread of $\pm 2\%$, $\pm 4\%$, or no spread. The spread-spectrum function is also available when the MAX9242/MAX9244/MAX9246/MAX9254 operate in non-DC-balanced mode. The modulation rate of the spread is 32kHz for a 33MHz LVDS clock input and scales linearly with frequency. The single-ended outputs have a separate supply, allowing +1.8V to +5V output logic levels.

The MAX9254 features high output drive current for both data and clock outputs for faster transition times in the presence of heavy capacitive loads.

The MAX9242/MAX9244/MAX9246/MAX9254 feature programmable DC balance, allowing isolation between a serializer and deserializer using AC-coupling. The MAX9242/MAX9244/MAX9246/MAX9254 operate with the MAX9209/MAX9213 serializers and are available with a rising-edge strobe (MAX9242) or falling-edge strobe (MAX9244/MAX9246/MAX9254). The LVDS inputs meet ISO 10605 ESD specifications with $\pm 30\text{kV}$ Air-Gap Discharge and $\pm 6\text{kV}$ Contact Discharge ratings.

Applications

Automotive Navigation Systems
Automotive DVD Entertainment Systems
Digital Copiers
Laser Printers

Selector Guide

PART	STROBE EDGE	OVER-SAMPLING	FREQUENCY RANGE	
			NON-DC BALANCE (MHz)	DC BALANCE (MHz)
MAX9242	Rising	Yes	20 to 40	16 to 34
MAX9244	Falling	Yes	20 to 40	16 to 34
MAX9246	Falling	No	8 to 20	6 to 18
MAX9254	Falling	Yes	20 to 40	16 to 34

Features

- ◆ Programmable $\pm 4\%$, $\pm 2\%$, or OFF Spread-Spectrum Output for Reduced EMI
- ◆ Programmable DC-Balanced or Non-DC-Balanced Modes
- ◆ DC Balance Allows AC-Coupling for Wider Input Common-Mode Voltage Range
- ◆ Spread Spectrum Operates in DC-Balanced or Non-DC-Balanced Mode
- ◆ High Output Drive (MAX9254)
- ◆ $\pi / 4$ Deskew by Oversampling (MAX9242/MAX9244/MAX9254)
- ◆ 16MHz-to-34MHz (DC-Balanced) and 20MHz-to-40MHz (Non-DC-Balanced) Operation (MAX9242/MAX9244/MAX9254)
- ◆ 6MHz-to-18MHz (DC-Balanced) and 8MHz-to-20MHz (Non-DC-Balanced) Operation (MAX9246)
- ◆ Rising-Edge (MAX9242) or Falling-Edge (MAX9244/MAX9246/MAX9254) Output Strobe
- ◆ High-Impedance Outputs when $\overline{\text{PWRDWN}}$ is Low Allow Output Busing
- ◆ Separate Output Supply Allows Interface to +1.8V, +2.5V, +3.3V, and +5V Logic
- ◆ LVDS Inputs Meet ISO 10605 ESD Protection at $\pm 30\text{kV}$ Air-Gap Discharge and $\pm 6\text{kV}$ Contact Discharge
- ◆ LVDS Inputs Meet IEC 61000-4-2 Level 4 ESD Protection at $\pm 15\text{kV}$ Air-Gap Discharge and $\pm 8\text{kV}$ Contact Discharge
- ◆ LVDS Inputs Conform to ANSI TIA/EIA-644 Standard
- ◆ +3.3V Main Power Supply

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX9242EUM	-40°C to +85°C	48 TSSOP	U48-1
MAX9242GUM	-40°C to +105°C	48 TSSOP	U48-1
MAX9244EUM	-40°C to +85°C	48 TSSOP	U48-1
MAX9244GUM	-40°C to +105°C	48 TSSOP	U48-1
MAX9246EUM	-40°C to +85°C	48 TSSOP	U48-1
MAX9246GUM	-40°C to +105°C	48 TSSOP	U48-1
MAX9254EUM	-40°C to +85°C	48 TSSOP	U48-1

Devices are available in lead-free packaging. Specify lead free by adding a + symbol at the end of the part number when ordering.

Pin Configuration appears at end of data sheet.



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ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)

V _{CC} , LVDSV _{CC} , PLLV _{CC}	-0.5V to +4.0V
V _{CCO}	-0.5V to +6.0V
RxIN ₋ , RxCLKIN ₋	-0.5V to +4.0V
PWRDWN	-0.5V to +6.0V
SSG, DCB	-0.5V to (V _{CC} + 0.5V)
RxOUT ₋ , RxCLKOUT	-0.5V to (V _{CCO} + 0.5V)
Continuous Power Dissipation (T _A = +70°C)	
48-Pin TSSOP (derate 16mW/°C above +70°C)	1282mW
ESD Protection	
Human Body Model (R _D = 1.5kΩ, C _S = 100pF)	
All Pins to GND	±2.5kV

IEC 61000-4-2 (R _D = 330Ω, C _S = 150pF)	
LVDS Inputs to GND (Air-Gap Discharge).....	±15kV
LVDS Inputs to GND (Contact Discharge).....	±8kV
ISO 10605 (R _D = 2.0kΩ, C _S = 330pF)	
LVDS Inputs to GND (Air-Gap Discharge).....	±30kV
LVDS Inputs to GND (Contact Discharge).....	±6kV
Operating Temperature Range	-40°C to +105°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = LVDSV_{CC} = PLLV_{CC} = +3.0V to +3.6V, V_{CCO} = +3.0V to +5.5V, PWRDWN = high; SSG = high, open, or low; DCB = high or low, differential input voltage |V_{ID}| = 0.05V to 1.2V, input common-mode voltage V_{CM} = |V_{ID} / 2| to 2.4V - |V_{ID} / 2|, unless otherwise noted. Typical values are at V_{CC} = V_{CCO} = LVDSV_{CC} = PLLV_{CC} = +3.3V, |V_{ID}| = 0.2V, V_{CM} = +1.25V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Power-Supply Range	V _{CC} , LVDSV _{CC} , PLLV _{CC}			3.0		3.6	V
Output-Supply Range	V _{CCO}			1.8		5.5	V
Worst-Case Supply Current	I _{CCW}	C _L = 8pF, worst-case pattern, V _{CC} = V _{CCO} = 3.0V to 3.6V, Figure 2 (MAX9242, MAX9244, MAX9254)	DC-balanced mode (SSG = low)	16MHz	45	61	mA
				34MHz	72	96	
			Non-DC-balanced mode (SSG = low)	20MHz	59	79	
				33MHz	80	106	
			DC-balanced mode (SSG = high or open)	16MHz	57	78	
				34MHz	93	125	
			Non-DC-balanced mode (SSG = high or open)	20MHz	71	96	
				33MHz	98	129	
			40MHz	115	145		

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MAX9242/MAX9244/MAX9246/MAX9254

DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = LVDSV_{CC} = PLLV_{CC} = +3.0V$ to $+3.6V$, $V_{CCO} = +3.0V$ to $+5.5V$, $\overline{PWRDWN} = \text{high}$; SSG = high, open, or low; DCB = high or low, differential input voltage $|V_{ID}| = 0.05V$ to $1.2V$, input common-mode voltage $V_{CM} = |V_{ID}| / 2$ to $2.4V - |V_{ID}| / 2$, unless otherwise noted. Typical values are at $V_{CC} = V_{CCO} = LVDSV_{CC} = PLLV_{CC} = +3.3V$, $|V_{ID}| = 0.2V$, $V_{CM} = +1.25V$, $T_A = +25^\circ C$.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS	
Worst-Case Supply Current	ICCW	C _L = 8pF, worst-case pattern, V _{CC} = V _{CCO} = 3.0V to 3.6V, Figure 2 (MAX9246)	DC-balanced mode (SSG = low)	6MHz	27	41	mA	
				8MHz	30	45		
				18MHz	43	61		
			Non-DC-balanced mode (SSG = low)	8MHz	33	47		
				10MHz	37	52		
				20MHz	52	73		
			DC-balanced mode (SSG = high or open)	6MHz	32	47		
				8MHz	38	57		
				18MHz	57	81		
			Non-DC-balanced mode (SSG = high or open)	8MHz	41	58		
				10MHz	46	65		
						20MHz		66
Power-Down Supply Current	ICCZ	PWRDWN = low				50	μA	
5V-TOLERANT LOGIC INPUT (PWRDWN)								
High-Level Input Voltage	V _{IH}			2.0		5.5	V	
Low-Level Input Voltage	V _{IL}			-0.3		+0.8	V	
Input Current	I _{IN}	PWRDWN = high or low level		-20		+20	μA	
Input Clamp Voltage	V _{CL}	I _{CL} = -18mA		-1.5			V	
THREE-LEVEL LOGIC INPUTS (DCB, SSG)								
High-Level Input Voltage	V _{IH}			2.5		V _{CC} + 0.3	V	
Mid-Level Input Current	I _{IM}	DCB, SSG open or connected to a driver with output in high-impedance state (Note 3)		-10		+10	μA	
Low-Level Input Voltage	V _{IL}			-0.3		+0.8	V	
Input Current	I _{IN}	DCB, SSG = high or low level, PWRDWN = high or low		-20		+20	μA	
Input Clamp Voltage	V _{CL}	I _{CL} = -18mA		-1.5			V	
SINGLE-ENDED OUTPUTS (RxOUT₋, RxCLKOUT)								
High-Level Output Voltage	V _{OH}	I _{OH} = -100μA		V _{CCO} - 0.1		V		
		I _{OH} = -2mA	RxCLKOUT (Note 4)		V _{CCO} - 0.25			
			RxOUT ₋				V _{CCO} - 0.43	
				MAX9254			V _{CCO} - 0.25	
Low-Level Output Voltage	V _{OL}	I _{OL} = 100μA		0.1		V		
		I _{OL} = 2mA	RxCLKOUT (Note 4)		0.2			
			RxOUT ₋				0.26	
				MAX9254			0.2	

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DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = LVDSV_{CC} = PLLV_{CC} = +3.0V$ to $+3.6V$, $V_{CCO} = +3.0V$ to $+5.5V$, $\overline{PWRDWN} = \text{high}$; SSG = high, open, or low; DCB = high or low, differential input voltage $|V_{ID}| = 0.05V$ to $1.2V$, input common-mode voltage $V_{CM} = |V_{ID}| / 2$ to $2.4V - |V_{ID}| / 2$, unless otherwise noted. Typical values are at $V_{CC} = V_{CCO} = LVDSV_{CC} = PLLV_{CC} = +3.3V$, $|V_{ID}| = 0.2V$, $V_{CM} = +1.25V$, $T_A = +25^{\circ}C$.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
High-Impedance Output Current	I_{OZ}	$\overline{PWRDWN} = \text{low}$, $V_{OUT} = -0.3V$ to $(V_{CCO} + 0.3V)$		-30		+30	μA
Output Short-Circuit Current (Note 5)	I_{OS}	$V_{CCO} = 3.0V$ to $3.6V$, $V_{OUT} = 0V$	RxCLKOUT (Note 4)	-10		-40	mA
			RxOUT_	-5		-20	
		$V_{CCO} = 4.5V$ to $5.5V$, $V_{OUT} = 0V$	RxCLKOUT (Note 4)	-28		-75	
			RxOUT_	-13		-37	
Output Short-Circuit Current (MAX9254) (Note 5)	I_{OS}	$V_{CCO} = 3.0V$ to $3.6V$, $V_{OUT} = 0V$	RxOUT_	-16		-51	mA
			RxCLKOUT (Note 4)				
		$V_{CCO} = 4.5V$ to $5.5V$, $V_{OUT} = 0V$	RxOUT_	-34		-93	
			RxCLKOUT (Note 4)				
LVDS INPUTS (RxIN_, RxCLKIN_)							
Differential Input High Threshold	V_{TH}	(Note 6)				50	mV
Differential Input Low Threshold	V_{TL}	(Note 6)		-50			mV
Input Current	I_{IN+} , I_{IN-}	$\overline{PWRDWN} = \text{high or low}$		-25		+25	μA
Power-Off Input Current	I_{INO+} , I_{INO-}	$V_{CC} = V_{CCO} = 0V$ or open		-40		+40	μA
Input Resistor 1	R_{IN1}	$\overline{PWRDWN} = \text{high or low}$, $V_{CC} = V_{CCO} = 0V$ or open, Figure 1	$-40^{\circ}C$ to $+85^{\circ}C$	42		78	k Ω
			$-40^{\circ}C$ to $+105^{\circ}C$	42		85	
Input Resistor 2	R_{IN2}	$\overline{PWRDWN} = \text{high or low}$, $V_{CC} = V_{CCO} = 0V$ or open, Figure 1	$-40^{\circ}C$ to $+85^{\circ}C$	246		410	k Ω
			$-40^{\circ}C$ to $+105^{\circ}C$	246		440	

AC ELECTRICAL CHARACTERISTICS

($V_{CC} = LVDSV_{CC} = PLLV_{CC} = +3.0V$ to $+3.6V$, $V_{CCO} = +3.0V$ to $+3.6V$, $C_L = 8pF$, $\overline{PWRDWN} = \text{high}$; SSG = high, open, or low; DCB = high or low, differential input voltage $|V_{ID}| = 0.1V$ to $1.2V$, input common-mode voltage $V_{CM} = |V_{ID}| / 2$ to $2.4V - |V_{ID}| / 2$, unless otherwise noted. Typical values are at $V_{CC} = V_{CCO} = LVDSV_{CC} = PLLV_{CC} = +3.3V$, $|V_{ID}| = 0.2V$, $V_{CM} = +1.25V$, $T_A = +25^{\circ}C$.) (Notes 6, 7, 8)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Rise Time	CLHT	$0.1 \times V_{CCO}$ to $0.9 \times V_{CCO}$, Figure 3	RxOUT_	2.9	4.7	6.5	ns
			RxCLKOUT	2.0	3.3	4.1	
Output Fall Time	CHLT	$0.9 \times V_{CCO}$ to $0.1 \times V_{CCO}$, Figure 3	RxOUT_	2.1	3.0	4.2	ns
			RxCLKOUT	1.10	1.94	2.70	
Output Rise Time (MAX9254)	CLHT	$0.1 \times V_{CCO}$ to $0.9 \times V_{CCO}$, Figure 3	RxOUT_	1.4	2.2	3.3	ns
Output Fall Time (MAX9254)	CHLT	$0.9 \times V_{CCO}$ to $0.1 \times V_{CCO}$, Figure 3	RxCLKOUT	1.1	1.8	2.8	ns
RxIN Skew Margin (Note 9)	RSKM	DC-balanced mode, Figure 4	16MHz	2560	3142		ps
			34MHz	900	1386		
		Non-DC-balanced mode, Figure 4	20MHz	2500	3164		
			40MHz	960	1371		

21-Bit Deserializers with Programmable Spread Spectrum and DC Balance

MAX9242/MAX9244/MAX9246/MAX9254

AC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = LVDSV_{CC} = PLLV_{CC} = +3.0V$ to $+3.6V$, $V_{CCO} = +3.0V$ to $+3.6V$, $C_L = 8pF$, $\overline{PWRDWN} = \text{high}$; SSG = high, open, or low; DCB = high or low, differential input voltage $|V_{ID}| = 0.1V$ to $1.2V$, input common-mode voltage $V_{CM} = |V_{ID}| / 2$ to $2.4V - |V_{ID}| / 2$, unless otherwise noted. Typical values are at $V_{CC} = V_{CCO} = LVDSV_{CC} = PLLV_{CC} = +3.3V$, $|V_{ID}| = 0.2V$, $V_{CM} = +1.25V$, $T_A = +25^\circ C$.) (Notes 6, 7, 8)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
RxCLKOUT High Time	RCOH	Figures 5a, 5b		0.35 x RCOP			ns
RxCLKOUT Low Time	RCOL	Figures 5a, 5b		0.35 x RCOP			ns
RxOUT Setup to RxCLKOUT	RSRC	Figures 5a, 5b		0.3 x RCOP			ns
RxOUT Hold from RxCLKOUT	RHRC	Figures 5a, 5b		0.45 x RCOP			ns
RxCLKIN to RxCLKOUT Delay	RCCD	SSG = low, Figures 6a, 6b		4.5 + (RCIP / 2)	6.5 + (RCIP / 2)	8.2 + (RCIP / 2)	ns
Deserializer Phase-Locked-Loop Set	RPLLS	Figure 7		65,600 x RCIP			ns
Deserializer Power-Down Delay	RPDD	Figure 8		100			ns
Deserializer Phase-Locked-Loop Set from SSG Change	RPLLS2	Figure 9		32,800 x RCIP			ns
Spread-Spectrum Output Frequency	$f_{RxCLKOUT}$	SSG = high, Figure 10	Maximum output frequency	$f_{RxCLKIN} + 3.6\%$	$f_{RxCLKIN} + 4.0\%$	$f_{RxCLKIN} + 4.4\%$	MHz
			Minimum output frequency	$f_{RxCLKIN} - 4.4\%$	$f_{RxCLKIN} - 4.0\%$	$f_{RxCLKIN} - 3.6\%$	
		SSG = open, Figure 10	Maximum output frequency	$f_{RxCLKIN} + 1.8\%$	$f_{RxCLKIN} + 2.0\%$	$f_{RxCLKIN} + 2.2\%$	
			Minimum output frequency	$f_{RxCLKIN} - 2.2\%$	$f_{RxCLKIN} - 2.0\%$	$f_{RxCLKIN} - 1.8\%$	
		SSG = low	$f_{RxCLKIN}$		$f_{RxCLKIN}$		
Spread-Spectrum Modulation Frequency	f_{SSM}	Figure 10		$f_{RxCLKIN} / 1016$			Hz

- Note 1:** Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground, except V_{TH} and V_{TL} .
- Note 2:** Maximum and minimum limits over temperature are guaranteed by design and characterization. Devices are production tested at $T_A = +25^\circ C$.
- Note 3:** To provide a mid level, leave the input open, or, if driven, put driver in high impedance. High-impedance leakage current must be less than $\pm 10\mu A$.
- Note 4:** RxCLKOUT limits are scaled based on RxOUT_ measurements, design, and characterization data.
- Note 5:** One output shorted at a time. Current out of the pin.
- Note 6:** V_{TH} , V_{TL} , and AC parameters are guaranteed by design and characterization, and are not production tested. Limits are set at ± 6 sigma.
- Note 7:** C_L includes probe and test jig capacitance.
- Note 8:** RCIP is the period of RxCLKIN. RCOP is the period of RxCLKOUT.
- Note 9:** RSKM is measured with less than 150ps cycle-to-cycle jitter on RxCLKIN.

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Test Circuits/Timing Diagrams

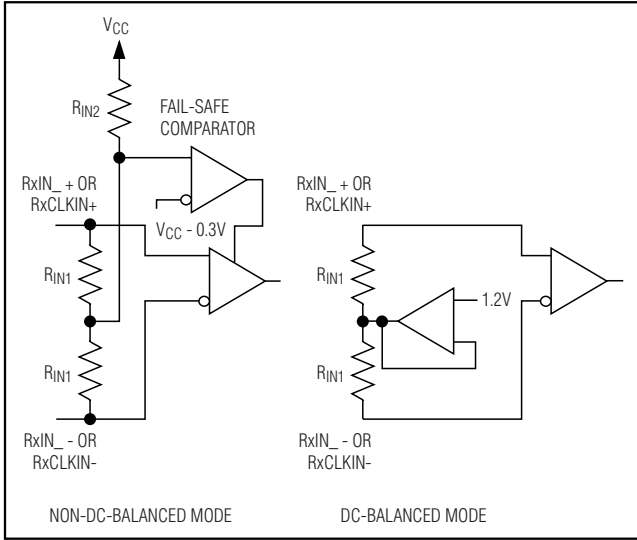


Figure 1. LVDS Input Circuits

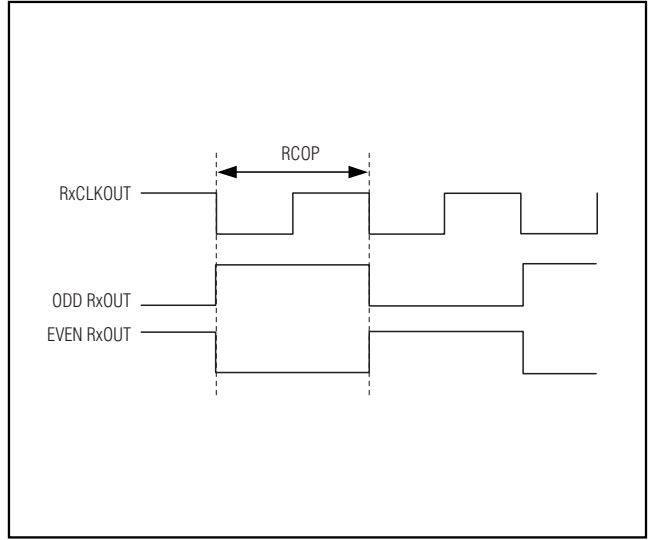


Figure 2. Worst-Case Test Pattern

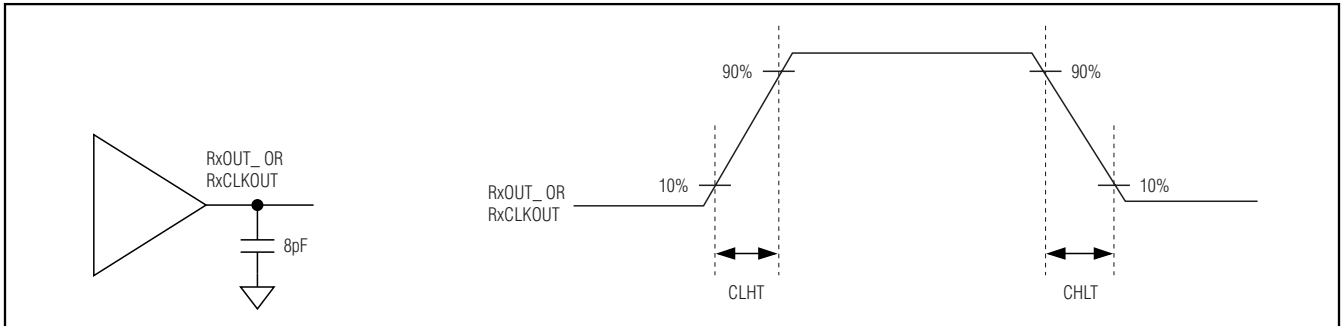


Figure 3. Output Load and Transition Times

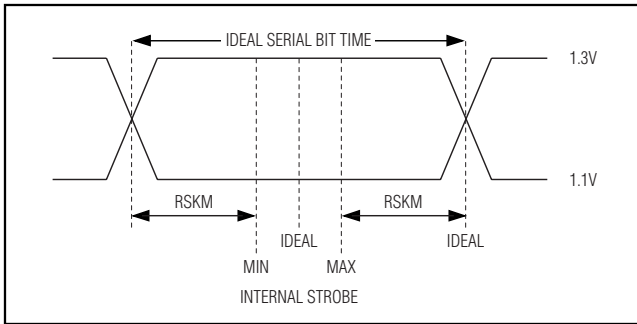


Figure 4. LVDS Receiver Input Skew Margin

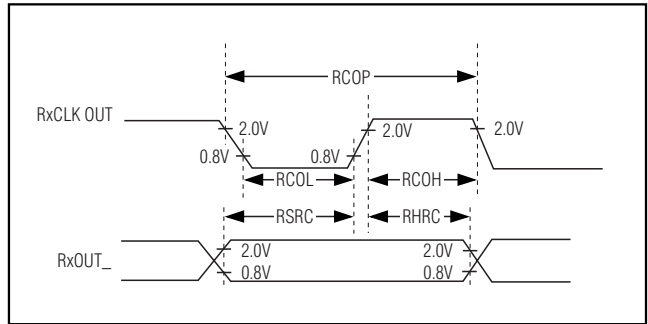


Figure 5a. Rising-Edge Output Setup/Hold and High/Low Times

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Test Circuits/Timing Diagrams (continued)

MAX9242/MAX9244/MAX9246/MAX9254

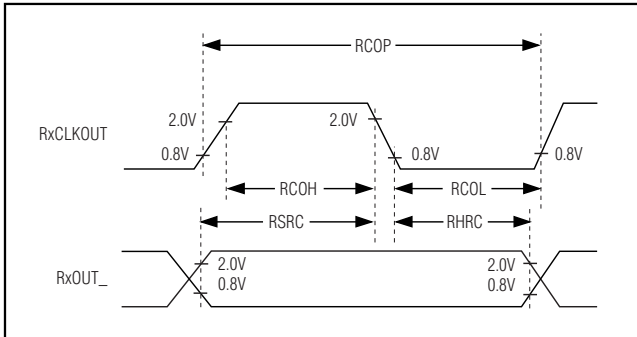


Figure 5b. Falling-Edge Output Setup/Hold and High/Low Times

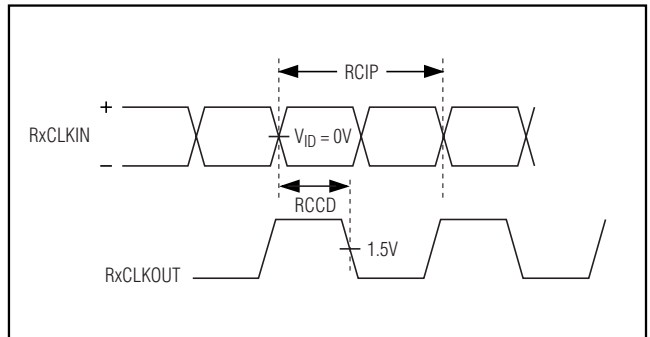


Figure 6a. Clock-IN to Clock-OUT Delay (MAX9244/MAX9246/MAX9254)

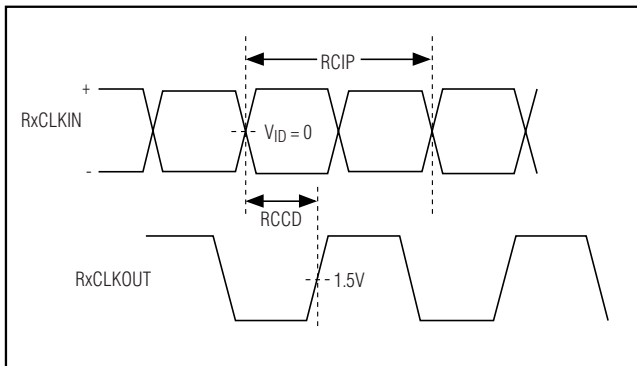


Figure 6b. Clock-IN to Clock-OUT Delay (MAX9242)

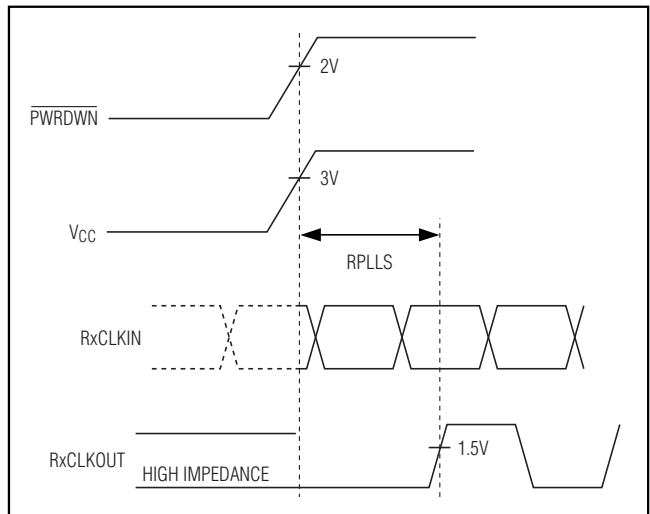


Figure 7. Phase-Locked-Loop Set Time

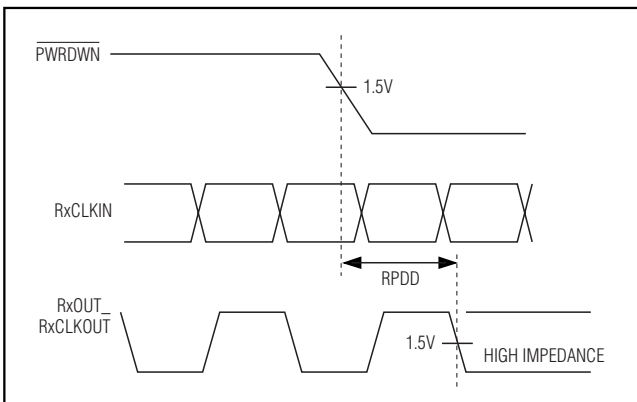


Figure 8. Power-Down Delay

21-Bit Deserializers with Programmable Spread Spectrum and DC Balance

Test Circuits/Timing Diagrams (continued)

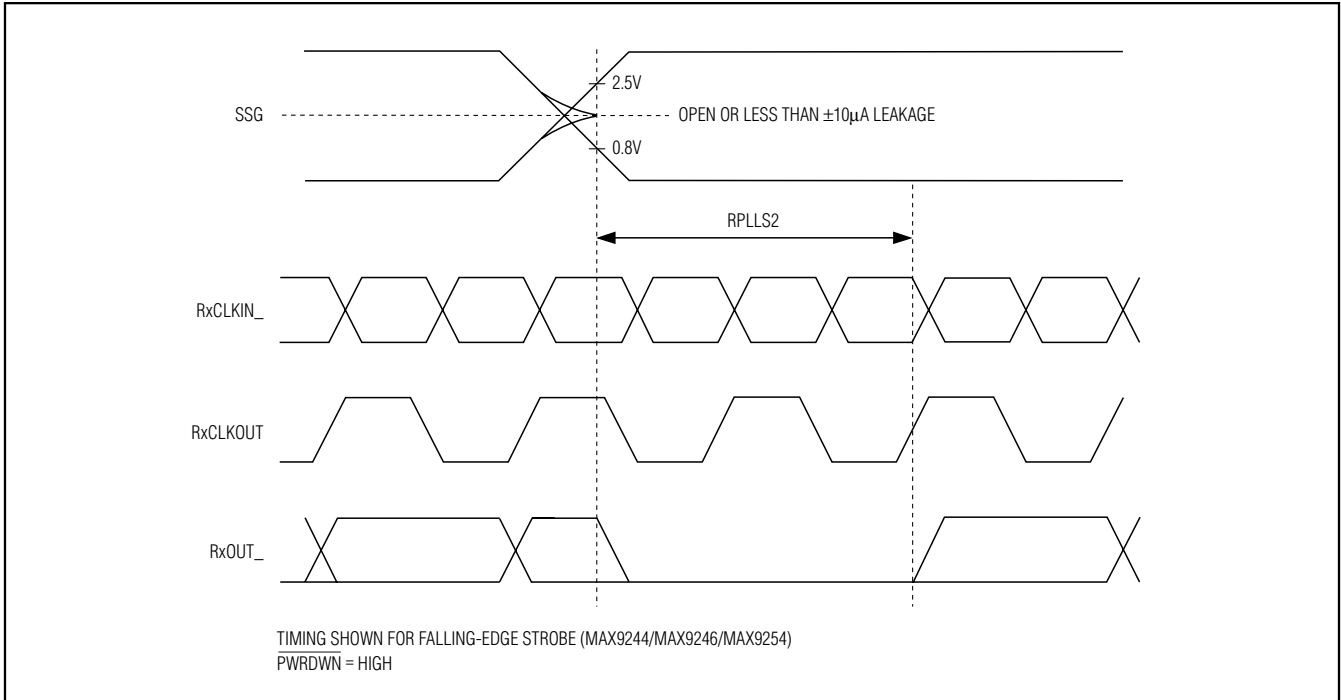


Figure 9. Phase-Locked-Loop Set Time from SSG Change

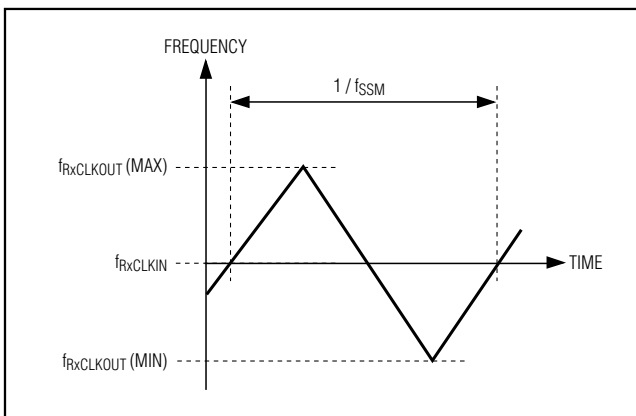


Figure 10. Simplified Modulation Profile

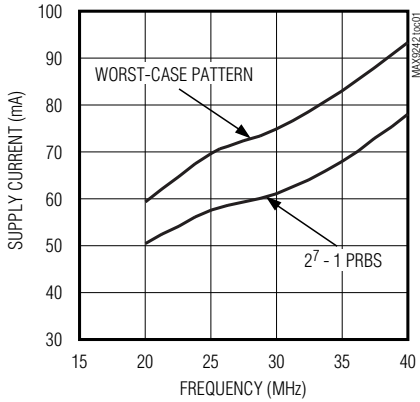
21-Bit Deserializers with Programmable Spread Spectrum and DC Balance

Typical Operating Characteristics

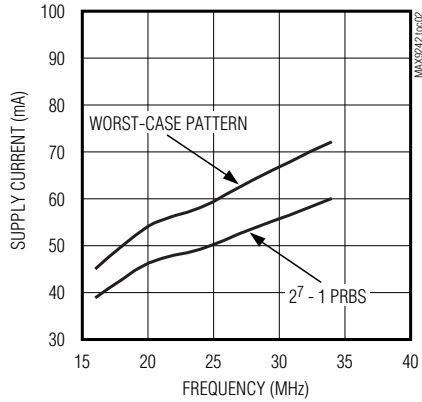
($V_{CC} = PLLV_{CC} = LVDSV_{CC} = V_{CCO} = +3.3V$, $C_L = 8pF$, $PWRDWN = high$, differential input voltage $|V_{ID}| = 0.2V$, input common-mode voltage $V_{CM} = 1.2V$, $T_A = +25^\circ C$, MAX9244/MAX9254, unless otherwise noted.)

MAX9242/MAX9244/MAX9246/MAX9254

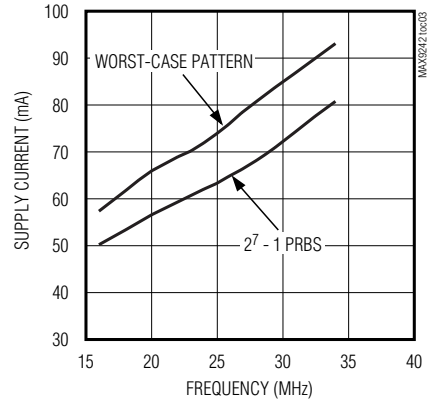
WORST-CASE AND PRBS SUPPLY CURRENT vs. FREQUENCY (NON-DC-BALANCED MODE, NO SPREAD)



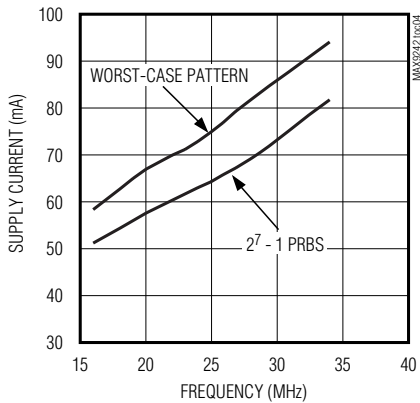
WORST-CASE AND PRBS SUPPLY CURRENT vs. FREQUENCY (DC-BALANCED MODE, NO SPREAD)



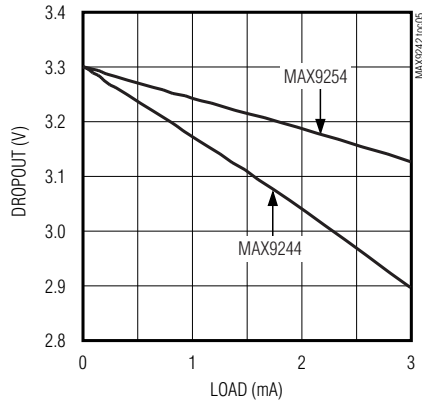
WORST-CASE AND PRBS SUPPLY CURRENT vs. FREQUENCY (DC-BALANCED MODE, 2% SPREAD)



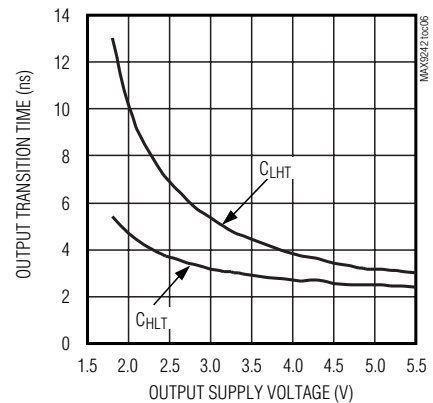
WORST-CASE AND PRBS SUPPLY CURRENT vs. FREQUENCY (DC-BALANCED MODE, 4% SPREAD)



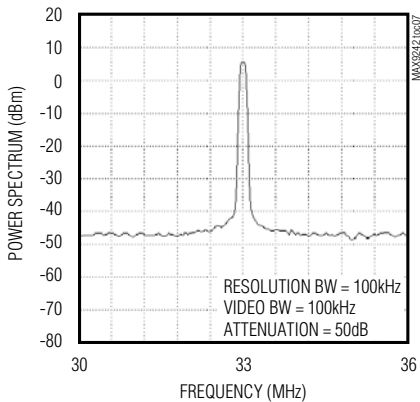
RxOUT_ OUTPUT LOADING



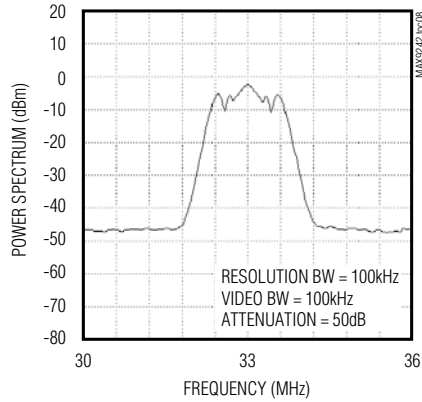
RxOUT_ TRANSITION TIME vs. OUTPUT SUPPLY VOLTAGE (V_{CCO})



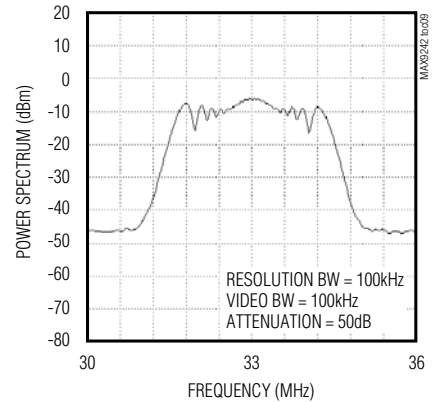
RxCLKOUT POWER SPECTRUM vs. FREQUENCY (RxCLKIN_ = 33MHz, NO SPREAD)



RxCLKOUT POWER SPECTRUM vs. FREQUENCY (RxCLKIN_ = 33MHz, 2% SPREAD)



RxCLKOUT POWER SPECTRUM vs. FREQUENCY (RxCLKIN_ = 33MHz, 4% SPREAD)

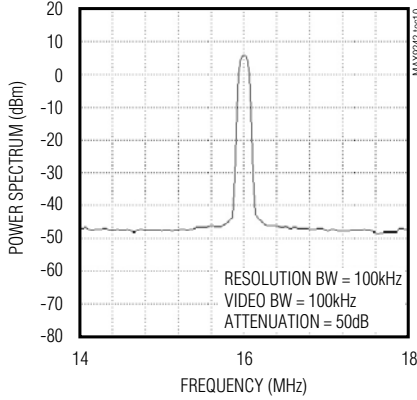


21-Bit Deserializers with Programmable Spread Spectrum and DC Balance

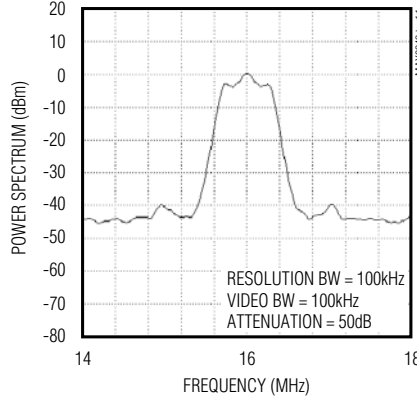
Typical Operating Characteristics (continued)

($V_{CC} = PLLV_{CC} = LVDSV_{CC} = V_{CC0} = +3.3V$, $C_L = 8pF$, $\overline{PWRDWN} = \text{high}$, differential input voltage $|V_{ID}| = 0.2V$, input common-mode voltage $V_{CM} = 1.2V$, $T_A = +25^\circ C$, MAX9244/MAX9254, unless otherwise noted.)

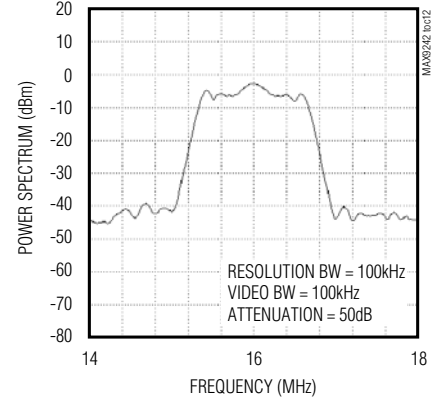
RxCLKOUT POWER SPECTRUM vs. FREQUENCY
(RxCLKIN_ = 16MHz, NO SPREAD)



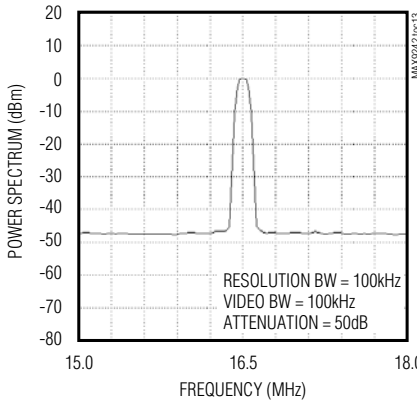
RxCLKOUT POWER SPECTRUM vs. FREQUENCY
(RxCLKIN_ = 16MHz, 2% SPREAD)



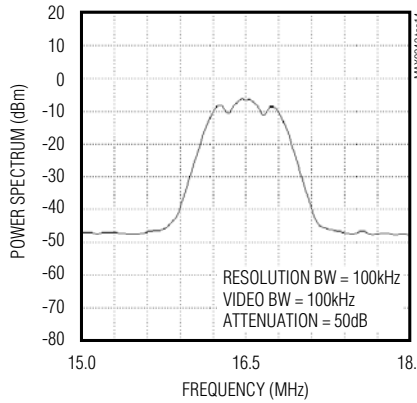
RxCLKOUT POWER SPECTRUM vs. FREQUENCY
(RxCLKIN_ = 16MHz, 4% SPREAD)



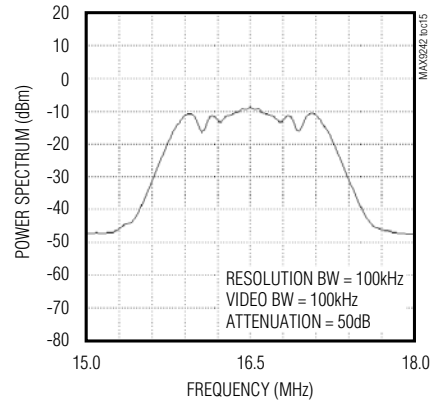
RxOUT_ POWER SPECTRUM vs. FREQUENCY
(RxCLKIN_ = 33MHz, NO SPREAD)



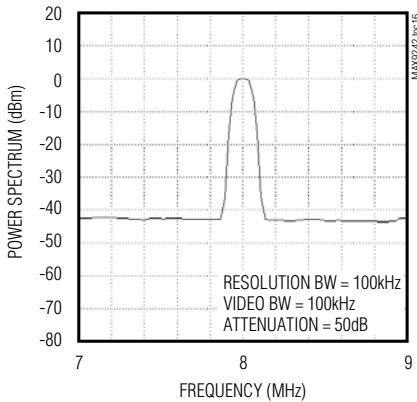
RxOUT_ POWER SPECTRUM vs. FREQUENCY
(RxCLKIN_ = 33MHz, 2% SPREAD)



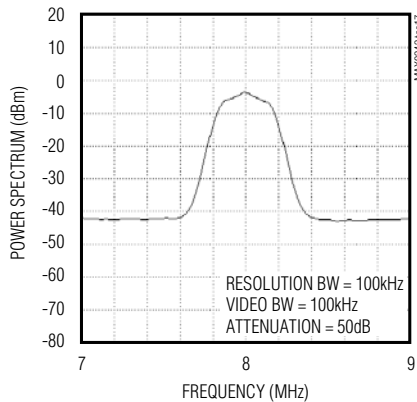
RxOUT_ POWER SPECTRUM vs. FREQUENCY
(RxCLKIN_ = 33MHz, 4% SPREAD)



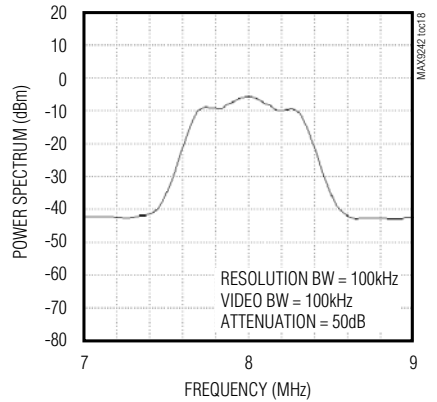
RxOUT_ POWER SPECTRUM vs. FREQUENCY
(RxCLKIN_ = 16MHz, NO SPREAD)



RxOUT_ POWER SPECTRUM vs. FREQUENCY
(RxCLKIN_ = 16MHz, 2% SPREAD)



RxOUT_ POWER SPECTRUM vs. FREQUENCY
(RxCLKIN_ = 16MHz, 4% SPREAD)



21-Bit Deserializers with Programmable Spread Spectrum and DC Balance

Pin Description

PIN	NAME	FUNCTION
1	RxOUT17	Channel 2 Single-Ended Outputs
2	RxOUT18	
3, 25, 32, 38, 44	GND	Ground
4	RxOUT19	Channel 2 Single-Ended Outputs
5	RxOUT20	
6	SSG	Three-Level-Logic, Spread-Spectrum Generator Control Input. SSG selects the frequency spread of RxCLKOUT relative to RxCLKIN (see Table 3).
7	DCB	Three-Level-Logic, DC-Balance Control Input. DCB selects DC-balanced, non-DC-balanced, or reserved operation (see Table 1).
8	RxIN0-	Inverting Channel 0 LVDS Serial-Data Input
9	RxIN0+	Noninverting Channel 0 LVDS Serial-Data Input
10	RxIN1-	Inverting Channel 1 LVDS Serial-Data Input
11	RxIN1+	Noninverting Channel 1 LVDS Serial-Data Input
12	LVDSV _{CC}	LVDS Supply Voltage. Bypass LVDSV _{CC} to GND with 0.1μF and 0.001μF capacitors in parallel as close to the pin as possible.
13, 18	LVDSGND	LVDS Ground
14	RxIN2-	Inverting Channel 2 LVDS Serial-Data Input
15	RxIN2+	Noninverting Channel 2 LVDS Serial-Data Input
16	RxCLKIN-	Inverting LVDS Parallel-Rate Clock Input
17	RxCLKIN+	Noninverting LVDS Parallel-Rate Clock Input
19, 21	PLL _{GND}	PLL Ground
20	PLL _{VCC}	PLL Supply Voltage. Bypass PLL _{VCC} to GND with 0.1μF and 0.001μF capacitors in parallel as close to the pin as possible.
22	$\overline{\text{PWRDWN}}$	5V-Tolerant LVTTTL/LVCMOS Power-Down Input. $\overline{\text{PWRDWN}}$ is internally pulled down to GND. Outputs are high impedance when $\overline{\text{PWRDWN}}$ = low or open.
23	RxCLKOUT	Parallel-Rate Clock Single-Ended Output. The MAX9242 has a rising-edge strobe. The MAX9244/MAX9246/MAX9254 have a falling-edge strobe.
24	RxOUT0	Channel 0 Single-Ended Outputs
26	RxOUT1	
27	RxOUT2	
28, 36, 48	V _{CC0}	Output Supply Voltage. Bypass each V _{CC0} to GND with 0.1μF and 0.001μF capacitors in parallel as close to the pin as possible.
29	RxOUT3	Channel 0 Single-Ended Outputs
30	RxOUT4	
31	RxOUT5	
33	RxOUT6	

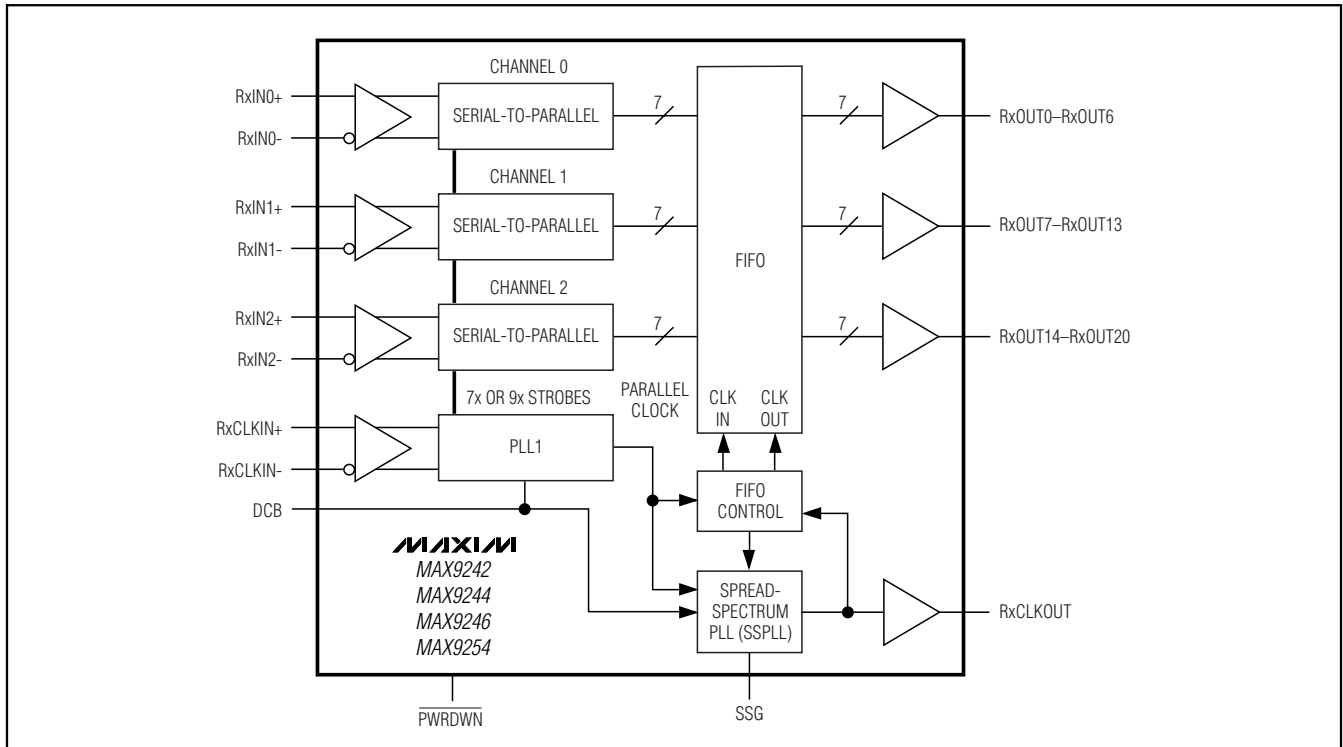
MAX9242/MAX9244/MAX9246/MAX9254

21-Bit Deserializers with Programmable Spread Spectrum and DC Balance

Pin Description (continued)

PIN	NAME	FUNCTION
34	RxOUT7	Channel 1 Single-Ended Outputs
35	RxOUT8	
37	RxOUT9	
39	RxOUT10	
40	RxOUT11	
41	RxOUT12	
42	V _{CC}	Digital Supply Voltage. Bypass V _{CC} to GND with 0.1μF and 0.001μF capacitors in parallel as close to the pin as possible.
43	RxOUT13	Channel 1 Single-Ended Output
45	RxOUT14	Channel 2 Single-Ended Outputs
46	RxOUT15	
47	RxOUT16	

Functional Diagram



21-Bit Deserializers with Programmable Spread Spectrum and DC Balance

Detailed Description

The MAX9242/MAX9244/MAX9246/MAX9254 deserialize three LVDS serial-data inputs into 21 single-ended LVC-MOS/ LVTTTL outputs. The outputs are programmable for no spread or for a spread of $\pm 2\%$ or $\pm 4\%$, relative to the LVDS input clock frequency. The MAX9242/MAX9244/MAX9254 operate at a parallel clock frequency of 16MHz to 34MHz in DC-balanced mode and 20MHz to 40MHz in non-DC-balanced mode. The MAX9246 operates at a 6MHz-to- 18MHz parallel clock frequency in DC-balanced mode and 8MHz-to-20MHz parallel clock frequency in non-DC-balanced mode. DC-balanced or non-DC-balanced operation is controlled by the DCB input. The MAX9242 has a rising-edge strobe and the MAX9244/MAX9246/MAX9254 have a falling-edge strobe.

DC Balance (DCB)

DC-balanced or non-DC-balanced operation is controlled by the DCB input (see Table 1). In the non-DC-balanced mode, each channel deserializes 7 bits every cycle of the parallel clock. In DC-balanced mode, 9 bits are deserialized every clock cycle (7 data bits + 2 DC-balanced bits). The highest serial-data rate on each channel in DC-balanced mode is $34\text{MHz} \times 9 = 306\text{Mbps}$. In non-DC-balanced mode, the maximum data rate is $40\text{MHz} \times 7 = 280\text{Mbps}$.

Table 1. DCB Function

DCB INPUT LEVEL	FUNCTION
High	Non-DC-balanced mode
Mid	Reserved
Low	DC-balanced mode

Data coding by the MAX9209/MAX9213 serializers (that are companion devices to the MAX9242/MAX9244/MAX9246/MAX9254 deserializers) limits the imbalance of ones and zeros transmitted on each channel. If +1 is assigned to each binary 1 transmitted and -1 is assigned to each binary 0 transmitted, the variation in the running sum of assigned values is called the digital sum variation (DSV). The maximum DSV for the data channels is 10. At most, 10 more zeros than ones, or 10 more ones than zeros, are ever transmitted. The maximum DSV for the clock channel is 5. Limiting the DSV and choosing the correct coupling capacitors maintain differential signal amplitude and reduces jitter due to droop on AC-coupled links.

To obtain DC balance on the data channels, the serializer parallel data is inverted or not inverted, depending on the sign of the digital sum at the word boundary. Two complementary bits are appended to each group of 7 parallel-input data bits to indicate to the MAX9242/MAX9244/MAX9246/MAX9254 deserializer whether the data bits are inverted (see Figures 11 and 12). The deserializer restores the original state of the parallel data. The LVDS clock signal alternates duty cycles of 4/9 and 5/9 to maintain DC balance.

Spread-Spectrum Generator (SSG)

The MAX9242/MAX9244/MAX9246/MAX9254 single-ended data and clock outputs are programmable for a variation of $\pm 2\%$ or $\pm 4\%$ around the LVDS input clock frequency. The modulation rate of the frequency variation is 32.48kHz for a 33MHz LVDS clock input and scales linearly with the input clock frequency (see Table 2). The spread spectrum can also be turned off. The output spread is controlled through the SSG input (see Table 3).

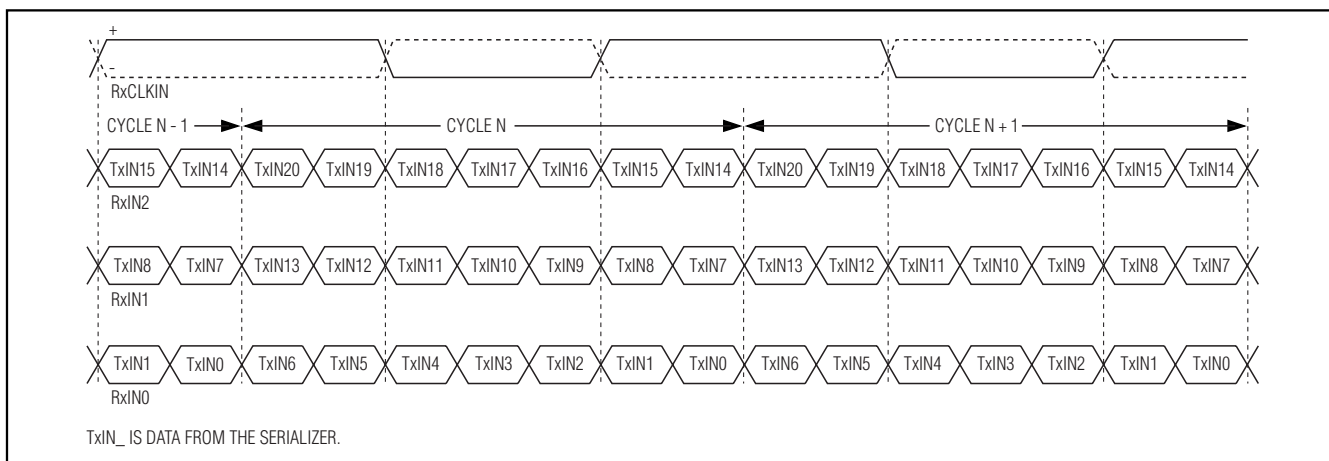


Figure 11. Deserializer Serial Input in Non-DC-Balanced Mode

21-Bit Deserializers with Programmable Spread Spectrum and DC Balance

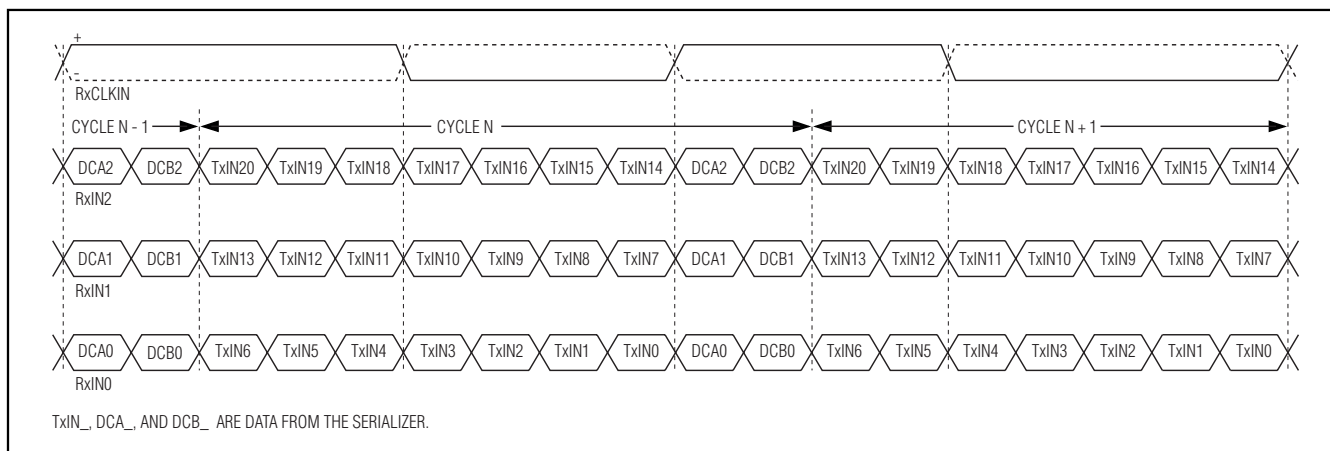


Figure 12. Deserializer Serial Input in DC-Balanced Mode

Table 2. Modulation Rate

$f_{RxCLKIN}$ (MHz)	f_M (kHz) = $f_{RxCLKIN} / 1016$
6	5.91
8	7.87
10	9.84
16	15.75
18	17.72
20	19.68
33	32.48
34	33.46
40	39.37

Table 3. SSG Function

SSG INPUT LEVEL	FUNCTION
High	RxCLKOUT frequency spread $\pm 4\%$ relative to RxCLKIN
Mid	RxCLKOUT frequency spread $\pm 2\%$ relative to RxCLKIN
Low	No spread on RxCLKOUT relative to RxCLKIN

Note: RxOUT_ data outputs are spread because RxCLKOUT strobes the output of the FIFO.

To select the mid level, leave the input open, or if driven, put the driver output in high impedance. The driver high-impedance leakage current must be less than $\pm 10\mu A$.

Any spread change causes a maximum delay time of $32,800 \times RCIP$ before output data is valid. When the spread amount is changed from $\pm 2\%$ to $\pm 4\%$ or vice-versa, the data outputs go low for one delay time (see Figure 13). Similarly, when the spread is changed from no spread to $\pm 2\%$ or $\pm 4\%$, the data outputs go low for one delay time (see Figure 14). The data outputs continue to switch but are not valid when the spread amount is changed from $\pm 2\%$ or $\pm 4\%$ to no spread (see Figure 15). The spread-spectrum function is also available when the MAX9242/MAX9244/MAX9246/MAX9254 operate in non-DC-balanced mode.

Hot Swap

When the MAX9242/MAX9244/MAX9246/MAX9254 are connected to an active serializer, they synchronize correctly. The PLL control voltage does not saturate in response to high-frequency glitches that may occur during a hot swap. The PWRDWN input on the MAX9242/MAX9244/MAX9246/MAX9254 does not need to be cycled when these devices are connected to an active serializer.

PLL Lock Time

The MAX9242/MAX9244/MAX9246/MAX9254 use two PLLs. The first PLL (PLL1) generates a 7x clock (non-DC-balanced mode) or a 9x clock (DC-balanced mode) from RxCLKIN for deserializing the LVDS inputs. The second PLL (SSPLL) is used for spread-spectrum modulation. During initial power-up, the PLL1 locks, and SSPLL locks immediately after. The PLL lock times are set by an internal counter. The maximum time to lock for each PLL is 32,800 clock periods. Power and clock should be stable to meet the lock time specification. After initialization, if the first PLL loses lock, it locks again and then the

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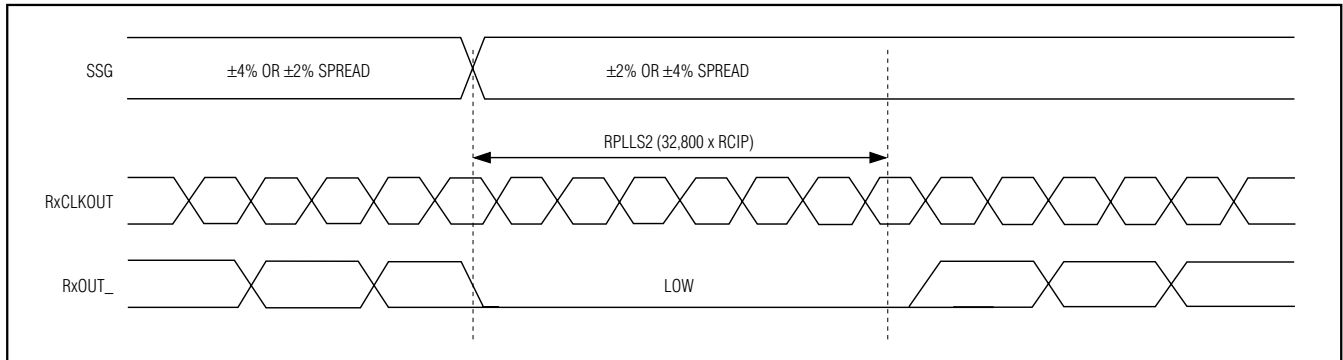


Figure 13. Output Waveforms when Spread Amount is Changed

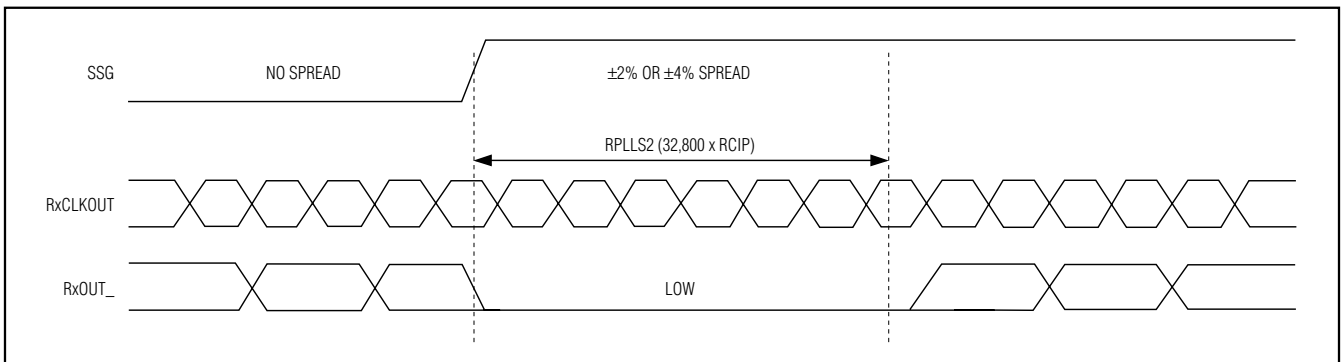


Figure 14. Output Waveforms when Spread is Added

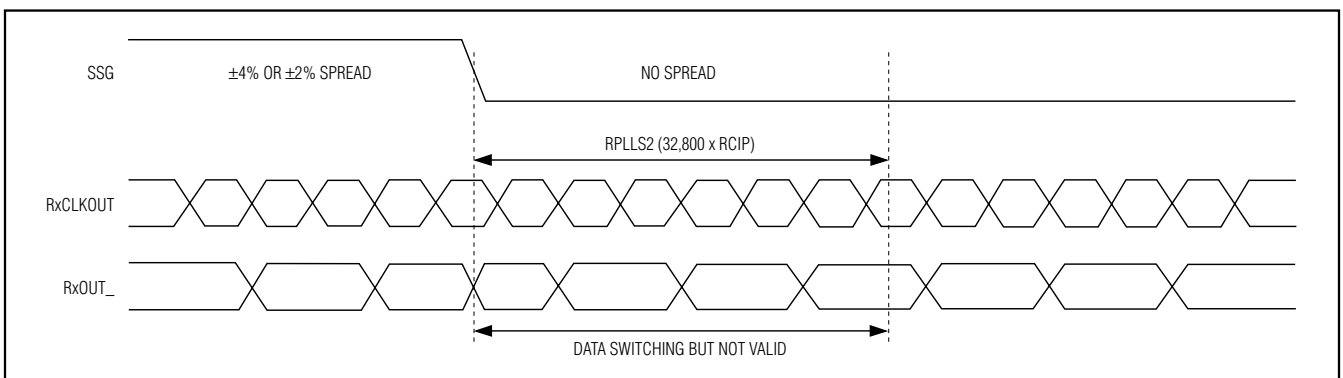


Figure 15. Output Waveforms when Spread is Removed

spread-spectrum PLL locks immediately after (see Figure 16). If the spread-spectrum PLL loses lock, it locks again with only one PLL lock delay (see Figure 17).

AC-Coupling Benefits

Bit errors experienced with DC-coupling (Figure 18) can be eliminated by increasing the receiver common-mode voltage range through AC-coupling. AC-coupling

increases the common-mode voltage range of an LVDS receiver to nearly the voltage rating of the capacitor. The typical LVDS driver output is 350mV centered on a 1.25V offset voltage, making single-ended output voltages of 1.425V and 1.075V. An LVDS receiver accepts signals from 0 to 2.4V, allowing approximately $\pm 1V$ common-mode difference between the driver and receiver on a

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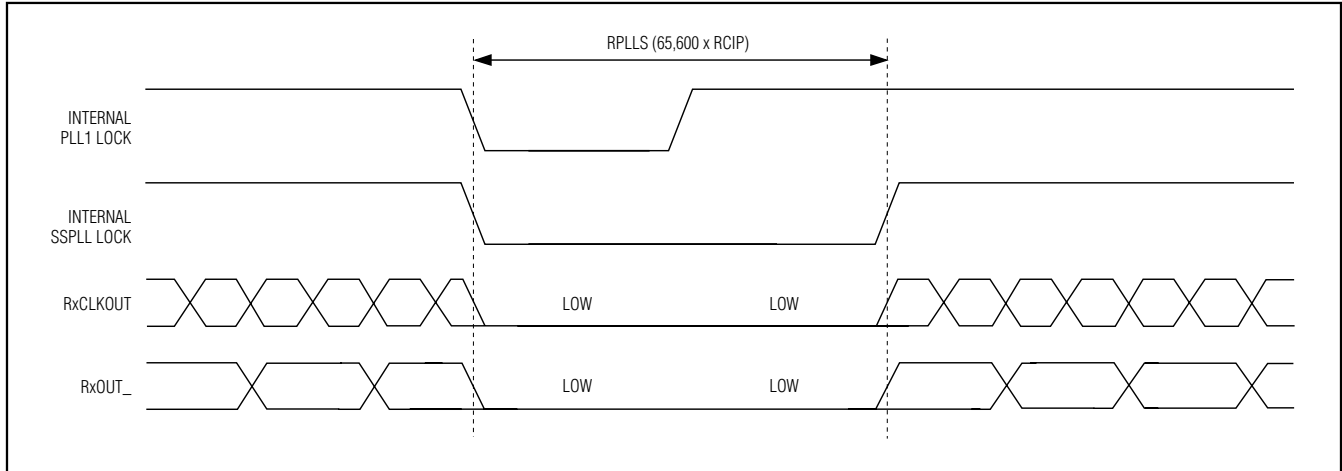


Figure 16. Output Waveforms when PLL1 Loses Lock and Locks Again

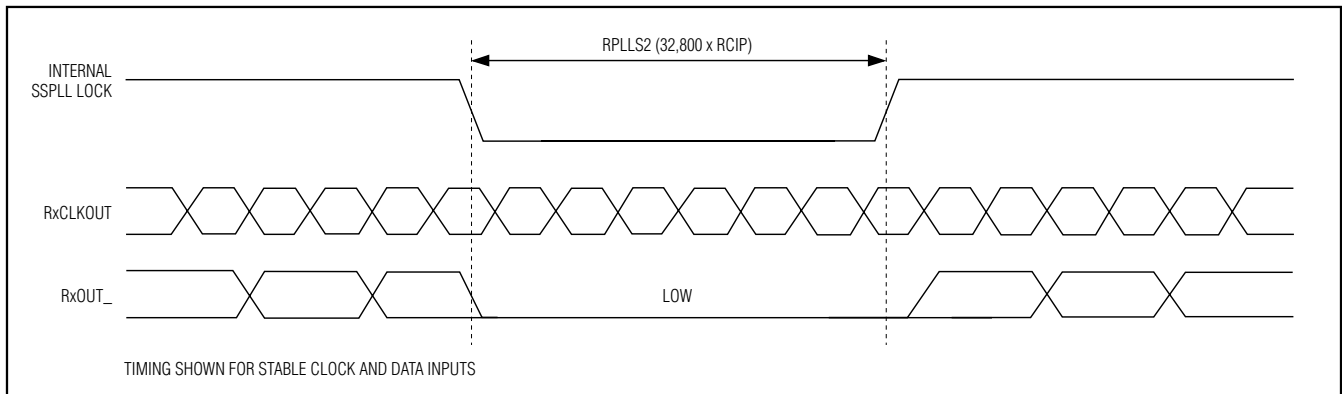


Figure 17. Output Waveforms if Spread-Spectrum PLL Loses Lock and Locks Again

DC-coupled link ($2.4V - 1.425V = 0.975V$ and $1.075V - 0V = 1.075V$). Common-mode voltage differences may be due to ground potential variation or common-mode noise. If there is more than $\pm 1V$ of difference, the receiver is not guaranteed to read the input signal correctly and may cause bit errors. AC-coupling filters low-frequency ground shifts and common-mode noise and passes high-frequency data. A common-mode voltage difference up to the voltage rating of the coupling capacitor (minus half the differential swing) is tolerated. DC-balanced coding of the data is required to maintain the differential signal amplitude and limit jitter on an AC-coupled link. A capacitor in series with each output of the LVDS driver is sufficient for AC-coupling. However, two capacitors—one at the serializer output and one at the deserializer input—provide protection in case either end of the cable is shorted to a high voltage.

Applications Information

Selection of AC-Coupling Capacitors

Voltage droop and the DSV of transmitted symbols cause signal transitions to start from different voltage levels. Because the transition time is finite, starting the signal transition from different voltage levels causes timing jitter. The time constant for an AC-coupled link needs to be chosen to reduce droop and jitter to an acceptable level.

The RC network for an AC-coupled link consists of the LVDS receiver termination resistor (R_T), the LVDS driver output resistor (R_O), and the series AC-coupling capacitors (C). The RC time constant for two equal-value series capacitors is $(C \times (R_T + R_O)) / 2$ (Figure 19). The RC time constant for four equal-value series capacitors is $(C \times (R_T + R_O)) / 4$ (Figure 20).

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MAX9242/MAX9244/MAX9246/MAX9254

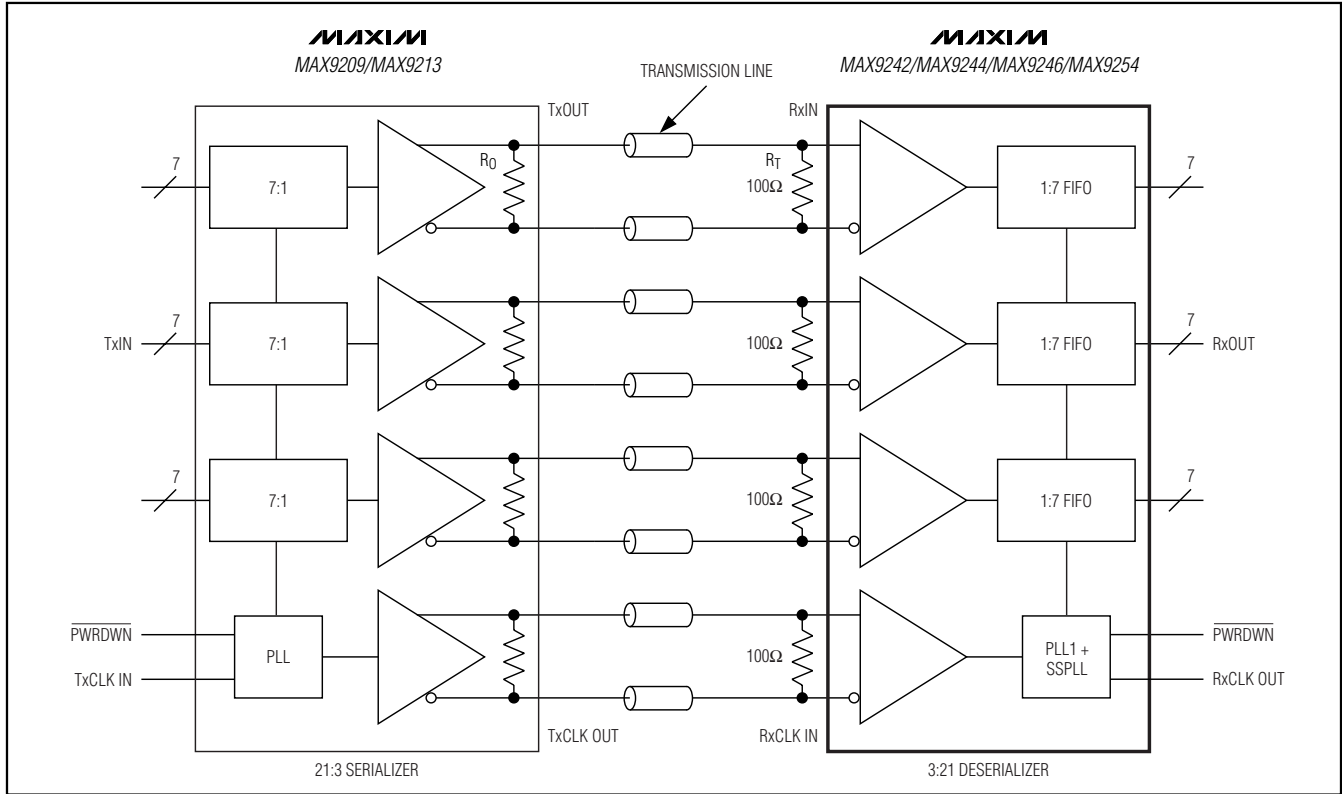


Figure 18. DC-Coupled Link, Non-DC-Balanced Mode

R_T is required to match the transmission line impedance (usually 100Ω) and R_0 is determined by the LVDS driver design (the minimum differential output resistance of 78Ω for the MAX9209/MAX9213 serializers is used in the following example). This condition leaves the capacitor selection to change the system time constant.

In the following example, the capacitor value for a 2% droop is calculated. Jitter due to this droop is then calculated assuming a 1ns transition time:

$$C = -(2 \times t_B \times DSV) / (\ln(1 - D) \times (R_T + R_0)) \quad (\text{Eq 1})$$

where:

- C = AC-coupling capacitor (F)
- t_B = bit time (s)
- DSV = digital sum variation (integer)
- ln = natural log
- D = droop (% of signal amplitude)
- R_T = termination resistor (Ω)
- R_0 = output resistance (Ω)

Equation 1 is for two series capacitors (Figure 19). The bit time (t_B) is the period of the parallel clock divided by 9.

The DSV is 10. See equation 3 for four series capacitors (Figure 20).

The capacitor for 2% maximum droop at 16MHz parallel rate clock is:

$$C = -(2 \times t_B \times DSV) / (\ln(1 - D) \times (R_T + R_0))$$

$$C = -(2 \times 6.95\text{ns} \times 10) / (\ln(1 - 0.02) \times (100\Omega + 78\Omega))$$

$$C = 0.038\mu\text{F}$$

Jitter due to droop is proportional to the droop and transition time:

$$t_J = t_T \times D \quad (\text{Eq 2})$$

where:

- t_J = jitter (s)
- t_T = transition time (s) (0 to 100%)
- D = droop (% of signal amplitude)

Jitter due to 2% droop and assumed 1ns transition time is:

$$t_J = 1\text{ns} \times 0.02$$

$$t_J = 20\text{ps}$$

The transition time in a real system depends on the frequency response of the cable driven by the serializer.

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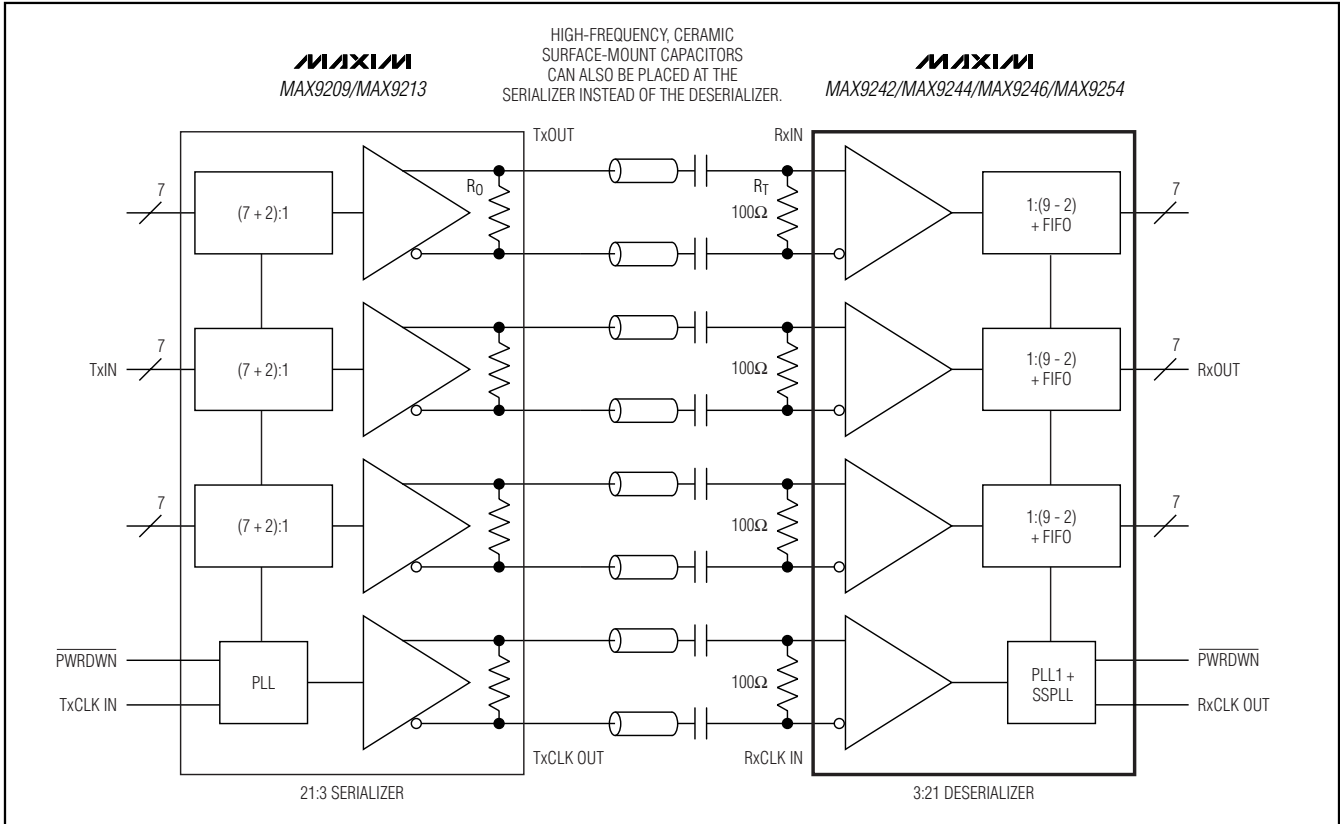


Figure 19. Two Capacitors per Link, AC-Coupled, DC-Balanced Mode

The capacitor value decreases for a higher frequency parallel clock and for higher levels of droop and jitter. Use high-frequency, surface-mount ceramic capacitors.

Equation 1 altered for four series capacitors (Figure 20) is:

$$C = -(4 \times t_B \times DSV) / (\ln(1 - D) \times (R_T + R_O)) \quad (\text{Eq 3})$$

Fail-Safe

The MAX9242/MAX9244/MAX9246/MAX9254 have fail-safe LVDS inputs in non-DC-balanced mode (Figure 1). Fail-safe drives the outputs low when the corresponding LVDS input is open, undriven and shorted, or undriven and parallel terminated. The fail-safe on the LVDS clock input drives all outputs low when power is stable. Fail-safe does not operate in DC-balanced mode.

Input Bias and Frequency Detection

In DC-balanced mode, the inverting and noninverting LVDS inputs are internally connected to +1.2V through 42kΩ (min) to provide biasing for AC-coupling (Figure 1). To prevent switching due to noise when the clock input is not driven, bias the clock inputs (RxCLKIN+,

RxCLKIN-) to differential +15mV by connecting a 10kΩ ±1% pullup resistor between the noninverting input and LVDSVCC, and a 10kΩ ±1% pulldown resistor between the inverting input and ground. These bias resistors, along with the 100Ω ±1% tolerant termination resistor, provide +15mV of differential input. The +15mV bias causes some small degradation of RSKM proportional to the slow rate of the clock input. For example, if the clock transitions 250mV in 500ps, the slew rate of 0.5mV/ps reduces RSKM by 30ps.

Unused LVDS Data Inputs

In non-DC-balanced mode, leave unused LVDS data inputs open. In non-DC-balanced mode, the input fail-safe circuit drives the corresponding outputs low, and no pullup or pulldown resistors are needed. In DC-balanced mode, at each unused LVDS data input, pull the inverting input up to LVDSVCC using a 10kΩ resistor, and pull the noninverting input down to ground using a 10kΩ resistor. Do not connect a termination resistor. The pullup and pulldown resistors drive the corresponding outputs low and prevent switching due to noise.

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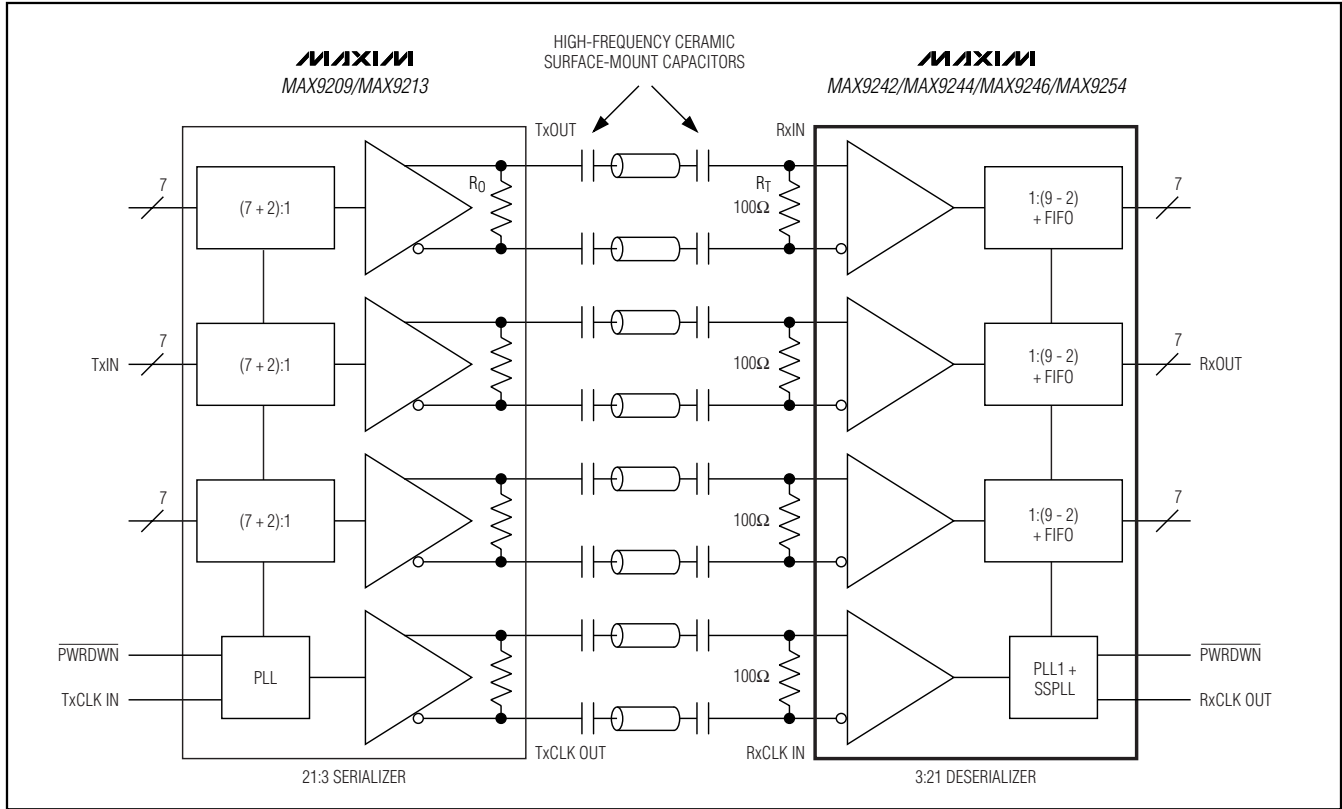


Figure 20. Four Capacitors per Link, AC-Coupled, DC-Balanced Mode

Link Power-Up Sequence

The recommended link power-up sequence is to power up the serializer, wait until the serializer PLL locks, and then power up the deserializer. This sequence prevents the deserializer from seeing an undriven or unstable input when powering up.

PWRDWN

Driving $\overline{\text{PWRDWN}}$ low puts the outputs in high impedance, stops the PLL, and reduces supply current to 50 μA or less. Driving $\overline{\text{PWRDWN}}$ high drives the outputs low until the PLL locks. The outputs of two deserializers can be bused to form a 2:1 mux with the outputs controlled by $\overline{\text{PWRDWN}}$. Wait 100ns between disabling one deserializer (driving $\overline{\text{PWRDWN}}$ low) and enabling the second one (driving $\overline{\text{PWRDWN}}$ high) to avoid contention of the bused outputs.

Power-Supply Bypassing

There are separate on-chip power domains for digital circuits, outputs, PLL, and LVDS inputs. Bypass each V_{CC} , V_{CCO} , $\text{PLL}V_{CC}$, and $\text{LVDS}V_{CC}$ with high-frequency,

surface-mount ceramic 0.1 μF and 0.001 μF capacitors in parallel as close to the device as possible, with the smallest value capacitor closest to the supply pin.

Cables and Connectors

Interconnect for LVDS typically has a differential impedance of 100 Ω . Use cables and connectors that have matched differential impedance to minimize impedance discontinuities.

Twisted-pair and shielded twisted-pair cables offer superior signal quality compared to ribbon cable and tend to generate less EMI due to magnetic field canceling effects. Balanced cables pick up noise as common mode, which is rejected by the LVDS receiver.

Board Layout

Keep the LVTTTL/LVCMOS outputs and LVDS input signals separated to prevent crosstalk. A four-layer PC board with separate layers for power, ground, LVDS inputs, and digital signals is recommended. Layout PC board traces for 100 Ω differential characteristic impedance. The trace dimensions depend on the type of

21-Bit Deserializers with Programmable Spread Spectrum and DC Balance

trace used (microstrip or stripline). Note that two 50Ω PC board traces do not have 100Ω differential impedance when brought close together—the impedance goes down when the traces are brought closer.

Route the PC board traces for an LVDS channel (there are two conductors per LVDS channel) in parallel to maintain the differential characteristic impedance. Place the termination resistor at the end of the PC board traces within a 1/4 inch of the LVDS receiver input. Avoid vias. If vias must be used, use only one pair per LVDS channel and place the via for each line at the same point along the length of the PC board traces. This way, any reflections will occur at the same time. Do not make vias into test points for ATE. Make LVDS clock and data pairs the same length on the PC board to avoid pair-to-pair skew. Make the PC board traces that make up a differential pair the same length to avoid skew within the differential pair.

5V-Tolerant Input

$\overline{\text{PWRDWN}}$ is 5V tolerant and is internally pulled down to GND. SSG and DCB are not 5V tolerant. The input voltage range for SSG and DCB is nominally ground to V_{CC} .

Skew Margin (RSKM)

Skew margin (RSKM) is the time allowed for degradation of the serial-data sampling setup and hold times by sources other than the deserializer. The deserializer sampling uncertainty is accounted for and does not need to be subtracted from RSKM. The main outside contributors of jitter and skew that subtract from RSKM are interconnect intersymbol interference, serializer pulse position uncertainty, and pair-to-pair path skew.

V_{CCO} Output Supply and Power Dissipation

The outputs have a separate supply (V_{CCO}) for interfacing to systems with 1.8V to 5V nominal input logic levels. The *DC Electrical Characteristics* table gives the maximum supply current for $V_{CCO} = 3.6V$ with 8pF load at several switching frequencies with all outputs switching in the worst-case switching pattern. The approximate incremental supply current for V_{CCO} other than 3.6V with the same 8pF load and worst-case pattern can be calculated using:

$$I_I = C_T V_I 0.5f_C \times 21 \text{ (data outputs)} \\ + C_T V_I f_C \times 1 \text{ (clock output)}$$

where:

I_I = incremental supply current

C_T = total internal (C_{INT}) and external (C_L) load capacitance

V_I = incremental supply voltage

f_C = output clock switching frequency

The incremental current is added to (for $V_{CCO} > 3.6V$) or subtracted from (for $V_{CCO} < 3.6V$) the *DC Electrical Characteristics* table maximum supply current. The internal output buffer capacitance is $C_{INT} = 6pF$. The worst-case pattern switching frequency of the data outputs is half the switching frequency of the output clock.

In the following example, the incremental supply current of the MAX9244 in spread and DC-balanced mode is calculated for $V_{CCO} = 5.5V$, $f_C = 34MHz$, and $C_L = 8pF$:

$$V_I = 5.5V - 3.6V = 1.9V$$

$$C_T = C_{INT} + C_L = 6pF + 8pF = 14pF$$

where:

$$I_I = C_T V_I 0.5f_C \times 21 \text{ (data outputs)} + C_T V_I f_C \times 1 \text{ (clock output)}$$

$$I_I = (14pF \times 1.9V \times 0.5 \times 34MHz \times 21) + (14pF \times 1.9V \times 34MHz)$$

$$I_I = 9.5mA + 0.9mA = 10.4mA.$$

The maximum supply current in DC-balanced mode for $V_{CC} = V_{CCO} = 3.6V$ at $f_C = 34MHz$ is 125mA (from the *DC Electrical Characteristics* table). Add 10.4mA to get the total approximate maximum supply current at $V_{CCO} = 5.5V$ and $V_{CC} = 3.6V$.

If the output supply voltage is less than $V_{CCO} = 3.6V$, the reduced supply current can be calculated using the same formula and method.

At high switching frequency, high supply voltage, and high capacitive loading, power dissipation can exceed the package power dissipation rating. Do not exceed the maximum package power dissipation rating. See the *Absolute Maximum Ratings* for maximum package power dissipation capacity and temperature derating.

Rising- or Falling-Edge Output Strobe

The MAX9242 has a rising-edge output strobe, which latches the parallel output data into the next chip on the rising edge of RxCLKOUT. The MAX9244/MAX9246/MAX9254 have a falling-edge output strobe, which latches the parallel output data into the next chip on the falling edge of RxCLKOUT. The deserializer output strobe polarity does not need to match the serializer input strobe polarity.

Three-Level Logic Inputs

SSG and DCB (DCB mid level is reserved) are three-level-logic inputs. A logic-high input voltage must be greater than +2.5V and a logic-low input voltage must be less than +0.8V. A mid-level logic is recognized by the MAX9242/MAX9244/MAX9246/MAX9254 when the input is left open or connected to a driver in a high-impedance state. A weak inverter on the input stage of

21-Bit Deserializers with Programmable Spread Spectrum and DC Balance

SSG and DCB provides the proper mid-level voltage under conditions of low input current. The mid-level input current must not be greater than $\pm 10\mu\text{A}$, and the mid-level logic state cannot be driven with an external voltage source.

IEC 61000-4-2 Level 4 and ISO 10605 ESD Protection

The MAX9242/MAX9244/MAX9246/MAX9254 ESD tolerance is rated for Human Body Model, IEC 61000-4-2 and ISO 10605. The ISO 10605 and IEC 61000-4-2 standards specify ESD tolerance for electronic systems. All LVDS inputs on the MAX9242/MAX9244/MAX9246/MAX9254 meet ISO 10605 ESD protection at $\pm 30\text{kV}$ Air-Gap Discharge and $\pm 6\text{kV}$ Contact Discharge and IEC 61000-4-2 ESD protection at $\pm 15\text{kV}$ Air-Gap Discharge and $\pm 8\text{kV}$ Contact Discharge. All other pins meet the Human Body Model ESD tolerance of $\pm 2.5\text{kV}$. The Human Body Model discharge components are $C_S = 100\text{pF}$ and $R_D = 1.5\text{k}\Omega$ (Figure 21). The IEC 61000-4-2 discharge components are $C_S = 150\text{pF}$ and $R_D = 330\Omega$ (see Figure 22). The ISO 10605 discharge components are $C_S = 330\text{pF}$ and $R_D = 2\text{k}\Omega$ (Figure 23).

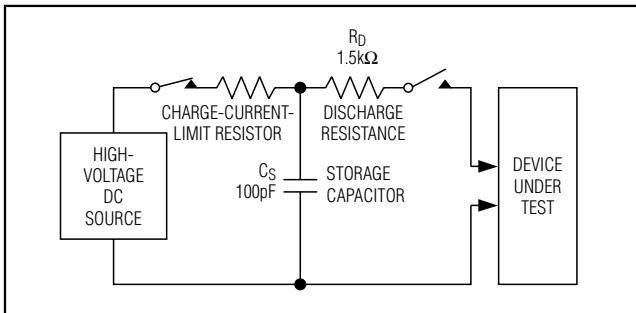


Figure 21. Human Body ESD Test Circuit

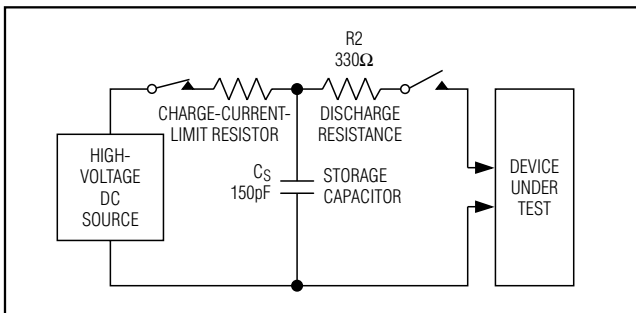


Figure 22. IEC 61000-4-2 Contact Discharge ESD Test Circuit

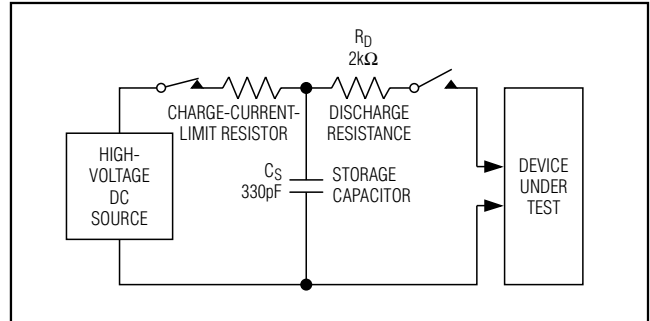
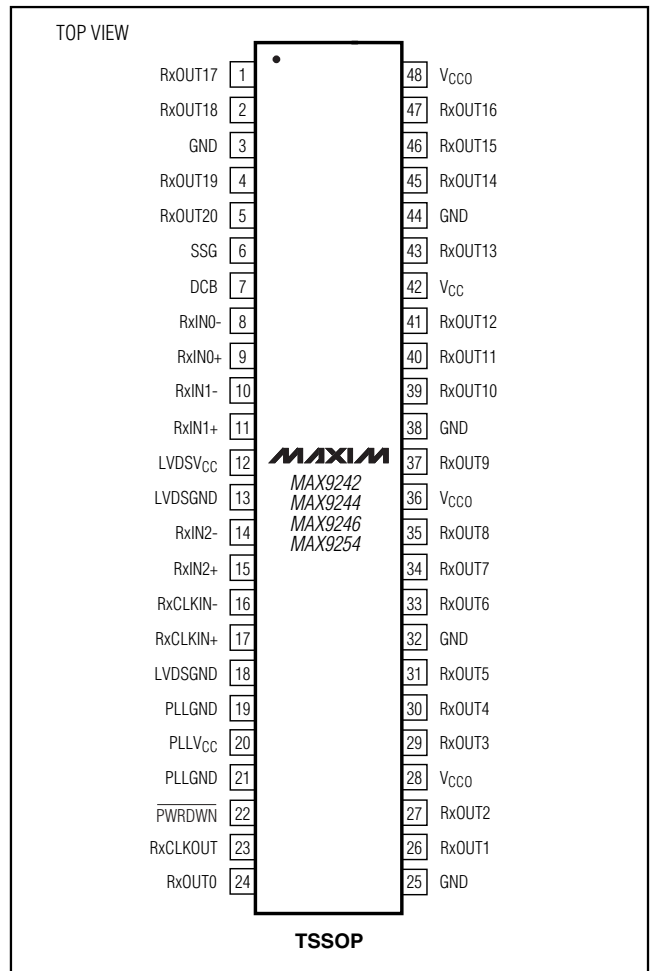


Figure 23. ISO 10605 Contact Discharge ESD Test Circuit

Pin Configuration



Chip Information

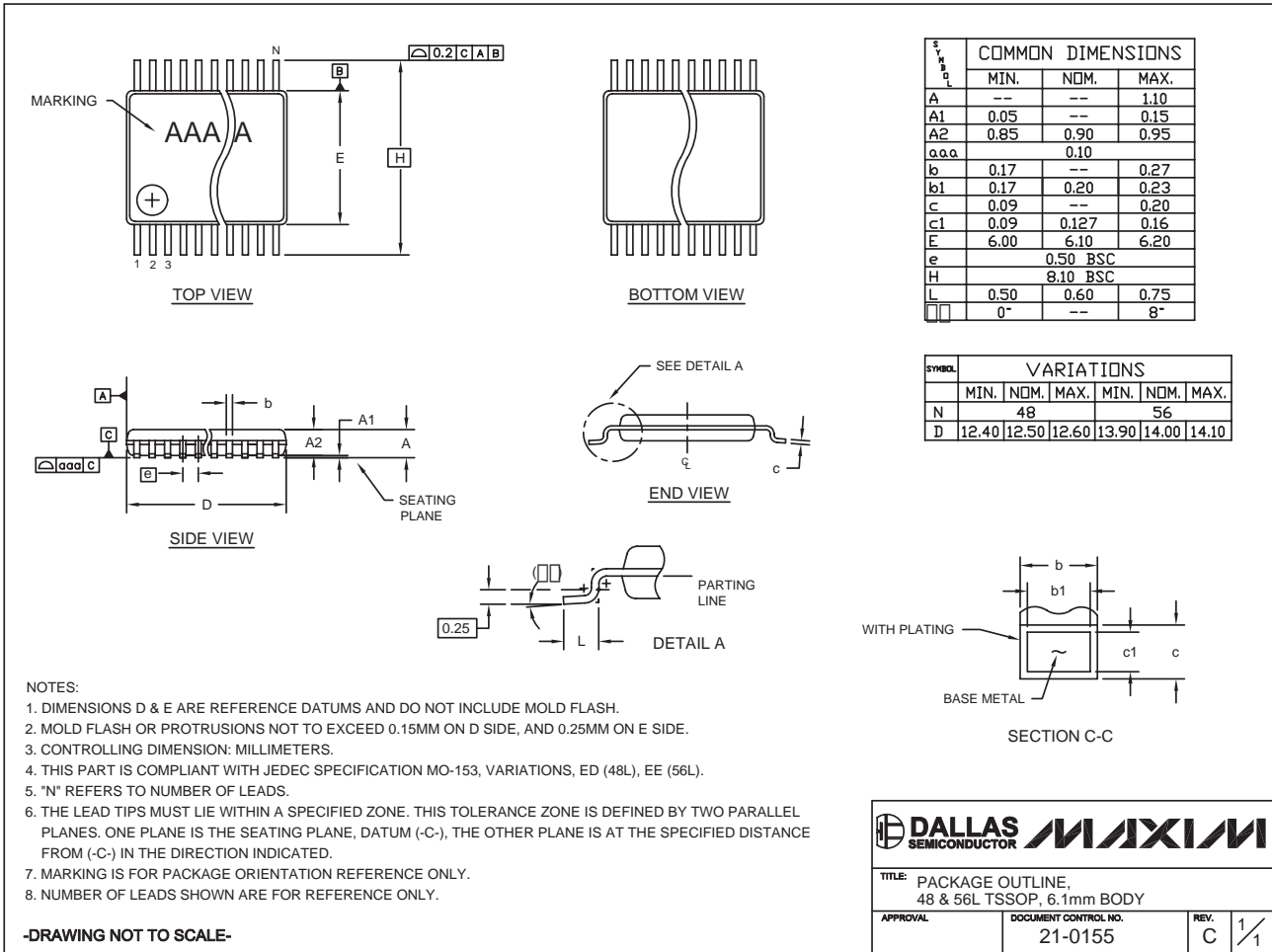
PROCESS: CMOS

MAX9242/MAX9244/MAX9246/MAX9254

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Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



48L TSSOP-EPS

Revision History

Pages changed at Rev 1: 1-4, 7-14, 17-22

Pages changed at Rev 2: 1, 2, 4, 22

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