P29FCT818/A (P29PCT818/A)
HIGH SPEED DIAGNOSTIC SCAN REGISTERS

FEATURES

- Function, Pinout, and Drive Compatible with the FCT and F Logic
- FCT-C speed at 9.0ns max. (Com'l)
  FCT-A speed at 13.0ns max. (Com'l)
- CMOS V_{OH} Levels for Low Power Consumption
  — Typically 1/3 of FAST Bipolar Logic
- Edge-rate Control Circuitry for Significantly Improved Noise Characteristics
- ESD protection exceeds 2000V
- Inputs and Outputs Interface Directly with TTL, NMOS, and CMOS Devices
- Outputs Meet Levels Required for CMOS Static RAM Low Power Standby Mode
- 24 mA Sink Current (Com'l), 20 mA (Mil)
  3 mA Source Current (Com'l), 3 mA (Mil)
- High Speed 8-Bit General Purpose Registers
- High Speed 8-Bit Serial Scan Registers
  — Expandable to Wider Widths
- Functionally Equivalent to Bipolar 29818 Type Devices
- Manufactured in 0.8 micron PACE Technology™

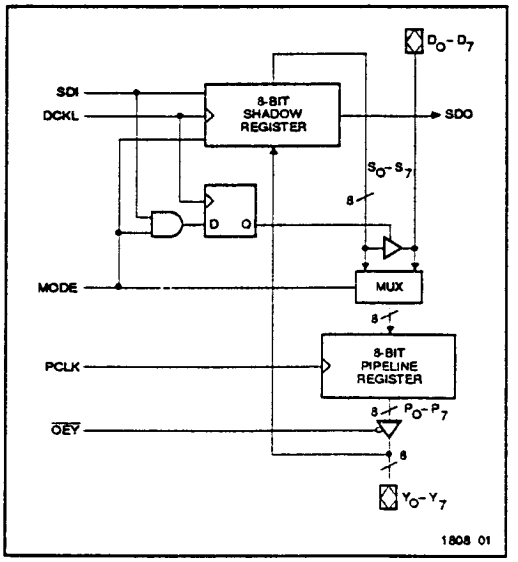
DESCRIPTION

The 'FCT818 each contain a high speed 8-bit general-purpose data pipeline register and a high speed 8-bit shadow register. The general-purpose register can be used in an 8-bit wide data path for a normal system application. The shadow register is designed for applications, such as diagnostics in sequential circuits, where it is desirable to load known data at a specific location in the circuit and to read the data at that location.

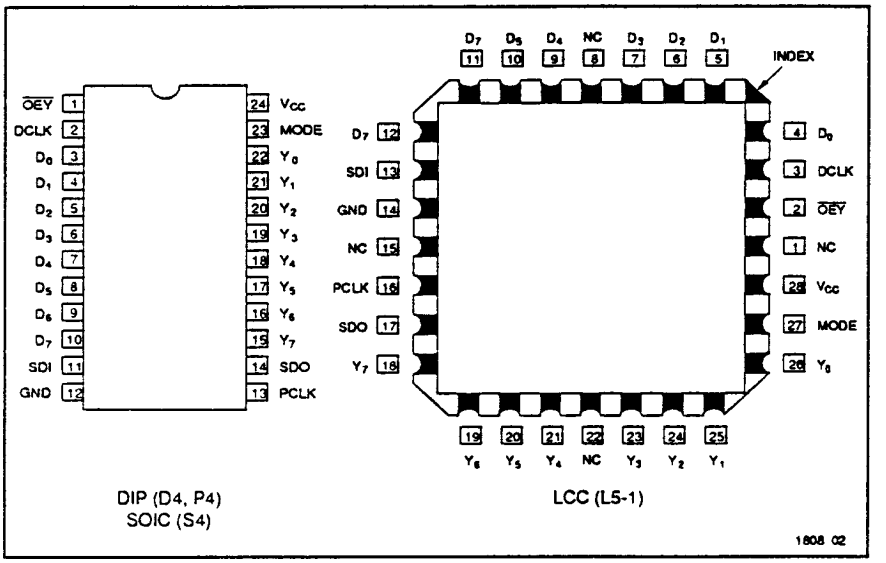
The shadow registers can load data from the output of the 'FCT818, and can be used as a right-shift register with bit-serial input SDI and output SDO, using DCLK. The data register input is multiplexed to enable loading from the shadow register or from the data input pins using PCLK. Note that data can be loaded simultaneously from the shadow register to the pipeline register, and from the pipeline register to the shadow register provided set-up and hold time requirements are satisfied with respect to the two independent clock inputs.

In a typical application, the general-purpose register in the 'FCT818 replaces an 8-bit data register in the normal data path of a system. The shadow register is placed in an auxiliary bit-serial loop which is used for diagnostics. During diagnostic operation, data is shifted serially into the shadow register, then transferred to the general-purpose register to load a known value into the data path. To read the contents at that point in the data path, the data is transferred from the data register into the shadow register, then shifted serially in the auxiliary diagnostic loop to make it accessible to the diagnostics controller. This data is then compared with the expected value to diagnose faulty operation of the sequential circuit.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



The contents of the shadow register can also be output by enabling the 8-bit wide D input/output port. In an application such as micro-program testing, the microinstruction register is formed using the general-purpose registers of 'FCT818 devices with cascaded shadow registers. To modify the microinstruction register, the corrected instruction word is shifted serially into the shadow registers and then transferred into the data registers. This word is also loaded easily into the Writeable Control Store (WCS) by enabling the D output from the shadow registers.

The 'FCT818 are manufactured with PACE Technology which is Performance Advanced CMOS Engineered to use 0.8 micron effective channel lengths giving 500 picoseconds loaded* internal gate delays. PACE Technology includes two-level metal and epitaxial substrates. In addition to very high performance and very high density, this technology features latch-up protection and single-event-upset protection, and is supported by a Class 1 facility for volume production.

The 'FCT818 are available in 24-pin 300 mil DIP and in 28-Pad 450 x 450 mil LCC packages providing excellent board level densities.

* For a fan-in/fan-out of 4 at 85°C junction temperature and 5.0V supply. For a fan-in/fan-out of 1, the internal gate delay is 200 picoseconds at room temperature and 5.0V supply.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.35		V		All inputs
V_{CD}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military/Commercial (CMOS)	V_{CC} – 0.2	V_{CC}		V	MIN	I_{OH} = –300µA
		Military/Commercial (Outputs D0–D7,SD0)	2.4	4.3		V	MIN	I_{OH} = –1mA
		Military (TTL)	2.4	4.3		V	MIN	I_{OH} = –3mA
		Commercial (TTL)	2.4	4.3		V	MIN	I_{OH} = –3mA
V_{OL}	Output LOW Voltage	Military/Commercial (CMOS)		V_{CC}	0.2	V	MIN	I_{OL} = 300µA
		Military (Outputs D0–D7,SD0)		0.3	0.5	V	MIN	I_{OL} = 4mA
		Commercial (Outputs D0–D7,SD0)		0.3	0.5	V	MIN	I_{OL} = 8mA
		Military (TTL)		0.3	0.5	V	MIN	I_{OL} = 20mA
		Commercial (TTL)		0.3	0.5	V	MIN	I_{OL} = 24mA
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = V_{CC}
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = GND
I_{IH}	Input HIGH Current[3]				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current[3]				–5	µA	MAX	V_{IN} = 0.5V
I_{OZH}	Off State I_{OUT} HIGH-Level Output Current				10	µA	MAX	V_{OUT} = V_{CC}
I_{OZL}	Off State I_{OUT} LOW-Level Output Current				–10	µA	MAX	V_{OUT} = GND
I_{OZH}	Off State I_{OUT} HIGH-Level Output Current[3]				10	µA	MAX	V_{OUT} = 2.7V
I_{OZL}	Off State I_{OUT} LOW-Level Output Current[3]				–10	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–15			mA	MAX	V_{OUT} = 0.0V
C_{IN}	Input Capacitance[3]			5	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[3]			9	12	pF	MAX	All outputs

1806 Tbl 01

Notes:

1. Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
3. This parameter is guaranteed but not tested.

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
I_{IN}	Input Current	–30 to +5.0	mA
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to V_{CC} + 0.5	V
V_{OUT}	Voltage Applied to Output	–0.5 to V_{CC} + 0.5	V

1808 Tbl 02

1808 Tbl 03

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

1808 Tbl 04

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1808 Tbl 05

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
I_{CC}	Quiescent Power Supply Current (CMOS inputs)	0.003	0.5	mA	V_{CC} = MAX, f_1 = 0, Outputs Open, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)		2.0	mA	V_{CC} = MAX, Outputs Open, f_1 = 0, V_{IN} = 3.4V
I_{CCD}	Dynamic Power Supply Current[3]		0.25	mA/ mHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, $\overline{OEY}$ = GND, Outputs Open, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$
I_C	Total Power Supply Current[5]		5.3	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{OEY}$ = GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$
			7.3	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{OEY}$ = GND, V_{IN} = 3.4V or V_{IN} = GND
			17.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits and Four Controls Toggling, $\overline{OEY}$ = GND, f_1 = 5MHz, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$
			30.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits and Four Controls Toggling, $\overline{OEY}$ = GND, f_1 = 5MHz, and V_{IN} = 3.4V or V_{IN} = GND

Notes can be found at the end of this data sheet.

1808 Tbl 06

AC CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter	'FCT818				'FCT818A				Units	Fig. No.
		MIL		COM'L		MIL		COM'L			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{PD}	PCLK TO Yx	—	18	—	13		12		9	ns	5
	MODE to SDO	—	18	—	16		18		16	ns	6
	SDI to SDO	—	18	—	16		18		15	ns	3
	DCLK to SDO	—	30	—	25		30		25	ns	5
t_S	Dx to PCLK	10		8		6		4		ns	4
	MODE to PCLK	15		15		15		15		ns	
	Yx to DCLK	5		5		5		5		ns	
	MODE to DCLK	12		12		12		12		ns	
	SDI to DCLK	10		10		10		10		ns	
	DCLK to PCLK	15		15		15		15		ns	
	DCLK to DCLK	45		40		45		40		ns	
t_H	Dx to PCLK	2		2		2		2		ns	4
	MODE to PCLK	0		0		0		0		ns	
	Yx to DCLK	5		5		5		5		ns	
	MODE to DCLK	5		2		5		2		ns	
	SDI to DCLK	0		0		0		0		ns	
t_{PLZ}	$\overline{OEY}$ to Yx		20		15		20		15	ns	7
	DCLK to Dx		45		45		45		45	ns	5
t_{PHZ}	$\overline{OEY}$ to Yx		30		25		30		25	ns	8
	DCLK to Dx		90		85		90		80	ns	5
t_{PZL}	$\overline{OEY}$ to Yx		20		15		20		15	ns	7
	DCLK to Dx		35		30		35		25	ns	5
t_{PZH}	$\overline{OEY}$ to Yx		20		15		20		15	ns	8
	DCLK to Dx		30		25		30		25	ns	5
t_W	PCLK (High and Low)	15		15		15		10		ns	5
	DCLK (High and Low)	25		25		25		15		ns	5

Note: AC Characteristics guaranteed with C_L = 50pF as shown in Figure 1.

1806 Tbl 07

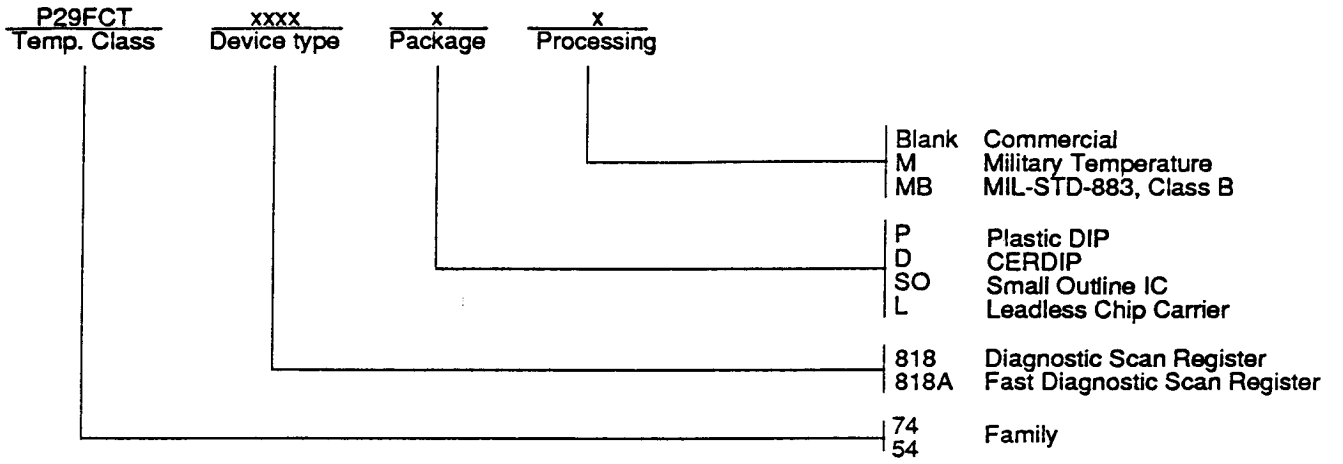
FUNCTION TABLE

Inputs				Outputs			Operation
MODE	SDI	DCLK	PCLK	SDO	Shadow Register	Pipeline Register	
L	X	⌐	X	S_7	$S_0 \leftarrow SDI$ $S_i \leftarrow S_{i-1}$	NA	Serial Shift; D_7–D_0 Output Disabled
L	X	X	⌐	S_7	NA	$P_i \leftarrow D_i$	Load Pipeline Register from Data Input
H	L	⌐	X	L	$S_i \leftarrow Y_i$	NA	Load Shadow Register from Y Output
H	H	⌐	X	H	Hold	NA	Hold Shadow Register; D_7–D_0 Output Enabled
H	X	X	⌐	SDI	NA	$P_i \leftarrow S_i$	Load Pipeline Register from Shadow Register

Note: NA = Not Applicable

1806 Tbl 08

ORDERING INFORMATION



1808 03

Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_1 = Input Frequency
N_1 = Number of Inputs at f_1
All currents are in milliamps and all frequencies are in megahertz.