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SSI 32F8101/8102/8103/8104
Low-Power Programmable Filter

Advance Information

December 1993

DESCRIPTION

The 32F810X is a high performance, low power, digitally programmable low-pass filter for applications requiring variable-frequency filtering. The device consists of three functional blocks: [1] a 7th-order 0.05° Equiripple Low-Pass filter, [2] two DACs for controlling the filter cutoff frequency and high-frequency peaking (boost), and [3] a Serial Port for programming the *fc* and Boost DACs. The device is offered in four frequency options: the 32F8101, 9-27 MHz; 32F8102, 6-18 MHz; 32F8103, 4-12 MHz; & 32F8104, 3-9 MHz.

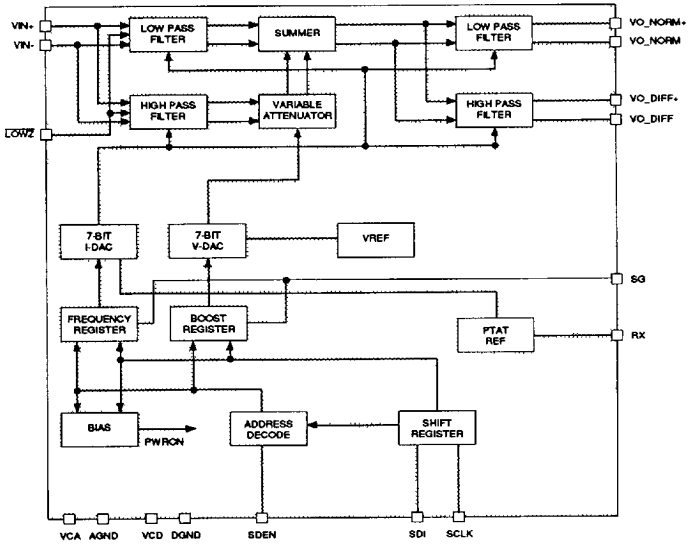
Cutoff frequency and boost are controlled by the two on-chip 7-bit DACs, which are programmed via the 3-line serial interface. Boost is programmable from 0 to 14.3 dB nominally at maximum *fc*, and is implemented using two symmetrical, real-axis zeroes. Both boost and *fc* control do not affect the flat group delay response.

The 32F810X device is ideal for variable data rate and variable frequency shaping applications. It requires only a +5V supply and has an Idle mode for minimal power dissipation. The SSI 32F810X is available in 16-lead SON, and 20-Lead SOV packages.

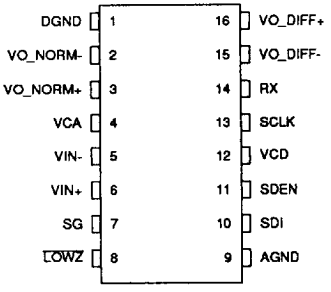
FEATURES

- **Programmable cutoff frequency:**
  - **32F8101 - 9 to 27 MHz**
  - **32F8102 - 6 to 18 MHz**
  - **32F8103 - 4 to 12 MHz**
  - **32F8104 - 3 to 9 MHz**
- **Programmable boost/equalization of 0 to 14.3 dB**
- **Matched normal and differentiated outputs**
- **± 10% *fc* accuracy**
- **± 2% maximum group delay variation**
- **Less than 1% total harmonic distortion**
- **Low-Z input switch controlled by $\overline{\text{LOWZ}}$ pin**
- **No external filter components required**
- **95 mW nominal power, <5 mW idle**

BLOCK DIAGRAM



PIN DIAGRAM



16-Lead SON

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 32F810X programmable filter consists of an electronically controlled low-pass filter with a separate differentiated low-pass output. A seven-pole, low-pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed equalization or bandwidth. Programmable bandwidth and boost/equalization is provided by internal 7-bit control DACs. High-frequency boost equalization is accomplished by a two-pole, low-pass with a two-pole, high-pass feed forward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations.

The filter implements a 0.05 degree equiripple linear phase response. The normalized transfer functions (i.e., $\omega c = 2\pi fc = 1$) are:

$$Vnorm/Vi = 13.65983 \cdot [(-Ks^2 + 1.31703)/D(s)] \cdot An$$

and

$$Vdiff/Vi = (Vnorm/Vi) \cdot (s/0.86133) \cdot Ad$$

Where D (s)=
$(S^2+1.68495s+1.31703)(S^2+1.54203\ s+2.95139)$
$(S^2+1\ .4558s+5.37034)(s+0.86133)$,

An and Ad are adjusted for a gain of 1 at $fs=(2/3)fc$.

FILTER OPERATION

Normally AC coupled differential signals are applied to the VIN± inputs of the filter, although DC coupling can be implemented. To improve settling time of the coupling capacitors, the VIN± inputs are placed into a Low-Z state when the $\overline{LOWZ}$ pin is brought high. The programmable bandwidth and boost/equalization features are controlled by internal DACs and the registers programmed through the serial port. The current reference for both DACs is set using a single 13.3 kΩ external resistor connected from pin RX to ground. The voltage at pin RX is proportional to absolute temperature (PTAT), hence the current for the DACs is a PTAT reference current.

Bandwidth Control: The programmable bandwidth is set by the filter cutoff DAC. This DAC has two separate 7-bit registers that can program the DAC value as follows:

$fc = 0.2126 \cdot$ DACF (MHz) for the 32F8101
$fc = 0.1417 \cdot$ DACF (MHz) for the 32F8102
$fc = 0.09449 \cdot$ DACF (MHz) for the 32F8103
$fc = 0.07087 \cdot$ DACF (MHz) for the 32F8104
where DACF = Cutoff Frequency Control Register value (decimal)

The filter cutoff set by the internal DAC is the unboosted 3 dB frequency. When boost/equalization is added, the actual 3 dB point will move out. Table 1 provides information on boost versus 3 dB frequency.

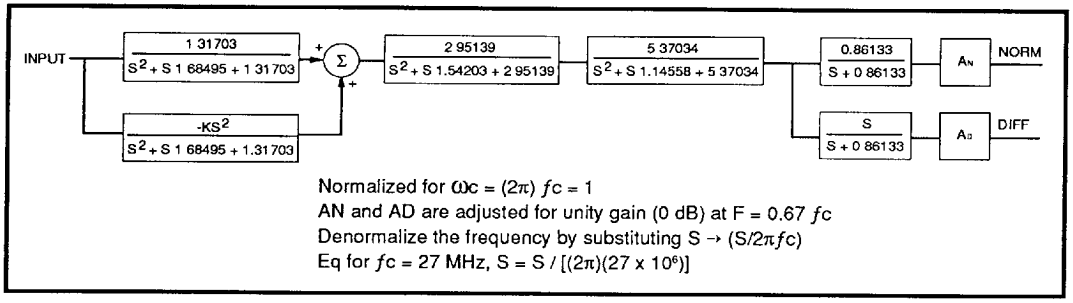


FIGURE 1: 32F8101/8102/8103/8104 Normalized Block Diagram

TABLE 1: Calculations

Typical change in f-3 dB point with boost

Boost (dB)	Gain@fc (dB)	Gain@ peak (dB)	$f$peak/fc	f-3dB/fc	K
0	-3	0.00	no peak	1.00	0
1	-2	0.00	no peak	1.21	0.16
2	-1	0.00	no peak	1.51	0.34
3	0	0.15	0.70	1.80	0.54
4	1	0.99	1.05	2.04	0.77
5	2	2.15	1.23	2.20	1.03
6	3	3.41	1.33	2.33	1.31
7	4	4.68	1.38	2.43	1.63
8	5	5.94	1.43	2.51	1.97
9	6	7.18	1.46	2.59	2.40
10	7	8.40	1.48	2.66	2.85
11	8	9.59	1.51	2.73	3.36
12	9	10.77	1.51	2.80	3.93
13	10	11.92	1.53	2.87	4.57
14	11	13.06	1.53	2.93	5.28
15	12	14.18	1.56	3.0	6.09

Notes:
1. fc is the original programmed cutoff frequency with no boost
2. f-3 dB is the new -3 dB value with boost implemented
3. $f$peak is the frequency where the amplitude reaches its maximum value with boost implemented

   i.e., fc = 9 MHz when boost = 0 dB

   if boost is programmed to 5 dB then f-3 dB = 19.8 MHz

   $f$peak = 11.07 MHz

4. $K = 1.31703 \left(10^{\frac{\text{BOOST (dB)}}{20}} - 1\right)$

BOOST/EQUALIZATION CONTROL

The programmable equalization is also controlled by an internal DAC. The 7-bit Filter Boost Control Register (FBCR) determines the amount of equalization that will be added to the 3 dB cutoff frequency, as follows:

$$\text{Boost} = 20 \log [(0.0339 \cdot \text{FBCR}) + 1] \text{ (dB)}$$
$$20 \log [(0.0283 \cdot \text{FBCR}) + (3.75 \cdot 10^{-5} \cdot \text{FBCR} \cdot \text{DACF}) + 1]$$

For example, with the DAC set for maximum output (FBCR = 7F hex or 127) at the maximum cutoff frequency (DACF = 7F hex or 127) there will be 14.3 dB of boost added at the 3 dB frequency. This will result in +10 dB of signal boost above the 0 dB baseline.

SERIAL INTERFACE OPERATION

The serial interface is a CMOS bi-directional port for reading and writing programming data from/to the internal registers of the 32F810X. For data transfers SDEN is brought high, serial data is presented at the SDATA pin, and a serial clock is applied to the SCLK pin.

After the SDEN goes high, the first 16 pulses applied to the SCLK pin will shift the data presented at the SDATA pin into an internal shift register on the rising edge of each clock. An internal counter prevents more than 16 bits from being shifted into the register. The data in the shift register is latched when SDEN goes low. If less than 16 clock pulses are provided before SDEN goes low, the data transfer is aborted.

All transfers are shifted into the serial port LSB first. The first byte of the transfer is address and instruction information. The LSB of this byte is the R/W bit which determines if the transfer is a read (1) or a write (0). The remaining seven bits determine the internal register to be accessed. The second byte contains the programming data. At initial power-up, the contents of the internal registers will be in an unknown state and they must be programmed prior to operation. During power down modes, the serial port remains active and register programming data is retained.

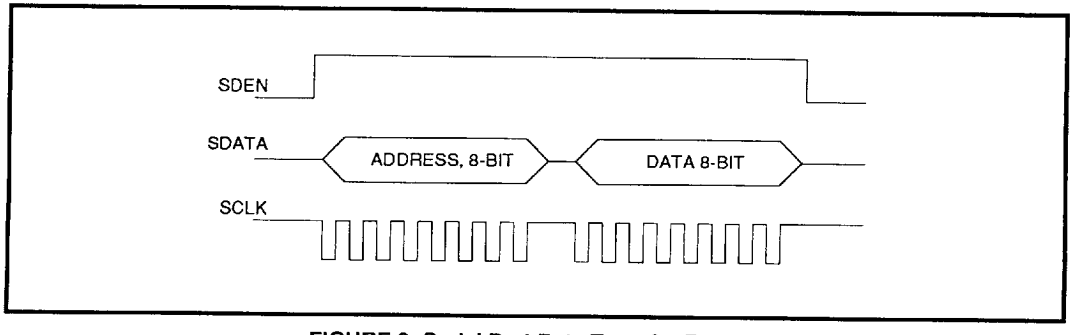


FIGURE 2: Serial Port Data Transfer Format

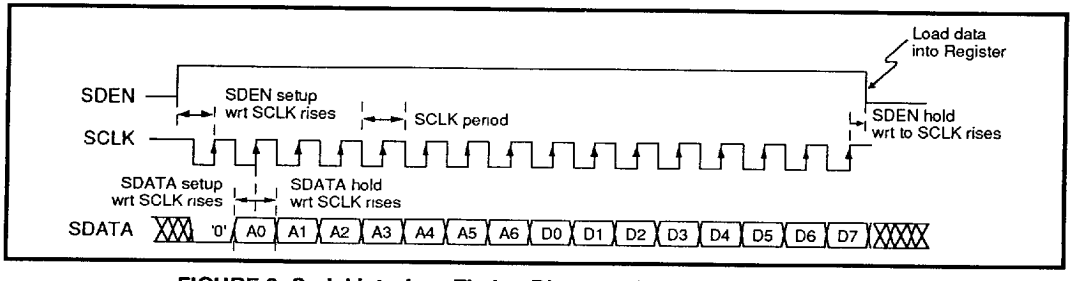


FIGURE 3: Serial Interface Timing Diagram - Writing Control Register

TABLE 2: Serial Port Register Mapping

REGISTER NAME	A6			ADDRESS			A0	R/W	D7	DATA BIT MAP						D0
POWER DOWN CONTROL	0	0	0	0	0	1	0	0	--	--	--	--	--	FILTER 1=DISABLE 0=ENABLE	--	
DATA MODE CUTOFF	0	0	0	0	0	1	1	0	*	DAC BIT 6	DAC BIT 5	DAC BIT 4	DAC BIT 3	DAC BIT 2	DAC BIT 1	DAC BIT 0
SERVO MODE CUTOFF	0	0	1	0	0	1	1	0	*	DAC BIT 6	DAC BIT 5	DAC BIT 4	DAC BIT 3	DAC BIT 2	DAC BIT 1	DAC BIT 0
FILTER BOOST, DATA	0	0	0	1	0	1	1	0	--	DAC BIT 6	DAC BIT 5	DAC BIT 4	DAC BIT 3	DAC BIT 2	DAC BIT 1	DAC BIT 0
FILTER BOOST, SERVO	0	0	1	1	0	1	1	0	--	DAC BIT 6	DAC BIT 5	DAC BIT 4	DAC BIT 3	DAC BIT 2	DAC BIT 1	DAC BIT 0

* These bits are used only for testing. They should be programmed to 0 in actual operation.

PIN DESCRIPTION

POWER SUPPLY PINS

NAME	TYPE	DESCRIPTION
VCA	-	Filter analog power supply pin
VCD	-	Serial port power supply pin
AGND	-	Filter analog ground pin
DGND	-	Serial port digital ground pin

INPUT PINS

VIN+, VIN-	I	FILTER SIGNAL INPUTS: The AGC output signals must be AC coupled into these pins.
SG	I	SERVO GATE: TTL input when high enables servo frequency and boost registers to the control DACs. When low the data frequency and boost registers are enabled.
$\overline{\text{LOWZ}}$	I	LOW_Z CONTROL: TTL input when low reduces the filter input resistance. When high, the input is at high impedance state.

OUTPUT PINS

VO_DIFF+, VO_DIFF-	O	DIFFERENTIAL DIFFERENTIATED OUTPUTS: Filter differentated outputs. These outputs are normally AC coupled.
VO_NORM+, VO_NORM-	O	DIFFERENTIAL NORMAL OUTPUTS: Filter normal low pass output signals. These outputs are normally AC coupled.
RX	-	REFERENCE RESISTOR INPUT: An external 13.3 kΩ, 1% resistor is connected from this pin to ground to establish a precise PTAT (proportional to absolute temperature) reference current for the filter.

SERIAL PORT PINS

SDEN	I/O	SERIAL DATA ENABLE: Serial enable CMOS compatible input. A high level TTL input enables the serial port.
SDI	I/O	SERIAL DATA: Serial data CMOS compatible input. NRZ programming data for the internal registers is applied to this input.
SCLK	I/O	SERIAL CLOCK: Serial clock CMOS compatible input. The clock applied to this pin is synchronized with the data applied to SDATA.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, the recommended operating conditions are as follows: 4.5V < POSITIVE SUPPLY VOLTAGE < 5.5V, 0 °C < T (ambient) < 70 °C, and 25 °C < T(junction) < 135 °C. Currents flowing into the chip are positive. Current maximums are currents with the highest absolute value.
Rx = 13.3 kΩ, Cx = 1000 pF from Rx pin to VCA. Input signals are AC-coupled into VIN±.

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device.

PARAMETER	RATING
Storage Temperature	-65 to 150 °C
Junction Operating Temperature	+130 °C
Positive Supply Voltage (Vp)	-0.5 to 7V
Voltage Applied to Logic Inputs	-0.5V to Vp + 0.5V
All other Pins	-0.5V to Vp + 0.5V

POWER SUPPLY CURRENT AND POWER DISSIPATION

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
ICC (VCA,D)	Output pins open Ta = 27 °C VP = 5.0 V, DACF = 127 Boost = 0 dB		19		mA
PWR Power Dissipation	Output pins open Ta = 27 °C VP = 5.0 V, Boost = 0 dB DACF = 127		95		mW
Sleep Mode Power	PWRON = 1			5	mW

TTL COMPATIBLE INPUTS

Input low voltage (VIL)		-0.3		0.8	V
Input high voltage (VIH)		2.0		VPD +0.3	V
Input low current (IIL)	VIL = 0.4V	-0.4			mA
Input high current (IIH)	VIH = 2.4V			100	µA

CMOS COMPATIBLE INPUTS

Input low voltage	Vp = 5.0V			1.5	V
Input high voltage	Vp = 5.0V	3.5			V

ELECTRICAL SPECIFICATIONS (continued)

SERIAL PORT

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
SCLK period		Read from serial port	140			ns
		Write to serial port	100			ns
SCLK low time	TCKL	Read from serial port	60			ns
		Write to serial port	40			ns
SCLK high time	TCKH	Read from serial port	60			ns
		Write to serial port	40			ns
Enable to SCLK	TSENS		35			ns
SCLK to disable	TSENH		100			ns
Data set-up time	TDS		15			ns
Data hold time	TDH		15			ns
SDATA tri-state delay	TSENDL				50	ns
SDATA turnaround time	TTRN		70			ns
SDEN low time	TSL		200			ns

PROGRAMMABLE FILTER CHARACTERISTICS

Filter cutoff range (32F8101)	*fc* @ -3 dB point *fc* = (0.2126 MHz) x DACF, Boost = 0 dB 42 ≤ DACF ≤ 127	9		27	MHz
Filter cutoff range (32F8102)	*fc* @ -3 dB point *fc* = (0.1417 MHz) x DACF, Boost = 0 dB 42 ≤ DACF ≤ 42	6		18	MHz
Filter cutoff range (32F8103)	*fc* @ -3 dB point *fc* = (0.09449 MHz) x DACF, Boost = 0 dB 42 ≤ DACF ≤ 127	4		12	MHz
Filter cutoff range (32F8104)	*fc* @ -3 dB point *fc* = (0.07087 MHz) x DACF, Boost = 0 dB 42 ≤ DACF ≤ 127	3		9	MHz
Filter cutoff accuracy	DACF = 42 and 125	-15		15	%
FNP,FNN differential gain AN	*f*=0.67x*fc*, boost=0 dB	0.7	1.0	1.25	V/V
FDP, FDN differential gain AD	*f*=0.67x*fc*, boost=0 dB	0.8AN		1.2AN	V/V

PROGRAMMABLE FILTER CHARACTERSITICS (continued)

PARAMETER	CONDITIONS		MIN	NOM	MAX	UNITS
Boost accuracy	6.3 dB, DACF = 42, DACS = 36		-1.0		+1.0	dB
	6.8 dB, DACF = 127, DACS = 36		-1.0		+1.0	dB
	9.5 dB, DACF = 42, DACS = 67		-1.25		+1.25	dB
	10 dB, DACF = 127, DACS = 67		-1.25		+1.25	dB
	13.6 dB, DACF = 42, DACS = 127		1.5		+1.5	dB
	14.3 dB, DACF = 127, DACS = 127		-1.5		+1.5	dB
Data mode group delay variation, DACF = 42 to 127, DACS = 0 to 127	fc = 3 to 9 MHz f = 0.2 fc to fc		-2		+2	%
	f = fc to 1.75 fc		-3		+3	%
Data mode group delay variation, DACS = 0 to 127	fc = max f = 0.2 fc to fc	32F8101	-0.5		+0.5	ns
		32F8102	-0.75		+0.75	ns
		32F8103	-1.0		+1.0	ns
		32F8104	-1.25		+1.25	ns
	fc = min f = 0.2 fc to fc	32F8101	-1.25		+1.25	ns
		32F8102	-1.9		+1.9	ns
		32F8103	-2.5		+2.5	ns
		32F8104	-3.75		+3.75	ns
	fc = max f = fc to 1.75fc	32F8101	-0.75		+0.75	ns
		32F8102	-1.15		+1.15	ns
		32F8103	-1.5		+1.5	ns
		32F8104	-1.9		+1.9	ns
	fc = min f = fc to 1.75fc	32F8101	-1.9		+1.9	ns
		32F8102	-2.85		+2.85	ns
		32F8103	-3.75		+3.75	ns
		32F8104	-5.65		+5.65	ns
Filter differential input dynamic range	THD = 1.5%, f = 0.67fc boost = 0 dB, normal and differentiated outputs		1.0			Vpp
Filter differential output dynamic range	THD = 1.5%, f = 0.67fc boost = 0 dB, normal and differentiated outputs		1.0			Vpp
Filter differential input resistance	Normal		5.0			kΩ
	Low-Z			600		Ω
Filter differential input capacitance					7.0	pF

ELECTRICAL SPECIFICATIONS (continued)

PROGRAMMABLE FILTER CHARACTERSITICS (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Output Noise Voltage: BW = 100 MHz, Rs = 50Ω					
32F8101					
differentiated output	fc = 27 MHz, boost = 0 dB		4.4	6.6	mV Rms
differentiated output	fc = 27 MHz, DACS =127		7.7	11.6	mV Rms
normal output	fc = 27 MHz, boost = 0 dB		2.5	3.8	mV Rms
normal output	fc = 27 MHz, DACS =127		3.7	5.6	mV Rms
32F8102					
differentiated output	fc = 18 MHz, boost = 0 dB		3.8	5.7	mV Rms
differentiated output	fc = 18 MHz, DACS =127		6.9	10.4	mV Rms
normal output	fc = 18 MHz, boost = 0 dB		2.2	3.3	mV Rms
normal output	fc = 18 MHz, DACS =127		3.2	4.8	mV Rms
32F8103					
differentiated output	fc = 9 MHz, boost = 0 dB		4.1	6.2	mV Rms
differentiated output	fc = 9 MHz, DACS =127		6.5	9.8	mV Rms
normal output	fc = 9 MHz, boost = 0 dB		2.2	3.3	mV Rms
normal output	fc = 9 MHz, DACS =127		3.1	4.7	mV Rms
32F8104					
differentiated output	fc = 9 MHz, boost = 0 dB		3.6	5.4	mV Rms
differentiated output	fc = 9 MHz, DACS =127		5.6	8.4	mV Rms
normal output	fc = 9 MHz, boost = 0 dB		2.0	3.0	mV Rms
normal output	fc = 9 MHz, DACS =127		2.7	4.1	mV Rms
Filter output sink current			0.5		mA
Filter output offset voltage		-200		200	mV
Filter output source current		2.0			mA
Filter output resistance	single ended			200	Ω
Rx pin voltage	Ta = 27 °C		600		mV
	Ta = 127 °C		800		mV
Rx resistance	1% fixed value		13.3		kΩ

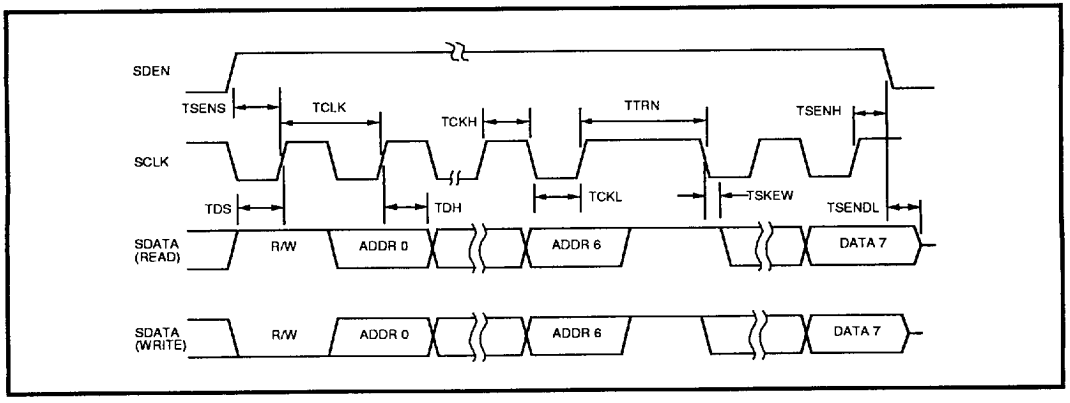
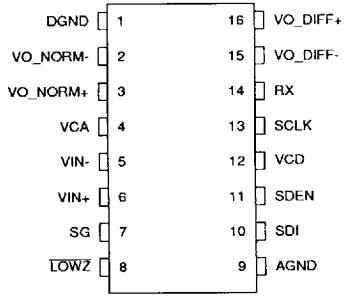


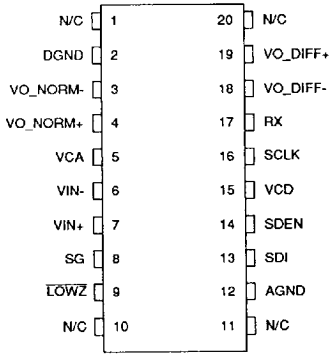
FIGURE 4: Serial Port Timing Information

PACKAGE PIN DESIGNATIONS

(Top View)



16-Lead SON



20-Lead SOV

THERMAL CHARACTERISTICS: θja

16-lead SON	100° C/W
20-lead SOV	125° C/W

CAUTION: Use handling procedures necessary for a static sensitive component.

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design

Silicon Systems, Inc , 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914