

# VN40AF, VN67AF, VN89AF n-Channel Enhancement-mode Vertical Power MOSFET

## FEATURES

- High speed, high current switching
- Current sharing capability when paralleled
- Directly interface to CMOS, DTL, TTL logic
- Simple DC biasing
- Extended safe operating area
- Inherently temperature stable
- Reliable, low cost plastic package

## ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Drain-source Voltage	
VN40AF .....	40V
VN67AF .....	60V
VN89AF .....	80V
Drain-gate Voltage	
VN40AF .....	40V
VN67AF .....	60V
VN89AF .....	80V
Continuous Drain Current (see note 1) .....	1.7A
Peak Drain Current (see note 2) .....	3.0A
Continuous Forward Gate Current .....	2.0mA
Peak-gate Forward Current .....	100mA
Peak-gate Reverse Current .....	100mA
Gate-source Forward (Zener) Voltage .....	+15V
Gate-source Reverse (Zener) Voltage .....	-0.3V
Thermal Resistance, Junction to Case .....	10.4°C/W
Continuous Device Dissipation at (or below)	
25°C Case Temperature .....	12W
Linear Derating Factor .....	96mW/°C
Operating Junction	
Temperature Range .....	-40 to +150°C
Storage Temperature Range .....	-40 to +150°C
Lead Temperature (1/16 in. from case for 10 sec) .....	+300°C

**Note 1.**  $T_C = 25^\circ\text{C}$ ; controlled by typical  $r_{DS(on)}$  and maximum power dissipation.

**Note 2.** Pulse width 80 $\mu\text{sec}$ , duty cycle 1.0%.

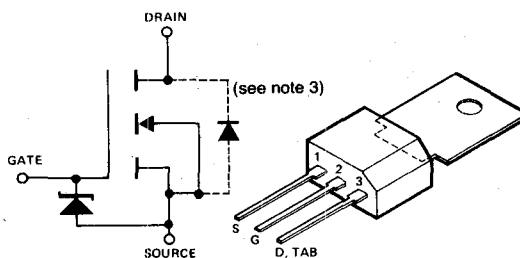
**Note 3.** The Drain-source diode is an integral part of the MOSFET structure.

## APPLICATIONS

- Switching power supplies
- DC to DC inverters
- CMOS and TTL to high current interface
- Line drivers
- Logic buffers
- Pulse amplifiers
- DC motor controllers

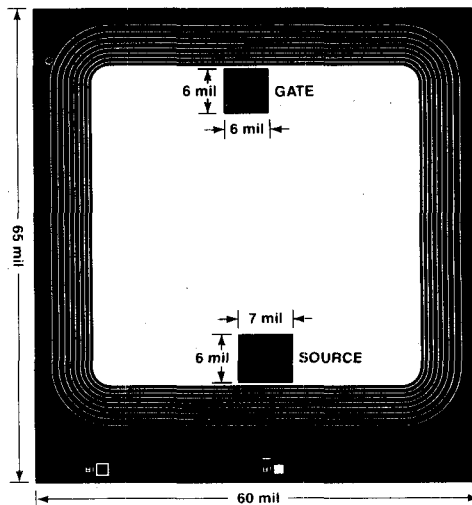
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## SCHEMATIC DIAGRAM (OUTLINE DWG. TO-202)



Body internally connected to source.  
Drain common to tab.

## CHIP TOPOGRAPHY



**ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

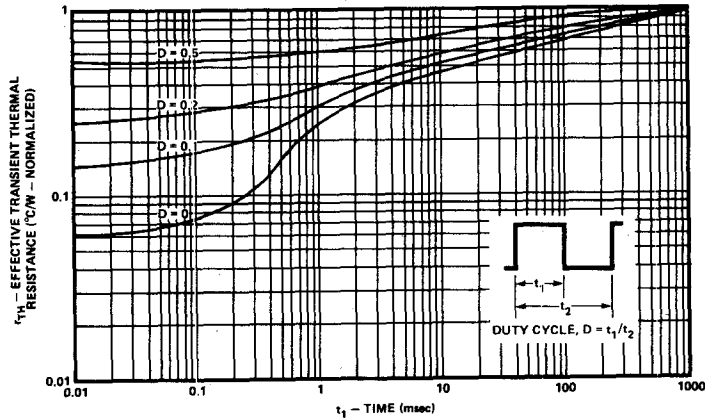
CHARACTERISTIC	VN40AF			VN67AF			VN89AF			UNIT	TEST CONDITIONS	
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
1 BV <sub>DSS</sub> Drain-Source Breakdown	40			60			80			V	V <sub>GS</sub> = 0, I <sub>D</sub> = 10μA	
2	40			60			80				V <sub>GS</sub> = 0, I <sub>D</sub> = 2.5mA	
3 V <sub>GS(th)</sub> Gate-Threshold Voltage	0.8	1.2		0.8	1.2		0.8	1.2			V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 1mA	
4 I <sub>GSS</sub> Gate-Body Leakage		0.01	10		0.01	10		0.01	10		V <sub>GS</sub> = 10V, V <sub>DS</sub> = 0	
5 7 8 <b>S T A T I C</b>	I <sub>DSS</sub> Zero Gate Voltage Drain Current		100		100		100		100	μA	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 0, T <sub>A</sub> = 125°C (Note 2)	
			10		10		10		10		V <sub>DS</sub> = Max. Rating, V <sub>GS</sub> = 0	
9 I <sub>D(on)</sub> ON-State Drain Current	1.0	2		1.0	2		1.0	2		nA	V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0	
10 11 12 13 <b>D Y N A M I C</b>	V <sub>DS(on)</sub> Drain-Source Saturation Voltage		0.3		0.3		0.4			A	V <sub>DS</sub> = 25V, V <sub>GS</sub> = 10V	
			1.0	2.0		1.0	1.7		1.4	1.9	V	V <sub>GS</sub> = 5V, I <sub>D</sub> = 0.1A
			1.0			1.0			1.3			V <sub>GS</sub> = 5V, I <sub>D</sub> = 0.3A
			2.2	5.0		2.2	3.5		2.2	4.5		V <sub>GS</sub> = 10V, I <sub>D</sub> = 0.5A
14 g <sub>m</sub> Forward Transconductance		250		250		250			mT	V <sub>DS</sub> = 24V, I <sub>D</sub> = 0.5A, f = 1KHz		
15 C <sub>iss</sub> Input Capacitance			50			50			50	pF	V <sub>GS</sub> = 0, V <sub>DS</sub> = 25V, f = 1.0 MHz	
16 C <sub>rss</sub> Reverse Transfer Capacitance			10			10			10			
17 C <sub>oss</sub> Common-Source Output Capacitance			50			50			50			
18 t <sub>d(on)</sub> Turn-ON Delay Time		2	5		2	5		2	5	ns	(Note 2)	
19 t <sub>r</sub> Rise Time		2	5		2	5		2	5			
20 t <sub>d(off)</sub> Turn-OFF Delay Time		2	5		2	5		2	5			
21 t <sub>f</sub> Fall Time		2	5		2	5		2	5			

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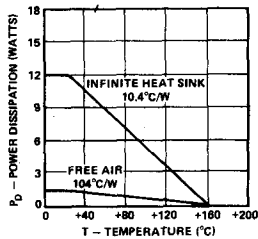
Note 1. Pulse test — 80μs pulse, 1% duty cycle.

Note 2. Sample test.

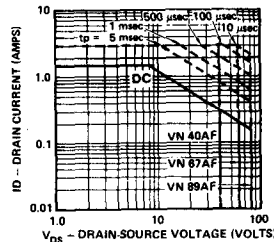
**THERMAL RESPONSE**



**POWER DISSIPATION vs CASE TEMPERATURE**



**DC SAFE OPERATING REGION T<sub>C</sub> = 25°C**



**BREAKDOWN VOLTAGE VARIATION WITH TEMPERATURE**

