Am29116A/Am29L116A/Am29116

High-Performance 16-Bit Bipolar Microprocessors

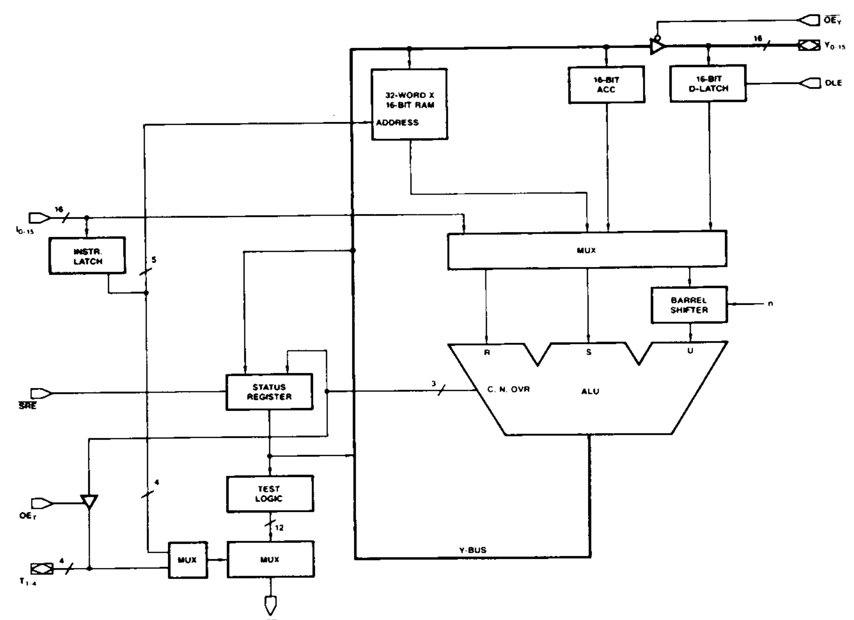
DISTINCTIVE CHARACTERISTICS

- **Optimized for High-Performance Controllers**
  Excellent solution for applications requiring speed and bit-manipulation power.
- **Fast**
  The Am29116 supports 100-ns microcycle time/10-MHz data rate for all instructions.
- **Speed-Enhanced Version**
  The Am29116A is 25% faster than the Am29116.
- **Low-Power Version**
  The Am29L116A is the same speed as the Am29116 and dissipates 25% less power.
- **Powerful Field Insertion/Extraction and Bit-Manipulation Instructions**
  Rotate and Merge, Rotate and Compare and bit-manipulation instructions provided for complex bit control.
- **Immediate Instruction Capability**
  May be used for storing constants in microcode or for configuring a second data port.
- **16-Bit Barrel Shifter**
- **32-Working Registers**

GENERAL DESCRIPTION

The Am29116 is a microprogrammable 16-bit bipolar microprocessor whose architecture and instruction set is optimized for high-performance peripheral controllers, like graphics controllers, disk controllers, communications controllers, front-end concentrators and modems. The device also performs well in microprogrammed processor applications, especially when combined with the Am29517, 16 x 16 Multiplier (65-ns worst-case 16 x 16 multiply). In addition to its complete arithmetic and logic instruction set, the Am29116 instruction set contains functions particularly useful in controller applications; bit set, bit reset, bit test, rotate and merge, rotate and compare, and cyclic-redundancy-check (CRC) generation.

BLOCK DIAGRAM



BD001962

Publication # 02112 Rev. E Amendment /0
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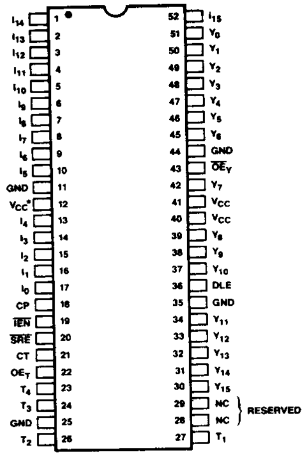
RELATED PRODUCTS

Part No.	Description
Am29112	High-Performance 8-Bit Slice Microprogram Sequencer
Am29C116	CMOS Version of the Am29116
Am29117	Two-Port Version of the Am29116
Am29C117	CMOS Version of the Am29117
Am29118	Eight-Bit Am29116 I/O Support

CONNECTION DIAGRAMS
Top View



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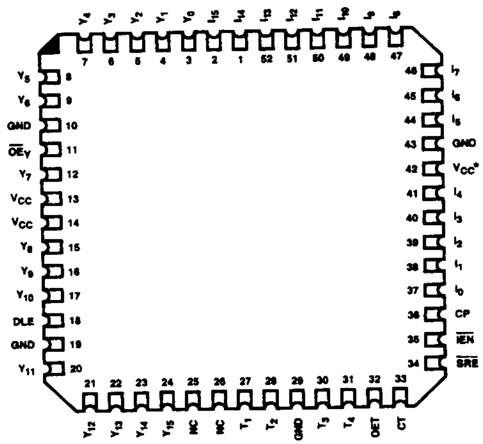
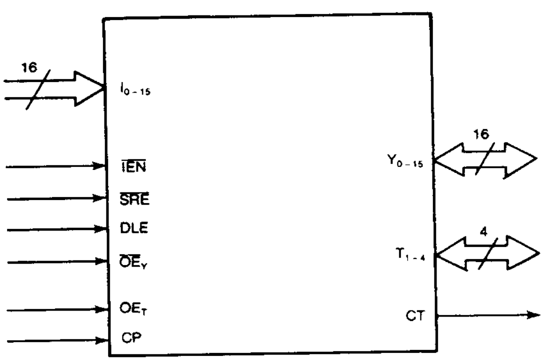


CD004183

Note: Pin 1 is marked for orientation.

*On the current bipolar devices, pin 12 is not connected (NC) internally. Historically, this pin was connected. CMOS options of the Am29116 currently use this pin for an internal V_{CC} connection.

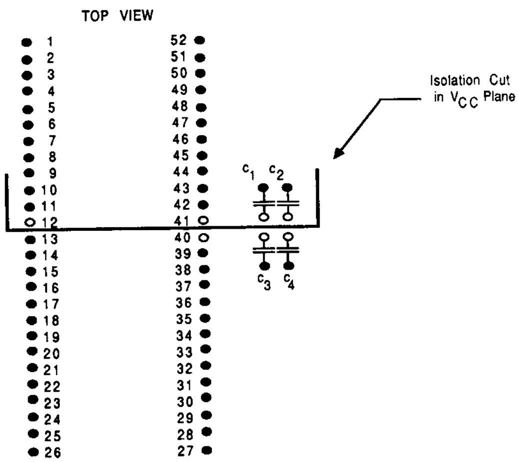
LOGIC SYMBOL



LS002252

GND = Ground
V_{CC} = Power Supply

V_{CC} AND GROUND PIN CONNECTIONS



● = Through Hole
○ = V_{CC} Plane Connection
$C_1 = C_3 = 0.1\ \mu F$
$C_2 = C_4 = 10\ \mu F$

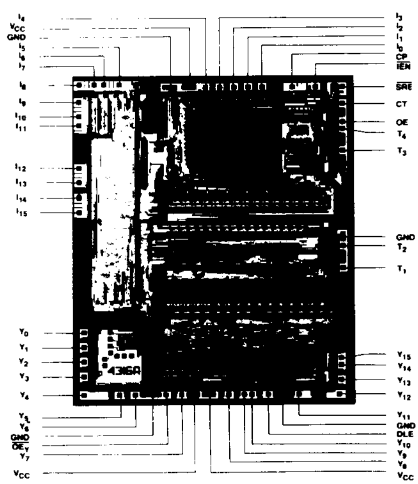
CD010201

The Am29116 Family of microprocessors consists of high-performance devices that operate in an environment of fast signal rise times and substantial switching currents. Attention must be paid to layout and decoupling to avoid undesired effects from this environment. The following suggestions may be of benefit in developing the layout scheme:

1. A multi-layer PC board with separate power, ground, and signal planes required for Schottky performance-level systems.
2. Tie the four ground pins immediately to the ground plane.
3. A U-shaped isolation cut should be made in the V_{CC} plane between pins 12 and 13 and pins 40 and 41. This isolation cut establishes a low-pass network that will provide sufficient inductive isolation between pin 40 (which supplies the TTL output drivers) and pin 41 (which supplies the internal ECL) so that transient currents will have no effect on the internal operation.
4. Pin 40 must be tied directly to the V_{CC} plane and decoupled with a bulk capacitor (10 μF) and a high-frequency capacitor (0.1 μF ceramic).
5. Pin 41 must be tied directly to the V_{CC} plane and decoupled with 0.1 μF and 10 μF capacitors.
6. The decoupling capacitors must be placed physically as close as possible to pin 40 and pin 41 respectively.

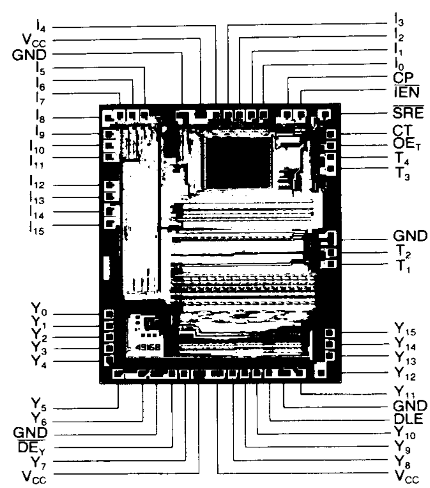
METALLIZATION AND PAD LAYOUTS

Am29116



Die Size: 0.251″ x 0.311″
Gate Count: 2500 Equivalent Gates

Am29116A/Am29L116A



Die Size: 0.205″ x 0.250″
Gate Count: 2500 Equivalent Gates

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing

AM29116A D C B

E. OPTIONAL PROCESSING
B = Burn-in

D. TEMPERATURE RANGE
C = Commercial (0 to +70°C)

C. PACKAGE TYPE
D = 52-Pin Topbrazed Ceramic DIP
TD 052 = DIP with Heat Sink
TDX052 = DIP without Heat Sink (Note 1)
L = 52-Pin Ceramic Leadless Chip Carrier (CLT052)
X = Dice

B. SPEED OPTION
Not Applicable

A. DEVICE NUMBER/DESCRIPTION
Am29116
High-Performance 16-Bit MPU
Am29116A
High-Speed, High-Performance 16-Bit MPU
Am29L116A
Low-Power, High-Performance 16-Bit MPU

Valid Combinations	
AM29116, AM29116A	DC, DCB, LC, XC
AM29L116A (Note 1)	

Notes: 1. 52-pin DIP without heat sink (TDX052) is available only for the Am29L116A Low-Power, High-Performance MPU.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL and CPL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) is formed by a combination of:

APL Products:
A. Device Number
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish

CPL Products:
A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temparature Range
E. CPL Status

APL Products

AM29116 /B U A

E. LEAD FINISH
A = Hot Solder DIP

D. PACKAGE TYPE
U = 52-Pin Ceramic Leadless Chip Carrier (CLT052)

C. DEVICE CLASS
/B = Class B

B. SPEED OPTION
Not Applicable

A. DEVICE NUMBER/DESCRIPTION
Am29116
High-Performance 16-Bit MPU

CPL Products

AM29116 /D M C

E. CPL STATUS
C = CPL Certified

D. TEMPERATURE RANGE
M = Military (–55 to +125°C)

C. PACKAGE TYPE
/D = 52-Pin Topbrazed Ceramic DIP (TD 052)

B. SPEED OPTION
Not Applicable

A. DEVICE NUMBER/DESCRIPTION
Am29116
High-Performance 16-Bit MPU

	Valid Combinations	
APL	AM29116	/BUA
CPL	AM29116	/DMC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A Tests consists of Subgroups:
1, 2, 3, 7, 8, 9, 10, 11

PIN DESCRIPTION

$Y_0 - Y_{15}$ Data I/O Lines — 16 (Input/Output)
When $\overline{OE}_Y$ is HIGH, Y_0-Y_{15} are used as external data inputs which allow data to be directly loaded into the 16-bit data latch. Having $\overline{OE}_Y$ LOW allows the ALU data to be output on Y_0-Y_{15}.

DLE Data Latch Enable (Input)
When DLE is HIGH, the 16-bit data latch is transparent and is latched when DLE is LOW.

$\overline{OE}_Y$ Output Enable (Input)
When $\overline{OE}_Y$ is HIGH, the 16-bit Y outputs are disabled (high-impedance); when $\overline{OE}_Y$ is LOW, the 16-bit Y outputs are enabled (HIGH or LOW).

$I_0 - I_{15}$ Instruction Inputs — 16 (Input)
Used to select the operations to be performed in the Am29116. Also used as data inputs while performing immediate instructions.

$\overline{IEN}$ Instruction Enable (Input)
With $\overline{IEN}$ LOW, data can be written into the RAM when the clock is LOW. The Accumulator can accept data during the LOW-HIGH transition of the clock. Having $\overline{IEN}$ LOW, the Status Register can be updated when $\overline{SRE}$ is LOW. With $\overline{IEN}$ HIGH, the conditional test output, CT, is disabled as a function of the instruction inputs. $\overline{IEN}$ should be LOW for the first half of the first cycle of an immediate instruction.

$\overline{SRE}$ Status Register Enable (Input)
When $\overline{SRE}$ and $\overline{IEN}$ are both LOW, the Status Register is updated at the end of all instructions with the exception of NO-OP, Save Status, and Test Status. Having either $\overline{SRE}$ or $\overline{IEN}$ HIGH will inhibit the Status Register from changing.

CP Clock Pulse (Input)
The clock input to the Am29116. The RAM latch is transparent when the clock is HIGH. When the clock goes LOW, the RAM output is latched. Data is written into the RAM during the low period of the clock provided $\overline{IEN}$ is LOW and if the instruction being executed designates the RAM as the destination of operation. The Accumulator and Status Register will accept data on the LOW-HIGH transition of the clock if $\overline{IEN}$ is also LOW. The instruction latch becomes transparent when it exits an immediate instruction mode during a LOW-HIGH transition of the clock.

$T_1 - T_4$ Input/Output Pins — 4 (Input/Output)
Under the control of OE_T, the four lower status bits Z, C, N, OVR become outputs on T_1-T_4, respectively when OE_T goes HIGH. When OE_T is LOW, T_1- T_4 are used as inputs to generate the CT output.

OE_T Output Enable (Input)
When OE_T is LOW, the 4-bit T outputs are disabled (high-impedance); when OE_T is HIGH, the 4-bit T outputs are enabled (HIGH or LOW).

CT Conditional Test (Output)
The condition code multiplexer selects one of the twelve condition code signals and places them on the CT output. A HIGH on the CT output indicates a passed condition and a LOW indicates a failed condition.

FUNCTIONAL DESCRIPTION

The following diagram (Figure 1) is a summary of devices within the Am29116 Family showing performance versus power.

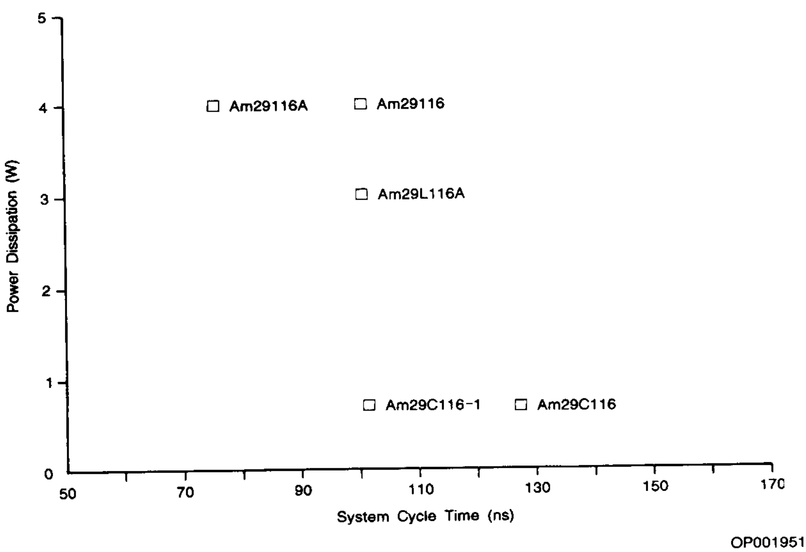
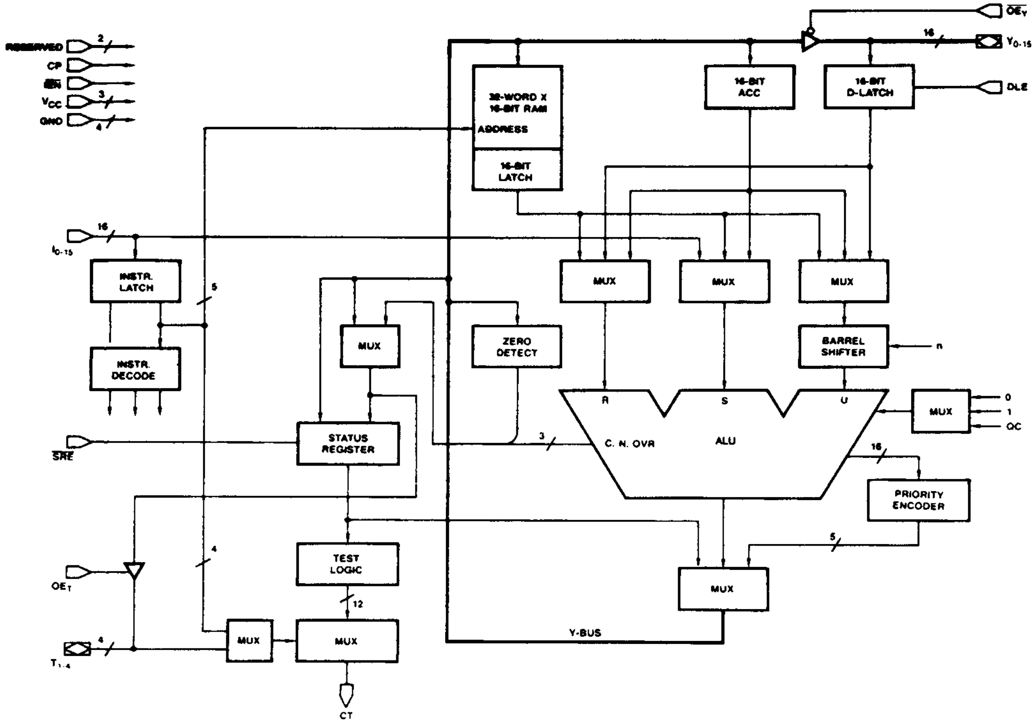


Figure 1. Am29116 Family (Performance Versus Power)



BD006540

Figure 2. Detailed Am29116 Block Diagram

ARCHITECTURE OF THE Am29116

The Am29116 is a high-performance, microprogrammable 16-bit bipolar microprocessor.

As shown in the Block Diagram, the device consists of the following elements interconnected with 16-bit data paths.

- 32-Word by 16-Bit RAM
- Accumulator
- Data Latch
- Barrel Shifter
- ALU
- Priority Encoder
- Status Register
- Condition-Code Generator/Multiplexer
- Three-State Output Buffers
- Instruction Latch and Decoder

32-Word by 16-Bit RAM

The 32-Word by 16-Bit RAM is a single-port RAM with a 16-bit latch at its output. The latches are transparent when the clock input (CP) is HIGH and latched when the clock input is LOW. Data is written into the RAM while the clock is LOW if the $\overline{\text{IEN}}$ input is also LOW and if the instruction being executed defines the RAM as the destination of the operation. For byte instructions, only the lower eight RAM bits are written into; for word instructions, all 16 bits are written into. With the use of an external multiplexer on five of the instruction inputs, it is possible to select separate read and write addresses for the same instruction. This two-address operation is not allowed for immediate instructions.

Accumulator

The 16-bit Accumulator is an edge-triggered register. The Accumulator accepts data on the LOW-to-HIGH transition of the clock input if the $\overline{\text{IEN}}$ input is LOW and if the instruction being executed defines the Accumulator as the destination of the operation. For byte instructions, only the lower eight bits of the Accumulator are written into; for word instructions, all 16 bits are written into.

Data Latch

The 16-bit Data Latch holds the data input to the Am29116 on the bi-directional Y bus. The latch is transparent when the DLE input is HIGH and latched when the DLE input is LOW.

Barrel Shifter

A 16-bit Barrel Shifter is used as one of the ALU inputs. This permits rotating data from either the RAM, the Accumulator or the Data Latch up to 15 positions. In the word mode, the Barrel Shifter rotates a 16-bit word; in the byte mode, it rotates only the lower eight bits.

Arithmetic Logic Unit

The Am29116 contains a 16-bit ALU with full carry lookahead across all 16 bits in the arithmetic mode. The ALU is capable of operating on either one, two or three operands, depending upon the instruction being executed. It has the ability to execute all conventional one and two operand operations, such as pass, complement, two's complement, add, subtract, AND, NAND, OR, NOR, EXOR, and EX-NOR. In addition, the ALU can also execute three-operand instructions such as rotate and merge, and rotate and compare with mask. All ALU operations can be performed on either a word or byte basis, byte operations being performed on the lower eight bits only.

The ALU produces three status outputs, C (carry), N (negative) and OVR (overflow). The appropriate flags are generated at the byte or word level, depending upon whether the device is executing in the byte or word mode. The Z (zero) flag, although not generated by the ALU, detects zero at both the byte and word level.

The carry input to the ALU is generated by the Carry Multiplexer which can select an input of zero, one, or the stored carry bit from the Status Register, QC. Using QC as the carry input allows execution of multiprecision addition and subtractions.

Priority Encoder

The Priority Encoder produces a binary-weighted code to indicate the locations of the highest order ONE at its input. The input to the Priority Encoder is generated by the ALU which performs an AND operation on the operand to be prioritized and a mask. The mask determines which bit locations to eliminate from prioritization. In the word mode, if no bit is HIGH, the output is a binary zero. If bit 15 is HIGH, the output is a binary one. Bit 14 produces a binary two, etc. Finally, if only bit 0 is HIGH, a binary 16 is produced.

In the byte mode, bits 8 thru 15 do not participate. If none of bits 7 thru 0 are HIGH, the output is a binary zero. If bit 7 is HIGH a binary one is produced. Bit 6 produces a binary two, etc. Finally, if only bit 0 is HIGH, a binary 8 is produced.

Status Register

The Status Register holds the 8-bit status word. With the Status-Register Enable, ($\overline{\text{SRE}}$) input LOW and the $\overline{\text{IEN}}$ input LOW, the Status Register is updated at the end of all instructions except NO-OP, Save-Status and Test-Status instructions. $\overline{\text{SRE}}$ going HIGH or $\overline{\text{IEN}}$ going HIGH inhibits the Status Register from changing.

The lower four bits of the Status Register contain the ALU status bits of Zero (Z), Carry, (C) Negative (N), and Overflow (OVR). The upper four bits contain a Link bit and three user-definable status bits (Flag 1, Flag 2, Flag 3).

With $\overline{\text{SRE}}$ LOW and $\overline{\text{IEN}}$ LOW, the lower four status bits are updated after each instruction except those mentioned above, NO-OP, Save Status, Status Test and the Status Set/Reset instruction for the upper four bits. Under the same conditions, the upper four status bits are changed only during their respective Status Set/Reset instructions and during Status Load instructions in the word mode. The Link-Status bit is also updated after each shift instruction.

The Status Register can be loaded from the internal Y-bus, and can also be selected as a source for the internal Y-bus. When the Status Register is loaded in the word mode, all 8-bits are updated; in the byte mode, only the lower 4 bits (Z, C, N, OVR) are updated.

When the Status Register is selected as a source in the word mode, all eight bits are loaded into the lower byte of the destination; the upper byte of the destination is loaded with all zeros. In the byte mode, the Status Register again loads into the lower byte of the destination, but the upper byte remains unchanged. This Store and Load combination allows saving the restoring the Status Register for interrupt and subroutine processing. The four lower status bits (Z, C, N, OVR) can be read directly via the bidirectional T bus. These four bits are available as outputs on the T_{1-4} outputs whenever OE_T is HIGH.

Condition-Code Generator/Multiplexer

The Condition-Code Generator/Multiplexer contains the logic necessary to develop the 12 condition-code test signals. The multiplexer portion can select one of these test signals and place it on the CT output for use by the microprogram sequence. The multiplexer may be addressed in two different ways. One way is through the Test Instruction. This instruction specifies the test condition to be placed in the CT output, but does not allow an ALU operation at the same time. The second method uses the bidirectional T bus as an input. This requires extra bits in the microword, but provides the ability to simultaneously test and execute. The test instruction lines, I_{0-4}, have priority over T_{1-4}, for testing status.

Three-State Output Buffers

There are two sets of Three-State Output Buffers in the Am29116. One set controls the bidirectional, 16-bit Y bus. These outputs are enabled by placing a LOW on the $\overline{OE}$ input. A HIGH puts the Y outputs in the high-impedance state, allowing data to be input to the Data latch from an external source.

The second set of Three-State Output Buffers controls the bidirectional 4-bit T bus and is enabled by placing a HIGH on the OE_T input. This allows storing the four internal ALU status bits (Z, C, N, OVR) externally. A LOW OE_T input forces the T outputs into the high-impedance state. External devices can then drive the T bus to select a test condition for the CT output.

Instruction Latch and Decoder

The 16-bit Instruction Latch is normally transparent to allow decoding of the Instruction Inputs by the Instruction Decoder into the internal control signals for the Am29116. All instructions except Immediate Instructions are executed in a single clock cycle.

Immediate instructions require two clock cycles for execution. During the first clock cycle, the Instruction Decoder recognizes that an Immediate Instruction is being specified and captures the data on the Instruction Inputs in the Instruction Latch. During the second clock cycle, the data on the Instruction Inputs is used as one of the operands for the function specified during the first clock cycle. At the end of the second clock cycle, the Instruction Latch is returned to its transparent state.

INSTRUCTION SET

The instruction set of the Am29116 is very powerful. In addition to the single and two operand logical and arithmetic instructions, the Am29116 instruction set contains functions particularly useful in controller applications: bit set, bit reset, bit test, rotate and merge, rotate and compare, and cyclic-redundancy-check (CRC) generation. Complex instructions like rotate and merge, rotate and compare, and prioritize are executed in a single microcycle.

Three data types are supported by the Am29116.

- Bit
- Byte
- Word (16-bit)

In the byte mode data is written into the lower half of the word and the upper half is unchanged. The special case is when the status register is specified as the destination. In the byte mode the LSH (OVR, N, C, Z) of the status register is updated and in the word mode all eight bits of the status register are updated. The status register does not change for save status and test status instructions. In the test status instructions the CT output has the result and the Y-bus is undefined.

The Am29116 Instruction Set can be divided into eleven types of instructions. These are:

- Single Operand
- Two Operand
- Single Bit Shift
- Rotate and Merge
- Bit Oriented
- Rotate by n Bits
- Rotate and Compare
- Prioritize
- Cyclic-Redundancy-Check
- Status
- No-Op

Each instruction type is arbitrarily divided into quadrants. Two of the sixteen instruction lines decode to four quadrants labelled from 0 to 3. The quadrants were defined mainly for convenience in classification of the instruction set and addressing modes and can be used together with the OP CODES to distinguish the instructions.

The following pages describe each of the instruction types in detail. Throughout the description $\overline{OE_Y}$ is assumed to be LOW allowing ALU outputs on the Y-bus.

Table 1 illustrates operand source-destination combinations for each instruction type.

TABLE 1. OPERAND SOURCE DESTINATION COMBINATIONS

Instruction Type	Operand Combinations (Note 1)		
Single Operand	Source (R/S)		Destination
	RAM (Note 2) ACC D D(0E) D(SE) I 0		RAM ACC Y Bus Status ACC and Status
Two Operand	Source (R)	Source (S)	Destination
	RAM RAM D D ACC D	ACC I RAM ACC I I	RAM ACC Y Bus Status ACC and Status
Single Bit Shift	Source (U)		Destination
	RAM ACC ACC D D D		RAM ACC Y Bus RAM ACC Y Bus
Rotate n Bits	Source (U)		Destination
	RAM ACC D		RAM ACC Y Bus
Bit Oriented	Source (R/S)		Destination
	RAM ACC D		RAM ACC Y Bus
Rotate and Merge	Rotated Source (U)	Mask (S)	Non-Rotated Source/ Destination (R)
	D D D D ACC RAM	I RAM I ACC I I	ACC ACC RAM RAM RAM ACC

Instruction Type	Operand Combinations (Note 1)		
Rotate and Compare	Rotated Source (U)	Mask (S)	Non-Rotated Source/ Destination (R)
	D	I	
	D	I	RAM
	D	ACC	RAM
	RAM	I	ACC
Prioritize (Note 3)	Source (R)	Mask (S)	Destination
	RAM ACC D	RAM ACC I 0	RAM ACC Y Bus
Cyclic Redundancy Check	Data In	Destination	Polynomial
	QLINK	RAM	ACC
No Operation	–		
Set Reset Status	Bits Affected		
	OVR, N, C, Z LINK Flag1 Flag2 Flag3		
Store Status	Source		Destination
	Status		RAM ACC Y Bus
Status Load	Source (R)	Source (S)	Destination
	D ACC D	ACC I I	Status Status and ACC
Test Status	Test Condition (CT)		
	$(N \oplus OVR) + Z$ $N \oplus OVR$ Z OVR Low C $Z + \overline{C}$ N LINK Flag 1 Flag 2 Flag 3		

Notes: 1. When there is no dividing line between the R&S OPERAND or SOURCE and DESTINATION, the two must be used as a given pair. But where there exists such a separation, any combination of them is possible.
2. In the SINGLE OPERAND INSTRUCTION, RAM cannot be used when both ACC and STATUS are designated as a DESTINATION.
3. In the PRIORITIZE INSTRUCTION, OPERAND and MASK must be different sources.

SINGLE OPERAND INSTRUCTIONS

The Single Operand Instructions contain four indicators: byte or word mode, opcode, source and destination. They are further subdivided into two types. The first type uses RAM as a source or destination or both, and the second type does not use RAM as a source or destination. Both types have different instruction formats as shown below. Under the control of instruction inputs, the desired function is performed on the source and the result is either stored in the specified destination or placed on the Y-bus or both. For a special case where 8-bit to 16-bit conversion is needed, the Am29116 is capable of extending sign bit (D(SE)) or binary zero (D(0E)) over 16-bits in the word mode. The least significant four bits of the Status Register (OVR, N, C, Z) are affected by the function performed in this category. The most significant bits of status register (FLAG1, FLAG2, FLAG3, LINK) are not affected. The only limitation in this type is that the RAM cannot be used as a source when both ACC and the Status Register are specified as a destination.

SINGLE OPERAND FIELD DEFINITIONS

	15 14	13 12	9 8	5 4	0
SOR	B/W	Quad	Opcode	SRC-Dest	RAM Address
SONR	B/W	Quad	Opcode	SRC	Dest

SINGLE OPERAND INSTRUCTION

	15	14 13	12 9	8 5	4 0
Instruction[1]	**B/W[2]**	**Quad[3]**	**Opcode**	**R/S[4] Dest[4]**	**RAM Address**
SOR	0 = B 1 = W	10	1100 MOVE SRC → Dest 1101 COMP $\overline{SRC}$ → Dest 1110 INC SRC + 1 → Dest 1111 NEG $\overline{SRC}$ + 1 → Dest	0000 SORA RAM ACC 0010 SORY RAM Y Bus 0011 SORS RAM Status 0100 SOAR ACC RAM 0110 SODR D RAM 0111 SOIR I RAM 1000 SOZR 0 RAM 1001 SOZER D(0E) RAM 1010 SOSER D(SE) RAM 1011 SORR RAM RAM	00000 R00 RAM Reg 00 .. .. 11111 R31 RAM Reg 31
Instruction	**B/W**	**Quad**	**Opcode**	**R/S[4]**	**Destination**
SONR	0 = B 1 = W	11	1100 MOVE SRC → Dest 1101 COMP $\overline{SRC}$ → Dest 1110 INC SRC + 1 → Dest 1111 NEG $\overline{SRC}$ + 1 → Dest	0100 SOA ACC 0110 SOD D 0111 SOI I 1000 SOZ 0 1001 SOZE D(0E) 1010 SOSE D(SE)	00000 NRY Y Bus 00001 NRA ACC 00100 NRS Status[5] 00101 NRAS ACC, Status[5]

Notes:
1. The instruction mnemonic designates different instruction formats used in the Am29116. They are useful in assembly microcode with the System 29 AMDASM™ meta assembler.
2. B = Byte Mode, W = Word Mode.
3. See Instruction Set description.
4. R = Source; S = Source; Dest = Destination.
5. When status is destination, Status i ← Yi i = 0 to 3 (Byte mode) i = 0 to 7 (Word mode)

Y BUS AND STATUS – SINGLE OPERAND INSTRUCTIONS

Instruction	Opcode	Description	B/W	Y — Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
SOR	MOVE	SRC → Dest	0 = B	Y ← SRC	NC	NC	NC	NC	0	U	0	U
SONR	COMP	$\overline{SRC}$ → Dest	1 = W	Y ← $\overline{SRC}$	NC	NC	NC	NC	0	U	0	U
	INC	SRC +1 → Dest		Y ← SRC +1	NC	NC	NC	NC	U	U	U	U
	NEG	$\overline{SRC}$ +1 → Dest		Y ← $\overline{SRC}$ +1	NC	NC	NC	NC	U	U	U	U

SRC = Source
U = Update
NC = No Change

0 = Reset
1 = Set
i = 0 to 15 when not specified

TWO OPERAND INSTRUCTIONS

The Two Operand Instructions contain five indicators: byte or word mode, opcode, R source, S source, and destination. They are further subdivided into two types. The first type uses RAM as the source and/or destination and the second type does not use RAM as source or destination. The first type has two formats; the only difference is in the quadrant. Under the control of instruction inputs, the desired function is performed on the specified sources and the result is stored in the specified destination or placed on the Y-bus or both. The least significant four bits of the status register (OVR, N, C, Z) are affected by the arithmetic functions performed and only the N and Z bits are affected by the logical functions performed. The OVR and C bits of the status register are forced to ZERO for logical functions. Add with carry and Subtract with carry instructions are useful for Multiprecision Add or Subtract.

TWO OPERAND FIELD DEFINITIONS

	15	14 13	12 9	8 5	4 0
TOR1	B/W	Quad	SRC-SRC -Dest	Opcode	RAM Address
TOR2	B/W	Quad	SRC-SRC -Dest	Opcode	RAM Address
TONR	B/W	Quad	SRC-SRC	Opcode	Dest

TWO OPERAND INSTRUCTIONS

Instruction	B/W	Quad			R[1]	S[1]	Dest[1]	Opcode			RAM Address		
TOR1	0 = B 1 = W	00	0000	TORAA	RAM	ACC	ACC	0000	SUBR	S minus R	00000	R00	RAM Reg 00
			0010	TORIA	RAM	I	ACC	0001	SUBRC[2]	S minus R with carry	. .	. .	. . . .
			0011	TODRA	D	RAM	ACC	0010	SUBS	R minus S	11111	R31	RAM Reg 31
			1000	TORAY	RAM	ACC	Y Bus	0011	SUBSC[2]	R minus S with carry			
			1010	TORIY	RAM	I	Y Bus	0100	ADD	R plus S			
			1011	TODRY	D	RAM	Y Bus	0101	ADDC	R plus S with carry			
			1100	TORAR	RAM	ACC	RAM	0110	AND	$R \cdot S$			
			1110	TORIR	RAM	I	RAM	0111	NAND	$\overline{R \cdot S}$			
			1111	TODRR	D	RAM	RAM	1000	EXOR	$R \oplus S$			
								1001	NOR	$\overline{R + S}$			
								1010	OR	$R + S$			
								1011	EXNOR	$\overline{R \oplus S}$			

Instruction	B/W	Quad			R[1]	S[1]	Dest[1]	Opcode			RAM Address		
TOR2	0 = B 1 = W	10	0001	TODAR	D	ACC	RAM	0000	SUBR	S minus R	00000	R00	RAM Reg 00
			0010	TOAIR	ACC	I	RAM	0001	SUBRC[2]	S minus R with carry	. .	. .	. . . .
			0101	TODIR	D	I	RAM	0010	SUBS	R minus S	11111	R31	RAM Reg 31
								0011	SUBSC[2]	R minus S with carry			
								0100	ADD	R plus S			
								0101	ADDC	R plus S with carry			
								0110	AND	$R \cdot S$			
								0111	NAND	$\overline{R \cdot S}$			
								1000	EXOR	$R \oplus S$			
								1001	NOR	$\overline{R + S}$			
								1010	OR	$R + S$			
								1011	EXNOR	$\overline{R \oplus S}$			

Note 1: R = Source
S = Source
Dest = Destination
Note 2: During subtraction the carry is interpreted as $\overline{\text{borrow}}$.

TWO OPERAND INSTRUCTIONS

Instruction	B/W	Quad	R[1] S[1]	Opcode	Destination
TONR	0 = B 1 = W	11	0001 TODA D ACC 0010 TOAI ACC I 0101 TODI D I	0000 SUBR S minus R 0001 SUBRC S minus R with carry 0010 SUBS R minus S 0011 SUBSC R minus S with carry 0100 ADD R plus S 0101 ADDC R plus S with carry 0110 AND $R \cdot S$ 0111 NAND $\overline{R \cdot S}$ 1000 EXOR $R \oplus S$ 1001 NOR $\overline{R + S}$ 1010 OR $R + S$ 1011 EXNOR $\overline{R \oplus S}$	00000 NRY Y Bus 00001 NRA ACC 00100 NRS Status[2] 00101 NRAS ACC, Status[2]

Notes 1: R = Source
S = Source
2: When status is destination,
Status $i \leftarrow Y_i$ $i = 0$ to 3 (Byte mode)
$i = 0$ to 7 (Word mode)
3: During subtraction the carry is interpreted as $\overline{\text{borrow}}$.
4: $OVR = C_8 \oplus C_7$ (Byte mode)
$OVR = C_{16} \oplus C_{15}$ (Word mode)

Y BUS AND STATUS CONTENTS – TWO OPERAND INSTRUCTIONS

Instruction	Opcode	Description	B/W	Y – Bus	Flag3	Flag2	Flag 1	LINK	OVR	N	C	Z
TOR1 TOR2 TONR	SUBR	S minus R	0 = B	$Y \leftarrow S + \overline{R} + 1$	NC	NC	NC	NC	U	U	U	U
	SUBRC	S minus R with carry	1 = w	$Y \leftarrow S + \overline{R} + QC$	NC	NC	NC	NC	U	U	U	U
	SUBS	R minus S		$Y \leftarrow R + \overline{S} + 1$	NC	NC	NC	NC	U	U	U	U
	SUBSC	R minus S with carry		$Y \leftarrow R + \overline{S} + QC$	NC	NC	NC	NC	U	U	U	U
	ADD	R plus S		$Y \leftarrow R + S$	NC	NC	NC	NC	U	U	U	U
	ADDC	R plus S with carry		$Y \leftarrow R + S + QC$	NC	NC	NC	NC	U	U	U	U
	AND	$R \cdot S$		$Y \leftarrow R_i$ AND S_i	NC	NC	NC	NC	0	U	0	U
	NAND	$\overline{R \cdot S}$		$Y_i \leftarrow R_i$ NAND S_i	NC	NC	NC	NC	0	U	0	U
	EXOR	$R \oplus S$		$Y_i \leftarrow R_i$ EXOR S_i	NC	NC	NC	NC	0	U	0	U
	NOR	$\overline{R + S}$		$Y_i \leftarrow R_i$ NOR S_i	NC	NC	NC	NC	0	U	0	U
	OR	$R + S$		$Y_i \leftarrow R_i$ OR S_i	NC	NC	NC	NC	0	U	0	U
	EXNOR	$\overline{R \oplus S}$		$Y_i \leftarrow R_i$ EXNOR S_i	NC	NC	NC	NC	0	0	0	U

U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

SINGLE BIT SHIFT INSTRUCTIONS

The Single Bit Shift Instructions contain four indicators: byte or word mode, direction and shift linkage, source and destination. They are further subdivided into two types. The first type uses RAM as the source and/or destination and the second type does not use RAM as source or destination. Under the control of the instruction inputs, the desired shift function is performed on the specified source and the result is stored in the specified destination or placed on the Y-bus or both. The direction and shift linkage indicator defines the direction of the shift (up or down) as well as what will be shifted into the vacant bit. On a shift-up instruction, the LSB may be loaded with ZERO, ONE, or the Link-Status bit (QLINK). The MSB is loaded into the Link-Status bit as shown in Figure 3. On a shift-down instruction, the MSB may be loaded with ZERO, ONE, the contents of the Status Carry flip-flop, (QC), the Exclusive-OR of the Negative-Status bit and the Overflow-Status bit (QN ⊕ QOVR) or the Link-Status bit. The LSB is loaded into the Link-Status bit as shown in Figure 4. The N and Z bits of the Status register are affected but the OVR and C bits are forced to ZERO. The Shift-Down with QN ⊕ QOVR is useful for Two's Complement multiplication.

SINGLE BIT SHIFT FIELD DEFINITIONS:

	15	14 13	12 9	8 5	4 0
SHFTR	B/W	Quad	SRC-Dest	Opcode	RAM Address

SHFTNR	B/W	Quad	SRC	Opcode	Dest

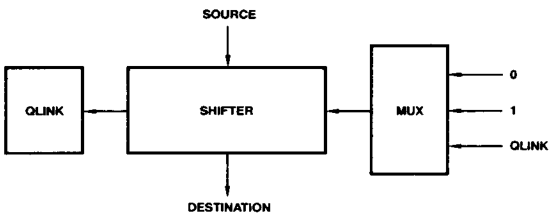


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Figure 3. Shift Up Function.

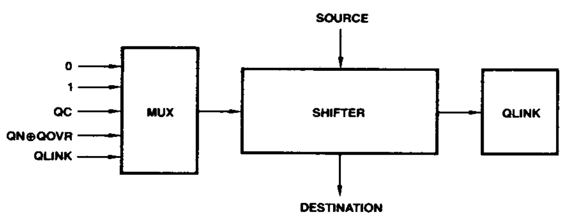

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Figure 4. Shift Down Function.

SINGLE BIT SHIFT INSTRUCTIONS

SINGLE BIT SHIFT

Instruction	B/W	Quad	U[1] Dest[1]	Opcode	RAM Address
SHFTR	0 = B 1 = W	10	0110 SHRR RAM RAM 0111 SHDR D RAM	0000 SHUPZ Up 0 0001 SHUP1 Up 1 0010 SHUPL Up QLINK 0100 SHDNZ Down 0 0101 SHDN1 Down 1 0110 SHDNL Down QLINK 0111 SHDNC Down QC 1000 SHDNOV Down QN⊕QOVR	00000 R00 RAM Reg 00 . . . . 11111 R31 RAM Reg 31

Instruction	B/W	Quad	U[1]	Opcode	Destination
SHFTNR	0 = B 1 = W	11	0110 SHA ACC 0111 SHD D	0000 SHUPZ Up 0 0001 SHUP1 Up 1 0010 SHUPL Up QLINK 0100 SHDNZ Down 0 0101 SHDN1 Down 1 0110 SHDNL Down QLINK 0111 SHDNC Down QC 1000 SHDNOV Down QN⊕QOVR	00000 NRY Y Bus 00001 NRA ACC

Note 1. U = Source
Dest = Destination

Y BUS AND STATUS – SINGLE BIT SHIFT INSTRUCTIONS

Instruction	Opcode	Description	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
SHR SHNR	SHUPZ SHUP1 SHUPL	Up 0 Up 1 Up QLINK	1 = W	$Y_i \leftarrow SRC_{i-1}$, $i = 1$ to 15; $Y_0 \leftarrow$ Shift Input	NC	NC	NC	SRC_{15}*	0	SRC_{14}	0	U
			0 = B	$Y_i \leftarrow SRC_{i-1}$, $i = 1$ to 7; $Y_0 \leftarrow$ Shift Input; $Y_8 \leftarrow SRC_7$, $Y_i \leftarrow SRC_{i-9}$ for $i = 9$ to 15	NC	NC	NC	SRC_7*	0	SRC_6	0	U
	SHDNZ SHDN1 SHDNL SHDNC SHCNOV	Down 0 Down 1 Down QLINK Down QC Down QN⊕QOVR	1 = W	$Y_i \leftarrow SRC_{i+1}$, $i = 0$ to 14; $Y_{15} \leftarrow$ Shift Input	NC	NC	NC	SRC_0*	0	Shift Input	0	U
			0 = B	$Y_i \leftarrow SRC_{i+1}$, $i = 0$ to 6; $Y_i \leftarrow SRC_{i-7}$, $i = 8$ to 14; $Y_{7,15} \leftarrow$ Shift Input	NC	NC	NC	SRC_0*	0	Shift Input	0	U

*Shifted Output is loaded into the QLINK.

SRC = Source
U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

BIT ORIENTED INSTRUCTIONS

The Bit Oriented Instructions contain four indicators: byte or word mode, operation, source/destination, and the bit position of the bit to be operated on (Bit 0 is the least significant bit). They are further subdivided into two types. The first type uses the RAM as both source and destination and has two kinds of formats which differ only by quadrant. The second type does not use the RAM as a source or a destination. Under the control of the instruction inputs, the desired function is performed on the specified source and the result is stored in the specified destination or placed on the Y-bus or both. The operations which can be performed are: Set Bit n which forces the n^{th} bit to a ONE leaving other bits unchanged; Reset Bit n which forces the n^{th} bit to ZERO leaving the other bits unchanged; Test Bit n, which sets the ZERO Status Bit depending on the state of bit n leaving all the bits unchanged; Load 2^n, which loads ONE in Bit position n and ZERO in all other bit positions; Load $\overline{2^n}$ which loads ZERO in bit position n and ONE in all other bit positions; increment by 2^n, which adds 2^n to the operand; and decrement by 2^n which subtracts 2^n from the operand. For all the Load, Set, Reset and Test instructions, the N and Z bits are affected and OVR and C bit of the Status register are forced to ZERO. For all arithmetic instructions the LSH (OVR, C, N, Z bits) of the Status register is affected.

BIT ORIENTED FIELD DEFINITIONS

	15 14	13 12	9 8	5	4 0
BOR1	B/W	Quad	n	Opcode	RAM Address
BOR2	B/W	Quad	n	Opcode	RAM Address
BONR	B/W	Quad	n	1100	Opcode

BIT ORIENTED INSTRUCTIONS

Instruction	B/W	Quad	n	Opcode	RAM Address
BOR1	0 = B 1 = W	11	0 to 15	1101 SETNR Set RAM, bit n 1110 RSTNR Reset RAM, bit n 1111 TSTNR Test RAM, bit n	00000 R00 RAM Reg 00 .. .. 11111 R31 RAM Reg 31
Instruction	**B/W**	**Quad**	**n**	**Opcode**	**RAM Address**
BOR2	0 = B 1 = W	10	0 to 15	1100 LD2NR $2^n \rightarrow$ RAM 1101 LDC2NR $\overline{2^n} \rightarrow$ RAM 1110 A2NR RAM plus $2^n \rightarrow$ RAM 1111 S2NR RAM minus $2^n \rightarrow$ RAM	00000 R00 RAM Reg 00 .. .. 11111 R31 RAM Reg 31
Instruction	**B/W**	**Quad**	**n**		**Opcode**
BONR	0 = B 1 = W	11	0 to 15	1100	00000 TSTNA Test ACC, bit n 00001 RSTNA Reset ACC, bit n 00010 SETNA Set ACC, bit n 00100 A2NA ACC plus $2^n \rightarrow$ ACC 00101 S2NA ACC minus $2^n \rightarrow$ ACC 00110 LD2NA $2^n \rightarrow$ ACC 00111 LDC2NA $\overline{2^n} \rightarrow$ ACC 10000 TSTND Test D, bit n 10001 RSTND Reset D, bit n 10010 SETND Set D, bit n 10100 A2NDY D plus $2^n \rightarrow$ Y BUS 10101 S2NDY D minus $2^n \rightarrow$ Y Bus 10110 LS2NY $2^n \rightarrow$ Y Bus 10111 LDC2NY $\overline{2^n} \rightarrow$ Y Bus

BIT ORIENTED INSTRUCTIONS

Y BUS AND STATUS – BIT ORIENTED INSTRUCTIONS

Instruction	Opcode	Description	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
BOR1	SETNR	Set RAM Bit n	0 = B 1 = W	$Y_i \leftarrow RAM_i$ for $i \neq n$; $Y_n \leftarrow 1$	NC	NC	NC	NC	0	U	0	0
	RSTNR	Reset RAM, Bit n		$Y_i \leftarrow RAM_i$ for $i \neq n$; $Y_n \leftarrow 0$	NC	NC	NC	NC	0	U	0	U
	TSTNR	Test Ram, Bit n		$Y_i \leftarrow 0$ for $i \neq n$; $Y_n \leftarrow SRC_n$	NC	NC	NC	NC	0	U	0	U
BOR2	LD2NR	$2^n \rightarrow RAM$		$Y_i \leftarrow 0$ for $i \neq n$; $Y_n \leftarrow 1$	NC	NC	NC	NC	0	U	0	0
	LDC2NR	$\overline{2^n} \rightarrow RAM$		$Y_i \leftarrow 1$ for $i \neq n$; $Y_n \leftarrow 0$	NC	NC	NC	NC	0	U	0	0
	A2NR	$RAM + 2^n \rightarrow RAM$		$Y_i \leftarrow RAM + 2^n$	NC	NC	NC	NC	U	U	U	U
	S2NR	$RAM - 2^n \rightarrow RAM$		$Y_i \leftarrow RAM - 2^n$	NC	NC	NC	NC	U	U	U	U
BONR	TSTNA	Test ACC, Bit n		$Y_i \leftarrow 0$ for $i \neq n$; $Y_n \leftarrow ACC_n$	NC	NC	NC	NC	0	U	0	U
	RSTNA	Reset ACC, Bit n		$Y_i \leftarrow ACC_i$ for $i \neq n$; $Y_n \leftarrow 0$	NC	NC	NC	NC	0	U	0	U
	SETNA	Set ACC, Bit n		$Y_i \leftarrow ACC_i$ for $i \neq n$; $Y_n \leftarrow 1$	NC	NC	NC	NC	0	U	0	0
	A2NA	$ACC + 2^n \rightarrow ACC$		$Y_i \leftarrow ACC + 2^n$	NC	NC	NC	NC	U	U	U	U
	S2NA	$ACC - 2^n \rightarrow ACC$		$Y_i \leftarrow ACC - 2^n$	NC	NC	NC	NC	U	U	U	U
	LD2NA	$2^n \rightarrow ACC$		$Y_i \leftarrow 0$ for $i \neq n$; $Y_n \leftarrow 1$	NC	NC	NC	NC	0	U	0	0
	LDC2NA	$\overline{2^n} \rightarrow ACC$		$Y_i \leftarrow 1$ for $i \neq n$; $Y_n \leftarrow 0$	NC	NC	NC	NC	0	U	0	0
	TSTND	Test D, Bit n		$Y_i \leftarrow 0$ for $i \neq n$; $Y_n \leftarrow D_n$	NC	NC	NC	NC	0	U	0	U
	RSTND	Reset D, Bit n*		$Y_i \leftarrow D_i$ for $i \neq n$; $Y_n \leftarrow 0$	NC	NC	NC	NC	0	U	0	U
	SETND	Set D, Bit n*		$Y_i \leftarrow D_i$ for $i \neq n$; $Y_n \leftarrow 1$	NC	NC	NC	NC	0	U	0	0
	A2NDY	$D + 2^n \rightarrow$ Y Bus		$Y \leftarrow D + 2^n$	NC	NC	NC	NC	U	U	U	U
	S2NDY	$D - 2^n \rightarrow$ Y Bus		$Y \leftarrow D - 2^n$	NC	NC	NC	NC	U	U	U	U
	LD2NY	$2^n \rightarrow$ Y Bus		$Y_i \leftarrow 0$ for $i \neq n$; $Y_n \leftarrow 1$	NC	NC	NC	NC	0	U	0	0
	LDC2NY	$\overline{2^n} \rightarrow$ Y Bus		$Y_i \leftarrow 1$ for $i \neq n$; $Y_n \leftarrow 0$	NC	NC	NC	NC	0	U	0	0

SRC = Source
U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

*Destination is not D Latch but Y Bus.

ROTATE BY n BITS INSTRUCTIONS

The Rotate by n Bits Instructions contain four indicators: byte or word mode, source, destination and the number of places the source is to be rotated. They are further subdivided into two types. The first type uses RAM as a source and/or a destination and the second type does not use RAM as a source or destination. The first type has two different formats and the only difference is in the quadrant. The second type has only one format as shown in the table. Under the control of instruction inputs, the n indicator specifies the number of bit positions the source is to be rotated up (0 to 15), and the result is either stored in the specified destination or placed on the Y-bus or both. An example of this instruction is given in Figure 5. In the Word mode, all 16-bits are rotated up while in the Byte mode, only the lower 8-bits (0-7) are rotated up; In the Word mode, a rotate up by n bits is equivalent to a rotate down by (16-n) bits. Similarly, in the Byte mode a rotate up by n bits is equivalent to a rotate down by (8-n) bits. The N and Z bits of the Status Register are affected and OVR and C bits are forced to ZERO.

EXAMPLE: n = 4, Word Mode

Source	0001	0011	0111	1111
Destination	0011	0111	1111	0001

EXAMPLE: n = 4, Byte Mode

Source	0001	0011	0111	1111
Destination	0001	0011	1111	0111

Figure 5. Rotate by n Example

ROTATE BY n BITS FIELD DEFINITIONS

	15 14	13 12	9 8	5 4	0
ROTR1	B/W	Quad	n	SRC-Dest	RAM Address
ROTR2	B/W	Quad	n	SRC-Dest	RAM Address
ROTNR	B/W	Quad	n	1100	SRC-Dest

ROTATE BY n BITS INSTRUCTIONS

Instruction	B/W	Quad	n			U[1]	Dest[1]	RAM Address		
ROTR1	0 = B 1 = W	00	0 to 15	1100 1110 1111	RTRA RTRY RTRR	RAM RAM RAM	ACC Y Bus RAM	00000 . . 11111	R00 . . R31	RAM Reg 00 . . . . RAM Reg 31

Instruction	B/W	Quad	n			U[1]	Dest[1]	RAM Address		
ROTR2	0 = B 1 = W	01	0 to 15	0000 0001	RTAR RTDR	ACC D	RAM RAM	00000 11111	R00 . . R31	RAM Reg 00 . . . . RAM Reg 31

Instruction	B/W	Quad	n				U[1]	Dest[1]
ROTNR	0 = B 1 = W	11	0 to 15	1100	11000 11001 11100 11101	RTDY RTDA RTAY RTAA	D D ACC ACC	Y Bus ACC Y Bus ACC

Note 1: U = Source
Dest = Destination

Y BUS AND STATUS – ROTATE BY n BITS INSTRUCTIONS

Instruction	Op-code	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
ROTR1 ROTR2 ROTNR		1 = W	$Y_i \leftarrow SRC_{(i-n)mod16}$	NC	NC	NC	NC	0	SRC_{15-n}	0	U
		0 = B	$Y_i \leftarrow SRC_{i+8} = SRC_{(i-n)mod8}$ for i = 0 to 7	NC	NC	NC	NC	0	SRC_{8-n}	0	U

SRC = Source
U = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

ROTATE AND MERGE INSTRUCTION

The Rotate and Merge Instructions contain five indicators: byte or word mode, rotated source, non-rotated source/destination, mask and the number of bit positions a source is to be rotated. The function performed by the Rotate and Merge instruction is illustrated in Figure 6. The rotated source, U, is rotated up by the Barrel Shifter n places. The mask input then selects, on a bit by bit basis, the rotated U input or R input. A ZERO in bit i of the mask will select the i^{th} bit of the R input as the i^{th} output bit, while ONE in bit i will select the i^{th} rotated U input as the output bit. The output word is stored in the non-rotated operand location. The N and Z bits are affected. The OVR and C bits of the Status register are forced to ZERO. An example of this instruction is given in Figure 7.

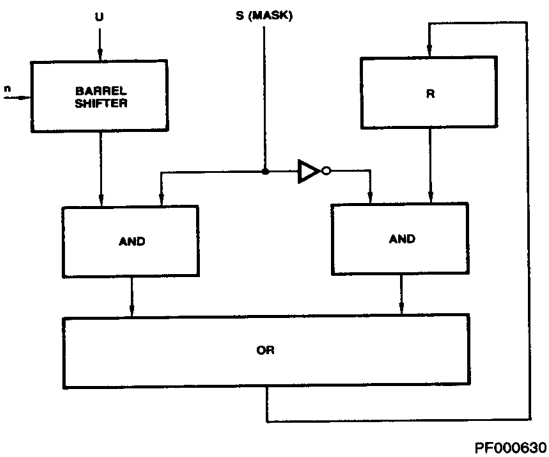

Figure 6. Rotate and Merge Function.

ROTATE AND MERGE FIELD DEFINITIONS:

	15	14 13	12 9	8 5	4 0
ROTM	B/W	Quad	n	ROT SRC-Non ROT SRC-Mask	RAM Address

EXAMPLE: n = 4, Word Mode

U	0011	0001	0101	0110
Rotated U	0001	0101	0110	0011
R	1010	1010	1010	1010
Mask (S)	0000	1111	0000	1111
Destination	1010	0101	1010	0011

Figure 7. Rotate and Merge Example.

ROTATE AND MERGE INSTRUCTION

Instruction	B/W	Quad	n			U[1]	R/Dest[1]	S[1]	RAM Address		
ROTM	0 = B 1 = W	01	0 to 15	0111	MDAI	D	ACC	I	00000	R00	RAM Reg 00
				1000	MDAR	D	ACC	RAM	..	..	....
				1001	MDRI	D	RAM	I	11111	R31	RAM Reg 31
				1010	MDRA	D	RAM	ACC			
				1100	MARI	ACC	RAM	I			
				1110	MRAI	RAM	ACC	I			

Note 1. U = Rotated Source
R/Dest = Non-Rotated Source and Destination
S = Mask

Y BUS AND STATUS – ROTATED MERGE

Instruction	Opcode	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
ROTM		1=W	$Y_i \leftarrow (\text{Non Rot Op})_i \cdot \overline{(\text{mask})_i} + (\text{Rot Op})_{(i-n)\text{mod } 16} \cdot (\text{mask})_i$	NC	NC	NC	NC	0	U	0	U
		0 = B	$Y_i \leftarrow (\text{Non Rot Op})_i \cdot \overline{(\text{mask})_i} + (\text{Rot Op})_{(i-n)\text{mod } 8} \cdot (\text{mask})_i$	NC	NC	NC	NC	0	U	0	U

U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

ROTATE AND COMPARE INSTRUCTIONS

The Rotate and Compare Instructions contain five indicators: byte or word mode, rotated source, non-rotated source, mask, and the number of bit positions the rotated source is to be rotated up. Under the control of instruction inputs, the function performed by the Rotate and Compare instruction is illustrated in Figure 8. The rotated operand is rotated by the Barrel Shifter n places. The mask is inverted and ANDed on a bit-by-bit basis with the output of the Barrel Shifter and R input. Thus, a ONE in the mask input eliminates that bit from the comparison. A ZERO allows the comparison. If the comparison passes, the Zero flag is set. If it fails, the Zero flag is reset. The N and Z bit are affected. The OVR and C bits of the Status register are forced to ZERO. An example of this instruction is given in Figure 9.

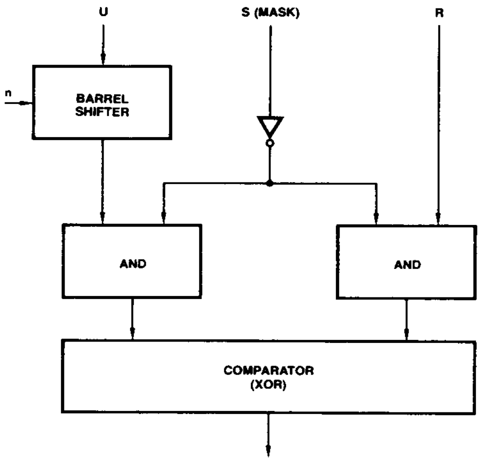

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Figure 8. Rotate and Compare Function.

ROTATE AND COMPARE FIELD DEFINITIONS

	15	14 13	12 9	8 5	4 0
ROTC	B/W	Quad	n	Rot Src- Non Rot Src- Mask	RAM Address

EXAMPLE: n = 4, Word Mode

U	0011	0001	0101	0110
U Rotated	0001	0101	0110	0011
R	0001	0101	1111	0000
Mask (S)	0000	0000	1111	1111
Z (status) = 1				

Figure 9. Rotate and Compare Examples.

ROTATE AND COMPARE INSTRUCTIONS

Instruction	B/W	Quad	n			U[1]	R[1]	S[1]	RAM Address		
ROTC	0=B 1 = W	01	0 to 15	0010	CDAI	D	ACC	I	00000	R00	RAM Reg 00
				0011	CDRI	D	RAM	I	..	..	...
				0100	CDRA	D	RAM	ACC	11111	R31	RAM Reg 31
				0101	CRAI	RAM	ACC	I			

Note 1. U = Rotated Source
R = Non-Rotated Source
S = Mask

Y BUS AND STATUS – ROTATE AND COMPARE

Instruction	Opcode	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
ROTC		1 = W	$Y_i \leftarrow (\text{Non Rot Op})_i \cdot \overline{(\text{mask})_i} \oplus (\text{Rot Op})_{(i-n)\text{mod } 16} \cdot (\text{mask})_i$	NC	NC	NC	NC	0	U	0	U
		0 = B	$Y_i \leftarrow (\text{Non Rot Op})_i \cdot \overline{(\text{mask})_i} \oplus (\text{Rot Op})_{(i-n)\text{mod } 8} \cdot (\text{mask})_i$	NC	NC	NC	NC	0	U	0	U

U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

PRIORITIZE INSTRUCTION

The Prioritize Instructions contain four indicators: byte or word mode, operand source (R), mask source (S) and destination. They are further subdivided into two types. The function performed by the Prioritize instruction is shown in Figure 10. The R operand is ANDed with the complement of the Mask operand. A ZERO in the Mask operand allows the corresponding bit in the R operand to participate in the priority encoding function. A ONE in the Mask operand forces the corresponding bit in the R operand to a ZERO, eliminating it from participation in the priority encoding function.

The priority encoder accepts a 16-bit input and produces a 5-bit binary-weighted code indicating the bit position of the highest priority active bit. If none of the inputs are active, the output is ZERO. In the Word mode, if input bit 15 is active, the output is 1, etc. Figure 11 lists the output as a function of the highest-priority active-bit position in both the Word and Byte mode. The N and Z bits are affected and the OVR and C bits of the status register are forced to ZERO. The only limitation in this instruction is that the operand and the mask must be different sources.

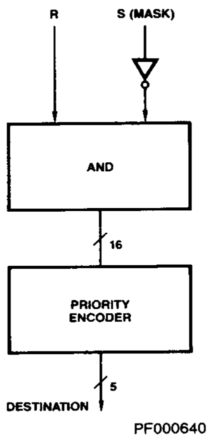


Figure 10. Prioritize Function.

PRIORITIZE INSTRUCTION FIELD DEFINITIONS

15	14 13	12 — 9	8 — 5	4 — 0
B/W	Quad	Destination	Source (R)	RAM Address/ Mask (S)
B/W	Quad	Mask (S)	Destination	RAM Address/ Source (R)
B/W	Quad	Mask (S)	Source (R)	RAM Address/ Destination
B/W	Quad	Mask (S)	Source (R)	Destination

WORD MODE		BYTE MODE*	
Highest Priority Active Bit	Encoder Output	Highest Priority Active Bit	Encoder Output
None	0	None	0
15	1	7	1
14	2	6	2
.	.	.	.
.	.	.	.
1	15	1	7
0	16	0	8

*Bits 8 through 15 do not participate.

Figure 11.

PRIORITIZE INSTRUCTION

Instruction	B/W	Quad	Destination	Source (R)	RAM Address/Mask (S)
PRT1	0 = B 1 = W	10	1000 PRIA ACC 1010 PR1Y Y Bus 1011 PR1R RAM	0111 RPT1A ACC 1001 PR1D D	00000 R00 RAM Reg 00 .. .. 11111 R31 RAM Reg 31
Instruction	**B/W**	**Quad**	**Mask (S)**	**Destination**	**RAM Address/Source (R)**
PRT2	0 = B 1 = W	10	1000 PRA Acc 1010 PRZ 0 1011 PRI I	0000 PR2A ACC 0010 PR2Y Y Bus	00000 R00 RAM Reg 00 .. .. 11111 R31 RAM Reg 31
Instruction	**B/W**	**Quad**	**Mask (S)**	**Source (R)**	**RAM Address/Dest**
PRT3	0 = B 1 = W	10	1000 PRA ACC 1010 PRZ 0 1011 PRI I	0011 PR3R RAM 0100 PR3A ACC 0110 PR3D D	00000 R00 RAM Reg 00 .. .. 11111 R31 RAM Reg 31
Instruction	**B/W**	**Quad**	**Mask (S)**	**Source (R)**	**Destination**
PRTNR	0 = B 1 = W	11	1000 PRA ACC 1010 PRZ 0 1011 PRI I	0100 PRTA ACC 0110 PRTD D	00000 NRY Y Bus 00001 NRA ACC

Y BUS AND STATUS - PRIORITIZE INSTRUCTION

Instruction	Opcode	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
PRT1 PRT2 PRT3 PRTNR		1 = W	$Y_i \leftarrow$ CODE $(SCR_n \cdot \overline{mask_n})$; $Y_m \leftarrow 0$; i = 0 to 4 and n = 0 to 15 m = 5 to 15	NC	NC	NC	NC	0	U	0	U
		0 = B	$Y_i \leftarrow$ CODE $(SCR_n \cdot \overline{mask_n})$; $Y_m \leftarrow 0$; i = 0 to 3 and n = 0 to 7 m = 4 to 15	NC	NC	NC	NC	0	U	0	U

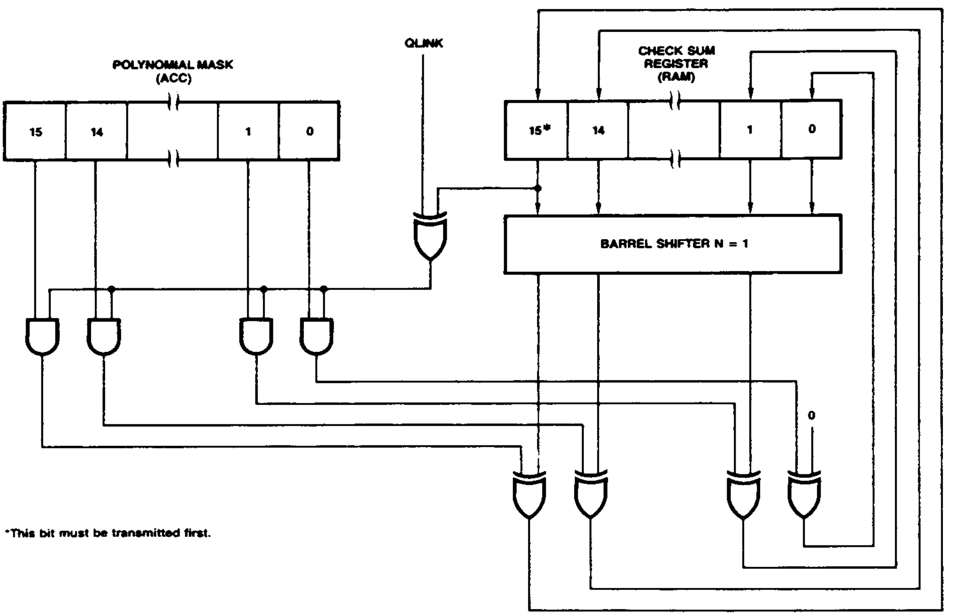
SRC = Source
U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

CRC INSTRUCTION

The CRC (Cyclic-Redundancy-Check) Instructions contain one indicator: address of a RAM register to use as the check sum register. The CRC instruction provides a method for generation of the check bits in a CRC calculation. Two CRC instructions are provided – CRC Forward and CRC Reverse. The reason for providing two instructions is that CRC standards do not specify which data bit is to be transmitted first, the LSB or the MSB, but they do specify which check bit must be transmitted first. Figure 12 illustrates the method used to generate these check bits for the CRC Forward function and Figure 13 illustrates method used for the 2CRC Reverse function. The ACC serves as a polynominal mask to define the generating polynomial while the RAM register holds the partial result and eventually the calculated check sum. The LINK-bit is used as the serial input. The serial input combines with the MSB of the check-sum register, according to the polynomial defined by the polynomial mask register. When the last input bit has been processed, the check-sum register contains the CRC check bits. The LINK, N and Z bits are affected and the OVR and C bits of the Status register are forced to ZERO.

CYCLIC-REDUNDANCY-CHECK DEFINITIONS:

	15	14 13	12 9	8 5	4 0
CRCF	1	Quad	0110	0011	RAM Address
CRCR	1	Quad	0110	1001	RAM Address

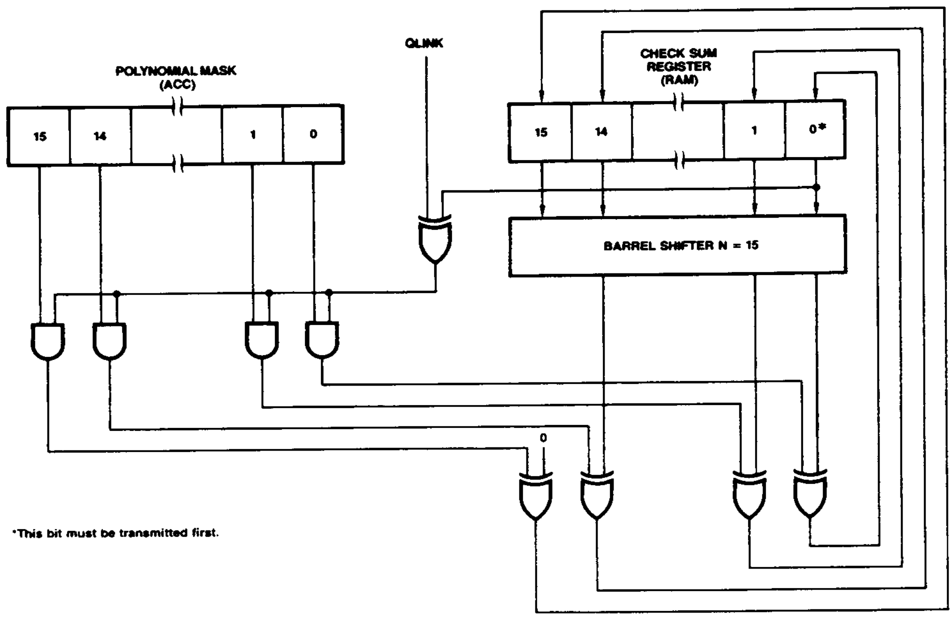


*This bit must be transmitted first.

PF000330

Figure 12. CRC Forward Function.

CRC INSTRUCTION



PF000320

Figure 13. CRC Reverse Function.

CYCLIC REDUNDANCY CHECK

Instruction	B/W	Quad			RAM Address		
CRCF	1	10	0110	0011	00000 .. 11111	R00 .. R31	RAM Reg 00 .... RAM Reg 31
Instruction	**B/W**	**Quad**			**RAM Address**		
CRCR	1	10	0110	1001	00000 .. 11111	R00 .. R31	RAM Reg 00 .... RAM Reg 31

Y BUS AND STATUS – CYCLIC REDUNDANCY CHECK

Instruction	Opcode	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
CRCF		1 = W	$Y_i \leftarrow [(QLINK \oplus RAM_{15}) \cdot ACC_i]$ $\oplus RAM_{i-1}$ for i = 15 to 1 $Y_0 \leftarrow [(QLINK \oplus RAM_{15}) \cdot ACC_0] \oplus 0$	NC	NC	NC	RAM_{15}*	0	U	0	U
CRCR		1 = W	$Y_i \leftarrow [(QLINK \oplus RAM_0) \cdot ACC_i]$ $\oplus RAM_{i+1}$ for i = 14 to 0 $Y_{15} \leftarrow [(QLINK \oplus RAM_0) \cdot ACC_{15}] \oplus 0$	NC	NC	NC	RAM_0*	0	U	0	U

*QLINK is loaded with the shifted out bit from the checksum register.

U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

STATUS INSTRUCTIONS

Status Instructions – The Set Status Instruction contains a single indicator. This indicator specifies which bit or group of bits, contained in the status register (Figure 14), are to be set (forced to a ONE).

7	6	5	4	3	2	1	0
Flag3	Flag2	Flag1	LINK	OVR	N	C	Z

MPR-775

Figure 14. Status Byte.

The Reset Status Instruction contains a single indicator. This indicator specifies which bit or group of bits, contained in the status register, are to be reset (forced to ZERO).

The Store Status Instruction contains two indicators; byte/word and a second indicator that specifies the destination of the status register. The Store Status Instruction allows the status of the processor to be saved and restored later, which is an especially useful function for interrupt handling.

The status register is always stored in the lower byte of the RAM or the ACC register. Depending upon byte or word mode the upper byte is unchanged or loaded with all ZEROs respectively.

The Load Status instructions are included in the single operand and two operand instruction types.

The Test Status Instructions contain a single indicator which specifies which one of the 12 possible test conditions are to be placed on the Conditional-Test output. Besides the eight bits in the Status register (QZ, QC, QN, QOVR, QLINK, QFlag1, QFlag 2, and QFlag3), four logical functions (QN $\oplus$ QOVR), (QN $\oplus$ QOVR) + QZ, QZ + $\overline{QC}$ and LOW may also be selected. These functions are useful in testing results of Two's Complement and unsigned number arithmetic operations. The status register may also be tested via the bidirectional T bus. The code to test the status register via T bus is similar to the code used by instruction lines I_1 to I_4 as shown below. Instruction lines I_{0-4} have priority over T bus for testing the status register on CT output. See the discussion on the status register for a full description.

T_4 I_4	T_3 I_3	T_2 I_2	T_1 I_1	CT
0	0	0	0	(N $\oplus$ OVR) + Z
0	0	0	1	N $\oplus$ OVR
0	0	1	0	Z
0	0	1	1	OVR
0	1	0	0	LOW*
0	1	0	1	C
0	1	1	0	Z + $\overline{C}$
0	1	1	1	N
1	0	0	0	LINK
1	0	0	1	Flag1
1	0	1	0	Flag2
1	0	1	1	Flag3

*LOW means CT is forced LOW

STATUS

	15	14 13	12 9	8 5	4 0
SETST	0	Quad	1011	1010	Opcode
RSTST	0	Quad	1010	1010	Opcode
SVSTR	B/W	Quad	0111	1010	RAM Address/Dest
SVSTNR	B/W	Quad	0111	1010	Destination

STATUS INSTRUCTIONS

Instruction	B/W	Quad			Opcode		
SETST	0	11	1011	1010	00011	SONCZ	Set OVR, N, C, Z
					00101	SL	Set LINK
					00110	SF1	Set Flag1
					01001	SF2	Set Flag2
					01010	SF3	Set Flag3
Instruction	**B/W**	**Quad**			**Opcode**		
RSTST	0	11	1010	1010	00011	RONCZ	Reset OVR, N, C, Z
					00101	RL	Reset LINK
					00110	RF1	Reset Flag1
					01001	RF2	Reset Flag2
					01010	RF3	Reset Flag3
Instruction	**B/W**	**Quad**			**RAM Address/Dest**		
SVSTR	0 = B 1 = W	10	0111	1010	00000	R00	RAM Reg 00
					..	..	....
					11111	R31	RAM Reg 31
					Destination		
SVSTNR	0 = B 1 = W	11	0111	1010	00000	NRY	Y Bus
					00001	NRA	ACC

STATUS INSTRUCTIONS

Instruction	B/W	Quad			Opcode (CT)		
Test	0	11	1001	1010	00000	TNOZ	Test (N⊕OVR) + Z
					00010	TNO	Test N⊕OVR
					00100	TZ	Test Z
					00110	TOVR	Test OVR
					01000	TLOW	Test LOW
					01010	TC	Test C
					01100	TZC	Test $Z + \overline{C}$
					01110	TN	Test N
					10000	TL	Test LINK
					10010	TF1	Test Flag1
					10100	TF2	Test Flag2
					10110	TF3	Test Flag3

Note: $\overline{IEN}$ · test status instruction has priority over T_{1-4} instruction.

Y BUS AND STATUS – FOR STATUS INSTRUCTIONS

Instruction	Opcode	Description	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
SETST	SONCZ	Set OVR, N, C, Z	0 = B	$Y_i \leftarrow 1$ for i = 0 to 15	NC	NC	NC	NC	1	1	1	1
	SL	Set LINK			NC	NC	NC	1	NC	NC	NC	NC
	SF1	Set Flag1			NC	NC	1	NC	NC	NC	NC	NC
	SF2	Set Flag2			NC	1	NC	NC	NC	NC	NC	NC
	SF3	Set Flag3			1	NC	NC	NC	NC	NC	NC	NC
RSTST	RONCZ	Reset OVR, N, C, Z	0 = B	$Y_i \leftarrow 0$ for i = 0 to 15	NC	NC	NC	NC	0	0	0	0
	RL	Reset LINK			NC	NC	NC	0	NC	NC	NC	NC
	RF1	Reset Flag1			NC	NC	0	NC	NC	NC	NC	NC
	RF2	Reset Flag2			NC	0	NC	NC	NC	NC	NC	NC
	RF3	Reset Flag3			0	NC	NC	NC	NC	NC	NC	NC
SVSTR SVSTNR		Save Status*	0 = B 1 = W	$Y_i \leftarrow$ Status for i – 0 to 7; $Y_i \leftarrow 0$ for i = 8 to 15	NC	NC	NC	NC	NC	NC	NC	NC
Test	TNOZ	Test (N⊕OVR) + Z	0 = B	**	NC	NC	NC	NC	NC	NC	NC	NC
	TNO	Test N⊕OVR			NC	NC	NC	NC	NC	NC	NC	NC
	TZ	Test Z			NC	NC	NC	NC	NC	NC	NC	NC
	TOVR	Test OVR			NC	NC	NC	NC	NC	NC	NC	NC
	TLOW	Test LOW			NC	NC	NC	NC	NC	NC	NC	NC
	TC	Test C			NC	NC	NC	NC	NC	NC	NC	NC
	TZC	Test $Z + \overline{C}$			NC	NC	NC	NC	NC	NC	NC	NC
	TN	Test N			NC	NC	NC	NC	NC	NC	NC	NC
	TL	Test LINK			NC	NC	NC	NC	NC	NC	NC	NC
	TF1	Test Flag1			NC	NC	NC	NC	NC	NC	NC	NC
	TF2	Test Flag2			NC	NC	NC	NC	NC	NC	NC	NC
	TF3	Test Flag3			NC	NC	NC	NC	NC	NC	NC	NC

U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

*In byte mode only the lower byte from the Y bus is loaded into the RAM or ACC and in word mode all 16-bits from the Y bus are loaded into the RAM or ACC.

**Y-Bus is Undefined.

NO-OP INSTRUCTION

The NO-OP Instruction has a fixed 16-bit code. This instruction does not change any internal registers in the Am29116. It preserves the status register, RAM register and the ACC register.

NO OPERATION FIELD DEFINITION

	15	14 13	12 9	8 5	4 0
NOOP	0	11	1000	1010	00000

NO-OP INSTRUCTION

Instruction	B/W	Quad			
NOOP	0	11	1000	1010	00000

Y BUS AND STATUS – NO-OP INSTRUCTION

Instruction	Opcode	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
NOOP		0 = B	*	NC	NC	NC	NC	NC	NC	NC	NC

SRC = Source
U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified
*Y-Bus is undefined.

SUMMARY OF MNEMONICS

Instruction Type

SOR	Single Operand RAM
SONR	Single Operand Non-RAM
TOR1	Two Operand RAM (Quad 0)
TOR2	Two Operand RAM (Quad 2)
TONR	Two Operand Non-RAM
SHFTR	Single Bit Shift RAM
SHFTNR	Single Bit Shift Non-RAM
ROTR1	Rotate n Bits RAM (Quad 0)
ROTR2	Rotate n Bits RAM (Quad 1)
ROTNR	Rotate n Bits Non-RAM
BOR1	Bit Oriented RAM (Quad 3)
BOR2	Bit Oriented RAM (Quad 2)
BONR	Bit Oriented Non-RAM
ROTM	Rotate and Merge
ROTC	Rotate and Compare
PRT1	Prioritize RAM; Type 1
PRT2	Prioritize RAM; Type 2
PRT3	Prioritize RAM; Type 3
PRTNR	Prioritize Non-RAM
CRCF	Cyclic Redundancy Check Forward
CRCR	Cyclic Redundancy Check Reverse
NOOP	No Operation
SETST	Set Status
RSTST	Reset Status
SVSTR	Save Status RAM
SVSTNR	Save Status Non-RAM
TEST	Test Status

SOURCE AND DESTINATION

Single Operand

SORA	Single Operand RAM to ACC
SORY	Single Operand RAM to Y Bus
SORS	Single Operand RAM to Status
SOAR	Single Operand ACC to RAM
SODR	Single Operand D to RAM
SOIR	Single Operand I to RAM
SOZR	Single Operand 0 to RAM
SOZER	Single Operand D(0E) to RAM
SOSER	Single Operand D(SE) to RAM
SORR	Single Operand RAM to RAM
SOA	Single Operand ACC
SOD	Single Operand D
SOI	Single Operand I
SOZ	Single Operand 0
SOZE	Single Operand D(0E)
SOSE	Single Operand D(SE)
NRY	Non-RAM Y Bus
NRA	Non-RAM ACC
NRS	Non-RAM Status
NRAS	Non-RAM ACC, Status

Two Operand

TORAA	Two Operand RAM, ACC to ACC
TORIA	Two Operand RAM, I to ACC
TODRA	Two Operand D, RAM to ACC
TORAY	Two Operand RAM, ACC to Y Bus
TORIY	Two Operand RAM, I to Y Bus
TODRY	Two Operand D, RAM to Y Bus
TORAR	Two Operand RAM, ACC to RAM
TORIR	Two Operand RAM, I to RAM
TODRR	Two Operand D, RAM to RAM
TODAR	Two Operand D, ACC to RAM
TOAIR	Two Operand ACC, I to RAM
TODIR	Two Operand D, I to RAM
TODA	Two Operand D, ACC
TOAI	Two Operand ACC, I
TODI	Two Operand D, I

Single Bit Shift

SHRR	Shift RAM, Store in RAM
SHDR	Shift D, Store in RAM
SHA	Shift ACC
SHD	Shift D

Rotate n Bits

RTRA	Rotate RAM, Store in ACC
RTRY	Rotate RAM, Place on Y Bus
RTRR	Rotate RAM, Store in RAM
RTAR	Rotate ACC, Store in RAM
RTDR	Rotate D, Store in RAM
RTDY	Rotate D, Place on Y Bus
RTDA	Rotate D, Store in ACC
RTAY	Rotate ACC, Place on Y Bus
RTAA	Rotate ACC, Store in ACC

Rotate and Merge

MDAI	Merge Disjoint Bits of D and ACC Using I as Mask and Store in ACC
MDAR	Merge Disjoint Bits of D and ACC Using RAM as Mask and Store in ACC
MDRI	Merge Disjoint Bits of D and RAM Using I as Mask and Store in RAM
MDRA	Merge Disjoint Bits of D and RAM Using ACC as Mask and Store in RAM
MARI	Merge Disjoint Bits of ACC and RAM Using I as Mask and Store in RAM
MRAI	Merge Disjoint Bits of RAM and ACC Using I as Mask and Store in ACC

Rotate and Compare

CDAI	Compare Unmasked Bits of D and ACC Using I as Mask

CDRI	Compare Unmasked Bits of D and RAM Using I as Mask
CDRA	Compare Unmasked Bits of D and RAM Using ACC as Mask
CRAI	Compare Unmasked Bits of RAM and ACC Using I as Mask

Prioritize

PR1A	ACC as Destination for Prioritize Type 1
PR1Y	Y Bus as Destination for Prioritize Type 1
PR1R	RAM as Destination for Prioritize Type 1
PRT1A	ACC as Source for Prioritize Type 1
PR1D	D as Source for Prioritize Type 1
PR2A	ACC as Destination for Prioritize Type 2
PR2Y	Y Bus as Destination for Prioritize Type 2
PR3R	RAM as Source for Prioritize Type 3
PR3A	ACC as Source for Prioritize Type 3
PR3D	D as Source for Prioritize Type 3
PRTA	ACC as source for Prioritize Type Non-RAM
PRTD	D as Source for Prioritize Type Non-RAM
PRA	ACC as Mask for Prioritize Type 2, 3, and Non-RAM
PRZ	Mask Equal to Zero for Prioritize Type 2, 3, and Non-RAM
PRI	I as Mask for Prioritize Type 2, 3, and Non-RAM

OPCODE

Addition

ADD	Add without Carry
ADDC	Add with Carry
A2NA	Add 2^n to ACC
A2NR	Add 2^n to RAM
A2NDY	Add 2^n to D, Place on Y Bus

Subtraction

SUBR	Subtract R from S without Carry
SUBRC	Subtract R from S with Carry
SUBS	Subtract S from R without Carry
SUBSC	Subtract S from R with Carry
S2NR	Subtract 2^n from RAM
S2NA	Subtract 2^n from ACC
S2NDY	Subtract 2^n from D, Place on Y Bus

Logical Operations

AND	Boolean AND
NAND	Boolean NAND
EXOR	Boolean EXOR
NOR	Boolean NOR
OR	Boolean OR
EXNOR	Boolean EXNOR

SHIFTS

SHUPZ	Shift Up Towards MSB with 0 Insert
SHUP1	Shift Up Towards MSB with 1 Insert
SHUPL	Shift Up Towards MSB with LINK Insert
SHDNZ	Shift Down Towards LSB with 0 Insert
SHDN1	Shift Down Towards LSB with 1 Insert
SHDNL	Shift Down Towards LSB with LINK Insert
SHDNC	Shift Down Towards LSB with Carry Insert
SHDNOV	Shift Down Towards LSB with Sign EXOR Overflow Insert

Loads

LD2NR	Load 2^n into RAM
LDC2NR	Load $\overline{2^n}$ into RAM
LD2NA	Load 2^n into ACC
LDC2NA	Load $\overline{2^n}$ into ACC
LD2NY	Place 2^n on Y Bus
LDC2NY	Place $\overline{2^n}$ on Y Bus

Bit Oriented

SETNR	Set RAM, Bit n
SETNA	Set ACC, Bit n
SETND	Set D, Bit n
SONCZ	Set OVR, N, C, Z, in Status Register
SL	Set LINK Bit in Status Register
SF1	Set Flag1 Bit in Status Register
SF2	Set Flag2 Bit in Status Register
SF3	Set Flag3 Bit in Status Register
RSTNR	Reset RAM, Bit n
RSTNA	Reset ACC, Bit n
RSTND	Reset D, Bit n
RONCZ	Reset OVR, N, C, Z, in Status Register
RL	Reset LINK Bit in Status Register
RF1	Reset Flag1 Bit in Status Register
RF2	Reset Flag2 Bit in Status Register
RF3	Reset Flag3 Bit in Status Register
TSTNR	Test RAM, Bit n
TSTNA	Test ACC, Bit n
TSTND	Test D, Bit n

Arithmetic Operations

MOVE	Move and Update Status
COMP	Complement (1's Complement)
INC	Increment
NEG	Two's Complement

Conditional Test

TNOZ	Test $(N \oplus OVR) + Z$
TNO	Test $N \oplus OVR$
TZ	Test Zero Bit
TOVR	Test Overflow Bit
TLOW	Test for LOW
TC	Test Carry Bit
TZC	Test $Z + \overline{C}$
TN	Test Negative Bit
TL	Test LINK Bit
TF1	Test Flag1 Bit
TF2	Test Flag2 Bit
TF3	Test Flag3 Bit

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65 to +150°C
(Case) Temperature Under Bias .... −55 to +125°C
Supply Voltage to Ground Potential ...... −0.5 V to +7.0 V
DC Voltage Applied to Outputs For
  High Output State .... −0.5 V to $+V_{CC}$ Max.
DC Input Voltage .... −0.5 V to +5.5 V
DC Output Current, Into Outputs .... 30 mA
DC Input Current .... −30 mA to +5.0 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
  Temperature (T_A) .... 0 to +70°C
  Supply Voltage .... +4.75 V to +5.25 V

Military (M) Devices
  Temperature (T_C) .... −55 to +125°C
  Supply Voltage .... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified; All APL and CPL products are included in Group A, Subgroup 1, 2, 3 tests unless otherwise noted.

Parameters	Description	Test Conditions (Note 2)			Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min. $V_{IN} = V_{IH}$ or V_{IL}	Y_{0-15} T_{1-4} CT	I_{OH} = −1.6 mA/−1.2 mA (COM'L/MIL)	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min. $V_{IN} = V_{IH}$ or V_{IL}	Y_{0-15} T_{1-4} CT	I_{OL} = 16 mA/12 mA (COM'L/MIL)			0.5	Volts
V_{IH}	Guaranteed Input Logical HIGH Voltage (Note 6)		All Inputs		2.0			Volts
V_{IL}	Guaranteed Input Logical LOW Voltage (Note 6)		All Inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = Min.	All Inputs	I_{IN} = −18 mA			−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = Max. V_{IN} = 0.5 Volts (Note 4)	$\overline{IEN}$ $\overline{SRE}$ DLE I_{0-4} I_{5-15} $\overline{OE}_T$ $\overline{OE}_Y$ CP T_{1-4} Y_{0-15}				−0.50 −0.50 −1.00 −1.00 −0.50 −0.50 −0.50 −1.50 −0.55 −0.55	mA
I_{IH}	Input HIGH Current	V_{CC} = Max. V_{IN} = 2.4 Volts (Note 4)	$\overline{IEN}$ $\overline{SRE}$ $\overline{DLE}$ I_{0-4} I_{5-15} $\overline{OE}_T$ $\overline{OE}_Y$ CP T_{1-4} Y_{0-15}				50 50 100 100 50 50 50 150 100 100	μA
I_I	Input HIGH Current	V_{CC} = Max. V_{IN} = 5.5 Volts	All Inputs				1.0	mA
I_{OZH}	Off State (HIGH Impedance) Output Current	V_{CC} = Max. V_O = 2.4 Volts (Note 4)	T_{1-4} Y_{0-15}				100	μA
I_{OZL}	Off State (HIGH Impedance) Output Current	V_{CC} = Max. V_O = 0.5 Volts (Note 4)	T_{1-4} Y_{0-15}				−550	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max. + 0.5 Volts V_O = 0.5 Volts (Note 3)			−30		−85	mA
I_{CC}	Power Supply Current (Note 5)	V_{CC} = Max.	COM'L	T_A = 0 to 70°C (Note 7)			735	mA
				T_A = 70°C			605	
			COM'L (Am29L116A only)	T_A = 0 to 70°C (Note 7)			550	
				T_A = 70°C			400	
			MIL (Am29116 only)	T_C = −55 to 125°C (Note 7)			745	
				T_C = 125°C			525	

Notes:
1. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2. For conditions shown as Min. or Max., use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Y_{0-15}, T_{1-4} are three-state outputs internally connected to TTL inputs. Input characteristics are measured under conditions such that the outputs are in the OFF state.
5. Worst case I_{CC} is at minimum temperature.
6. These input levels provide zero noise immunity and should be tested only in a static, noise-free environment.
7. Cold start.

GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

($T_A = 0$ to $+70°C$, $V_{CC} = 4.75$ to 5.25 V, $C_L = 50$ pF)

A. Combinational Delays (nsec)

		Outputs		
		Y_{0-15}	T_{1-4}	CT
Input	I_{0-4} (ADDR)	79	84	–
	I_{0-15} (DATA)	79	84	–
	I_{0-15} (INSTR)	79	84	48
	DLE	58*	60	–
	T_{1-4}	–	–	39
	CP	56	62	36
	Y_{0-15}	62*	64	–
	$\overline{IEN}$	–	–	43

Y_{0-15} must be stored in the Data Latch and is source disabled before the delay to Y_{0-15} as an output can be measured.
*Guaranteed indirectly by other tests.

B. Enable/Disable Times (nsec)
($C_L = 5$ pF for disable only)

From Input	To Output	Enable t_{PZH}	Enable t_{PZL}	Disable t_{PHZ}	Disable t_{PLZ}
$\overline{OE}_Y$	Y_{0-15}	20	20	20	20
OE_T	T_{1-4}	25	25	25	25

C. Clock and Pulse Requirements (nsec)

Input	Min Low Time	Min High Time
CP	20	30
DLE	–	15
$\overline{IEN}$	22	–

D. Set-up and Hold Times (nsec)

Input	With Respect to	High-to-Low Transition Set-up	High-to-Low Transition Hold	Low-to-High Transition Set-up	Low-to-High Transition Hold	Comment
I_{0-4} (RAM ADDR)	CP	(t_{s1}) 24	(t_{h1}) 0	–	–	Single ADDR (Source)
I_{0-4} (RAM ADDR)	CP and $\overline{IEN}$ both LOW	(t_{s2}) 10	–	–	(t_{h7}) 0	Two ADDR (Destination)
I_{0-15} (DATA)	CP	–	–	(t_{s8}) 65	(t_{h8}) 0	
I_{0-15} (INSTR)	CP	(t_{s3}) 38*	(t_{h3})* 17	(t_{s9}) 65	(t_{h9}) 0	
$\overline{IEN}$ HIGH	CP	(t_{s4}) 10	–	–	(t_{h10}) 0	Disable
$\overline{IEN}$ LOW	CP	– ; (t_{s5}) 20	– ; (t_{h5})* 0	(t_{s11}) 22 ; –	(t_{h11})** 0 ; –	Enable ; Immediate first cycle
$\overline{SRE}$	CP	–	–	(t_{s12}) 17	(t_{h12}) 0	
Y	CP	–	–	(t_{s13}) 44	(t_{h13}) 0	
Y	DLE	(t_{s6}) 10	(t_{h6}) 6	–	–	
DLE	CP	–	–	(t_{s14}) 42	(t_{h14}) 0	

*Timing for immediate instruction for first cycle.
**Status register and accumulator destination only.

Am29116 SWITCHING CHARACTERISTICS (Cont'd.)

(All APL and CPL products are included in Group A, Subgroup 9, 10, 11 tests unless otherwise noted)

GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE

($T_C = -55$ to $+125°C$, $V_{CC} = 4.5$ to 5.5 V, $C_L = 50$ pF)

A. Combinational Delays (nsec)

		Outputs		
		Y_{0-15}	T_{1-4}	CT
Input	I_{0-4} (ADDR)	100	103	–
	I_{0-15} (DATA)	100	103	–
	I_{0-15} (INSTR)	100	103	50
	DLE	68* †	70	–
	T_{1-4}	–	–	46
	CP	70	73	43
	Y_{0-15}	70* †	72	–
	$\overline{IEN}$	–	–	50

Y_{0-15} must be stored in the Data Latch and its source disabled before the delay to Y_{0-15} as an output can be measured.
*Guaranteed indirectly by other tests.

B. Enable/Disable Times (nsec)
(C_L = 5 pF for disable only)

From Input	To Output	Enable		Disable	
		t_{PZH}	t_{PZL}	t_{PHZ}	t_{PLZ}
$\overline{OE}_Y$	Y_{0-15}	25	25	25	25
OE_T	T_{1-4}	30	30	30	30

C. Clock and Pulse Requirements (nsec)

Input	Min Low Time	Min High Time
CP	33	50
DLE	–	20
$\overline{IEN}$	33	–

D. Set-up and Hold Times (nsec)

Input	With Respect to	High-to-Low Transition Set-up	High-to-Low Transition Hold	Low-to-High Transition Set-up	Low-to-High Transition Hold	Comment
I_{0-4} (RAM ADDR)	CP	(t_{s1}) 24	(t_{h1}) 0	–	–	Single ADDR (Source)
I_{0-4} (RAM ADDR)	CP and $\overline{IEN}$ both LOW	(t_{s2}) 10	–	–	(t_{h7}) 0	Two ADDR (Destination)
I_{0-15} (DATA)	CP	–	–	(t_{s8}) 76	(t_{h8}) 3	
I_{0-15} (INSTR)	CP	(t_{s3})* 57	(t_{h3})* 17	(t_{s9}) 76	(t_{h9}) 3	
$\overline{IEN}$ HIGH	CP	(t_{s4}) 10	–	–	(t_{h10}) 1	Disable
$\overline{IEN}$ LOW	CP	– / (t_{s5}) 20	– / (t_{h5})* 3	(t_{s11}) 28 / –	(t_{h11})** 1 / –	Enable / Immediate first cycle
$\overline{SRE}$	CP	–	–	(t_{s12}) 19	(t_{h12}) 0	
Y	CP	–	–	(t_{s13}) 50	(t_{h13}) 2	
Y	DLE	(t_{s6}) 11	(t_{h6}) 7	–	–	
DLE	CP	–	–	(t_{s14}) 50	(t_{h14}) 0	

*Timing for immediate instruction for first cycle.
**Status register and accumulator destination only.

† = Not included in Group A tests

Am29116A SWITCHING CHARACTERISTICS

GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

($T_A = 0$ to $+70°C$, $V_{CC} = 4.75$ to 5.25 V, $C_L = 50$ pF)

A. Combinational Delays (nsec)

		Outputs		
		Y_{0-15}	T_{1-4}	CT
Input	I_{0-4} (ADDR)	53	60	–
	I_{0-15} (DATA)	53	60	–
	I_{0-15} (INSTR)	53	60	29
	DLE	39*	39	–
	T_{1-4}	–	–	25
	CP	39	41	26
	Y_{0-15}	39*	39	–
	$\overline{IEN}$	–	–	25

Y_{0-15} must be stored in the Data Latch and is source disabled before the delay to Y_{0-15} as an output can be measured.
*Guaranteed indirectly by other tests.

B. Enable/Disable Times (nsec)
($C_L = 5$ pF for disable only)

From Input	To Output	Enable		Disable	
		t_{PZH}	t_{PZL}	t_{PHZ}	t_{PLZ}
$\overline{OE}_Y$	Y_{0-15}	22	22	22	22
OE_T	T_{1-4}	25	25	25	25

C. Clock and Pulse Requirements (nsec)

Input	Min Low Time	Min High Time
CP	20	30
DLE	–	15
$\overline{IEN}$	20	–

D. Set-up and Hold Times (nsec)

Input	With Respect to	High-to-Low Transition Set-up	High-to-Low Transition Hold	Low-to-High Transition Set-up	Low-to-High Transition Hold	Comment
I_{0-4} (RAM ADDR)	CP	(t_{s1}) 13	(t_{h1}) 0	–	–	Single ADDR (Source)
I_{0-4} (RAM ADDR)	CP and $\overline{IEN}$ both LOW	(t_{s2}) 7	–	–	(t_{h7}) 2	Two ADDR (Destination)
I_{0-15} (DATA)	CP	–	–	(t_{s8}) 45	(t_{h8}) 0	
I_{0-15} (INSTR)	CP	(t_{s3}) 24*	(t_{h3})* 5	(t_{s9}) 45	(t_{h9}) 0	
$\overline{IEN}$ HIGH	CP	(t_{s4}) 5	–	–	(t_{h10}) 1	Disable
$\overline{IEN}$ LOW	CP	– ; (t_{s5}) 7	– ; (t_{h5})* 1	(t_{s11}) 20 ; –	(t_{h11})** 1 ; –	Enable ; Immediate first cycle
$\overline{SRE}$	CP	–	–	(t_{s12}) 12	(t_{h12}) 2	
Y	CP	–	–	(t_{s13}) 32	(t_{h13}) 0	
Y	DLE	(t_{s6}) 6	(t_{h6}) 6	–	–	
DLE	CP	–	–	(t_{s14}) 30	(t_{h14}) 0	

*Timing for immediate instruction for first cycle.
**Status register and accumulator destination only.

Am29L116A SWITCHING CHARACTERISTICS

GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

(T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25 V, C_L = 50 pF)

A. Combinational Delays (nsec)

		Outputs		
		Y_{0-15}	T_{1-4}	CT
Input	I_{0-4} (ADDR)	79	84	–
	I_{0-15} (DATA)	79	84	–
	I_{0-15} (INSTR)	79	84	48
	DLE	58*	60	–
	T_{1-4}	–	–	39
	CP	56	62	36
	Y_{0-15}	62*	64	–
	$\overline{IEN}$	–	–	43

Y_{0-15} must be stored in the Data Latch and is source disabled before the delay to Y_{0-15} as an output can be measured.
*Guaranteed indirectly by other tests.

B. Enable/Disable Times (nsec)
(C_L = 5 pF for disable only)

From Input	To Output	Enable		Disable	
		t_{PZH}	t_{PZL}	t_{PHZ}	t_{PLZ}
$\overline{OE}_Y$	Y_{0-15}	20	20	20	20
OE_T	T_{1-4}	30	30	25	25

C. Clock and Pulse Requirements (nsec)

Input	Min Low Time	Min High Time
CP	20	30
DLE	–	15
$\overline{IEN}$	20	–

D. Set-up and Hold Times (nsec)

Input	With Respect to	High-to-Low Transition Set-up	High-to-Low Transition Hold	Low-to-High Transition Set-up	Low-to-High Transition Hold	Comment
I_{0-4} (RAM ADDR)	CP	(t_{s1}) 24	(t_{h1}) 0	–	–	Single ADDR (Source)
I_{0-4} (RAM ADDR)	CP and $\overline{IEN}$ both LOW	(t_{s2}) 10	–	–	(t_{h7}) 1	Two ADDR (Destination)
I_{0-15} (DATA)	CP	–	–	(t_{s8}) 65	(t_{h8}) 2	
I_{0-15} (INSTR)	CP	(t_{s3}) 38*	(t_{h3}) 17*	(t_{s9}) 65	(t_{h9}) 2	
$\overline{IEN}$ HIGH	CP	(t_{s4}) 10	–	–	(t_{h10}) 1	Disable
$\overline{IEN}$ LOW	CP	– / (t_{s5}) 20	– / (t_{h5})* 0	(t_{s11}) 22 / –	(t_{h11})** 2 / –	Enable / Immediate first cycle
$\overline{SRE}$	CP	–	–	(t_{s12}) 17	(t_{h12}) 0	
Y	CP	–	–	(t_{s13}) 44	(t_{h13}) 1	
Y	DLE	(t_{s6}) 12	(t_{h6}) 6	–	–	
DLE	CP	–	–	(t_{s14}) 42	(t_{h14}) 0	

*Timing for immediate instruction for first cycle.
**Status register and accumulator destination only.

Test Philosophy and Methods

The following points give the general philosophy that we apply to tests that must be properly engineered if they are to be implemented in an automatic testing environment. The specifics of what philosophies are applied to which test are shown in the data sheet and the data-sheet reconciliation that follow.

Capacitive Loading for AC Testing

Automatic testers and their associated hardware have stray capacitance that varies from one type of tester to another, but is generally around 50 pF. This, of course, makes it impossible to make direct measurements of parameters that call for smaller capacitive load than the associated stray capacitance. Typical examples of this are the so-called "float delays" that measure the propagation delays in to and out of the high-impedance state and are usually specified at a load capacitance of 5.0 pF. In these cases, the test is performed at the higher load capacitance (typically 50 pF) and engineering correlations based on data taken with a bench setup are used to determine the result at the lower capacitance.

Similarly, a product may be specified at more than one capacitive load. Since the typical automatic tester is not capable of switching loads in mid-test, it is impractical to make measurements at both capacitances even though they may both be greater than the stray capacitance. In these cases, a measurement is made at one of the two capacitances. The result at the other capacitance is determined from engineering correlations based on data taken with a bench setup and the knowledge that certain DC tests are performed in order to facilitate this correlation.

AC loads specified in the data sheet are used for bench testing. Automatic tester loads, which simulate the data-sheet loads, may be used during production testing.

Threshold Testing

The noise associated with automatic testing, the long inductive cables, and the high gain of bipolar devices frequently give rise to oscillations when testing high-speed circuits. These oscillations are not indicative of a reject device, but instead, of an overtaxed system. To minimize this problem, thresholds are tested at least once for each input pin. Thereafter, "hard" high and low levels are used for other tests. Generally this means that function and AC testing are performed at "hard" input levels.

AC Testing

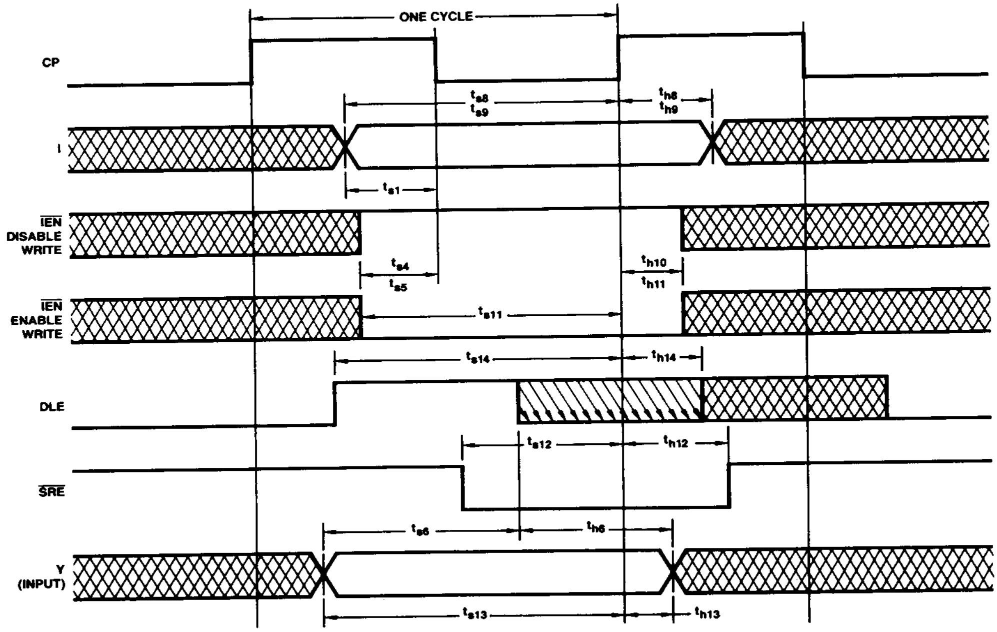
AC parameters are specified that cannot be measured accurately on automatic testers because of tester limitations. Data-input hold times fall into this category. In these cases, the parameter in question is tested by correlating the tester to bench data or oscilloscope measurements made on the tester by engineering (supporting data on file).

Certain AC tests are redundant since they can be shown to be predicted by other tests that have already been performed. In these cases, the redundant tests are not performed.

Output Short-Circuit Current Testing

When performing I_{OS} tests on devices containing RAM or registers, great care must be taken that undershoot caused by grounding the high-state output does not trigger parasitic elements which in turn cause the device to change state. In order to avoid this effect, it is common to make the measurement at a voltage (V_{output}) that is slightly above ground. The V_{CC} is raised by the same amount so that the result (as confirmed by Ohm's law and precise bench testing) is identical to the $V_{OUT} = 0$, $V_{CC} =$ Max. case.

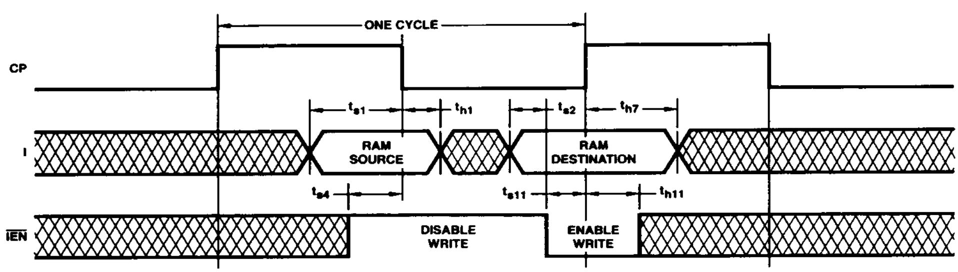
SWITCHING WAVEFORMS (Cont'd.)



WF002560

Single Address Access Timing

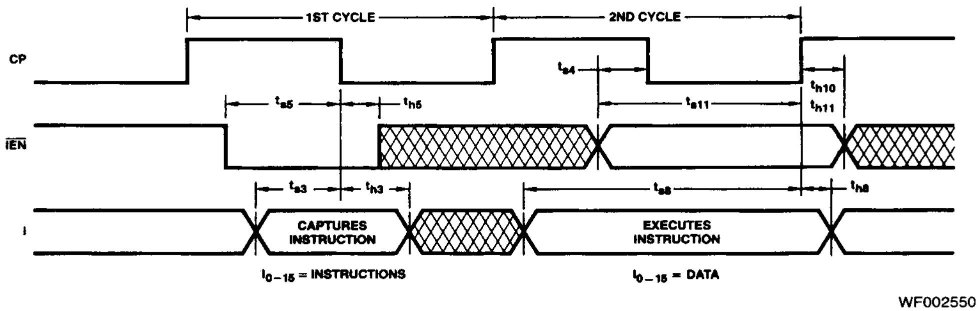
If t_{h6} is satisfied, t_{h13} need not be satisfied.



WF002540

Double Address Access Timing

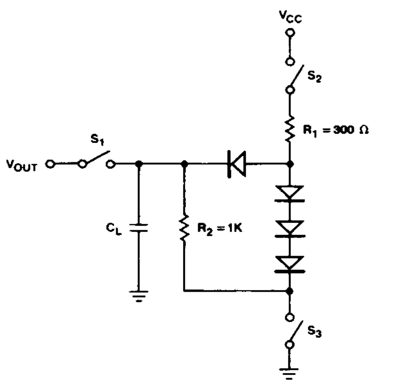
SWITCHING WAVEFORMS



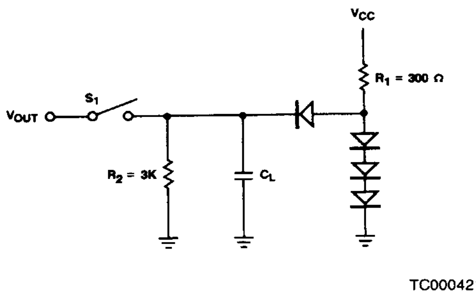
Immediate Instruction Cycle Timing

SWITCHING TEST CIRCUITS

A. THREE-STATE OUTPUTS



B. NORMAL OUTPUTS

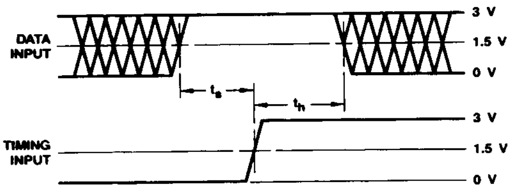


Notes: 1. $C_L = 50$ pF includes scope probe, wiring and stray capacitances without device in test fixture.

2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test. S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. $C_L = 5.0$ pF for output disable tests.

SWITCHING TEST WAVEFORMS

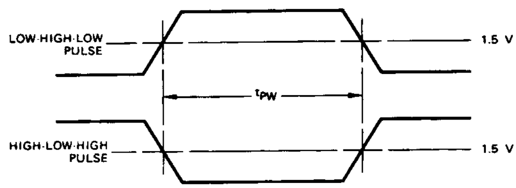
SET-UP, HOLD, AND RELEASE TIMES



WFR02970

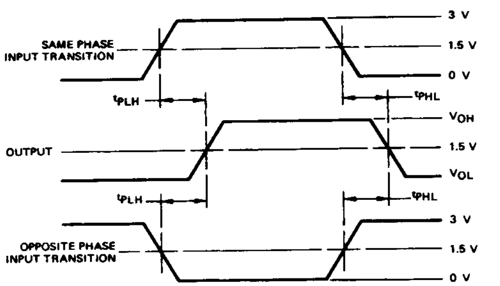
Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

PULSE WIDTH



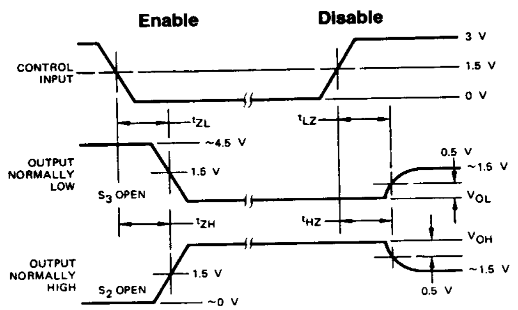
WFR02790

PROPAGATION DELAY



WFR02980

ENABLE AND DISABLE TIMES

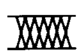
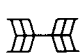


WFR02660

Notes: 1. Diagram shown for Input Control Enable-LOW and Input Control Disable-HIGH.
2. S_1, S_2 and S_3 of Load Circuit are closed except where shown.

Note: 1. Pulse Generator for All Pulses: Rate $\leqslant 1.0$ MHz; $Z_O = 50\ \Omega$; $t_r \leqslant 2.5$ ns; $t_f \leqslant 2.5$ ns.

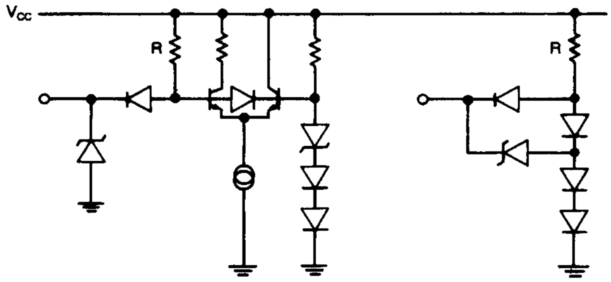
KEY TO SWITCHING WAVEFORM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010

INPUT/OUTPUT CURRENT DIAGRAMS

TTL

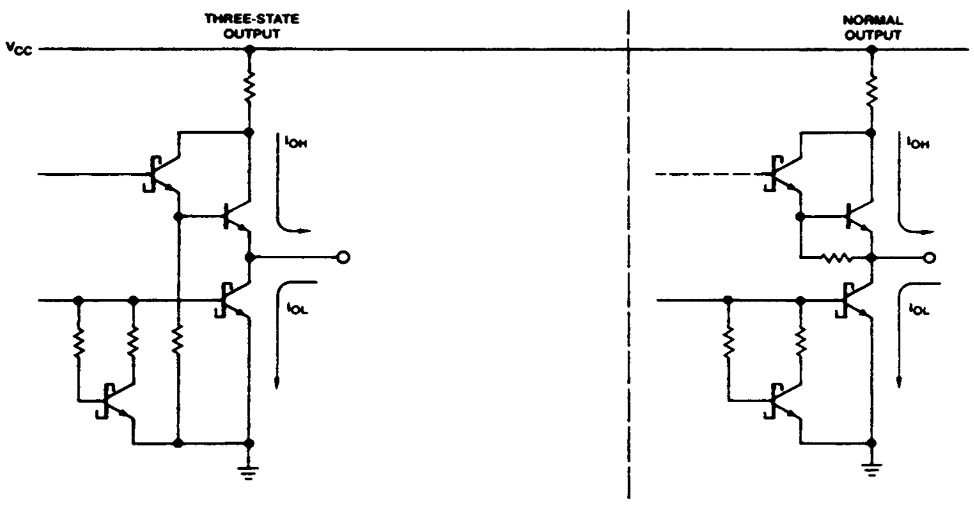


INPUT	R
$\overline{IEN}$	18K
$\overline{SRE}$	18K
DLE	9K
I_{0-4}	9K
I_{5-15}	18K
$\overline{OE}_Y$	18K
CP	6K
T_{1-4}	18K

INPUT	R
OE_T	18K

TC003062

$C_I \approx 5.0$ pF, all inputs



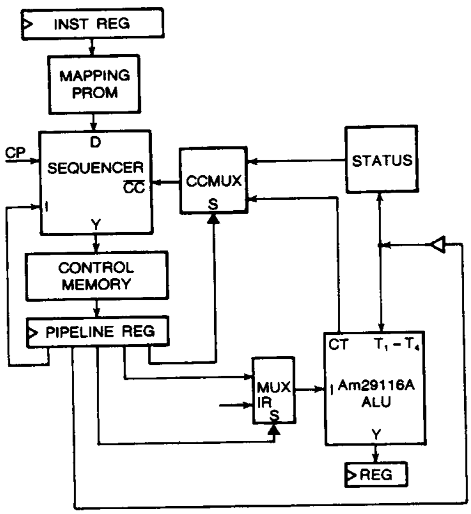
ICR00521

$C_O \approx 5.0$ pF, all outputs

Note: Actual current flow direction shown.

Am29116A System Cycle Times

SYSTEM BLOCK DIAGRAM



BD005950

DATA PATH TIMING ANALYSIS

I. Without Any External Logic

a.

Pipeline Register	(29821)	CP–Q	12 ns
RALU	(29116A)	$I\text{–}T_{1-4}$	60
Status Register	(29821)	Setup	4
Cycle Time:			**76 ns**

b.

Pipeline Register	(29821)	CP–Q	12 ns
RALU	(29116A)	I–Y	53
Data Register	(29821)	Setup	4
Cycle Time:			**69 ns**

II. With Multiplexers for Address, N-Count, etc.

a.

Pipeline Register	(29821)	CP–Q	12 ns
Multiplexer	(F157)	Sel–Y	15
RALU	(29116A)	$I\text{–}T_{1-4}$	60
Status Register	(29821)	Setup	4
Cycle Time:			**91 ns**

b.

Pipeline Register	(29821)	CP–Q	12 ns
Multiplexer	(F157)	Sel–Y	15
RALU	(29116A)	I–Y	53
Data Register	(29821)	Setup	4
Cycle Time:			**84 ns**

III. Using Y-Bus as Input/Output in One Cycle

a.

Pipeline Register	(29821)	CP–Q	12 ns
Decoder	(2924)	Sel–Y	12
Source Select	(29821)	OE–Y	15
RALU	(29116A)	$Y_{IN} - Y_{OUT}$	39
Destination	(29821)	Setup	4
Cycle Time:			**82 ns**

DLE can go LOW 6 ns (Y to DLE Setup) after data is valid on Y-bus (i.e., 45 ns after CP ↑). $\overline{OE}_Y$ should go LOW before 68 ns ($\overline{OE}_Y$ Enable is 22 ns) from CP ↑. Therefore a 50% duty cycle will work at 90 ns with DLE tied to $\overline{OE}_Y$ to CP.

CONTROL PATH TIMING ANALYSIS

				Am2910A	Am29112 (est.)	Am29331 (est.)	Type
I.	**Pipeline Register**	(29821)					Branch Map
	Mapping PROM	(27S190A)					
	Register	(29821)	CP–Q	12 ns	12	12	
	Sequencer		D–Y	20	23*	19	
	Control Memory		t_{AA}	40	40	40	
	Pipeline Register	(29821)	Setup	4	4	4	
		Cycle Time:		**76**	**79**	**75**	
II.	**Pipeline Register**	(29821)	CP–Q	12	12	12	Branch
	Buffer Enable	(2959)	OE–Y	20	20	NA	
	Sequencer		I, D–Y	20	23**	20	
	Control Memory		t_{AA}	40	40	40	
	Pipeline Register	(29821)	Setup	4	4	4	
		Cycle Time:		**96**	**99**	**76**	
III.	**Pipeline Register**	(29821)	CP–Q	12	12	12	Conditional Branch
	RALU	(29116A)	I, T–CT	29	29	29	
	CC–MUX	(2923)	D–W	7	7	NA	
	Polarity	(74S86)	D–Y	11	NA	NA	
	Sequencer		CC–Y	30	26	23	
	Control Memory		t_{AA}	40	40	40	
	Pipeline Register	(29821)	Setup	4	4	4	
		Cycle Time:		**133**	**118**	**108**	
IV.	**Pipeline Register**	(29821)	CP–Q	12	12	12	Conditional Branch Using External Status Register
	CC–MUX	(2923)	Sel–W	15	15	NA	
	Polarity	(74S86)	D–Y	11	NA	NA	
	Sequencer		CC–Y	30	26	23	
	Control Memory		t_{AA}	40	40	40	
	Pipeline Register	(29821)	Setup	4	4	4	
		Cycle Time:		**112**	**97**	**79**	
V.	**Pipeline Register**	(29821)	CP–Q	12	12	12	Instruction to Output Path
	Sequencer		I–Y	35	35*	20	
	Control Memory		t_{AA}	40	40	40	
	Pipeline Register	(29821)	Setup	4	4	4	
		Cycle Time:		**91**	**91**	**76**	
VI.	**Sequencer**		CP–Y	40	31	24	Clock to Output Path
	Control Memory		t_{AA}	40	40	40	
	Pipeline Register	(29821)	Setup	4	4	4	
		Cycle Time:		**84**	**75**	**68**	

* For the Am29112 Instruction 18 (Test SP with D (TSTSP.P)) is not used. If Instruction 18 is used D–Y is 35 ns and I–Y is 47 ns.
**For the Am29112 Relative Branch Instructions are not used. If the Relative Branch Instructions are used D–Y is 43 ns.

THE USE OF AN EXTERNAL STATUS REGISTER IN REDUCING MICROCYCLE LENGTH

The standard connection of the CT pin of the Am29116 and microcycle length calculation arising from that connection are shown below:

CRITICAL PATH TIMING (FIGURE A)

Part Number	Path	Maximum Commercial Delay (ns)
Pipeline Register	CP–Q	12
Am29116A	I, T–CT	29
Am2923 CC–MUX	D–W	7
74S86 Polarity	D–Y	11
Am2910A	CC–Y	30
Control Memory	t_{AA}	40
Pipeline Register	Setup	4
		133

While 133 ns cycle time is quite fast, it can be improved by using an external register for status testing.

CRITICAL PATH TIMING (FIGURE B)

Part Number	Path	Maximum Commercial Delay (ns)
Am29821 Status Reg	CP–Y	12
Am2923 CC–MUX	Sel–W	15
74S86 Polarity	D–Y	11
Am2910A	CC–Y	30
Control Memory	t_{AA}	40
Pipeline Register	Setup	4
		112

The cycle time has been reduced from 133 ns to 112 ns.

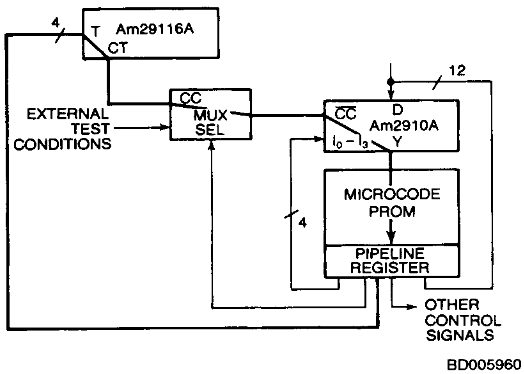


Figure A.

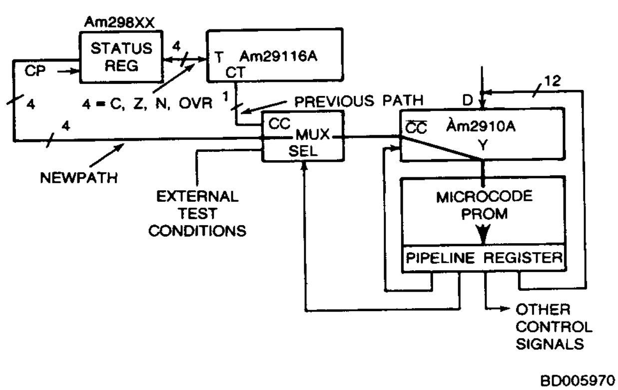
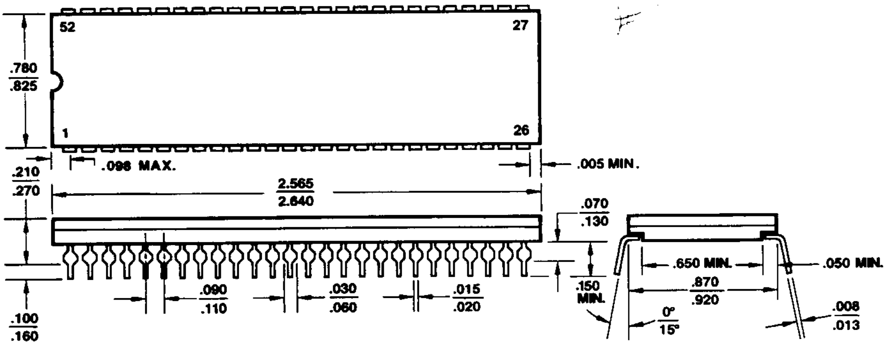


Figure B.

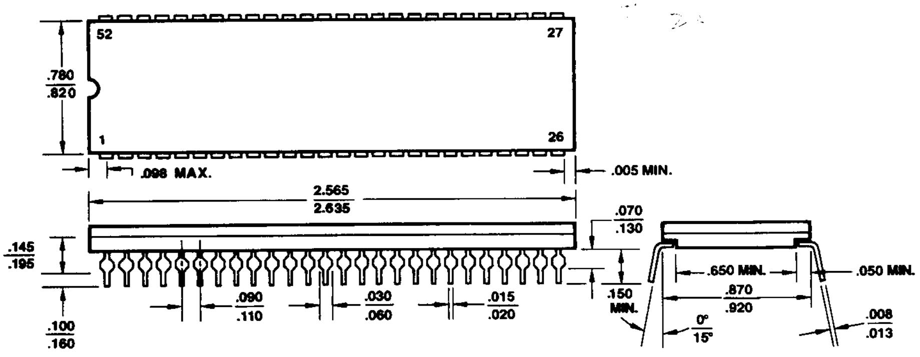
PHYSICAL DIMENSIONS (Cont'd.)

TD 052



PID # 07805A

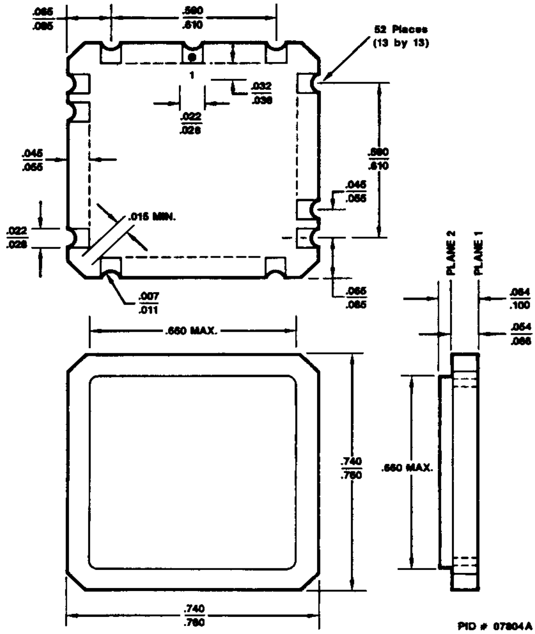
TDX052



PID # 07806A

PHYSICAL DIMENSIONS

CLT052



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