

## 8 bit 30/50 MSPS Flash A/D Converter

Evaluation Board Available — CXA1016PPCB/CXA1016KPCB  
CXA1056PPCB/CXA1056KPCB

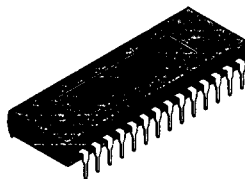
### Description

CXA1016P/CXA1016K/CXA1056P/CXA1056K are 8 bit high-speed A/D converter ICs for various applications. They can be used widely for various purposes which require high-speed A/D conversions.

CXA1016P/CXA1056P are assembled in the plastic DIP packages and CXA1016K/CXA1056K are in the ceramic lead-less chip carriers.

28 pin DIP (Plastic)

44 pin LCC (Ceramic)



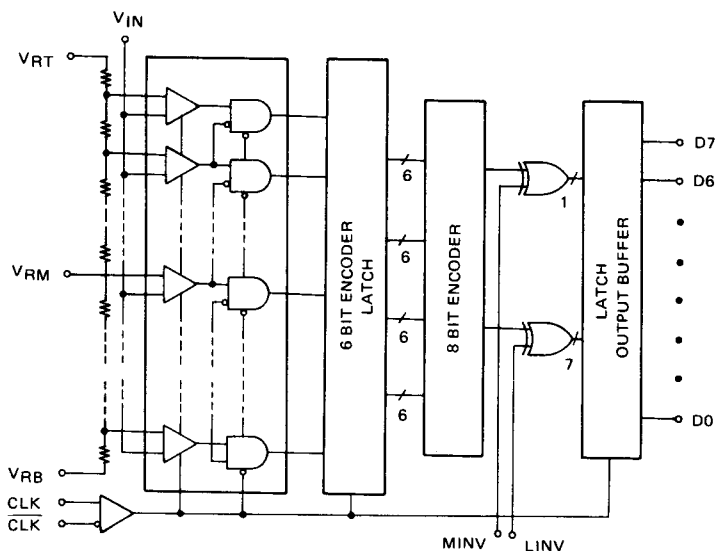
### Features (CXA1016P/CXA1016K)

- Resolution 8 bits  $\pm 1/2$  LSB
- High-speed operation Maximum conversion Rate 30 MSPS
- Wide analog input bandwidth 30MHz ( $-3$ dB)
- Low input capacitance 35 pF (typ)
- Low power consumption 420 mW (typ)

### Features (CXA1056P/CXA1056K)

- Resolution 8 bits  $\pm 1/2$  LSB
- High-speed operation Maximum conversion Rate 50 MSPS
- Wide analog input bandwidth 50MHz ( $-3$ dB)
- Low input capacitance 35 pF (typ)
- Low power consumption 550 mW (typ)

### Block Diagram



**Absolute Maximum Ratings (Ta=25°C)**

|                               |                                                     |                        |                          |
|-------------------------------|-----------------------------------------------------|------------------------|--------------------------|
| • Supply voltage              | V <sub>EE</sub>                                     | 0 to -7                | V                        |
| • Analog input voltage        | V <sub>IN</sub>                                     | 0.5 to V <sub>EE</sub> | V                        |
| • Reference input voltage     | V <sub>RT</sub> , V <sub>RB</sub> , V <sub>RM</sub> | 0.5 to V <sub>EE</sub> | V                        |
|                               | V <sub>RT</sub> -V <sub>RB</sub>                    | 2.5                    | V                        |
| • Digital input voltage       | CLK, $\overline{\text{CLK}}$ , MINV, LINV           | 0.5 to -4              | V                        |
| • VRM pin input current       | I <sub>VRM</sub>                                    | -3 to +3               | mA                       |
| • Digital output current      | ID <sub>0</sub> to ID <sub>7</sub>                  | 0 to -10               | mA                       |
| • Operating temperature       | T <sub>a</sub>                                      | -20 to +100            | °C (CXA1016P/CXA1056P)   |
|                               | T <sub>c</sub>                                      | -25 to +125            | °C (CXA1016K/CXA1056K)*1 |
| • Storage temperature         | T <sub>stg</sub>                                    | -55 to +150            | °C                       |
| • Allowable power dissipation | P <sub>D</sub>                                      | 1.48                   | W (CXA1016P/CXA1056P)    |
|                               |                                                     | 1.08                   | W (CXA1016K/CXA1056K)    |

\*1 Heat sinking is required above 100°C (CXA1016K)/86°C (CXA1056K).

**Recommended Operating Conditions (CXA1016P/CXA1016K)**

|                           |                                                           | Min.  | Typ.            | Max.            | Unit |
|---------------------------|-----------------------------------------------------------|-------|-----------------|-----------------|------|
| • Supply voltage          | A <sub>V<sub>EE</sub></sub> , D <sub>V<sub>EE</sub></sub> | -5.7  | -5.2            | -5.0            | V    |
|                           | A <sub>V<sub>EE</sub></sub> -D <sub>V<sub>EE</sub></sub>  | -0.05 | 0               | 0.05            | V    |
|                           | A <sub>GND</sub> -D <sub>GND</sub>                        | -0.05 | 0               | 0.05            | V    |
| • Reference input voltage | V <sub>RT</sub>                                           | -0.1  | 0               | 0.1             | V    |
|                           | V <sub>RB</sub>                                           | -2.2  | -2              | -1.8            | V    |
| • Analog input voltage    | V <sub>IN</sub>                                           |       | V <sub>RB</sub> | V <sub>RT</sub> |      |
| • Clock pulse width       | T <sub>pw1</sub>                                          | 25    |                 |                 | ns   |
|                           | T <sub>pw0</sub>                                          | 8     |                 |                 | ns   |

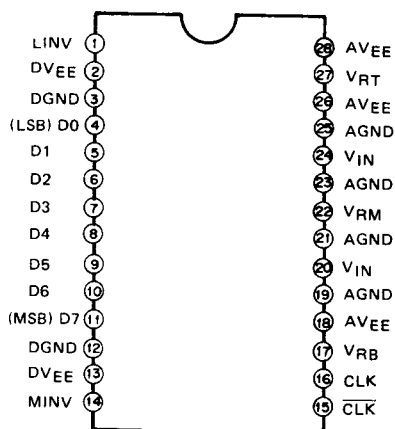
**Recommended Operating Conditions (CXA1056P/CXA1056K)**

|                           |                                                           | Min.  | Typ.            | Max.            | Unit |
|---------------------------|-----------------------------------------------------------|-------|-----------------|-----------------|------|
| • Supply voltage          | A <sub>V<sub>EE</sub></sub> , D <sub>V<sub>EE</sub></sub> | -5.7  | -5.2            | -5.0            | V    |
|                           | A <sub>V<sub>EE</sub></sub> -D <sub>V<sub>EE</sub></sub>  | -0.05 | 0               | 0.05            | V    |
|                           | A <sub>GND</sub> -D <sub>GND</sub>                        | -0.05 | 0               | 0.05            | V    |
| • Reference input voltage | V <sub>RT</sub>                                           | -0.1  | 0               | 0.1             | V    |
|                           | V <sub>RB</sub>                                           | -2.2  | -2              | -1.8            | V    |
| • Analog input voltage    | V <sub>IN</sub>                                           |       | V <sub>RB</sub> | V <sub>RT</sub> |      |
| • Clock pulse width       | T <sub>pw1</sub>                                          | 15    |                 |                 | ns   |
|                           | T <sub>pw0</sub>                                          | 5     |                 |                 | ns   |

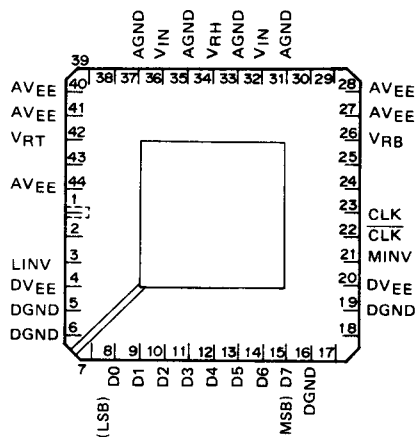
**Pin Configuration (Top View)**

The pin numbers without indication are empty pins. (not connected)

CXA1016P/CXA1056P



CXA1016K/CXA1056K



## Pin Description

| Symbol                         | Function                                                                                                                                |
|--------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| AVEE                           | Analog VEE, -5.2V (typ). Coupled with $\sim 6\Omega$ between DVEE.                                                                      |
| LINV                           | Input pin for output polarity inversion of D <sub>0</sub> (LSB)~D <sub>6</sub> . (See the code table)                                   |
| DVEE                           | Digital VEE, -5.2V (typ).                                                                                                               |
| DGND                           | Digital GND, which is separated from the Analog GND.                                                                                    |
| D <sub>0</sub> ~D <sub>7</sub> | Digital data output pin, ECL level. D <sub>0</sub> : LSB~D <sub>7</sub> : MSB.<br>Pull-down resistors are necessary externally.         |
| MINV                           | Input pin for output polarity inversion of D <sub>7</sub> (MSB) (See the code table). ECL level. "0" level is held when it is released. |
| CLK                            | Inverse clock input pin, ECL level.                                                                                                     |
| CLK                            | Clock input pin, ECL level.                                                                                                             |
| V <sub>RB</sub>                | Reference voltage (bottom), -2V (typ).                                                                                                  |
| AGND                           | Analog GND                                                                                                                              |
| V <sub>IN</sub>                | Analog input, input range is V <sub>RT</sub> ~V <sub>RB</sub>                                                                           |
| V <sub>RM</sub>                | Middle point of the reference voltage, it can be used as a linearity correction pin.                                                    |
| V <sub>RT</sub>                | Reference voltage (top), 0V (typ).                                                                                                      |
|                                | Empty pins (not connected), 2 and 19 are used to be grounded to DGND, the others are used to be grounded to AGND.                       |

## Output Coding

| MINV<br>LINV    | 0<br>0     | 0<br>1     | 1<br>0     | 1<br>1     |
|-----------------|------------|------------|------------|------------|
| 0V              | 111 ... 11 | 100 ... 00 | 011 ... 11 | 000 ... 00 |
| .               | 111 ... 10 | 100 ... 01 | 011 ... 10 | 000 ... 01 |
| .               | .          | .          | .          | .          |
| .               | .          | .          | .          | .          |
| .               | .          | .          | .          | .          |
| V <sub>IN</sub> | 100 ... 00 | 111 ... 11 | 000 ... 00 | 011 ... 11 |
| .               | 011 ... 11 | 000 ... 00 | 111 ... 11 | 100 ... 00 |
| .               | .          | .          | .          | .          |
| .               | .          | .          | .          | .          |
| .               | .          | .          | .          | .          |
| .               | 000 ... 01 | 011 ... 10 | 100 ... 01 | 111 ... 10 |
| -2V             | 000 ... 00 | 011 ... 11 | 100 ... 00 | 111 ... 11 |

1: V<sub>IH</sub>, V<sub>OH</sub>0: V<sub>IL</sub>, V<sub>OL</sub>

## Electrical Characteristics (CXA1016P/CXA1016K)

(Ta=25°C, VEE=-5.2V, VRT=0V, VRB=-2V)

| Item                             | Symbol       | Condition                                         | Min.  | Typ.  | Max. | Unit |
|----------------------------------|--------------|---------------------------------------------------|-------|-------|------|------|
| Maximum Conversion Rate          | Fc           | VIN=0 to -2V,<br>fin=1 kHz, ramp                  | 30    |       |      | MSPS |
| Supply Current                   | IEE          |                                                   |       | -75   | -100 | mA   |
| Analog Input Capacitance         | CIN          | VIN=-1V+0.07 Vrms                                 |       | 35    | 40   | pF   |
| Analog Input Bias Current        | IIN          | VIN=-1V                                           |       | 60    | 90   | μA   |
| Reference Resistor               | Rr (VRT~VRB) |                                                   | 70    | 80    | 100  | Ω    |
| Offset Voltage                   | VRT          |                                                   | 7     | 9     | 11   | mV   |
|                                  | VRB          |                                                   | 15    | 17    | 19   | mV   |
| Digital Input Voltage            | VIH          |                                                   | -1.0  | -0.9  | -0.7 | V    |
|                                  | VIL          |                                                   | -1.9  | -1.75 | -1.6 | V    |
| Digital Input Current            | IiH          | VIH=-0.9V                                         | 0     |       | 0.4  | mA   |
|                                  | IiL          | VIL=-1.75V                                        | -0.05 |       | 0.35 | mA   |
| Digital Output Voltage           | VOH          | RL=620Ω ~ VEE                                     | -1.0  |       |      | V    |
|                                  | VOL          |                                                   |       |       | -1.6 | V    |
| Output Data Delay                | Td           | RL=620Ω ~ VEE                                     |       | 4.0   | 5.0  | ns   |
| Non-linearity Error              |              | Fc = 30 MSPS,<br>VIN=0 to -2V,<br>fin=1 kHz, ramp |       |       | ±1/2 | LSB  |
| Differential Non-linearity Error |              | Fc = 30 MSPS                                      |       |       | ±1/2 | LSB  |
| Differential Gain                | DG           | NTSC 40 IRE mod.<br>ramp, Fc = 30 MSPS            |       |       | 1.5. | %    |
| Differential Phase               | DP           |                                                   |       |       | 0.5  | deg. |
| Aperture Jitter                  | Taj          |                                                   |       | 45    |      | ps   |
| Sampling Delay                   | Tsd          |                                                   | 6.3   | 6.8   | 7.3  | ns   |
| Full scale input BW (-3dB)       | BWf          | *1                                                |       | 30    |      | MHz  |

\*1 Source impedance = 50 Ω

Without a buffer amplifier driving A/D input

## Electrical Characteristics (CXA1056P/CXA1056K)

(Ta=25°C, VEE=−5.2V, VRT=0V, VRB=−2V)

| Item                             | Symbol       | Condition                                         | Min.  | Typ.  | Max. | Unit |
|----------------------------------|--------------|---------------------------------------------------|-------|-------|------|------|
| Maximum Conversion Rate          | Fc           | VIN=0 to −2V,<br>fin=1 kHz, ramp                  | 50    |       |      | MSPS |
| Supply Current                   | IEE          |                                                   |       | −95   | −120 | mA   |
| Analog Input Capacitance         | CIN          | VIN=−1V+0.07 Vrms                                 |       | 35    | 40   | pF   |
| Analog Input Bias Current        | IIN          | VIN=−1V                                           |       | 75    | 115  | μA   |
| Reference Resistor               | Rr (VRT~VRB) |                                                   | 70    | 80    | 100  | Ω    |
| Offset Voltage                   | VRT          |                                                   | 7     | 9     | 11   | mV   |
|                                  | VRB          |                                                   | 15    | 17    | 19   | mV   |
| Digital Input Voltage            | VIH          |                                                   | −1.0  | −0.9  | −0.7 | V    |
|                                  | VIL          |                                                   | −1.9  | −1.75 | −1.6 | V    |
| Digital Input Current            | IiH          | VIH=−0.9V                                         | 0     |       | 0.4  | mA   |
|                                  | IiL          | VIL=−1.75V                                        | −0.05 |       | 0.35 | mA   |
| Digital Output Voltage           | VOH          | Rℓ=620Ω ~ VEE                                     | −1.0  |       |      | V    |
|                                  | VOL          |                                                   |       |       | −1.6 | V    |
| Output Data Delay                | Td           | Rℓ=620Ω ~ VEE                                     |       | 4.0   | 5.0  | ns   |
| Non-linearity Error              |              | Fc = 50 MSPS,<br>VIN=0 to −2V,<br>fin=1 kHz, ramp |       |       | ±1/2 | LSB  |
| Differential Non-linearity Error |              | Fc = 50 MSPS                                      |       |       | ±1/2 | LSB  |
| Differential Gain                | DG           | NTSC 40 IRE mod.<br>ramp, Fc = 50 MSPS            |       |       | 1.5  | %    |
| Differential Phase               | DP           |                                                   |       |       | 0.5  | deg. |
| Aperture Jitter                  | Taj          |                                                   |       | 30    |      | ps   |
| Sampling Delay                   | Tsd          |                                                   | 5.4   | 5.7   | 6.0  | ns   |
| Full scale input BW (−3dB)       | BWF          | *1                                                |       | 50    |      | MHz  |

\*1 Source impedance = 50 Ω

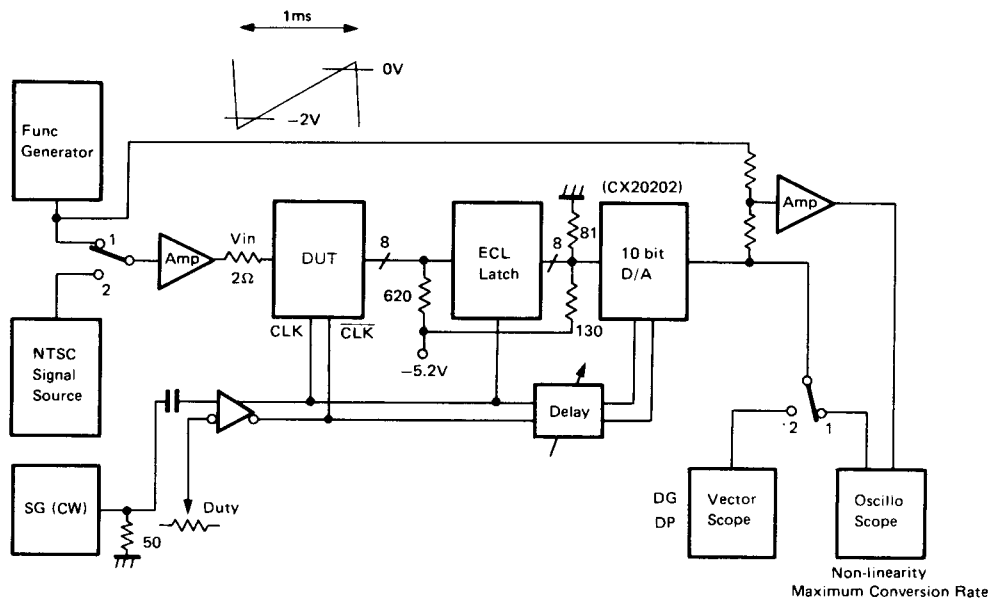
Without a buffer amplifier driving A/D input

# Electrical Characteristics Test Circuit

## Maximum Conversion Frequency Test Circuit

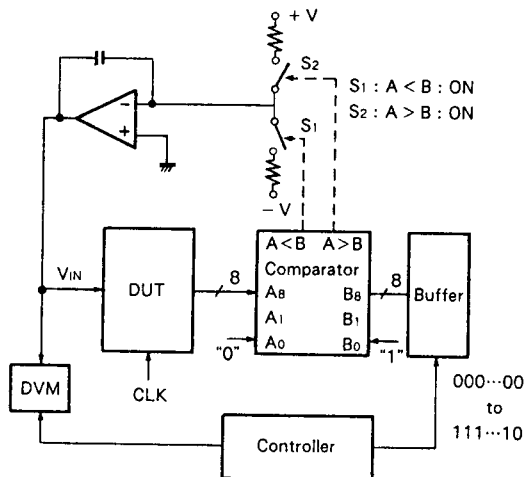
## Differential Gain Error Test Circuit

## Differential Phase Error Test Circuit



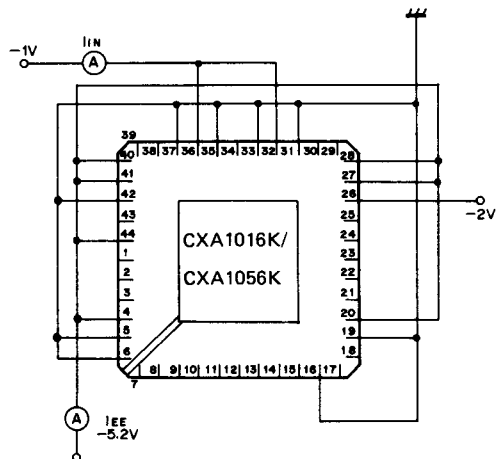
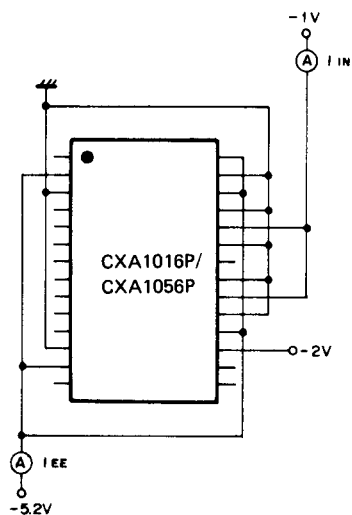
## Differential Non-linearity Test Circuit

## Integral Non-linearity Test Circuit

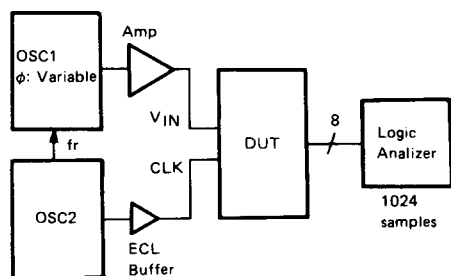


### Power Supply Current Test Circuit

### Analog Input Bias Current Test Circuit



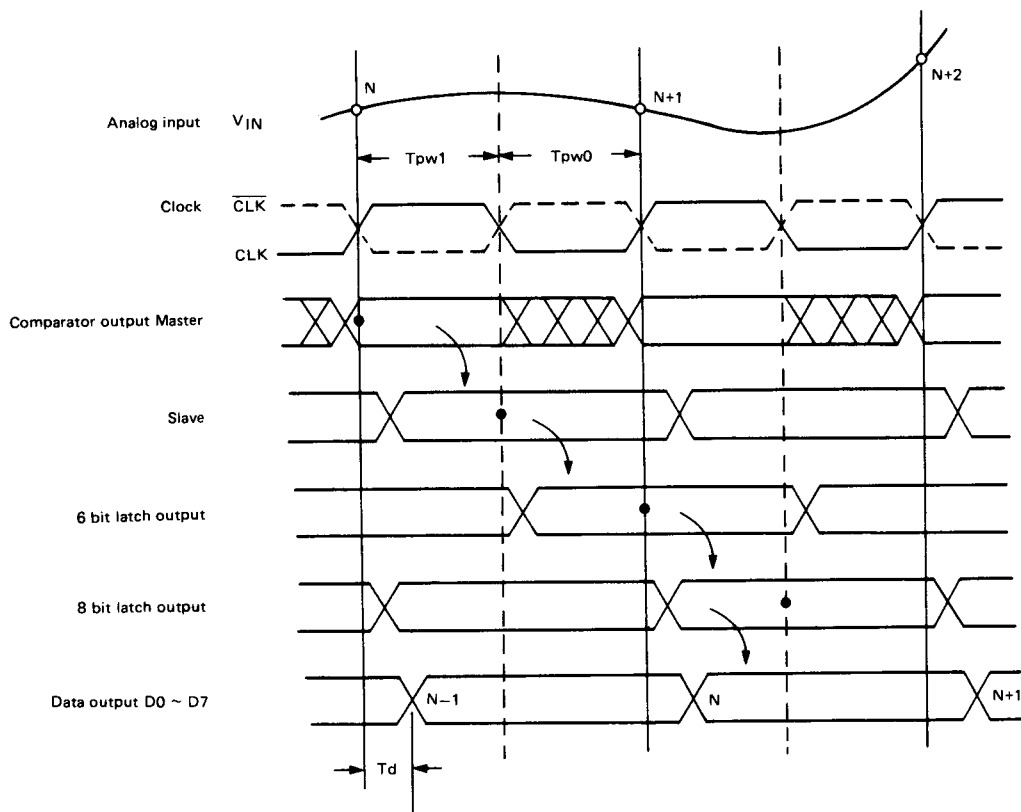
### Aperture Jitter Test Circuit



**Description of Function** (See the block diagram and timing chart.)

1. The reference voltage, which is obtained by dividing equally the voltage across  $V_{RT}$  to  $V_{RB}$  into 256 by the reference resistor ladder, is applied to the respective  $\oplus$  (positive) input sides of 256 clocked comparators. An analog input is applied to the  $\ominus$  (negative) input sides of all the 256 clocked comparators from the  $V_{IN}$  pin.
2. When the state of CLK is in Low, the master (front stage) of the comparator compares the respective reference voltage and the analog input voltage which is ever-changing.
3. When the CLK moves from Low into Hi, each master latches the state immediately prior to the above simultaneously, and as a result, it provides conditions of "11 . . . . 1100 . . 0" in sequence from the  $V_{RT}$  side to the  $V_{RB}$  side.
4. The output of the master is ANDed between the respective adjacent outputs, and "1" stands only when neighboring 2 outputs become "10", and the all other outputs become "0".
5. The result of the AND is latched when CLK moves from Hi into Low. Output of the slave is divided into 4 blocks and each block has 32 clocked comparators, and they are coded into binary codes of 6 bits respectively by the transistor matrix circuit.
6. The 6 bit codes are further coded into 8 bit codes by the transistor matrix circuit after they are respectively latched, and they are then output into the ECL level by the output buffer after being 8 bit latched. The output data is delayed 1 clock from the data sampling point and appears at the output pin.
7. Two polarity inversion inputs such as MINV and LINV are fed externally to the output buffer, and each of them selects output polarity of MSB and other polarity than MSB respectively.

## Timing Chart

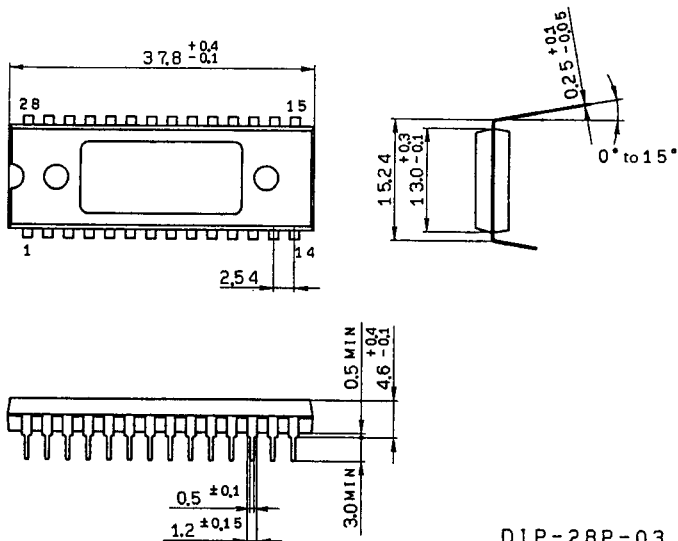


Dots (•) in the chart denote respective latch timings.

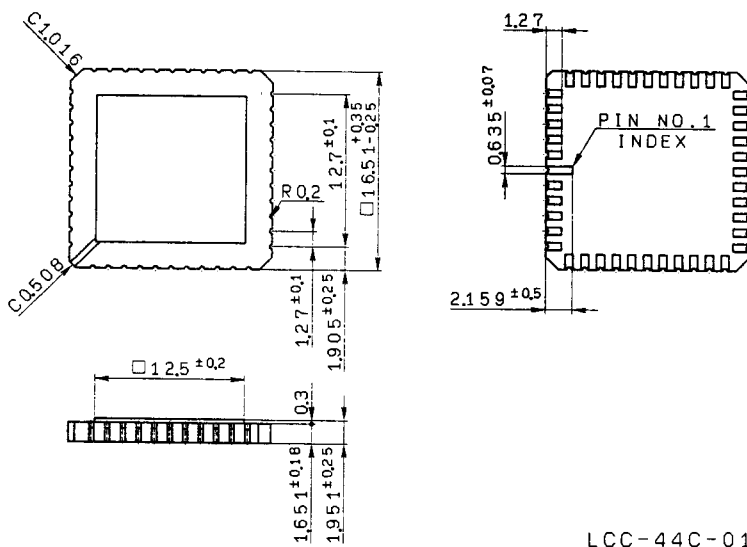
\*See page 54 for  $T_{pw1}$  and  $T_{pw0}$ .

## Package Outline Unit: mm

CXA1016P/CXA1056P 28 pin DIP (Plastic)



CXA1016K/CXA1056K 44 pin LCC (Ceramic)



## Sony Package Product Name

T-90-20

| Type            | Package name                      |                 | Package                            | Features  |                                      |                   |                         |
|-----------------|-----------------------------------|-----------------|------------------------------------|-----------|--------------------------------------|-------------------|-------------------------|
|                 | Symbol                            | Description     |                                    | Material* | Lead pitch                           | Lead shape        | Lead pull out direction |
| Inserted        | Standard                          | DIP             | DUAL IN LINE PACKAGE               | P<br>C    | 2.54mm<br>(100MIL)                   | Through Hole Lead | 2-direction             |
|                 |                                   | SIP             | SINGLE IN LINE PACKAGE             | P         | 2.54mm<br>(100MIL)                   | Through Hole Lead | 1-direction             |
|                 |                                   | ZIP             | ZIG ZAG IN LINE PACKAGE            | P         | 2.54mm<br>(100MIL)<br>Zig Zag inline | Through Hole Lead | 1-direction             |
|                 |                                   | PGA             | PIN GRID ARRAY                     | C         | 2.54mm<br>(100MIL)                   | Through Hole Lead | 4-direction             |
|                 |                                   | PIGGY BACK      | PIGGY BACK                         | C         | 2.54mm<br>(100MIL)                   | Through Hole Lead | 2-direction             |
|                 | Shrink                            | SDIP            | SHRINK DUAL IN LINE PACKAGE        | P         | 1.778mm<br>(70MIL)                   | Through Hole Lead | 2-direction             |
| Surface mounted | Standard flat package             | QFP             | QUAD FLAT PACKAGE                  | P         | 1.0mm<br>0.8mm                       | Gull-Wing         | 4-direction             |
|                 |                                   | SOP             | SMALL OUTLINE PACKAGE              | P         | 1.27mm<br>(50MIL)                    | Gull-Wing         | 2-direction             |
|                 | Shrink flat package               | VQFP            | VERY SMALL QUAD FLAT PACKAGE       | P         | 0.5mm                                | Gull-Wing         | 4-direction             |
|                 |                                   | VSOP            | VERY SMALL OUTLINE PACKAGE         | P         | 0.65mm                               | Gull Wing         | 2-direction             |
|                 | Standard chip carrier             | PLCC            | PLASTIC LEADED CHIP CARRIER        | P         | 1.27mm<br>(50MIL)                    | J-bend            | 4-direction             |
|                 |                                   | LCC             | LEAD LESS CHIP CARRIER             | C         | 1.27mm<br>(50MIL)                    | Lead less         | Package side            |
|                 | Shrink chip carrier               | SPLCC<br>(PLCC) | SHRINK PLASTIC LEADED CHIP CARRIER | P         | 1.27mm Max.<br>(50MIL Max.)          | J-bend            | 4-direction             |
|                 | Standard 2-direction chip carrier | SOJ             | SMALL OUTLINE J-LEAD PACKAGE       | P         | 1.27mm<br>(50MIL)                    | J-bend            | 2-direction             |

\*P.....Plastic, C.....Ceramic