



CYPRESS
SEMICONDUCTOR

CY10E301
CY100E301

Combinatorial ECL 16P8 Programmable Logic Device

Features

- Standard 16P8 pinout and architecture
 - 16 inputs, 8 outputs
 - User-programmable output polarity
- Ultra high speed/standard power
 - $t_{PD} = 4 \text{ ns (max.)}$
 - $I_{EE} = 240 \text{ mA (max.)}$
- Low-power version
 - $t_{PD} = 6 \text{ ns (max.)}$
 - $I_{EE} = 170 \text{ mA (max.)}$
- Both 10KH- and 100K-compatible I/O versions available
- Enhanced test features
 - Additional test input terms
 - Additional test product terms
- Security fuse

Functional Description

Cypress Semiconductor's PLD family offers the user the highest level of performance in ECL programmable logic devices. These PLDs are developed using an advanced STAR[®] bipolar process incorporating proven Ti-W fuses.

The CY10E301 is 10KH-compatible and the CY100E301 is 100K-compatible. These PLDs implement the familiar sum-of-products logic functions by selectively programming cell elements to configure the AND gates by disconnecting either the true or the complement input term. If all inputs are disconnected from an AND gate, then a logical true will exist at the output of this AND gate. An output polarity fuse is also provided to allow an active LOW

to occur if this fuse is blown. A security feature provides the user protection for the implementation of proprietary logic. When invoked by blowing the security fuse, the contents of the array cannot be accessed in the verify mode.

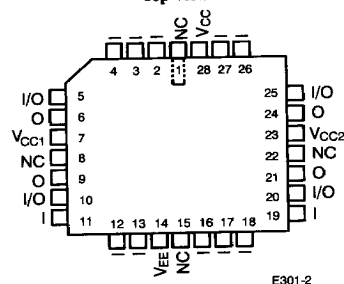
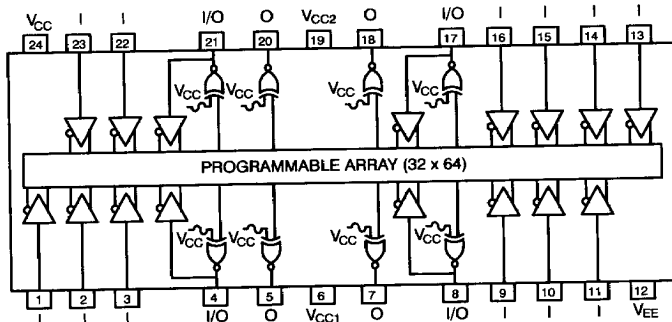
The CY10E301 and CY100E301 can be programmed using Cypress's QuickPro II or other industry-standard programming equipment. Programming support information can be obtained from local Cypress Semiconductor sales offices.

Logic Block Diagram

Pin Configuration

PDIP/CerDIP
Top View

PLCC/CLCC
Top View



E301-2

E301-1

Selection Guide

		10E301-4 100E301-4	10E301-5	10E301L-6 100E301L-6
Maximum Input to Output Propagation Delay Time (ns)		4	5	6
I_{EE} (mA)	Commercial	-240		-170
	Military		-240	

STAR is a trademark of Aspen Semiconductor.

Maximum Ratings

(Above which the useful life may be impaired. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability. For user guidelines, not tested.)

Storage Temperature	– 65°C to +150°C
Ambient Temperature with Power Applied	– 55°C to +125°C
Supply Voltage V_{EE} to V_{CC}	–7.0V to +0.5V
Input Voltage	V_{EE} to +0.5V
Output Current	–50 mA

Operating Range Referenced to V_{CC} at Ground

Range	Version	Temperature	V_{CC}
Commercial (Standard, L)	10E	0°C to +75°C Ambient	–5.2V $\pm$ 5%
Commercial (Standard, L)	100E	0°C to +85°C Ambient	–4.5V $\pm$ 0.3V
Military	10E	–55°C to +125°C Case	–5.2V $\pm$ 5%

Electrical Characteristics Over the Operating Range^[1]

Parameters	Description	Test Conditions	Temperature ^[2]	10E301		100E301		Units
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	10KH, $R_L = 50\Omega$ to –2V, $V_{IN} = V_{IH}$ Min. or V_{IL} Max.	$T_C = -55^\circ\text{C}$	–1140	–920			mV
			$T_A = 0^\circ\text{C}$	–1020	–840			mV
			$T_A = +25^\circ\text{C}$	–980	–810			mV
			$T_A = +75^\circ\text{C}$	–920	–735			mV
			$T_C = +125^\circ\text{C}$	–900	–700			mV
		100K, $R_L = 50\Omega$ to –2V, $V_{IN} = V_{IH}$ Min. or V_{IL} Max.	$T_A = 0^\circ\text{C}$ to 85°C			–1025	–880	mV
V_{OL}	Output LOW Voltage	10KH, $R_L = 50\Omega$ to –2V, $V_{IN} = V_{IH}$ Min. or V_{IL} Max.	$T_C = -55^\circ\text{C}$	–1950	–1650			mV
			$T_A = 0^\circ\text{C}$	–1950	–1630			mV
			$T_A = +25^\circ\text{C}$	–1950	–1630			mV
			$T_A = +75^\circ\text{C}$	–1950	–1600			mV
			$T_C = +125^\circ\text{C}$	–1950	–1590			mV
		100K, $R_L = 50\Omega$ to –2V, $V_{IN} = V_{IH}$ Min. or V_{IL} Max.	$T_A = 0^\circ\text{C}$ to 85°C			–1810	–1620	mV
V_{IH}	Input HIGH Voltage	10KH	$T_C = -55^\circ\text{C}$	–1270	–920			mV
			$T_A = 0^\circ\text{C}$	–1170	–840			mV
			$T_A = +25^\circ\text{C}$	–1130	–810			mV
			$T_A = +75^\circ\text{C}$	–1070	–735			mV
			$T_C = +125^\circ\text{C}$	–1050	–700			mV
		100K	$T_A = 0^\circ\text{C}$ to 85°C			–1165	–880	mV
V_{IL}	Input LOW Voltage Supply Current (All inputs and outputs open)	10KH	$T_C = -55^\circ\text{C}$	–1950	–1520			mV
			$T_A = 0^\circ\text{C}$	–1950	–1480			mV
			$T_A = +25^\circ\text{C}$	–1950	–1480			mV
			$T_A = +75^\circ\text{C}$	–1950	–1450			mV
			$T_C = +125^\circ\text{C}$	–1950	–1440			mV
		100K	$T_A = 0^\circ\text{C}$ to 85°C			–1810	–1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IH}$ Max.			220		220	μA
I_{IL}	Input LOW Current	$V_{IN} = V_{IL}$ Min. (Except I/O Pins)		0.5		0.5		μA
I_{EE}		Commercial L (Low Power)		–170		–170		mA
		Commercial (Standard Power)		–240		–240		mA
		Military		–240				mA

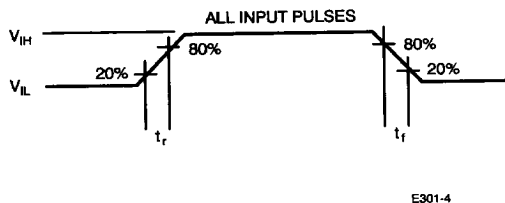
Notes:

1. See AC Test Loads and Waveforms for test conditions.

2. Commercial grade is specified as ambient temperature with transverse air flow greater than 500 linear feet per minute. Military grade is specified as case temperature.



Parameters	Description	Min.	Typ.	Max.	Units
C _{IN}	Input Capacitance		4	8	pF
C _{OUT}	Output Capacitance		6	10	pF



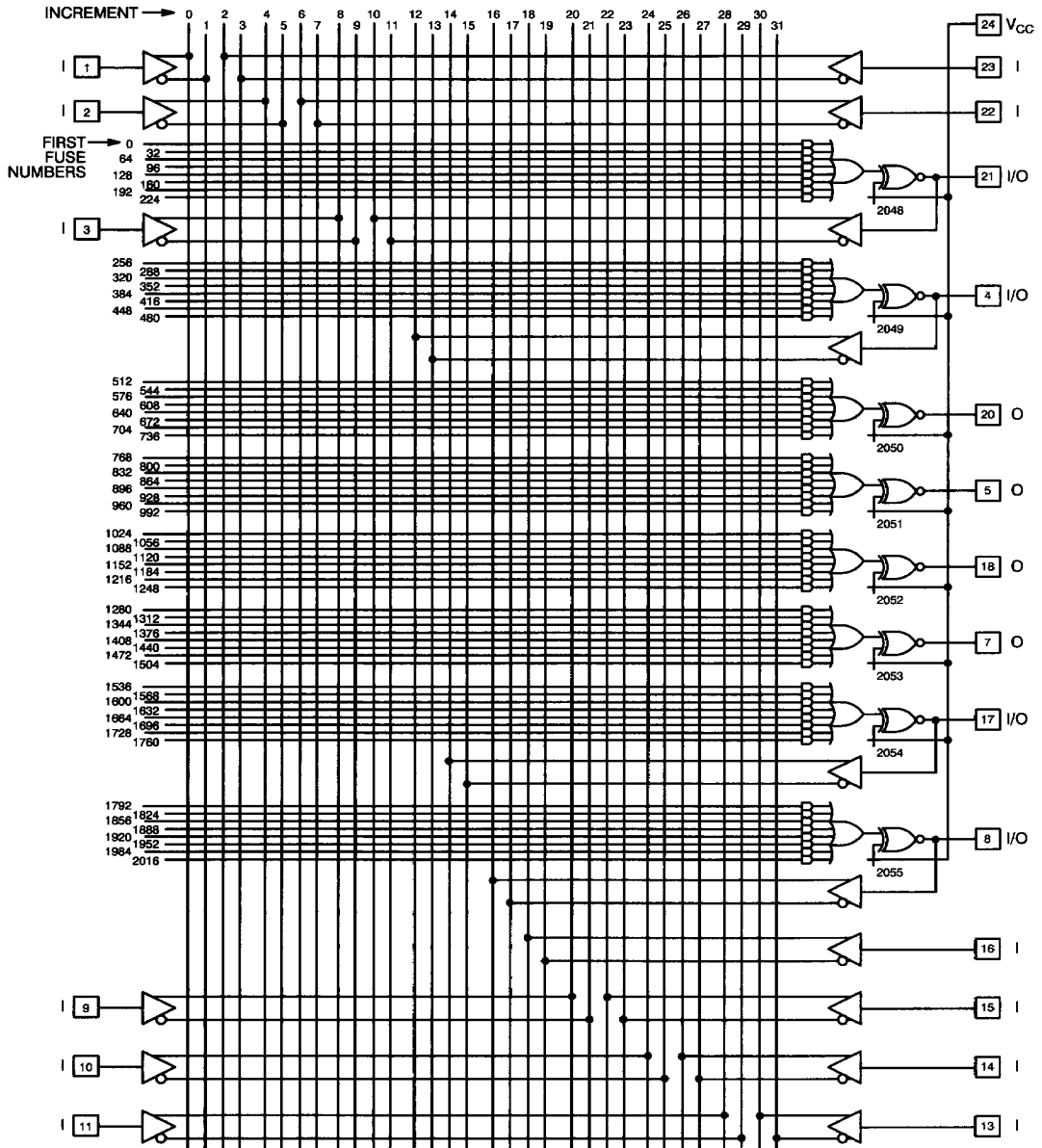
Notes:

3. Tested initially and after any design or process changes that may affect these parameters.
4. $V_{IL} = V_{IL} \text{ Min.}$, $V_{IH} = V_{IH} \text{ Max.}$ on 10E version.
5. $V_{IL} = -1.7V$, $V_{IH} = -0.9V$ on 100E version
6. $R_L = 50\Omega$, $C < 5 \text{ pF}$ (includes fixture and stray capacitance).
7. All coaxial cables should be 50Ω with equal lengths. The delay of the coaxial cables should be "nulled" out of the measurement.
8. $t_r = t_f = 0.7 \text{ ns}$
9. All timing measurements are made from the 50% point of all waveforms.

Parameters	Description	10E301-4 100E301-4		10E301-5		10E301L-6 100E301L-6		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{PD}	Input to Output Propagation Delay		4.0		5.0		6.0	ns
t _r	Output Rise Time	0.35	1.5	0.35	1.5	0.35	1.5	ns
t _f	Output Fall Time	0.35	1.5	0.35	1.5	0.35	1.5	ns

The diagram illustrates the propagation delay t_{PD} of a CMOS inverter. The **INPUT** signal transitions from a high level V_{IH} to a low level V_{IL} . The **OUTPUT** signal, which was previously at a high level V_{OH} , transitions to a low level V_{OL} after a time delay t_{PD} . The delay is measured from the midpoint of the input transition to the midpoint of the output transition.

Functional Logic Diagram (DIP Pinout)



JEDEC fuse number = first fuse number + increment

E301-6

Ordering Information

I/O	t _{PD} (ns)	I _{EE} (mA)	Ordering Code	Package Type	Operating Range
10KH	4	240	CY10E301-4DC	D14	Commercial
			CY10E301-4YC	Y64	
	5	240	CY10E301-5DMB	D14	Military
			CY10E301-5YMB	Y64	
	6	170	CY10E301L-6JC	J64	Commercial
			CY10E301L-6PC	P13A	
100K	4	240	CY100E301-4DC	D14	Commercial
			CY100E301-4YC	Y64	
	6	170	CY100E301L-6JC	J64	Commercial
			CY100E301L-6PC	P13A	

Document #: 32-A-00011-B