INCH-POUND

MIL-M-38510/240A
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SUPERSEDING
MIL-M-38510/240(USAF)
15 November 1978

MILITARY SPECIFICATION

MICROCIRCUITS, MEMORY, DIGITAL, NMOS, 16,384 BIT DYNAMIC RANDOM ACCESS MEMORY (DRAM), MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, N-channel dynamic NMOS 16,384/1-bit random access memory microcircuits. Two product assurance classes (S and B) and a choice of case outlines and lead finishes are provided and are reflected in the complete Part or Identifying Number (PIN) (see 6.7).

1.2 Classification.

1.2.1 Device type. The device type shall be as shown in the following:

Device type	Circuit organization	Access time
01,04 (T_{case} = -55°C instant on to +110°C operating)	16,384/1-bit RAM	200 ns
02,05 (T_{case} = -55°C instant on to +110°C operating)	16,384/1-bit RAM	250 ns
03 (T_{case} = -55°C instant on to +110°C operating)	16,384/1-bit RAM	200 ns (page mode operation guaranteed)

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline shall be designated as follows:

Case outline	MIL-M-38510, appendix C, case outline
E	D-2 (16-lead, .840" x .310" x .200"), dual-in-line package
F	F-5 (16-lead, .390" x .260" x .085"), flat package
Z	See figure 1 (18-lead, .360" x .240" x .048"), leadless chip carrier package

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center, RBE-2, Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

AMSC N/A FSC 5962

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1.3 Absolute maximum ratings:

Voltage on any pin relative to substrate:	
Device types 01 through 03	-0.3 V to +20 V
Device types 04 and 05	-1.0 V to +7 V
Power dissipation (minimum cycle time)	1.0 W maximum
Thermal resistance (minimum cycle time)	θ_{JC} = 15°C/W maximum
Voltage on V_{DD} relative to V_{SS}:	
Device types 01 through 03 only	-1.0 V to +16 V
Voltage on V_{CC} relative to V_{SS}:	
Device types 01 through 03	-1.0 V to +15 V
Device types 04 and 05	-1.0 V to +7 V
V_{BB} - V_{SS} (V_{DD} - V_{SS} > 0)	
Device types 01 through 03	-0.3 V maximum
Lead temperature (soldering, 5 seconds)	270°C maximum
Maximum junction temperature, T_J	150°C

1.3.1 Alpha particle induced error rate. The error rate shall not exceed 1 error in 5 x 10^6 device operating hours, under the following test conditions:

a. Nominal power supplies.

b. T_C = 25°C.

c. Device in a checkerboard pattern.

d. Cycle time equal to 375 ns.

1.4 Recommended operating conditions:

	Min	Max	Unit
Supply voltages:			
V_{DD} (device types 01 through 03)	10.8	16	V dc
V_{BB} (device types 01 through 03)	-4.5	-7	V dc
V_{CC}	4.5	5.5	V dc
V_{SS}	0 1/	0 1/	V dc
High level input voltages:			
Addresses (V_{IH}):			
Device types 01 through 03	2.4	7.0	V dc
Device types 04 and 05	2.4	6.5	V dc
Clocks (V_{IHC}):			
Device types 01 through 03	2.7	7.0	V dc
Device types 04 and 05	2.7	6.5	V dc
Data In (V_{IH}):			
Device types 01 through 03	2.4	7.0	V dc
Device types 04 and 05	2.4	6.5	V dc
Low level input voltage:			
All inputs (V_{IL})	-1.0	0.8	V dc
Refresh cycle time (t_{REF})		1.0	ms
Operating case temperature	-55	+110	°C

1/ V_{SS} is common for all supplies.

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Unless otherwise indicated, copies of federal and military specifications, standards, and handbooks are available from the Naval Publications and Forms Center, (ATTN: NPODS), 5801 Tabor Avenue, Philadelphia, PA 19120-5099.)

2.2 Order of precedence. In the event of a conflict between the text of this document and the references cited herein (except for related associated detail specifications, specification sheets, or MS standards), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Detail specifications. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510, and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.2 Functional block diagram. The functional block diagram shall be as specified on figure 3. Upon implementing design changes, the manufacturer must submit a new block diagram to the qualifying activity for inclusion in this specification. The block diagram shall clearly define the row address inputs and the column address inputs.

3.2.3 Schematic circuits and bit address maps. Schematic circuits and bit maps shall be submitted to the qualifying activity as a prerequisite for qualification. All manufacturers' schematics and bit maps shall be maintained and available upon request.

3.2.3.1 Truth table. The truth table shall be as specified on figure 4.

3.2.3.2 Functional tests. The functional tests used to test these devices are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, then alternate test patterns to accomplish the same results shall be submitted to the qualifying activity for approval.

TABLE I. Electrical performance characteristics.

Characteristics	Symbol	Conditions $-55^\circ C \leq T_C \leq +110^\circ C$ $V_{SS} = 0$ V 4.5 V dc $\leq V_{CC} \leq$ 5.5 V dc unless otherwise specified		Device types	Limits		Unit
					Min	Max	
Output high voltage	V_{OH}	I_{OH} = -5.0 mA, V_{CC} = 4.5 V		All	2.4		V
Output low voltage	V_{OL}	I_{OL} = 4.2 mA, V_{CC} = 4.5 V		All		0.4	V
Input leakage All inputs	$I_{I(L)(H)}$	V_{IN} = 0 to 7.0 V		All	-10	+10	µA
		V_{IN} = 0 to 6.5 V for devices 04 and 05					
Output leakage	$I_{O(L)(H)}$	$\overline{RAS}$ and $\overline{CAS}$ = V_{IHC} V_{OUT} = 0.0 to 5.5 V		All	-10	+10	µA
Supply current from V_{DD}	I_{DD1} 1/	$\overline{RAS}$ and $\overline{CAS}$ cycling	t_{RC} = 375 ns	01,03		35	mA
			t_{RC} = 410 ns	02			
	I_{DD2}	$\overline{RAS}$ and $\overline{CAS}$ = V_{IHC} D_{OUT} = High Z		01,02,03		2.25	mA
	I_{DD3} 1/	$\overline{RAS}$ cycling $\overline{CAS}$ = V_{IHC}	t_{RC} = 375 ns	01,03		27	mA
			t_{RC} = 410 ns	02			
	I_{DD4} 1/	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling	t_{PC} = 225 ns	01,03		27	mA
			t_{PC} = 275 ns	02			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Characteristics	Symbol	Conditions $-55^\circ C \leq T_C \leq +110^\circ C$ $V_{SS} = 0$ V 4.5 V dc $\leq V_{CC} \leq$ 5.5 V dc unless otherwise specified		Device types	Limits		Unit
					Min	Max	
Supply current from V_{BB}	I_{BB1} 1/	$\overline{RAS}$ and $\overline{CAS}$ cycling	t_{RC} = 375 ns	01,03		400	µA
			t_{RC} = 410 ns	02			
	I_{BB2}	$\overline{RAS}$ and $\overline{CAS}$ = V_{IHC} D_{OUT} = High Z		01,02,03		200	µA
	I_{BB3} 1/	$\overline{RAS}$ cycling $\overline{CAS}$ = V_{IHC}	t_{RC} = 375 ns	01,03		400	µA
			t_{RC} = 410 ns	02			
	I_{BB4} 1/	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling	t_{PC} = 225 ns	01,03		400	µA
			t_{PC} = 275 ns	02			
Supply current from V_{CC}	I_{CC1} 2/	$\overline{RAS}$ and $\overline{CAS}$ cycling		01,02,03		600	µA
				04,05		50	mA
	I_{CC2}	$\overline{RAS}$ and $\overline{CAS}$ = V_{IHC} D_{OUT} = High Z		01,02,03	-10	+10	µA
				04,05		5	mA
	I_{CC3}	$\overline{RAS}$ cycling, t_{RC} = 375 ns $\overline{CAS}$ = V_{IHC}		01,02,03	-10	+10	µA
				04,05		35	mA
	I_{CC4} 2/	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling D_{OUT} = High Z		01,02,03		1,000	µA
				04,05		35	mA
Random read or write cycle time	t_{RC}	See figures 6, 7, 8, 10		01,03,04	375	10,120	ns
				02,05	410		
Read-write cycle time	t_{RWC}	See figures 6, 9		01,03,04	375	10,120	ns
				02,05	425		
Page mode cycle time	t_{PC}	$\overline{RAS}$ = V_{IL} See figures 6, 11, 12		01,03,04	225		ns
				02,05	275		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Characteristics	Symbol	Conditions $-55^{\circ}C \leq T_C \leq +110^{\circ}C$ $V_{SS} = 0\ V$ $4.5\ V\ dc \leq V_{CC} \leq 5.5\ V\ dc$ unless otherwise specified	Device types	Limits		Unit
				Min	Max	
Access time from $\overline{RAS}$	t_{RAC} 3/	See figures 6, 7, 9, 11 4/ t_{RCD} = Min	01,03,04		200	ns
			02,05		250	
Access time from $\overline{CAS}$	t_{CAC} 3/	See figures 6, 7, 9, 11 t_{RCD} > Max	01,03,04		135	ns
			02,05		165	
Output buffer turn off delay	t_{OFF}	See figures 6, 7, 9, 11	01,03,04		50	ns
			02,05		60	
$\overline{RAS}$ precharge time	t_{RP}	See figures 6 through 12	01,03,04	120	1,000	ns
			02,05	150		
$\overline{RAS}$ pulse width	t_{RAS}	See figures 6 through 12	01,03,04	200	10,000	ns
			02,05	250		
$\overline{RAS}$ hold time	t_{RSH}	See figures 6, 7, 8, 9, 11, 12	01,03,04	135		ns
			02,05	165		
$\overline{CAS}$ hold time	t_{CSH}	See figures 6, 7, 8, 9, 11, 12	01,03,04	200		ns
			02,05	250		
$\overline{CAS}$ pulse width	t_{CAS}	See figures 6, 7, 8, 9, 11, 12	01,03,04	135	10,000	ns
			02,05	165		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	See figures 6, 7, 8, 9, 11, 12	01,03,04	30	65	ns
			02,05	35	85	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	See figures 6, 7, 8, 9, 11, 12	All	0		ns
Row address setup time	t_{ASR}	See figures 6 through 12	All	0		ns
Row address hold time	t_{RAH}	See figures 6 through 12	01,03,04	30		ns
			02,05	35		
Column address setup time	t_{ASC}	See figures 6, 7, 8, 9, 11, 12	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Characteristics	Symbol	Conditions $-55^{\circ}C \leq T_C \leq +110^{\circ}C$ $V_{SS} = 0$ V 4.5 V dc $\leq V_{CC} \leq$ 5.5 V dc unless otherwise specified	Device types	Limits Min	Limits Max	Unit
Column address hold time	t_{CAH}	See figures 6, 7, 8, 9, 11, 12	01,03,04	60		ns
			02,05	75		
Column address hold time referenced to $\overline{RAS}$	t_{AR}	See figures 6, 7, 8, 9, 11, 12	01,03,04	125		ns
			02,05	160		
Read command setup time	t_{RCS}	See figures 6, 7, 9, 11	All	0		ns
Read command hold time	t_{RCH}	See figures 6, 7, 9, 11	All	0		ns
Write command hold time	t_{WCH}	See figures 6, 8, 12	01,03,04	60		ns
			02,05	75		
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	See figures 6, 8, 12	01,03,04	125		ns
			02,05	160		
Write command pulse width	t_{WP}	See figures 6, 8, 9, 12	01,03,04	60		ns
			02,05	75		
Write command to $\overline{RAS}$ lead time	t_{RWL}	See figures 6, 8, 9, 12	01,03,04	80		ns
			02,05	100		
Write command to $\overline{CAS}$ lead time	t_{CWL}	See figures 6, 8, 9, 12	01,03,04	80		ns
			02,05	100		
Data in setup time to $\overline{CAS}$	$t_{DS(C)}$	See figures 6, 8, 12	All	0		ns
Data in setup time to write (late write)	$t_{DS(W)}$	See figures 6, 9	All	10		ns
Data in hold time	t_{DH}	See figures 6, 8, 9, 12	01,03,04	60		ns
			02,05	75		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Characteristics	Symbol	Conditions $-55°C \le T_C \le +110°C$ $V_{SS} = 0$ V 4.5 V dc $\le V_{CC} \le$ 5.5 V dc unless otherwise specified	Device types	Limits		Unit
				Min	Max	
Data in hold time referenced to $\overline{RAS}$	t_{DHR}	See figures 6, 8, 9, 12	01,03,04	125		ns
			02,05	160		
$\overline{CAS}$ precharge time (page mode only)	t_{CP}	See figures 6, 11, 12	01,03,04	80		ns
			02,05	100		
Refresh period	t_{REF}		All		1.0	ms
Write command setup time	t_{WCS}	See figures 6, 8	All	0		ns
$\overline{CAS}$ to $\overline{WRITE}$ delay	t_{CWD}	See figures 6, 9	01,03,04	95		ns
			02,05	125		
$\overline{RAS}$ to $\overline{WRITE}$ delay	t_{RWD}	See figures 6, 9	01,03,04	160		ns
			02,05	200		

1/ Depends on cycle rate. Limits are for cycle rates listed in conditions column.
2/ Depends on output load.
3/ Load = One Schottky TTL + 50 pF or equivalent.
4/ Device type 03 has page mode operation tested.

3.2.4 Case outline. The case outline shall be in accordance with 1.2.3.

3.3 Lead material and finish. Lead material and finish shall be in accordance with MIL-M-38510 (see 6.4).

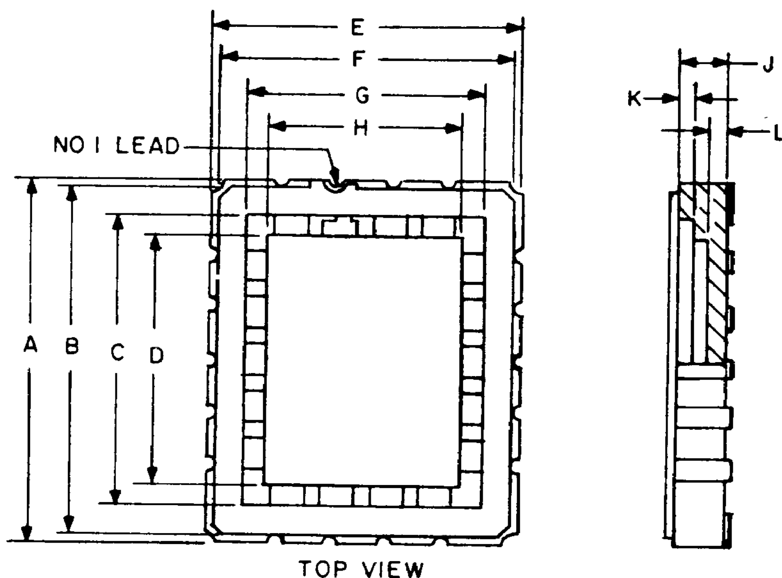
3.4 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and shall apply over the full case operating temperature range, unless otherwise specified.

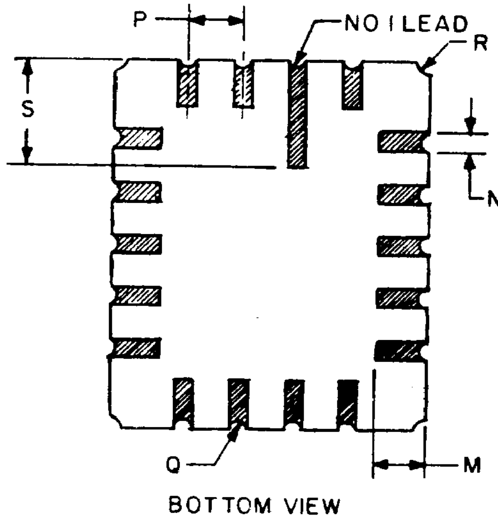
3.5 Rebonding. Rebonding shall be in accordance with MIL-M-38510.

3.6 Electrical test requirements. Electrical test requirements shall be as specified in table III for the applicable device type and device class. The subgroups of table III which constitute the minimum electrical test requirements for screening, qualification, and quality conformance by device class are specified in table II.

3.7 Marking. Marking shall be in accordance with MIL-M-38510.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 46 (see MIL-M-38510, appendix E).



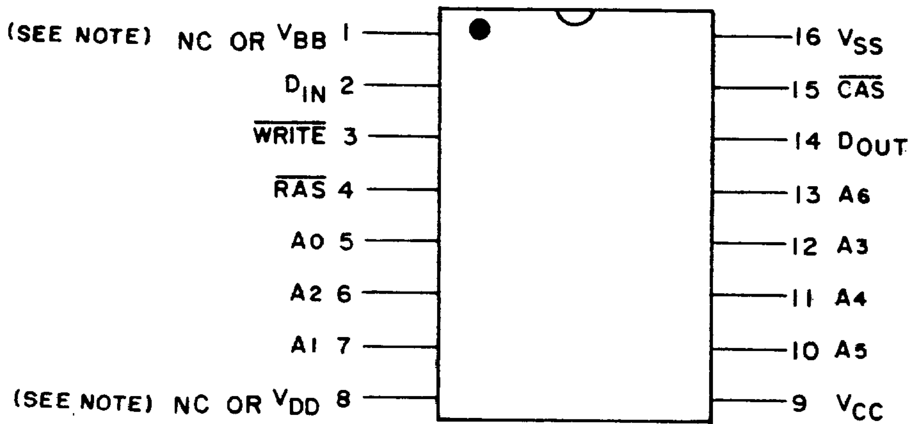


Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	.350	.360	8.89	9.14	
B	.330	.340	8.38	8.64	
C	.275	.285	6.99	7.24	
D	.235	.245	5.97	6.22	
E	.285	.290	7.24	7.37	
F	.265	.275	6.73	6.99	
G	.210	.220	5.33	5.59	
H	.170	.180	4.32	4.57	
J	.042	.048	1.07	1.22	
K	.012	.018	.33	.46	
L	.012	.018	.33	.46	
M	.040	.050	1.02	1.27	
N	.020	.030	.51	.76	5
P	.045	.055	1.14	1.40	2
Q	.008R		.20R		5
R	.012R		.30R		3
S	.090	.110	2.29	2.79	1

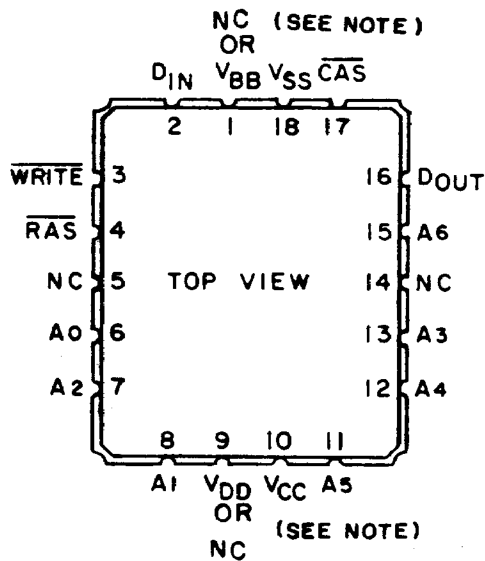
NOTES:
1. Index area: A notch, identification mark or elongation shall be used to identify pin 1.
2. 14 spaces.
3. Applies to all four corners.
4. Shaded areas are metallized to facilitate external connections
5. 18 locations.
6. No organic or polymeric materials shall be molded to the package.

FIGURE 1. Case outline Z (.360" x .290" x .048") leadless chip carrier package.

Cases E and F



Case Z



NOTE: NC for device types 04 and 05
V_{BB} and V_{DD} for device types 01 - 03

FIGURE 2. Terminal connections.

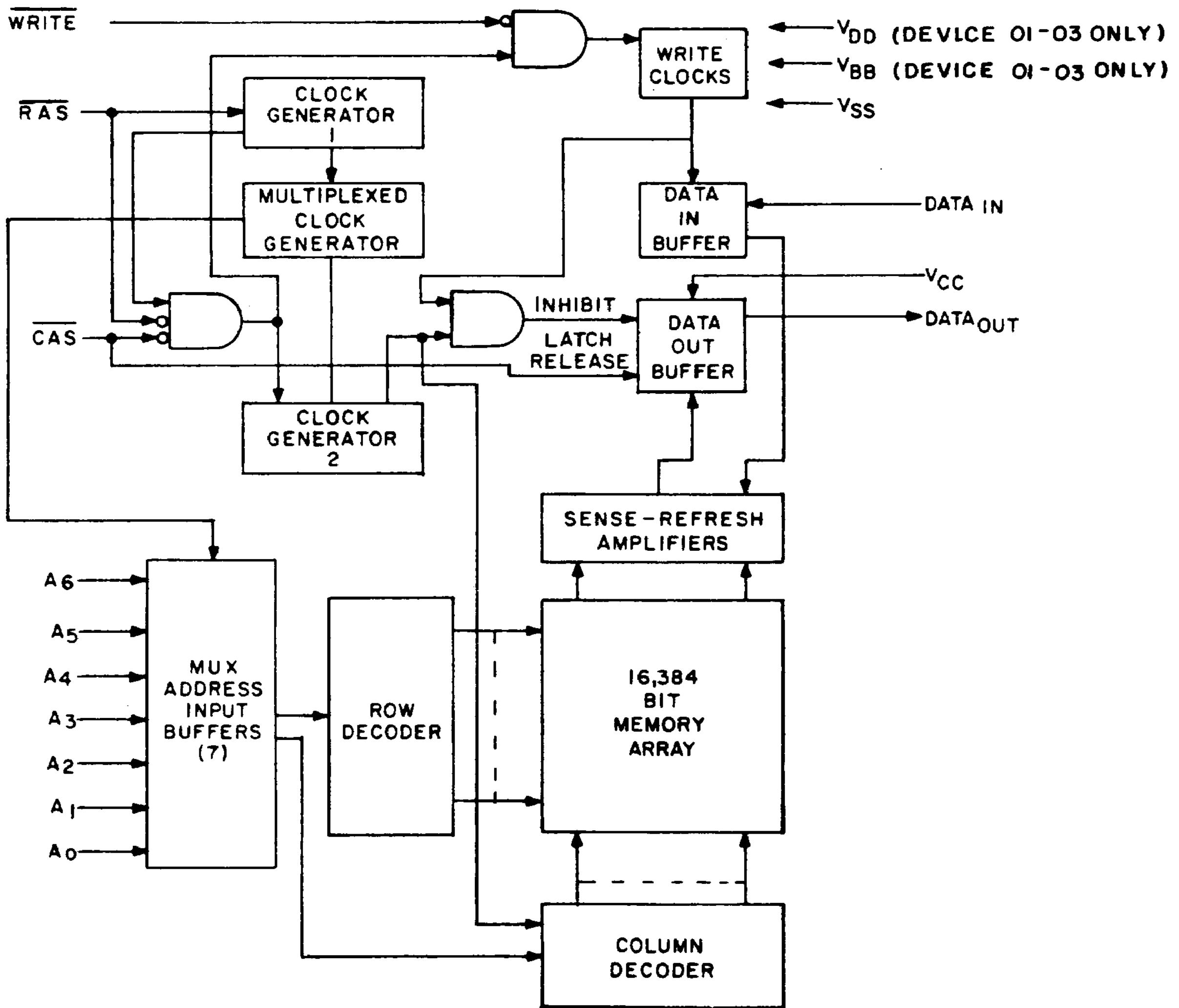


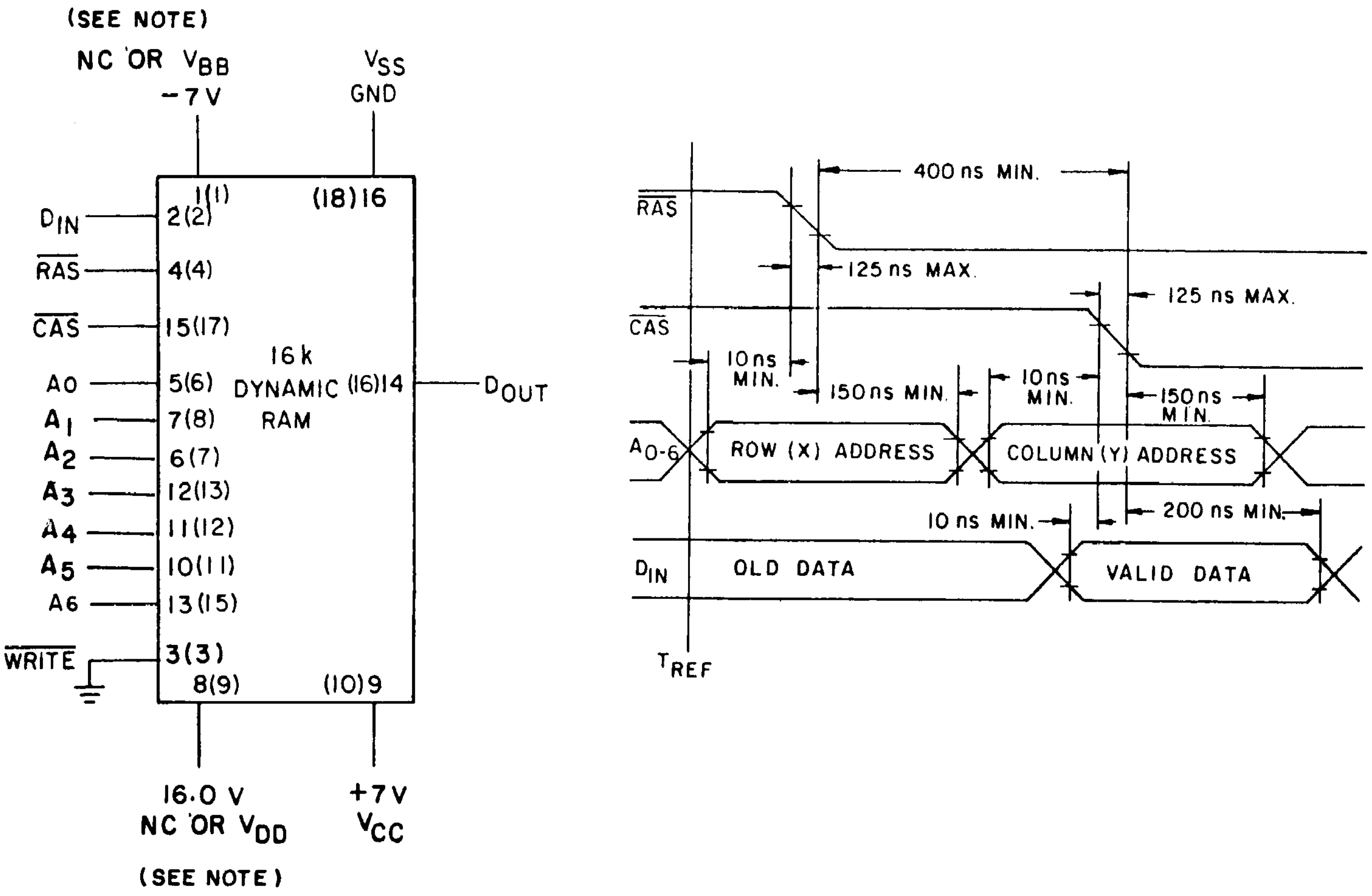
FIGURE 3. Block diagram.

Truth table						
Operation	Inputs					Output
	$\overline{RAS}$	$\overline{CAS}$	D_{IN}	ADDR	$\overline{Write}$	D_{OUT} see note 2
Chip not selected	H	H	X see note 3	X	X	High Z
Write "L" in cell A_{xy} See note 4	L	L	L	A_{xy}	L	High Z See note 5
Write "H" in cell A_{xy}	L	L	H	A_{xy}	L	High Z See note 5
Read data in cell A_{xy}	L	L	X	A_{xy}	H	Data (A_{xy})
$\overline{RAS}$ only refresh	L	H	X	A_x	X	High Z

NOTES

1. Eight intialization cycles required before truth table applies. All timing requirements must be applied.
2. D_{OUT} is not inverted from D_{IN}.
3. "X" = Don't care.
4. A_{xy} denotes proper address logic to address cell A_{xy}.
5. For "EARLY WRITE" timing, data out remains at high impedance. For "LATE WRITE" timing, data out is valid from access time to the beginning of a subsequent cycle, or until $\overline{CAS}$ goes to a high level high level.

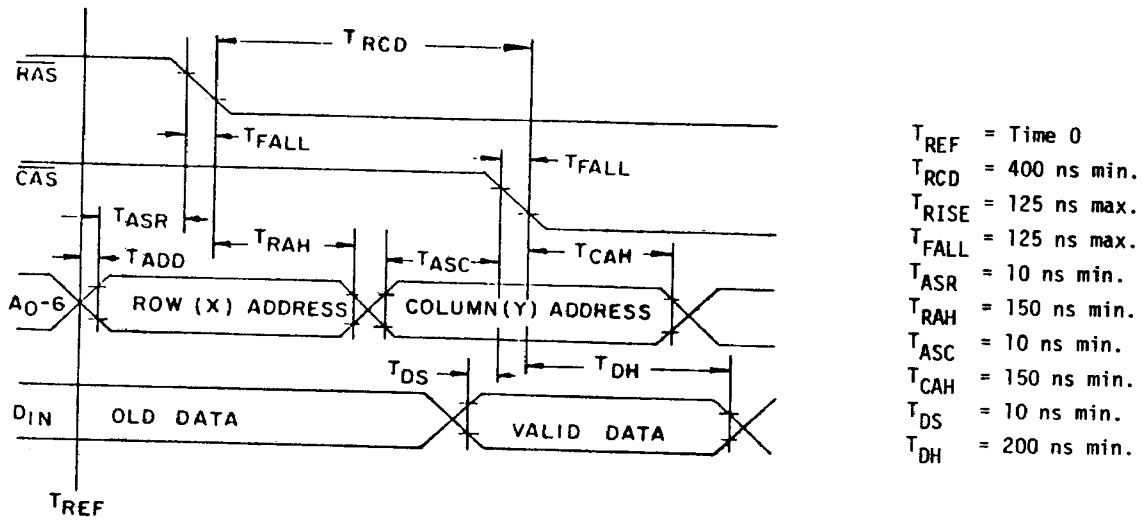
FIGURE 4. Truth table.



NOTE: NC for device types 04 and 05
V_{BB} and V_{DD} for device types 01 - 03.

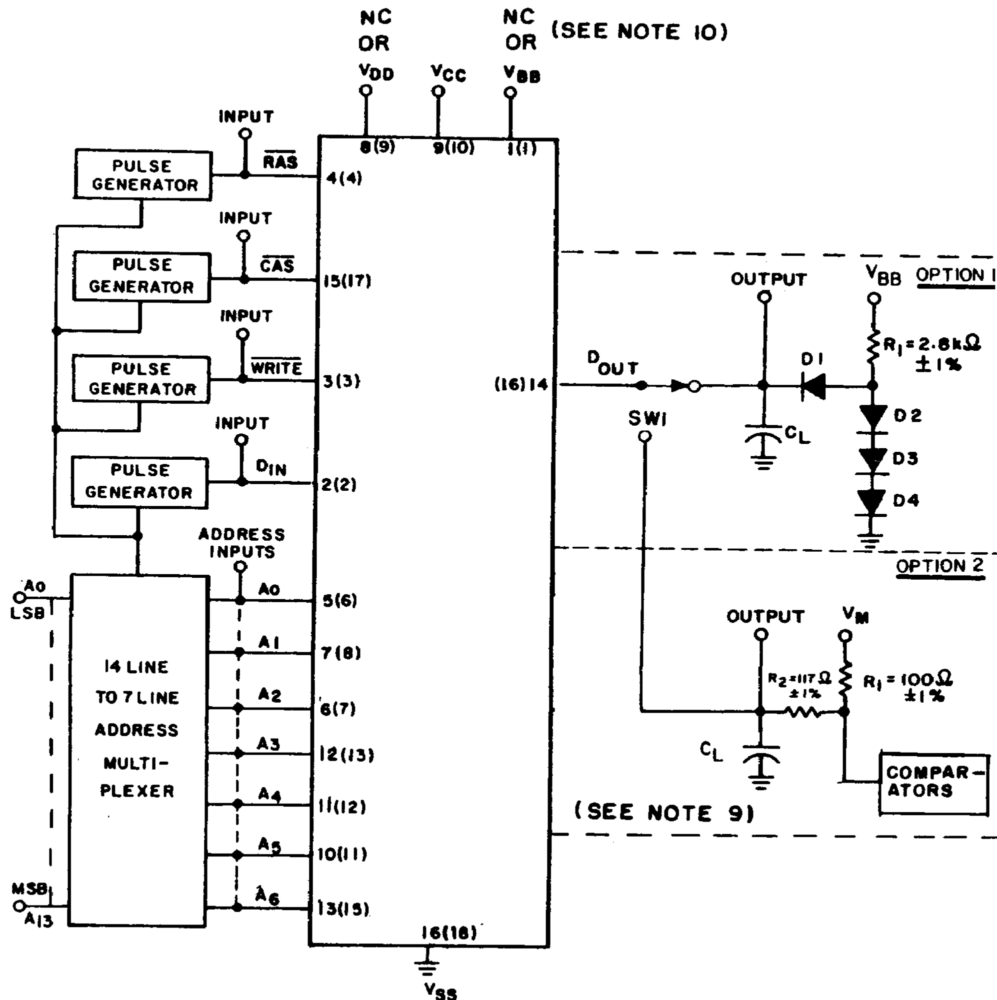
Pin connections for case outline Z are in parentheses

FIGURE 5. Burn-in and steady state life test circuit.



NOTE: Measurement points are V_{IL} and V_{IH}.

FIGURE 5. Burn-in and steady state life test circuit - Continued.



NOTES:
1. C_L = 50 pF minimum (includes scope probe, wiring, and stray wiring without package in test fixture).
2. D1-D4 are 1N3064.
3. All generators t_{TLH} and $t_{THL} \leq$ 10 ns.
4. All resistors are 1/2 watt.
5. Option 1 or option 2 load circuit may be used for all ac tests except the high impedance test, where option 2 shall be used and V_M = 1.3 V dc.
6. Pin connections for case outline Z are in parentheses.
7. SW1 is a software switch.
8. Option 2 conditions are: V_M = 1.3 V, V_{OH} = 1.125 V.
9. Output circuit option: Option 1 is used for device types 01 through 03, option 2 is used for device types 04 and 05.
10. NC for device types 04 and 05, V_{BB} and V_{DD} for device types 01 through 03.

FIGURE 6. Switching time test circuits.

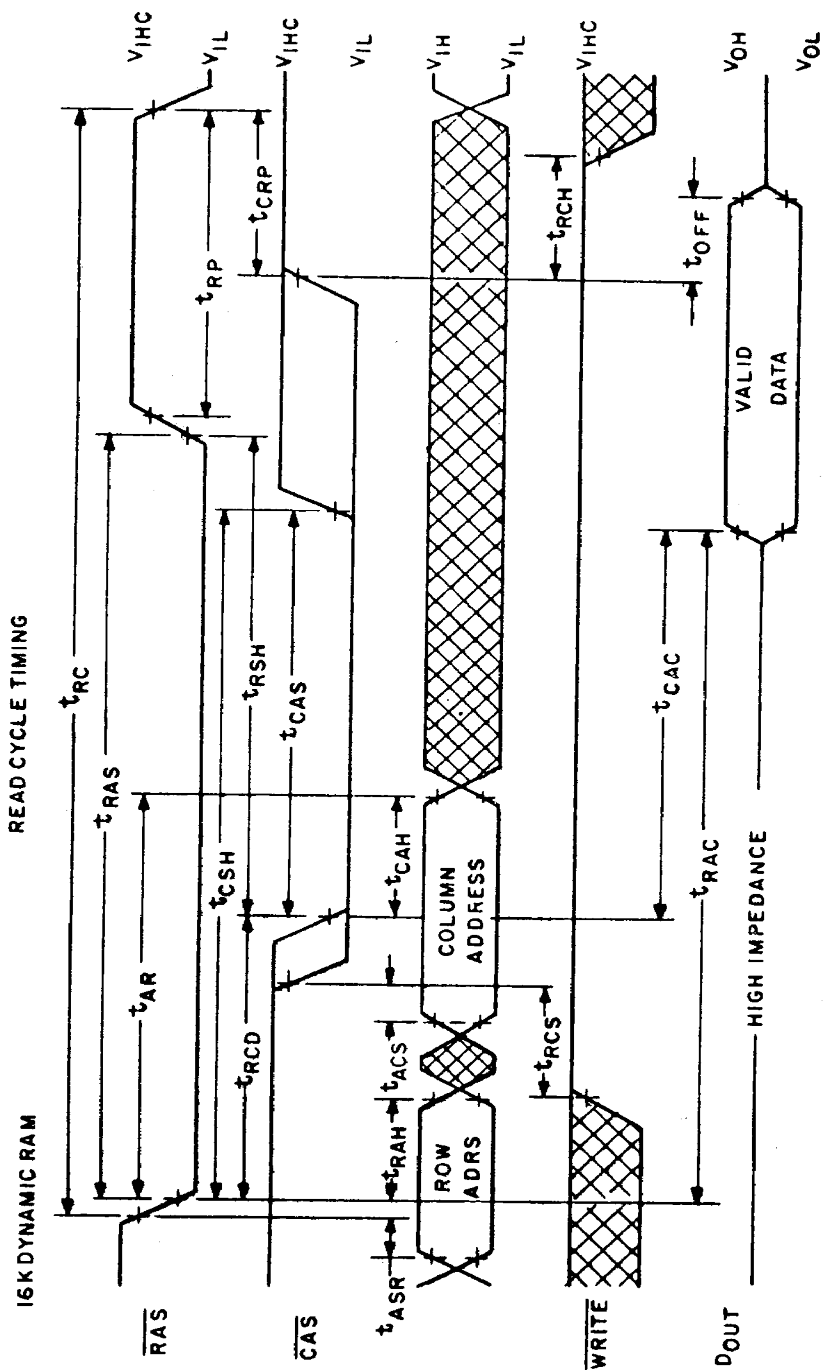


FIGURE 7. Read cycle waveforms.

FIGURE 8. **Write cycle waveforms.**

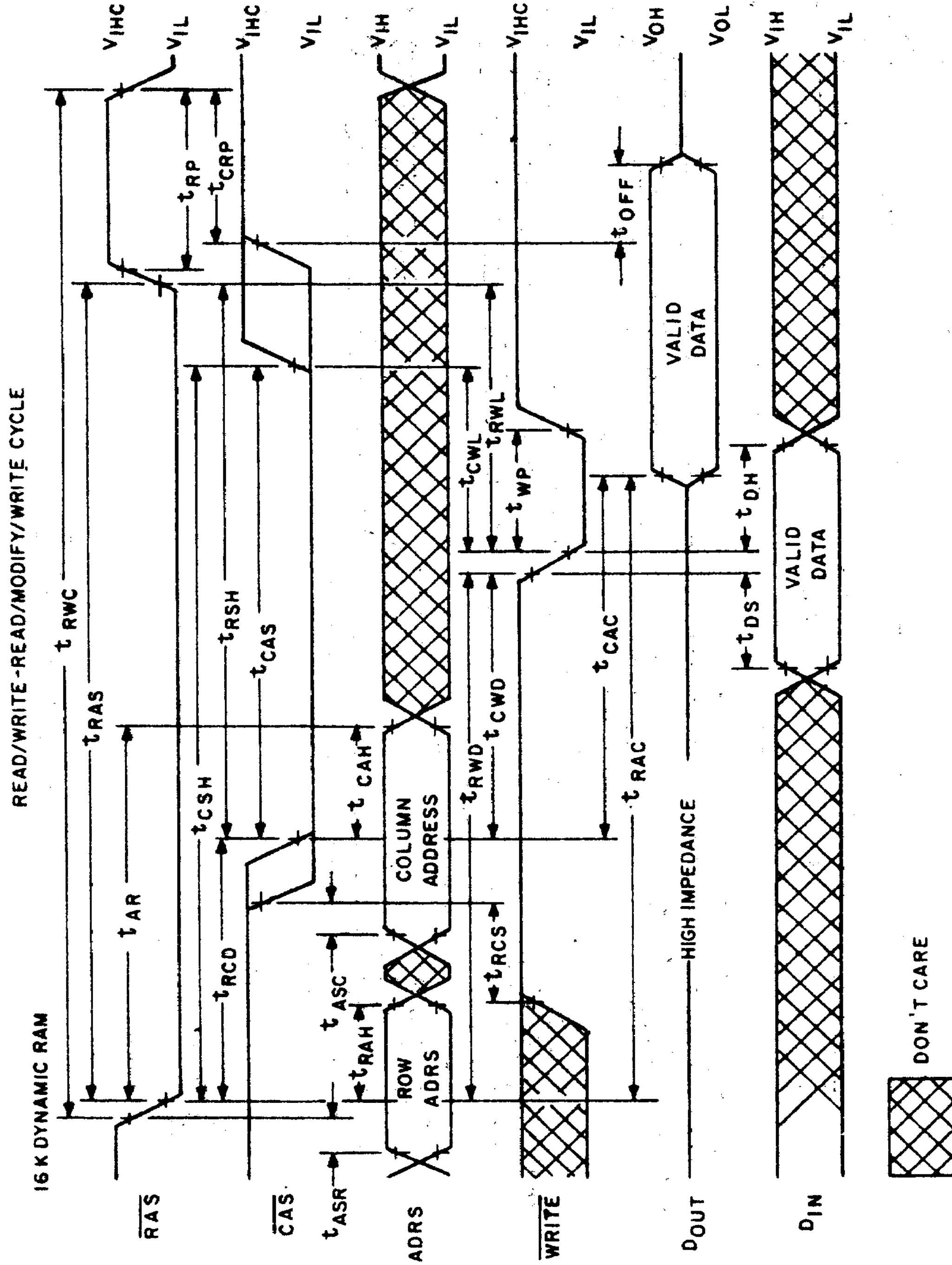
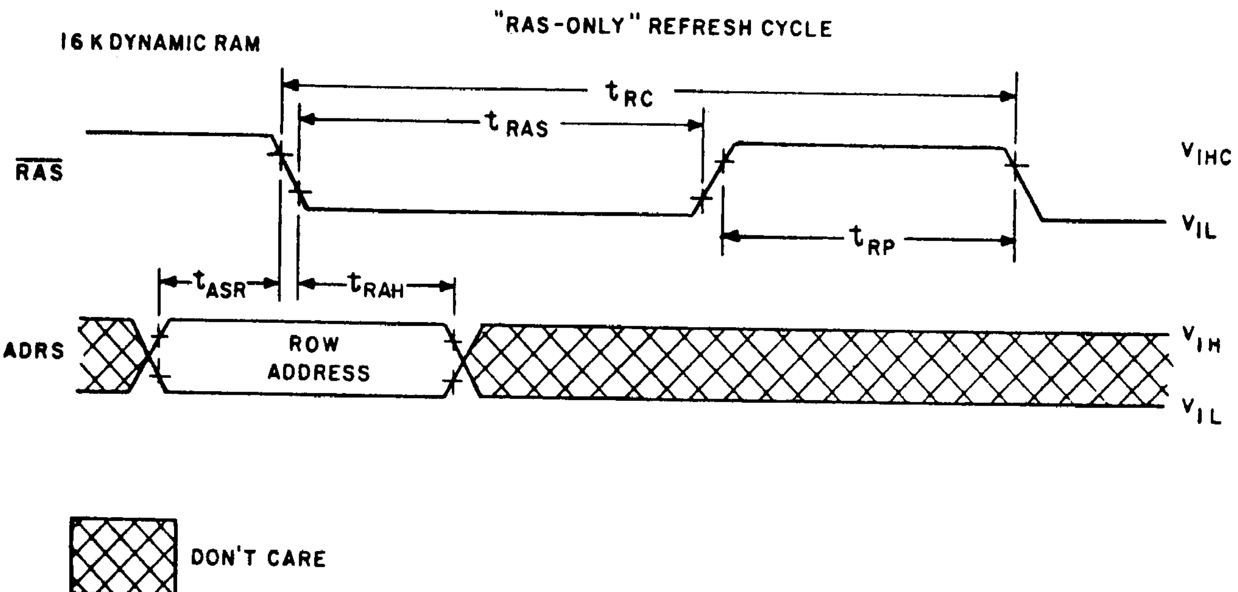


FIGURE 9. Read/write, read modify write cycle waveforms.



NOTE: $\overline{CAS}$ = V_{IHC}, $\overline{WRITE}$ and D_{IN} don't care.
D_{OUT} = High impedance

FIGURE 10. "RAS-ONLY" refresh cycle waveforms.

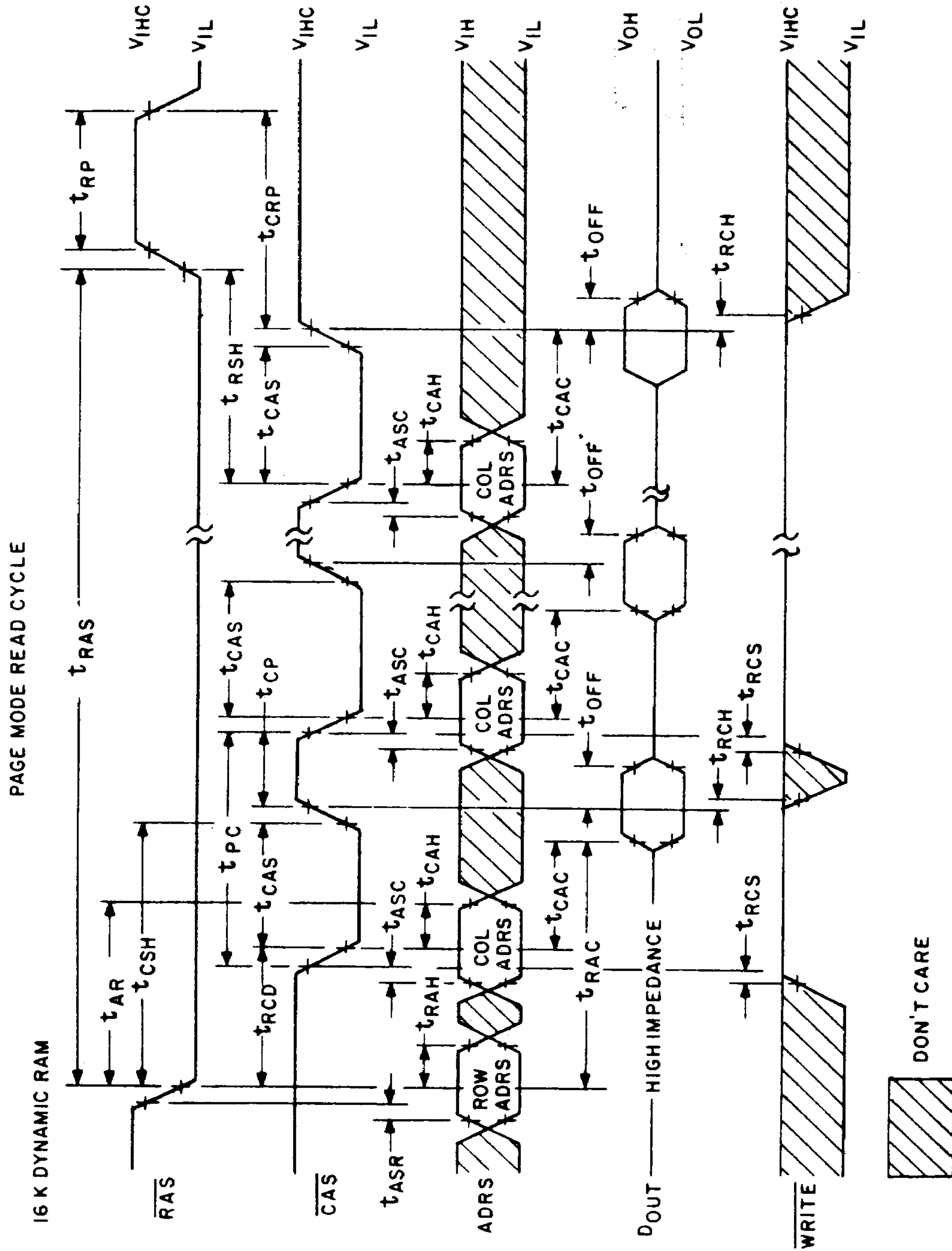


FIGURE 11. Page mode read cycle waveforms.

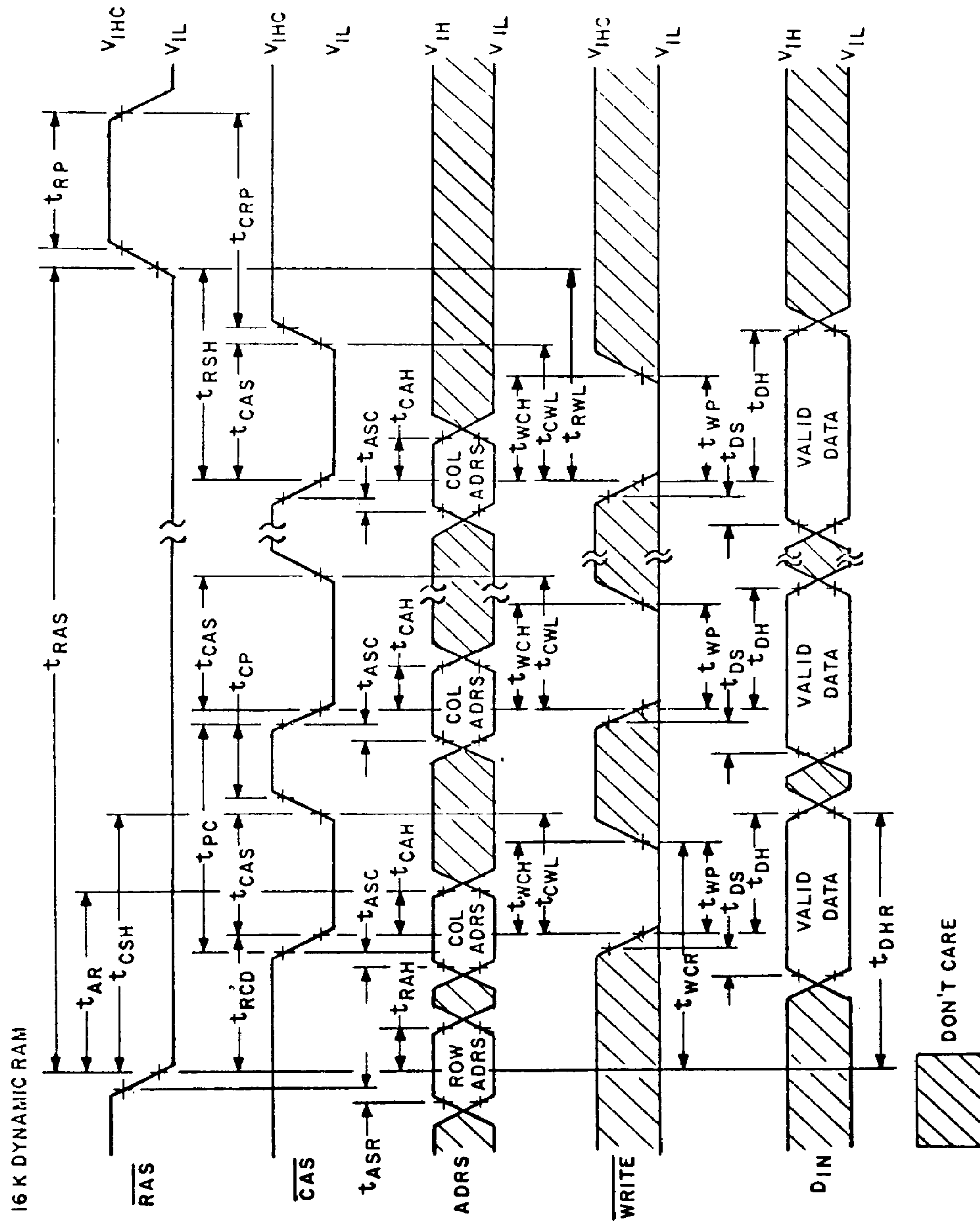


FIGURE 12. Page mode write cycle waveforms.

TABLE III. Group A inspection for device types 01, 02, and 03.
Terminal conditions (pins not designated may be high ≥ 2.4 V or low ≤ 0.45 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E,F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	---	Algo-rithms	Measured terminal	Test Limits		
			Case Z	1	2	3	4	6	7	8	9	10	11	12	13	15	16	17	18	5,14					
			Test No.	V_{BB}	D_{IN}	$\overline{WRITE}$	$\overline{RAS}$	A_0	A_2	A_1	V_{DD}	V_{CC}	A_5	A_4	A_3	A_6	D_{OUT}	$\overline{CAS}$	V_{SS}	NC			Min	Max	Units
1 $T_C = 25°C$ 1/	$I_{IL(ad)}$	3009	1	-5.5 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	13.2 V	5.0 V	0.0 V	0.0 V	0.0 V	0.0 V	OPEN	0.0 V	0.0 V			A_0	-10	+10	µA
			2	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			A_2	"	"	"
			3	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			A_1	"	"	"
			4	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			A_5	"	"	"
			5	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			A_4	"	"	"
			6	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			A_3	"	"	"
			7	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			A_6	"	"	"
	$I_{IH(ad)}$	3010	8	"	7.0 V	7.0 V	7.0 V	7.0 V	7.0 V	7.0 V	"	"	7.0 V	7.0 V	7.0 V	7.0 V	"	7.0 V	"			A_0	"	"	"
			9	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			A_2	"	"	"
			10	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			A_1	"	"	"
			11	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			A_5	"	"	"
			12	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			A_4	"	"	"
			13	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			A_3	"	"	"
			14	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			A_6	"	"	"

See footnotes at end of table.

TABLE III. Group A inspection for device types 01, 02, and 03 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.4 V or low ≤ 0.45 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E,F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	---	Algo-rithms	Measured terminal	Test Limits		
			Case Z	1	2	3	4	6	7	8	9	10	11	12	13	15	16	17	18	5,14			Min	Max	Units
			Test No.	V_{BB}	D_{IN}	$\overline{WRITE}$	$\overline{RAS}$	A_0	A_2	A_1	V_{DD}	V_{CC}	A_5	A_4	A_3	A_6	D_{OUT}	$\overline{CAS}$	V_{SS}	NC					
1 T_C = 25°C	$I_{IL(D_{IN})}$	3009 1/	15	-5.5 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	13.2 V	5.0 V	0.0 V	0.0 V	0.0 V	0.0 V	OPEN	0.0 V	0.0 V			D_{IN}	-10	+10	µA
	$I_{IL(\overline{WR})}$		16	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			$\overline{WRITE}$	"	"	"
	$I_{IL(\overline{RAS})}$		17	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			$\overline{RAS}$	"	"	"
	$I_{IL(\overline{CAS})}$		18	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			$\overline{CAS}$	"	"	"
	$I_{IH(D_{IN})}$	3010 1/	19	"	7.0 V	7.0 V	7.0 V	7.0 V	7.0 V	7.0 V	"	"	7.0 V	7.0 V	7.0 V	7.0 V	"	7.0 V	"			D_{IN}	"	"	"
	$I_{IH(\overline{WR})}$		20	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			$\overline{WRITE}$	"	"	"
	$I_{IH(\overline{RAS})}$		21	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			$\overline{RAS}$	"	"	"
	$I_{IH(\overline{CAS})}$		22	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			$\overline{CAS}$	"	"	"
	I_{OLZ} 2/	3009	23	-4.5 V	0.0 V	0.0 V	5.0 V	0.0 V	0.0 V	0.0 V	"	5.5 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	5.0 V	"			D_{OUT}	"	"	"
	I_{OHZ} 2/	3010	24	-4.5 V	0.0 V	0.0 V	5.0 V	0.0 V	0.0 V	0.0 V	"	5.5 V	0.0 V	0.0 V	0.0 V	0.0 V	5.5 V	5.0 V	"			D_{OUT}	"	"	"
	V_{OL}	3007	25	-5.5 V	3/	3/	3/	3/	3/	3/	10.8 V	4.5 V	3/	3/	3/	3/	4.2 mA	3/	"			D_{OUT}		0.4	V
	V_{OH}	3006	26	-5.5 V	3/	3/	3/	3/	3/	3/	10.8 V	4.5 V	3/	3/	3/	3/	-5.0 mA	3/	"			D_{OUT}	2.4		V

See footnotes at end of table.

TABLE III. Group A inspection for device types 01, 02, and 03 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.4 V or low ≤ 0.45 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E,F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	---	Algorithms 4/	Measured terminal	Test Limits		
			Case Z	1	2	3	4	6	7	8	9	10	11	12	13	15	16	17	18	5,14			Min	Max	Units
			Test No.	V_{BB}	D_{IN}	$\overline{WRITE}$	$\overline{RAS}$	A_0	A_2	A_1	V_{DD}	V_{CC}	A_5	A_4	A_3	A_6	D_{OUT}	$\overline{CAS}$	V_{SS}	NC					
1 $T_C = 25°C$	$I_{CC}2$	3005	27	-5.5 V	0.0 V	2.7 V	2.7 V	0.0 V	0.0 V	0.0 V	13.2 V	5.5 V	0.0 V	0.0 V	0.0 V	0.0 V		2.7 V	0.0 V			V_{CC}	-10	+10	µA
	$I_{BB}2$		28	-5.5 V	"	"	"	"	"	"	"	"	"	"	"	"		"	"			V_{BB}		200	µA
	$I_{DD}2$		29	-4.5 V	"	"	"	"	"	"	"	"	"	"	"	"		"	"			V_{DD}		2.25	mA
	$I_{CC}1$		30	-5.5 V	6/	6/	6/	6/	6/	6/	"	"	6/	6/	6/	6/	5/	6/	"		Pat. 7	V_{CC}		2.2	mA
	$I_{BB}1$		31	-5.5 V	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		"	V_{BB}		400	µA
	$I_{DD}1$		32	-4.5 V	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		"	V_{DD}		35	mA
	V_{OZ}		33	-4.5 V	7/	7/	7/	7/	7/	7/	10.8 V	4.5 V	7/	7/	7/	7/		7/			Pat. 9	D_{OUT}	2.05	2.45	V
2	Same tests, terminal conditions, and limits as for subgroup 1, except $T_C = 110°C$.																								
3	Same tests, terminal conditions, and limits as for subgroup 1, except $T_C = -55°C$, and $I_{DD}1$ limit is 40 mA and $I_{BB}1$ is 400 µA.																								
9 $T_C = 25°C$ 9/	V_{BUMP}		34	8/	7/	7/	7/	7/	7/	7/	8/	5.0 V	7/	7/	7/	7/	5/	7/	0.0 V		8/	D_{OUT}			ns
	t_{RAC}		35	-4.5 V	"	"	"	"	"	"	10.8 V	4.5 V	"	"	"	"	"	"	"		Pat. 1, 2,3	"		10/	"
			36	-4.5 V	"	"	"	"	"	"	13.2 V	"	"	"	"	"	"	"	"		"	"		"	"
			37	-5.5 V	"	"	"	"	"	"	10.8 V	"	"	"	"	"	"	"	"		"	"		"	"
			38	"	"	"	"	"	"	"	13.2 V	"	"	"	"	"	"	"	"		"	"		"	"
			39	"	"	"	"	"	"	"	10.8 V	"	"	"	"	"	"	"	"		Pat. 4, 5	"		1.0	ms
			40	"	"	"	"	"	"	"	10.8 V	"	"	"	"	"	"	"	"		Pat. 6	"		10/	ns

See footnotes at end of table.

TABLE III. Group A inspection for device types 01, 02, and 03 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.4 V or low ≤ 0.45 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E,F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	---	Algo-rithms 4/	Measured terminal	Test Limits		
			Case Z	1	2	3	4	6	7	8	9	10	11	12	13	15	16	17	18	5,14					
			Test No.	V_{BB}	D_{IN}	$\overline{WRITE}$	$\overline{RAS}$	A_0	A_2	A_1	V_{DD}	V_{CC}	A_5	A_4	A_3	A_6	D_{OUT}	$\overline{CAS}$	V_{SS}	NC			Min	Max	Units
9 $T_C = 25°C$ 9/	t_{CAC} 13/		41	-4.5 V	11/	11/	11/	11/	11/	11/	10.8 V	4.5 V	11/	11/	11/	11/	5/	11/	0.0 V		Pat. 8	D_{OUT}		12/	ns
	"		42	-4.5 V	"	"	"	"	"	"	13.2 V	"	"	"	"	"	"	"	"		"	"		"	"
	"		43	-5.5 V	"	"	"	"	"	"	10.8 V	"	"	"	"	"	"	"	"		"	"		"	"
	"		44	-5.5 V	"	"	"	"	"	"	13.2 V	"	"	"	"	"	"	"	"		"	"		"	"
10 9/	Same tests, terminal conditions, and limits as for subgroup 9, except $T_C = 110°C$.																								
11 9/	Same tests, terminal conditions, and limits as for subgroup 10, except $T_C = -55°C$, and omit test 39 and 40.																								

1/ I_{IL} and I_{IH} may be measured by paralleling inputs A_0-A_6, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, and D_{IN} (all other pin conditions as defined).

2/ Multiple toggles between 5.0 V and 0.0 V are applied to $\overline{RAS}$ and $\overline{CAS}$; after toggling, $\overline{RAS}$ and $\overline{CAS}$ are at 5.0 V.

3/ These tests are listed but not tested. The output limits shall be set and used as conditions for dynamic go/no-go testing.

4/ See the appendix for description of algorithms.

5/ Output loaded with one Standard Schottky TTL and 50 pF.

6/ All input levels and timing edges are set to table I limits.

7/ All input levels and timing edges are set to table I limits with t_{RCD} at minimum.

8/ V_{BUMP}, at minimum V_{DD} and maximum V_{BB} the entire matrix is written (low level) to discharge cells. The V_{DD} and V_{BB} supplies are then slewed in the positive direction, and the entire matrix is read for discharged cells. V_{DD} is slewed from 10.8 V to 11.8 V; V_{BB} is slewed from -5.5 V to -5.0 V.

9/ When variables data is required (e.g., during qualification), the minimum data to be recorded shall be the worse case value per device for tests 35, 36, 37, and 38, pattern 1 of subgroup 10 (high temperature). Variables data shall not be conducted for other tests in subgroups 9, 10, and 11, but the tests shall be conducted for the limit values on an attribute basis.

10/ For device type 01, t_{RAC} = 200 ns; for device type 02, t_{RAC} = 250 ns.

11/ All input levels and timing edges are set to table I limits with page mode timing.

12/ For device type 01 and 03, t_{CAC} = 135 ns; for device type 02, t_{CAC} = 165 ns.

13/ Page mode tested for device type 03 only.

TABLE III. Group A inspection for device types 04 and 05.
Terminal conditions (pins not designated may be high ≥ 2.4 V or low ≤ 0.45 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E,F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	---	Algo-rithms	Measured terminal	Test Limits		
			Case Z	1	2	3	4	6	7	8	9	10	11	12	13	15	16	17	18	5,14					
			Test No.	NC	D_{IN}	$\overline{WRITE}$	$\overline{RAS}$	A_0	A_2	A_1	NC	V_{CC}	A_5	A_4	A_3	A_6	D_{OUT}	$\overline{CAS}$	V_{SS}	NC			Min	Max	Units
1 T_C = 25°C 1/	$I_{IL(ad)}$	3009	1		0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V		5.0 V	0.0 V	0.0 V	0.0 V	0.0 V	OPEN	0.0 V	0.0 V			A_0	-10	+10	µA
			2		"	"	"	"	"	"		"	"	"	"	"	"	"	"			A_2	"	"	"
			3		"	"	"	"	"	"		"	"	"	"	"	"	"	"			A_1	"	"	"
			4		"	"	"	"	"	"		"	"	"	"	"	"	"	"			A_5	"	"	"
			5		"	"	"	"	"	"		"	"	"	"	"	"	"	"			A_4	"	"	"
			6		"	"	"	"	"	"		"	"	"	"	"	"	"	"			A_3	"	"	"
			7		"	"	"	"	"	"		"	"	"	"	"	"	"	"			A_6	"	"	"
	$I_{IH(ad)}$	3010	8		6.5 V	6.5 V	6.5 V	6.5 V	6.5 V	6.5 V		"	6.5 V	6.5 V	6.5 V	6.5 V	"	6.5 V	"			A_0	"	"	"
			9		"	"	"	"	"	"		"	"	"	"	"	"	"	"			A_2	"	"	"
			10		"	"	"	"	"	"		"	"	"	"	"	"	"	"			A_1	"	"	"
			11		"	"	"	"	"	"		"	"	"	"	"	"	"	"			A_5	"	"	"
			12		"	"	"	"	"	"		"	"	"	"	"	"	"	"			A_4	"	"	"
			13		"	"	"	"	"	"		"	"	"	"	"	"	"	"			A_3	"	"	"
			14		"	"	"	"	"	"		"	"	"	"	"	"	"	"			A_6	"	"	"

See footnotes at end of table.

TABLE III. Group A inspection for device types 04 and 05 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.4 V or low ≤ 0.45 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E,F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	---	Algo-rithms	Measured terminal	Test Limits		
			Case Z	1	2	3	4	6	7	8	9	10	11	12	13	15	16	17	18	5,14					
			Test No.	NC	D_{IN}	$\overline{WRITE}$	$\overline{RAS}$	A_0	A_2	A_1	NC	V_{CC}	A_5	A_4	A_3	A_6	D_{OUT}	$\overline{CAS}$	V_{SS}	NC			Min	Max	Units
1 T_C = 25°C	$I_{IL(D_{IN})}$	3009 1/	15		0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V		5.5 V	0.0 V	0.0 V	0.0 V	0.0 V	OPEN	0.0 V	0.0 V			D_{IN}	-10	+10	µA
	$I_{IL(\overline{WR})}$		16		"	"	"	"	"	"		"	"	"	"	"	"	"	"			$\overline{WRITE}$	"	"	"
	$I_{IL(\overline{RAS})}$		17		"	"	"	"	"	"		"	"	"	"	"	"	"	"			$\overline{RAS}$	"	"	"
	$I_{IL(\overline{CAS})}$		18		"	"	"	"	"	"		"	"	"	"	"	"	"	"			$\overline{CAS}$	"	"	"
	$I_{IH(D_{IN})}$	3010 1/	19		6.5 V	6.5 V	6.5 V	6.5 V	6.5 V	6.5 V		"	6.5 V	6.5 V	6.5 V	6.5 V	"	6.5 V	"			D_{IN}	"	"	"
	$I_{IH(\overline{WR})}$		20		"	"	"	"	"	"		"	"	"	"	"	"	"	"			$\overline{WRITE}$	"	"	"
	$I_{IH(\overline{RAS})}$		21		"	"	"	"	"	"		"	"	"	"	"	"	"	"			$\overline{RAS}$	"	"	"
	$I_{IH(\overline{CAS})}$		22		"	"	"	"	"	"		"	"	"	"	"	"	"	"			$\overline{CAS}$	"	"	"
	I_{OLZ} 2/	3009	23		0.0 V	0.0 V	5.0 V	0.0 V	0.0 V	0.0 V		"	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	5.0 V	"			D_{OUT}	"	"	"
	I_{OHZ} 2/	3010	24		0.0 V	0.0 V	5.0 V	0.0 V	0.0 V	0.0 V		"	0.0 V	0.0 V	0.0 V	0.0 V	5.5 V	5.0 V	"			D_{OUT}	"	"	"
	V_{OL}	3007	25		3/	3/	3/	3/	3/	3/		4.5 V	3/	3/	3/	3/	4.2 mA	3/	"			D_{OUT}		0.4	V
	V_{OH}	3006	26		3/	3/	3/	3/	3/	3/		4.5 V	3/	3/	3/	3/	-5.0 mA	3/	"			D_{OUT}	2.4		V

See footnotes at end of table.

TABLE III. Group A inspection for device types 04 and 05 - Continued.
Terminal conditions (pins not designated may be high $\geq$ 2.4 V or low $\leq$ 0.45 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E,F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	---	Algorithms 4/	Measured terminal	Test Limits		
			Case Z	1	2	3	4	6	7	8	9	10	11	12	13	15	16	17	18	5,14			Min	Max	Units
			Test No.	NC	D_{IN}	$\overline{WRITE}$	$\overline{RAS}$	A_0	A_2	A_1	NC	V_{CC}	A_5	A_4	A_3	A_6	D_{OUT}	$\overline{CAS}$	V_{SS}	NC					
1 T_C = 25°C	$I_{CC}2$	3005	27		0.0 V	2.7 V	2.7 V	0.0 V	0.0 V	0.0 V		5.5 V	0.0 V	0.0 V	0.0 V	0.0 V		2.7 V	0.0 V			V_{CC}		+10	mA
	$I_{CC}1$		28		6/	6/	6/	6/	6/	6/		5.5 V	6/	6/	6/	6/	5/	6/	0.0 V		Pat. 7	V_{CC}		50	mA
	V_{OZ}		29		7/	7/	7/	7/	7/	7/		4.5 V	7/	7/	7/	7/		7/	0.0 V		Pat. 9	D_{OUT}	2.05	2.45	V
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = 110°C.																								
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C.																								
9 T_C = 25°C 8/	V_{BUMP}		30		7/	7/	7/	7/	7/	7/		5.0 V	7/	7/	7/	7/	5/	7/	0.0 V		Pat. 10	D_{OUT}			ns
	t_{RAC}		31		"	"	"	"	"	"		4.5 V	"	"	"	"	"	"	"		Pat. 1, 2,3	"			"
			32		"	"	"	"	"	"		5.5 V	"	"	"	"	"	"	"		"	"		9/	"
			33		"	"	"	"	"	"		4.5 V	"	"	"	"	"	"	"		Pat. 4, 5	"		1.0	ms
			34		"	"	"	"	"	"		4.5 V	"	"	"	"	"	"	"		Pat. 6	"		9/	ns

See footnotes at end of table.

TABLE III. Group A inspection for device types 04 and 05 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.4 V or low ≤ 0.45 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E,F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	---	Algorithms 4/	Measured terminal	Test Limits		
			Case Z	1	2	3	4	6	7	8	9	10	11	12	13	15	16	17	18	5,14			Min	Max	Units
			Test No.	NC	D_{IN}	$\overline{WRITE}$	$\overline{RAS}$	A_0	A_2	A_1	NC	V_{CC}	A_5	A_4	A_3	A_6	D_{OUT}	$\overline{CAS}$	V_{SS}	NC					
9 $T_C = 25°C$ 8/	t_{CAC}		35		10/	10/	10/	10/	10/	10/		4.5 V	10/	10/	10/	10/	5/	10/	0.0 V		Pat. 8	D_{OUT}		11/	ns
			36		"	"	"	"	"	"		"	"	"	"	"	"	"	"		"	"		"	"
			37		"	"	"	"	"	"		"	"	"	"	"	"	"	"		"	"		"	"
			38		"	"	"	"	"	"		"	"	"	"	"	"	"	"		"	"		"	"
10 8/	Same tests, terminal conditions, and limits as for subgroup 9, except $T_C = 110°C$.																								
11 8/	Same tests, terminal conditions, and limits as for subgroup 10, except $T_C = -55°C$, and omit test 33 and 34.																								

1/ I_{IL} and I_{IH} may be measured by paralleling inputs A_0-A_6, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, and D_{IN} (all other pin conditions as defined).

2/ Multiple toggles between 5.0 V and 0.0 V are applied to $\overline{RAS}$ and $\overline{CAS}$; after toggling, $\overline{RAS}$ and $\overline{CAS}$ are at 5.0 V.

3/ These tests are listed but not tested. The output limits shall be set and used as conditions for dynamic go/no-go testing.

4/ See the appendix for description of algorithms.

5/ Output loaded with one Standard Schottky TTL and 50 pF.

6/ All input levels and timing edges are set to table I limits.

7/ All input levels and timing edges are set to table I limits with t_{RCD} at minimum.

8/ When variables data is required (e.g., during qualification), the minimum data to be recorded shall be the worse case value per device for tests 31 and 32, pattern 1 of subgroup 10 (high temperature). Variables data shall not be conducted for other tests in subgroups 9, 10, and 11, but tests shall be conducted for the limit values on an attribute basis.

9/ For device type 04 t_{RAC} = 200 ns; for device type 05 t_{RAC} = 250 ns.

10/ All input levels and timing edges are set to table I limits with page mode timing.

11/ For device type 04 t_{CAC} = 135 ns; for device type 05 t_{CAC} = 165 ns.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

a. When the alternate screening option of 3.3 of method 5004 is applied to class B devices, the following additional items are applicable:

   1. Internal visual, method 2010, condition B. In addition to the changes indicated by 3.3.1 of method 5004, the following additional clarifications and deletions are applicable:

      (a) Metallization inspection shall be applicable to the top layer metal conductor (i.e., Al) and need not include "underlying conductors" such as polysilicon.

      (b) Omit 3.2.1.1(b) through 3.2.1.1(e), 3.2.1.2(b) through 3.2.1.2(e) and 3.2.3(e) (items 3.2.1.1(f) and 3.2.3(g) do not apply).

   2. Burn-in duration for class B shall be 160 hours minimum.

   3. The following voltage stress test may be used to satisfy 3.3.1c of method 5004 of MIL-STD-883. The voltage stress test shall be added to screening procedure (method 5004 of MIL-STD-883) after seal (3.1.6 of method 5004) and before the interim electrical screen (3.1.9 of method 5004). Voltage stress test condition is shown in figure 5, (same as burn-in) or equivalent, with the following voltage modifications:

      (a) V_{DD} = +16 volts, V_{BB} = -7.0 volts.

      (b) T_A = 125°C minimum for 12 hours minimum.

b. Burn-in test (method 1015 of MIL-STD-883):

   1. Test condition D, using the circuit shown on figure 5, or equivalent.

   2. T_A = 125°C minimum.

c. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters' test prior to burn-in is optional at the discretion of the manufacturer.

d. The percent defective allowable (PDA) is specified as 5 percent for class S devices and 10 percent for class B devices based on failures from group A, subgroup 2 and 10 combined tests, after cooldown as final electrical test in accordance with method 5004 of MIL-STD-883, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from pre burn-in screening may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, then all screening failures shall be included in the PDA. The verified failures of group A, subgroups 2 and 10, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent defective for that lot, and the lot shall be accepted or rejected based on the PDA for the applicable device class.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.3.1 Qualification extension. When authorized by the qualifying activity, for qualification inspection, if a manufacturer qualifies one device type which is manufactured identically to a slower device type on this specification, the slower device type may be part I qualified without further qualification testing. At the manufacturer's request, the slower device types will be added to the QPL.

4.3.2 Electrostatic discharge sensitivity qualification inspection. Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015. The option to categorize devices as ESD sensitive without performing the test is not allowed. Only those device types that pass ESDS testing at 500 volts or greater shall be considered as conforming to the requirements of this specification. ESDS testing shall be measured only for initial qualification and after process or design changes which may affect ESDS classification.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirement	Subgroups (see table III	
	Class S devices	Class B devices
Interim electrical parameters (pre burn-in)(method 5004)	1, 9, 10	2, 10
Final electrical test parameters (method 5004)	1, 2*, 3, 9, 10*, 11	2*, 10*
Group A test requirements (method 5005)	1, 2, 3, 9, 10, 11	2, 10
Group C end point electrical parameters (method 5005)	NA	2, 10
Group D end point electrical parameters (method 5005)	1, 2, 3, 10	2, 10

* The PDA applies to subgroups (see 4.2d).

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 4 through 8 for class S and subgroups 1, 3 through 9, and 11 for class B of table I of method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883 and as follows:

a. Subgroup 3 (solderability) shall be omitted for devices in package Z.

b. Subgroup 4 (lead integrity) for class S devices shall be omitted for devices in package Z.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

a. End point electrical parameters shall be as specified in table II herein.

b. Steady state life test (method 1005 of MIL-STD-883) conditions:

1. Test condition D, using the circuit shown on figure 5, or equivalent.

2. T_A = 125°C minimum.

3. Test duration - 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883 and as follows:

a. End point electrical parameters shall be as specified in table II herein.

b. Subgroup 2 (lead integrity) shall be omitted for package Z.

c. For moisture resistance and salt atmosphere of subgroups 3 and 5, omit initial conditioning for package Z.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit V_{SS} terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

4.5.2 Life test, burn-in, and voltage stress cooldown procedure. When devices are measured at 25°C following application of the operating life or burn-in test condition, they shall be cooled to 35°C prior to removal of the bias.

4.6 Inspection of packaging. Inspection of packaging shall be in accordance with MIL-M-38510, except that the rough handling test shall not apply.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents must specify the following:

a. Title, number, and date of the specification.

b. Issue of DODISS to be cited in the solicitation, and if required, the specific issue of individual documents referenced (see 2.1).

c. Part or Identifying Number (PIN) (see 6.7).

d. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

e. Requirement for certificate of compliance, if applicable.

f. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.

g. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action and reporting of results, if applicable.

h. Requirements for product assurance options.

i. Requirements for special lead lengths or lead forming, if applicable. Unless otherwise specified, these requirements shall not apply to direct purchase by or direct shipment to the Government.

j. Requirement for "JAN" marking.

6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

V_{DD}	Supply voltage, drain
V_{SS}	Common or reference voltage node
V_{BB}	Supply voltage, substrate
V_{CC}	Supply voltage, output buffer
$\overline{RAS}$	Row address strobe, input
$\overline{CAS}$	Column address strobe, input
$\overline{WRITE}$ OR $\overline{WR}$	Read or write input
D_{IN}	Data-input
D_{OUT}	Data-output
A_0 through A_6, ADDR, or ADRS	Address input
LSB	Least significant address bit
MSB	Most significant address bit
Pat. 1 through 10	Test pattern algorithms

6.4 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish C (see 3.3). Longer lead lengths and lead forming shall not affect the Part or Identifying Number (PIN).

6.5 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

Military device type	Generic-industry type
01 and 04	45H16, 4116, 2117, (200 ns access time)
02 and 05	45H16, 4116, 2117, (250 ns access time)
03	4116, (200 ns access time, page mode operation)

6.6 Handling. MOS devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. Input protection circuitry has been designed into the device to minimize the effect of this static buildup. However, the following handling practices are recommended:

a. Devices should be handled on benches with conductive and grounded surface.

b. Ground test equipment, tools, and operator.

c. Do not handle devices by the leads.

d. Store devices in conductive foam or carriers.

e. Avoid the use of plastic, rubber, or silk in MOS areas.

f. Maintain relative humidity above 50 percent, if practical.

6.7 Part or Identifying Number (PIN). The PIN shall be in accordance with MIL-M-38510, and as specified herein.

6.8 Application and operation guidelines.

6.8.1 Initialization. The device requires eight cycles after power up before it will operate properly. Any cycle that performs refresh may be used.

6.8.2 Addressing. Addressing 1 of 16,384(2^{14}) cells requires handling a 14-bit address word. This is accomplished with minimum pin count by multiplexing two 7-bit address fields onto the seven address inputs (A_0-A_6). The two fields are brought on chip in succession by the high to low transition of the row address information on chip for decoding.

6.8.3 Read operation. When a valid row address is presented to the address inputs, the row address strobe ($\overline{RAS}$) can fall and thereby clock the row address into the address latches. After a row address hold time (t_{RAH}), the column address can be presented to the device and the column address strobe ($\overline{CAS}$) can fail to latch the column address onto the chip. The $\overline{WRITE}$ input is held at a logic "1" (high) level. The output is in the high impedance state and will remain in that state until access time. At access time it will turn on and assume the appropriate level ("1" or "0"). A feature referred to as "Gated $\overline{CAS}$" is simply a delayed internal signal that is gated with the external $\overline{CAS}$ signal which causes the on chip $\overline{CAS}$ clock to occur at a fixed interval after $\overline{RAS}$. This allows $\overline{CAS}$ to become active (low) any time after row address hold time (t_{RAH}) has been satisfied but before the maximum $\overline{RAS}$ to $\overline{CAS}$ delay time (t_{RCD}) without affecting access time referenced to $\overline{RAS}$ (t_{RAC}). $\overline{CAS}$ can occur later than t_{RCD} maximum without affecting device operation but access time will be controlled exclusively by $\overline{CAS}$ which is access time referenced to $\overline{CAS}$ (t_{CAC}).

6.8.4 Write operation. The same procedure applies for latching the address information on chip that was explained for the read operation. Data can be written into the device in several ways. In all cases, however, writing is accomplished by the falling edge of $\overline{CAS}$ or $\overline{WRITE}$ (while $\overline{RAS}$ is low) whichever occurs latest. Data is latched onto the chip.

a. Early write - Data in and $\overline{WRITE}$ precede the fall of $\overline{CAS}$ by a setup time (t_{DS} and t_{WCS}, respectively) and remain valid for a hold time t_{DH} and t_{WCH}). The setup and hold times are with respect to the falling edge of $\overline{CAS}$. Data out remains in the high impedance state for the entire cycle.

b. Late write - The fall of $\overline{WRITE}$ occurs after data in and $\overline{CAS}$ by a specified time ($\overline{CAS}$ to $\overline{WRITE}$ delay t_{CWD}). Data in setup and hold times are referenced to the fall of $\overline{WRITE}$. Data out will contain data from the selected cell at access time. If the fall of $\overline{WRITE}$ occurs prior to the $\overline{CAS}$ to $\overline{WRITE}$ delay limit, the state of the data out pin is indeterminate.

6.8.5 Page mode operation. The 16K dynamic RAM can be operated in the "Page Mode" manner. The is, for each row address issued, several column addresses can be issued before a new row address is required. The sequence calls for issuing a row address strobe followed by a number of column addresses and strobes while holding the row address strobe low. Writing occurs in a normal fashion in relation to $\overline{CAS}$ as was described earlier. The user must adhere to the refresh requirements and the maximum pulse width requirements for the $\overline{RAS}$ clock.

6.8.6 Refresh operations. The basic device constraint is that no cell shall be refreshed at intervals exceeding 1.0 millisecond. There are 128 cells along each row in the storage matrix and there are 128 such rows. A normal read or refresh cycle refreshes 128 cells in a row simultaneously. A row address 128 cycle "burst" every millisecond or a single distributed cycle every 7.812 microsecond at each of the 128 row addresses will accomplish complete memory refreshing. A refresh cycle can be accomplished in two ways. Either a normal read cycle or a "$\overline{RAS}$ only" cycle will accomplish refresh. The $\overline{RAS}$ only refresh requires less power than a standard $\overline{RAS}/\overline{CAS}$ cycle.

6.9 Changes from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of the changes.

APPENDIX

FUNCTIONAL ALGORITHMS

Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion.

NOTE: Step 1 of all algorithms may be performed initially and if testing is continuous (no dead time exceeding 5 ms between tests), step 1 does not have to be repeated for each algorithm.

PATTERN 1

ADDRESS COMPLEMENT, DATA BACKGROUND = Y-BAR

This pattern produces a checkerboard and its complement in an inter-digitated array. It produces maximum address line noise and checks the decoder dynamic response times. It is performed in the following manner:

Step 1 - Perform 8 pump cycles
Step 2 - Load memory with background data
Step 3 - Read entire memory (DATA verification)
Step 4 - Read minimum address location
Step 5 - Read maximum address location
Step 6 - Read location minimum +1
Step 7 - Read location minimum -1
Step 8 - Continue incrementing and decrementing from minimum and maximum locations until all locations have been read
Step 9 - Repeat steps 2 through 8 with complement data

Test time = 3N x cycle time + 8 cycles

PATTERN 2

SHIFTING DIAGONAL, INITIAL DATA BACKGROUND = MAJOR DIAGONAL

This pattern is a good test for sense line imbalance and response plus restore noise in addition to multiple selection. It is performed in the following manner:

Step 1 - Perform 8 pump cycles
Step 2 - Load memory with data background, scan from minimum location to maximum location
Step 3 - Read data in the memory, scan from maximum location to minimum location
Step 4 - Repeat steps 2 and 3, each time shifting the diagonal by one until it has occupied every position in the memory (128 load/read scans)
Step 5 - Repeat steps 2 through 4 with complement data

Test time = 256N x cycle time + 8 cycles

PATTERN 3

MARCH DATA, DATA BACKGROUND = ALL "0"

This pattern tests for address uniqueness and multiple selection. It is performed in the following manner:

Step 1 - Perform 8 pump cycles
Step 2 - Load memory with background data
Step 3 - Read location 0
Step 4 - Write data complement in location 0
Step 5 - Read data complement in location 0
Step 6 - Repeat steps 3 through 5 for all other locations in the memory (sequentially)
Step 7 - Read data complement at maximum location
Step 8 - Write data at maximum location
Step 9 - Read data at maximum location
Step 10- Repeat steps 7 through 9 for all other locations in the memory (decrementing from maximum location to minimum location)
Step 11- Repeat steps 3 through 10 with data background of all "1"

Test time = 14N x cycle time + 8 cycles

PATTERN 4

STATIC REFRESH (PERIPHERY RETENTION)

This pattern tests for periphery retention time by attempting to write after a lengthy pause. This test is performed at 110°C (case) only, and is not used to measure the retention time of the periphery circuits, but to insure that they will hold for at least 5 ms. It is performed in the following manner:

Step 1 - Perform 8 pump cycles
Step 2 - Load memory with all "0's"
Step 3 - Read memory all "0's"
Step 4 - Pause (stop all clocks) 5 ms
Step 5 - Load memory with all "1's"
Step 6 - Read memory, all "1's"
Step 7 - Pause (stop all clocks) 5 ms
Step 8 - Load memory with all "0's"
Step 9 - Read memory, all "0's"

Test time = 6N x cycle time + 8 cycles + 10 ms

PATTERN 5

REFRESH TEST (CELL RETENTION)

This test is used to check the retention time of the memory cells under dynamic conditions. It is done at high temperature only and is performed in the following manner:

Step 1 - Perform 8 pump cycles
Step 2 - Load memory with DATA as shown in the following
Step 3 - Read entire memory (DATA verification)
Step 4 - Alternate reading between LOC.63 and LOC.64*
Step 5 - Read entire memory
Step 6 - Load memory with $\overline{\text{DATA}}$
Step 7 - Repeat steps 3 through 5

PATTERN 5 - Continued

REFRESH TEST (CELL RETENTION)

*Refresh (t_{REF}) = # reads x cycle time

```
          |000000000000000000000|
          |0                   0|
          |0     8K ARRAY      0|
          |0                   0|
          |000000000000000000000|
LOC.63    |111111111111111111111|

LOC.64    |111111111111111111111|
          |000000000000000000000|
          |0     8K ARRAY      0|
          |0                   0|
          |0                   0|
          |000000000000000000000|
```

PATTERN 6

EXTENDED CYCLE TEST (10 µs), DATA BACKGROUND = X-BAR

This test is used to verify the 10 µs maximum limit on $\overline{RAS}$ and $\overline{CAS}$ pulse widths. Front and back edge timing is held to normal cycle timing while the cycle is increased to allow 10 µs of $\overline{RAS}$ and $\overline{CAS}$ active time (low level). It is performed in the following manner:

Step 1 - Perform 8 pump cycles
Step 2 - Write data in location 0
Step 3 - Read data in location 0
Step 4 - Repeat steps 2 and 3 for all other locations in the memory (sequentially)
Step 5 - Repeat steps 2 through 4 with complement data

Test time = 4N x cycle time + 8 cycles

PATTERN 7

CONTINUOUS READ, DATA BACKGROUND = X-BAR

This pattern is used to allow the maximum amount of current (I_{CC}) 2/ to be drawn from the V_{CC} power supply. It is performed in the following manner with normal cycle timing:

Step 1 - Perform 8 pump cycles
Step 2 - Load memory with background data
Step 3 - Sequentially read entire memory
Step 4 - Repeat step 3 as many times as necessary to achieve a stabilized current reading

Test time - Undefined

2/ Also applies to I_{DD} and I_{BB} currents.

PATTERN 8

PAGE MODE, DATA BACKGROUND = ADDRESS PARITY

This pattern checks for device functionality during page mode operation. It is performed in the following manner:

Step 1 - Perform 8 pump cycles
Step 2 - Load memory with background data, normal cycle timing
Step 3 - Strobe in row address, hold $\overline{RAS}$ low
Step 4 - Write data complement in as many columns as possible for $\overline{RAS}$ active time of 10 μs
Step 5 - Strobe in same row address, hold $\overline{RAS}$ low
Step 6 - Read columns just written
Step 7 - Repeat steps 3 through 6 until all rows and columns have been checked
Step 8 - Complement background data and repeat steps 2 through 7

PATTERN 9

OUTPUT HIGH IMPEDANCE

This test checks for a high impedance state on the output when the device is de-selected. It is performed in the following manner:

Step 1 - Perform 8 pump cycles
Step 2 - Load memory with checkerboard, normal cycle
Step 3 - Hold $\overline{RAS}$ and $\overline{CAS}$ high
Step 4 - Wait 60 ns minimum
Step 5 - Measure output voltage (tristate voltage) +.2 V
Step 6 - Measure output voltage (tristate voltage) -.2 V

NOTE 1: Tristate voltage and wait time is dependent on output loading conditions. Using option 2 of figure 6 (switching time test circuit) with Vm = 4.5 V dc, tristate voltage shall be tested at +2.25 ±.2 V dc.

PATTERN 10

V_{BUMP}/V_{BOGGLE} DATA BACKGROUND = ALL "0" (discharged state)

This pattern indicates sense amplifier margin by slewing the supply voltage between memory writing and reading. It is performed in the following manner:

Step 1 - Perform 8 pump cycles
Step 2 - Pause 600 μs ramping V_{CC} to 4.5 V inhibiting all clocks
Step 3 - Load memory with background data
Step 4 - Pause 600 μs ramping V_{CC} to 5.5 V inhibiting all clocks
Step 5 - Read memory with background data
Step 6 - Repeat steps 2 through 5 for background data complement
Step 7 - Load memory with background data
Step 8 - Pause 600 μs ramping V_{CC} to 4.5 V inhibiting all clocks
Step 9 - Read memory with background data
Step 10- Pause 600 μs ramping V_{CC} to 5.5 V inhibiting all clocks
Step 11- Repeat steps 7 through 9 for background data complement

Test time = (8N + 8) x cycle time + 280 μs

CONCLUDING MATERIAL

Custodians:
Army - ER
Navy - EC
Air Force - 17

Review activities:
Army - AR, MI
Navy - OS, SH, TD
Air Force - 11, 19, 85, 99
DLA - ES

User activities:
Army - SM
Navy - AS, CG, MC

Preparing activity:
Air Force - 17

Agent:
DLA - ES

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