FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-11203-3E

MEMORY

CMOS 8M × 36 Bit SYNCHRONOUS DRAM MODULE

MB85502-012/-015

CMOS 8M × 36 Bit Synchronous DRAM Module

■ DESCRIPTION

The Fujitsu MB85502 is a fully decoded, CMOS Synchronous Dynamic Random Access Memory (SDRAM) module consisting of eighteen MB81116421 devices which organized as two banks of 2,097,152-word × 4-bit. The MB85502 organized as 8,388,608 × 36-bit is optimized for those applications requiring high speed, high performance, large memory shortage, and high density memory organizations.

This module is ideally suited for supercomputers, workstations, laser printers, high resolution graphic adapters, accelerators and other applications where a simple interface is needed.

The all inputs/ outputs are LVTTL compatible, and supply voltage tolerance is ±9%.

■ ABSOLUTE MAXIMUM RATINGS (See NOTE)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to +4.6	V *1
Input Voltage	V_{IN}	–0.5 to +4.6	V *1
Output Voltage	V_{OUT}	–0.5 to +4.6	V *1
Short Circuit Output Current	I_{OUT}	±50	mA
Power Dissipation	P_D	24	W
Storage Temperature	T_{STG}	–55 to +125	°C

*1 V_{SS} = 0 V

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

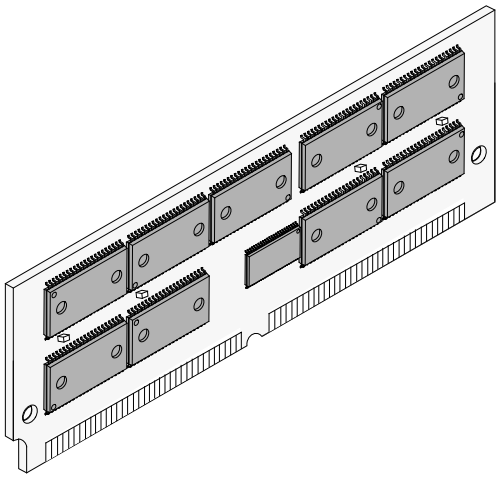
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

■ PRODUCT LINE & FEATURES

Parameter	MB85502-012	MB85502-015
Clock Frequency	84 MHz max.	67 MHz max.
Burst Mode Cycle Time	12 ns min.	15 ns min.
$\overline{RAS}$ Access Time	71 ns max.	79 ns max.
$\overline{CAS}$ Access Time	36 ns max.	39 ns max.
Output Valid From Clock (CL = 3)	13 ns max.	14 ns max.
Operating Current (Burst Mode)	6199 mW max.	5641 mW max.
Power Down Mode Current	436 mW max. (ADD=L)	

- 8M words × 36 bits (MB81116421 × 18)
- 72 pin socket type (pin pitch 1.27 mm)
- 84 MHz (Max.) data transfer
- +3.3 V±0.3 V supply voltage
- 4096 refresh cycles every 65.6 ms
- Dual bank operation
- LVTTL compatible I/O
- Programmable burst type
- Programmable burst length
- Auto and Self-refresh
- CKE power down mode
- Output Enable and Input Data Mask

■ PACKAGE

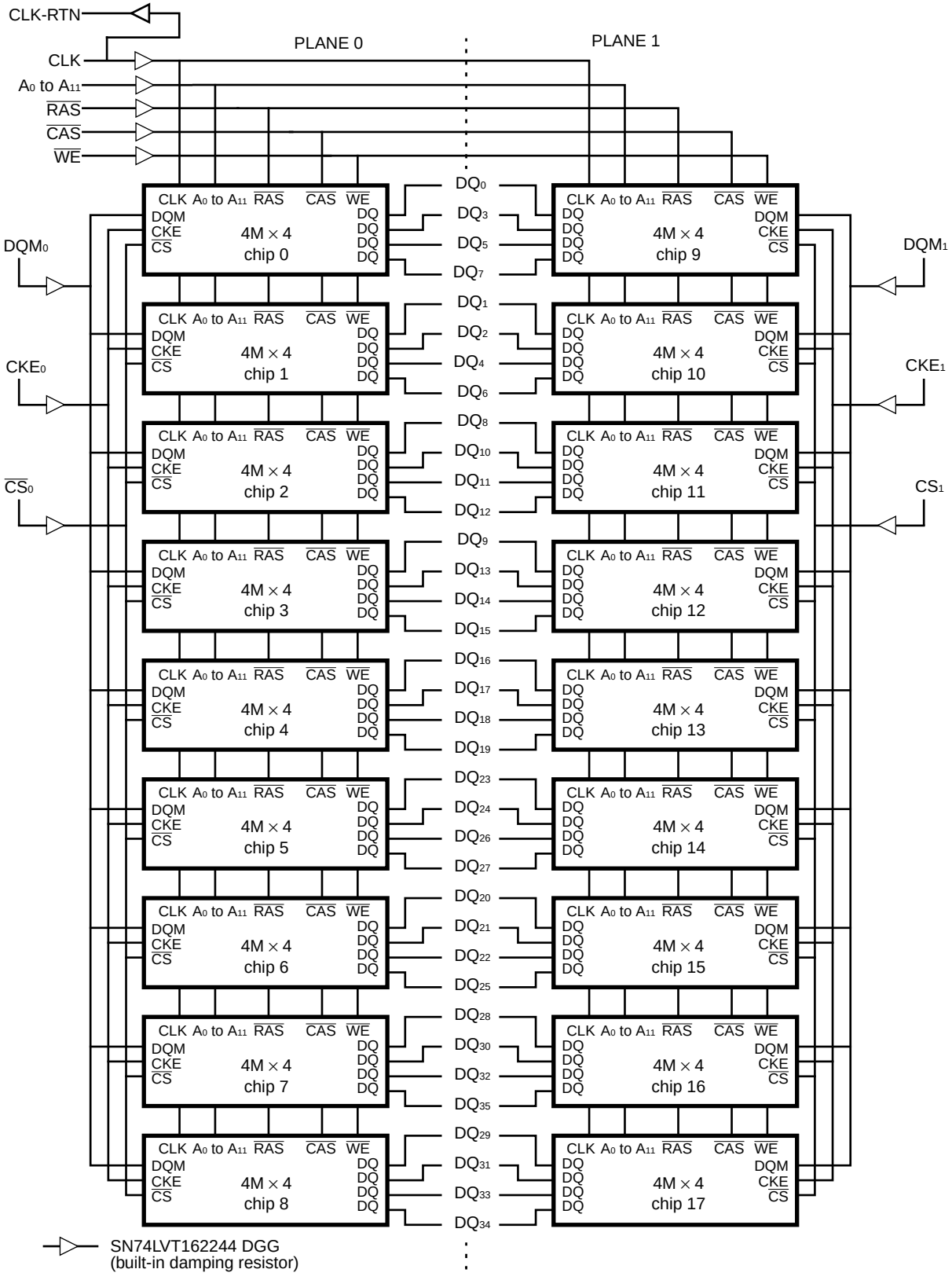


MSS-72P-P70

■ PIN ASSIGNMENT

DQ_0	2	1	V_{SS}
DQ_2	4	3	DQ_1
DQ_4	6	5	DQ_3
DQ_6	8	7	DQ_5
V_{CC}	10	9	DQ_7
DQ_9	12	11	DQ_8
DQ_{11}	14	13	DQ_{10}
DQ_{13}	16	15	DQ_{12}
DQ_{14}	18	17	V_{SS}
NC	20	19	DQ_{15}
$\overline{CS}_1$	22	21	$\overline{CS}_0$
A_2	24	23	A_3
V_{CC}	26	25	A_1
A_{10}	28	27	A_0
NC	30	29	A_{11}
$\overline{RAS}$	32	31	V_{SS}
$\overline{WE}$	34	33	$\overline{CAS}$
A_5	36	35	A_4
A_7	38	37	A_6
A_9	40	39	A_8
V_{SS}	42	41	NC
CKE_1	44	43	CKE_0
CLK	46	45	CLK-RTN
DQM_0	48	47	V_{CC}
DQ_{16}	50	49	DQM_1
DQ_{18}	52	51	DQ_{17}
DQ_{20}	54	53	DQ_{19}
V_{SS}	56	55	DQ_{21}
DQ_{23}	58	57	DQ_{22}
DQ_{25}	60	59	DQ_{24}
DQ_{26}	62	61	V_{CC}
DQ_{28}	64	63	DQ_{27}
DQ_{30}	66	65	DQ_{29}
DQ_{32}	68	67	DQ_{31}
DQ_{34}	70	69	DQ_{33}
V_{SS}	72	71	DQ_{35}

FUNCTIONAL BLOCK DIAGRAM



■ RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol		Value			Unit	Ambient Oprating Temp.
				Min.	Typ.	Max.		
Supply Voltage	*1	V_{CC}		3.0	3.3	3.6	V	0°C to +70 °C
		V_{SS}		0	0	0		
Input High Voltage, All Inputs	*1 *2	LVTTL	V_{IH}	2.0	—	V_{CC} +0.3	V	
Input Low Voltage, All Inputs	*1 *2		V_{IL}	–0.3	—	0.8	V	

*1: V_{SS} = 0 V.

*2: Ambient temp. depend on cycle time and cooling conditions.

Note: This figures are recommened value to guarantee LSI's normal operation.
Requirements of electric characteristics (DC/AD) is guaranteed within this value.

■ CAPACITANCE

(T_A = 25°C, f = 1 MHz, V_{CC} = +3.3 V)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance, A_0 to A_{11}	C_{IN1}	—	16	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	16	pF
Input Capacitance, CLK	C_{IN3}	—	16	pF
Input Capacitance, DQM_0, DQM_1	C_{IN4}	—	16	pF
Input Capacitance, CKE_0, CKE_1	C_{IN5}	—	16	pF
Input Capacitance, $\overline{CS_0}$, $\overline{CS_1}$	C_{IN6}	—	16	pF
I/O Capacitance, (DQ_0 to DQ_{35})	C_{DQ}	—	22	pF

■ DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Conditions	Value		Unit
				Min.	Max.	
Input Leakage Current	All inputs except DQ	I_{LI}	V_{IN} = 0 V	–10	10	µA
			V_{IN} = V_{CC}	–10	10	
Input Hold Current		$I_{I\ (Hold)}$	V_{IN} = 0.8 V	75	—	µA
			V_{IN} = 2 V	—	–75	
Output Leakage Current		I_{LO}	0 V ≤ V_{IN} ≤ V_{CC} Output high impedance	–20	20	µA
Output High Voltage 1	LVTTL	V_{OH}	I_{OH} = –2.0 mA	2.4	—	V
Output Low Voltage 1		V_{OL}	I_{OL} = +2.0 mA	—	0.4	V
Operating Current (Average Power Supply Current) 2	MB85502-012	I_{CC1S}	No Burst: t_{CK} = min. One bank active	—	1204 (169)	mA
	MB85502-015				1126 (136)	
	MB85502-012	I_{CC1D}	No Burst: t_{CK} = min. Two banks active	—	1588 (238)	mA
	MB85502-015				1451 (191)	
Precharge Standby Current (Power Supply Current) 2	ADD=Fix “L”	I_{CC2P}	CKE = V_{IL} Two banks idle t_{CK} = min. Power down mode	—	121 (103)	mA
	ADD=Fix “H”				117 (99)	
	ADD=Change				248 (230)	
	ADD=Fix “L”	I_{CC2N}	CKE = V_{IH} Two banks idle t_{CK} = min.	—	641 (102)	mA
	ADD=Fix “H”				639 (99)	
	ADD=Change				770 (230)	
Active Standby Current (Power Supply Current) 2	ADD=Fix “L”	I_{CC3P}	CKE = V_{IL} One bank active t_{CK} = min.	—	642 (103)	mA
	ADD=Fix “H”				639 (99)	
	ADD=Change				770 (230)	
	ADD=Fix “L”	I_{CC3N}	CKE = V_{IH} One bank active t_{CK} = min.	—	912 (102)	mA
	ADD=Fix “H”				909 (99)	
	ADD=Change				1040 (230)	
Burst Mode Current (Average Power Supply Current) 2	MB85502-012	I_{CC4}	t_{CK} = min.	—	1722 (327)	mA
	MB85502-015				1567 (262)	

(Continued)

■ DC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Conditions	Value		Unit
				Min.	Max.	
Refresh Current #1 (Average Power Supply Current) [2]	MB85502-012	I_{CC5S}	One bank active Auto-Refresh; t_{CK} = min., t_{RC}=min. ADD=Fix Low	—	1134 (99)	mA
	MB85502-015				1070 (80)	
	MB85502-012	I_{CC5D}	Two banks active Auto-Refresh; t_{CK} = min. t_{RC}=min., t_{RRD} = min. ADD=Fix Low	—	1463 (113)	mA
	MB85502-015				1351 (91)	
Refresh Current #2 (Average Power Supply Current) [2]		I_{CC6}	Self-Refresh; CKE = V_{IL} ADD=Fix Low	—	382 (103)	mA

1. V_{SS} = 0 V
2. I_{CC} depends on output pin, load condition and number of clock cycle.

Note: All figures except for I_{CC2} are value for one side(stand by = I_{CC2}) operation.
( ) shows supply consumption of driver, V_{IH} = V_{CC}.
ADD = change is the value of change at burst mode 84 MHZ.

■ AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

Parameter	Notes	Symbol	MB85502-012		MB85502-015		Unit
			Min.	Max.	Min.	Max.	
Clock Period	CAS latency = 3	t_{CK}	12	100	15	100	ns
4	CAS latency = 2		17.5		20		ns
	CAS latency = 1		35		40		ns
Clock High Time		t_{CH}	4	—	4	—	ns
Clock Low Time		t_{CL}	4	—	4	—	ns
$\overline{CS}$ Setup Time		t_{SC}	3	—	3	—	ns
$\overline{CS}$ Hold Time		t_{HC}	3	—	3	—	ns
Input Setup Time		t_{SI}	3	—	3	—	ns
Input Hold Time		t_{HI}	3	—	3	—	ns
Data Input Setup Time*		t_{SID}	0	—	0	—	ns
Data Input Hold Time*		t_{HID}	7	—	7	—	ns
Output Valid from Clock (t_{CLK} = min.)	CAS latency = 3	t_{AC}	—	13	—	14	ns
5, 6	CAS latency = 2			18.5		20	ns
	CAS latency = 1			36		39	ns
Output in Low-Z		t_{OLZ}	5	—	5	—	ns
Output in High-Z		t_{OHZ}	4	17	4	20	ns
Output Hold Time 7		t_{OH}	4	—	4	—	ns
Time between Refresh		t_{REF}	—	65.6	—	65.6	ms
Transition Time		t_T	0.5	2	0.5	2	ns
Power Down Exit Time		t_{PDE}	15	—	18	—	ns

* : DQ_0 to DQ_{35} (D_{IN} input)

■ AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

BASE VALUES FOR CLOCK COUNT/LATENCY

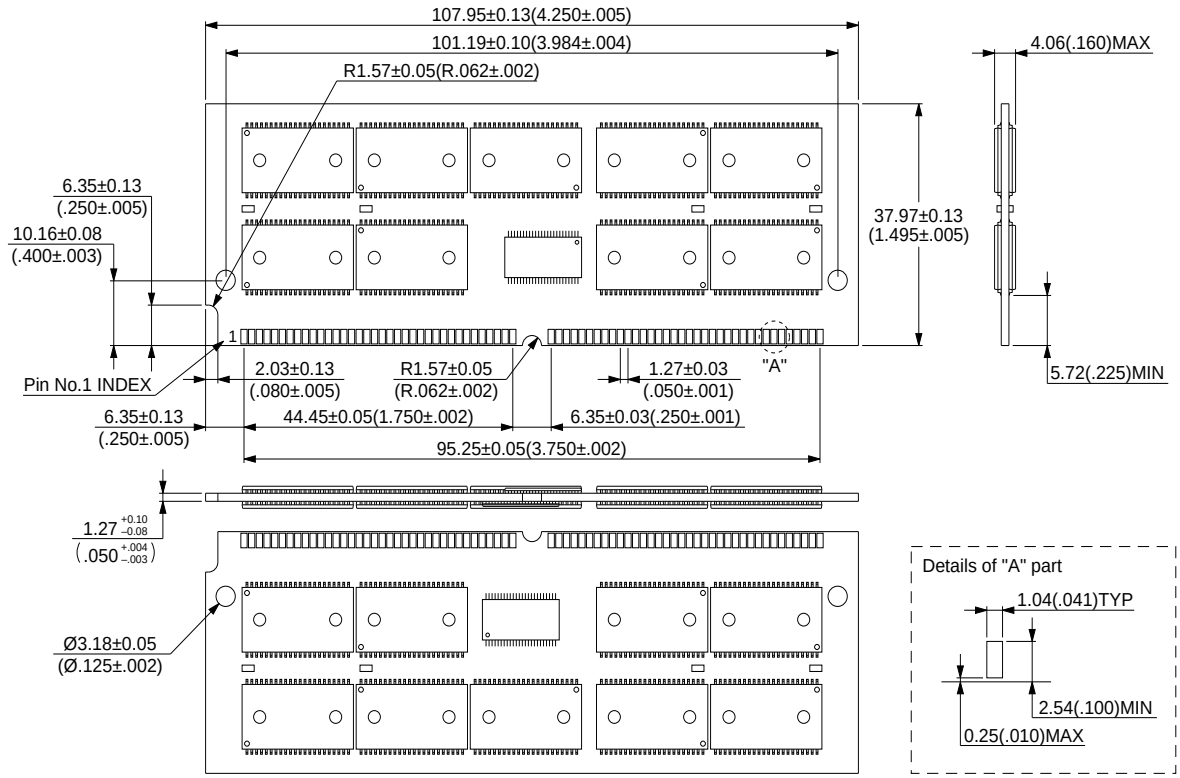
Parameter	Notes	Symbol	MB85502-012		MB85502-015		Unit
			Min.	Max.	Min.	Max.	
$\overline{RAS}$ Cycle Time	8	t_{RC}	110	—	120	—	ns
$\overline{RAS}$ Access Time	9	t_{RAC}	—	71	—	79	ns
$\overline{CAS}$ Access Time	10, 12	t_{CAC}	—	36	—	39	ns
$\overline{RAS}$ Precharge Time		t_{RP}	40	—	40	—	ns
$\overline{RAS}$ Active Time		t_{RAS}	70	10000	80	10000	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11	t_{RCD}	35	—	40	—	ns
Write Recovery Time		t_{WR}	20	—	25	—	ns
$\overline{RAS}$ to $\overline{CAS}$ Bank Active Delay Time		t_{RRD}	35	—	40	—	ns

Notes: 1. An initial pause (DESL on NOP) of 200 µs is required after power-up followed by a minimum of eight Auto-Refresh cycles.
2. 1.4 V or V_{REF} is the reference level for measuring timing of input signals. Transition times are measured between V_{IH} (min.) and V_{IL} (max.).
3. AC characteristics assume t_T = 1 ns and 30 pF of capacitive load.
4. Maximum value is a reference value and a device may work at a slower untested clock rate.
5. Assumes t_{RCD} and t_{CAC} are satisfied.
6. t_{AC} also specifies the access time at burst mode except for first access.
7. Specified where output buffer is no longer driven.
8. Actual clock count of t_{RC} (l_{RC}) will be sum of clock count of t_{RAS} (l_{RAS}) and t_{RP} (l_{RP}).
9. t_{RAC} is a reference value. Maximum value is obtained from the sum of t_{RCD} (min.) and t_{CAC} (max.).
10. Assumes t_{RAC} and t_{AC} are satisfied.
11. Operation within the t_{RCD} (min.) ensures that t_{RAC} can be met; if t_{RCD} is greater than the specified t_{RCD} (min.), access time is determined by t_{CAC} or t_{AC}.
12. l_{CAC} is programmed at mode register.

*Source: See MB81116421 Data Sheet for detailes on the electricals.

■ PACKAGE DIMENSIONS

72 pin, Plastic SIMM
(MSS-72P-P70)



Dimensions in mm(inches).

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