Index of /ds/NM/

Name	Last modified	Size	Description
Parent Directory			
NM24C00.pdf	07-Aug-98 00:00	83K	
NM24C02.pdf	09-Feb-00 00:00	104K	
NM24C02U.pdf	22-Dec-99 00:13	99K	
NM24C02U_NM24C03U.pdf	22-Dec-99 00:13	99K	
NM24C02_03.pdf	09-Feb-00 00:00	104K	
NM24C03.pdf	09-Feb-00 00:00	104K	
NM24C03U.pdf	22-Dec-99 00:13	99K	
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NM24C04U.pdf	22-Dec-99 00:13	89K	
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NM24W04.pdf	22-Dec-99 00:13	104K
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NM25C640.pdf	22-Dec-99 00:13	93K
NM25CO20.pdf	07-Aug-98 00:00	103K
NM25CO40.pdf	11-Aug-98 00:00	103K
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NM27LV210.pdf	22-Dec-99 00:13	77K
NM34C02.pdf	22-Dec-99 00:13	90K
NM34W02.pdf	22-Dec-99 00:13	93K
NM93C06.pdf	22-Dec-99 00:13	88K
NM93C46.pdf	22-Dec-99 00:13	90K
NM93C46A.pdf	22-Dec-99 00:13	98K
NM93C56.pdf	22-Dec-99 00:13	89K
NM93C56A.pdf	22-Dec-99 00:13	104K
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NM93C86AU.pdf	15-May-99 00:00	83K
NM93CS06.pdf	09-Feb-00 00:00	164K
NM93CS46.pdf	09-Feb-00 00:01	163K
NM93CS56.pdf	09-Feb-00 00:01	163K
NM93CS66.pdf	09-Feb-00 00:01	163K
NM95HS01.pdf	06-Oct-98 16:47	144K
NM95HS02.pdf	06-Oct-98 16:47	144K
NM95MS14.pdf	06-Oct-98 16:47	112K
NM95MS15.pdf	06-Oct-98 16:47	117K
NM95MS16.pdf	22-Dec-99 00:13	138K
NM95MS18.pdf	31-Aug-98 10:58	140K
NMC27C16B.pdf	22-Dec-99 00:13	71K
NMC27C32B.pdf	22-Dec-99 00:13	70K

NMC27C64.pdf	22-Dec-99 00:13	82K
NMT2222.pdf	22-Dec-99 00:13	160K
NMT2907.pdf	22-Dec-99 00:13	58K

FAIRCHILD SEMICONDUCTOR™

PRELIMINARY

July 1998

NM24C00 – 512-Bit Standard 2-Wire Bus Interface Serial EEPROM

General Description

The NM24C00 devices are 512 bits of CMOS non-volatile electrically erasable memory. This device conforms to all specifications in the I²C™ 2-wire protocol and is designed to minimize device pin count, and simplify PC board layout requirements.

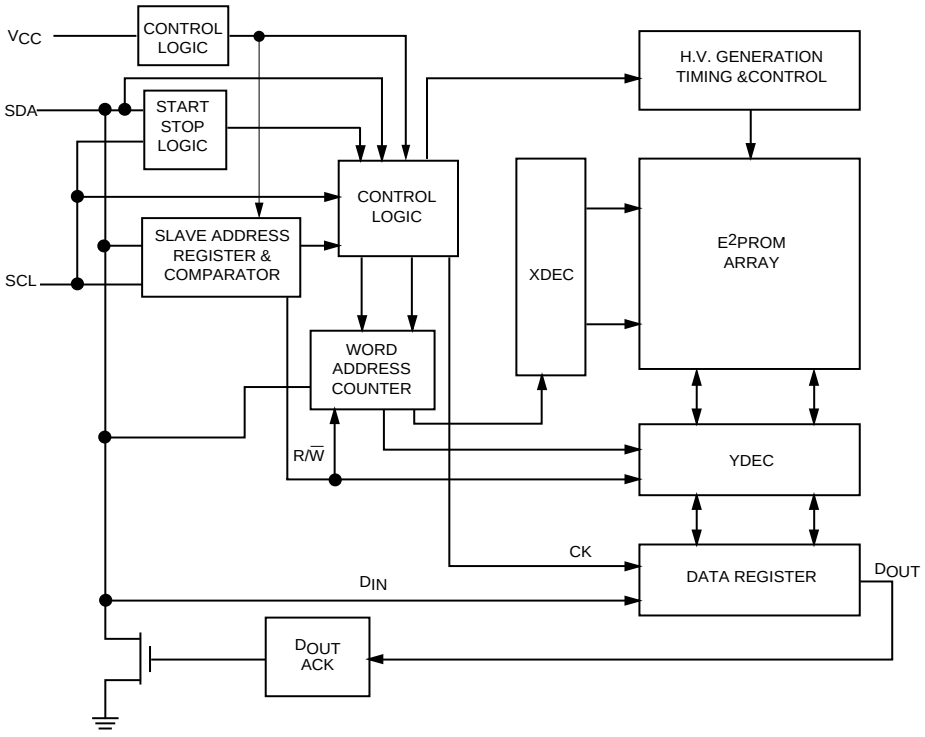
This communications protocol uses CLOCK (SCL) and DATA I/O (SDA) lines to synchronously clock data between the master (for example a microprocessor) and the slave EEPROM device(s).

Fairchild EEPROMs are designed and tested for applications requiring high endurance, high reliability and low power consumption.

Features

- Extended operating voltage 2.7V – 5.5V
- 400 kHz clock frequency (F)
- 500µA active current typical
  10µA standby current typical
  1µA standby typical (L)
  0.1µA standby typical (LZ)
- I²C compatible interface
  – Provides bidirectional data transfer protocol
- Self timed write cycle
  Typical write cycle time of 6ms
- Endurance: 1,000,000 data changes
- Data retention greater than 40 years
- Packages available: 8-pin SO and 8-pin TSSOP
- Internal ERASE/WRITE logic is disabled if V_{CC} is below 3.8V (V_{CC} = 5 ± 10%). Available on the 5V version NM24C00 (only).

Block Diagram



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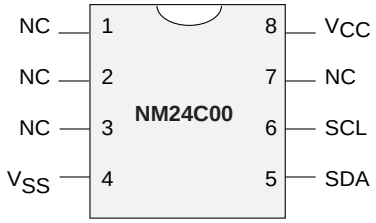
Connection Diagrams

SO Package (M8) and TSSOP Package (MT8)



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Top View
See Package
Number M08A and MTC8

Pin Names

V_{SS}	Ground
SDA	Data I/O
SCL	Clock Input
NC	No Internal Connection
V_{CC}	Power Supply

Ordering Information

								Letter	Description
							Package	M8	8-pin SOIC
								MT8	8-pin TSSOP
						Temp. Range		None	0 to 70°C
								V	-40 to +125°C
								E	-40 to +85°C
					Voltage Operating Range			Blank	4.5V to 5.5V
								L	2.7V to 5.5V
								LZ	2.7V to 5.5V and <1µA Standby Current
				SCL Clock Frequency				Blank	100KHz
								F	400KHz
			Density					00	512bit
		C						C	CMOS Technology
	24						**Interface**	24	IIC - 2 Wire
NM								**NM**	**Fairchild Non-Volatile Memory**

Absolute Maximum Ratings

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltages with Respect to Ground	6.5V to –0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min.

Operating Conditions

Ambient Operating Temperature	
NM24C00	0°C to +70°C
NM24C00E	-40°C to +85°C
NM24C00V	-40°C to +125°C
Positive Power Supply	
NM24C00	4.5V to 5.5V
NM24C00L	2.7V to 5.5V
NM24C00LZ	2.7V to 5.5V

Standard V_{CC} (4.5V to 5.5V) DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		0.5	1.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		10	50	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	1	µA
V_{IL}	Input Low Voltage		–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Low V_{CC} (2.7V to 5.5V) DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		0.5	1.0	mA
I_{SB} (Note 2)	Standby Current for L Standby Current for LZ	V_{IN} = GND or V_{CC} V_{IN} = GND or V_{CC}		1 0.1	10 1	µA µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	1	µA
V_{IL}	Input Low Voltage		–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Capacitance T_A = +25°C, f = 1.0 MHz, V_{CC} = 5V (Note 1)

Symbol	Test	Conditions	Max	Units
$C_{I/O}$	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN}	Input Capacitance (A0, A1, A2, SCL)	V_{IN} = 0V	6	pF

AC Conditions of Test

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10 ns
Input & Output Timing Levels	V_{CC} x 0.5
Output Load	1 TTL Gate and C_L = 100 pF

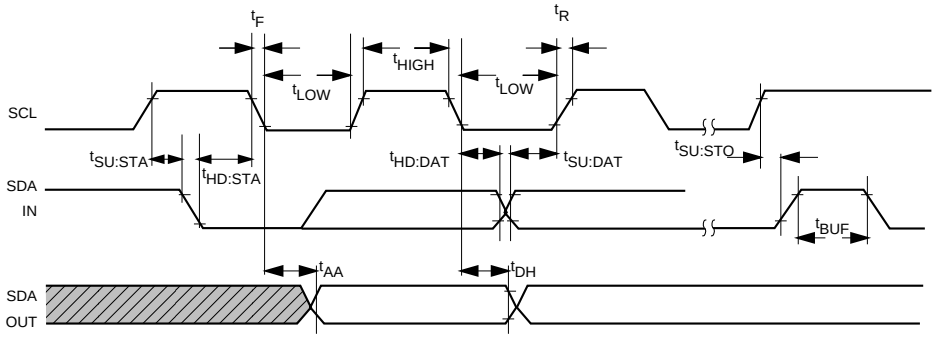
Note 1: Typical values are for T_A = 25°C and nominal supply voltage (5V).

Read and Write Cycle Limits (Standard and Low V_{CC} Range - 2.7V-5.5V)

Symbol	Parameter	100 kHz		400kHz		Units
		Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		100		400	kHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs (Minimum V_{IN} Pulse width)		100		50	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	0.1	0.9	µs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		1.3		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		0.6		µs
t_{LOW}	Clock Low Period	4.7		1.5		µs
t_{HIGH}	Clock High Period	4.0		0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		µs
$t_{HD:DAT}$	Data in Hold Time	0		0		µs
$t_{SU:DAT}$	Data in Setup Time	250		100		ns
t_R	SDA and SCL Rise Time		1		0.3	µs
t_F	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		0.6		µs
t_{DH}	Data Out Hold Time	300		50		ns
t_{WR} (Note 2)	Write Cycle Time - NM24C00 - NM24C00L, NM24C00LZ		10 15		10 15	ms

Note 2: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the NM24C00 bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

BUS TIMING



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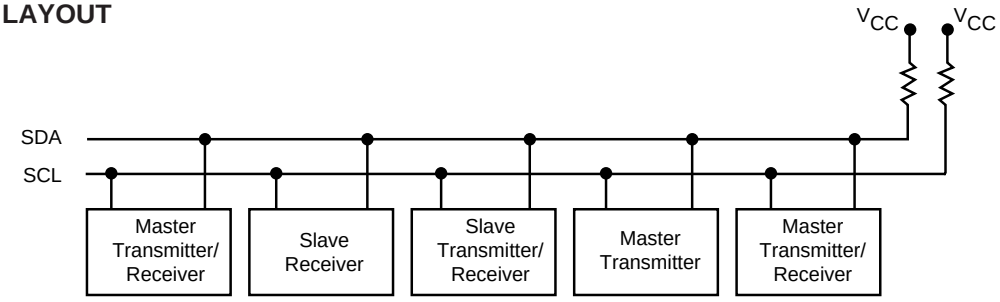
SYSTEM LAYOUT



Note 3: Due to open drain configuration of SDA, a bus-level pull-up resistor is called for, (typical value = 4.7 kΩ)

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DEFINITIONS	
WORD	8 bits (byte) of data
MASTER	Any I^2C device CONTROLLING the transfer of data (such as a microprocessor)
SLAVE	Device being controlled (EEPROMs are always considered Slaves)
TRANSMITTER	Device currently SENDING data on the bus (may be either a Master or Slave).
RECEIVER	Device currently receiving data on the bus (Master or Slave)

Pin Descriptions

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

SDA Serial Data

This is a bi-directional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pull-up resistor to V_{CC}.

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

Noise Protection

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

Device Operation

The NM24C00 supports a bi-directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the NM24C00 works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

Bus Characteristics

The following bus protocol has been defined:

1. Data transfer may be initiated only when the bus is not busy.
2. During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 1).

Bus not Busy

Both data and clock lines remain HIGH.

Start Condition

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGh determines a START condition. All commands must be preceded by a START condition.

Stop Condition

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited.

Bus Characteristics (Continued)

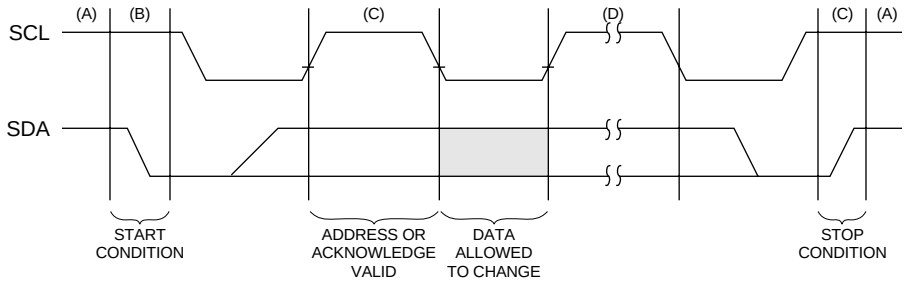
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The NM24C00 does not generate any acknowledge bits if an internal programming cycle is in progress,

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that ha been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition (Figure 2).

DATA TRANSFER SEQUENCE ON THE SERIAL BUS (Figure 1)



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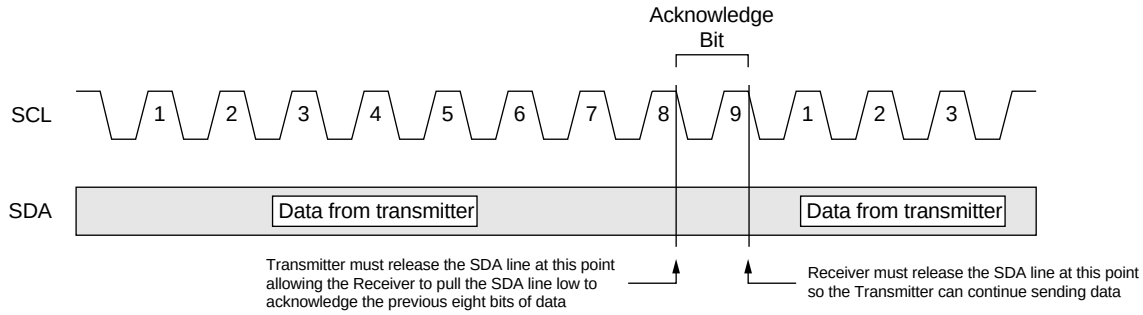
ACKNOWLEDGE TIMING (Figure 2)



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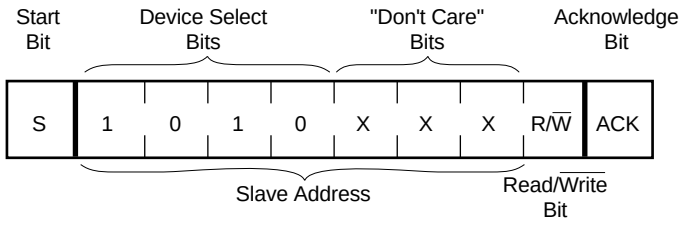
Device Addressing

After generating a START condition, the bus master transmits a control byte consisting of a slave address and an R/$\overline{W}$ bit that indicates what type of operation is to be performed. The slave address for the NM24C00 consists of a 4-bit device code (1010) followed by three "don't care" bits.

The last bit of the control byte determines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected (Figure 3). The NM24C00 monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

CONTROL BYTE FORMAT (FIGURE 3)



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Write Operations

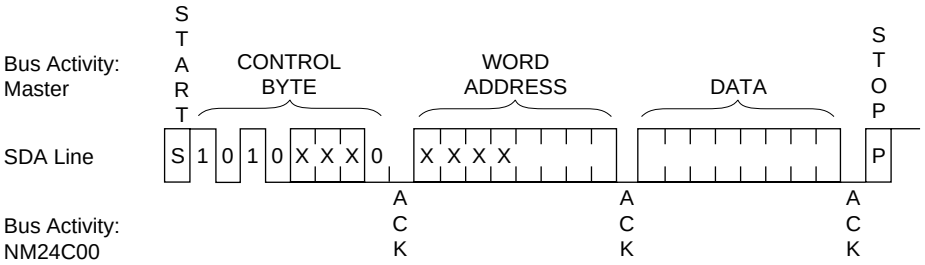
Byte Write

Following the start signal from the master, the device code (4 bits), the "don't care" bits (3 bits), and the R/W bit (which is a logic low) are placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after is has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the NM24C00. Only the lower six address bits are used by the device, and the upper four bits are "don't cares." The NM24C00 will acknowledge the address byte and the master device will then transmit the data word to be written into the addressed memory location. The NM24C00 acknowledges again and the master generates a stop condition. This intiates the internal write cycle, and during this time the NM24C00 will not generate acknowledge signals (Figure 4) . After a byte write command, the interal address counter will not be incremented and will point to the same address location that was just written. If a stop bit is transmitted to the device at any point in the write command sequence before the entire sequence is complete, then the command will abort and no data will be written. If more than 8 data bits are transmitted before the stop bit is sent, then the device will clear the previously loaded byte and begin loading the data buffer again. If more than one data byte is transmitted to the device and a stop bit is sent before a fill eight data bits have been transmitted, then the write command will abort and no data will be written. The NM24C00M8/MT8 employs a V_{CC} threshold detector circuit which disables the internal programming circuit if V_{CC} is below 3.8V.

Low V_{CC} Lockout

NM24C00 provides data security against inadvertent writes that could potentially happen during the time the device is being powered on, powered down and brown out conditions by monitoring the V_{CC} voltage during a write cycle. Whenever a write cycle is started, the built-in circuitry starts to monitor the V_{CC} level throughout the duration of the write command sequence until the master issues the required STOP condition to start the actual internal write operation. If the sensed V_{CC} voltage is below 3.8V at any point during this monitoring period, the device prohibits the write operation and does not generate the ACK pulse. This low V_{CC} lockout feature is only available for standard 5V device.

BYTE WRITE (FIGURE 4)



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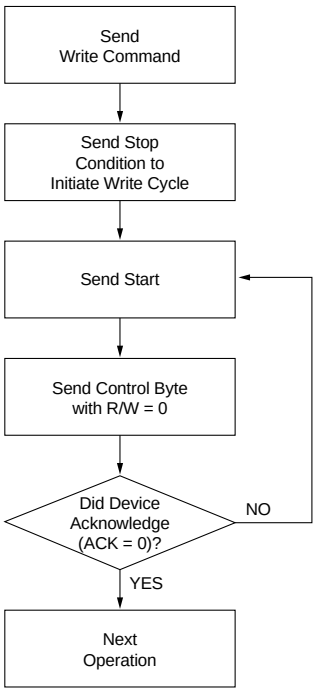
X = "Don't Care" Bit

Acknowledge Polling

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/W = 0). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, then the start bit and control byte must be re-sent. If the cycle is complete,. then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5 for flow diagram.

ACKNOWLEDGE POLLING FLOW (FIGURE 5)



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Read Operations

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

Current Address Read

The NM24C00 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous read operation was tp address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with the R/$\overline{W}$ bit set to one, the device issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the device discontinues transmission (Figure 6).

Random Read

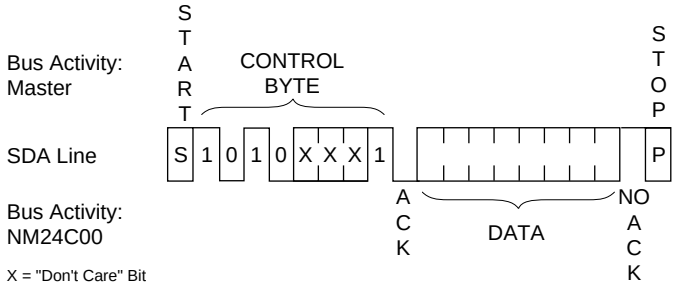
Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the device as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The NM24C00 will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the device discontinues transmission (Figure 7). After this command, the internal address counter will point to the address location following the one that was just read.

Sequential Read

Sequential reads are initiated in the same was as a random read except that after the device transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the device to transmit the next sequentially addressed 8-bit word (Figure 8).

To provide sequential reads the NM24C00 contains an internal address pointer which is incrmented by one at the completion of each read operation. This address pointer allows the entire memory to be serially read during one operation.

CURRENT ADDRESS READ (Figure 6)



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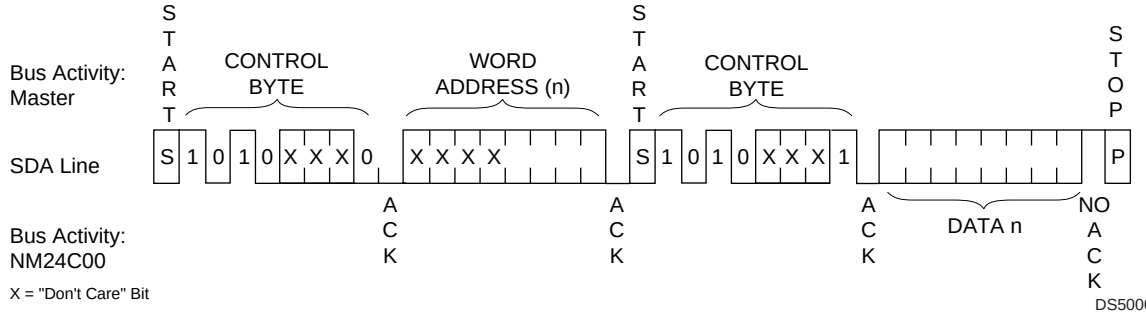
RANDOM READ (Figure 7)



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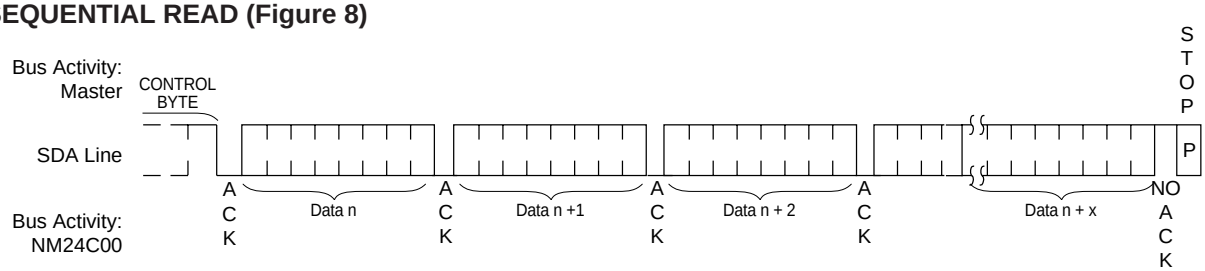
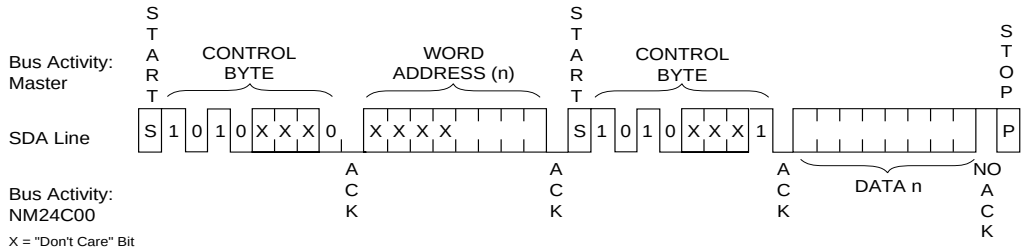
SEQUENTIAL READ (Figure 8)



DS500068-14

Read Operations (Continued)

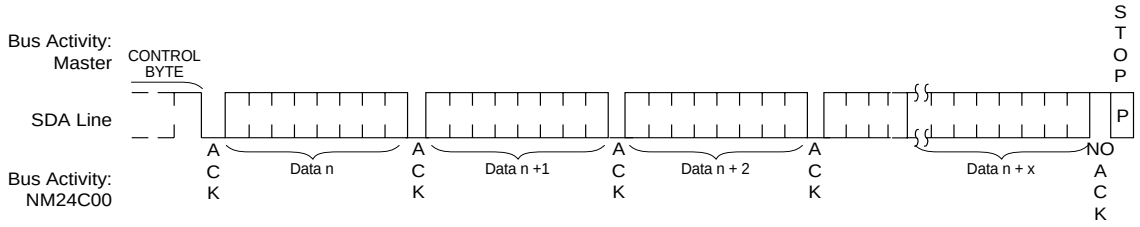
Random Read (Figure 9)



X = "Don't Care" Bit

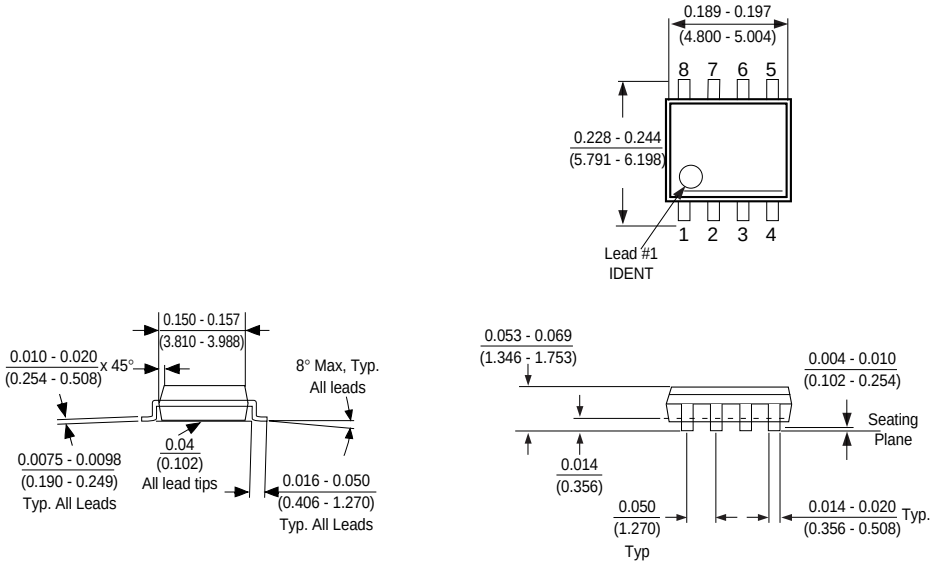
DS500068-18

Sequential Read (Figure 10)



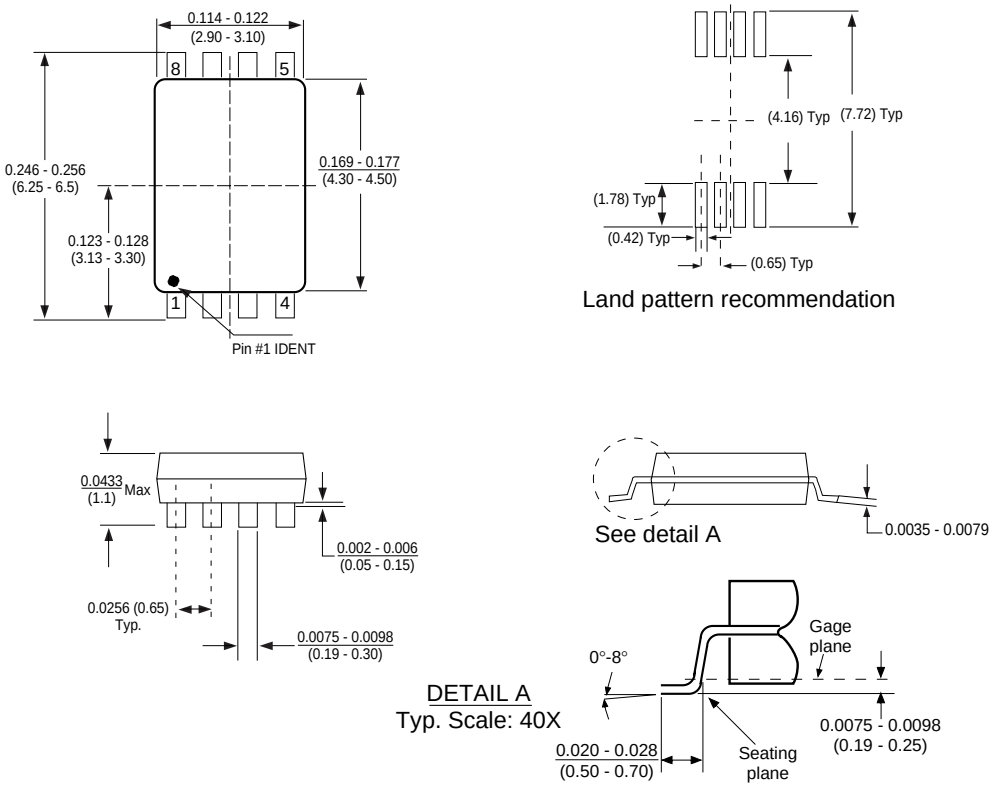
DS500068-19

Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin Molded Small Outline Package (M8)
Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted



Notes: Unless otherwise specified
1. Reference JEDEC registration MO153. Variation AA. Dated 7/93

8-Pin Molded TSSOP, JEDEC (MT8)
Package Number MTC08

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

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FAIRCHILD
SEMICONDUCTOR™

February 2000

NM24C02/03 – 2K-Bit Standard 2-Wire Bus Interface Serial EEPROM

General Description

The NM24C02/03 devices are 2048 bits of CMOS non-volatile electrically erasable memory. These devices conform to all specifications in the Standard IIC 2-wire protocol and are designed to minimize device pin count, and simplify PC board layout requirements.

The upper half (upper 1Kbit) of the memory of the NM24C03 can be write protected by connecting the WP pin to V_{CC}. This section of memory then becomes unalterable unless WP is switched to V_{SS}.

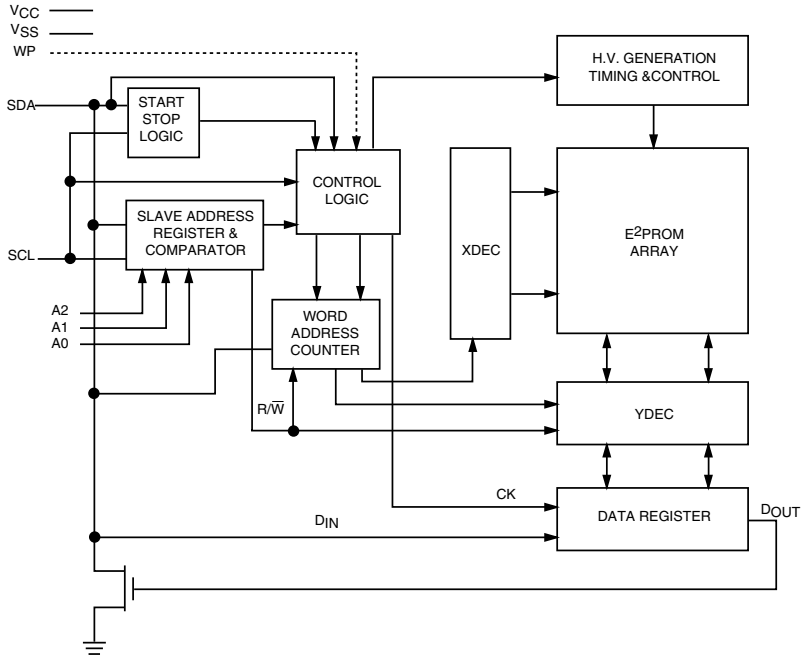
This communications protocol uses CLOCK (SCL) and DATA I/O (SDA) lines to synchronously clock data between the master (for example a microprocessor) and the slave EEPROM device(s). The Standard IIC protocol allows for a maximum of 16K of EEPROM memory which is supported by the Fairchild family in 2K, 4K, 8K, and 16K devices, allowing the user to configure the memory as the application requires with any combination of EEPROMs. In order to implement higher EEPROM memory densities on the IIC bus, the Extended IIC protocol must be used. (Refer to the NM24C32 or NM24C65 datasheets for more information.)

Fairchild EEPROMs are designed and tested for applications requiring high endurance, high reliability and low power consumption.

Features

- Extended operating voltage 2.7V – 5.5V
- 400 KHz clock frequency (F) at 2.7V - 5.5V
- 200µA active current typical
  10µA standby current typical
  1µA standby current typical (L)
  0.1µA standby current typical (LZ)
- IIC compatible interface
  – Provides bi-directional data transfer protocol
- Schmitt trigger inputs
- Sixteen byte page write mode
  – Minimizes total write time per byte
- Self timed write cycle
  Typical write cycle time of 6ms
- Hardware Write Protect for upper half (NM24C03 only)
- Endurance: 1,000,000 data changes
- Data retention greater than 40 years
- Packages available: 8-pin DIP, 8-pin SO, and 8-pin TSSOP
- Available in three temperature ranges
  - Commercial: 0° to +70°C
  - Extended (E): -40° to +85C
  - Automotive (V): -40° to +125°C

Block Diagram



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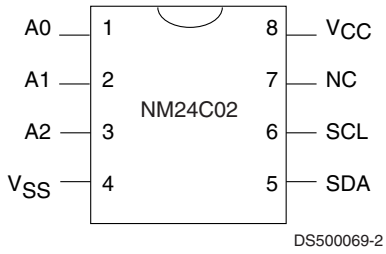
Connection Diagrams

Dual-in-Line Package (N), SO Package (M8) and TSSOP Package (MT8)

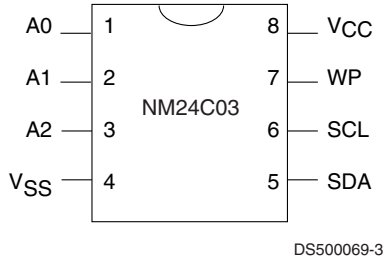


See Package Number N08E, M08A and MTC08

Pin Names

A0,A1,A2	Device Address Inputs
V_{SS}	Ground
SDA	Serial Data I/O
SCL	Serial Clock Input
NC	No Connection
V_{CC}	Power Supply

Dual-in-Line Package (N), SO Package (M8) and TSSOP Package (MT8)

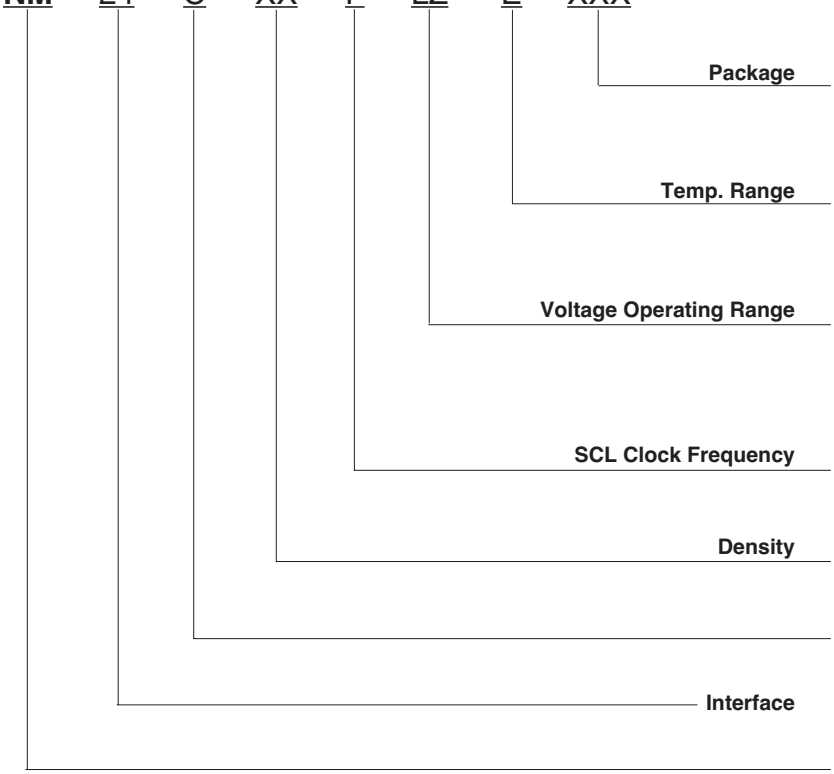


See Package Number N08E, M08A and MTC08

Pin Names

A0,A1,A2	Device Address Inputs
V_{SS}	Ground
SDA	Serial Data I/O
SCL	Serial Clock input
WP	Write Protect
V_{CC}	Power Supply

Ordering Information



	Letter	Description
Package	N	8-pin DIP
	M8	8-pin SOIC
	MT8	8-pin TSSOP
Temp. Range	None	0 to 70°C
	V	-40 to +125°C
	E	-40 to +85°C
Voltage Operating Range	Blank	4.5V to 5.5V
	L	2.7V to 5.5V
	LZ	2.7V to 5.5V and <1μA Standby Current
SCL Clock Frequency	Blank	100KHz
	F	400KHz
Density	02	2K
	03	2K with Write Protect
	C	CMOS Technology
Interface	24	IIC
	NM	**Fairchild Non-Volatile Memory**

Product Specifications

Absolute Maximum Ratings

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltages with Respect to Ground	6.5V to –0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min.

Operating Conditions

Ambient Operating Temperature	
NM24C02/03	0°C to +70°C
NM24C02E/03E	-40°C to +85°C
NM24C02V/03V	-40°C to +125°C
Positive Power Supply	
NM24C02/03	4.5V to 5.5V
NM24C02L/03L	2.7V to 5.5V
NM24C02LZ/03LZ	2.7V to 5.5V

DC Electrical Characteristics (2.7V to 5.5V)

Symbol	Parameter	Test Conditions		Limits			Units
				Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 400 KHz f_{SCL} = 100 KHz			0.2	1.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}	V_{CC} = 2.7V - 5.5V V_{CC} = 2.7V - 5.5V (L) V_{CC} = 2.7V - 4.5V (LZ)		10 1 0.1	50 10 1	µA µA µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}			0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}			0.1	1	µA
V_{IL}	Input Low Voltage			–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA				0.4	V

Capacitance T_A = +25°C, f = 100/400 KHz, V_{CC} = 5V (Note 2)

Symbol	Test	Conditions	Max	Units
$C_{I/O}$	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN}	Input Capacitance (A0, A1, A2, SCL)	V_{IN} = 0V	6	pF

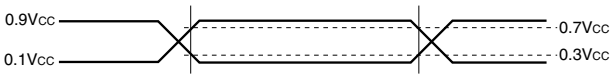
Note 1: Typical values are T_A = 25°C and nominal supply voltage of 5V for 4.5V-5.5V operation and at 3V for 2.7V-4.5V operation.

Note 2: This parameter is periodically sampled and not 100% tested.

AC Test Conditions

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10 ns
Input & Output Timing Levels	V_{CC} x 0.3 to V_{CC} x 0.7
Output Load	1 TTL Gate and C_L = 100 pF

AC Testing Input/Output Waveforms



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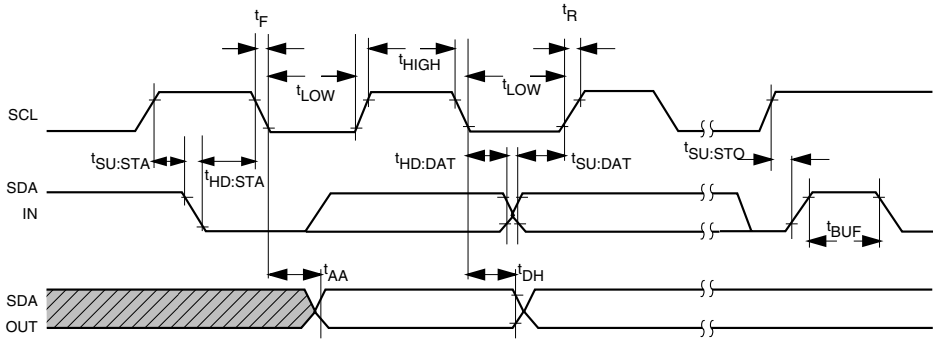
Read and Write Cycle Limits (Standard and Low V_{CC} Range 2.7V - 5.5V)

Symbol	Parameter	100 KHz		400 KHz		Units
		Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		100		400	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs (Minimum V_{IN} Pulse width)		100		50	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	0.1	0.9	µs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		1.3		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		0.6		µs
t_{LOW}	Clock Low Period	4.7		1.5		µs
t_{HIGH}	Clock High Period	4.0		0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		µs
$t_{HD:DAT}$	Data in Hold Time	20		20		ns
$t_{SU:DAT}$	Data in Setup Time	250		100		ns
t_R	SDA and SCL Rise Time		1		0.3	µs
t_F	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		0.6		µs
t_{DH}	Data Out Hold Time	300		50		ns
t_{WR} (Note 3)	Write Cycle Time - NM24C02/03 - NM24C02/03L, NM24C02/03LZ		10 15		10 15	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the NM24C02/03 bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address. Refer "Write Cycle Timing" diagram.

Bus Timing



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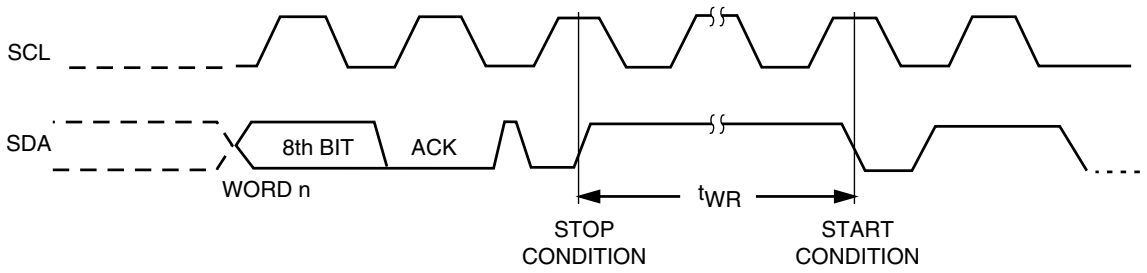
Write Cycle Timing



Note: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle.

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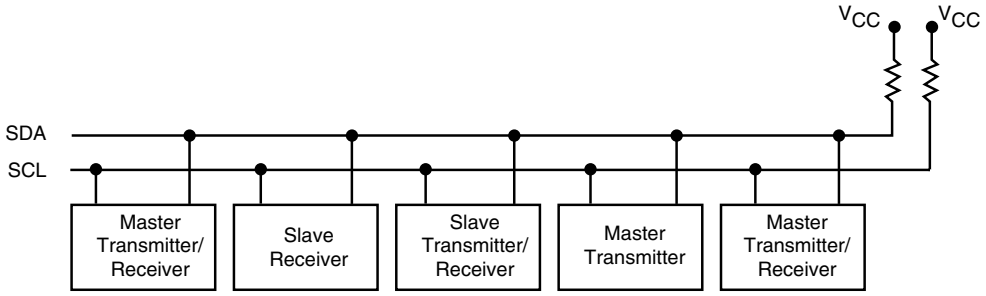
Typical System Configuration



Note: Due to open drain configuration of SDA and SCL, a bus-level pull-up resistor is called for, (typical value = 4.7kΩ)

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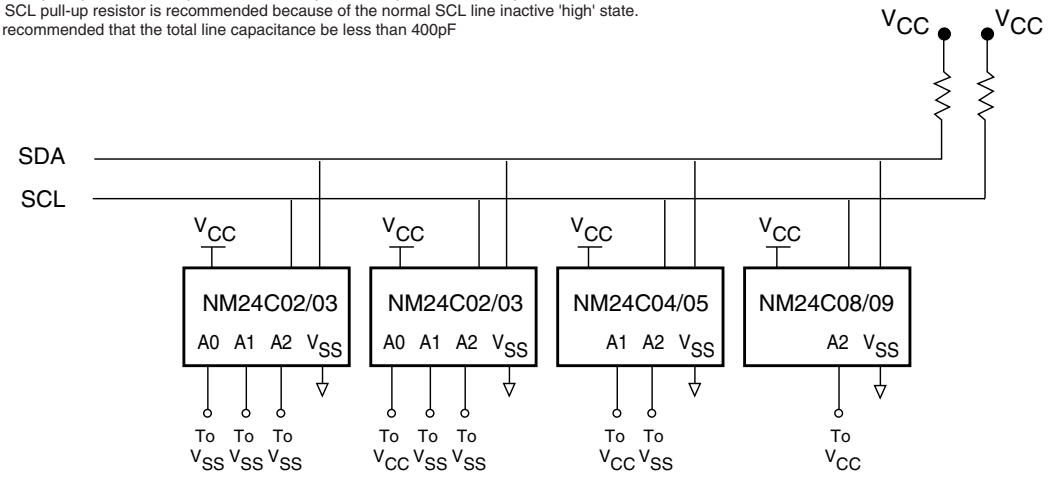
Example of 16K of Memory on 2-Wire Bus

Note: The SDA pull-up resistor is required due to the open-drain/open collector output of IIC bus devices.
The SCL pull-up resistor is recommended because of the normal SCL line inactive 'high' state.
It is recommended that the total line capacitance be less than 400pF



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Device	Address Pins Present			Memory Size	# of Page Blocks
	A0	A1	A2		
NM24C02/03	Yes	Yes	Yes	2048 Bits	1
NM24C04/05	No	Yes	Yes	4096 Bits	2
NM24C08/09	No	No	Yes	8192 Bits	4
NM24C16/17	No	No	No	16,384 Bits	8

Background Information (IIC Bus)

IIC bus allows synchronous bi-directional communication between a TRANSMITTER and a RECEIVER using a Clock signal (SCL) and a Data signal (SDA). Additionally there are up to three Address signals (A2, A1 and A0) which collectively serve as "chip select signal" to a device (example EEPROM) on the IIC bus.

All communication on the IIC bus must be started with a valid START condition (by a MASTER), followed by transmittal (by the MASTER) of byte(s) of information (Address/Data). For every byte of information received, the addressed RECEIVER provides a valid ACKNOWLEDGE pulse to further continue the communication unless the RECEIVER intends to discontinue the communication. Depending on the direction of transfer (Write or Read), the RECEIVER can be a SLAVE or the MASTER. A typical IIC communication concludes with a STOP condition (by the MASTER).

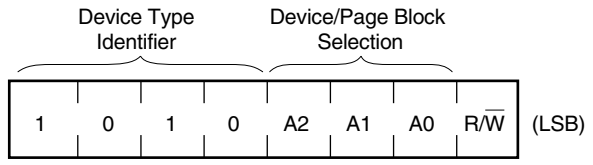
Addressing an EEPROM memory location involves sending a command string with the following information:

[DEVICE TYPE]—[DEVICE/PAGE BLOCK SELECTION]—[R/W BIT]—{acknowledge pulse}—[ARRAY ADDRESS]

Slave Address

Slave Address is an 8-bit information consisting of a Device type field (4bits), Device/Page block selection field (3bits) and Read/Write bit (1bit).

Slave Address Format



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Device Type

IIC bus is designed to support a variety of devices such as RAMs, EPROMs etc., along with EEPROMS. Hence to properly identify various devices on the IIC bus, a 4-bit “Device Type” identifier string is used. For EEPROMS, this 4-bit string is 1-0-1-0. Every IIC device on the bus internally compares this 4-bit string to its own “Device Type” string to ensure proper device selection.

Device/Page Block Selection

When multiple devices of the same type (e.g. multiple EEPROMS) are present on the IIC bus, then the A2, A1 and A0 address information bits are also used as part of the Slave Address. Every IIC device on the bus internally compares this 3-bit string to its own physical configuration (A2, A1 and A0 pins) to ensure proper device selection. This comparison is in addition to the “Device Type” comparison. In addition to selecting an EEPROM, these 3 bits are also used to select a “page block” within the selected EEPROM. Each page block is 2Kbit (256Bytes) in size. Depending on the density, an EEPROM can contain from a minimum of 1 to a maximum of 8 page blocks (in multiples of 2) and selection of a page block within a device is by using A2, A1 and A0 bits.

Read/Write Bit

Last bit of the Slave Address indicates if the intended access is Read or Write. If the bit is "1," then the access is Read, whereas if the bit is "0," then the access is Write.

Acknowledge

Acknowledge is an active LOW pulse on the SDA line driven by an addressed receiver to the addressing transmitter to indicate receipt of 8-bits of data. The receiver provides an ACK pulse for every 8-bits of data received. This handshake mechanism is done as follows: After transmitting 8-bits of data, the transmitter releases the SDA line and waits for the ACK pulse. The addressed receiver, if present, drives the ACK pulse on the SDA line during the 9th clock and releases the SDA line back (to the transmitter). Refer *Figure 3*.

Array Address

Array address is an 8-bit information containing the address of a memory location to be selected within a page block of the device.

16K bit Addressing Limitation:

Standard IIC specification limits the maximum size of EEPROM memory on the bus to 16K bits. This limitation is due to the addressing protocol implemented which consists of the 8-bit Slave Address and an additional 8-bit field called Array Address. This Array Address selects 1 out of 256 locations (2^8=256). Since the data format of IIC specification is 8-bit wide, a total of 256 x 8 = 2048 = 2K bit now becomes addressable by this 8-bit Array Address. This 2K bit is typically referred as a “Page Block”. Combining this 8-bit Array Address with the 3-bit Device/Page address (part of Slave Address) allows a maximum of 8 pages (2^3=8) of memory that can be addressed. Since each page is 2K bit in size, 8 x 2K bit = 16K bit is the maximum size of memory that is addressable on the Standard IIC bus. This 16Kb of memory can be in the form of a single 16Kb EEPROM device or multiple EEPROMs of varying density (in 2Kb multiples) to a maximum total of 16Kb. To address the needs of systems that require more than 16Kb on the IIC bus, a different specification called “Extended IIC Specification” is used. Please refer to NM24C32xx Datasheet for more information on Extended IIC Specification.

DEFINITIONS	
WORD	8 bits (byte) of data
PAGE	16 sequential byte locations starting at a 16-byte address boundary, that may be programmed during a "page write" programming cycle
PAGE BLOCK	2048 (2K) bits organized into 16 pages of addressable memory. (8 bits) x (16 bytes) x (16 pages) = 2048 bits
MASTER	Any IIC device CONTROLLING the transfer of data (such as a microprocessor)
SLAVE	Device being controlled (EEPROMs are always considered Slaves)
TRANSMITTER	Device currently SENDING data on the bus (may be either a Master or Slave).
RECEIVER	Device currently RECEIVING data on the bus (Master or Slave)

Pin Descriptions

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bi-directional pin used to transfer data into and out of the device. It is an open drain output and may be wire–ORed with any number of open drain or open collector outputs.

Write Protect (WP) (NM24C03 Only)

If tied to V_{CC}, PROGRAM operations onto the upper half (upper 1Kbit) of the memory will not be executed. READ operations are possible. If tied to V_{SS}, normal operation is enabled, READ/WRITE over the entire memory is possible.

This feature allows the user to assign the upper half of the memory as ROM which can be protected against accidental programming. When write is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

This pin has an internal pull-down circuit. However, on systems where write protection is not required it is recommended that this pin is tied to V_{SS}.

Device Selection Inputs A2, A1 and A0 (as appropriate)

These inputs collectively serve as "chip select" signal to an EEPROM when multiple EEPROMs are present on the same IIC bus. Hence these inputs, if present, should be connected to V_{CC} or V_{SS} in a unique manner to allow proper selection of an EEPROM amongst multiple EEPROMs. During a typical addressing sequence, every EEPROM on the IIC bus compares the configuration of these inputs to the respective 3 bit "Device/Page block selection" information (part of slave address) to determine a valid selection. For e.g. if the 3 bit "Device/Page block selection" is 1-0-1, then the EEPROM whose "Device Selection inputs" (A2, A1 and A0) are connected to V_{CC}-V_{SS}-V_{CC} respectively, is selected.

Depending on the density, only appropriate number of "Device Selection inputs" are provided on an EEPROM. For every "Device selection input" that is not present on the device, the corresponding bit in the "Device/Page block selection" field is used to select a "Page Block" within the device instead of the device itself. Following table illustrates the above:

EEPROM Density	Number of Page Blocks	Device Selection Inputs Provided			Address Bits Selecting Page Block
2k bit	1	A0	A1	A2	None
4k bit	2	—	A1	A2	A0
8k bit	4	—	—	A2	A0 and A1
16k bit	8	—	—	—	A0, A1 and A2

Note that even when just one EEPROM present on the IIC bus, these pins should be tied to V_{CC} or V_{SS} to ensure proper termination.

Device Operation

The NM24C02/03 supports a bi-directional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the NM24C02/03 will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to *Figure 1* and *Figure 2* on next page.

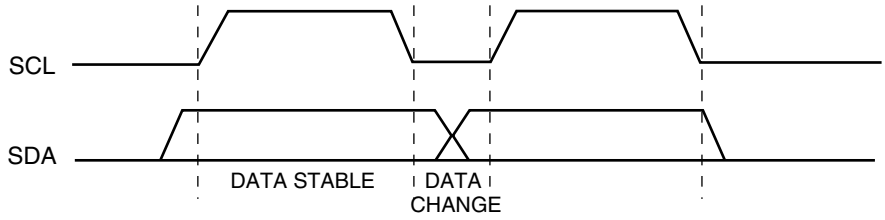
Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The NM24C02/03 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Stop Condition

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the NM24C02/03 to place the device in the standby power mode, except when a Write operation is being executed, in which case a second stop condition is required after t_{WR} period, to place the device in standby mode.

Data Validity (Figure 1)



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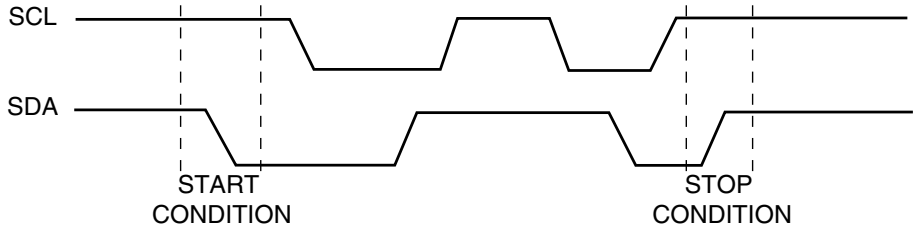
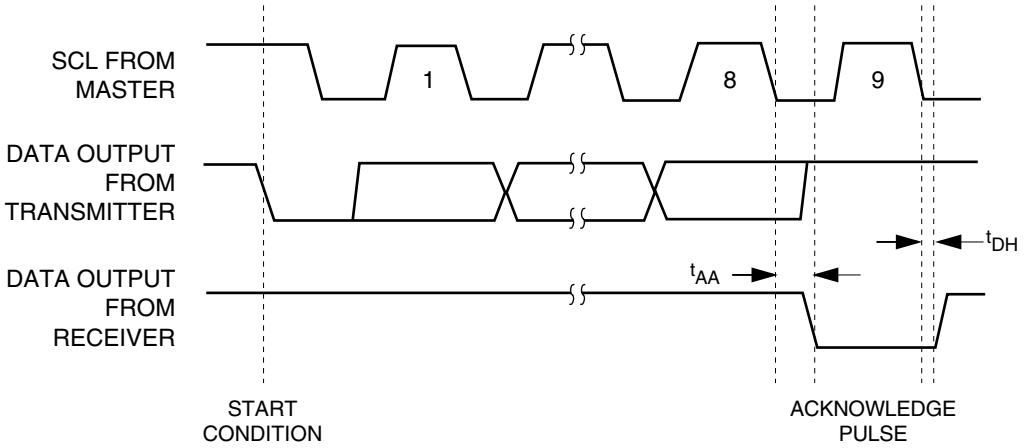
Start and Stop Definition (Figure 2)



DS500069-11

Acknowledge Response from Receiver (Figure 3)



DS500069-12

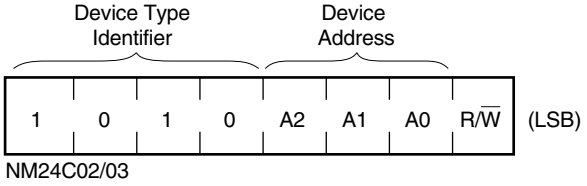
Acknowledge

The NM24C02/03 device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the NM24C02/03 will respond with an acknowledge after the receipt of each subsequent eight bit byte.

In the read mode the NM24C02/03 slave will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected, NM24C02/03 will continue to transmit data. If an acknowledge is not detected,NM24C02/03 will terminate further data transmissions and await the stop condition to return to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are those of the device type identifier. This is fixed as 1010 for all EEPROM devices.



NM24C02/03

Refer the following table for Slave Addresses string details:

Device	A0	A1	A2	Page Blocks	Page Block Addresses
NM24C02/03	A	A	A	1	(None)

A: Refers to a hardware configured Device Address pin.

All IIC EEPROMs use an internal protocol that defines a PAGE BLOCK size of 2K bits (for Word addresses 0x00 through 0xFF). Therefore, address bits A0, A1, or A2 (if designated 'P') are used to access a PAGE BLOCK in conjunction with the Word address used to access any individual data byte.

The last bit of the slave address defines whether a write or read condition is requested by the master. A '1' indicates that a read operation is to be executed, and a '0' initiates the write mode.

A simple review: After the NM24C02/03 recognizes the start condition, the devices interfaced to the IIC bus wait for a slave address to be transmitted over the SDA line. If the transmitted slave address matches an address of one of the devices, the designated slave pulls the line LOW with an acknowledge signal and awaits further transmissions.

Write Operations

BYTE WRITE

For a write operation a second address field is required which is a word address that is comprised of eight bits and provides access to any one of the 256 bytes in the selected page of memory. Upon receipt of the byte address the NM24C02/03 responds with an acknowledge and waits for the next eight bits of data, again, responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the NM24C02/03 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the NM24C02/03 inputs are disabled, and the device will not respond to any requests from the master for the duration of t_{WR}. Refer to *Figure 4* for the address, acknowledge and data transfer sequence.

PAGE WRITE

To minimize write cycle time, NM24C02/03 offer Page Write feature, by which, up to a maximum of 16 contiguous bytes locations can be programmed all at once (instead of 16 individual byte writes). To facilitate this feature, the memory array is organized in terms of "Pages." A Page consists of 16 contiguous byte locations starting at every 16-Byte address boundary (for example, starting at array address 0x00, 0x10, 0x20 etc.). Page Write operation limits access to byte locations within a page. In other words a single Page Write operation will not cross over to locations on another page but will "roll over" to the beginning of the page whenever end of Page is reached and additional locations are a continued to be accessed. A Page Write operation can be initiated to begin at any location within a page (starting address of the Page Write operation need not be the starting address of a Page).

Page Write is initiated in the same manner as the Byte Write operation; but instead of terminating the cycle after transmitting the first data byte, the master can further transmit up to 15 more bytes. After the receipt of each byte, NM24C02/03 will respond with an acknowledge pulse, increment the internal address counter to the next address and is ready to accept the next data. If the master should transmit more than sixteen bytes prior to generating the STOP condition, the address counter will "roll over" and previously written data will be overwritten. As with the Byte Write operation, all inputs are disabled until completion of the internal write cycle. Refer to *Figure 5* for the address, acknowledge and data transfer sequence.

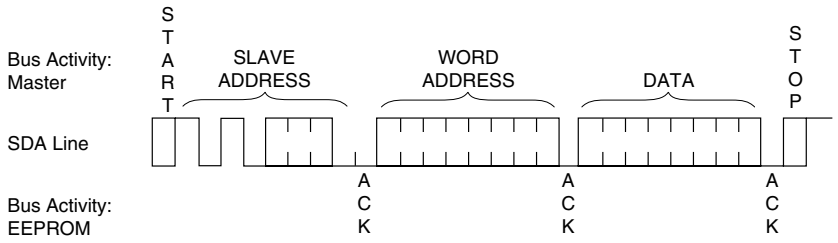
Acknowledge Polling

Once the stop condition is issued to indicate the end of the host's write operation the NM24C02/03 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the NM24C02/03 is still busy with the write operation no ACK will be returned. If the NM24C02/03 has completed the write operation an ACK will be returned and the host can then proceed with the next read or write operation.

Write Protection (NM24C03 Only)

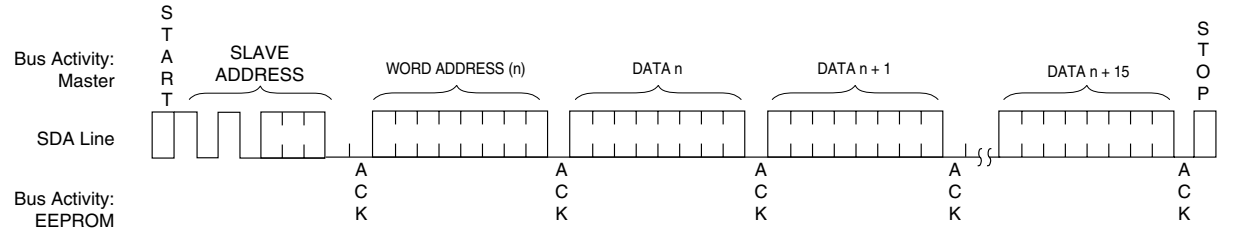
Programming of the upper half (upper 1Kbit) of the memory will not take place if the WP pin of the NM24C03 is connected to V_{CC}. The NM24C03 will respond to slave and byte addresses; but if the memory accessed is write protected by the WP pin, the NM24C03 will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the stop condition is asserted.

Byte Write (Figure 4)



DS500069-13

Page Write (Figure 5)



DS500069-14

Read Operations

Read operations are initiated in the same manner as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to a one. There are three basic read operations: current address read, random read, and sequential read.

Current Address Read

Internally the NM24C02/03 contains an address counter that maintains the address of the last byte accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ set to one, the NM24C02/03 issues an acknowledge and transmits the eight bit byte. The master will not acknowledge the transfer but does generate a stop condition, and therefore the NM24C02/03 discontinues transmission. Refer to *Figure* 6 for the sequence of address, acknowledge and data transfer.

Random Read

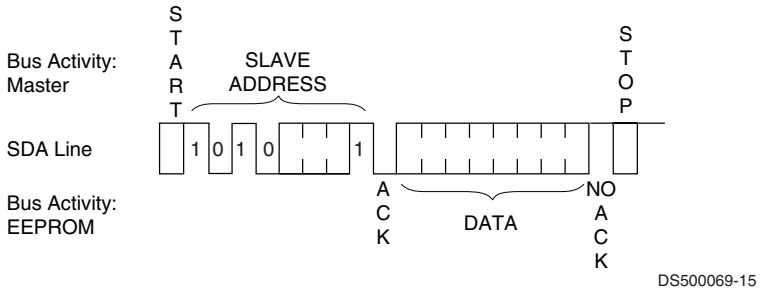
Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, slave address with the R/$\overline{W}$ bit set to zero and then the byte address it is to read. After the byte address acknowledge, the master immediately issues another start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the NM24C02/03 and then by the eight bit byte. The master will not acknowledge the transfer but does generate the stop condition, and therefore the NM24C02/03 discontinues transmission. Refer to *Figure 7* for the address, acknowledge and data transfer sequence.

Sequential Read

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted in the same manner as the other read modes; however, the master now responds with an acknowledge, indicating it requires additional data. The NM24C02/03 continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge or by generating a stop condition.

The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. After the entire memory has been read, the counter "rolls over" to the beginning of the memory. NM24C02/03 continues to output data for each acknowledge received. Refer to *Figure 8* for the address, acknowledge, and data transfer sequence.

Current Address Read (Figure 6)



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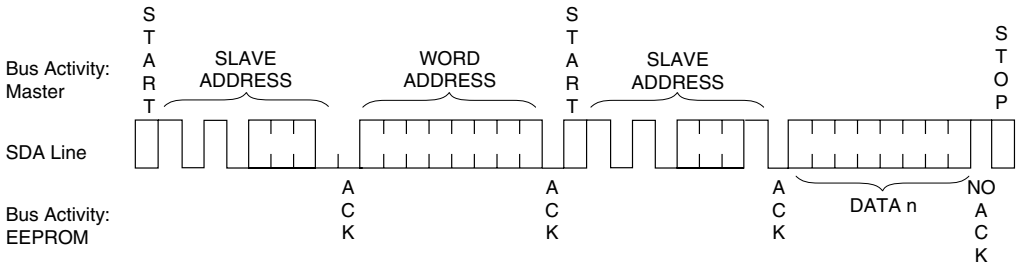
Random Read (Figure 7)



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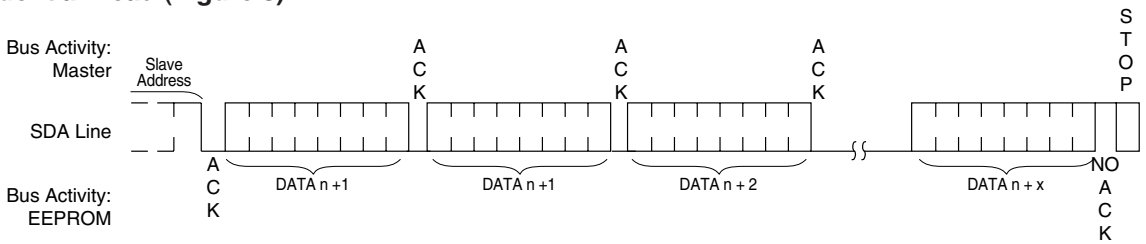
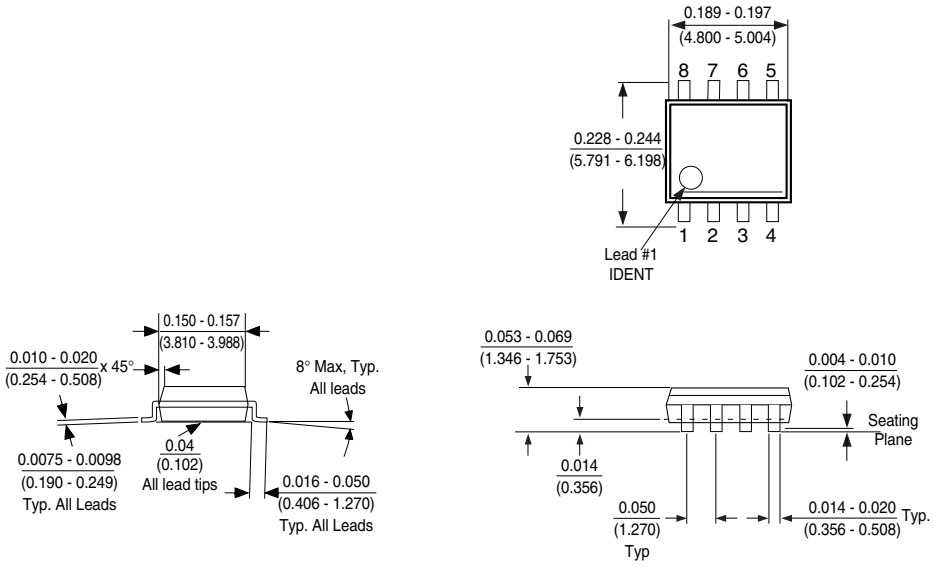
Sequential Read (Figure 8)

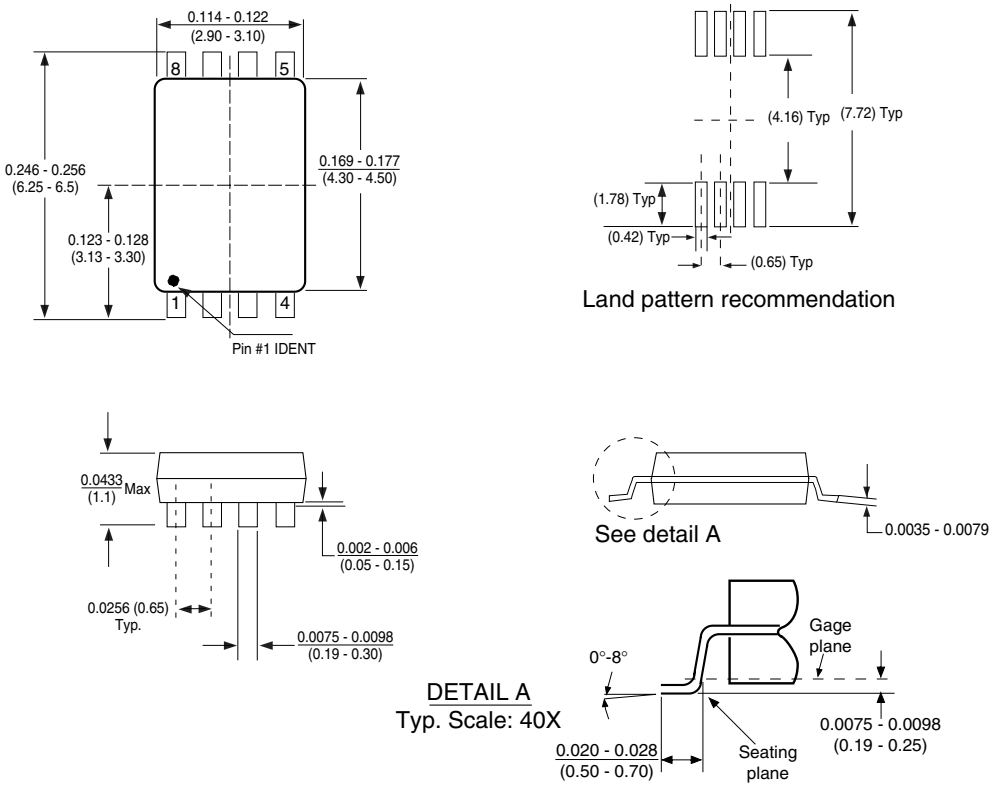


DS500069-17

Physical Dimensions inches (millimeters) unless otherwise noted



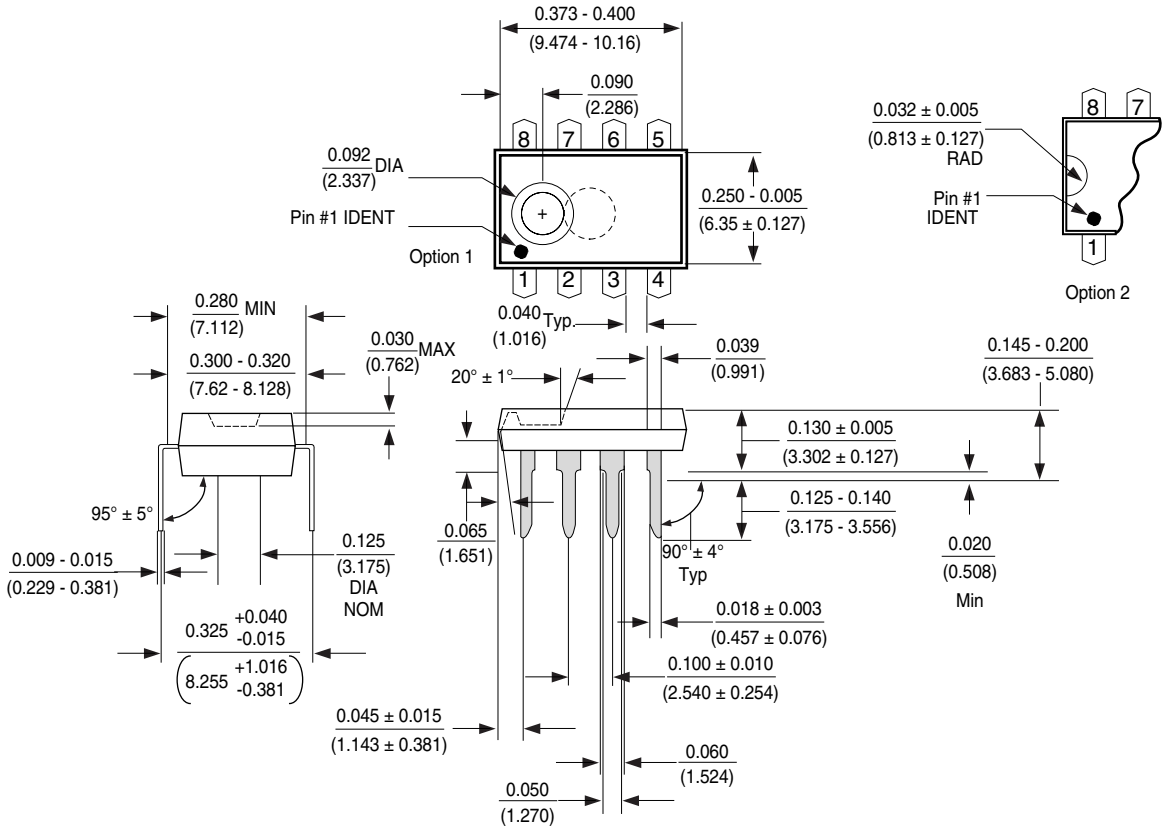
8-Pin Molded Small Outline Package (M8)
Package Number M08A



Notes: Unless otherwise specified
1. Reference JEDEC registration MO153. Variation AA. Dated 7/93

8-Pin Molded Thin Shrink Small Outline Package (MT8)
Package Number MTC08

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Package Number N08E

Life Support Policy

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

August 1999

NM24C02U/NM24C03U 2K-Bit Serial EEPROM 2-Wire Bus Interface

General Description

The NM24C02U/NM24C03U are 2K (2,048) bit serial interface CMOS EEPROMs (Electrically Erasable Programmable Read-Only Memory). These devices fully conform to the **Standard** I²C™ 2-wire protocol which uses Clock (SCL) and Data I/O (SDA) pins to synchronously clock data between the "master" (for example a microprocessor) and the "slave" (the EEPROM device). In addition, the serial interface allows a minimal pin count packaging designed to simplify PC board layout requirements and offers the designer a variety of low voltage and low power options.

NM24C03U incorporates a hardware "Write Protect" feature, by which, the upper half of the memory can be disabled against programming by connecting the WP pin to V_{CC}. This section of memory then effectively becomes a ROM (Read-Only Memory) and can no longer be programmed as long as WP pin is connected to V_{CC}.

Fairchild EEPROMs are designed and tested for applications requiring high endurance, high reliability and low power consumption for a continuously reliable non-volatile solution for all markets.

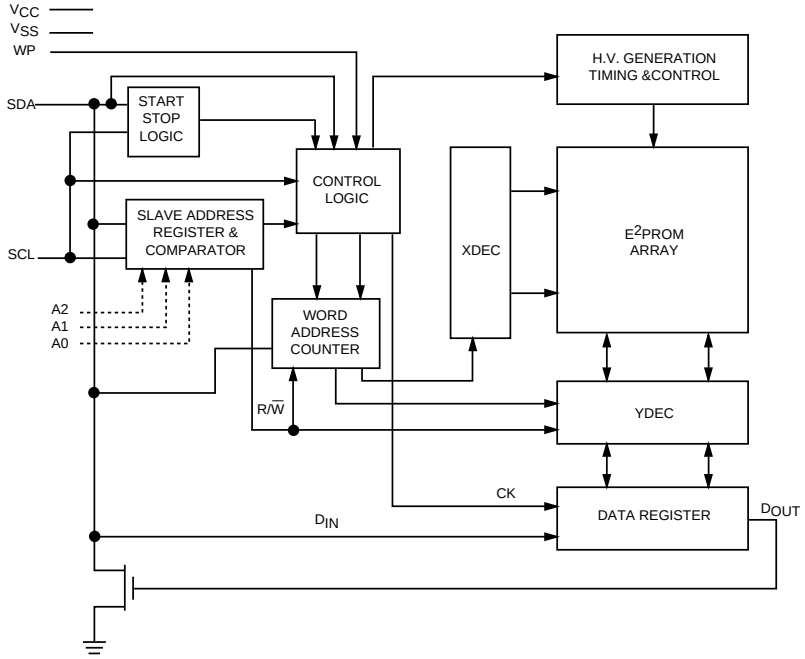
Functions

- I²C™ compatible interface
- 2,048 bits organized as 256 x 8
- Extended 2.7V – 5.5V operating voltage
- 100 KHz or 400 KHz operation
- Self timed programming cycle (6ms typical)
- "Programming complete" indicated by ACK polling
- NM24C03U: Memory "Upper Block" Write Protect pin

Features

- The I²C™ interface allows the smallest I/O pincount of any EEPROM interface
- 16 byte page write mode to minimize total write time per byte
- Typical 200µA active current (I_{CCA})
- Typical 1µA standby current (I_{SB}) for "L" devices and 0.1µA standby current for "LZ" devices
- Endurance: Up to 1,000,000 data changes
- Data retention greater than 40 years

Block Diagram

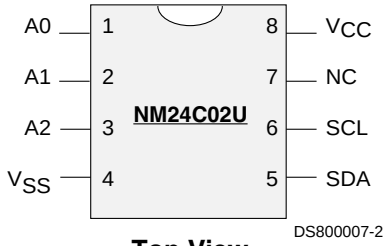


DS800007-1

I²C™ is a registered trademark of Philips Electronics N.V.

Connection Diagrams

Dual-in-Line Package (N), SO Package (M8), and TSSOP Package (MT8)

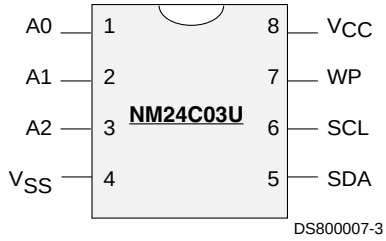


Top View
See Package Number N08E, M08A, and MTC08

Pin Names

A0,A1,A2	Device Address Inputs
V_{SS}	Ground
SDA	Serial Data I/O
SCL	Serial Clock Input
NC	No Connection
V_{CC}	Power Supply

Dual-in-Line Package (N), SO Package (M8), and TSSOP Package (MT8)

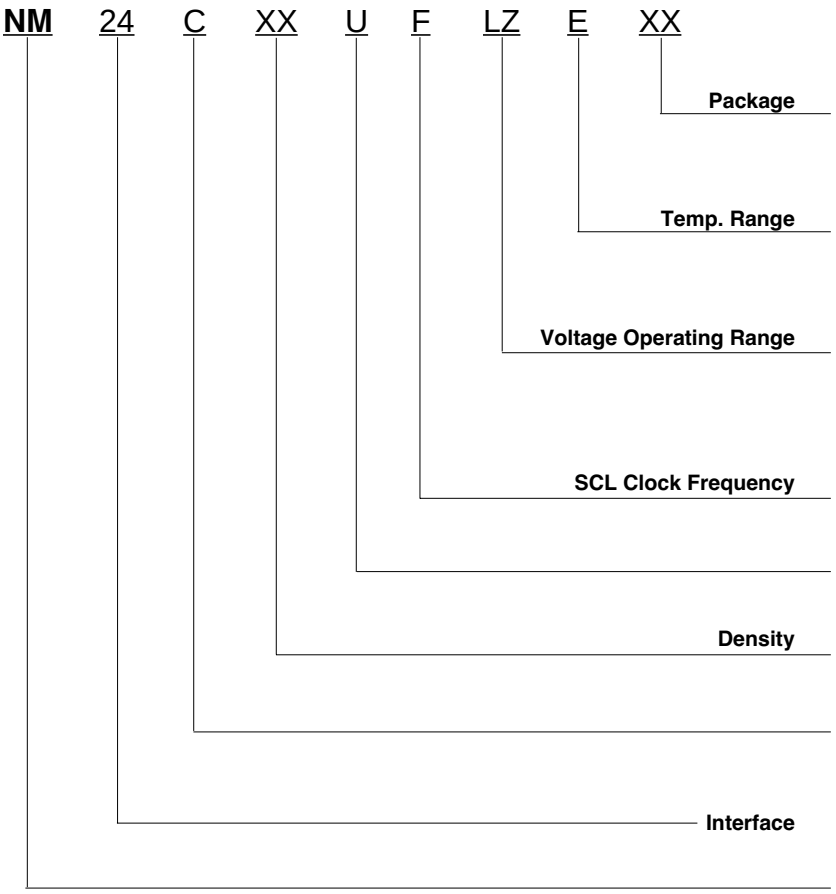


Top View
See Package Number N08E, M08A, and MTC08

Pin Names

A0,A1,A2	Device Address Inputs
V_{SS}	Ground
SDA	Serial Data I/O
SCL	Serial Clock input
WP	Write Protect
V_{CC}	Power Supply

Ordering Information



	Letter	Description
Package	N	8-pin DIP
	M8	8-pin SOIC
	MT8	8-pin TSSOP
Temp. Range	None	0 to 70°C
	V	-40 to +125°C
	E	-40 to +85°C
Voltage Operating Range	Blank	4.5V to 5.5V
	L	2.7V to 5.5V
	LZ	2.7V to 5.5V and <1µA Standby Current
SCL Clock Frequency	Blank	100KHz
	F	400KHz
	Ultralite	CS100UL Process
Density	02	2K
	03	2K with Write Protect
	C	CMOS Technology
	W	Total Array Write Protect
Interface	24	IIC
NM		**Fairchild Non-Volatile Memory**

Product Specifications

Absolute Maximum Ratings

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltages with Respect to Ground	6.5V to –0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min.

Operating Conditions

Ambient Operating Temperature	
NM24C02U/03U	0°C to +70°C
NM24C02UE/03UE	-40°C to +85°C
NM24C02UV/03UV	-40°C to +125°C
Positive Power Supply	
NM24C02U/03U	4.5V to 5.5V
NM24C02UL/03UL	2.7V to 5.5V
NM24C02ULZ/03ULZ	2.7V to 5.5V

Standard V_{CC} (4.5V to 5.5V) DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 400 KHz f_{SCL} = 100 KHz		0.2	1.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		10	50	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	1	µA
V_{IL}	Input Low Voltage		–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Low V_{CC} (2.7V to 5.5V) DC Electrical Characteristics

Symbol	Parameter	Test Conditions		Limits			Units
				Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 400 KHz f_{SCL} = 100 KHz			0.2	1.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}	V_{CC} = 2.7V - 4.5V V_{CC} = 2.7V - 4.5V V_{CC} = 4.5V - 5.5V		1 0.1 10	10 1 50	µA µA µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}			0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}			0.1	1	µA
V_{IL}	Input Low Voltage			–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA				0.4	V

Capacitance T_A = +25°C, f = 100/400 KHz, V_{CC} = 5V (Note 2)

Symbol	Test	Conditions	Max	Units
$C_{I/O}$	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN}	Input Capacitance (A0, A1, A2, SCL)	V_{IN} = 0V	6	pF

Note 1: Typical values are T_A = 25°C and nominal supply voltage (5V).

Note 2: This parameter is periodically sampled and not 100% tested.

AC Conditions of Test

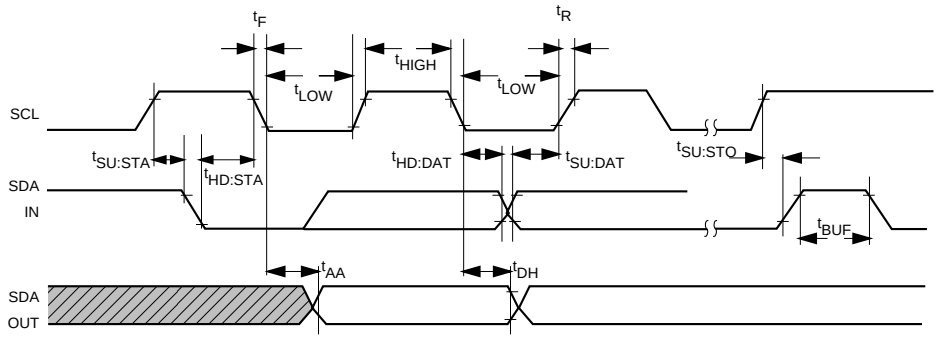
Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10 ns
Input & Output Timing Levels	V_{CC} x 0.5
Output Load	1 TTL Gate and C_L = 100 pF

Read and Write Cycle Limits (Standard and Low V_{CC} Range)

Symbol	Parameter	100 KHz		400 KHz		Units
		Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		100		400	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs (Minimum V_{IN} Pulse width)		100		50	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	0.1	0.9	µs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		1.3		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		0.6		µs
t_{LOW}	Clock Low Period	4.7		1.5		µs
t_{HIGH}	Clock High Period	4.0		0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		µs
$t_{HD:DAT}$	Data in Hold Time	0		0		µs
$t_{SU:DAT}$	Data in Setup Time	250		100		ns
t_R	SDA and SCL Rise Time		1		0.3	µs
t_F	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		0.6		µs
t_{DH}	Data Out Hold Time	300		50		ns
t_{WR} (Note 3)	Write Cycle Time - NM24C02U/03U - NM24C02U/03UL, NM24C02U/03ULZ		10 15		10 15	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the NM24C02U/03U bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

Bus Timing



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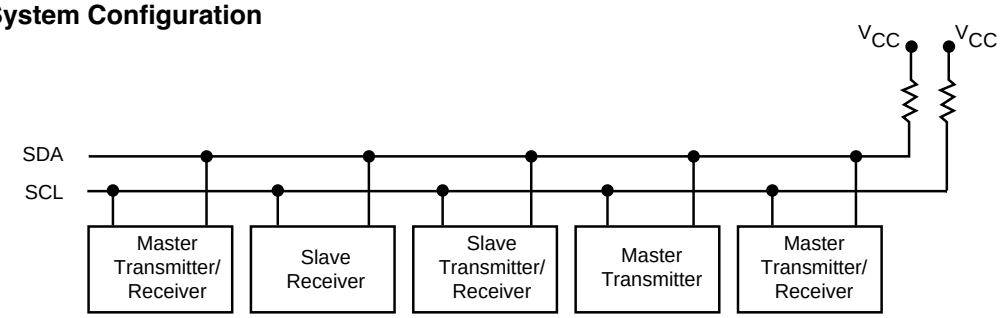
System Layout

Typical System Configuration

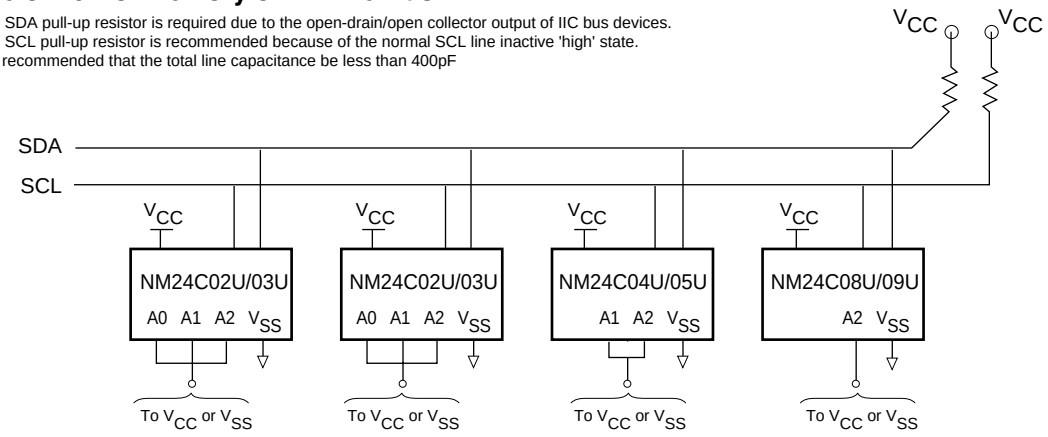


Note: Due to open drain configuration of SDA, a bus-level pull-up resistor is called for, (typical value = 4.7kΩ)

DS800007-20

Example of 16K of Memory on 2-Wire Bus

Note: The SDA pull-up resistor is required due to the open-drain/open collector output of IIC bus devices.
The SCL pull-up resistor is recommended because of the normal SCL line inactive 'high' state.
It is recommended that the total line capacitance be less than 400pF



DS800007-9

Device	Address Pins			Memory Size	# of Page Blocks
	A0	A1	A2		
NM24C02U/03U	ADR	ADR	ADR	2048 Bits	1

Device Operation Inputs (A0, A1, A2)

Device address pins A0, A1, and A2 are connected to V_{CC} or V_{SS} to configure the EEPROM chip address. Table I shows the active pins.

Table 1.

Device	A0	A1	A2	Effects of Addresses
NM24C02U/03U	ADR	ADR	ADR	2^3 = 8; 8*x (1x2K)** = 16K

* Max # of devices on bus ** Number of page blocks per density

Under the Standard IIC protocol, the maximum density addressable using the three pin configuration of the IIC protocol is 16K. Any combination of densities can be used up to this limit.

Background Information (IIC Bus)

As mentioned, the IIC bus allows synchronous bidirectional communication between Transmitter/Receiver using the SCL (clock) and SDA (Data I/O) lines. All communication must be started with a valid START condition, concluded with a STOP condition and acknowledged by the Receiver with an ACKNOWLEDGE condition.

- Hardware configuring the A0, A1, and A2 pins (Device Address pins) with pull-up or pull-down to V_{CC} or V_{SS}. **All unused pins must be grounded** (tied to V_{SS}).
- Software addressing the required PAGE BLOCK within the device memory array (as sent in the Slave Address string).

For devices with densities greater than 16K, a different protocol, the Extended IIC protocol, is used. Refer to NM24C32U datasheet (for example) for additional details.

Addressing an EEPROM memory location involves sending a command string with the following information: [DEVICE TYPE]–[DEVICE ADDRESS]–[PAGE BLOCK ADDRESS]–[BYTE ADDRESS]

DEFINITIONS	
WORD	8 bits (byte) of data
PAGE	16 sequential addresses (one byte each) that may be programmed during a 'Page Write' programming cycle
PAGE BLOCK	2048 (2K) bits organized into **16 pages of addressable memory. (8 bits) x (16 bytes) x (16 pages) = 2048 bits**
MASTER	Any IIC device CONTROLLING the transfer of data (such as a microprocessor)
SLAVE	Device being controlled (EEPROMs are always considered Slaves)
TRANSMITTER	Device currently SENDING data on the bus (may be either a Master or Slave).
RECEIVER	Device currently RECEIVING data on the bus (Master or Slave)

Pin Descriptions

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire–ORed with any number of open drain or open collector outputs.

WP Write Protection (NM24C03U Only)

If tied to V_{CC}, PROGRAM operations onto the upper half of the memory will not be executed. READ operations are possible. If tied to V_{SS}, normal operation is enabled, READ/WRITE over the entire memory is possible.

This feature allows the user to assign the upper half of the memory as ROM which can be protected against accidental programming. When write is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

Device Operation

The NM24C02U/03U supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the NM24C02U/03U will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to *Figure 2* and *Figure 3* on next page.

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The NM24C02U/03U continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Stop Condition

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the NM24C02U/03U to place the device in the standby power mode.

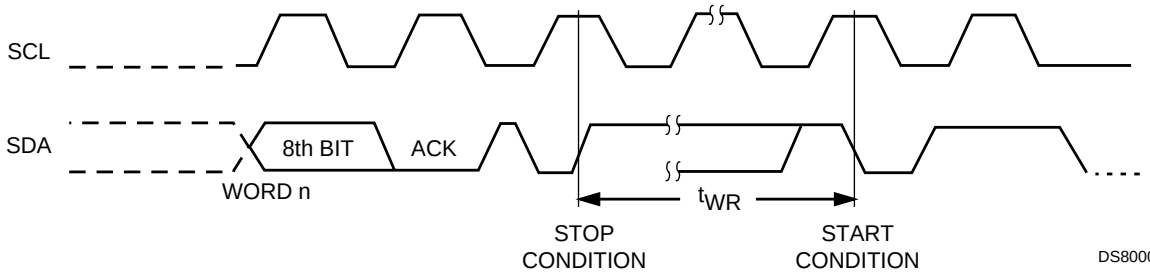
Write Cycle Timing

Acknowledge

Acknowledge is a hardware convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits.

During the ninth clock cycle the receiver will pull the SDA line to LOW to acknowledge that it received the eight bits of data. Refer to *Figure 4.*

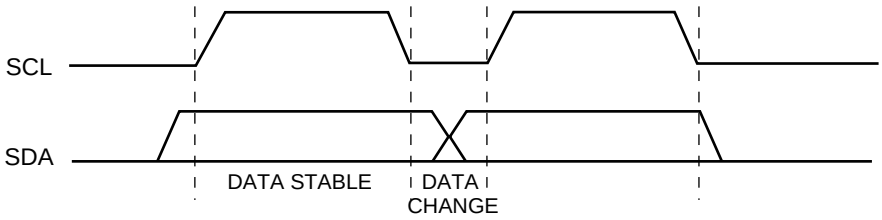
Write Cycle Timing (Figure 1)



DS800007-10

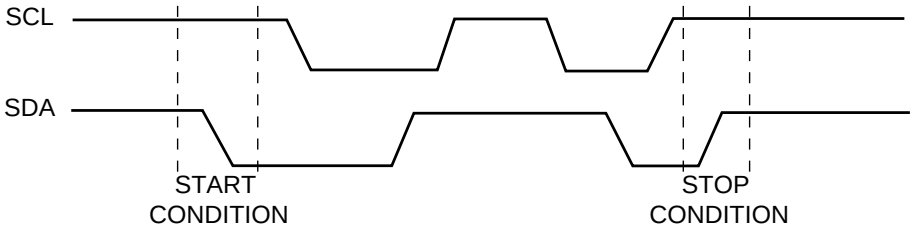
Note: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle.

Data Validity (Figure 2)



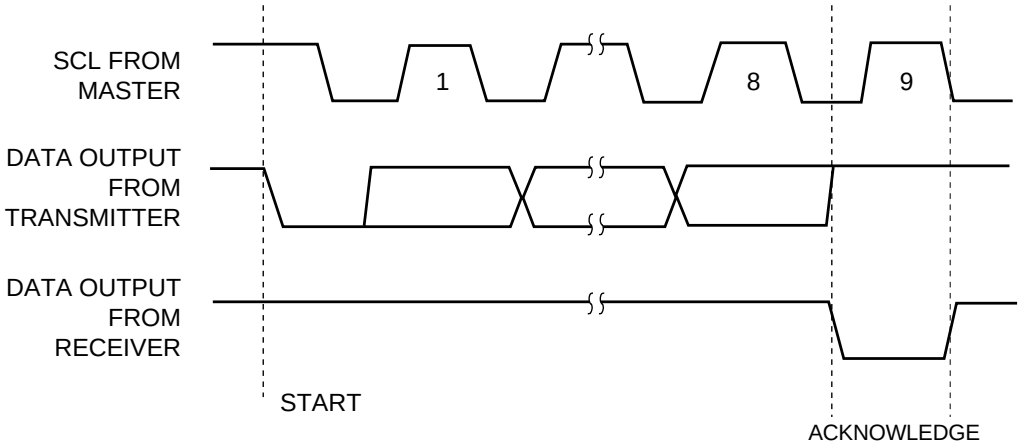
DS800007-11

Start and Stop Definition (Figure 3)



DS800007-12

Acknowledge Response from Receiver (Figure 4)



DS800007-13

Write Cycle Timing (Continued)

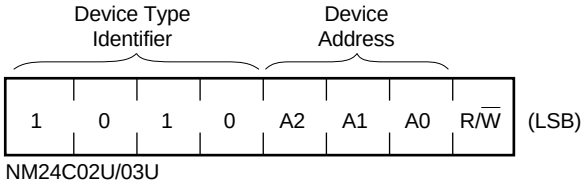
The NM24C02U/03U device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the NM24C02U/03U will respond with an acknowledge after the receipt of each subsequent eight bit byte.

In the read mode the NM24C02U/03U slave will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are those of the device type identifier (*see Figure 5)*. This is fixed as 1010 for all EEPROM devices.

Slave Addresses (Figure 5)



DS800007-14

Refer to the following table for Slave Addresses string details:

Device	A0	A1	A2	Page Blocks	Page Block Addresses
NM24C02U/03U	A	A	A	1	(None)

A: Refers to a hardware configured Device Address pin.

All IIC EEPROMs use an internal protocol that defines a PAGE BLOCK size of 2K bits (for Word addressess 0000 through 1111). Therefore, address bits A0, A1, or A2 (if designated 'P') are used to access a PAGE BLOCK in conjunction with the Word address used to access any individual data byte (Word).

The last bit of the slave address defines whether a write or read condition is requested by the master. A '1' indicates that a read operation is to be executed, and a '0' initiates the write mode.

A simple review: After the NM24C02U/03U recognizes the start condition, the devices interfaced to the IIC bus wait for a slave address to be transmitted over the SDA line. If the transmitted slave address matches an address of one of the devices, the designated slave pulls the line LOW with an acknowledge signal and awaits further transmissions.

Write Operations

BYTE WRITE

For a write operation a second address field is required which is a word address that is comprised of eight bits and provides access to any one of the 256 bytes in the selected page of memory. Upon receipt of the byte address the NM24C02U/03U responds with an acknowledge and waits for the next eight bits of data, again, responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the NM24C02U/03U begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the NM24C02U/03U inputs are disabled, and the device will not respond to any requests from the master. Refer to *Figure 6* for the address, acknowledge and data transfer sequence.

PAGE WRITE

The NM24C02U/03U is capable of a sixteen byte page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data byte is transferred, the master can transmit up to fifteen more bytes. After the receipt of each byte, the NM24C02U/03U will respond with an acknowledge.

After the receipt of each byte, the internal address counter increments to the next address and the next SDA data is accepted. If the master should transmit more than sixteen bytes prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to *Figure 7* for the address, acknowledge, and data transfer sequence.

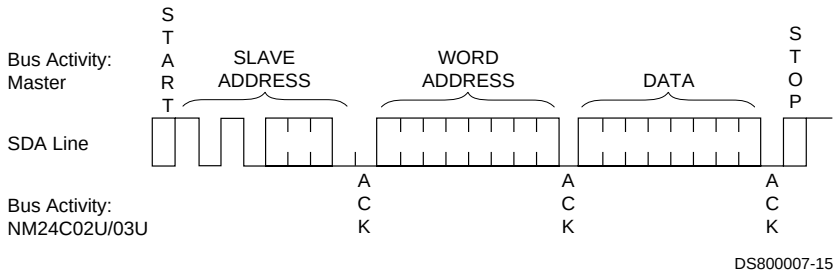
Acknowledge Polling

Once the stop condition is issued to indicate the end of the host's write operation the NM24C02U/03U initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the NM24C02U/03U is still busy with the write operation no ACK will be returned. If the NM24C02U/03U has completed the write operation an ACK will be returned and the host can then proceed with the next read or write operation.

Write Protection (NM24C03U Only)

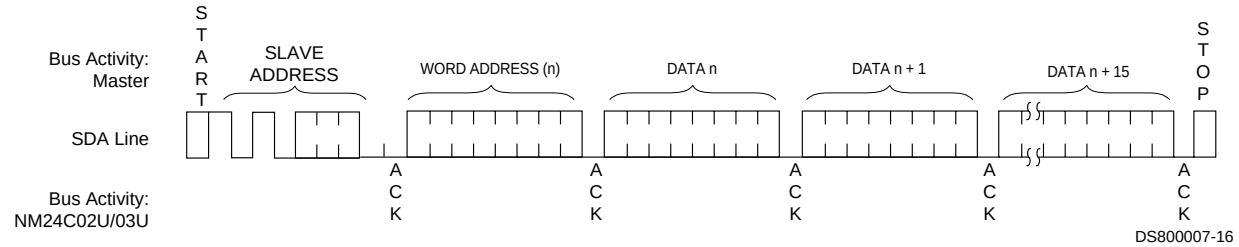
Programming of the upper half of the memory will not take place if the WP pin of the NM24C03U is connected to V_{CC}. The NM24C03U will accept slave and byte addresses; but if the memory accessed is write protected by the WP pin, the NM24C03U will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the stop condition is asserted.

Byte Write (Figure 6)



DS800007-15

Page Write (Figure 7)



DS800007-16

Read Operations

Read operations are initiated in the same manner as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to a one. There are three basic read operations: current address read, random read, and sequential read.

Current Address Read

Internally the NM24C02U/03U contains an address counter that maintains the address of the last byte accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ set to one, the NM24C02U/03U issues an acknowledge and transmits the eight bit byte. The master will not acknowledge the transfer but does generate a stop condition, and therefore the NM24C02U/03U discontinues transmission. Refer to *Figure* 8 for the sequence of address, acknowledge and data transfer.

Random Read

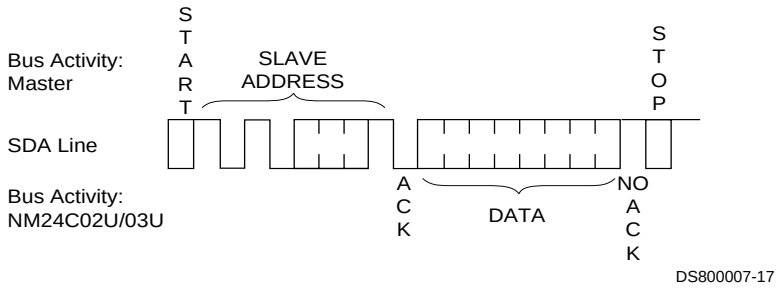
Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, slave address and then the byte address it is to read. After the byte address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the NM24C02U/03U and then by the eight bit data. The master will not acknowledge the transfer but does generate the stop condition, and therefore the NM24C02U/03U discontinues transmission. Refer to *Figure 9* for the address, acknowledge and data transfer sequence.

Sequential Read

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted in the same manner as the other read modes; however, the master now responds with an acknowledge, indicating it requires additional data. The NM24C02U/03U continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge or by generating a stop condition.

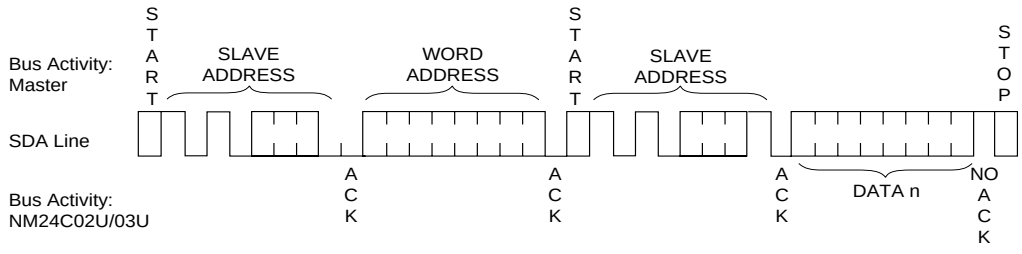
The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. After the entire memory has been read, the counter "rolls over" and the NM24C02U/03U continues to output data for each acknowledge received. Refer to *Figure 10* for the address, acknowledge, and data transfer sequence.

Current Address Read (Figure 8)



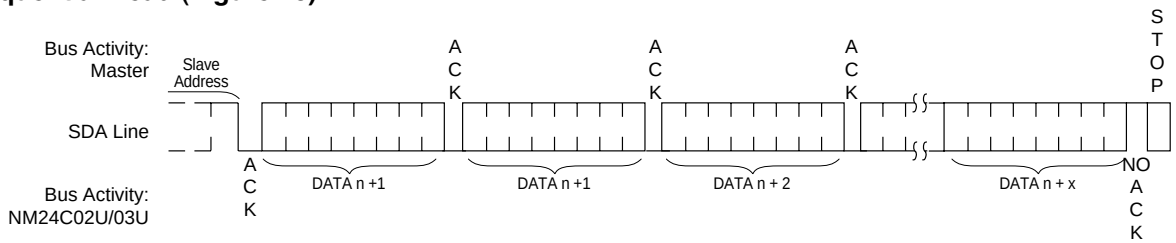
DS800007-17

Random Read (Figure 9)



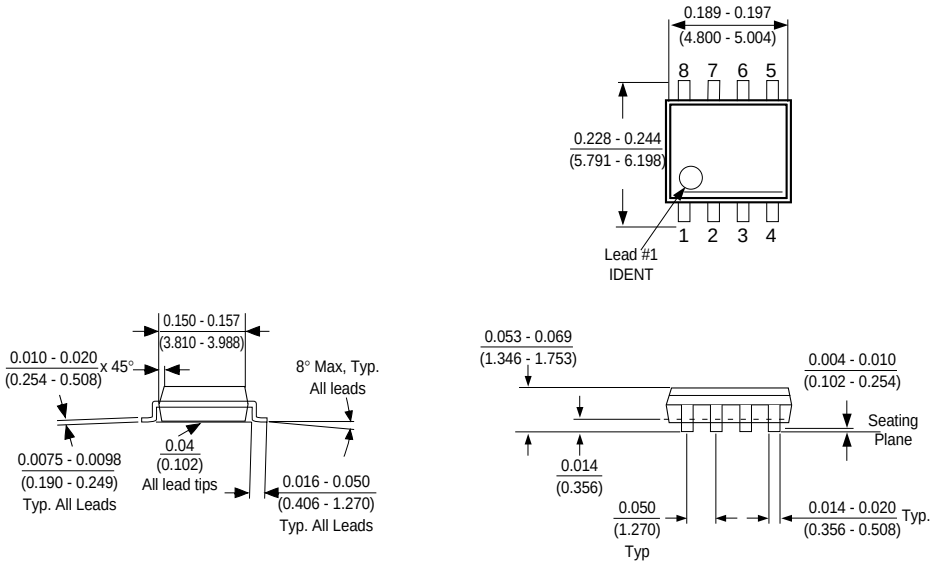
DS800007-18

Sequential Read (Figure 10)

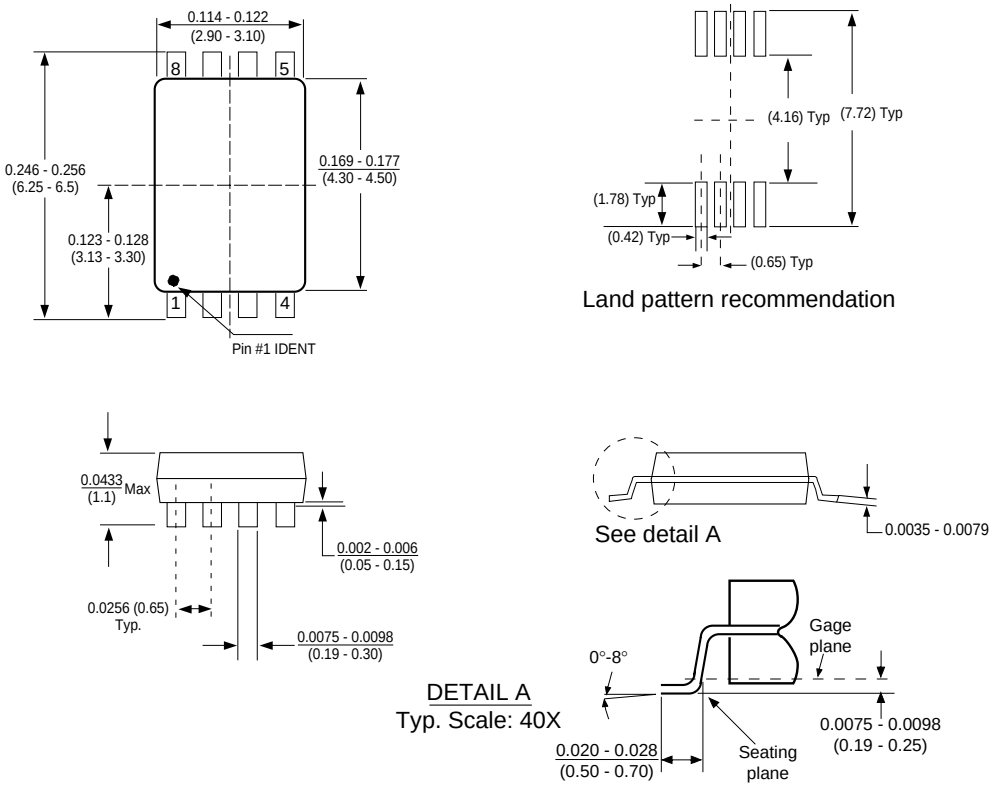


DS800007-19

Physical Dimensions inches (millimeters) unless otherwise noted



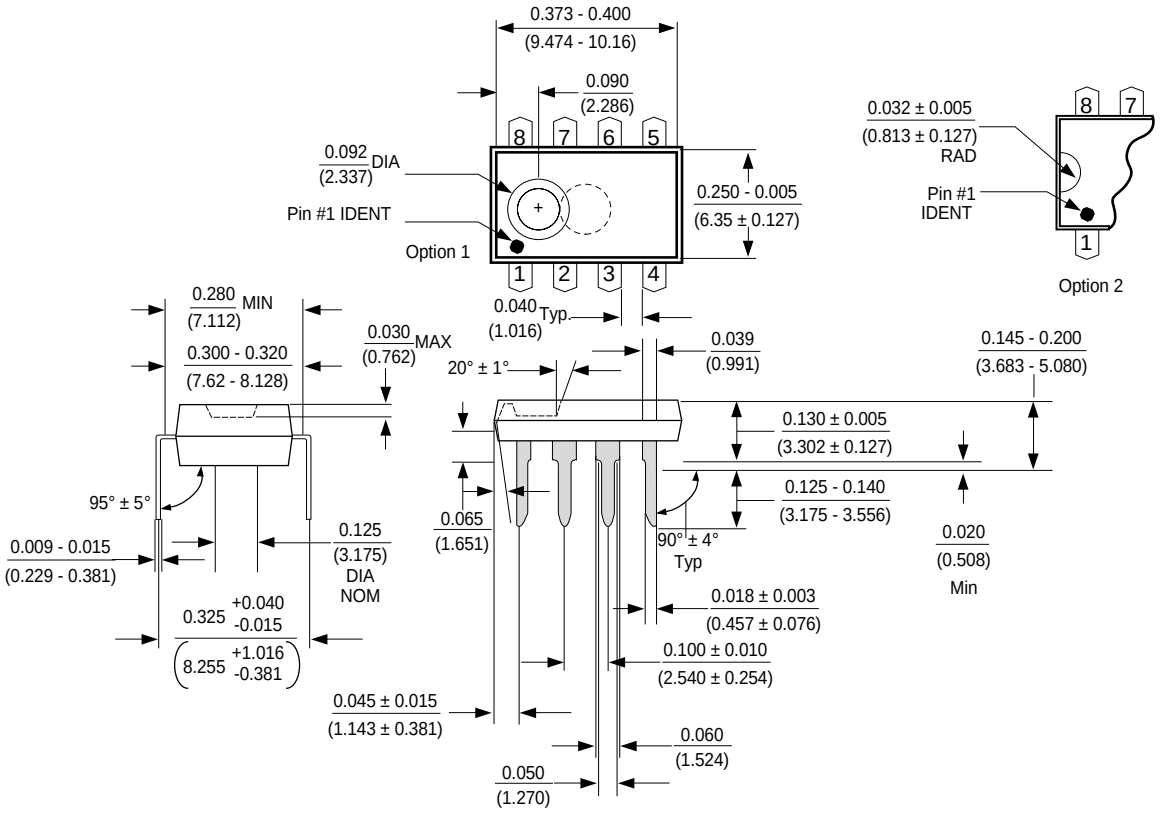
8-Pin Molded Small Outline Package (M8)
Package Number M08A



Notes: Unless otherwise specified
1. Reference JEDEC registration MO153. Variation AA. Dated 7/93

8-Pin Molded Thin Shrink Small Outline Package
Package Number MTC08

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Package Number N08E

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

February 2000

NM24C04/05 – 4K-Bit Standard 2-Wire Bus Interface Serial EEPROM

General Description

The NM24C04/05 devices are 4096 bits of CMOS non-volatile electrically erasable memory. These devices conform to all specifications in the Standard IIC 2-wire protocol and are designed to minimize device pin count, and simplify PC board layout requirements.

The upper half (upper 2Kbit) of the memory of the NM24C05 can be write protected by connecting the WP pin to V_{CC}. This section of memory then becomes unalterable unless WP is switched to V_{SS}.

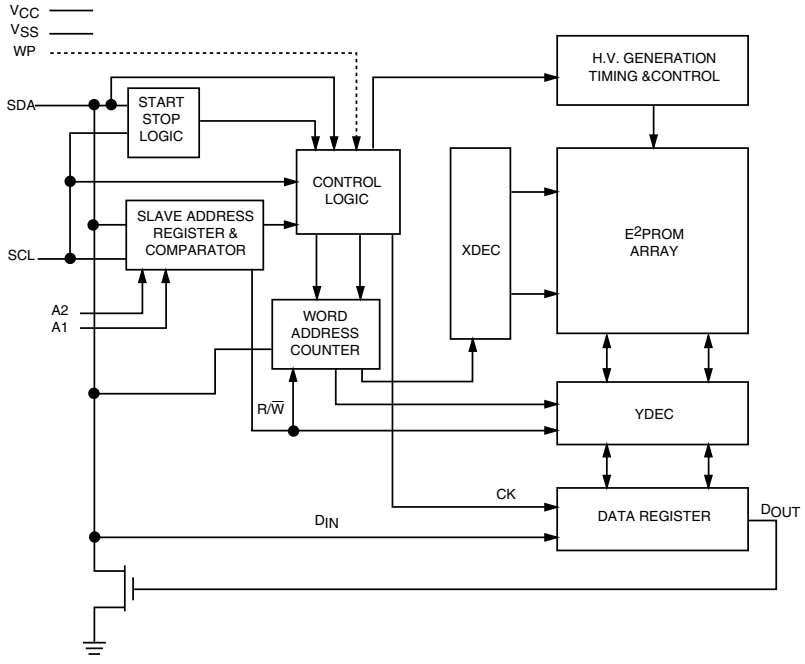
This communications protocol uses CLOCK (SCL) and DATA I/O (SDA) lines to synchronously clock data between the master (for example a microprocessor) and the slave EEPROM device(s). The Standard IIC protocol allows for a maximum of 16K of EEPROM memory which is supported by the Fairchild family in 2K, 4K, 8K, and 16K devices, allowing the user to configure the memory as the application requires with any combination of EEPROMs. In order to implement higher EEPROM memory densities on the IIC bus, the Extended IIC protocol must be used. (Refer to the NM24C32 or NM24C65 datasheets for more information.)

Fairchild EEPROMs are designed and tested for applications requiring high endurance, high reliability and low power consumption.

Features

- Extended operating voltage 2.7V – 5.5V
- 400 KHz clock frequency (F) at 2.7V - 5.5V
- 200µA active current typical
  - 10µA standby current typical
  - 1µA standby current typical (L)
  - 0.1µA standby current typical (LZ)
- IIC compatible interface
  - – Provides bi-directional data transfer protocol
- Schmitt trigger inputs
- Sixteen byte page write mode
  - – Minimizes total write time per byte
- Self timed write cycle
  - Typical write cycle time of 6ms
- Hardware Write Protect for upper half (NM24C05 only)
- Endurance: 1,000,000 data changes
- Data retention greater than 40 years
- Packages available: 8-pin DIP, 8-pin SO, and 8-pin TSSOP
- Available in three temperature ranges
  - - Commercial: 0° to +70°C
  - - Extended (E): -40° to +85C
  - - Automotive (V): -40° to +125°C

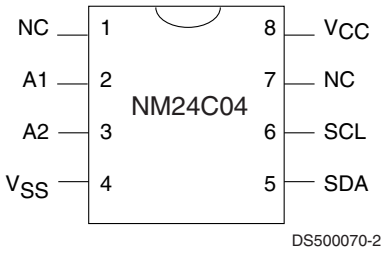
Block Diagram



DS500070-1

Connection Diagrams

Dual-in-Line Package (N), SO Package (M8) and TSSOP Package (MT8)

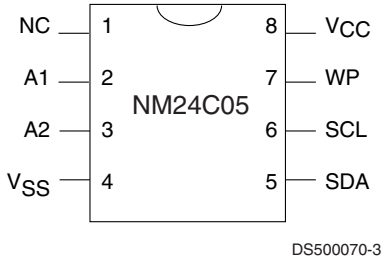


See Package Number N08E, M08A and MTC08

Pin Names

A1,A2	Device Address Inputs
V_{SS}	Ground
SDA	Serial Data I/O
SCL	Serial Clock Input
NC	No Connection
V_{CC}	Power Supply

Dual-in-Line Package (N), SO Package (M8) and TSSOP Package (MT8)

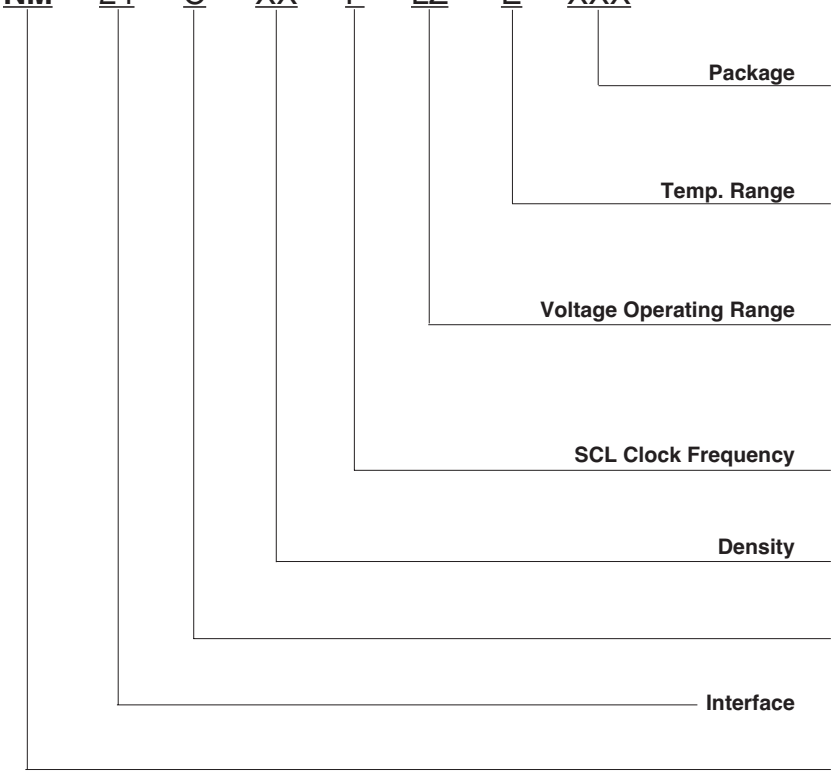


See Package Number N08E, M08A and MTC08

Pin Names

A1,A2	Device Address Inputs
V_{SS}	Ground
SDA	Serial Data I/O
SCL	Serial Clock input
WP	Write Protect
V_{CC}	Power Supply
NC	No Connection

Ordering Information



	Letter	Description
Package	N	8-pin DIP
	M8	8-pin SOIC
	MT8	8-pin TSSOP
Temp. Range	None	0 to 70°C
	V	-40 to +125°C
	E	-40 to +85°C
Voltage Operating Range	Blank	4.5V to 5.5V
	L	2.7V to 5.5V
	LZ	2.7V to 5.5V and <1μA Standby Current
SCL Clock Frequency	Blank	100KHz
	F	400KHz
Density	04	4K
	05	4K with Write Protect
	C	CMOS Technology
Interface	24	IIC
	NM	**Fairchild Non-Volatile Memory**

Product Specifications

Absolute Maximum Ratings

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltages with Respect to Ground	6.5V to –0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min.

Operating Conditions

Ambient Operating Temperature	
NM24C04/05	0°C to +70°C
NM24C04E/05E	-40°C to +85°C
NM24C04V/05V	-40°C to +125°C
Positive Power Supply	
NM24C04/05	4.5V to 5.5V
NM24C04L/05L	2.7V to 5.5V
NM24C04LZ/05LZ	2.7V to 5.5V

DC Electrical Characteristics (2.7V to 5.5V)

Symbol	Parameter	Test Conditions		Limits			Units
				Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 400 KHz f_{SCL} = 100 KHz			0.2	1.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}	V_{CC} = 2.7V - 5.5V V_{CC} = 2.7V - 5.5V (L) V_{CC} = 2.7V - 4.5V (LZ)		10 1 0.1	50 10 1	µA µA µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}			0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}			0.1	1	µA
V_{IL}	Input Low Voltage			–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA				0.4	V

Capacitance T_A = +25°C, f = 100/400 KHz, V_{CC} = 5V (Note 2)

Symbol	Test	Conditions	Max	Units
$C_{I/O}$	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN}	Input Capacitance (A0, A1, A2, SCL)	V_{IN} = 0V	6	pF

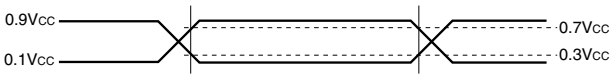
Note 1: Typical values are T_A = 25°C and nominal supply voltage of 5V for 4.5V-5.5V operation and at 3V for 2.7V-4.5V operation.

Note 2: This parameter is periodically sampled and not 100% tested.

AC Test Conditions

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10 ns
Input & Output Timing Levels	V_{CC} x 0.3 to V_{CC} x 0.7
Output Load	1 TTL Gate and C_L = 100 pF

AC Testing Input/Output Waveforms



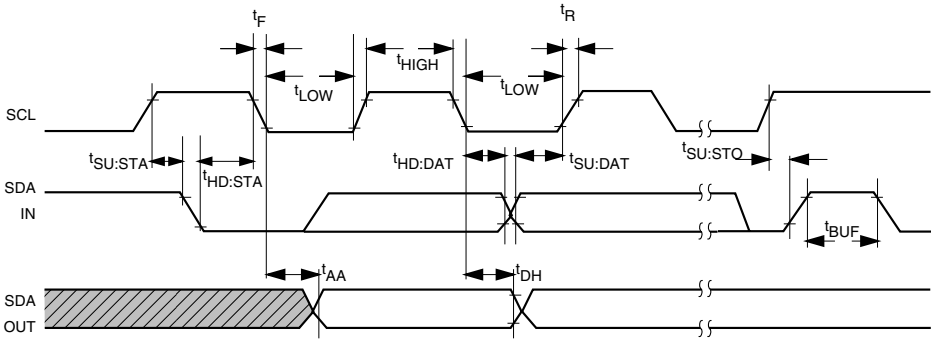
DS500070-4

Read and Write Cycle Limits (Standard and Low V_{CC} Range 2.7V - 5.5V)

Symbol	Parameter	100 KHz		400 KHz		Units
		Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		100		400	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs (Minimum V_{IN} Pulse width)		100		50	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	0.1	0.9	µs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		1.3		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		0.6		µs
t_{LOW}	Clock Low Period	4.7		1.5		µs
t_{HIGH}	Clock High Period	4.0		0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		µs
$t_{HD:DAT}$	Data in Hold Time	20		20		ns
$t_{SU:DAT}$	Data in Setup Time	250		100		ns
t_R	SDA and SCL Rise Time		1		0.3	µs
t_F	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		0.6		µs
t_{DH}	Data Out Hold Time	300		50		ns
t_{WR} (Note 3)	Write Cycle Time - NM24C04/05 - NM24C04/05L, NM24C04/05LZ		10 15		10 15	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the NM24C04/05 bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address. Refer "Write Cycle Timing" diagram.

Bus Timing



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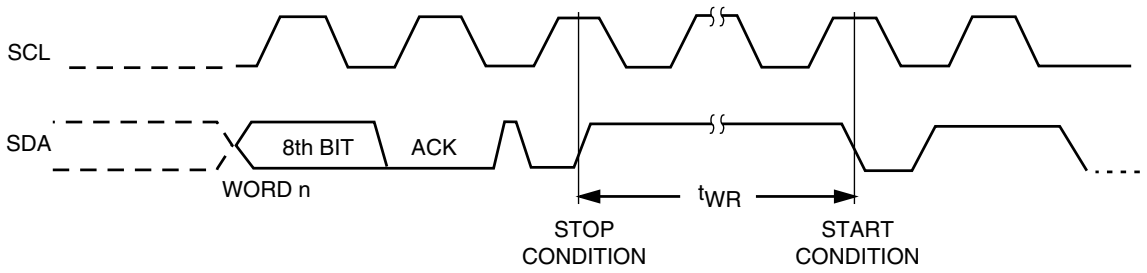
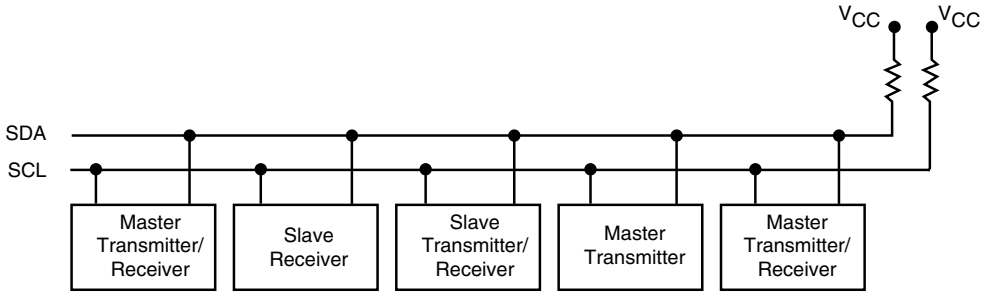
Write Cycle Timing



Note: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle.

DS500070-6

Typical System Configuration



Note: Due to open drain configuration of SDA and SCL, a bus-level pull-up resistor is called for, (typical value = 4.7kΩ)

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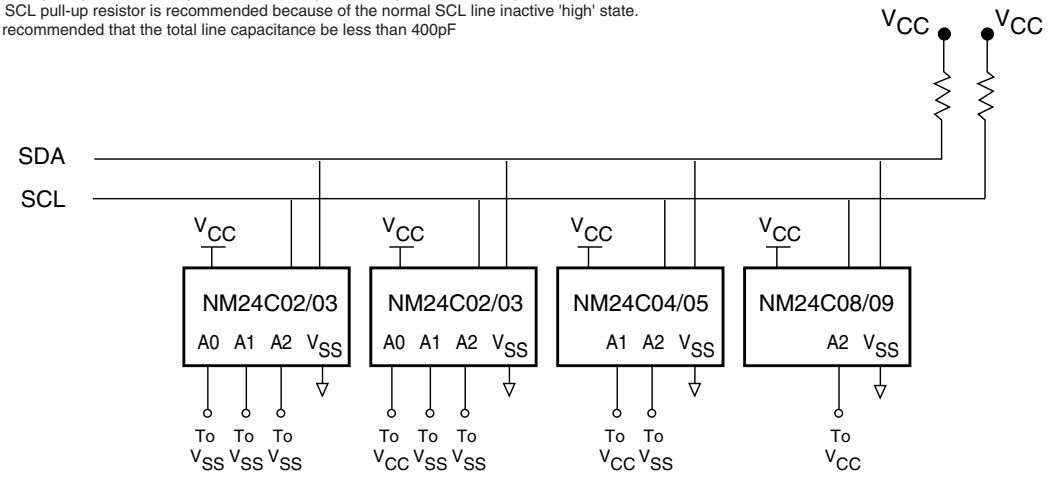
Example of 16K of Memory on 2-Wire Bus

Note: The SDA pull-up resistor is required due to the open-drain/open collector output of IIC bus devices.
The SCL pull-up resistor is recommended because of the normal SCL line inactive 'high' state.
It is recommended that the total line capacitance be less than 400pF



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Device	Address Pins Present			Memory Size	# of Page Blocks
	A0	A1	A2		
NM24C02/03	Yes	Yes	Yes	2048 Bits	1
NM24C04/05	No	Yes	Yes	4096 Bits	2
NM24C08/09	No	No	Yes	8192 Bits	4
NM24C16/17	No	No	No	16,384 Bits	8

Background Information (IIC Bus)

IIC bus allows synchronous bi-directional communication between a TRANSMITTER and a RECEIVER using a Clock signal (SCL) and a Data signal (SDA). Additionally there are up to three Address signals (A2, A1 and A0) which collectively serve as "chip select signal" to a device (example EEPROM) on the IIC bus.

All communication on the IIC bus must be started with a valid START condition (by a MASTER), followed by transmittal (by the MASTER) of byte(s) of information (Address/Data). For every byte of information received, the addressed RECEIVER provides a valid ACKNOWLEDGE pulse to further continue the communication unless the RECEIVER intends to discontinue the communication. Depending on the direction of transfer (Write or Read), the RECEIVER can be a SLAVE or the MASTER. A typical IIC communication concludes with a STOP condition (by the MASTER).

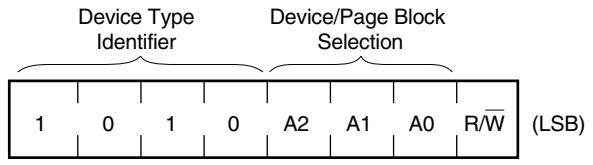
Addressing an EEPROM memory location involves sending a command string with the following information:

[DEVICE TYPE]—[DEVICE/PAGE BLOCK SELECTION]—[R/W BIT]—{acknowledge pulse}—[ARRAY ADDRESS]

Slave Address

Slave Address is an 8-bit information consisting of a Device type field (4bits), Device/Page block selection field (3bits) and Read/Write bit (1bit).

Slave Address Format



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Device Type

IIC bus is designed to support a variety of devices such as RAMs, EPROMs etc., along with EEPROMS. Hence to properly identify various devices on the IIC bus, a 4-bit “Device Type” identifier string is used. For EEPROMS, this 4-bit string is 1-0-1-0. Every IIC device on the bus internally compares this 4-bit string to its own “Device Type” string to ensure proper device selection.

Device/Page Block Selection

When multiple devices of the same type (e.g. multiple EEPROMS) are present on the IIC bus, then the A2, A1 and A0 address information bits are also used as part of the Slave Address. Every IIC device on the bus internally compares this 3-bit string to its own physical configuration (A2, A1 and A0 pins) to ensure proper device selection. This comparison is in addition to the “Device Type” comparison. In addition to selecting an EEPROM, these 3 bits are also used to select a “page block” within the selected EEPROM. Each page block is 2Kbit (256Bytes) in size. Depending on the density, an EEPROM can contain from a minimum of 1 to a maximum of 8 page blocks (in multiples of 2) and selection of a page block within a device is by using A2, A1 and A0 bits.

Read/Write Bit

Last bit of the Slave Address indicates if the intended access is Read or Write. If the bit is "1," then the access is Read, whereas if the bit is "0," then the access is Write.

Acknowledge

Acknowledge is an active LOW pulse on the SDA line driven by an addressed receiver to the addressing transmitter to indicate receipt of 8-bits of data. The receiver provides an ACK pulse for every 8-bits of data received. This handshake mechanism is done as follows: After transmitting 8-bits of data, the transmitter releases the SDA line and waits for the ACK pulse. The addressed receiver, if present, drives the ACK pulse on the SDA line during the 9th clock and releases the SDA line back (to the transmitter). Refer *Figure 3*.

Array Address

Array address is an 8-bit information containing the address of a memory location to be selected within a page block of the device.

16K bit Addressing Limitation:

Standard IIC specification limits the maximum size of EEPROM memory on the bus to 16K bits. This limitation is due to the addressing protocol implemented which consists of the 8-bit Slave Address and an additional 8-bit field called Array Address. This Array Address selects 1 out of 256 locations (2^8=256). Since the data format of IIC specification is 8-bit wide, a total of 256 x 8 = 2048 = 2K bit now becomes addressable by this 8-bit Array Address. This 2K bit is typically referred as a “Page Block”. Combining this 8-bit Array Address with the 3-bit Device/Page address (part of Slave Address) allows a maximum of 8 pages (2^3=8) of memory that can be addressed. Since each page is 2K bit in size, 8 x 2K bit = 16K bit is the maximum size of memory that is addressable on the Standard IIC bus. This 16Kb of memory can be in the form of a single 16Kb EEPROM device or multiple EEPROMs of varying density (in 2Kb multiples) to a maximum total of 16Kb. To address the needs of systems that require more than 16Kb on the IIC bus, a different specification called “Extended IIC Specification” is used. Please refer to NM24C32xx Datasheet for more information on Extended IIC Specification.

DEFINITIONS	
WORD	8 bits (byte) of data
PAGE	16 sequential byte locations starting at a 16-byte address boundary, that may be programmed during a "page write" programming cycle
PAGE BLOCK	2048 (2K) bits organized into 16 pages of addressable memory. (8 bits) x (16 bytes) x (16 pages) = 2048 bits
MASTER	Any IIC device CONTROLLING the transfer of data (such as a microprocessor)
SLAVE	Device being controlled (EEPROMs are always considered Slaves)
TRANSMITTER	Device currently SENDING data on the bus (may be either a Master or Slave).
RECEIVER	Device currently RECEIVING data on the bus (Master or Slave)

Pin Descriptions

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bi-directional pin used to transfer data into and out of the device. It is an open drain output and may be wire–ORed with any number of open drain or open collector outputs.

Write Protect (WP) (NM24C05 Only)

If tied to V_{CC}, PROGRAM operations onto the upper half (upper 2Kbit) of the memory will not be executed. READ operations are possible. If tied to V_{SS}, normal operation is enabled, READ/WRITE over the entire memory is possible.

This feature allows the user to assign the upper half of the memory as ROM which can be protected against accidental programming. When write is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

This pin has an internal pull-down circuit. However, on systems where write protection is not required it is recommended that this pin is tied to V_{SS}.

Device Selection Inputs A2, A1 and A0 (as appropriate)

These inputs collectively serve as "chip select" signal to an EEPROM when multiple EEPROMs are present on the same IIC bus. Hence these inputs, if present, should be connected to V_{CC} or V_{SS} in a unique manner to allow proper selection of an EEPROM amongst multiple EEPROMs. During a typical addressing sequence, every EEPROM on the IIC bus compares the configuration of these inputs to the respective 3 bit "Device/Page block selection" information (part of slave address) to determine a valid selection. For e.g. if the 3 bit "Device/Page block selection" is 1-0-1, then the EEPROM whose "Device Selection inputs" (A2, A1 and A0) are connected to V_{CC}-V_{SS}-V_{CC} respectively, is selected.

Depending on the density, only appropriate number of "Device Selection inputs" are provided on an EEPROM. For every "Device selection input" that is not present on the device, the corresponding bit in the "Device/Page block selection" field is used to select a "Page Block" within the device instead of the device itself. Following table illustrates the above:

EEPROM Density	Number of Page Blocks	Device Selection Inputs Provided			Address Bits Selecting Page Block
2k bit	1	A0	A1	A2	None
4k bit	2	—	A1	A2	A0
8k bit	4	—	—	A2	A0 and A1
16k bit	8	—	—	—	A0, A1 and A2

Note that even when just one EEPROM present on the IIC bus, these pins should be tied to V_{CC} or V_{SS} to ensure proper termination.

Device Operation

The NM24C04/05 supports a bi-directional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the NM24C04/05 will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to *Figure 1* and *Figure 2* on next page.

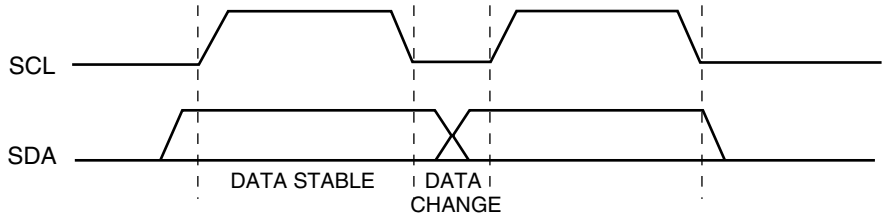
Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The NM24C04/05 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Stop Condition

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the NM24C04/05 to place the device in the standby power mode, except when a Write operation is being executed, in which case a second stop condition is required after t_{WR} period, to place the device in standby mode.

Data Validity (Figure 1)



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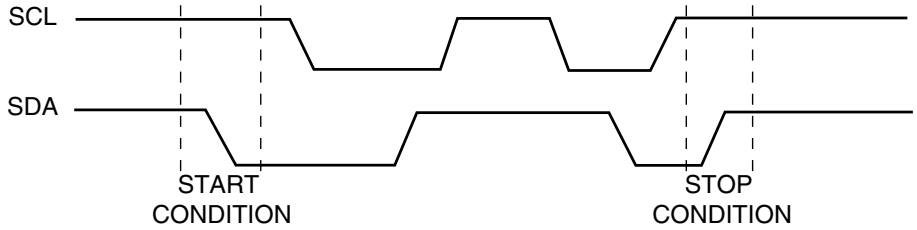
Start and Stop Definition (Figure 2)



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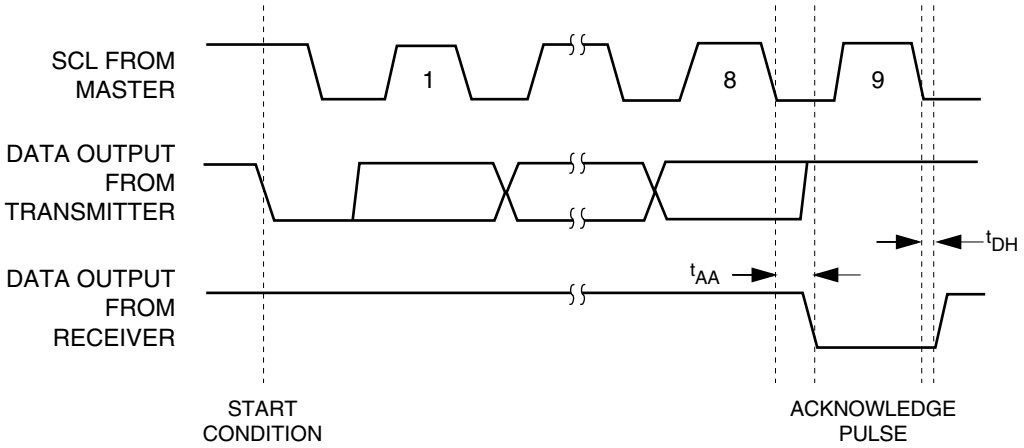
Acknowledge Response from Receiver (Figure 3)



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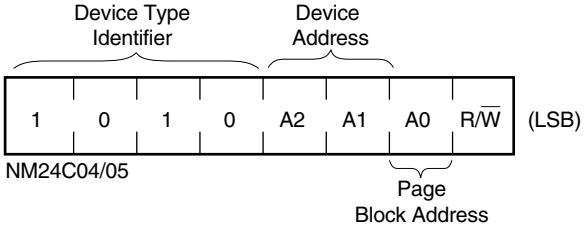
Acknowledge

The NM24C04/05 device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the NM24C04/05 will respond with an acknowledge after the receipt of each subsequent eight bit byte.

In the read mode the NM24C04/05 slave will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected, NM24C04/05 will continue to transmit data. If an acknowledge is not detected,NM24C04/05 will terminate further data transmissions and await the stop condition to return to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are those of the device type identifier. This is fixed as 1010 for all EEPROM devices.



Refer the following table for Slave Addresses string details:

Device	A0	A1	A2	Page Blocks	Page Block Addresses
NM24C04/05	P	A	A	2	0, 1

A: Refers to a hardware configured Device Address pin.

P: Refers to an internal PAGE BLOCK.

All IIC EEPROMs use an internal protocol that defines a PAGE BLOCK size of 2K bits (for Word addresses 0x00 through 0xFF). Therefore, address bits A0, A1, or A2 (if designated 'P') are used to access a PAGE BLOCK in conjunction with the Word address used to access any individual data byte.

The last bit of the slave address defines whether a write or read condition is requested by the master. A '1' indicates that a read operation is to be executed, and a '0' initiates the write mode.

A simple review: After the NM24C04/05 recognizes the start condition, the devices interfaced to the IIC bus wait for a slave address to be transmitted over the SDA line. If the transmitted slave address matches an address of one of the devices, the designated slave pulls the line LOW with an acknowledge signal and awaits further transmissions.

Write Operations

BYTE WRITE

For a write operation a second address field is required which is a word address that is comprised of eight bits and provides access to any one of the 256 bytes in the selected page of memory. Upon receipt of the byte address the NM24C04/05 responds with an acknowledge and waits for the next eight bits of data, again, responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the NM24C04/05 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the NM24C04/05 inputs are disabled, and the device will not respond to any requests from the master for the duration of t_{WR}. Refer to *Figure 4* for the address, acknowledge and data transfer sequence.

PAGE WRITE

To minimize write cycle time, NM24C04/05 offer Page Write feature, by which, up to a maximum of 16 contiguous bytes locations can be programmed all at once (instead of 16 individual byte writes). To facilitate this feature, the memory array is organized in terms of "Pages." A Page consists of 16 contiguous byte locations starting at every 16-Byte address boundary (for example, starting at array address 0x00, 0x10, 0x20 etc.). Page Write operation limits access to byte locations within a page. In other words a single Page Write operation will not cross over to locations on another page but will "roll over" to the beginning of the page whenever end of Page is reached and additional locations are a continued to be accessed. A Page Write operation can be initiated to begin at any location within a page (starting address of the Page Write operation need not be the starting address of a Page).

Page Write is initiated in the same manner as the Byte Write operation; but instead of terminating the cycle after transmitting the first data byte, the master can further transmit up to 15 more bytes. After the receipt of each byte, NM24C04/05 will respond with an acknowledge pulse, increment the internal address counter to the next address and is ready to accept the next data. If the master should transmit more than sixteen bytes prior to generating the STOP condition, the address counter will "roll over" and previously written data will be overwritten. As with the Byte Write operation, all inputs are disabled until completion of the internal write cycle. Refer to *Figure 5* for the address, acknowledge and data transfer sequence.

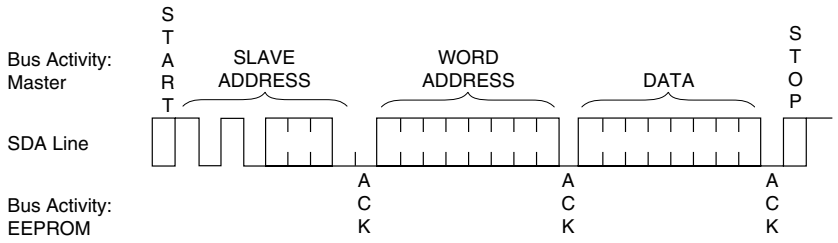
Acknowledge Polling

Once the stop condition is issued to indicate the end of the host's write operation the NM24C04/05 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the NM24C04/05 is still busy with the write operation no ACK will be returned. If the NM24C04/05 has completed the write operation an ACK will be returned and the host can then proceed with the next read or write operation.

Write Protection (NM24C05 Only)

Programming of the upper half (upper 2Kbit) of the memory will not take place if the WP pin of the NM24C05 is connected to V_{CC}. The NM24C05 will respond to slave and byte addresses; but if the memory accessed is write protected by the WP pin, the NM24C05 will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the stop condition is asserted.

Byte Write (Figure 4)



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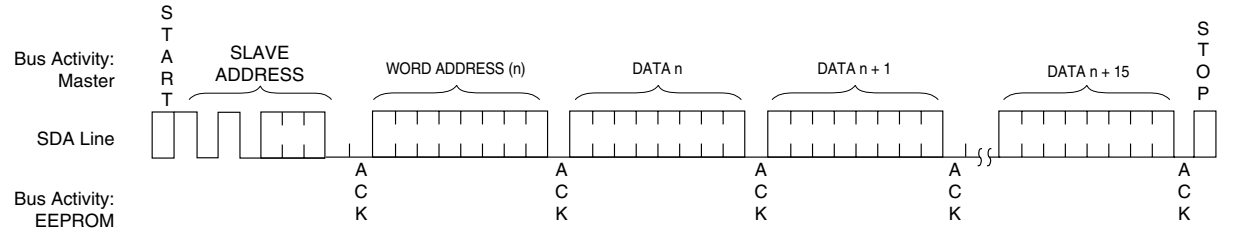
Page Write (Figure 5)



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Read Operations

Read operations are initiated in the same manner as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to a one. There are three basic read operations: current address read, random read, and sequential read.

Current Address Read

Internally the NM24C04/05 contains an address counter that maintains the address of the last byte accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ set to one, the NM24C04/05 issues an acknowledge and transmits the eight bit byte. The master will not acknowledge the transfer but does generate a stop condition, and therefore the NM24C04/05 discontinues transmission. Refer to *Figure* 6 for the sequence of address, acknowledge and data transfer.

Random Read

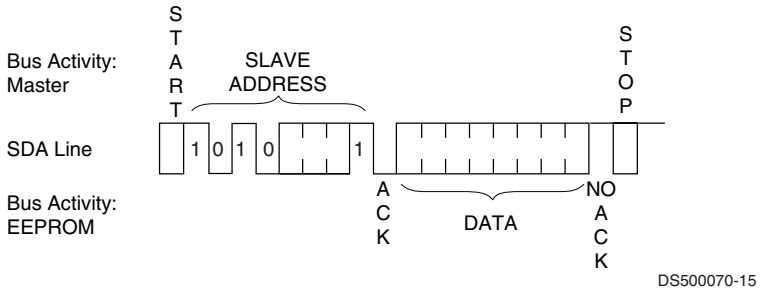
Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, slave address with the R/$\overline{W}$ bit set to zero and then the byte address it is to read. After the byte address acknowledge, the master immediately issues another start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the NM24C04/05 and then by the eight bit byte. The master will not acknowledge the transfer but does generate the stop condition, and therefore the NM24C04/05 discontinues transmission. Refer to *Figure 7* for the address, acknowledge and data transfer sequence.

Sequential Read

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted in the same manner as the other read modes; however, the master now responds with an acknowledge, indicating it requires additional data. The NM24C04/05 continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge or by generating a stop condition.

The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. After the entire memory has been read, the counter "rolls over" to the beginning of the memory. NM24C04/05 continues to output data for each acknowledge received. Refer to *Figure 8* for the address, acknowledge, and data transfer sequence.

Current Address Read (Figure 6)



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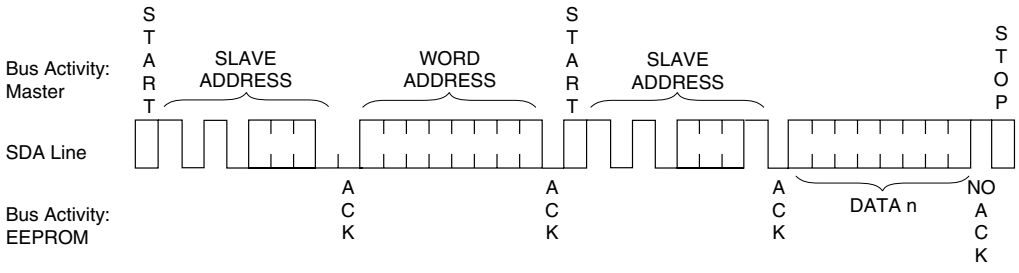
Random Read (Figure 7)



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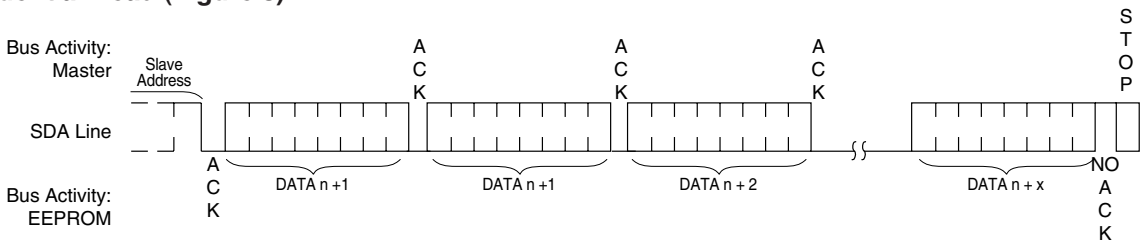
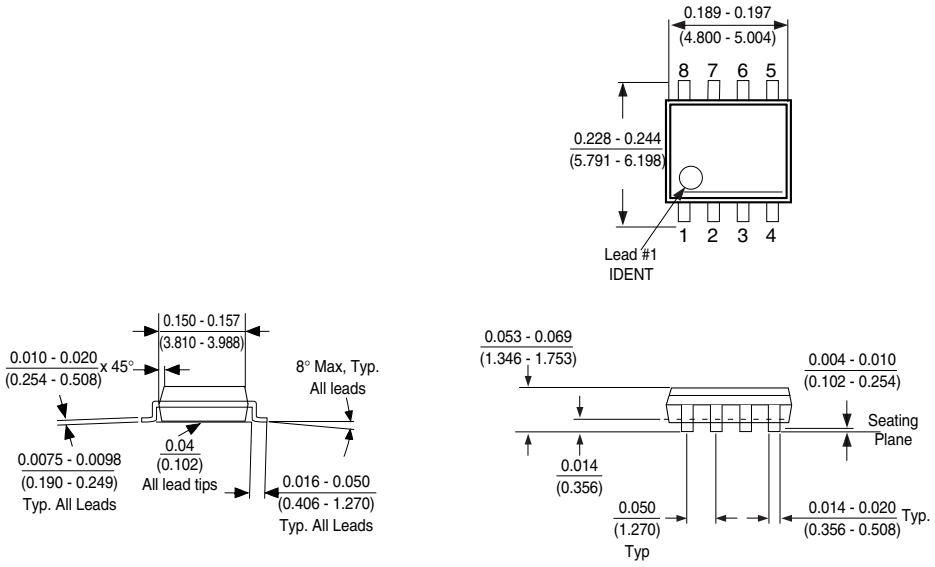
Sequential Read (Figure 8)

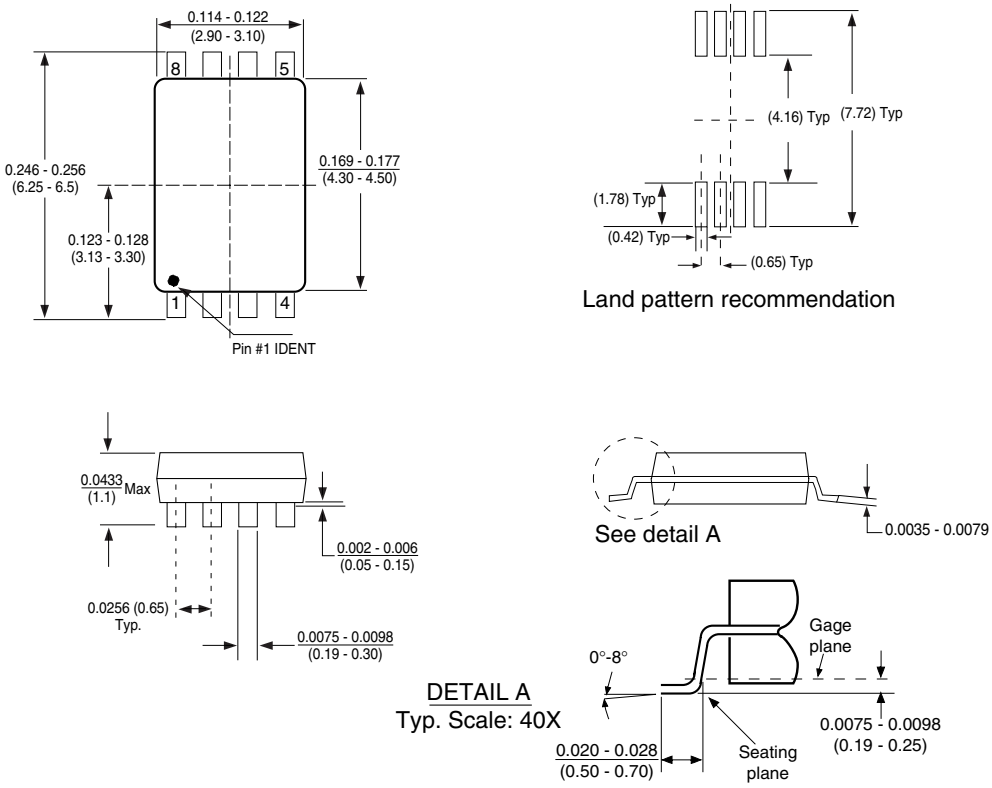


DS500070-17

Physical Dimensions inches (millimeters) unless otherwise noted



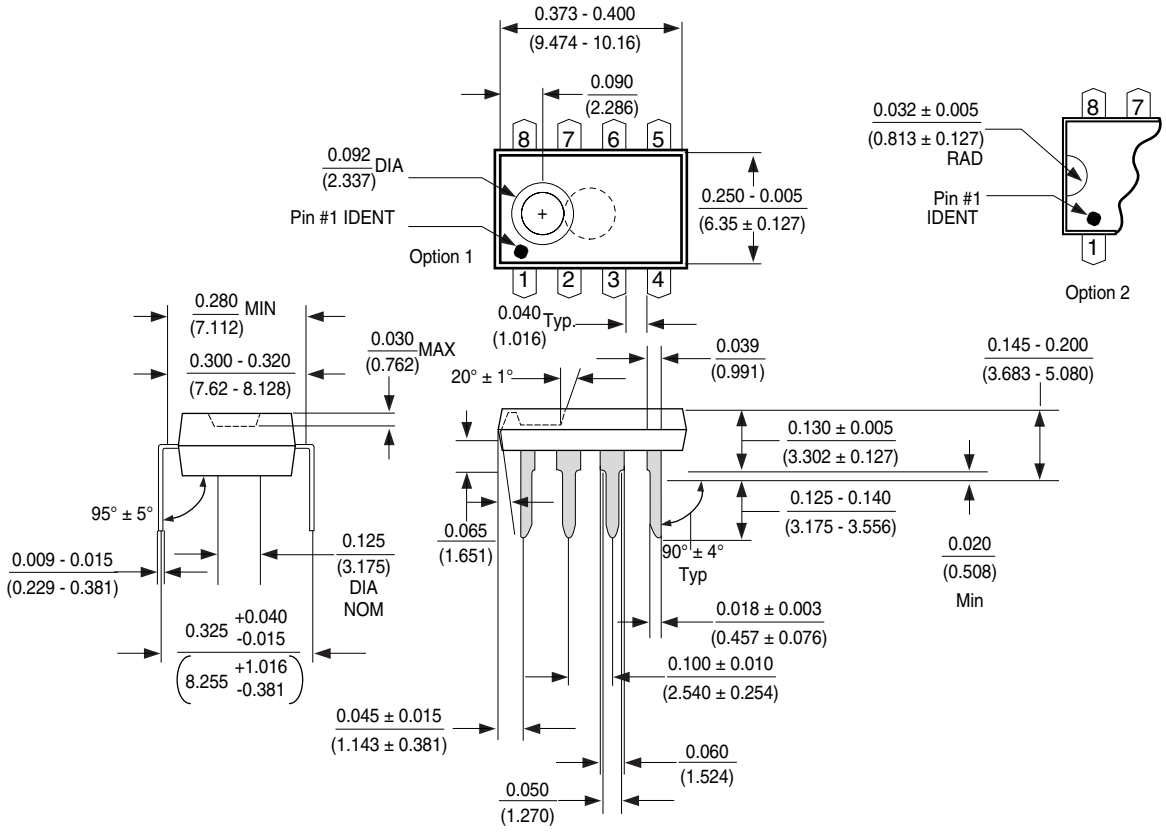
8-Pin Molded Small Outline Package (M8)
Package Number M08A



Notes: Unless otherwise specified
1. Reference JEDEC registration MO153. Variation AA. Dated 7/93

8-Pin Molded Thin Shrink Small Outline Package (MT8)
Package Number MTC08

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Package Number N08E

Life Support Policy

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

August 1999

NM24C04U/NM24C05U 4K-Bit Serial EEPROM 2-Wire Bus Interface

General Description

The NM24C04U/05U devices are 4K (4,096) bit serial interface CMOS EEPROMs (Electrically Erasable Programmable Read-Only Memory). These devices fully conform to the **Standard** I²C™ 2-wire protocol which uses Clock (SCL) and Data I/O (SDA) pins to synchronously clock data between the "master" (for example a microprocessor) and the "slave" (the EEPROM device). In addition, the serial interface allows a minimal pin count packaging designed to simplify PC board layout requirements and offers the designer a variety of low voltage and low power options.

NM24C05U incorporates a hardware "Write Protect" feature, by which, the upper half of the memory can be disabled against programming by connecting the WP pin to V_{CC}. This section of memory then effectively becomes a ROM (Read-Only Memory) and can no longer be programmed as long as WP pin is connected to V_{CC}.

Fairchild EEPROMs are designed and tested for applications requiring high endurance, high reliability and low power consumption for a continuously reliable non-volatile solution for all markets.

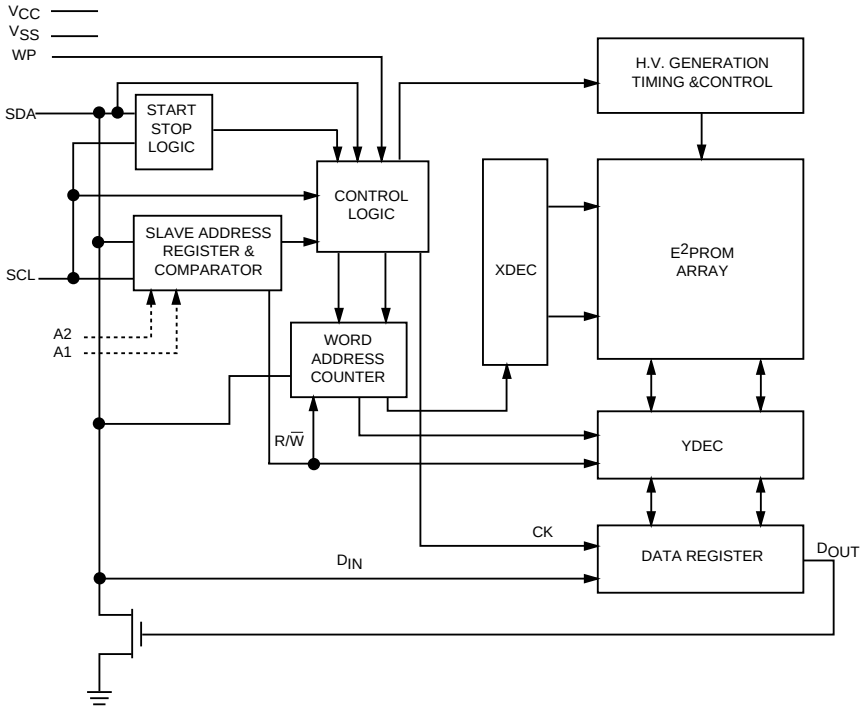
Functions

- I²C™ compatible interface
- 4,096 bits organized as 512 x 8
- Extended 2.7V – 5.5V operating voltage
- 100 KHz or 400 KHz operation
- Self timed programming cycle (6ms typical)
- "Programming complete" indicated by ACK polling
- NM24C05U: Memory "Upper Block" Write Protect pin

Features

- The I²C™ interface allows the smallest I/O pincount of any EEPROM interface
- 16 byte page write mode to minimize total write time per byte
- Typical 200µA active current (I_{CCA})
- Typical 1µA standby current (I_{SB}) for "L" devices and 0.1µA standby current for "LZ" devices
- Endurance: Up to 1,000,000 data changes
- Data retention greater than 40 years

Block Diagram

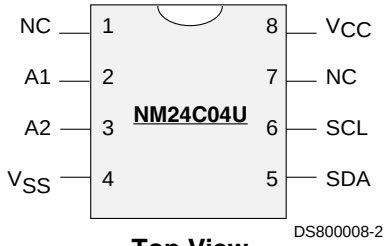


DS800008-1

I²C™ is a registered trademark of Philips Electronics N.V.

Connection Diagrams

Dual-in-Line Package (N), SO Package (M8), and TSSOP Package (MT8)



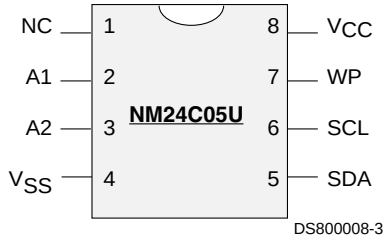
Top View

See Package Number N08E, M08A, and MTC08

Pin Names

A1,A2	Device Address Inputs
V_{SS}	Ground
SDA	Serial Data I/O
SCL	Serial Clock Input
NC	No Connection
V_{CC}	Power Supply

Dual-in-Line Package (N), SO Package (M8), and TSSOP Package (MT8)



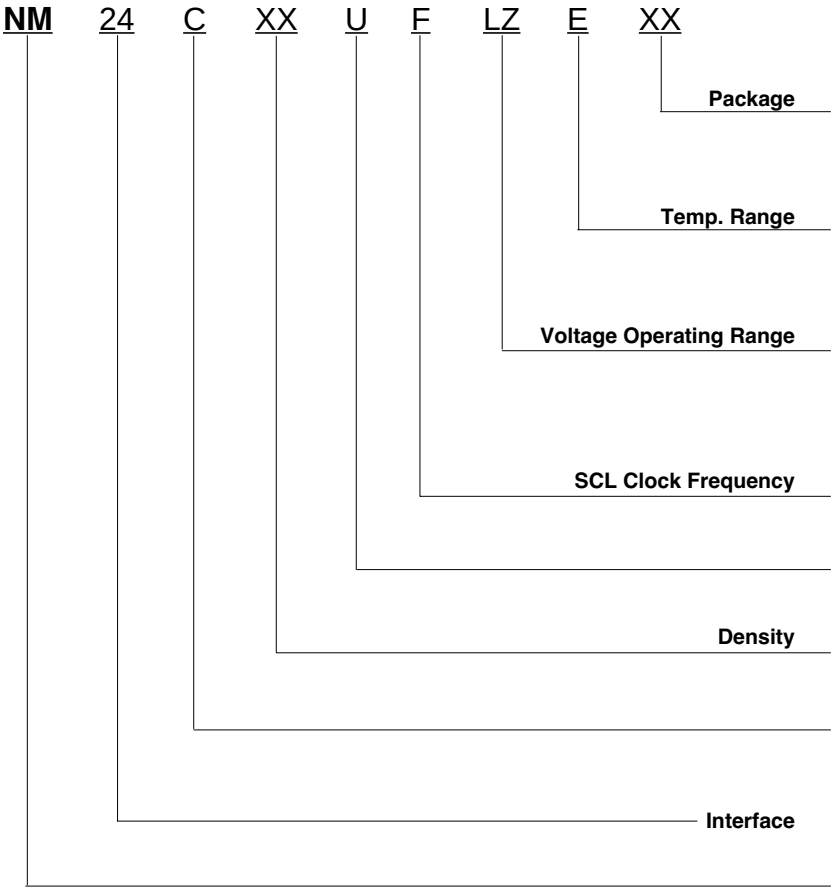
Top View

See Package Number N08E, M08A, and MTC08

Pin Names

NC	No Connection
A1,A2	Device Address Inputs
V_{SS}	Ground
SDA	Serial Data I/O
SCL	Serial Clock input
WP	Write Protect
V_{CC}	Power Supply

Ordering Information



	Letter	Description
Package	N	8-pin DIP
	M8	8-pin SOIC
	MT8	8-pin TSSOP
Temp. Range	None	0 to 70°C
	V	-40 to +125°C
	E	-40 to +85°C
Voltage Operating Range	Blank	4.5V to 5.5V
	L	2.7V to 5.5V
	LZ	2.7V to 5.5V and <1µA Standby Current
SCL Clock Frequency	Blank	100KHz
	F	400KHz
	Ultralite	CS100UL Process
Density	04	4K
	05	4K with Write Protect
	C	CMOS Technology
	W	Total Array Write Protect
Interface	24	IIC
NM		**Fairchild Non-Volatile Memory**

Product Specifications

Absolute Maximum Ratings

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltages with Respect to Ground	6.5V to –0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min.

Operating Conditions

Ambient Operating Temperature	
NM24C04U/05U	0°C to +70°C
NM24C04UE/05UE	-40°C to +85°C
NM24C04UV/05UV	-40°C to +125°C
Positive Power Supply	
NM24C04U/05U	4.5V to 5.5V
NM24C04UL/05UL	2.7V to 5.5V
NM24C04ULZ/05ULZ	2.7V to 5.5V

Standard V_{CC} (4.5V to 5.5V) DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 400 KHz f_{SCL} = 100 KHz		0.2	1.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		10	50	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	1	µA
V_{IL}	Input Low Voltage		–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Low V_{CC} (2.7V to 5.5V) DC Electrical Characteristics

Symbol	Parameter	Test Conditions		Limits			Units
				Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 400 KHz f_{SCL} = 100 KHz			0.2	1.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}	V_{CC} = 2.7V - 4.5V V_{CC} = 2.7V - 4.5V V_{CC} = 4.5V - 5.5V		1 0.1 10	10 1 50	µA µA µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}			0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}			0.1	1	µA
V_{IL}	Input Low Voltage			–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA				0.4	V

Capacitance T_A = +25°C, f = 100/400 KHz, V_{CC} = 5V (Note 2)

Symbol	Test	Conditions	Max	Units
$C_{I/O}$	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN}	Input Capacitance (A0, A1, A2, SCL)	V_{IN} = 0V	6	pF

Note 1: Typical values are T_A = 25°C and nominal supply voltage (5V).

Note 2: This parameter is periodically sampled and not 100% tested.

AC Conditions of Test

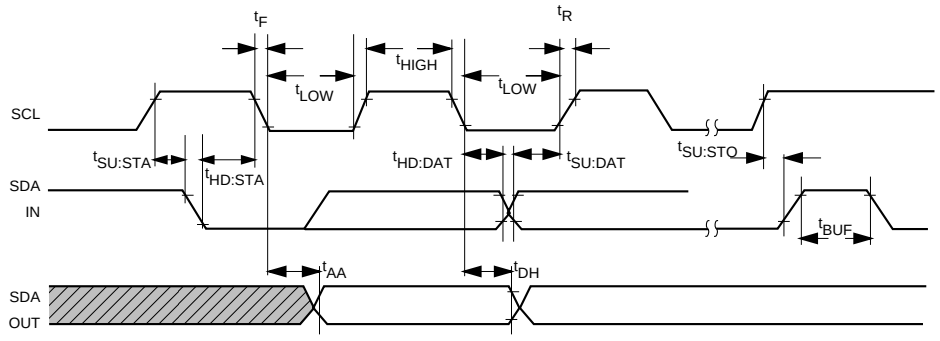
Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10 ns
Input & Output Timing Levels	V_{CC} x 0.5
Output Load	1 TTL Gate and C_L = 100 pF

Read and Write Cycle Limits (Standard and Low V_{CC} Range 2.7V - 5.5V)

Symbol	Parameter	100 KHz		400 KHz		Units
		Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		100		400	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs (Minimum V_{IN} Pulse width)		100		50	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	0.1	0.9	µs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		1.3		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		0.6		µs
t_{LOW}	Clock Low Period	4.7		1.5		µs
t_{HIGH}	Clock High Period	4.0		0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		µs
$t_{HD:DAT}$	Data in Hold Time	0		0		µs
$t_{SU:DAT}$	Data in Setup Time	250		100		ns
t_R	SDA and SCL Rise Time		1		0.3	µs
t_F	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		0.6		µs
t_{DH}	Data Out Hold Time	300		50		ns
t_{WR} (Note 3)	Write Cycle Time - NM24C04U/05U - NM24C04U/05UL, NM24C04U/05ULZ		10 15		10 15	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the NM24C04U/05U bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

Bus Timing



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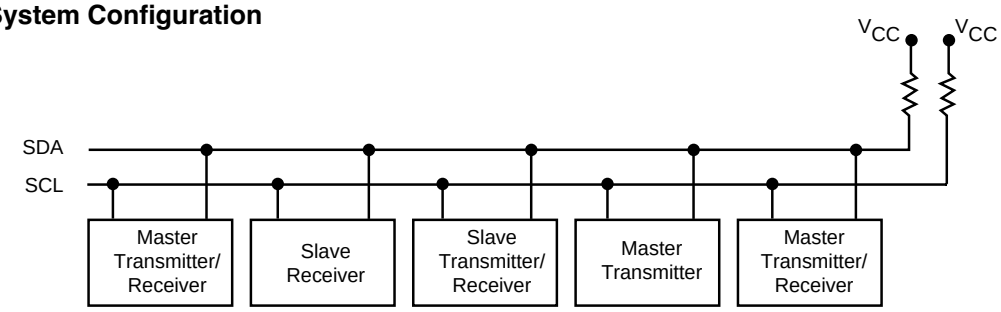
System Layout

Typical System Configuration



Note: Due to open drain configuration of SDA, a bus-level pull-up resistor is called for, (typical value = 4.7kΩ)

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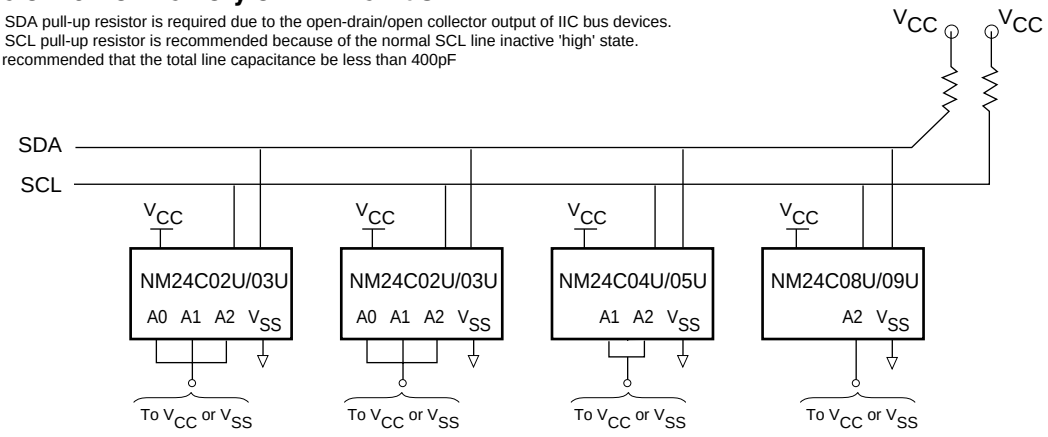
Example of 16K of Memory on 2-Wire Bus

Note: The SDA pull-up resistor is required due to the open-drain/open collector output of IIC bus devices. The SCL pull-up resistor is recommended because of the normal SCL line inactive 'high' state. It is recommended that the total line capacitance be less than 400pF



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Device	Address Pins			Memory Size	# of Page Blocks
	A0	A1	A2		
NM24C04U/05U	No Connect	ADR	ADR	4096 Bits	2

Device Operation Inputs (A1, A2)

Device address pins A1 and A2 are connected to V_{CC} or V_{SS} to configure the EEPROM chip address. Table I shows the active pins.

Table 1.

Device	A0	A1	A2	Effects of Addresses
NM24C04U/05U	x	ADR	ADR	2^2 = 4; 4*x (2x2K)** = 16K

* Max # of devices on bus ** Number of page blocks per density

Under the Standard IIC protocol the maximum density addressable using the three pin configuration of the IIC protocol is 16K. Any combination of densities can be used up to this limit.

Background Information (IIC Bus)

As mentioned, the IIC bus allows synchronous bidirectional communication between Transmitter/Receiver using the SCL (clock) and SDA (Data I/O) lines. All communication must be started with a valid START condition, concluded with a STOP condition and acknowledged by the Receiver with an ACKNOWLEDGE condition.

As shown below, the EEPROMs on the IIC bus may be configured in any manner required, the total memory addressed can not exceed 16K (16,384 bits). EEPROM memory address programming is controlled by 2 methods:

- Hardware configuring the A1 and A2 pins (Device Address pins) with pull-up or pull-down to V_{CC} or V_{SS}. **All unused pins must be grounded** (tied to V_{SS}).
- Software addressing the required PAGE BLOCK within the device memory array (as sent in the Slave Address string).

For devices with densities greater than 16K, a different protocol, the Extended IIC protocol, is used. Refer to NM24C32U datasheet (for example) for additional details.

Addressing an EEPROM memory location involves sending a command string with the following information: [DEVICE TYPE]–[DEVICE ADDRESS]–[PAGE BLOCK ADDRESS]–[BYTE ADDRESS]

DEFINITIONS	
WORD	8 bits (byte) of data
PAGE	16 sequential addresses (one byte each) that may be programmed during a 'Page Write' programming cycle
PAGE BLOCK	2048 (2K) bits organized into **16 pages of addressable memory. (8 bits) x (16 bytes) x (16 pages) = 2048 bits**
MASTER	Any IIC device CONTROLLING the transfer of data (such as a microprocessor)
SLAVE	Device being controlled (EEPROMs are always considered Slaves)
TRANSMITTER	Device currently SENDING data on the bus (may be either a Master or Slave).
RECEIVER	Device currently RECEIVING data on the bus (Master or Slave)

Pin Descriptions

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire–ORed with any number of open drain or open collector outputs.

WP Write Protection (NM24C05U Only)

If tied to V_{CC}, PROGRAM operations onto the upper half of the memory will not be executed. READ operations are possible. If tied to V_{SS}, normal operation is enabled, READ/WRITE over the entire memory is possible.

This feature allows the user to assign the upper half of the memory as ROM which can be protected against accidental programming. When write is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

Device Operation

The NM24C04U/05U supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the NM24C04U/05U will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to *Figure 2* and *Figure 3* on next page.

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The NM24C04U/05U continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Stop Condition

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the NM24C04U/05U to place the device in the standby power mode.

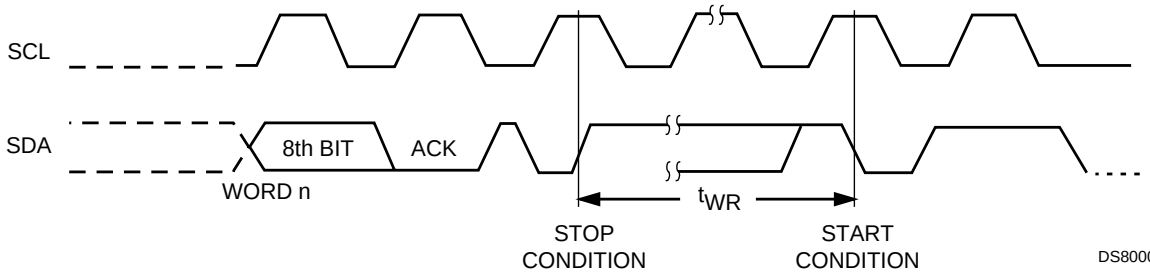
Write Cycle Timing

Acknowledge

Acknowledge is a hardware convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits.

During the ninth clock cycle the receiver will pull the SDA line to LOW to acknowledge that it received the eight bits of data. Refer to *Figure 4.*

Write Cycle Timing (Figure 1)



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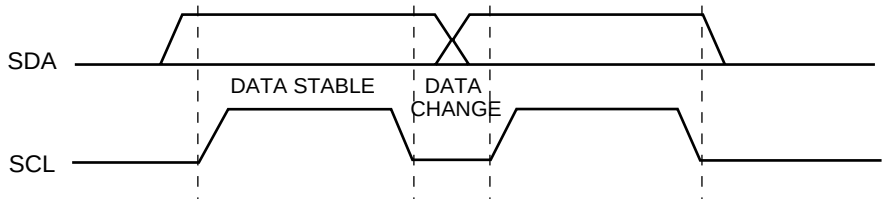
Note: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle.

Data Validity (Figure 2)



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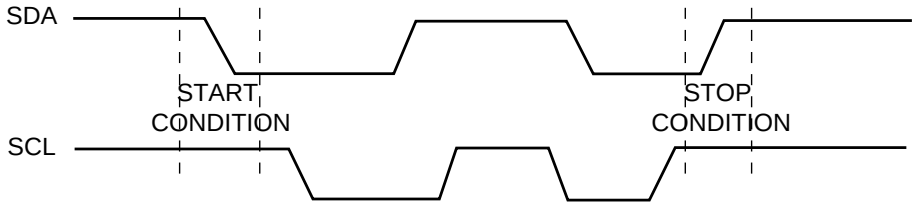
Start and Stop Definition (Figure 3)



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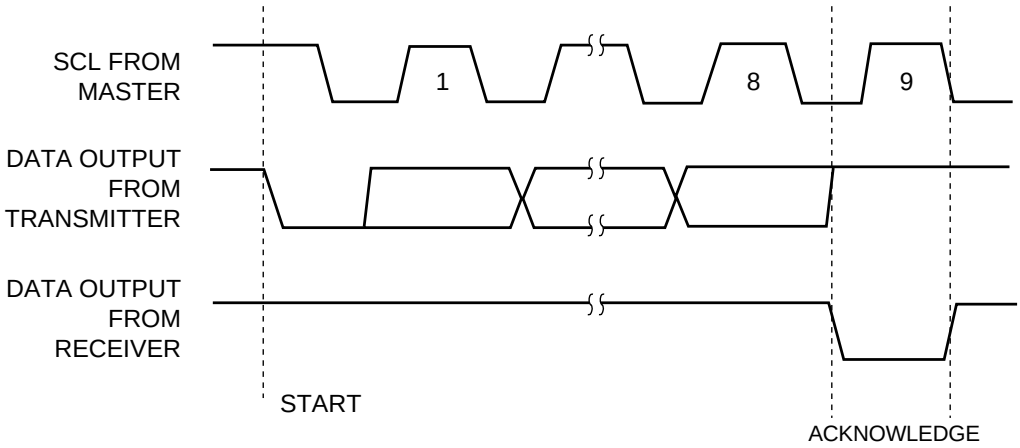
Acknowledge Response from Receiver (Figure 4)



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Write Cycle Timing (Continued)

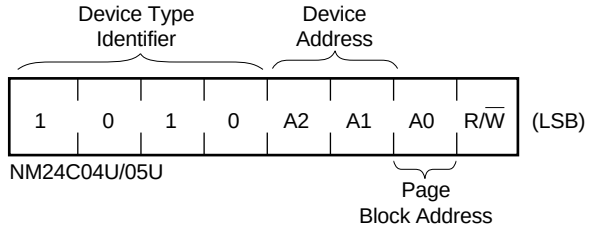
The NM24C04U/05U device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the NM24C04U/05U will respond with an acknowledge after the receipt of each subsequent eight bit byte.

In the read mode the NM24C04U/05U slave will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are those of the device type identifier (*see Figure 5)*. This is fixed as 1010 for all EEPROM devices.

Slave Addresses (Figure 5)



DS800008-14

Refer to the following table for Slave Addresses string details:

Device	A0	A1	A2	Page Blocks	Page Block Addresses
NM24C04U/05U	P	A	A	2	00 01

A: Refers to a hardware configured Device Address pin
P: Refers to an internal PAGE BLOCK memory segment.

All IIC EEPROMs use an internal protocol that defines a PAGE BLOCK size of 2K bits (for Word addressess 0000 through 1111). Therefore, address bits A0, A1, or A2 (if designated 'P') are used to access a PAGE BLOCK in conjunction with the Word address used to access any individual data byte (Word).

The last bit of the slave address defines whether a write or read condition is requested by the master. A '1' indicates that a read operation is to be executed, and a '0' initiates the write mode.

A simple review: After the NM24C04U/05U recognizes the start condition, the devices interfaced to the IIC bus wait for a slave address to be transmitted over the SDA line. If the transmitted slave address matches an address of one of the devices, the designated slave pulls the line LOW with an acknowledge signal and awaits further transmissions.

Write Operations

BYTE WRITE

For a write operation a second address field is required which is a word address that is comprised of eight bits and provides access to any one of the 256 bytes in the selected page of memory. Upon receipt of the byte address the NM24C04U/05U responds with an acknowledge and waits for the next eight bits of data, again, responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the NM24C04U/05U begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the NM24C04U/05U inputs are disabled, and the device will not respond to any requests from the master. Refer to *Figure 6* for the address, acknowledge and data transfer sequence.

PAGE WRITE

The NM24C04U/05U is capable of a sixteen byte page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data byte is transferred, the master can transmit up to fifteen more bytes. After the receipt of each byte, the NM24C04U/05U will respond with an acknowledge.

After the receipt of each byte, the internal address counter increments to the next address and the next SDA data is accepted. If the master should transmit more than sixteen bytes prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to *Figure 7* for the address, acknowledge, and data transfer sequence.

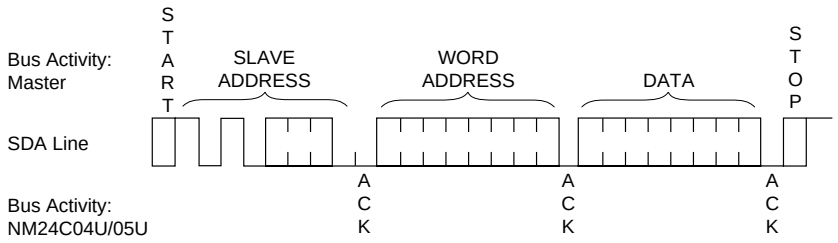
Acknowledge Polling

Once the stop condition is issued to indicate the end of the host's write operation the NM24C04U/05U initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the NM24C04U/05U is still busy with the write operation no ACK will be returned. If the NM24C04U/05U has completed the write operation an ACK will be returned and the host can then proceed with the next read or write operation.

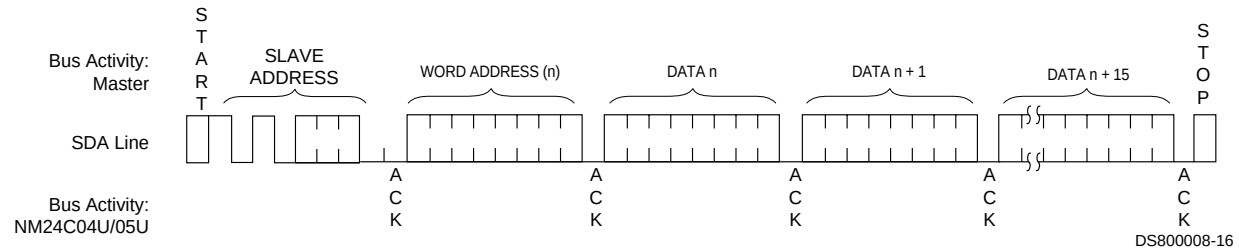
Write Protection (NM24C05U Only)

Programming of the upper half of the memory will not take place if the WP pin of the NM24C05U is connected to V_{CC}. The NM24C05U will accept slave and byte addresses; but if the memory accessed is write protected by the WP pin, the NM24C05U will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the stop condition is asserted.

Byte Write (Figure 6)



Page Write (Figure 7)



Read Operations

Read operations are initiated in the same manner as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to a one. There are three basic read operations: current address read, random read, and sequential read.

Current Address Read

Internally the NM24C04U/05U contains an address counter that maintains the address of the last byte accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ set to one, the NM24C04U/05U issues an acknowledge and transmits the eight bit byte. The master will not acknowledge the transfer but does generate a stop condition, and therefore the NM24C04U/05U discontinues transmission. Refer to *Figure* 8 for the sequence of address, acknowledge and data transfer.

Random Read

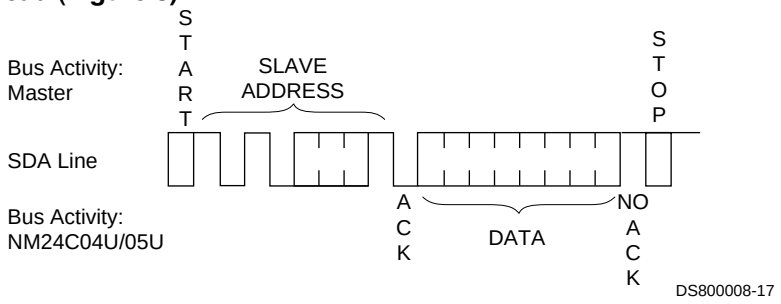
Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, slave address and then the byte address it is to read. After the byte address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the NM24C04U/05U and then by the eight bit data. The master will not acknowledge the transfer but does generate the stop condition, and therefore the NM24C04U/05U discontinues transmission. Refer to *Figure 9* for the address, acknowledge and data transfer sequence.

Sequential Read

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted in the same manner as the other read modes; however, the master now responds with an acknowledge, indicating it requires additional data. The NM24C04U/05U continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge or by generating a stop condition.

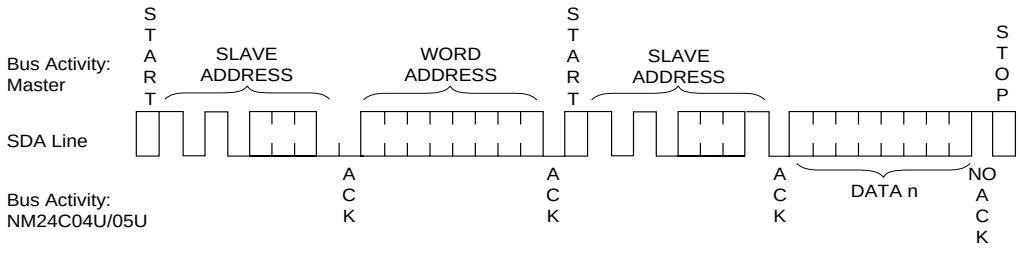
The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. After the entire memory has been read, the counter "rolls over" and the NM24C04U/05U continues to output data for each acknowledge received. Refer to *Figure 10* for the address, acknowledge, and data transfer sequence.

Current Address Read (Figure 8)



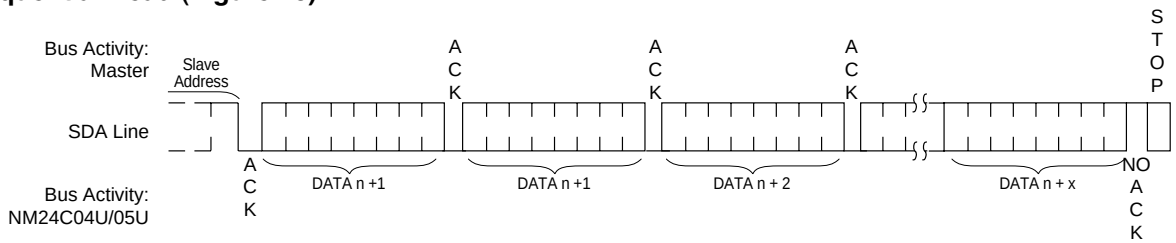
DS800008-17

Random Read (Figure 9)



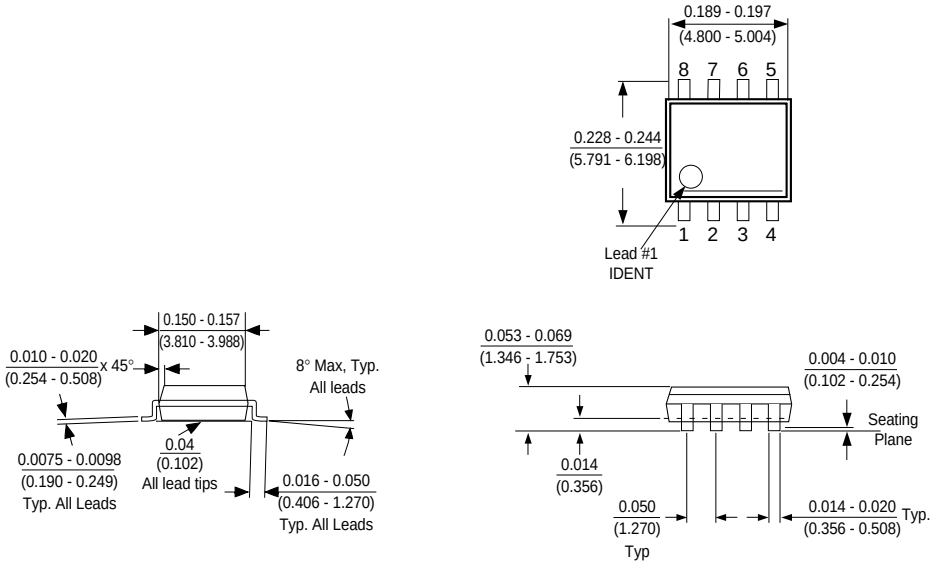
DS800008-18

Sequential Read (Figure 10)

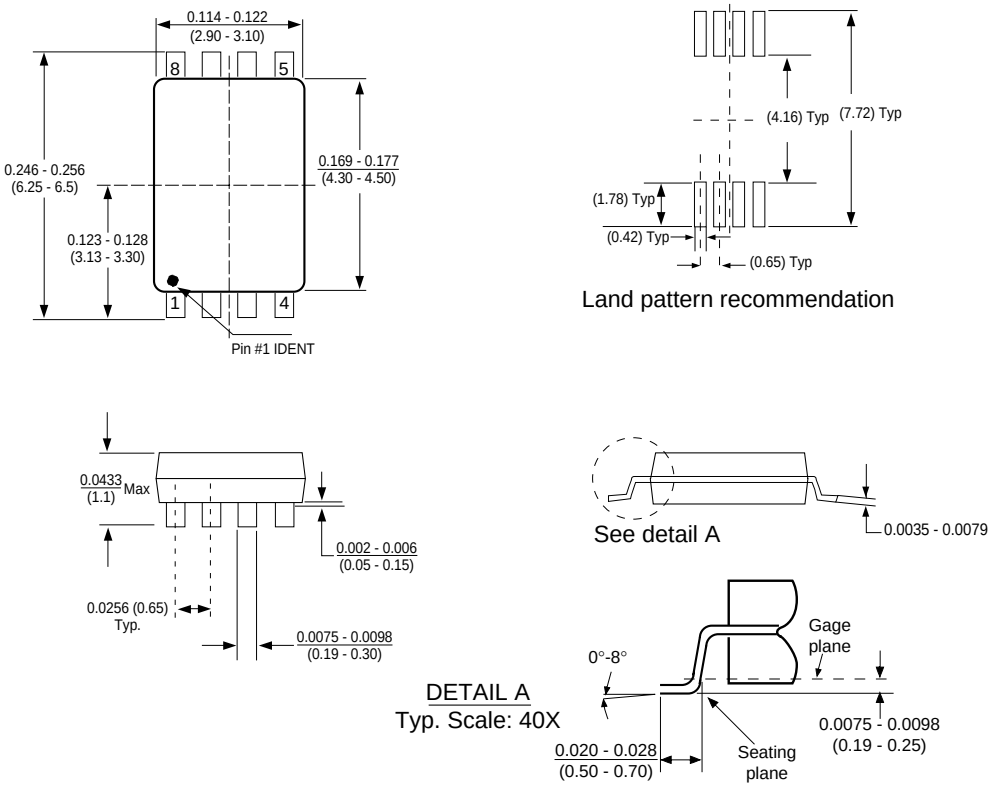


DS800008-19

Physical Dimensions inches (millimeters) unless otherwise noted



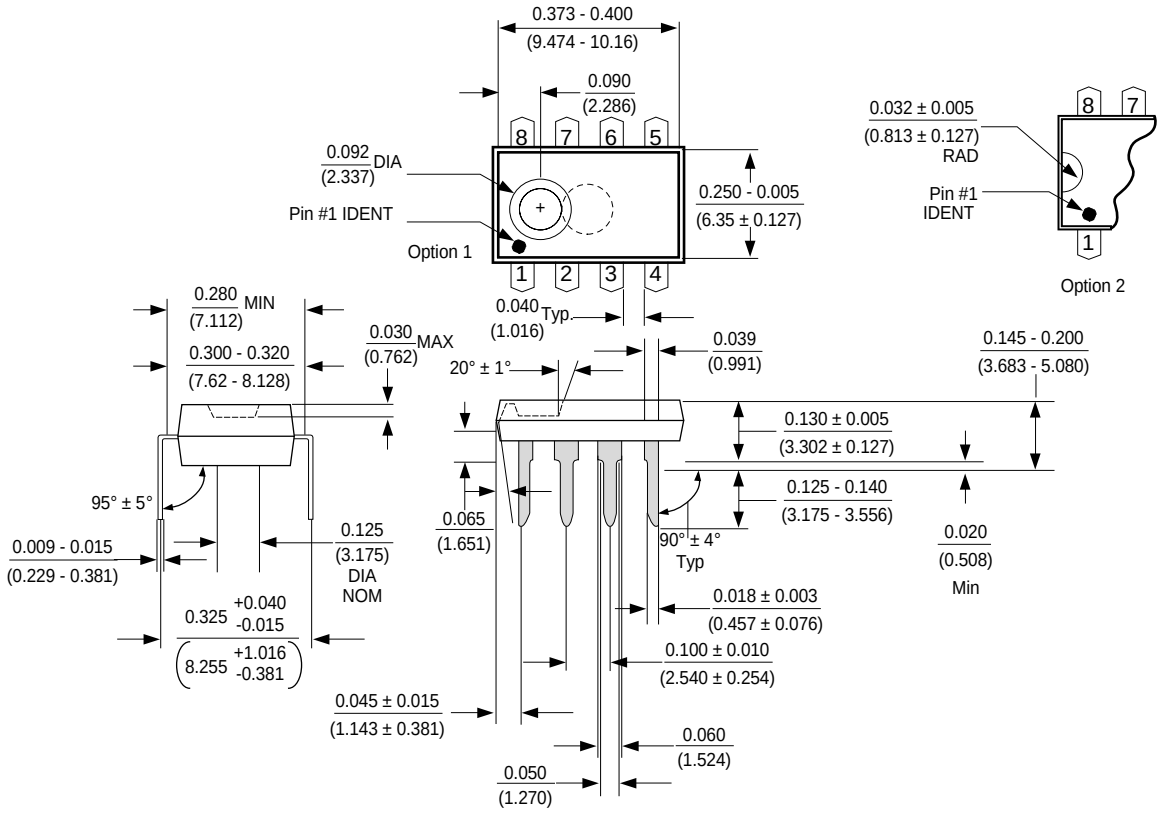
8-Pin Molded Small Outline Package (M8)
Package Number M08A



Notes: Unless otherwise specified
1. Reference JEDEC registration MO153. Variation AA. Dated 7/93

8-Pin Molded Thin Shrink Small Outline Package
Package Number MTC08

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Package Number N08E

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD
SEMICONDUCTOR™

February 2000

NM24C08/09 – 8K-Bit Standard 2-Wire Bus Interface Serial EEPROM

General Description

The NM24C08/09 devices are 8192 bits of CMOS non-volatile electrically erasable memory. These devices conform to all specifications in the Standard IIC 2-wire protocol and are designed to minimize device pin count, and simplify PC board layout requirements.

The upper half (upper 4Kbit) of the memory of the NM24C09 can be write protected by connecting the WP pin to V_{CC}. This section of memory then becomes unalterable unless WP is switched to V_{SS}.

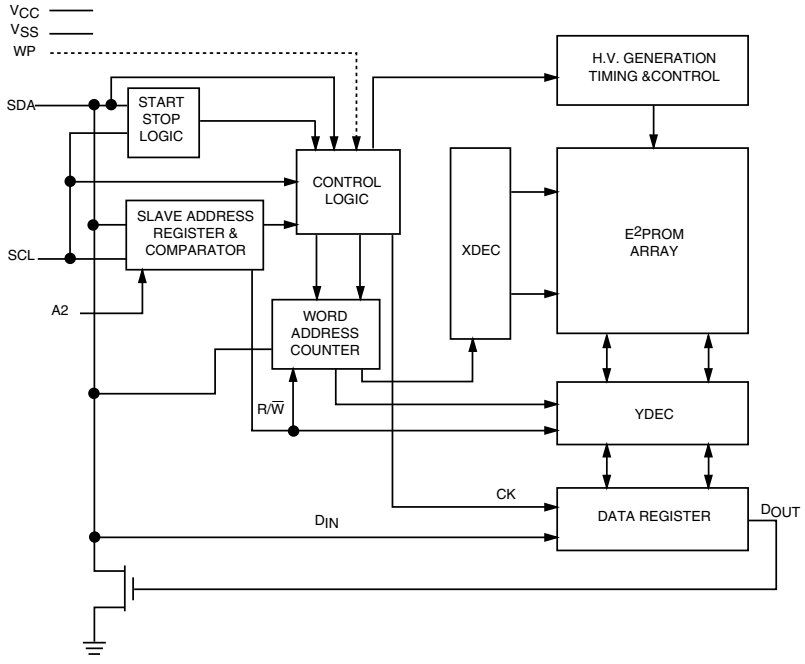
This communications protocol uses CLOCK (SCL) and DATA I/O (SDA) lines to synchronously clock data between the master (for example a microprocessor) and the slave EEPROM device(s). The Standard IIC protocol allows for a maximum of 16K of EEPROM memory which is supported by the Fairchild family in 2K, 4K, 8K, and 16K devices, allowing the user to configure the memory as the application requires with any combination of EEPROMs. In order to implement higher EEPROM memory densities on the IIC bus, the Extended IIC protocol must be used. (Refer to the NM24C32 or NM24C65 datasheets for more information.)

Fairchild EEPROMs are designed and tested for applications requiring high endurance, high reliability and low power consumption.

Features

- Extended operating voltage 2.7V – 5.5V
- 400 KHz clock frequency (F) at 2.7V - 5.5V
- 200µA active current typical
  - 10µA standby current typical
  - 1µA standby current typical (L)
  - 0.1µA standby current typical (LZ)
- IIC compatible interface
  - – Provides bi-directional data transfer protocol
- Schmitt trigger inputs
- Sixteen byte page write mode
  - – Minimizes total write time per byte
- Self timed write cycle
  - Typical write cycle time of 6ms
- Hardware Write Protect for upper half (NM24C09 only)
- Endurance: 1,000,000 data changes
- Data retention greater than 40 years
- Packages available: 8-pin DIP, 8-pin SO, and 8-pin TSSOP
- Available in three temperature ranges
  - - Commercial: 0° to +70°C
  - - Extended (E): -40° to +85C
  - - Automotive (V): -40° to +125°C

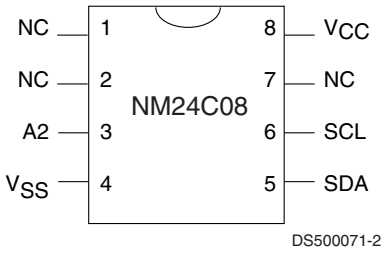
Block Diagram



DS500071-1

Connection Diagrams

Dual-in-Line Package (N), SO Package (M8) and TSSOP Package (MT8)



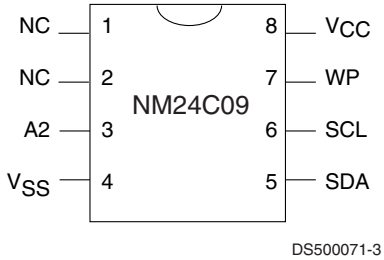
DS500071-2

See Package Number N08E, M08A and MTC08

Pin Names

A2	Device Address Input
V_{SS}	Ground
SDA	Serial Data I/O
SCL	Serial Clock Input
NC	No Connection
V_{CC}	Power Supply

Dual-in-Line Package (N), SO Package (M8) and TSSOP Package (MT8)



DS500071-3

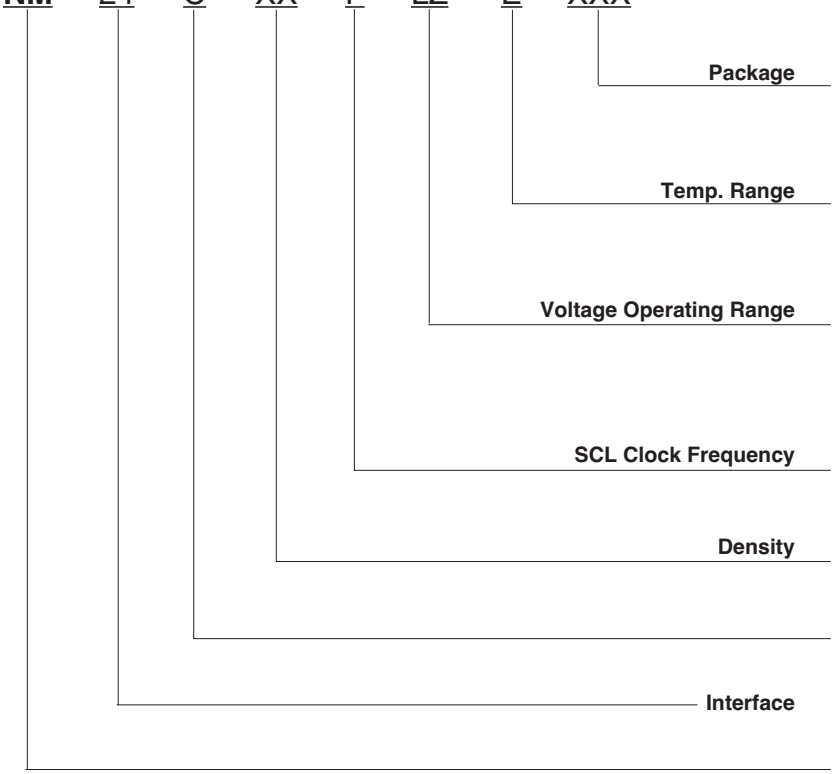
See Package Number N08E, M08A and MTC08

Pin Names

A2	Device Address Input
V_{SS}	Ground
SDA	Serial Data I/O
SCL	Serial Clock input
WP	Write Protect
V_{CC}	Power Supply
NC	No Connection

NOTE: Pins designated as "NC" are typically unbonded pins. However some of them are bonded for special testing purposes. Hence if a signal is applied to these pins, care should be taken that the voltage applied on these pins does not exceed the V_{CC} applied to the device. This will ensure proper operation.

Ordering Information



	Letter	Description
Package	N	8-pin DIP
	M8	8-pin SOIC
	MT8	8-pin TSSOP
Temp. Range	None	0 to 70°C
	V	-40 to +125°C
	E	-40 to +85°C
Voltage Operating Range	Blank	4.5V to 5.5V
	L	2.7V to 5.5V
	LZ	2.7V to 5.5V and <1µA Standby Current
SCL Clock Frequency	Blank	100KHz
	F	400KHz
Density	08	8K
	09	8K with Write Protect
	C	CMOS Technology
Interface	24	IIC
	NM	**Fairchild Non-Volatile Memory**

Product Specifications

Absolute Maximum Ratings

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltages with Respect to Ground	6.5V to –0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min.

Operating Conditions

Ambient Operating Temperature	
NM24C08/09	0°C to +70°C
NM24C08E/09E	-40°C to +85°C
NM24C08V/09V	-40°C to +125°C
Positive Power Supply	
NM24C08/09	4.5V to 5.5V
NM24C08L/09L	2.7V to 5.5V
NM24C08LZ/09LZ	2.7V to 5.5V

DC Electrical Characteristics (2.7V to 5.5V)

Symbol	Parameter	Test Conditions		Limits			Units
				Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 400 KHz f_{SCL} = 100 KHz			0.2	1.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}	V_{CC} = 2.7V - 5.5V V_{CC} = 2.7V - 5.5V (L) V_{CC} = 2.7V - 4.5V (LZ)		10 1 0.1	50 10 1	µA µA µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}			0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}			0.1	1	µA
V_{IL}	Input Low Voltage			–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA				0.4	V

Capacitance T_A = +25°C, f = 100/400 KHz, V_{CC} = 5V (Note 2)

Symbol	Test	Conditions	Max	Units
$C_{I/O}$	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN}	Input Capacitance (A0, A1, A2, SCL)	V_{IN} = 0V	6	pF

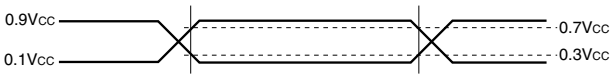
Note 1: Typical values are T_A = 25°C and nominal supply voltage of 5V for 4.5V-5.5V operation and at 3V for 2.7V-4.5V operation.

Note 2: This parameter is periodically sampled and not 100% tested.

AC Test Conditions

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10 ns
Input & Output Timing Levels	V_{CC} x 0.3 to V_{CC} x 0.7
Output Load	1 TTL Gate and C_L = 100 pF

AC Testing Input/Output Waveforms



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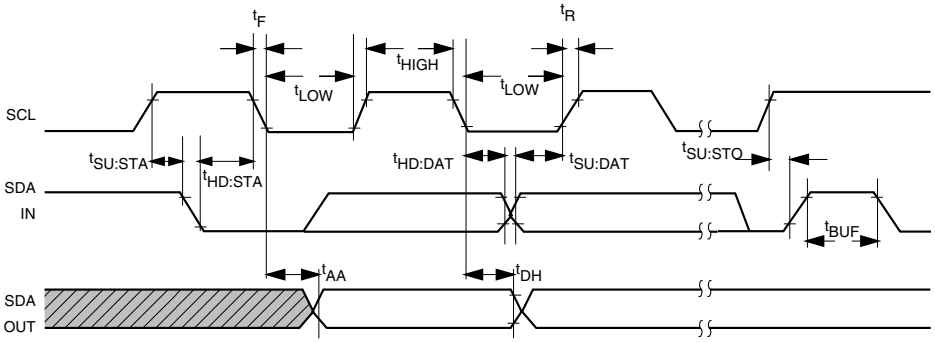
Read and Write Cycle Limits (Standard and Low V_{CC} Range 2.7V - 5.5V)

Symbol	Parameter	100 KHz		400 KHz		Units
		Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		100		400	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs (Minimum V_{IN} Pulse width)		100		50	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	0.1	0.9	µs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		1.3		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		0.6		µs
t_{LOW}	Clock Low Period	4.7		1.5		µs
t_{HIGH}	Clock High Period	4.0		0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		µs
$t_{HD:DAT}$	Data in Hold Time	20		20		ns
$t_{SU:DAT}$	Data in Setup Time	250		100		ns
t_R	SDA and SCL Rise Time		1		0.3	µs
t_F	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		0.6		µs
t_{DH}	Data Out Hold Time	300		50		ns
t_{WR} (Note 3)	Write Cycle Time - NM24C08/09 - NM24C08/09L, NM24C08/09LZ		10 15		10 15	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the NM24C08/09 bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address. Refer "Write Cycle Timing" diagram.

Bus Timing



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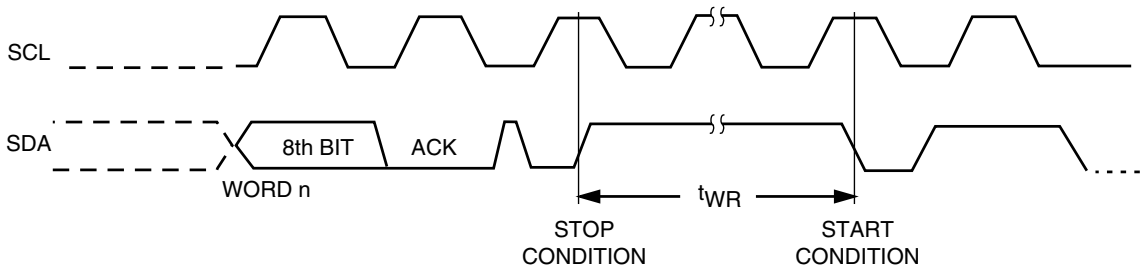
Write Cycle Timing



Note: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle.

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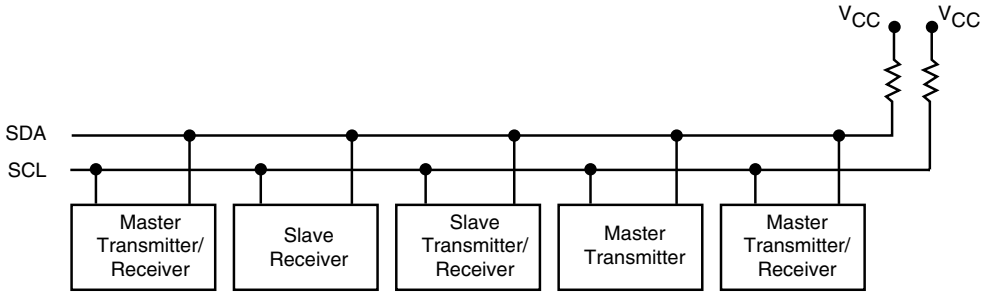
Typical System Configuration



Note: Due to open drain configuration of SDA and SCL, a bus-level pull-up resistor is called for, (typical value = 4.7kΩ)

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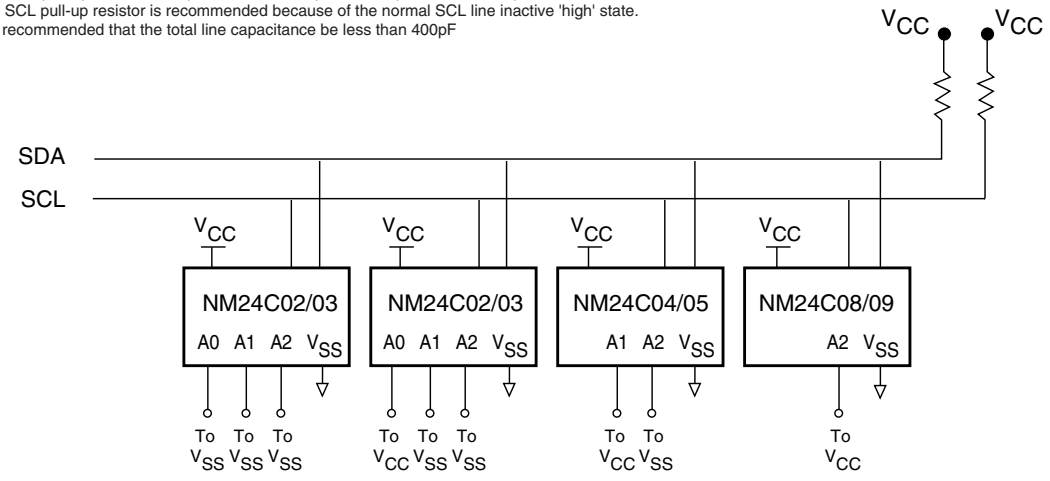
Example of 16K of Memory on 2-Wire Bus

Note: The SDA pull-up resistor is required due to the open-drain/open collector output of IIC bus devices.
The SCL pull-up resistor is recommended because of the normal SCL line inactive 'high' state.
It is recommended that the total line capacitance be less than 400pF



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Device	Address Pins Present			Memory Size	# of Page Blocks
	A0	A1	A2		
NM24C02/03	Yes	Yes	Yes	2048 Bits	1
NM24C04/05	No	Yes	Yes	4096 Bits	2
NM24C08/09	No	No	Yes	8192 Bits	4
NM24C16/17	No	No	No	16,384 Bits	8

Background Information (IIC Bus)

IIC bus allows synchronous bi-directional communication between a TRANSMITTER and a RECEIVER using a Clock signal (SCL) and a Data signal (SDA). Additionally there are up to three Address signals (A2, A1 and A0) which collectively serve as "chip select signal" to a device (example EEPROM) on the IIC bus.

All communication on the IIC bus must be started with a valid START condition (by a MASTER), followed by transmittal (by the MASTER) of byte(s) of information (Address/Data). For every byte of information received, the addressed RECEIVER provides a valid ACKNOWLEDGE pulse to further continue the communication unless the RECEIVER intends to discontinue the communication. Depending on the direction of transfer (Write or Read), the RECEIVER can be a SLAVE or the MASTER. A typical IIC communication concludes with a STOP condition (by the MASTER).

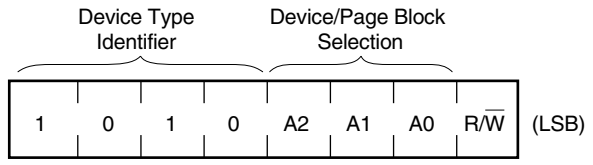
Addressing an EEPROM memory location involves sending a command string with the following information:

[DEVICE TYPE]—[DEVICE/PAGE BLOCK SELECTION]—[R/W BIT]—{acknowledge pulse}—[ARRAY ADDRESS]

Slave Address

Slave Address is an 8-bit information consisting of a Device type field (4bits), Device/Page block selection field (3bits) and Read/Write bit (1bit).

Slave Address Format



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Device Type

IIC bus is designed to support a variety of devices such as RAMs, EPROMs etc., along with EEPROMS. Hence to properly identify various devices on the IIC bus, a 4-bit “Device Type” identifier string is used. For EEPROMS, this 4-bit string is 1-0-1-0. Every IIC device on the bus internally compares this 4-bit string to its own “Device Type” string to ensure proper device selection.

Device/Page Block Selection

When multiple devices of the same type (e.g. multiple EEPROMS) are present on the IIC bus, then the A2, A1 and A0 address information bits are also used as part of the Slave Address. Every IIC device on the bus internally compares this 3-bit string to its own physical configuration (A2, A1 and A0 pins) to ensure proper device selection. This comparison is in addition to the “Device Type” comparison. In addition to selecting an EEPROM, these 3 bits are also used to select a “page block” within the selected EEPROM. Each page block is 2Kbit (256Bytes) in size. Depending on the density, an EEPROM can contain from a minimum of 1 to a maximum of 8 page blocks (in multiples of 2) and selection of a page block within a device is by using A2, A1 and A0 bits.

Read/Write Bit

Last bit of the Slave Address indicates if the intended access is Read or Write. If the bit is "1," then the access is Read, whereas if the bit is "0," then the access is Write.

Acknowledge

Acknowledge is an active LOW pulse on the SDA line driven by an addressed receiver to the addressing transmitter to indicate receipt of 8-bits of data. The receiver provides an ACK pulse for every 8-bits of data received. This handshake mechanism is done as follows: After transmitting 8-bits of data, the transmitter releases the SDA line and waits for the ACK pulse. The addressed receiver, if present, drives the ACK pulse on the SDA line during the 9th clock and releases the SDA line back (to the transmitter). Refer *Figure 3*.

Array Address

Array address is an 8-bit information containing the address of a memory location to be selected within a page block of the device.

16K bit Addressing Limitation:

Standard IIC specification limits the maximum size of EEPROM memory on the bus to 16K bits. This limitation is due to the addressing protocol implemented which consists of the 8-bit Slave Address and an additional 8-bit field called Array Address. This Array Address selects 1 out of 256 locations (2^8=256). Since the data format of IIC specification is 8-bit wide, a total of 256 x 8 = 2048 = 2K bit now becomes addressable by this 8-bit Array Address. This 2K bit is typically referred as a “Page Block”. Combining this 8-bit Array Address with the 3-bit Device/Page address (part of Slave Address) allows a maximum of 8 pages (2^3=8) of memory that can be addressed. Since each page is 2K bit in size, 8 x 2K bit = 16K bit is the maximum size of memory that is addressable on the Standard IIC bus. This 16Kb of memory can be in the form of a single 16Kb EEPROM device or multiple EEPROMs of varying density (in 2Kb multiples) to a maximum total of 16Kb. To address the needs of systems that require more than 16Kb on the IIC bus, a different specification called “Extended IIC Specification” is used. Please refer to NM24C32xx Datasheet for more information on Extended IIC Specification.

DEFINITIONS	
WORD	8 bits (byte) of data
PAGE	16 sequential byte locations starting at a 16-byte address boundary, that may be programmed during a "page write" programming cycle
PAGE BLOCK	2048 (2K) bits organized into 16 pages of addressable memory. (8 bits) x (16 bytes) x (16 pages) = 2048 bits
MASTER	Any IIC device CONTROLLING the transfer of data (such as a microprocessor)
SLAVE	Device being controlled (EEPROMs are always considered Slaves)
TRANSMITTER	Device currently SENDING data on the bus (may be either a Master or Slave).
RECEIVER	Device currently RECEIVING data on the bus (Master or Slave)

Pin Descriptions

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bi-directional pin used to transfer data into and out of the device. It is an open drain output and may be wire–ORed with any number of open drain or open collector outputs.

Write Protect (WP) (NM24C09 Only)

If tied to V_{CC}, PROGRAM operations onto the upper half (upper 4Kbit) of the memory will not be executed. READ operations are possible. If tied to V_{SS}, normal operation is enabled, READ/WRITE over the entire memory is possible.

This feature allows the user to assign the upper half of the memory as ROM which can be protected against accidental programming. When write is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

This pin has an internal pull-down circuit. However, on systems where write protection is not required it is recommended that this pin is tied to V_{SS}.

Device Selection Inputs A2, A1 and A0 (as appropriate)

These inputs collectively serve as "chip select" signal to an EEPROM when multiple EEPROMs are present on the same IIC bus. Hence these inputs, if present, should be connected to V_{CC} or V_{SS} in a unique manner to allow proper selection of an EEPROM amongst multiple EEPROMs. During a typical addressing sequence, every EEPROM on the IIC bus compares the configuration of these inputs to the respective 3 bit "Device/Page block selection" information (part of slave address) to determine a valid selection. For e.g. if the 3 bit "Device/Page block selection" is 1-0-1, then the EEPROM whose "Device Selection inputs" (A2, A1 and A0) are connected to V_{CC}-V_{SS}-V_{CC} respectively, is selected.

Depending on the density, only appropriate number of "Device Selection inputs" are provided on an EEPROM. For every "Device selection input" that is not present on the device, the corresponding bit in the "Device/Page block selection" field is used to select a "Page Block" within the device instead of the device itself. Following table illustrates the above:

EEPROM Density	Number of Page Blocks	Device Selection Inputs Provided			Address Bits Selecting Page Block
2k bit	1	A0	A1	A2	None
4k bit	2	—	A1	A2	A0
8k bit	4	—	—	A2	A0 and A1
16k bit	8	—	—	—	A0, A1 and A2

Note that even when just one EEPROM present on the IIC bus, these pins should be tied to V_{CC} or V_{SS} to ensure proper termination.

Device Operation

The NM24C08/09 supports a bi-directional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the NM24C08/09 will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to *Figure 1* and *Figure 2* on next page.

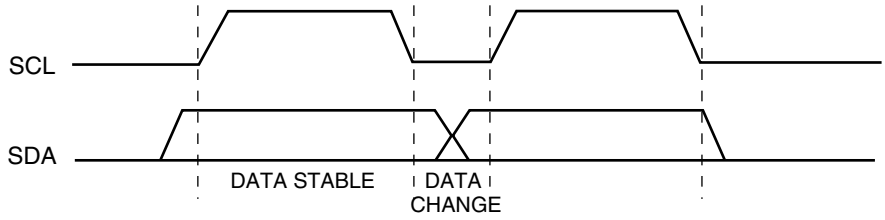
Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The NM24C08/09 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Stop Condition

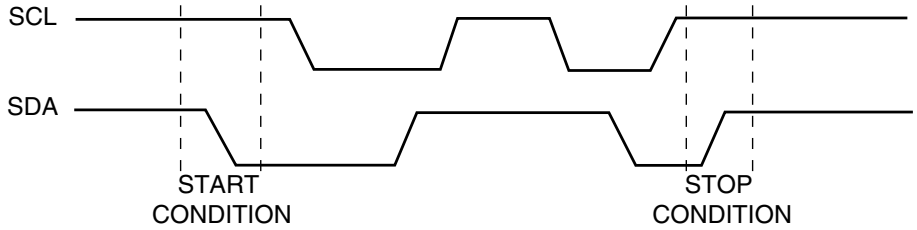
All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the NM24C08/09 to place the device in the standby power mode, except when a Write operation is being executed, in which case a second stop condition is required after t_{WR} period, to place the device in standby mode.

Data Validity (Figure 1)



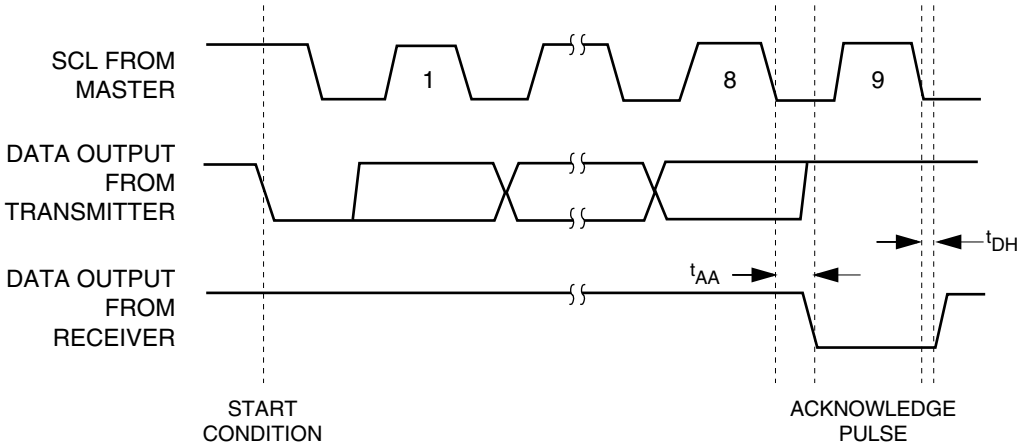
DS500071-10

Start and Stop Definition (Figure 2)



DS500071-11

Acknowledge Response from Receiver (Figure 3)



DS500071-12

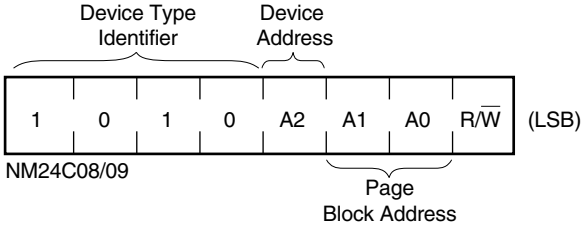
Acknowledge

The NM24C08/09 device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the NM24C08/09 will respond with an acknowledge after the receipt of each subsequent eight bit byte.

In the read mode the NM24C08/09 slave will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected, NM24C08/09 will continue to transmit data. If an acknowledge is not detected,NM24C08/09 will terminate further data transmissions and await the stop condition to return to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are those of the device type identifier. This is fixed as 1010 for all EEPROM devices.



Refer the following table for Slave Addresses string details:

Device	A0	A1	A2	Page Blocks	Page Block Addresses
NM24C08/09	P	P	A	4	00, 01, 10, 11

A: Refers to a hardware configured Device Address pin.

P: Refers to an internal PAGE BLOCK.

All IIC EEPROMs use an internal protocol that defines a PAGE BLOCK size of 2K bits (for Word addresses 0x00 through 0xFF). Therefore, address bits A0, A1, or A2 (if designated 'P') are used to access a PAGE BLOCK in conjunction with the Word address used to access any individual data byte.

The last bit of the slave address defines whether a write or read condition is requested by the master. A '1' indicates that a read operation is to be executed, and a '0' initiates the write mode.

A simple review: After the NM24C08/09 recognizes the start condition, the devices interfaced to the IIC bus wait for a slave address to be transmitted over the SDA line. If the transmitted slave address matches an address of one of the devices, the designated slave pulls the line LOW with an acknowledge signal and awaits further transmissions.

Write Operations

BYTE WRITE

For a write operation a second address field is required which is a word address that is comprised of eight bits and provides access to any one of the 256 bytes in the selected page of memory. Upon receipt of the byte address the NM24C08/09 responds with an acknowledge and waits for the next eight bits of data, again, responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the NM24C08/09 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the NM24C08/09 inputs are disabled, and the device will not respond to any requests from the master for the duration of t_{WR}. Refer to *Figure 4* for the address, acknowledge and data transfer sequence.

PAGE WRITE

To minimize write cycle time, NM24C08/09 offer Page Write feature, by which, up to a maximum of 16 contiguous bytes locations can be programmed all at once (instead of 16 individual byte writes). To facilitate this feature, the memory array is organized in terms of "Pages." A Page consists of 16 contiguous byte locations starting at every 16-Byte address boundary (for example, starting at array address 0x00, 0x10, 0x20 etc.). Page Write operation limits access to byte locations within a page. In other words a single Page Write operation will not cross over to locations on another page but will "roll over" to the beginning of the page whenever end of Page is reached and additional locations are a continued to be accessed. A Page Write operation can be initiated to begin at any location within a page (starting address of the Page Write operation need not be the starting address of a Page).

Page Write is initiated in the same manner as the Byte Write operation; but instead of terminating the cycle after transmitting the first data byte, the master can further transmit up to 15 more bytes. After the receipt of each byte, NM24C08/09 will respond with an acknowledge pulse, increment the internal address counter to the next address and is ready to accept the next data. If the master should transmit more than sixteen bytes prior to generating the STOP condition, the address counter will "roll over" and previously written data will be overwritten. As with the Byte Write operation, all inputs are disabled until completion of the internal write cycle. Refer to *Figure 5* for the address, acknowledge and data transfer sequence.

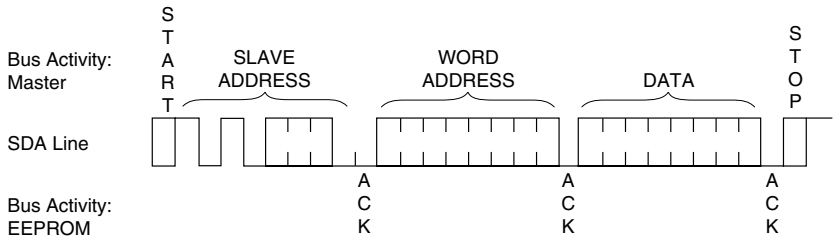
Acknowledge Polling

Once the stop condition is issued to indicate the end of the host's write operation the NM24C08/09 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the NM24C08/09 is still busy with the write operation no ACK will be returned. If the NM24C08/09 has completed the write operation an ACK will be returned and the host can then proceed with the next read or write operation.

Write Protection (NM24C09 Only)

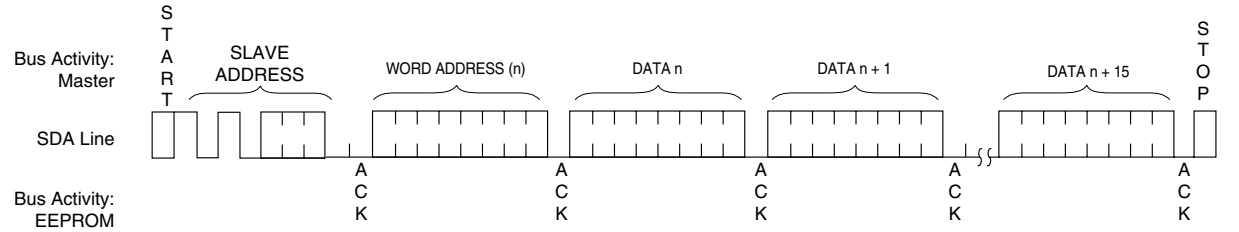
Programming of the upper half (upper 4Kbit) of the memory will not take place if the WP pin of the NM24C09 is connected to V_{CC}. The NM24C09 will respond to slave and byte addresses; but if the memory accessed is write protected by the WP pin, the NM24C09 will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the stop condition is asserted.

Byte Write (Figure 4)



DS500071-13

Page Write (Figure 5)



DS500071-14

Read Operations

Read operations are initiated in the same manner as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to a one. There are three basic read operations: current address read, random read, and sequential read.

Current Address Read

Internally the NM24C08/09 contains an address counter that maintains the address of the last byte accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ set to one, the NM24C08/09 issues an acknowledge and transmits the eight bit byte. The master will not acknowledge the transfer but does generate a stop condition, and therefore the NM24C08/09 discontinues transmission. Refer to *Figure* 6 for the sequence of address, acknowledge and data transfer.

Random Read

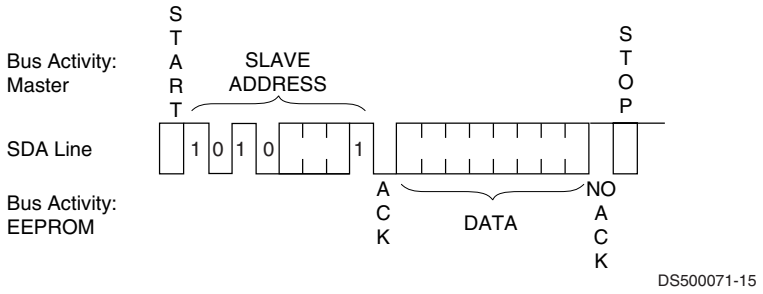
Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, slave address with the R/$\overline{W}$ bit set to zero and then the byte address it is to read. After the byte address acknowledge, the master immediately issues another start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the NM24C08/09 and then by the eight bit byte. The master will not acknowledge the transfer but does generate the stop condition, and therefore the NM24C08/09 discontinues transmission. Refer to *Figure 7* for the address, acknowledge and data transfer sequence.

Sequential Read

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted in the same manner as the other read modes; however, the master now responds with an acknowledge, indicating it requires additional data. The NM24C08/09 continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge or by generating a stop condition.

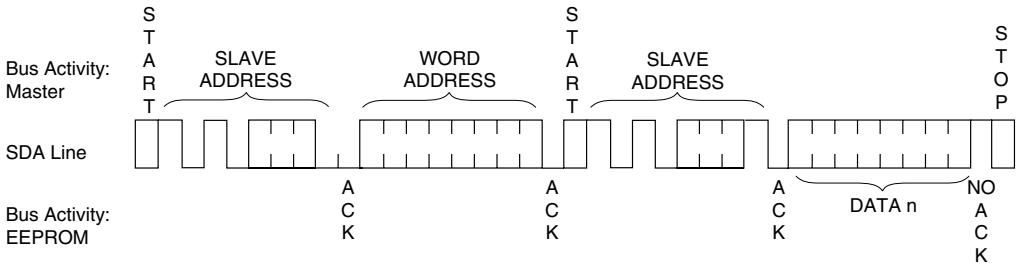
The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. After the entire memory has been read, the counter "rolls over" to the beginning of the memory. NM24C08/09 continues to output data for each acknowledge received. Refer to *Figure 8* for the address, acknowledge, and data transfer sequence.

Current Address Read (Figure 6)



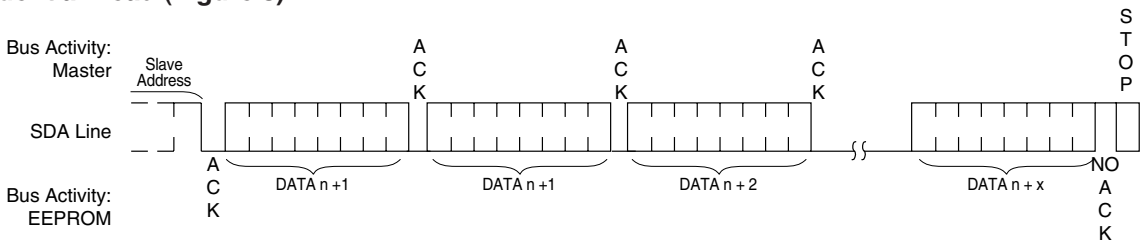
DS500071-15

Random Read (Figure 7)



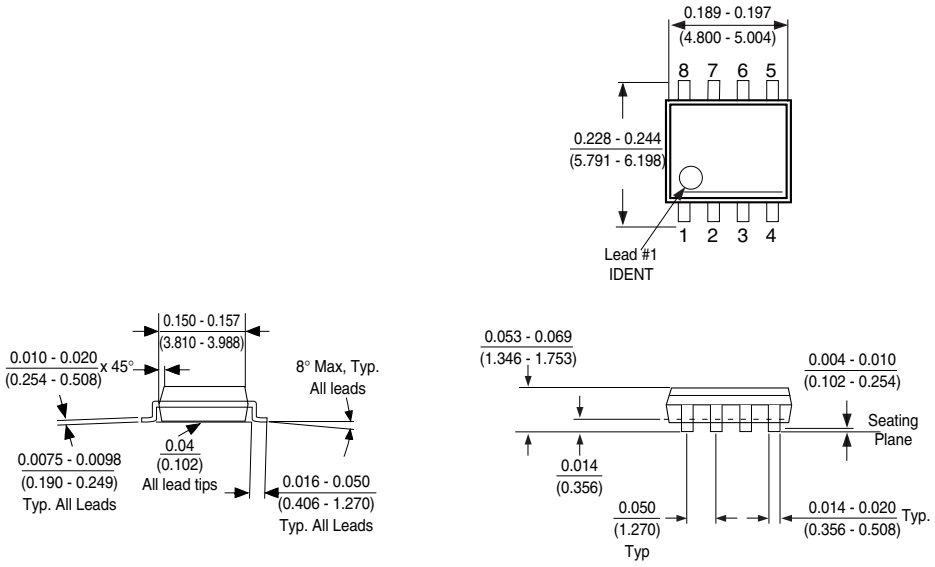
DS500071-16

Sequential Read (Figure 8)

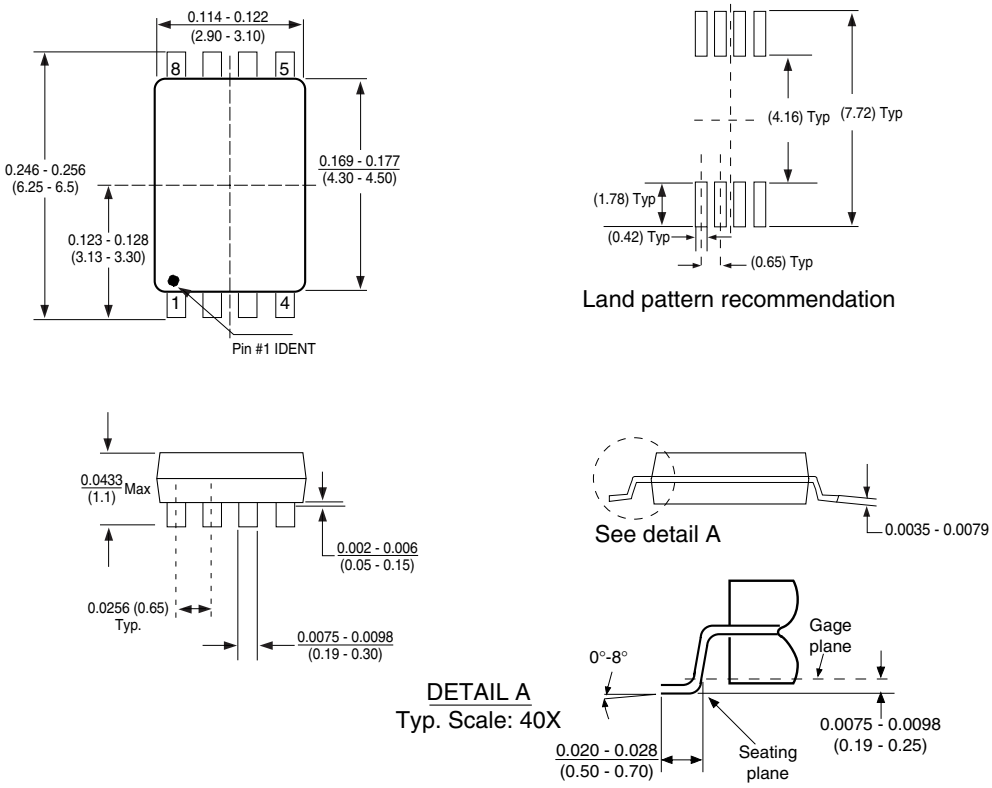


DS500071-17

Physical Dimensions inches (millimeters) unless otherwise noted



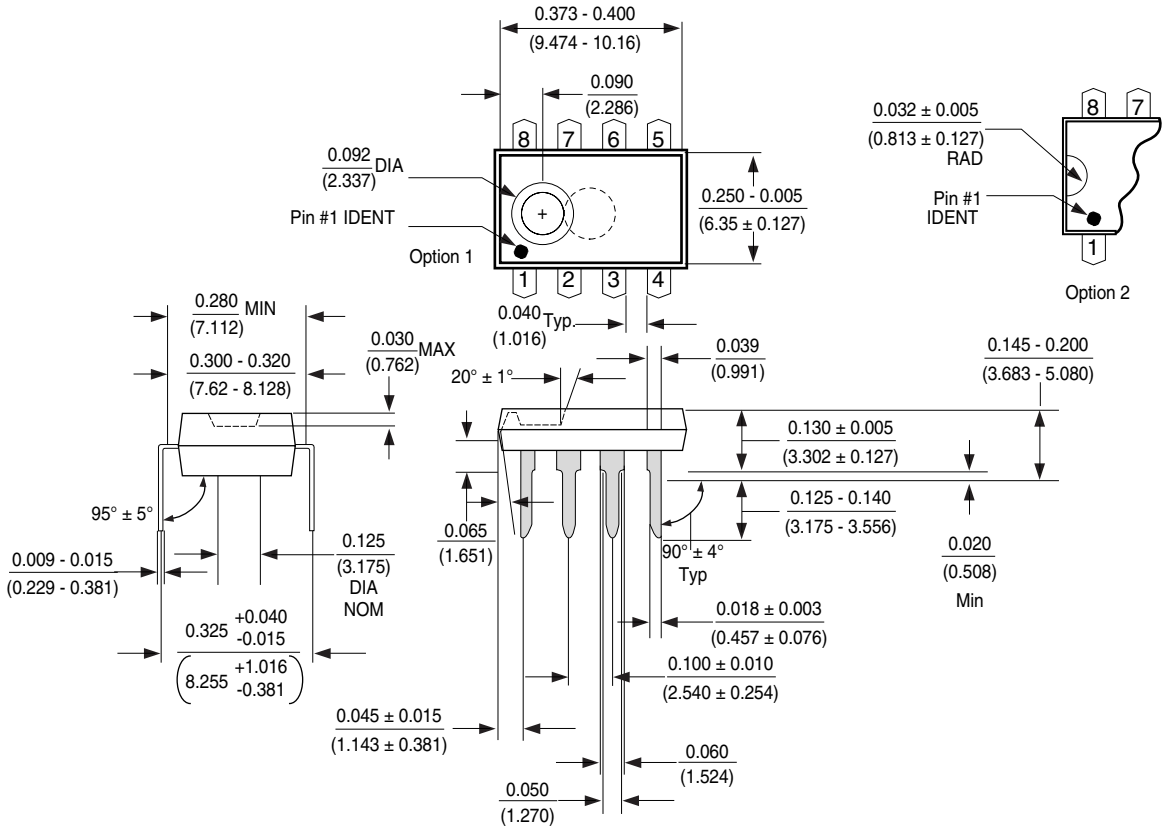
8-Pin Molded Small Outline Package (M8)
Package Number M08A



Notes: Unless otherwise specified
1. Reference JEDEC registration MO153. Variation AA. Dated 7/93

8-Pin Molded Thin Shrink Small Outline Package (MT8)
Package Number MTC08

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Package Number N08E

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

August 1999

NM24C08U/NM24C09U 8K-Bit Serial EEPROM 2-Wire Bus Interface

General Description,

The NM24C08U/09U devices are 8K (8,192) bit serial interface CMOS EEPROMs (Electrically Erasable Programmable Read-Only Memory). These devices fully conform to the **Standard** I²C™ 2-wire protocol which uses Clock (SCL) and Data I/O (SDA) pins to synchronously clock data between the "master" (for example a microprocessor) and the "slave" (the EEPROM device). In addition, the serial interface allows a minimal pin count packaging designed to simplify PC board layout requirements and offers the designer a variety of low voltage and low power options.

NM24C09U incorporates a hardware "Write Protect" feature, by which, the upper half of the memory can be disabled against programming by connecting the WP pin to V_{CC}. This section of memory then effectively becomes a ROM (Read-Only Memory) and can no longer be programmed as long as WP pin is connected to V_{CC}.

Fairchild EEPROMs are designed and tested for applications requiring high endurance, high reliability and low power consumption for a continuously reliable non-volatile solution for all markets.

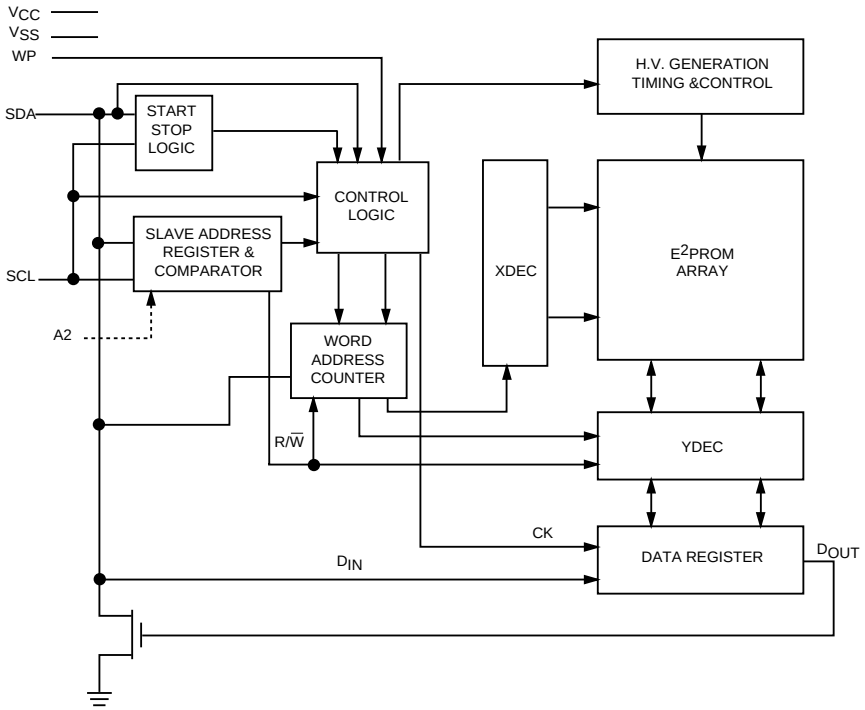
Functions

- I²C™ compatible interface
- 8,192 bits organized as 1,024 x 8
- Extended 2.7V – 5.5V operating voltage
- 100 KHz or 400 KHz operation
- Self timed programming cycle (6ms typical)
- "Programming complete" indicated by ACK polling
- NM24C09U: Memory "Upper Block" Write Protect pin

Features

- The I²C™ interface allows the smallest I/O pincount of any EEPROM interface
- 16 byte page write mode to minimize total write time per byte
- Typical 200µA active current (I_{CCA})
- Typical 1µA standby current (I_{SB}) for "L" devices and 0.1µA standby current for "LZ" devices
- Endurance: Up to 1,000,000 data changes
- Data retention greater than 40 years

Block Diagram

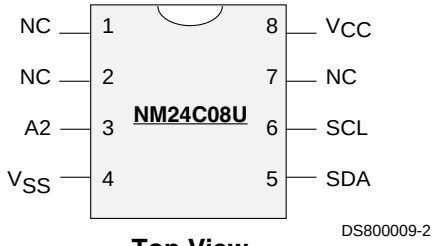


DS800009-1

I²C™ is a registered trademark of Philips Electronics N.V.

Connection Diagrams

Dual-In-Line Package (N), SO Package (M8), and TSSOP Package (MT8)



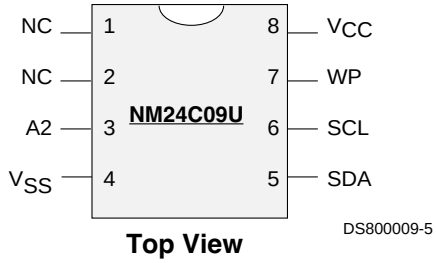
Top View

See Package Number N08E, M08A, and MTC08

Pin Names

A2	Device Address Input
V_{SS}	Ground
SDA	Serial Data I/O
SCL	Serial Clock Input
NC	No Connection
V_{CC}	Power Supply

Dual-In-Line Package (N), SO Package (M8), and TSSOP Package (MT8)



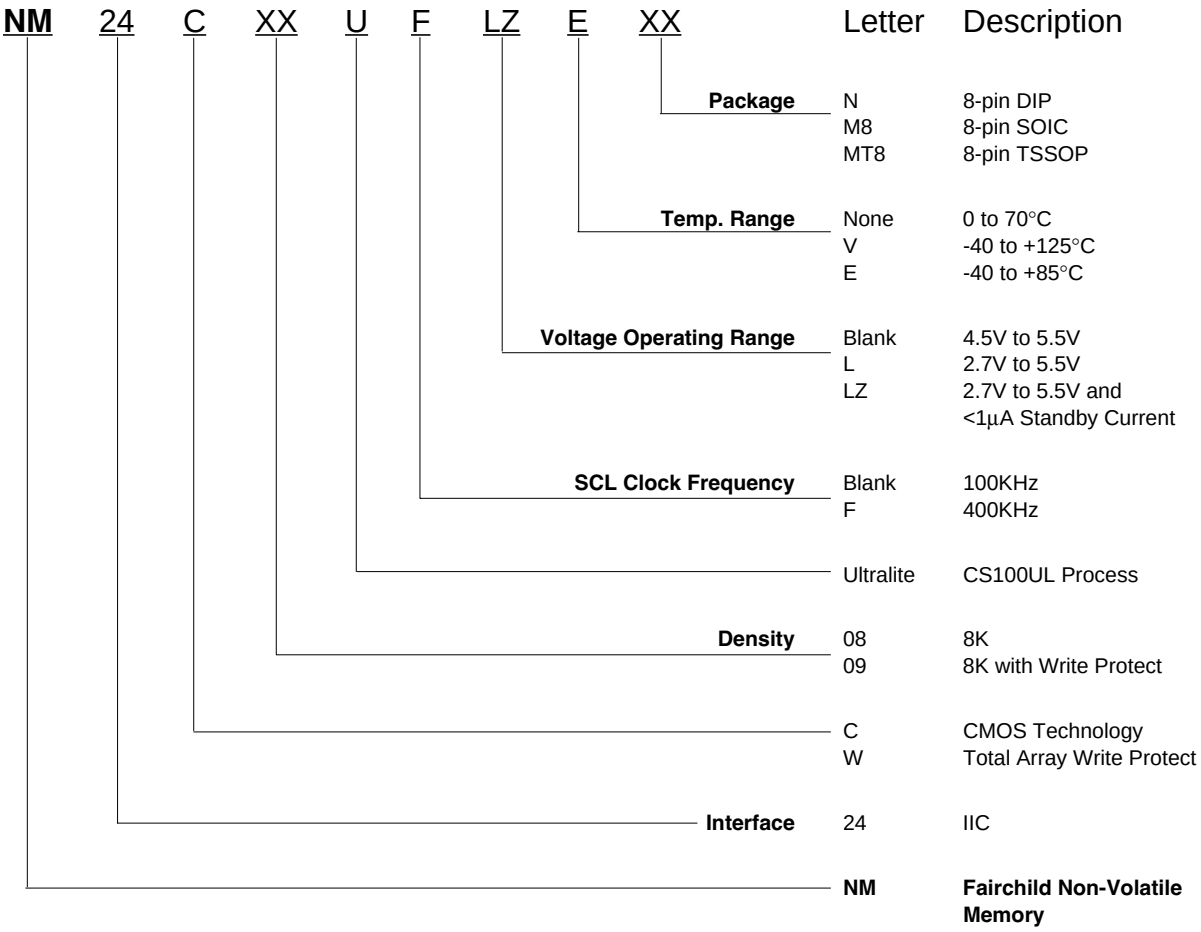
Top View

See Package Number N08E, M08A, and MTC08

Pin Names

NC	No Connection
A2	Device Address Input
V_{SS}	Ground
SDA	Serial Data I/O
SCL	Serial Clock input
WP	Write Protect
V_{CC}	Power Supply

Ordering Information



	Letter	Description
Package	N	8-pin DIP
	M8	8-pin SOIC
	MT8	8-pin TSSOP
Temp. Range	None	0 to 70°C
	V	-40 to +125°C
	E	-40 to +85°C
Voltage Operating Range	Blank	4.5V to 5.5V
	L	2.7V to 5.5V
	LZ	2.7V to 5.5V and <1µA Standby Current
SCL Clock Frequency	Blank	100KHz
	F	400KHz
	Ultralite	CS100UL Process
Density	08	8K
	09	8K with Write Protect
	C	CMOS Technology
	W	Total Array Write Protect
Interface	24	IIC
NM		**Fairchild Non-Volatile Memory**

Product Specifications

Absolute Maximum Ratings

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltages with Respect to Ground	6.5V to –0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min.

Operating Conditions

Ambient Operating Temperature	
NM24C08U/09U	0°C to +70°C
NM24C08UE/09UE	-40°C to +85°C
NM24C08UV/09UV	-40°C to +125°C
Positive Power Supply	
NM24C08U/09U	4.5V to 5.5V
NM24C08UL/09UL	2.7V to 5.5V
NM24C08ULZ/09ULZ	2.7V to 5.5V

Standard V_{CC} (4.5V to 5.5V) DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 400 KHz f_{SCL} = 100 KHz		0.2	1.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		10	50	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	1	µA
V_{IL}	Input Low Voltage		–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Low V_{CC} (2.7V to 5.5V) DC Electrical Characteristics

Symbol	Parameter	Test Conditions		Limits			Units
				Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 400 KHz f_{SCL} = 100 KHz			0.2	1.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}	V_{CC} = 2.7V - 4.5V V_{CC} = 2.7V - 4.5V V_{CC} = 4.5V - 5.5V		1 0.1 10	10 1 50	µA µA µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}			0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}			0.1	1	µA
V_{IL}	Input Low Voltage			–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA				0.4	V

Capacitance T_A = +25°C, f = 100/400 KHz, V_{CC} = 5V (Note 2)

Symbol	Test	Conditions	Max	Units
$C_{I/O}$	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN}	Input Capacitance (A0, A1, A2, SCL)	V_{IN} = 0V	6	pF

Note 1: Typical values are T_A = 25°C and nominal supply voltage (5V).

Note 2: This parameter is periodically sampled and not 100% tested.

AC Conditions of Test

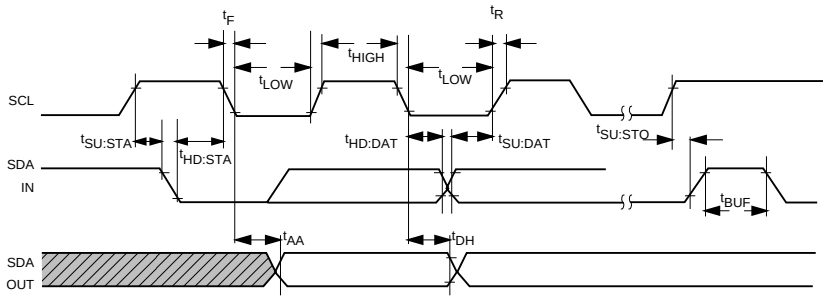
Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10 ns
Input & Output Timing Levels	V_{CC} x 0.5
Output Load	1 TTL Gate and C_L = 100 pF

Read and Write Cycle Limits (Standard and Low V_{CC} Range 2.7V - 5.5V)

Symbol	Parameter	100 KHz		400 KHz		Units
		Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		100		400	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs (Minimum V_{IN} Pulse width)		100		50	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	0.1	0.9	µs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		1.3		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		0.6		µs
t_{LOW}	Clock Low Period	4.7		1.5		µs
t_{HIGH}	Clock High Period	4.0		0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		µs
$t_{HD:DAT}$	Data in Hold Time	0		0		µs
$t_{SU:DAT}$	Data in Setup Time	250		100		ns
t_R	SDA and SCL Rise Time		1		0.3	µs
t_F	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		0.6		µs
t_{DH}	Data Out Hold Time	300		50		ns
t_{WR} (Note 3)	Write Cycle Time - NM24C08U/09U - NM24C08U/09UL, NM24C08U/09ULZ		10 15		10 15	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the NM24C08U/09U bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

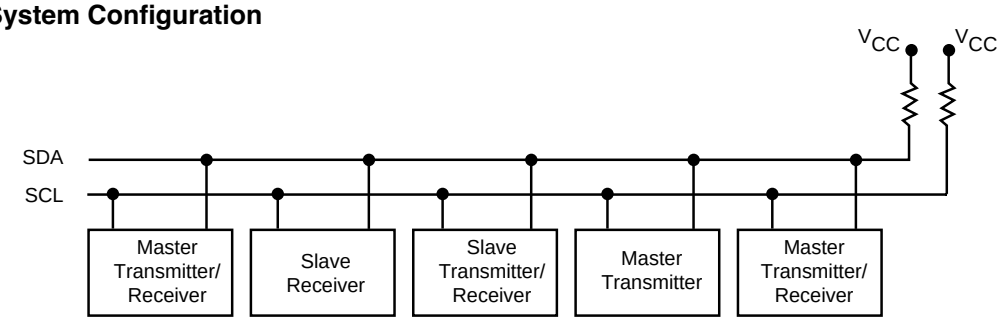
Bus Timing



DS800009-8

System Layout

Typical System Configuration

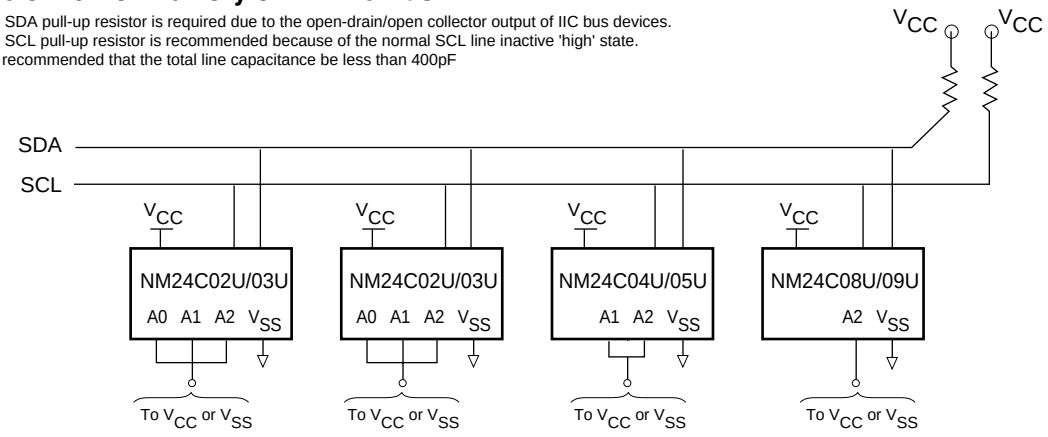


Note: Due to open drain configuration of SDA, a bus-level pull-up resistor is called for, (typical value = 4.7kΩ)

DS800009-20

Example of 16K of Memory on 2-Wire Bus

Note: The SDA pull-up resistor is required due to the open-drain/open collector output of IIC bus devices. The SCL pull-up resistor is recommended because of the normal SCL line inactive 'high' state. It is recommended that the total line capacitance be less than 400pF



DS800009-9

Device	Address Pins			Memory Size	# of Page Blocks
	A0	A1	A2		
NM24C08U/09U	No Connect	No Connect	ADR	8192 Bits	4

Device Operation Input (A2)

Device address pin A2 is connected to V_{CC} or V_{SS} to configure the EEPROM chip address. Table 1 shows the active pin.

Table 1.

Device	A0	A1	A2	Effects of Addresses
NM24C08U/09U	x	x	ADR	2^1 = 2; 2 x (4 x 2k) = 16K

Background Information (IIC Bus)

As mentioned, the IIC bus allows synchronous bidirectional communication between Transmitter/Receiver using the SCL (clock) and SDA (Data I/O) lines. All communication must be started with a valid START condition, concluded with a STOP condition and acknowledged by the Receiver with an ACKNOWLEDGE condition.

As shown below, the EEPROMs on the IIC bus may be configured in any manner required, the total memory addressed can not exceed 16K (16,384 bits). EEPROM memory address programming is controlled by 2 methods:

- Hardware configuring the A2 pin (Device Address pin) with pull-up or pull-down to V_{CC} or V_{SS}. **All unused pins must be grounded** (tied to V_{SS}).
- Software addressing the required PAGE BLOCK within the device memory array (as sent in the Slave Address string).

For devices with densities greater than 16K, a different protocol, the Extended IIC protocol, is used. Refer to NM24C32U datasheet (for example) for additional details.

Addressing an EEPROM memory location involves sending a command string with the following information: [DEVICE TYPE]–[DEVICE ADDRESS]–[PAGE BLOCK ADDRESS]–[BYTE ADDRESS]

DEFINITIONS	
BYTE	8 bits (byte) of data
PAGE	16 sequential addresses (one byte each) that may be programmed during a 'Page Write' programming cycle
PAGE BLOCK	2048 (2K) bits organized into **16 pages of addressable memory. (8 bits) x (16 bytes) x (16 pages) = 2048 bits**
MASTER	Any IIC device CONTROLLING the transfer of data (such as a microprocessor)
SLAVE	Device being controlled (EEPROMs are always considered Slaves)
TRANSMITTER	Device currently SENDING data on the bus (may be either a Master or Slave).
RECEIVER	Device currently RECEIVING data on the bus (Master or Slave)

Pin Descriptions

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire–ORed with any number of open drain or open collector outputs.

WP Write Protection (NM24C09U Only)

If tied to V_{CC}, PROGRAM operations onto the upper half of the memory will not be executed. READ operations are possible. If tied to V_{SS}, normal operation is enabled, READ/WRITE over the entire memory is possible.

This feature allows the user to assign the upper half of the memory as ROM which can be protected against accidental programming. When write is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

Device Operation

The NM24C08U/09U supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the NM24C08U/09U will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to *Figure 2* and *Figure 3* on next page.

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The NM24C08U/09U continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Stop Condition

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the NM24C08U/09U to place the device in the standby power mode.

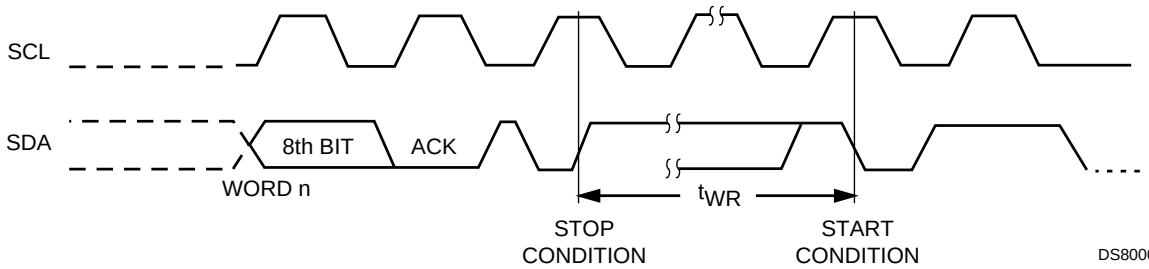
Write Cycle Timing

Acknowledge

Acknowledge is a hardware convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits.

During the ninth clock cycle the receiver will pull the SDA line to LOW to acknowledge that it received the eight bits of data. Refer to *Figure 4.*

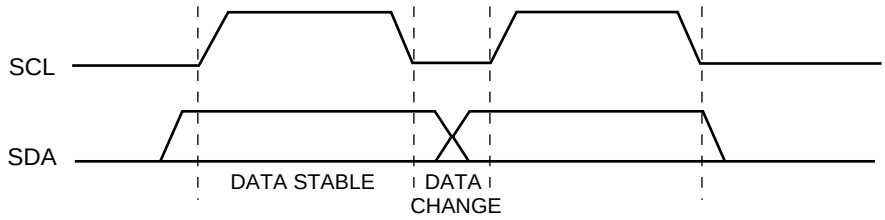
Write Cycle Timing



DS800009-10

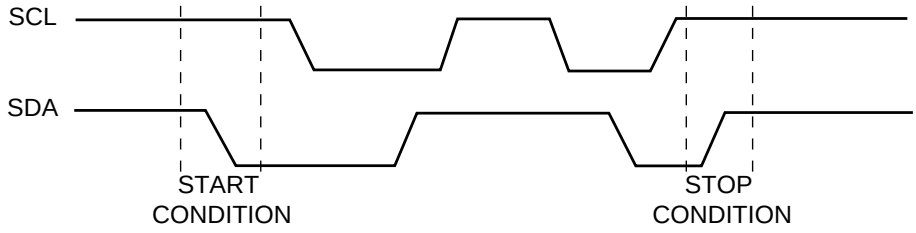
Note: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle.

Data Validity (Figure 2)



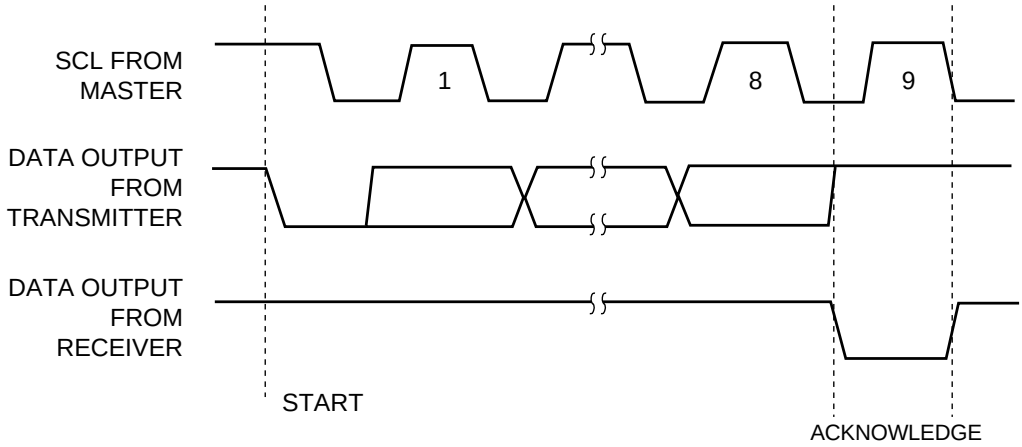
DS800009-11

Start and Stop Definition (Figure 3)



DS800009-12

Acknowledge Response from Receiver (Figure 4)



DS800009-13

Write Cycle Timing (Continued)

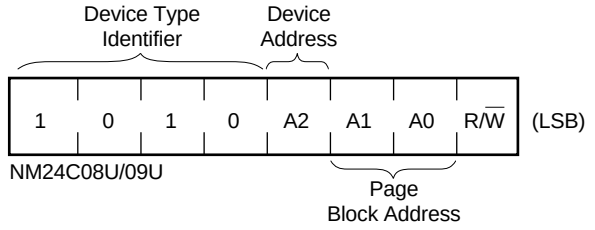
The NM24C08U/09U device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the NM24C08U/09U will respond with an acknowledge after the receipt of each subsequent eight bit byte.

In the read mode the NM24C08U/09U slave will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are those of the device type identifier (*see Figure 5)*. This is fixed as 1010 for all EEPROM devices.

Slave Addresses (Figure 5)



DS800009-14

Refer to the following table for Slave Addresses string details:

Device	A0	A1	A2	Page Blocks	Page Block Addresses
NM24C08U/09U	P	P	A	4	00 01 10 11

A: Refers to a hardware configured Device Address pin
P: Refers to an internal PAGE BLOCK memory segment.

All IIC EEPROMs use an internal protocol that defines a PAGE BLOCK size of 2K bits (for Word addressess 0000 through 1111). Therefore, address bits A0, A1, or A2 (if designated 'P') are used to access a PAGE BLOCK in conjunction with the Word address used to access any individual data byte (Word).

The last bit of the slave address defines whether a write or read condition is requested by the master. A '1' indicates that a read operation is to be executed, and a '0' initiates the write mode.

A simple review: After the NM24C08U/09U recognizes the start condition, the devices interfaced to the IIC bus wait for a slave address to be transmitted over the SDA line. If the transmitted slave address matches an address of one of the devices, the designated slave pulls the line LOW with an acknowledge signal and awaits further transmissions.

Write Operations

BYTE WRITE

For a write operation a second address field is required which is a word address that is comprised of eight bits and provides access to any one of the 256 bytes in the selected page of memory. Upon receipt of the byte address the NM24C08U/09U responds with an acknowledge and waits for the next eight bits of data, again, responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the NM24C08U/09U begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the NM24C08U/09U inputs are disabled, and the device will not respond to any requests from the master. Refer to *Figure 6* for the address, acknowledge and data transfer sequence.

PAGE WRITE

The NM24C08U/09U is capable of a sixteen byte page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data byte is transferred, the master can transmit up to fifteen more bytes. After the receipt of each byte, the NM24C08U/09U will respond with an acknowledge.

After the receipt of each byte, the internal address counter increments to the next address and the next SDA data is accepted. If the master should transmit more than sixteen bytes prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to *Figure 7* for the address, acknowledge, and data transfer sequence.

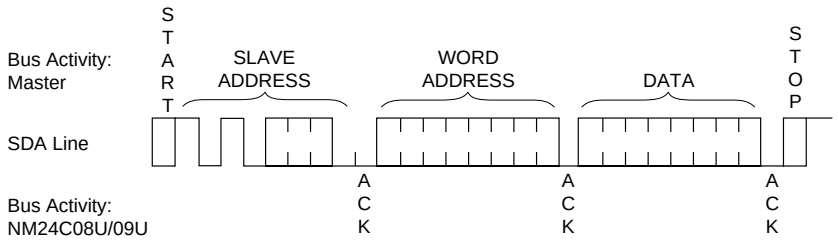
Acknowledge Polling

Once the stop condition is issued to indicate the end of the host's write operation the NM24C08U/09U initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the NM24C08U/09U is still busy with the write operation no ACK will be returned. If the NM24C08U/09U has completed the write operation an ACK will be returned and the host can then proceed with the next read or write operation.

Write Protection (NM24C09U Only)

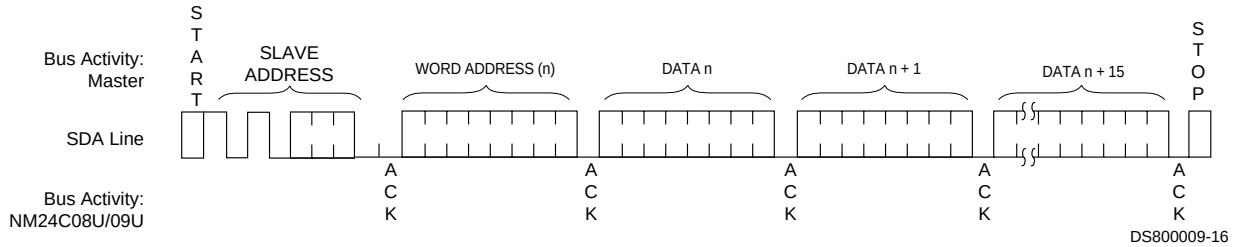
Programming of the upper half of the memory will not take place if the WP pin of the NM24C09U is connected to V_{CC}. The NM24C09U will accept slave and byte addresses; but if the memory accessed is write protected by the WP pin, the NM24C09U will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the stop condition is asserted.

Byte Write (Figure 6)



DS800009-15

Page Write (Figure 7)



DS800009-16

Read Operations

Read operations are initiated in the same manner as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to a one. There are three basic read operations: current address read, random read, and sequential read.

Current Address Read

Internally the NM24C08U/09U contains an address counter that maintains the address of the last byte accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ set to one, the NM24C08U/09U issues an acknowledge and transmits the eight bit byte. The master will not acknowledge the transfer but does generate a stop condition, and therefore the NM24C08U/09U discontinues transmission. Refer to *Figure* 8 for the sequence of address, acknowledge and data transfer.

Random Read

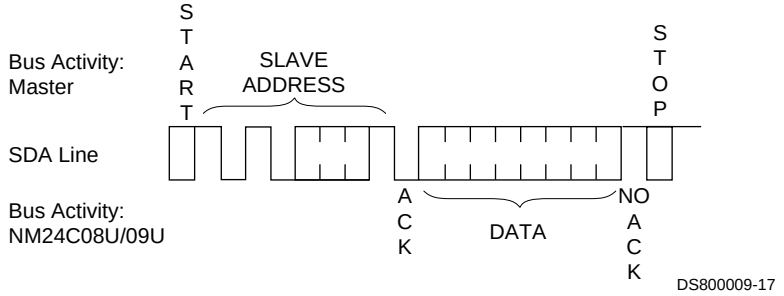
Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, slave address and then the byte address it is to read. After the byte address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the NM24C08U/09U and then by the eight bit data. The master will not acknowledge the transfer but does generate the stop condition, and therefore the NM24C08U/09U discontinues transmission. Refer to *Figure 9* for the address, acknowledge and data transfer sequence.

Sequential Read

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted in the same manner as the other read modes; however, the master now responds with an acknowledge, indicating it requires additional data. The NM24C08U/09U continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge or by generating a stop condition.

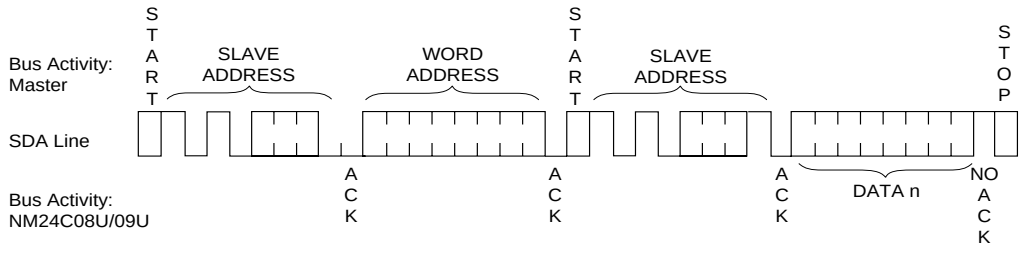
The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. After the entire memory has been read, the counter "rolls over" and the NM24C08U/09U continues to output data for each acknowledge received. Refer to *Figure 10* for the address, acknowledge, and data transfer sequence.

Current Address Read (Figure 8)



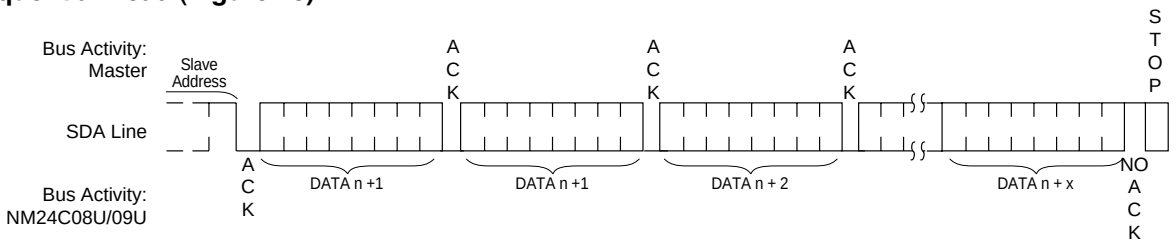
DS800009-17

Random Read (Figure 9)



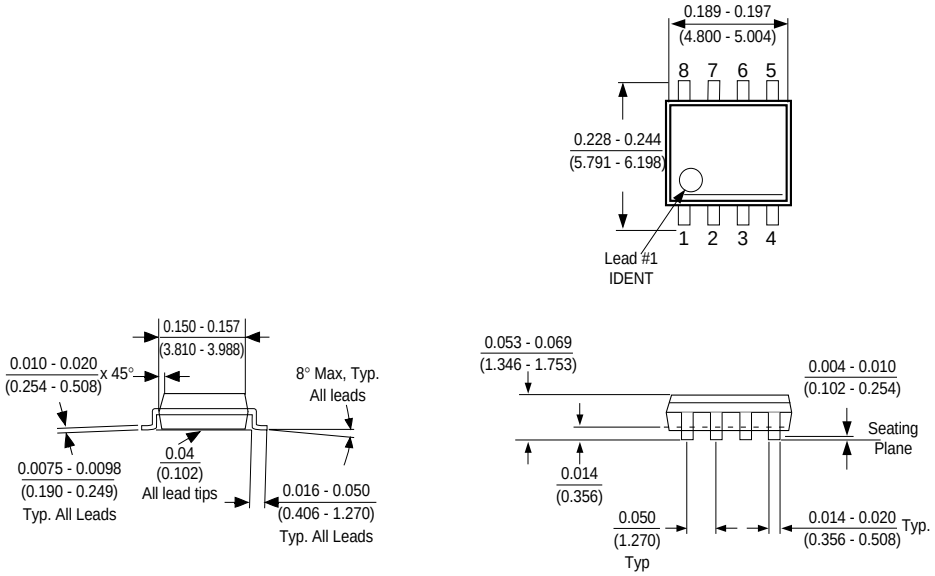
DS800009-18

Sequential Read (Figure 10)

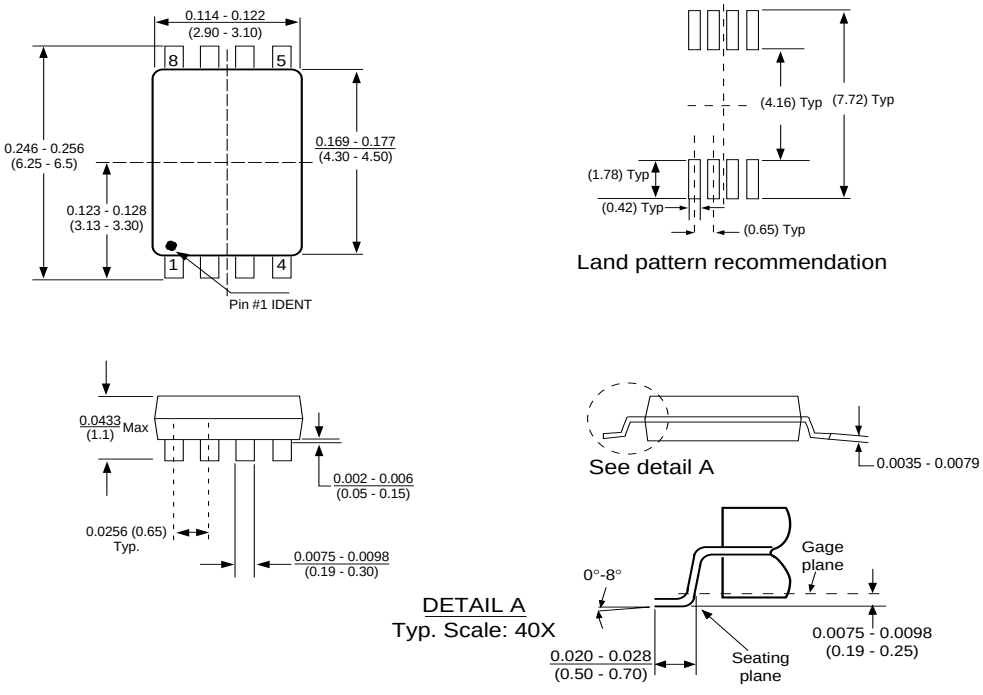


DS800009-19

Physical Dimensions inches (millimeters) unless otherwise noted



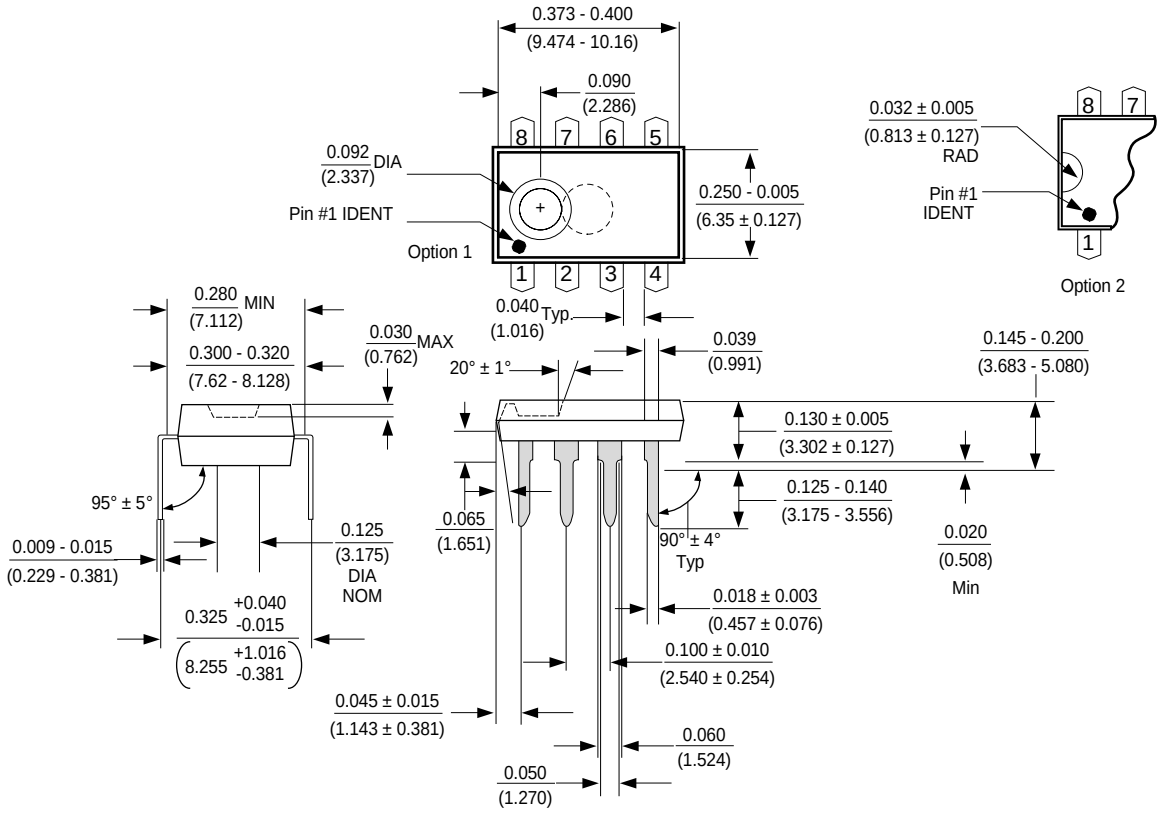
8-Pin Molded Small Outline Package (M8)
Package Number M08A



Notes: Unless otherwise specified
1. Reference JEDEC registration MO153. Variation AA. Dated 7/93

8-Pin Molded Thin Shrink Small Outline Package
Package Number MTC08

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Package Number N08E

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD
SEMICONDUCTOR™

February 2000

NM24C16/17 – 16K-Bit Standard 2-Wire Bus Interface Serial EEPROM

General Description

The NM24C16/17 devices are 16,384 bits of CMOS non-volatile electrically erasable memory. These devices conform to all specifications in the Standard IIC 2-wire protocol and are designed to minimize device pin count, and simplify PC board layout requirements.

The upper half (upper 8Kbit) of the memory of the NM24C17 can be write protected by connecting the WP pin to V_{CC}. This section of memory then becomes unalterable unless WP is switched to V_{SS}.

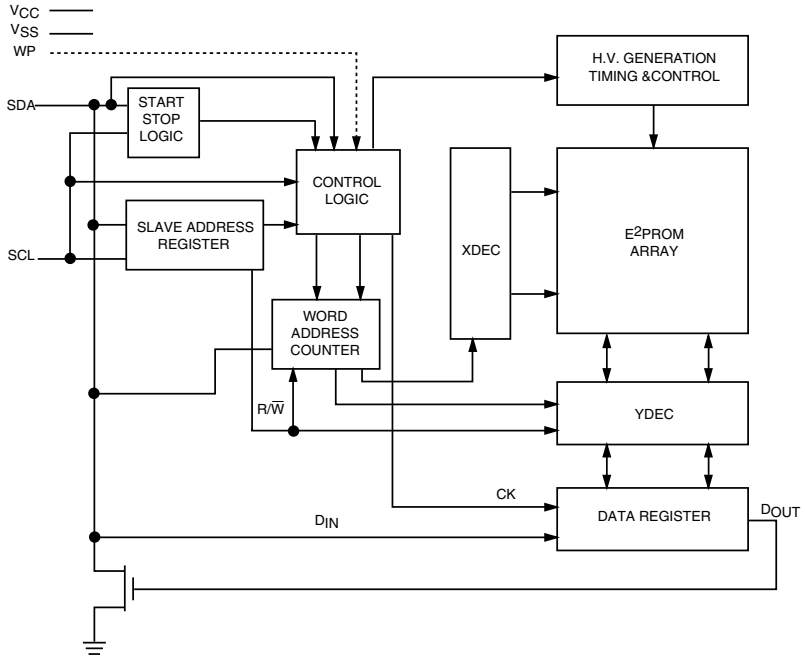
This communications protocol uses CLOCK (SCL) and DATA I/O (SDA) lines to synchronously clock data between the master (for example a microprocessor) and the slave EEPROM device(s). The Standard IIC protocol allows for a maximum of 16K of EEPROM memory which is supported by the Fairchild family in 2K, 4K, 8K, and 16K devices, allowing the user to configure the memory as the application requires with any combination of EEPROMs. In order to implement higher EEPROM memory densities on the IIC bus, the Extended IIC protocol must be used. (Refer to the NM24C32 or NM24C65 datasheets for more information.)

Fairchild EEPROMs are designed and tested for applications requiring high endurance, high reliability and low power consumption.

Features

- Extended operating voltage 2.7V – 5.5V
- 400 KHz clock frequency (F) at 2.7V - 5.5V
- 200µA active current typical
  10µA standby current typical
  1µA standby current typical (L)
  0.1µA standby current typical (LZ)
- IIC compatible interface
  – Provides bi-directional data transfer protocol
- Schmitt trigger inputs
- Sixteen byte page write mode
  – Minimizes total write time per byte
- Self timed write cycle
  Typical write cycle time of 6ms
- Hardware Write Protect for upper half (NM24C17 only)
- Endurance: 1,000,000 data changes
- Data retention greater than 40 years
- Packages available: 8-pin DIP, 8-pin SO, and 8-pin TSSOP
- Available in three temperature ranges
  - Commercial: 0° to +70°C
  - Extended (E): -40° to +85C
  - Automotive (V): -40° to +125°C

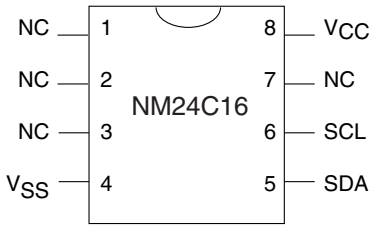
Block Diagram



DS500072-1

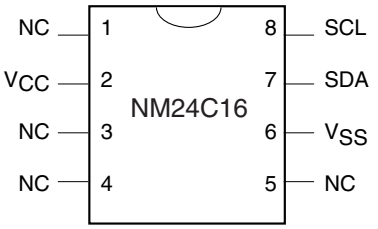
Connection Diagrams

Dual-in-Line Package (N) and SO Package (M8)



DS500072-2

TSSOP Package (MT8)



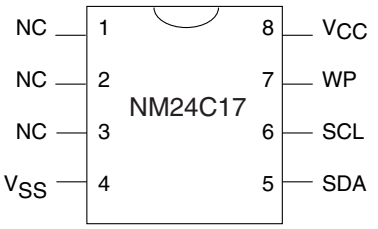
DS500072-3

See Package Number N08E, M08A and MTC08

Pin Names

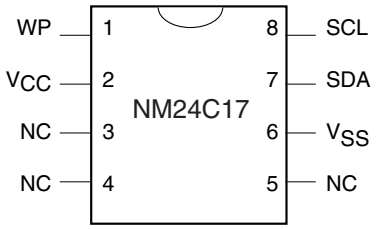
V_{SS}	Ground
SDA	Serial Data I/O
SCL	Serial Clock Input
NC	No Connection
V_{CC}	Power Supply

Dual-in-Line Package (N) and SO Package (M8)



DS500072-4

TSSOP Package (MT8)



DS500072-5

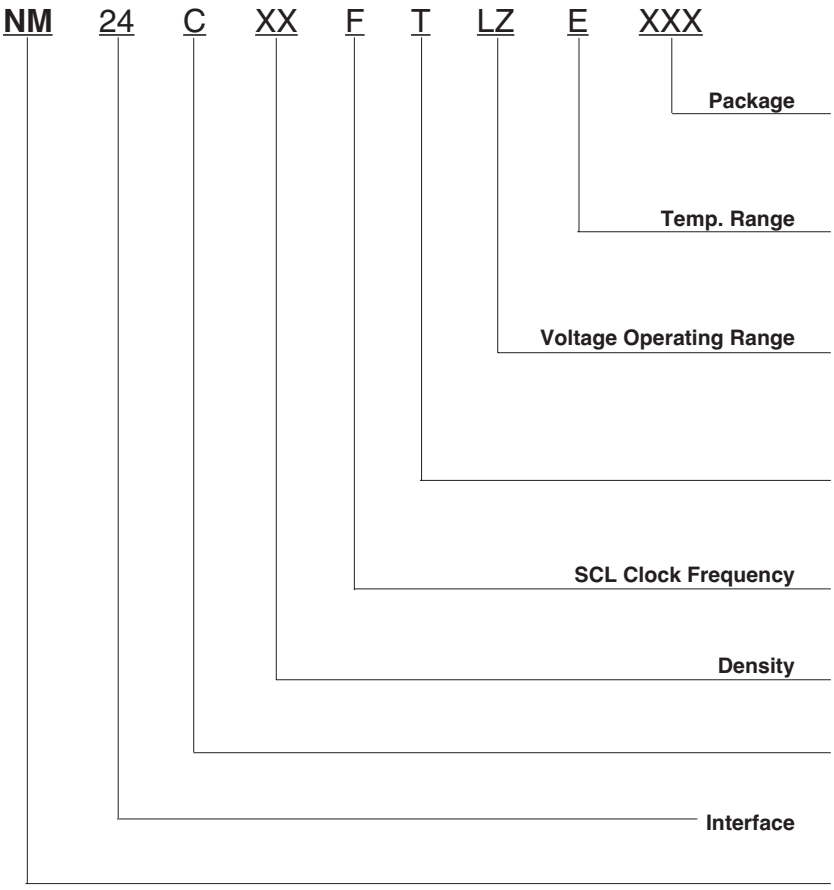
See Package Number N08E, M08A and MTC08

Pin Names

NC	No Connection
V_{SS}	Ground
SDA	Serial Data I/O
SCL	Serial Clock input
WP	Write Protect
V_{CC}	Power Supply

NOTE: Pins designated as "NC" are typically unbonded pins. However some of them are bonded for special testing purposes. Hence if a signal is applied to these pins, care should be taken that the voltage applied on these pins does not exceed the V_{CC} applied to the device. This will ensure proper operation.

Ordering Information



	Letter	Description
Package	N	8-pin DIP
	M8	8-pin SOIC
	MT8	8-pin TSSOP
Temp. Range	None	0 to 70°C
	V	-40 to +125°C
	E	-40 to +85°C
Voltage Operating Range	Blank	4.5V to 5.5V
	L	2.7V to 5.5V
	LZ	2.7V to 5.5V and <1µA Standby Current
	Blank	Normal Pin Out
	T	Rotated Die Pin Out
SCL Clock Frequency	Blank	100KHz
	F	400KHz
Density	16	16K
	17	16K with Write Protect
	C	CMOS Technology
Interface	24	IIC
	NM	**Fairchild Non-Volatile Memory**

Product Specifications

Absolute Maximum Ratings

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltages with Respect to Ground	6.5V to –0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min.

Operating Conditions

Ambient Operating Temperature	
NM24C16/17	0°C to +70°C
NM24C16E/17E	-40°C to +85°C
NM24C16V/17V	-40°C to +125°C
Positive Power Supply	
NM24C16/17	4.5V to 5.5V
NM24C16L/17L	2.7V to 5.5V
NM24C16LZ/17LZ	2.7V to 5.5V

DC Electrical Characteristics (2.7V to 5.5V)

Symbol	Parameter	Test Conditions		Limits			Units
				Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 400 KHz f_{SCL} = 100 KHz			0.2	1.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}	V_{CC} = 2.7V - 5.5V V_{CC} = 2.7V - 5.5V (L) V_{CC} = 2.7V - 4.5V (LZ)		10 1 0.1	50 10 1	µA µA µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}			0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}			0.1	1	µA
V_{IL}	Input Low Voltage			–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA				0.4	V

Capacitance T_A = +25°C, f = 100/400 KHz, V_{CC} = 5V (Note 2)

Symbol	Test	Conditions	Max	Units
$C_{I/O}$	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN}	Input Capacitance (A0, A1, A2, SCL)	V_{IN} = 0V	6	pF

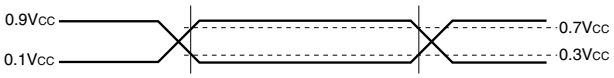
Note 1: Typical values are T_A = 25°C and nominal supply voltage of 5V for 4.5V-5.5V operation and at 3V for 2.7V-4.5V operation.

Note 2: This parameter is periodically sampled and not 100% tested.

AC Test Conditions

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10 ns
Input & Output Timing Levels	V_{CC} x 0.3 to V_{CC} x 0.7
Output Load	1 TTL Gate and C_L = 100 pF

AC Testing Input/Output Waveforms



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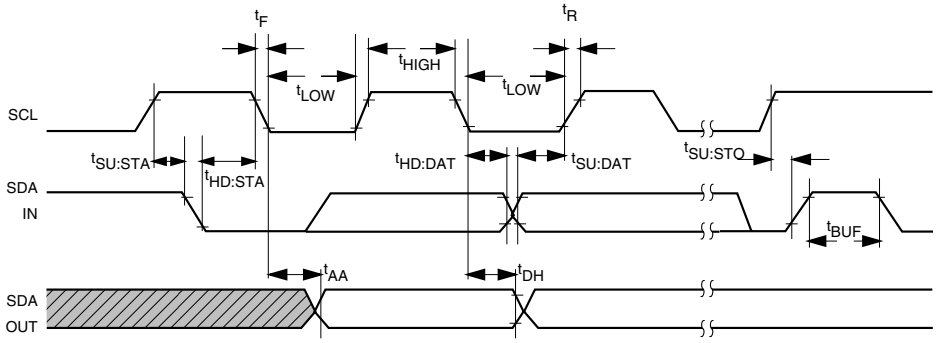
Read and Write Cycle Limits (Standard and Low V_{CC} Range 2.7V - 5.5V)

Symbol	Parameter	100 KHz		400 KHz		Units
		Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		100		400	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs (Minimum V_{IN} Pulse width)		100		50	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	0.1	0.9	µs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		1.3		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		0.6		µs
t_{LOW}	Clock Low Period	4.7		1.5		µs
t_{HIGH}	Clock High Period	4.0		0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		µs
$t_{HD:DAT}$	Data in Hold Time	20		20		ns
$t_{SU:DAT}$	Data in Setup Time	250		100		ns
t_R	SDA and SCL Rise Time		1		0.3	µs
t_F	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		0.6		µs
t_{DH}	Data Out Hold Time	300		50		ns
t_{WR} (Note 3)	Write Cycle Time - NM24C16/17 - NM24C16/17L, NM24C16/17LZ		10 15		10 15	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the NM24C16/17 bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address. Refer "Write Cycle Timing" diagram.

Bus Timing



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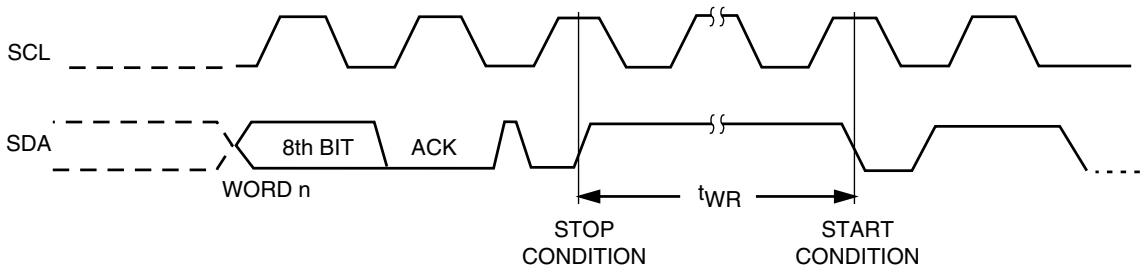
Write Cycle Timing



Note: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle.

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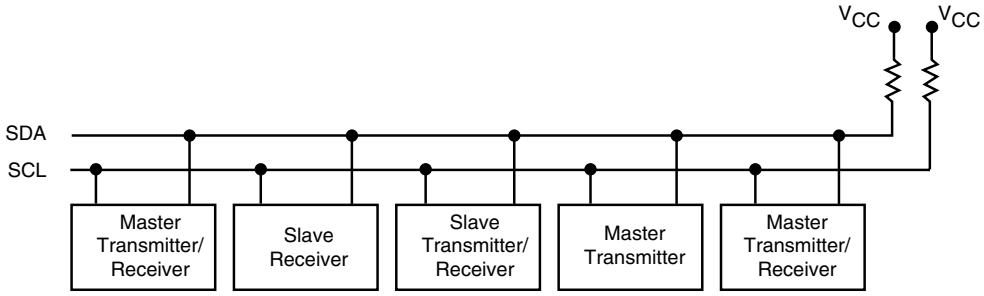
Typical System Configuration



Note: Due to open drain configuration of SDA and SCL, a bus-level pull-up resistor is called for, (typical value = 4.7kΩ)

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Background Information (IIC Bus)

IIC bus allows synchronous bi-directional communication between a TRANSMITTER and a RECEIVER using a Clock signal (SCL) and a Data signal (SDA). Additionally there are up to three Address signals (A2, A1 and A0) which collectively serve as "chip select signal" to a device (example EEPROM) on the IIC bus.

All communication on the IIC bus must be started with a valid START condition (by a MASTER), followed by transmittal (by the MASTER) of byte(s) of information (Address/Data). For every byte of information received, the addressed RECEIVER provides a valid ACKNOWLEDGE pulse to further continue the communication unless the RECEIVER intends to discontinue the communication. Depending on the direction of transfer (Write or Read), the RECEIVER can be a SLAVE or the MASTER. A typical IIC communication concludes with a STOP condition (by the MASTER).

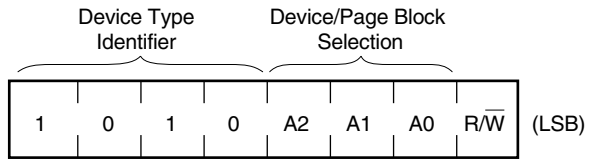
Addressing an EEPROM memory location involves sending a command string with the following information:

[DEVICE TYPE]—[DEVICE/PAGE BLOCK SELECTION]—[R/W BIT]—{acknowledge pulse}—[ARRAY ADDRESS]

Slave Address

Slave Address is an 8-bit information consisting of a Device type field (4bits), Device/Page block selection field (3bits) and Read/Write bit (1bit).

Slave Address Format



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Device Type

IIC bus is designed to support a variety of devices such as RAMs, EPROMs etc., along with EEPROMS. Hence to properly identify various devices on the IIC bus, a 4-bit “Device Type” identifier string is used. For EEPROMS, this 4-bit string is 1-0-1-0. Every IIC device on the bus internally compares this 4-bit string to its own “Device Type” string to ensure proper device selection.

Device/Page Block Selection

When multiple devices of the same type (e.g. multiple EEPROMS) are present on the IIC bus, then the A2, A1 and A0 address information bits are also used as part of the Slave Address. Every IIC device on the bus internally compares this 3-bit string to its own physical configuration (A2, A1 and A0 pins) to ensure proper device selection. This comparison is in addition to the “Device Type” comparison. In addition to selecting an EEPROM, these 3 bits are also used to select a “page block” within the selected EEPROM. Each page block is 2Kbit (256Bytes) in size. Depending on the density, an EEPROM can contain from a minimum of 1 to a maximum of 8 page blocks (in multiples of 2) and selection of a page block within a device is by using A2, A1 and A0 bits.

Read/Write Bit

Last bit of the Slave Address indicates if the intended access is Read or Write. If the bit is "1," then the access is Read, whereas if the bit is "0," then the access is Write.

Acknowledge

Acknowledge is an active LOW pulse on the SDA line driven by an addressed receiver to the addressing transmitter to indicate receipt of 8-bits of data. The receiver provides an ACK pulse for every 8-bits of data received. This handshake mechanism is done as follows: After transmitting 8-bits of data, the transmitter releases the SDA line and waits for the ACK pulse. The addressed receiver, if present, drives the ACK pulse on the SDA line during the 9th clock and releases the SDA line back (to the transmitter). Refer *Figure 3*.

Array Address

Array address is an 8-bit information containing the address of a memory location to be selected within a page block of the device.

16K bit Addressing Limitation:

Standard IIC specification limits the maximum size of EEPROM memory on the bus to 16K bits. This limitation is due to the addressing protocol implemented which consists of the 8-bit Slave Address and an additional 8-bit field called Array Address. This Array Address selects 1 out of 256 locations (2^8=256). Since the data format of IIC specification is 8-bit wide, a total of 256 x 8 = 2048 = 2K bit now becomes addressable by this 8-bit Array Address. This 2K bit is typically referred as a “Page Block”. Combining this 8-bit Array Address with the 3-bit Device/Page address (part of Slave Address) allows a maximum of 8 pages (2^3=8) of memory that can be addressed. Since each page is 2K bit in size, 8 x 2K bit = 16K bit is the maximum size of memory that is addressable on the Standard IIC bus. This 16Kb of memory can be in the form of a single 16Kb EEPROM device or multiple EEPROMs of varying density (in 2Kb multiples) to a maximum total of 16Kb. To address the needs of systems that require more than 16Kb on the IIC bus, a different specification called “Extended IIC Specification” is used. Please refer to NM24C32xx Datasheet for more information on Extended IIC Specification.

DEFINITIONS	
WORD	8 bits (byte) of data
PAGE	16 sequential byte locations starting at a 16-byte address boundary, that may be programmed during a "page write" programming cycle
PAGE BLOCK	2048 (2K) bits organized into 16 pages of addressable memory. (8 bits) x (16 bytes) x (16 pages) = 2048 bits
MASTER	Any IIC device CONTROLLING the transfer of data (such as a microprocessor)
SLAVE	Device being controlled (EEPROMs are always considered Slaves)
TRANSMITTER	Device currently SENDING data on the bus (may be either a Master or Slave).
RECEIVER	Device currently RECEIVING data on the bus (Master or Slave)

Pin Descriptions

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bi-directional pin used to transfer data into and out of the device. It is an open drain output and may be wire–ORed with any number of open drain or open collector outputs.

Write Protect (WP) (NM24C17 Only)

If tied to V_{CC}, PROGRAM operations onto the upper half (upper 8Kbit) of the memory will not be executed. READ operations are possible. If tied to V_{SS}, normal operation is enabled, READ/WRITE over the entire memory is possible.

This feature allows the user to assign the upper half of the memory as ROM which can be protected against accidental programming. When write is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

This pin has an internal pull-down circuit. However, on systems where write protection is not required it is recommended that this pin is tied to V_{SS}.

Device Selection Inputs A2, A1 and A0 (as appropriate)

These inputs collectively serve as "chip select" signal to an EEPROM when multiple EEPROMs are present on the same IIC bus. Hence these inputs, if present, should be connected to V_{CC} or V_{SS} in a unique manner to allow proper selection of an EEPROM amongst multiple EEPROMs. During a typical addressing sequence, every EEPROM on the IIC bus compares the configuration of these inputs to the respective 3 bit "Device/Page block selection" information (part of slave address) to determine a valid selection. For e.g. if the 3 bit "Device/Page block selection" is 1-0-1, then the EEPROM whose "Device Selection inputs" (A2, A1 and A0) are connected to V_{CC}-V_{SS}-V_{CC} respectively, is selected.

Depending on the density, only appropriate number of "Device Selection inputs" are provided on an EEPROM. For every "Device selection input" that is not present on the device, the corresponding bit in the "Device/Page block selection" field is used to select a "Page Block" within the device instead of the device itself. Following table illustrates the above:

EEPROM Density	Number of Page Blocks	Device Selection Inputs Provided			Address Bits Selecting Page Block
2k bit	1	A0	A1	A2	None
4k bit	2	—	A1	A2	A0
8k bit	4	—	—	A2	A0 and A1
16k bit	8	—	—	—	A0, A1 and A2

Note that even when just one EEPROM present on the IIC bus, these pins should be tied to V_{CC} or V_{SS} to ensure proper termination.

Device Operation

The NM24C16/17 supports a bi-directional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the NM24C16/17 will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to *Figure 1* and *Figure 2* on next page.

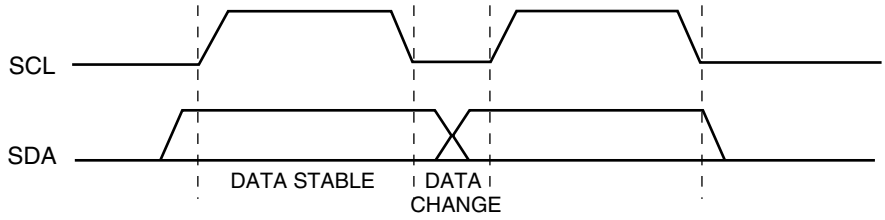
Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The NM24C16/17 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Stop Condition

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the NM24C16/17 to place the device in the standby power mode, except when a Write operation is being executed, in which case a second stop condition is required after t_{WR} period, to place the device in standby mode.

Data Validity (Figure 1)



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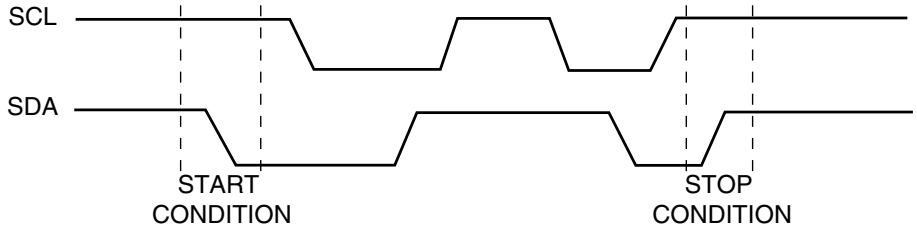
Start and Stop Definition (Figure 2)



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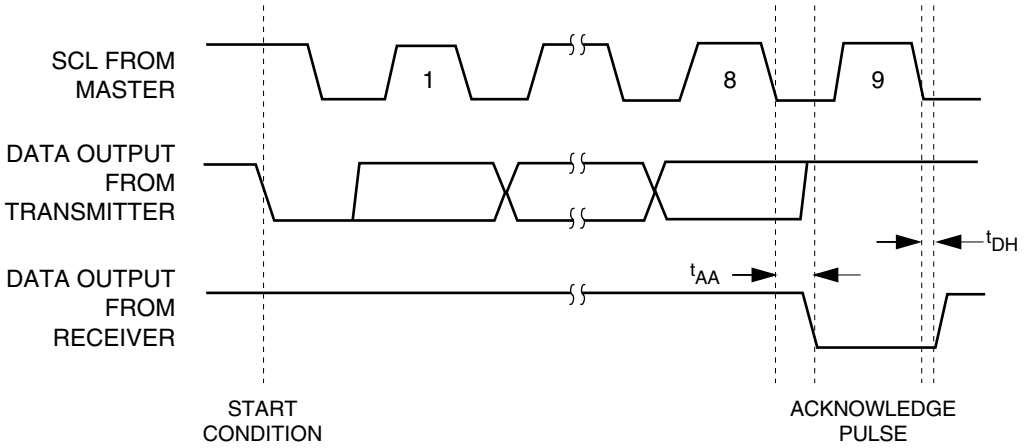
Acknowledge Response from Receiver (Figure 3)



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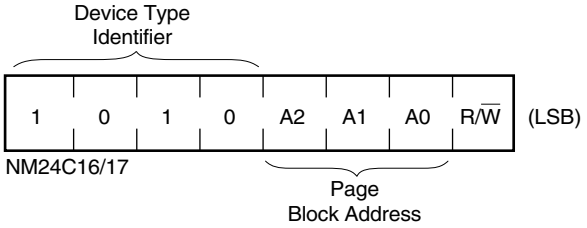
Acknowledge

The NM24C16/17 device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the NM24C16/17 will respond with an acknowledge after the receipt of each subsequent eight bit byte.

In the read mode the NM24C16/17 slave will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected, NM24C16/17 will continue to transmit data. If an acknowledge is not detected,NM24C16/17 will terminate further data transmissions and await the stop condition to return to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are those of the device type identifier. This is fixed as 1010 for all EEPROM devices.



Refer the following table for Slave Addresses string details:

Device	A0	A1	A2	Page Blocks	Page Block Addresses
NM24C16/17	P	P	P	8	000, 001, 010 ... 111

P: Refers to an internal PAGE BLOCK.

All IIC EEPROMs use an internal protocol that defines a PAGE BLOCK size of 2K bits (for Word addresses 0x00 through 0xFF). Therefore, address bits A0, A1, or A2 (if designated 'P') are used to access a PAGE BLOCK in conjunction with the Word address used to access any individual data byte.

The last bit of the slave address defines whether a write or read condition is requested by the master. A '1' indicates that a read operation is to be executed, and a '0' initiates the write mode.

A simple review: After the NM24C16/17 recognizes the start condition, the devices interfaced to the IIC bus wait for a slave address to be transmitted over the SDA line. If the transmitted slave address matches an address of one of the devices, the designated slave pulls the line LOW with an acknowledge signal and awaits further transmissions.

Write Operations

BYTE WRITE

For a write operation a second address field is required which is a word address that is comprised of eight bits and provides access to any one of the 256 bytes in the selected page of memory. Upon receipt of the byte address the NM24C16/17 responds with an acknowledge and waits for the next eight bits of data, again, responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the NM24C16/17 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the NM24C16/17 inputs are disabled, and the device will not respond to any requests from the master for the duration of t_{WR}. Refer to *Figure 4* for the address, acknowledge and data transfer sequence.

PAGE WRITE

To minimize write cycle time, NM24C16/17 offer Page Write feature, by which, up to a maximum of 16 contiguous bytes locations can be programmed all at once (instead of 16 individual byte writes). To facilitate this feature, the memory array is organized in terms of "Pages." A Page consists of 16 contiguous byte locations starting at every 16-Byte address boundary (for example, starting at array address 0x00, 0x10, 0x20 etc.). Page Write operation limits access to byte locations within a page. In other words a single Page Write operation will not cross over to locations on another page but will "roll over" to the beginning of the page whenever end of Page is reached and additional locations are a continued to be accessed. A Page Write operation can be initiated to begin at any location within a page (starting address of the Page Write operation need not be the starting address of a Page).

Page Write is initiated in the same manner as the Byte Write operation; but instead of terminating the cycle after transmitting the first data byte, the master can further transmit up to 15 more bytes. After the receipt of each byte, NM24C16/17 will respond with an acknowledge pulse, increment the internal address counter to the next address and is ready to accept the next data. If the master should transmit more than sixteen bytes prior to generating the STOP condition, the address counter will "roll over" and previously written data will be overwritten. As with the Byte Write operation, all inputs are disabled until completion of the internal write cycle. Refer to *Figure 5* for the address, acknowledge and data transfer sequence.

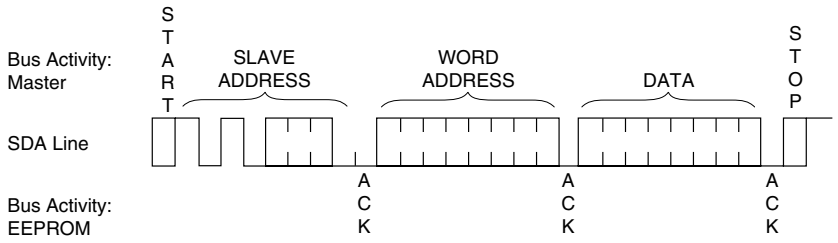
Acknowledge Polling

Once the stop condition is issued to indicate the end of the host's write operation the NM24C16/17 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the NM24C16/17 is still busy with the write operation no ACK will be returned. If the NM24C16/17 has completed the write operation an ACK will be returned and the host can then proceed with the next read or write operation.

Write Protection (NM24C17 Only)

Programming of the upper half (upper 8Kbit) of the memory will not take place if the WP pin of the NM24C17 is connected to V_{CC}. The NM24C17 will respond to slave and byte addresses; but if the memory accessed is write protected by the WP pin, the NM24C17 will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the stop condition is asserted.

Byte Write (Figure 4)



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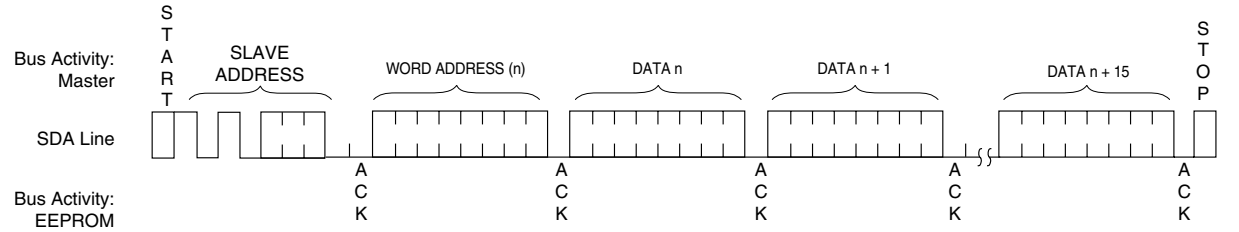
Page Write (Figure 5)



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Read Operations

Read operations are initiated in the same manner as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to a one. There are three basic read operations: current address read, random read, and sequential read.

Current Address Read

Internally the NM24C16/17 contains an address counter that maintains the address of the last byte accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ set to one, the NM24C16/17 issues an acknowledge and transmits the eight bit byte. The master will not acknowledge the transfer but does generate a stop condition, and therefore the NM24C16/17 discontinues transmission. Refer to *Figure* 6 for the sequence of address, acknowledge and data transfer.

Random Read

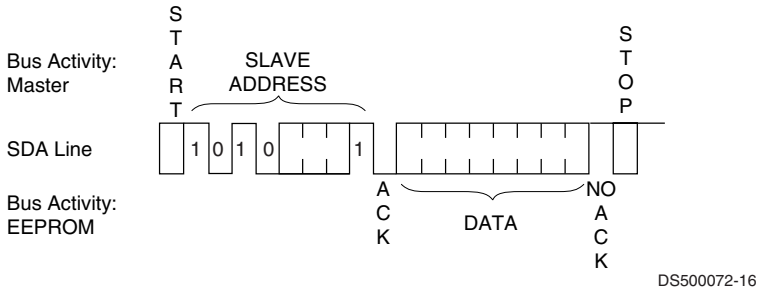
Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, slave address with the R/$\overline{W}$ bit set to zero and then the byte address it is to read. After the byte address acknowledge, the master immediately issues another start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the NM24C16/17 and then by the eight bit byte. The master will not acknowledge the transfer but does generate the stop condition, and therefore the NM24C16/17 discontinues transmission. Refer to *Figure 7* for the address, acknowledge and data transfer sequence.

Sequential Read

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted in the same manner as the other read modes; however, the master now responds with an acknowledge, indicating it requires additional data. The NM24C16/17 continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge or by generating a stop condition.

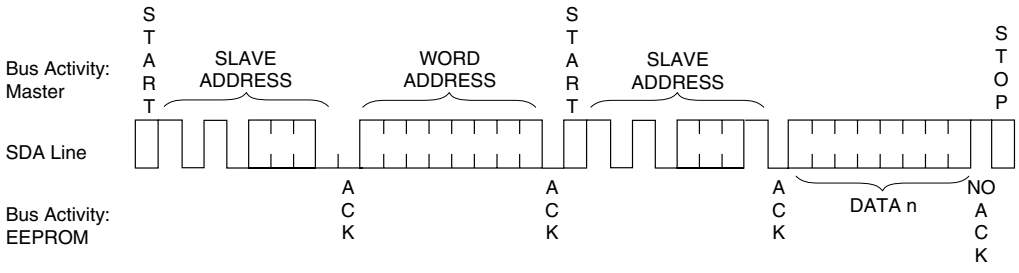
The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. After the entire memory has been read, the counter "rolls over" to the beginning of the memory. NM24C16/17 continues to output data for each acknowledge received. Refer to *Figure 8* for the address, acknowledge, and data transfer sequence.

Current Address Read (Figure 6)



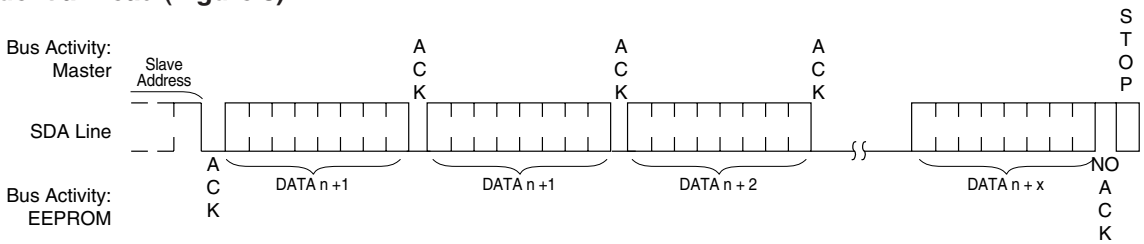
DS500072-16

Random Read (Figure 7)



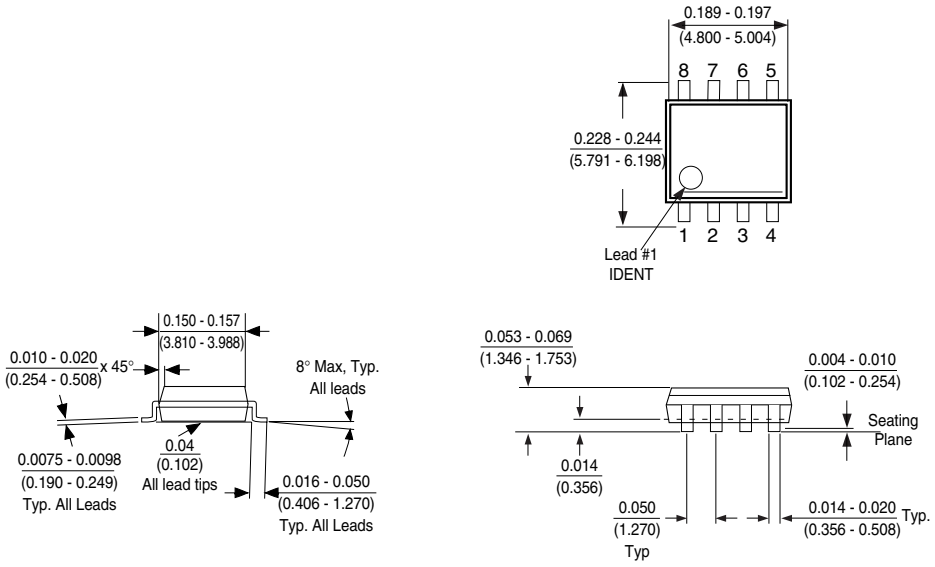
DS500072-17

Sequential Read (Figure 8)

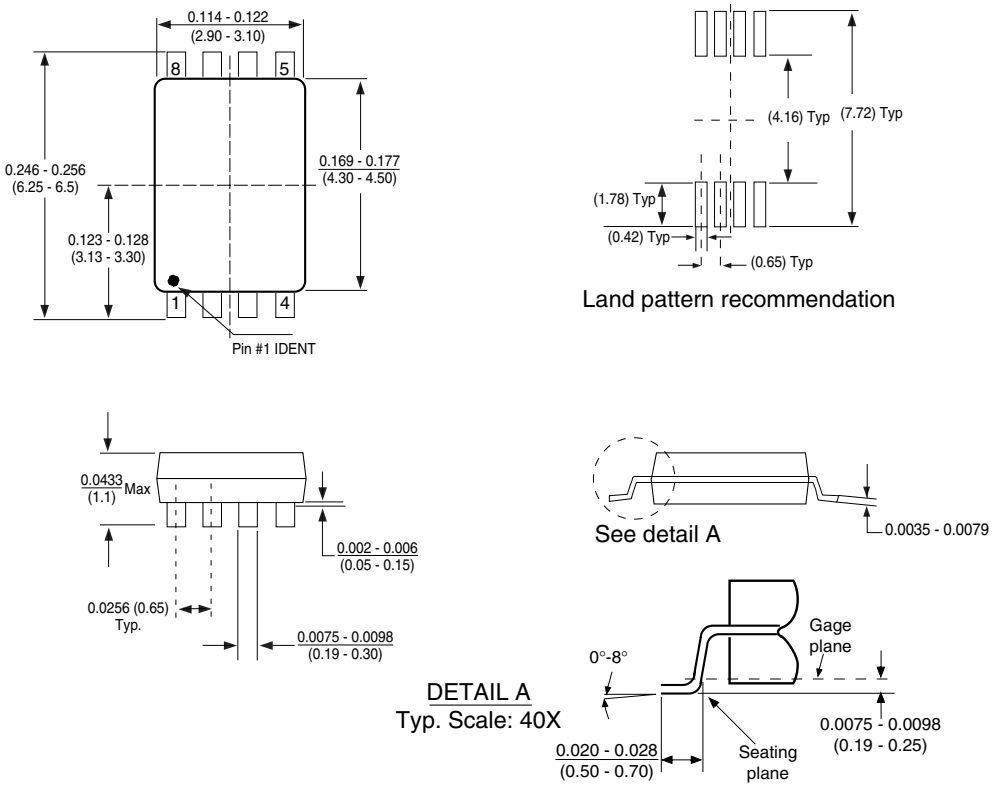


DS500072-18

Physical Dimensions inches (millimeters) unless otherwise noted



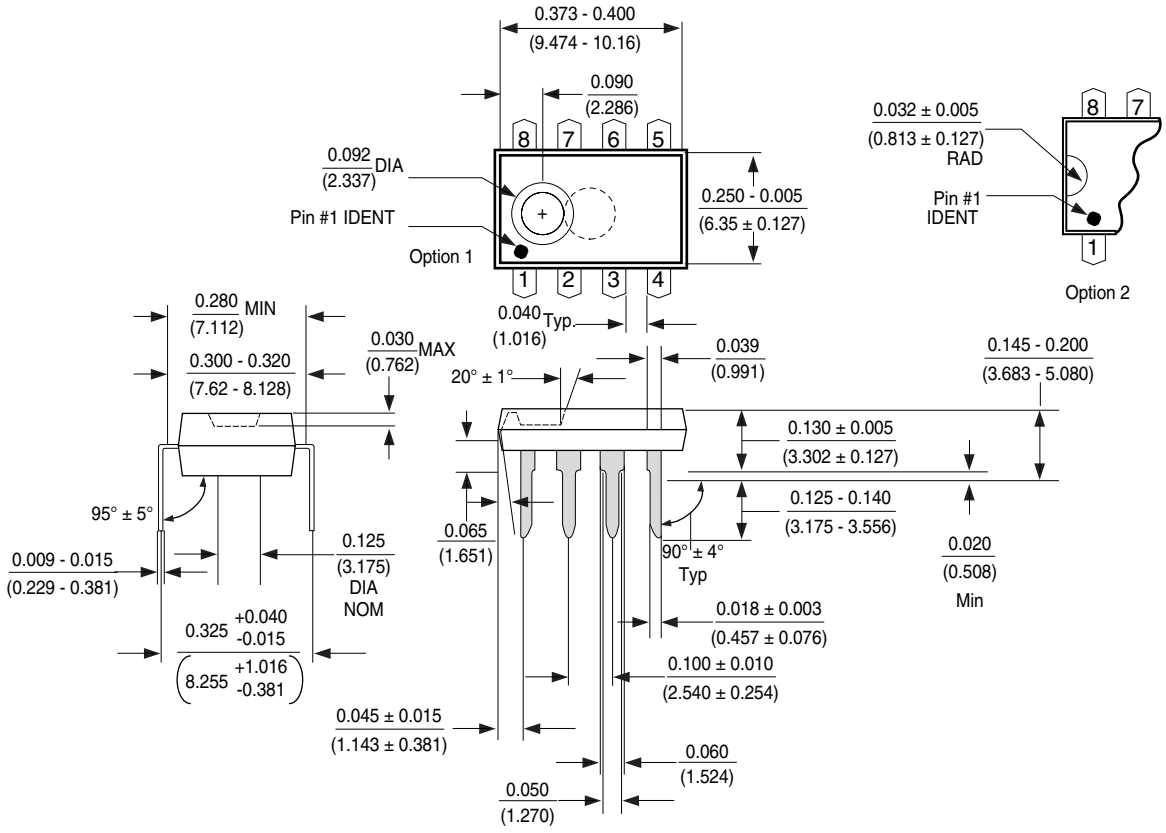
8-Pin Molded Small Outline Package (M8)
Package Number M08A



Notes: Unless otherwise specified
1. Reference JEDEC registration MO153. Variation AA. Dated 7/93

8-Pin Molded Thin Shrink Small Outline Package (MT8)
Package Number MTC08

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Package Number N08E

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

August 1999

NM24C16U/NM24C17U 16K-Bit Serial EEPROM 2-Wire Bus Interface

General Description

The NM24C16U/17U devices are 16K (16,384) bit serial interface CMOS EEPROMs (Electrically Erasable Programmable Read-Only Memory). These devices fully conform to the **Standard** I²C™ 2-wire protocol which uses Clock (SCL) and Data I/O (SDA) pins to synchronously clock data between the "master" (for example a microprocessor) and the "slave" (the EEPROM device). In addition, the serial interface allows a minimal pin count packaging designed to simplify PC board layout requirements and offers the designer a variety of low voltage and low power options.

NM24C17U incorporates a hardware "Write Protect" feature, by which, the upper half of the memory can be disabled against programming by connecting the WP pin to V_{CC}. This section of memory then effectively becomes a ROM (Read-Only Memory) and can no longer be programmed as long as WP pin is connected to V_{CC}.

Fairchild EEPROMs are designed and tested for applications requiring high endurance, high reliability and low power consumption for a continuously reliable non-volatile solution for all markets.

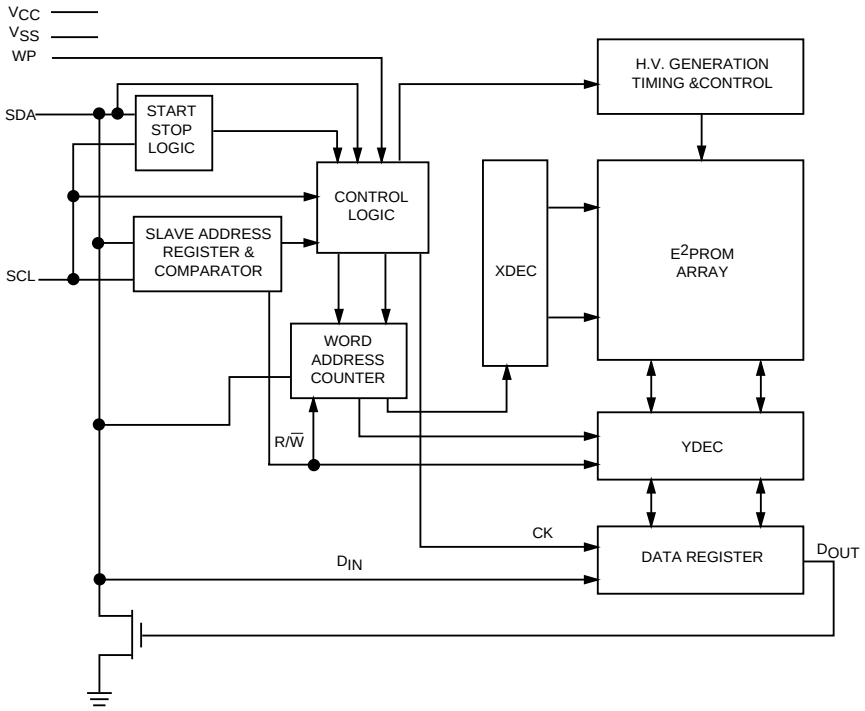
Functions

- I²C™ compatible interface
- 4,096 bits organized as 512 x 8
- Extended 2.7V – 5.5V operating voltage
- 100 KHz or 400 KHz operation
- Self timed programming cycle (6ms typical)
- "Programming complete" indicated by ACK polling
- NM24C17U: Memory "Upper Block" Write Protect pin

Features

- The I²C™ interface allows the smallest I/O pincount of any EEPROM interface
- 16 byte page write mode to minimize total write time per byte
- Typical 200µA active current (I_{CCA})
- Typical 1µA standby current (I_{SB}) for "L" devices and 0.1µA standby current for "LZ" devices
- Endurance: Up to 1,000,000 data changes
- Data retention greater than 40 years

Block Diagram

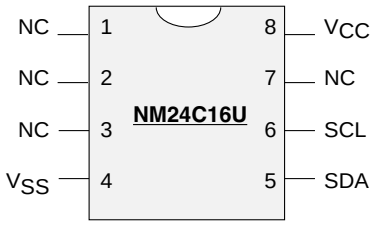


DS800010-1

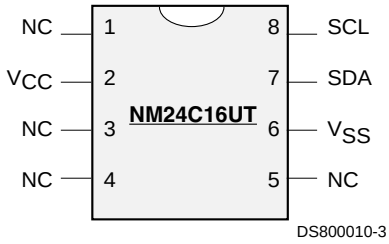
I²C™ is a registered trademark of Philips Electronics N.V.

Connection Diagrams

Dual-In-Line Package (N),
8-Pin SO Package (M8)



8-Pin TSSOP Package (MT8)
Rotated Die (24C16UT)

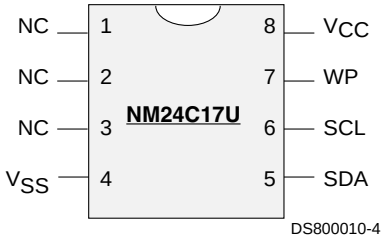


Top View
See Package Number N08E, M08A and MTC08

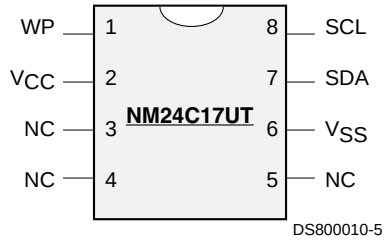
Pin Names

V_{SS}	Ground
SDA	Serial Data I/O
SCL	Serial Clock Input
NC	No Connection
V_{CC}	Power Supply

Dual-In-Line Package (N),
8-Pin SO Package (M8)



8-Pin TSSOP Package (MT8)
Rotated Die (24C17UT)

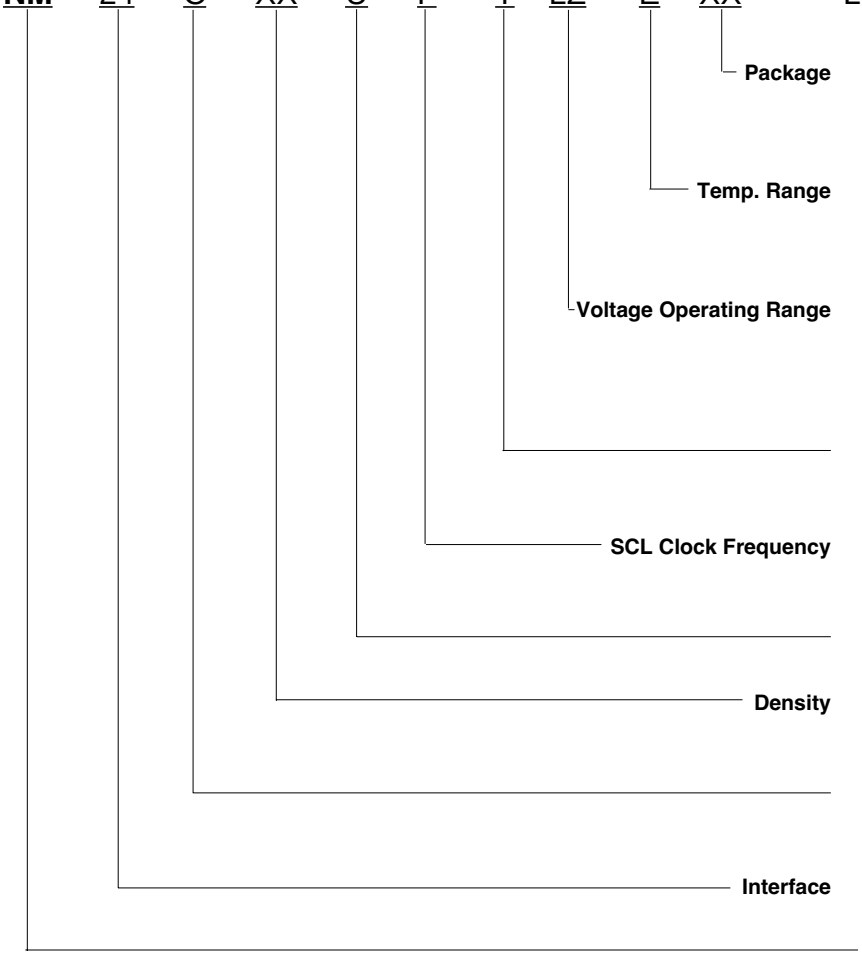


Top View
See Package Number N08E, M08A and MTC08

Pin Names

V_{SS}	Ground
SDA	Serial Data I/O
SCL	Serial Clock input
WP	Write Protect
V_{CC}	Power Supply
NC	No Connection

Ordering Information



	Letter	Description
Package	N	8-pin DIP
	M8	8-pin SOIC
	MT8	8-pin TSSOP
Temp. Range	None	0 to 70°C
	V	-40 to +125°C
	E	-40 to +85°C
Voltage Operating Range	Blank	4.5V to 5.5V
	L	2.7V to 5.5V
	LZ	2.7V to 5.5V and <1µA Standby Current
	Blank	Normal Pin Out
	T	Rotated Die Pin Out
SCL Clock Frequency	Blank	100KHz
	F	400KHz
	Ultralite	CS100UL Process
Density	16	16K
	17	16K with Write Protect
	C	CMOS Technology
	W	Total Array Write Protect
Interface	24	IIC
NM	**NM**	**Fairchild Non-Volatile Memory**

Product Specifications

Absolute Maximum Ratings

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltages with Respect to Ground	6.5V to –0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min.

Operating Conditions

Ambient Operating Temperature	
NM24C16U/17U	0°C to +70°C
NM24C16UE/17UE	-40°C to +85°C
NM24C16UV/17UV	-40°C to +125°C
Positive Power Supply	
NM24C16U/17U	4.5V to 5.5V
NM24C16UL/17UL	2.7V to 5.5V
NM24C16ULZ/17ULZ	2.7V to 5.5V

Standard V_{CC} (4.5V to 5.5V) DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 400 KHz f_{SCL} = 100 KHz		0.2	1.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		10	50	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	1	µA
V_{IL}	Input Low Voltage		–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Low V_{CC} (2.7V to 5.5V) DC Electrical Characteristics

Symbol	Parameter	Test Conditions		Limits			Units
				Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 400 KHz f_{SCL} = 100 KHz			0.2	1.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}	V_{CC} = 2.7V - 4.5V V_{CC} = 2.7V - 4.5V V_{CC} = 4.5V - 5.5V		1 0.1 10	10 1 50	µA µA µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}			0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}			0.1	1	µA
V_{IL}	Input Low Voltage			–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA				0.4	V

Capacitance T_A = +25°C, f = 100/400 KHz, V_{CC} = 5V (Note 2)

Symbol	Test	Conditions	Max	Units
$C_{I/O}$	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN}	Input Capacitance (A0, A1, A2, SCL)	V_{IN} = 0V	6	pF

Note 1: Typical values are T_A = 25°C and nominal supply voltage (5V).

Note 2: This parameter is periodically sampled and not 100% tested.

AC Conditions of Test

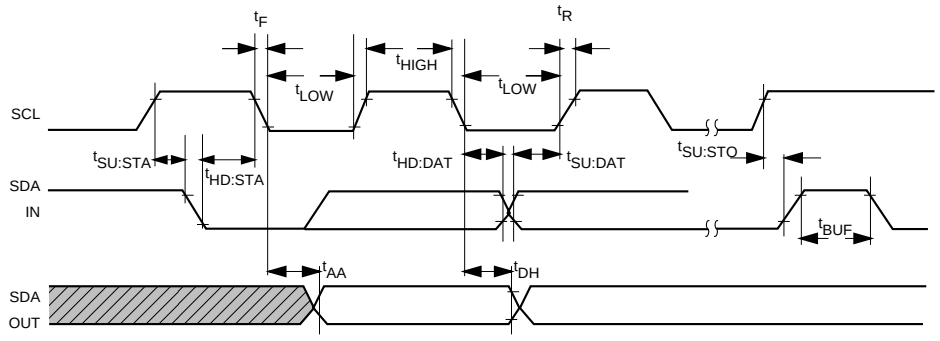
Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10 ns
Input & Output Timing Levels	V_{CC} x 0.5
Output Load	1 TTL Gate and C_L = 100 pF

Read and Write Cycle Limits (Standard and Low V_{CC} Range 2.7V - 5.5V)

Symbol	Parameter	100 KHz		400 KHz		Units
		Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		100		400	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs (Minimum V_{IN} Pulse width)		100		50	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	0.1	0.9	µs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		1.3		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		0.6		µs
t_{LOW}	Clock Low Period	4.7		1.5		µs
t_{HIGH}	Clock High Period	4.0		0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		µs
$t_{HD:DAT}$	Data in Hold Time	0		0		µs
$t_{SU:DAT}$	Data in Setup Time	250		100		ns
t_R	SDA and SCL Rise Time		1		0.3	µs
t_F	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		0.6		µs
t_{DH}	Data Out Hold Time	300		50		ns
t_{WR} (Note 3)	Write Cycle Time - NM24C16U/17U - NM24C16U/17UL, NM24C16U/17ULZ		10 15		10 15	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the NM24C16U/17U bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

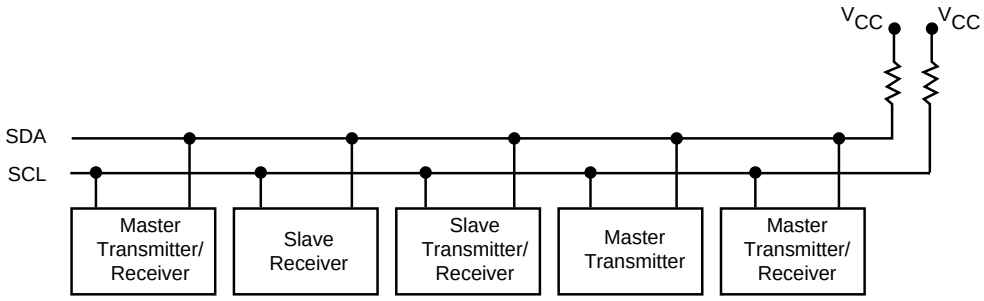
Bus Timing



DS800010-8

System Layout

Typical System Configuration



Note: Due to open drain configuration of SDA, a bus-level pull-up resistor is called for, (typical value = 4.7kΩ)

DS800010-20

Example of 16K of Memory on 2-Wire Bus

Device	Address Pins			Memory Size	# of Page Blocks
	A0	A1	A2		
NM24C16U/17U	No Connect	No Connect	No Connect	16,384 Bits	8

Device Operation

Background Information (IIC Bus)

As mentioned, the IIC bus allows synchronous bidirectional communication between Transmitter/Receiver using the SCL (clock) and SDA (Data I/O) lines. All communication must be started with a valid START condition, concluded with a STOP condition and acknowledged by the Receiver with an ACKNOWLEDGE condition.

As shown below, the EEPROMs on the IIC bus may be configured in any manner required, the total memory addressed can not exceed 16K (16,384 bits). EEPROM memory address programming is controlled by 2 methods:

- **All unused pins must be grounded** (tied to V_{SS}).
- Software addressing the required PAGE BLOCK within the device memory array (as sent in the Slave Address string).

For devices with densities greater than 16K, a different protocol, the Extended IIC protocol, is used. Refer to NM24C32U datasheet (for example) for additional details.

Addressing an EEPROM memory location involves sending a command string with the following information: [DEVICE TYPE]–[DEVICE ADDRESS]–[PAGE BLOCK ADDRESS]–[BYTE ADDRESS]

DEFINITIONS	
WORD	8 bits (byte) of data
PAGE	16 sequential addresses (one byte each) that may be programmed during a 'Page Write' programming cycle
PAGE BLOCK	2048 (2K) bits organized into **16 pages of addressable memory. (8 bits) x (16 pages) = 2048 bits**
MASTER	Any IIC device CONTROLLING the transfer of data (such as a microprocessor)
SLAVE	Device being controlled (EEPROMs are always considered Slaves)
TRANSMITTER	Device currently SENDING data on the bus (may be either a Master or Slave).
RECEIVER	Device currently RECEIVING data on the bus (Master or Slave)

Pin Descriptions

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire–ORed with any number of open drain or open collector outputs.

WP Write Protection (NM24C17U Only)

If tied to V_{CC}, PROGRAM operations onto the upper half of the memory will not be executed. READ operations are possible. If tied to V_{SS}, normal operation is enabled, READ/WRITE over the entire memory is possible.

This feature allows the user to assign the upper half of the memory as ROM which can be protected against accidental programming. When write is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

Device Operation

The NM24C16U/17U supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the NM24C16U/17U will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to *Figure 2* and *Figure 3* on next page.

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The NM24C16U/17U continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Stop Condition

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the NM24C16U/17U to place the device in the standby power mode.

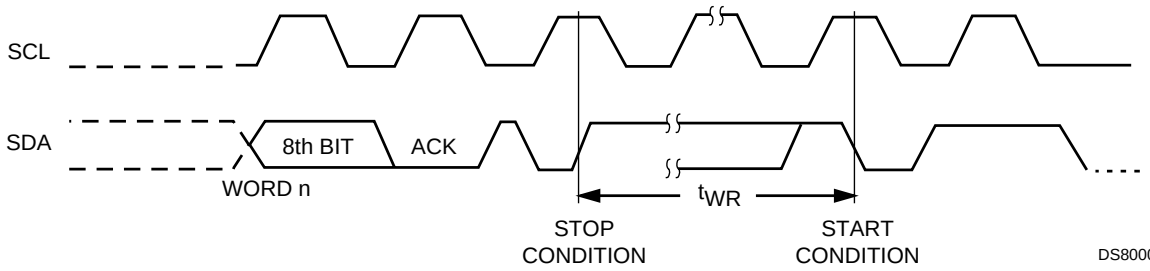
Write Cycle Timing

Acknowledge

Acknowledge is a hardware convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits.

During the ninth clock cycle the receiver will pull the SDA line to LOW to acknowledge that it received the eight bits of data. Refer to *Figure 4.*

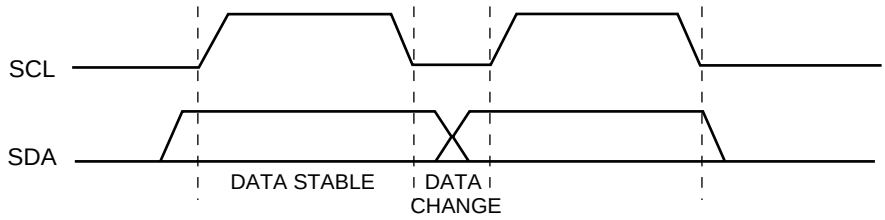
Write Cycle Timing (Figure 1)



DS800010-10

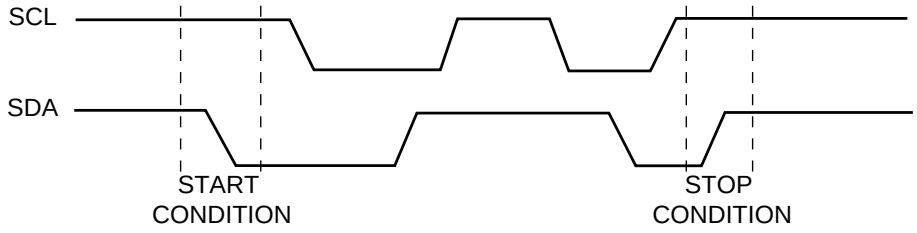
Note: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle.

Data Validity (Figure 2)



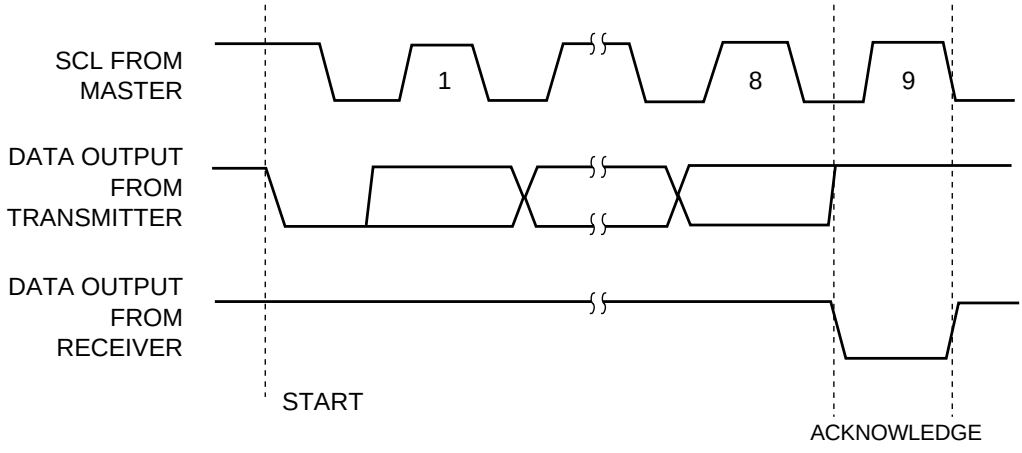
DS800010-11

Start and Stop Definition (Figure 3)



DS800010-12

Acknowledge Response from Receiver (Figure 4)



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Write Cycle Timing (Continued)

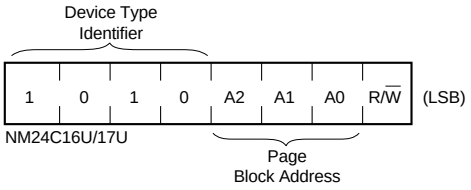
The NM24C16U/17U device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the NM24C16U/17U will respond with an acknowledge after the receipt of each subsequent eight bit byte.

In the read mode the NM24C16U/17U slave will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are those of the device type identifier (*see Figure 5)*. This is fixed as 1010 for all EEPROM devices.

Slave Addresses (Figure 5)



DS800010-14

Refer to the following table for Slave Addresses string details:

Device	A0	A1	A2	Page Blocks	Page Block Addresses
NM24C16U/17U	P	P	P	8	000 001 010 011 ... 111

P: Refers to an internal PAGE BLOCK memory segment.

All IIC EEPROMs use an internal protocol that defines a PAGE BLOCK size of 2K bits (for Word addressess 0000 through 1111). Therefore, address bits A0, A1, or A2 (if designated 'P') are used to access a PAGE BLOCK in conjunction with the Word address used to access any individual data byte (Word).

The last bit of the slave address defines whether a write or read condition is requested by the master. A '1' indicates that a read operation is to be executed, and a '0' initiates the write mode.

A simple review: After the NM24C16U/17U recognizes the start condition, the devices interfaced to the IIC bus wait for a slave address to be transmitted over the SDA line. If the transmitted slave address matches an address of one of the devices, the designated slave pulls the line LOW with an acknowledge signal and awaits further transmissions.

Write Operations

BYTE WRITE

For a write operation a second address field is required which is a word address that is comprised of eight bits and provides access to any one of the 256 bytes in the selected page of memory. Upon receipt of the byte address the NM24C16U/17U responds with an acknowledge and waits for the next eight bits of data, again, responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the NM24C16U/17U begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the NM24C16U/17U inputs are disabled, and the device will not respond to any requests from the master. Refer to *Figure 6* for the address, acknowledge and data transfer sequence.

PAGE WRITE

The NM24C16U/17U is capable of a sixteen byte page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data byte is transferred, the master can transmit up to fifteen more bytes. After the receipt of each byte, the NM24C16U/17U will respond with an acknowledge.

After the receipt of each byte, the internal address counter increments to the next address and the next SDA data is accepted. If the master should transmit more than sixteen bytes prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to *Figure 7* for the address, acknowledge, and data transfer sequence.

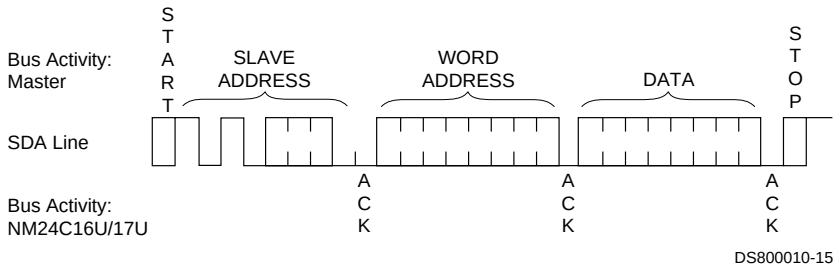
Acknowledge Polling

Once the stop condition is issued to indicate the end of the host's write operation the NM24C16U/17U initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the NM24C16U/17U is still busy with the write operation no ACK will be returned. If the NM24C16U/17U has completed the write operation an ACK will be returned and the host can then proceed with the next read or write operation.

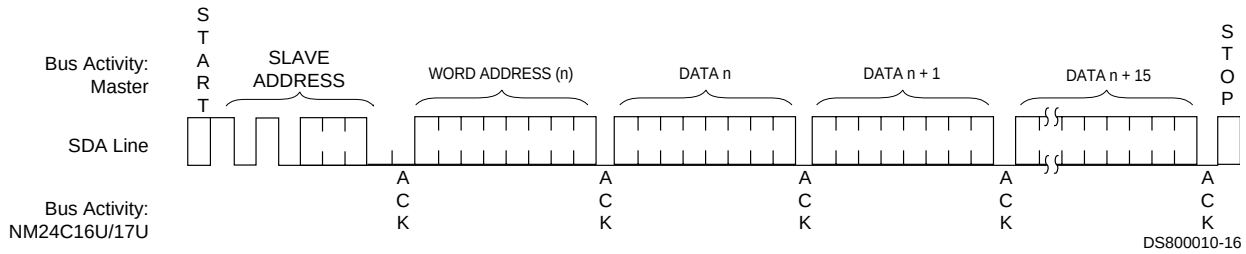
Write Protection (NM24C17U Only)

Programming of the upper half of the memory will not take place if the WP pin of the NM24C17U is connected to V_{CC}. The NM24C17U will accept slave and byte addresses; but if the memory accessed is write protected by the WP pin, the NM24C17U will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the stop condition is asserted.

Byte Write (Figure 6)



Page Write (Figure 7)



Read Operations

Read operations are initiated in the same manner as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to a one. There are three basic read operations: current address read, random read, and sequential read.

Current Address Read

Internally the NM24C16U/17U contains an address counter that maintains the address of the last byte accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ set to one, the NM24C16U/17U issues an acknowledge and transmits the eight bit byte. The master will not acknowledge the transfer but does generate a stop condition, and therefore the NM24C16U/17U discontinues transmission. Refer to *Figure* 8 for the sequence of address, acknowledge and data transfer.

Random Read

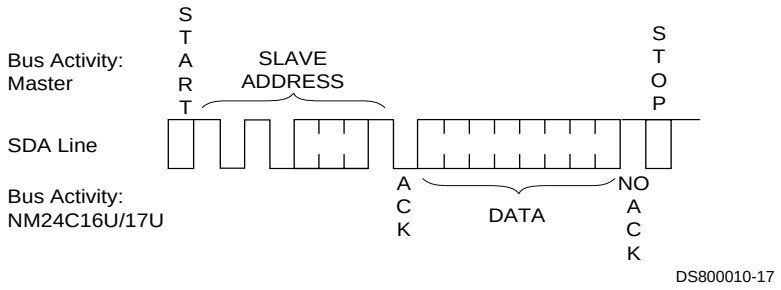
Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, slave address and then the byte address it is to read. After the byte address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the NM24C16U/17U and then by the eight bit data. The master will not acknowledge the transfer but does generate the stop condition, and therefore the NM24C16U/17U discontinues transmission. Refer to *Figure 9* for the address, acknowledge and data transfer sequence.

Sequential Read

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted in the same manner as the other read modes; however, the master now responds with an acknowledge, indicating it requires additional data. The NM24C16U/17U continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge or by generating a stop condition.

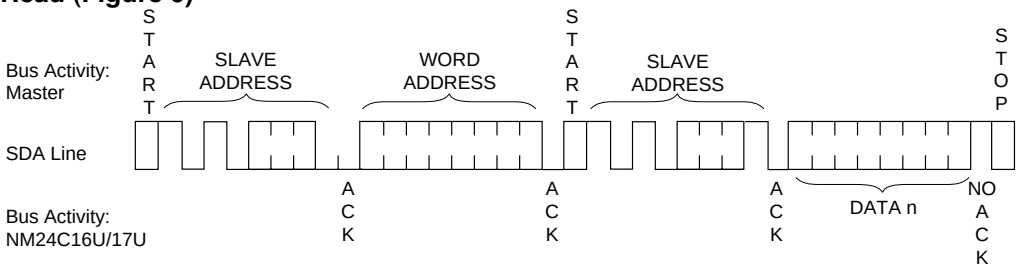
The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. After the entire memory has been read, the counter "rolls over" and the NM24C16U/17U continues to output data for each acknowledge received. Refer to *Figure 10* for the address, acknowledge, and data transfer sequence.

Current Address Read (Figure 8)



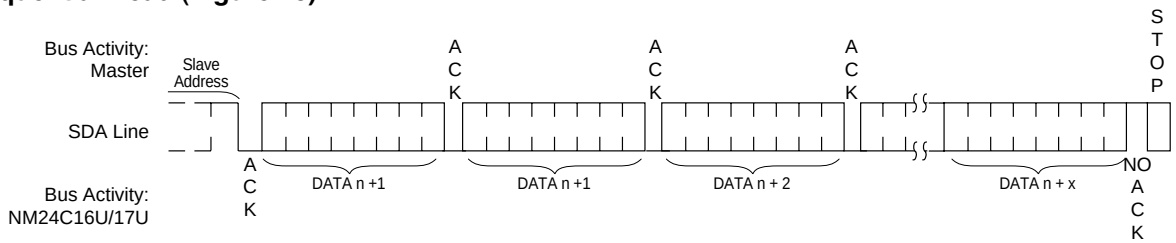
DS800010-17

Random Read (Figure 9)



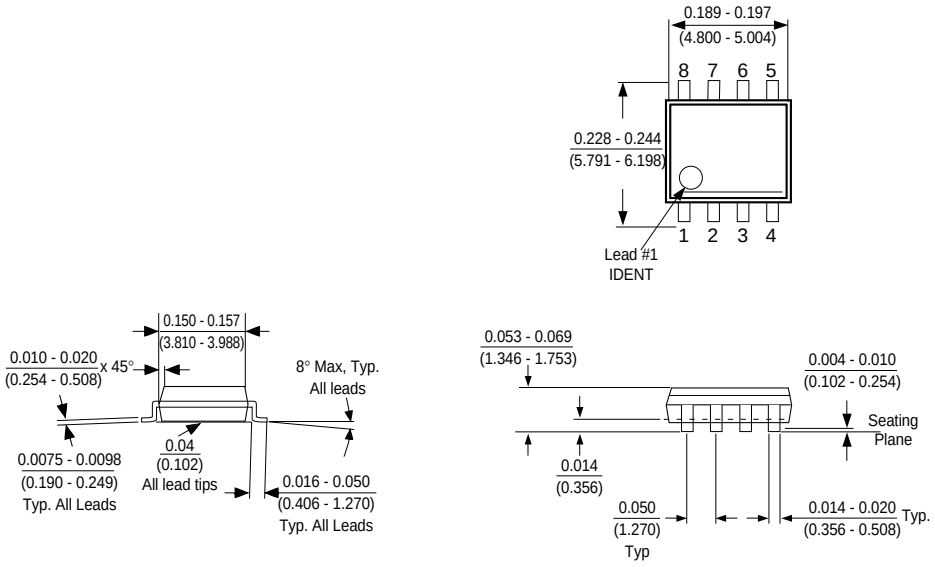
DS800010-18

Sequential Read (Figure 10)

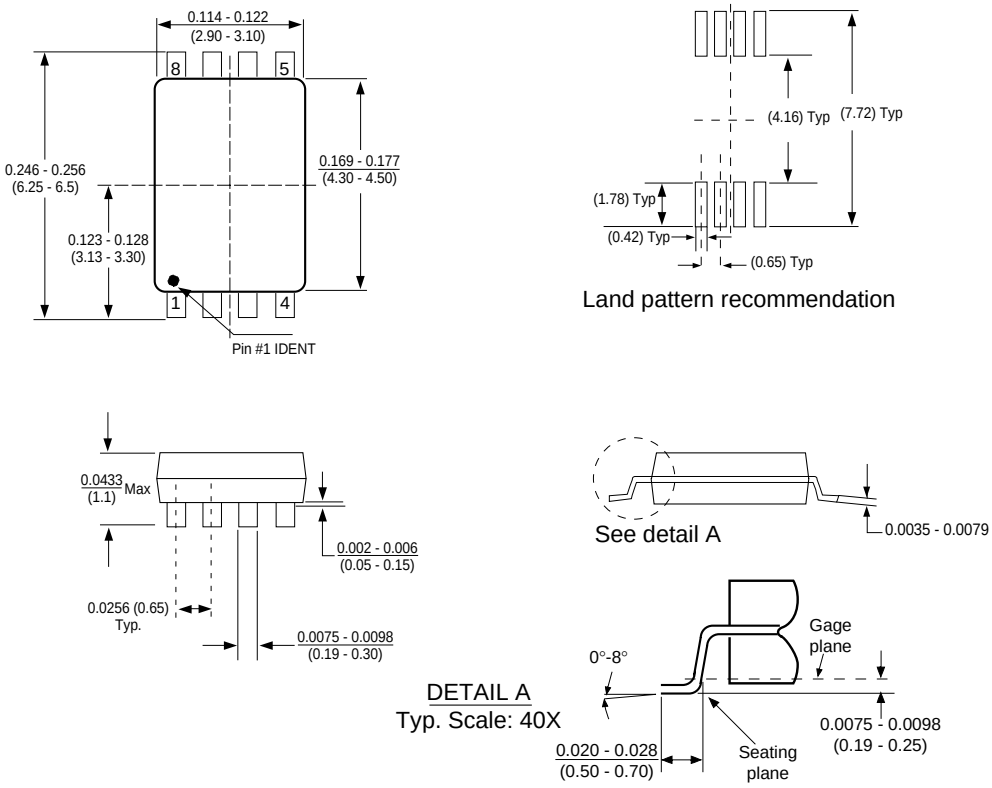


DS800010-19

Physical Dimensions inches (millimeters) unless otherwise noted



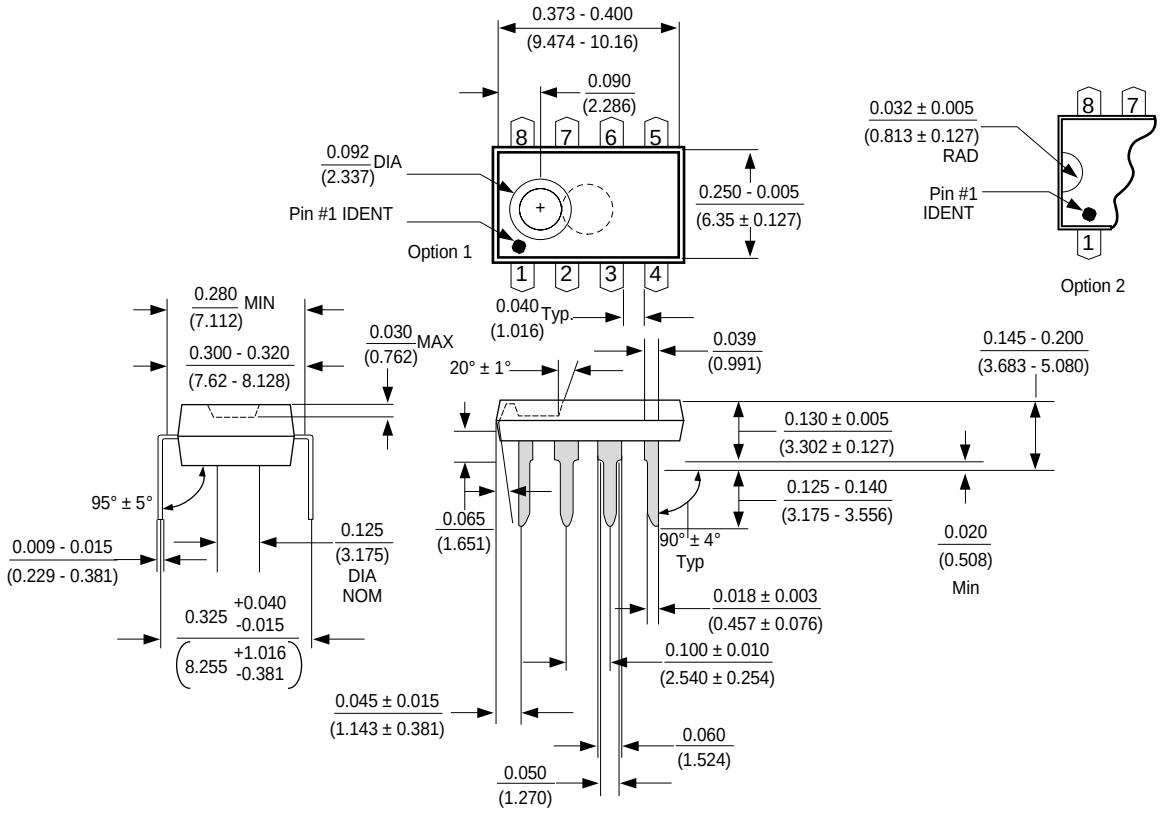
8-Pin Molded Small Outline Package (M8)
Package Number M08A



Notes: Unless otherwise specified
1. Reference JEDEC registration MO153. Variation AA. Dated 7/93

8-Pin Molded Thin Shrink Small Outline Package
Package Number MTC08

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Package Number N08E

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD
SEMICONDUCTOR™

PRELIMINARY
March 1999

NM24C32
32K-Bit Extended 2-Wire Bus Interface Serial EEPROM with Write Protect

General Description:

The NM24C32 devices are 32,768 bits of CMOS nonvolatile electrically erasable memory. These devices offer the designer different low voltage and low power options, and they conform to all specifications in the Extended IIC 2-wire protocol. Furthermore, they are designed to minimize device pin count and simplify PC board layout requirements.

The upper half of the memory can be disabled (Write Protection) by connecting the WP pin to V_{CC}. This section of memory then becomes ROM.

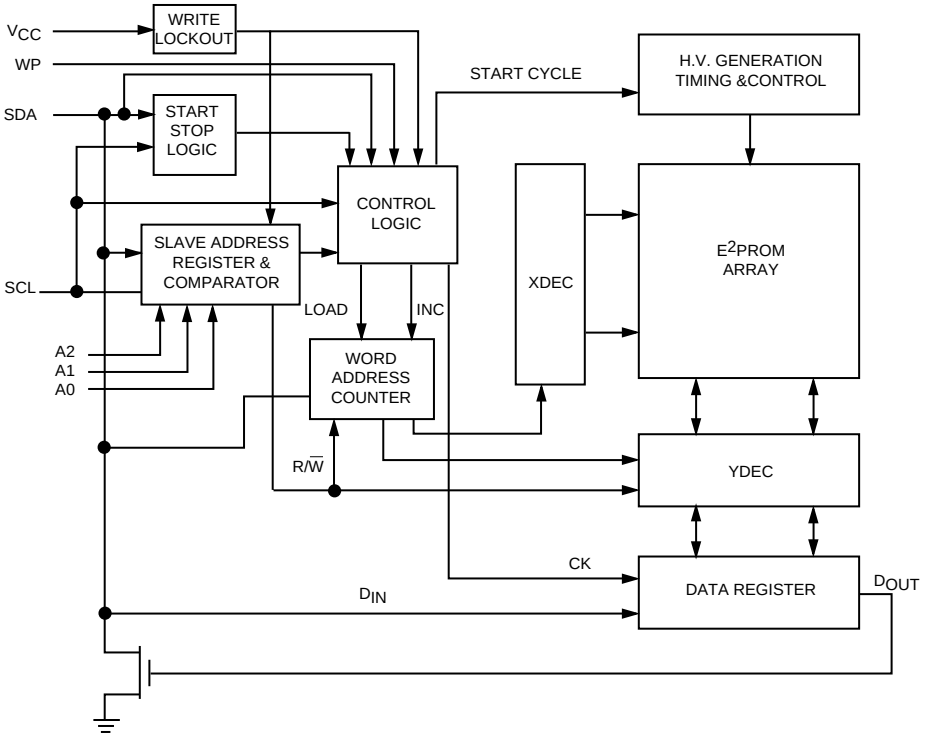
This communication protocol uses CLOCK (SCL) and DATA I/O (SDA) lines to synchronously clock data between the master (for example a microprocessor) and the slave EEPROM device(s).

Fairchild EEPROMs are designed and tested for applications requiring high endurance, high reliability, and low power consumption.

Features:

- Extended operating voltage 2.7V – 5.5V
- 400 KHz clock frequency (F) at 2.7V - 5.5V
- 200µA active current typical
  10µA standby current typical
  1µA standby typical (L)
  0.1µA standby typical (LZ)
- IIC compatible interface
  – Provides bidirectional data transfer protocol
- 32 byte page write mode
  – Minimizes total write time per byte
- Self timed write cycle
  Typical write cycle time of 6ms
- Hardware write protect for upper block
- Endurance: 1,000,000 data changes
- Data retention greater than 40 years
- Packages available: 8-pin SO, 8-pin DIP
- Low V_{CC} programming lockout (3.8V - on Standard V_{CC} devices only).

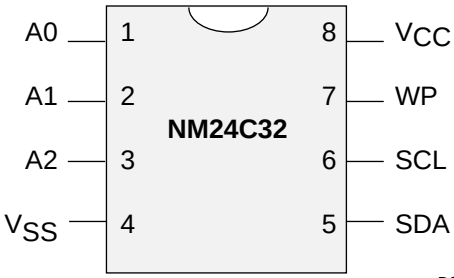
Block Diagram



DS500073-1

Connection Diagram

Dual-In-Line Package (N)
and 8-Pin SO Package (M8)



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Top View
See Package Number N08E and M08A

Pin Names

A0, A1, A2	Device Address Input
V_{SS}	Ground
SDA	Data I/O
SCL	Clock Input
WP	Write Protect
V_{CC}	Power Supply

Ordering Information

NM 24 C XX F LZ E XX

	Letter	Description
Package	N	8-Pin DIP
	M8	8-Pin SOIC
Temp. Range	None	0 to 70°C
	V	-40 to +125°C
	E	-40 to +85°C
Voltage Operating Range	Blank	4.5V to 5.5V
	L	2.7V to 4.5V
	LZ	2.7V to 4.5V and <1µA Standby Current
SCL Clock Frequency	Blank	100KHz
	F	400KHz
Density	32	32K with Write Protect
	C	CMOS
Interface	24	IIC
	NM	**Fairchild Non-Volatile Memory**

Product Specifications

Absolute Maximum Ratings

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltages with Respect to Ground	6.5V to –0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min.

Operating Conditions

Ambient Operating Temperature	
NM24C32	0°C to +70°C
NM24C32E	-40°C to +85°C
NM24C32V	-40°C to +125°C
Positive Power Supply	
NM24C32	4.5V to 5.5V
NM24C32L	2.7V to 4.5V
NM24C32LZ	2.7V to 4.5V

Standard V_{CC} (4.5V to 5.5V) DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		0.2	1.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		10	50	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	1	µA
V_{IL}	Input Low Voltage		–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Low V_{CC} (2.7V to 4.5V) DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		0.2	1.0	mA
I_{SB}	Standby Current for L	V_{IN} = GND or V_{CC}		1	10	µA
(Note 1)	Standby Current for LZ	V_{IN} = GND or V_{CC}		0.1	1	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	1	µA
V_{IL}	Input Low Voltage		–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Capacitance T_A = +25°C, f = 100/400 KHz, V_{CC} = 5V (Note 2)

Symbol	Test	Conditions	Max	Units
$C_{I/O}$	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN}	Input Capacitance (A0, A1, A2, SCL)	V_{IN} = 0V	6	pF

Note 1: Typical values are for T_A = 25°C and nominal supply voltage (5V).

Note 2: This parameter is periodically sampled and not 100% tested.

AC Conditions of Test

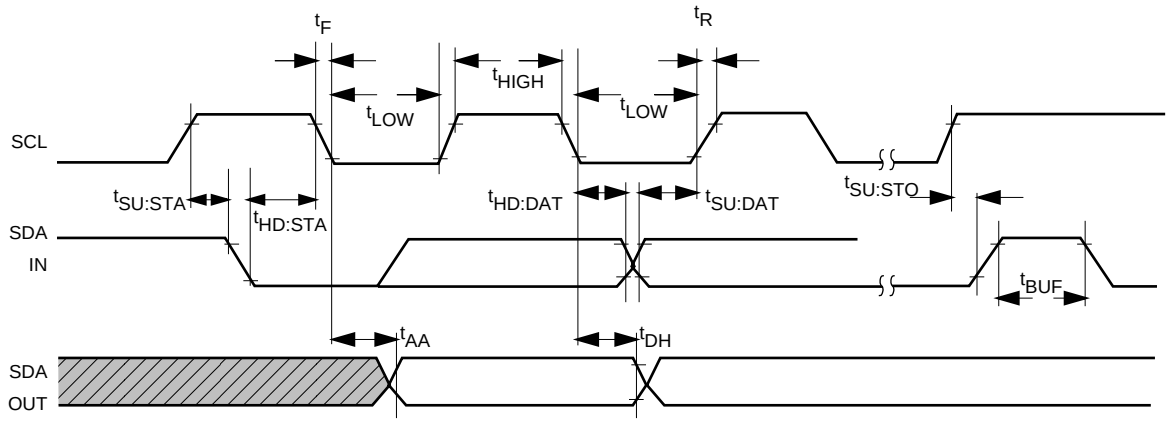
Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10 ns
Input & Output Timing Levels	V_{CC} x 0.5
Output Load	1 TTL Gate and C_L = 100 pF

Read and Write Cycle Limits (Standard and Low V_{CC} Range - 2.7V-5.5V)

Symbol	Parameter	100 KHz		400 KHz		Units
		Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		100		400	kHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs (Minimum V_{IN} Pulse width)		100		50	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	0.1	0.9	µs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		1.3		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		0.6		µs
t_{LOW}	Clock Low Period	4.7		1.5		µs
t_{HIGH}	Clock High Period	4.0		0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		µs
$t_{HD:DAT}$	Data in Hold Time	0		0		ns
$t_{SU:DAT}$	Data in Setup Time	250		100		ns
t_R	SDA and SCL Rise Time		1		0.3	µs
t_F	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		0.6		µs
t_{DH}	Data Out Hold Time	300		50		ns
t_{WR} (Note 3)	Write Cycle Time - NM24C32 - NM24C32L, NM24C32LZ		10 15		10 15	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the NM24C32 bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address

Bus Timing



DS500073-3

BACKGROUND INFORMATION (IIC Bus)

As mentioned, the IIC bus allows synchronous bidirectional communication between Transmitter/Receiver using the SCL (clock) and SDA (Data I/O) lines. All communication must be started with a valid START condition, concluded with a STOP condition and acknowledged by the Receiver with an ACKNOWLEDGE condition.

In addition, since the IIC bus is designed to support other devices such as RAM, EPROM, etc., the device type identifier string, or slave address, must follow the START condition. For EEPROMs, the first 4-bits of the slave address is '1010'. This is then followed by the device selection bits A2, A1 and A0.The final bit in the slave address determines the type of operation performed (READ/WRITE). A "1" signifies a READ while a "0" signifies a WRITE. The slave address is then followed by two bytes that define the word address, which is then followed by the data byte.

The EEPROMs on the IIC bus may be configured in any manner required, providing the total memory addressed does not exceed 4M bits in the Extended IIC protocol. EEPROM memory addressing is controlled by hardware configuring the A2, A1, and A0 pins (Device Address pins) with pull-up or pull-down resistors. ALL UNUSED PINS MUST BE GROUNDED (tied to V_{SS}).

Addressing an EEPROM memory location involves sending a command string with the following information:

[DEVICE TYPE]-[DEVICE ADDRESS]-[PAGE BLOCK ADDRESS]-[BYTE ADDRESS]

	Definitions
Word	8 bits (byte) of data
Page	32 sequential addresses (one byte each) that may be programmed during a "Page Write" programming cycle.
Master	Any IIC device CONTROLLING the transfer of data (such as a microcontroller).
Slave	Device being controlled (EEPROMS are always considered Slaves).
Transmitter	Device currently SENDING data on the bus (may be either a Master or Slave).
Receiver	Device currently receiving data on the bus (Master or Slave).

Pin Description

SERIAL CLOCK (SCL)

The SCL input is used to clock all data into and out of the device.

SERIAL DATA (SDA)

SDA is a biderectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

Device Address Inputs (A0, A1, A2)

Device address pins A0, A1, and A2 are connected to V_{CC} or V_{SS} to configure the EEPROM address for multiple device configuration. A total of eight different devices can be attached to the same SDA bus.

Write Protection (WP)

If WP is tied to V_{CC}, program WRITE operations onto the upper half of the memory will not be executed. READ operations are always available.

If WP is tied to V_{SS}, normal memory operation is enabled, READ/WRITE over the entire memory array.

This feature allows the user to assign the upper half of the memory as ROM which can be protected against accidental programming writes. When WRITE is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

Device Operation

The NM24C32xxx supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving devices as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the NM24C32xxx is considered a slave in all applications.

CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH and reserved for indicating start and stop conditions. *Refer to Figures 2 and 3.*

START CONDITION

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The NM24C32xxx continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

STOP CONDITION

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the NM24C32xxx to place the device in the standby power mode.

Write Cycle Timing

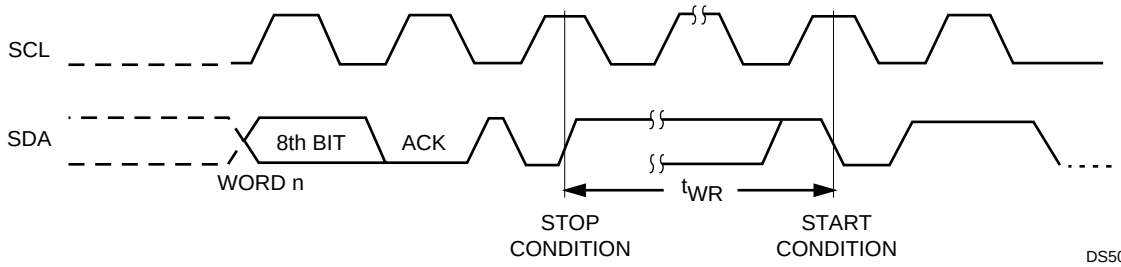
ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to *Figure 4.*

The NM24C32xxx device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the NM24C32xxx will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the READ mode the NM24C32xxx slave will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to the standby power mode.

Write Cycle Timing (Figure 1)



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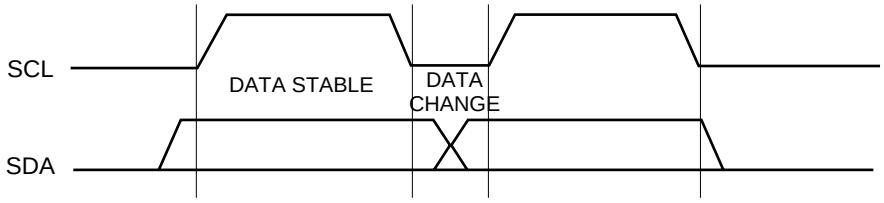
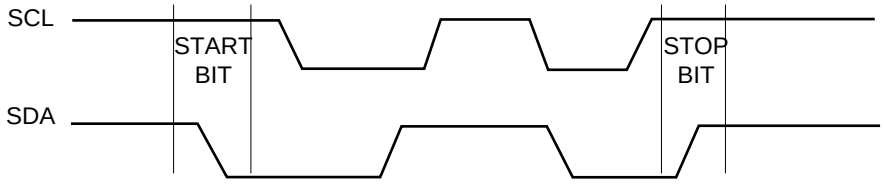
Data Validity (Figure 2)



DS500073-5

Definition of Start and Stop (Figure 3)



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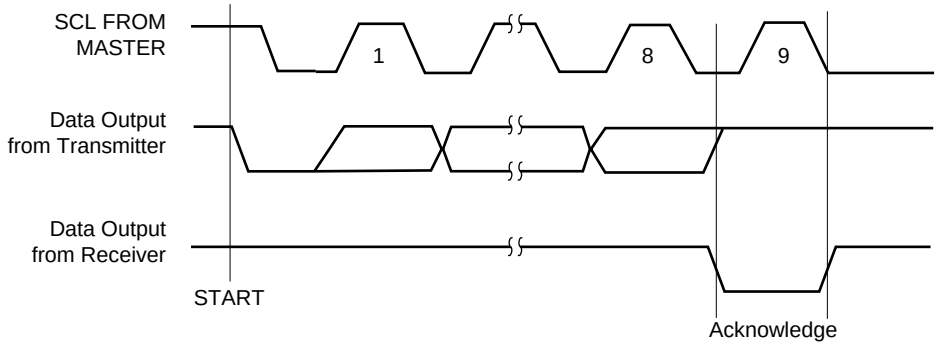
Acknowledge Response from Receiver (Figure 4)



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DEVICE ADDRESSING

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are those of the device type identifier. This is fixed as 1010 for all EEPROM devices.

The next three bits identifies the device address. Address from 000 to 111 are acceptable thus allowing up to eight devices to be connected to the IIC bus.

The last bit of the slave address defines whether a write or read condition is requested by the master. A "1" indicates that a READ operation is to be executed and a "0" initiates the WRITE mode.

A simple review: After the NM24C32xxx recognizes the start condition, the devices interfaced to the IIC bus waits for a slave address to be transmitted over the SDA line. If the transitted slave address matches an address of one of the devices, the designated slave pulls the line LOW with an acknowledge. signal and awaits further transmissions.

Write Operations

BYTE WRITE

For a WRITE operation, two additional address bytes, with 12 active bits, are required after the SLAVE acknowledge to address the full memory array. The first byte indicates the high-order byte of the word address. Only the four least signicant bits can be changed, the other bits are pre-assigned the value "0". Following the acknowledgement from the first word address, the next byte indicates the low-order byte of the word address. Upon receipt of the word address, the NM24C32xxx responds with another acknowledge and waits for the next eight bits of data, again, responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the NM24C32xxx begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress, the device's inputs are disabled and the device will not respond to any requests from the master. Refer to *Figure 5* for the address, acknowledge and data transfer sequence.

PAGE WRITE

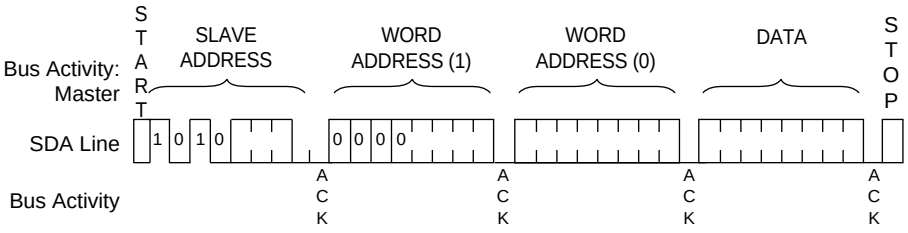
The NM24C32xxx is capable of thirty-two byte page write operation. It is initiated in the same manner as the byte write operation; but instead of termination the write cycle after the first data word is transfered, the master can transmit up to thirty-one more words. After the receipt of each word, the device responds with an acknowledge.

After the receipt of each word, the internal address counter increments to the next address and the next SDA data is accepted. If the master should transmit more than thirty-two words prior to generating the stop condition, the address counter will "roll over" and the previous written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to *Figure 6* for the address, acknowledge and data transfer sequence.

Acknowledge Polling

Once the stop condition is isssued to indicate the end of the host's write operation, the NM24C32xxx initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the NM24C32xxx is still busy with the write operation, no ACK will be returned. If the device has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

Byte Write (Figure 5)



DS500073-8

Write Protection

Programming of the upper half of memory will not take place if the WP pin is connected to V_{CC}. The device will accept slave and word addresses; but if the memory accessed is write protected by the WP pin, the NM24C32xxx will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the stop condition is asserted.

Low V_{CC} Lockout

NM24C32xxx provides data security against inadvertent writes that could potentially happen during the time the device is being powered on, powered down and brown out conditions by monitoring the V_{CC} voltage during a write cycle. Whenever a write cycle is started, the built-in circuitry starts to monitor the V_{CC} level throughout the duration of the write command sequence until the master issues the required STOP condition to start the actual internal write operation. If the sensed V_{CC} voltage is below 3.8V at any point during this monitoring period, the device prohibits the write operation and does not generate the ACK pulse. This low V_{CC} lockout feature is only available for standard 5V device.

Read Operation

Read operations are initiated in the same manner as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to "1". There are three basic read operations: current address read, random read and sequential read.

CURRENT ADDRESS READ

Internally the NM24C32xxx contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n+1. Upon receipt of the slave address with R/$\overline{W}$ set to one, the NM24C32xxx issues an acknowledge and transmits the eight bit word. The master will not acknowledge acknowledge the transfer but does generate a stop condition, and therefore discontinues transmission. Refer to *Figure 7* for the sequence of address, acknowledge and data transfer.

RANDOM READ

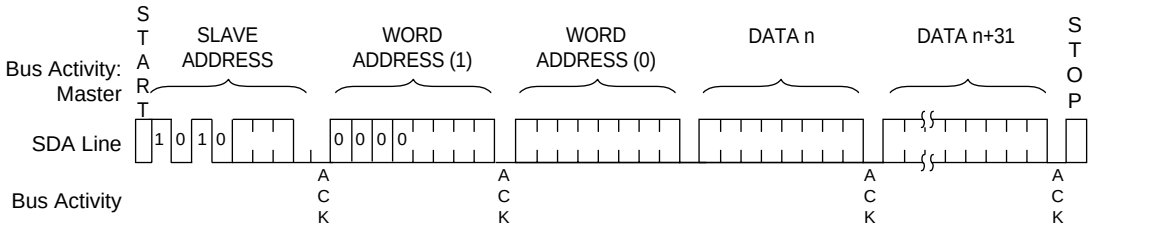
Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to "1", the master must first perform a "dummy" write operation. The master issues a start condition, slave address and then the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to "1". This will be followed by an acknowledge from the NM24C32xxx and then by the eight bit word. The master will not acknowledge the transfer but does generate the stop condition, and therefore the NM24C32xxx discontinues transmission. Refer to *Figure 8* for the address, acknowledge and data transfer sequence.

SEQUENTIAL READ

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted in the same manner as the other read modes; however, the master now responds with an acknowledge, indicating it requires additional data. The NM24C32xxx continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge or by generating a stop condition.

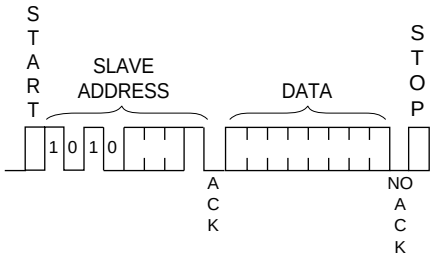
The data output is sequential, with the data from address n followed by the data n+1. The address counter for read operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. After the entire memory has been read, the counter "rolls over" and the NM24C32xxx continues to output data for each acknowledge received. Refer to *Figure 9* for the address, acknowledge and data transfer sequence.

Page Write (Figure 6)



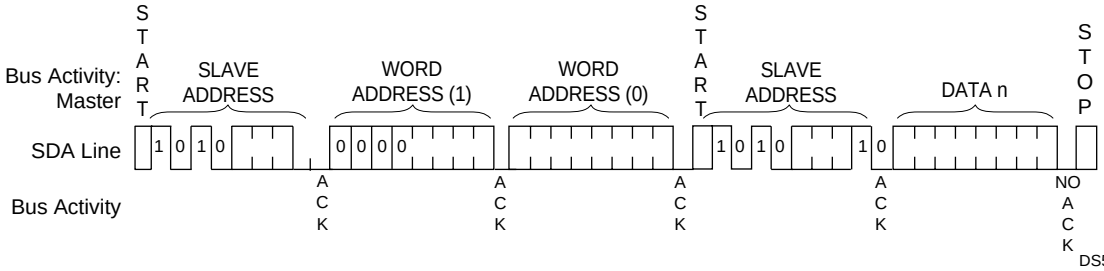
DS500073-9

Current Address Read (Figure 7)



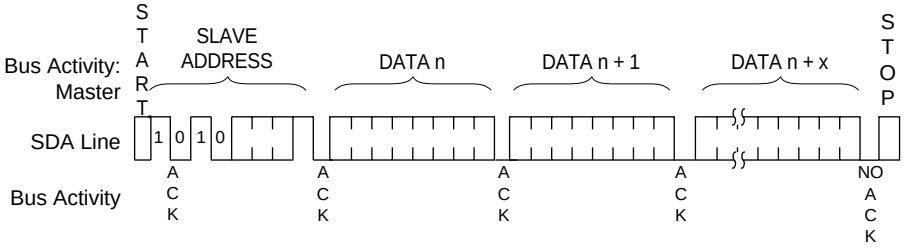
DS500073-10

Random Read (Figure 8)



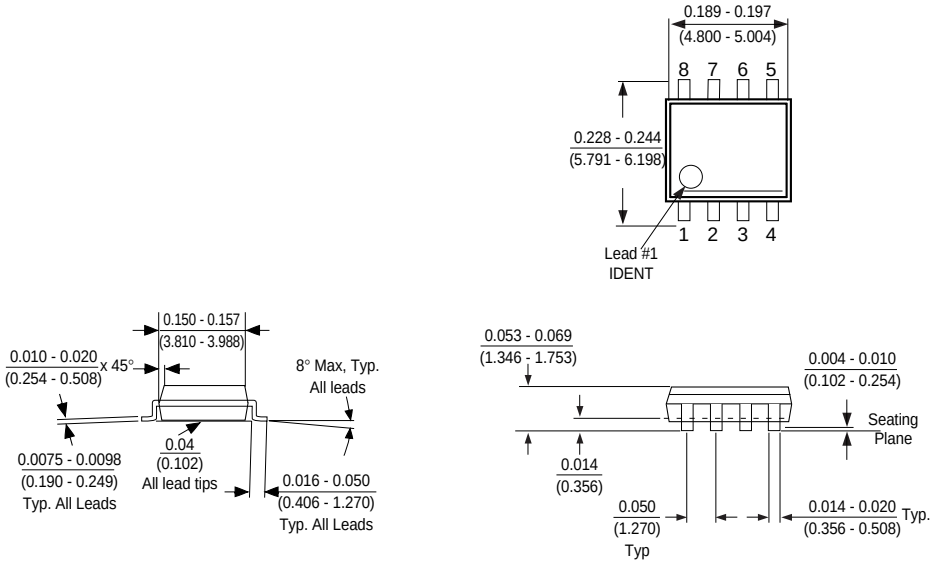
DS500073-11

Sequential Read (Figure 9)



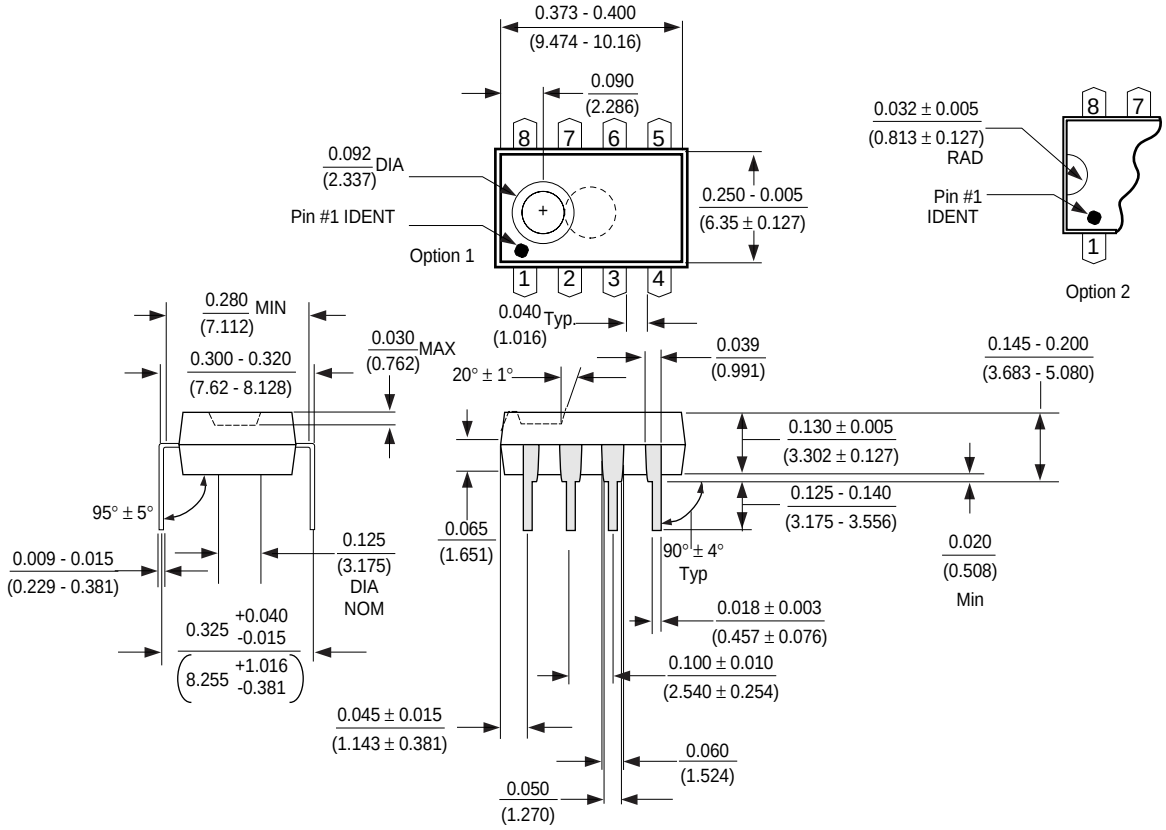
DS500073-12

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Small Out-Line Package (M8)
Order Number NM24C32xxxM8 or NM24C32xxxEM8
Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Order Number NM24C32xxxN or NM24C32xxxEN
Package Number N08E

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

PRELIMINARY

August 1999

NM24C32U
32K-Bit Serial EEPROM with Write Protect 2-Wire Bus Interface

General Description:

The NM24C32U is a 32K (32,768) bit serial interface CMOS EEPROM (Electrically Erasable Programmable Read-Only Memory). This device fully conforms to the **Extended** I²C™ 2-wire protocol which uses Clock (SCL) and Data I/O (SDA) pins to synchronously clock data between the "master" (for example a microprocessor) and the "slave" (the EEPROM device). In addition, the serial interface allows a minimal pin count packaging designed to simplify PC board layout requirements and offers the designer a variety of low voltage and low power options.

NM24C32U incorporates a hardware "Write Protect" feature, by which, the upper half of the memory can be disabled against programming by connecting the WP pin to V_{CC}. This section of memory then effectively becomes a ROM (Read-Only Memory) and can no longer be programmed as long as WP pin is connected to V_{CC}.

Fairchild EEPROMs are designed and tested for applications requiring high endurance, high reliability and low power consumption for a continuously reliable non-volatile solution for all markets.

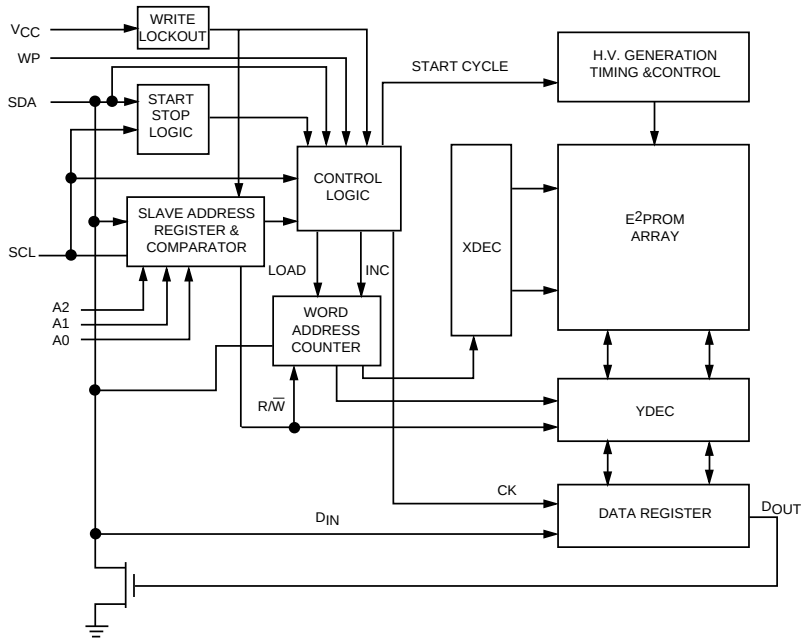
Functions

- I²C™ compatible interface
- 32,768 bits organized as 4,096 x 8
- Extended 2.7V – 5.5V operating voltage
- 100 KHz or 400 KHz operation
- Self timed programming cycle (6ms typical)
- "Programming complete" indicated by ACK polling
- Memory "Upper Block" Write Protect pin

Features

- The I²C™ interface allows the smallest I/O pincount of any EEPROM interface
- 32 byte page write mode to minimize total write time per byte
- Low V_{CC} programming lockout (3.8V)
  — **"H" option (Standard V_{CC} range) parts only**
- Typical 200µA active current (I_{CCA})
- Typical 1µA standby current (I_{SB}) for "L" devices and 0.1µA standby current for "LZ" devices
- Endurance: Up to 1,000,000 data changes
- Data retention greater than 40 years

Block Diagram

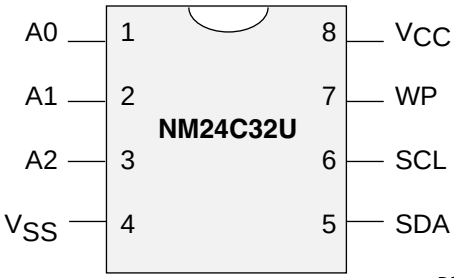


I²C™ is a registered trademark of Philips Electronics N.V.

DS800011-1

Connection Diagram

Dual-In-Line Package (N)
and 8-Pin SO Package (M8)



DS800011-2

Top View
See Package Number N08E and M08A

Pin Names

A0, A1, A2	Device Address Input
V_{SS}	Ground
SDA	Data I/O
SCL	Clock Input
WP	Write Protect
V_{CC}	Power Supply

Ordering Information

NM 24 C XX U F LZ E XX

	Letter	Description
Package	N	8-Pin DIP
	M8	8-Pin SOIC
Temp. Range	None	0 to 70°C
	V	-40 to +125°C
	E	-40 to +85°C
Voltage Operating Range	Blank	4.5V to 5.5V
	L	2.7V to 5.5V
	LZ	2.7V to 5.5V and <1µA Standby Current
	H	4.5V to 5.5V and V_{CC} Lockout
SCL Clock Frequency	Blank	100KHz
	F	400KHz
	Ultralite	CS100UL Process
Density	32	32K with Write Protect
	C	CMOS
Interface	24	IIC
NM	**NM**	**Fairchild Non-Volatile Memory**

Product Specifications

Absolute Maximum Ratings

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltages with Respect to Ground	6.5V to –0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min.

Operating Conditions

Ambient Operating Temperature	
NM24C32U	0°C to +70°C
NM24C32UE	-40°C to +85°C
NM24C32UV	-40°C to +125°C
Positive Power Supply	
NM24C32U/NM24C32UH	4.5V to 5.5V
NM24C32UL	2.7V to 5.5V
NM24C32ULZ	2.7V to 5.5V

Standard V_{CC} (4.5V to 5.5V) DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 400 KHz f_{SCL} = 100 KHz		0.2	1.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		10	50	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	1	µA
V_{IL}	Input Low Voltage		–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Low V_{CC} (2.7V to 5 .5V) DC Electrical Characteristics

Symbol	Parameter	Test Conditions		Limits			Units
				Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 400 KHz f_{SCL} = 100 KHz			0.2	1.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}	V_{CC} = 2.7V - 4.5V V_{CC} = 2.7V - 4.5V V_{CC} = 4.5V - 5.5V		1 0.1 10	10 1 50	µA µA µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}			0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}			0.1	1	µA
V_{IL}	Input Low Voltage			–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA				0.4	V

Capacitance T_A = +25°C, f = 100/400 KHz, V_{CC} = 5V (Note 2)

Symbol	Test	Conditions	Max	Units
$C_{I/O}$	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN}	Input Capacitance (A0, A1, A2, SCL)	V_{IN} = 0V	6	pF

Note 1: Typical values are T_A = 25°C and nominal supply voltage (5V).

Note 2: This parameter is periodically sampled and not 100% tested.

AC Conditions of Test

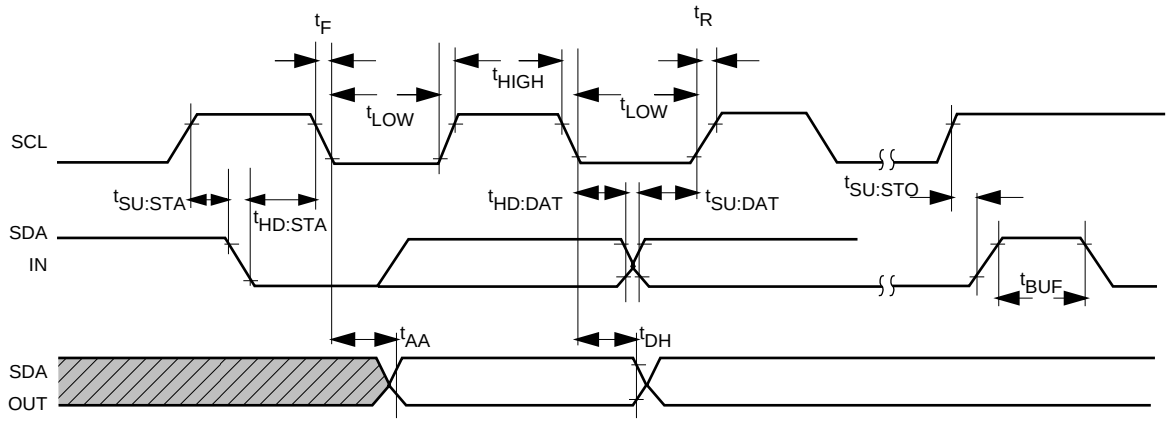
Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10 ns
Input & Output Timing Levels	V_{CC} x 0.5
Output Load	1 TTL Gate and C_L = 100 pF

Read and Write Cycle Limits (Standard and Low V_{CC} Range - 2.7V-5.5V)

Symbol	Parameter	100 KHz		400 KHz		Units
		Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		100		400	kHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs (Minimum V_{IN} Pulse width)		100		50	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	0.1	0.9	µs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		1.3		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		0.6		µs
t_{LOW}	Clock Low Period	4.7		1.5		µs
t_{HIGH}	Clock High Period	4.0		0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		µs
$t_{HD:DAT}$	Data in Hold Time	0		0		µs
$t_{SU:DAT}$	Data in Setup Time	250		100		ns
t_R	SDA and SCL Rise Time		1		0.3	µs
t_F	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		0.6		µs
t_{DH}	Data Out Hold Time	300		50		ns
t_{WR} (Note 3)	Write Cycle Time - NM24C32U - NM24C32UL, NM24C32ULZ		10 15		10 15	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the NM24C32U bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address

Bus Timing



DS800011-3

BACKGROUND INFORMATION (IIC Bus)

As mentioned, the IIC bus allows synchronous bidirectional communication between Transmitter/Receiver using the SCL (clock) and SDA (Data I/O) lines. All communication must be started with a valid START condition, concluded with a STOP condition and acknowledged by the Receiver with an ACKNOWLEDGE condition.

In addition, since the IIC bus is designed to support other devices such as RAM, EPROM, etc., the device type identifier string, or slave address, must follow the START condition. For EEPROMs, the first 4-bits of the slave address is '1010'. This is then followed by the device selection bits A2, A1 and A0.The final bit in the slave address determines the type of operation performed (READ/WRITE). A "1" signifies a READ while a "0" signifies a WRITE. The slave address is then followed by two bytes that define the word address, which is then followed by the data byte.

The EEPROMs on the IIC bus may be configured in any manner required, providing the total memory addressed does not exceed 4M bits in the Extended IIC protocol. EEPROM memory addressing is controlled by hardware configuring the A2, A1, and A0 pins (Device Address pins) with pull-up or pull-down resistors. ALL UNUSED PINS MUST BE GROUNDED (tied to V_{SS}).

Addressing an EEPROM memory location involves sending a command string with the following information:

[DEVICE TYPE]-[DEVICE ADDRESS]-[PAGE BLOCK ADDRESS]-[BYTE ADDRESS]

	Definitions
Word	8 bits (byte) of data
Page	32 sequential addresses (one byte each) that may be programmed during a "Page Write" programming cycle.
Master	Any IIC device CONTROLLING the transfer of data (such as a microcontroller).
Slave	Device being controlled (EEPROMS are always considered Slaves).
Transmitter	Device currently SENDING data on the bus (may be either a Master or Slave).
Receiver	Device currently RECEIVING data on the bus (Master or Slave).

Pin Description

SERIAL CLOCK (SCL)

The SCL input is used to clock all data into and out of the device.

SERIAL DATA (SDA)

SDA is a biderectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

Device Address Inputs (A0, A1, A2)

Device address pins A0, A1, and A2 are connected to V_{CC} or V_{SS} to configure the EEPROM address for multiple device configuration. A total of eight different devices can be attached to the same SDA bus.

Write Protection (WP)

If WP is tied to V_{CC}, program WRITE operations onto the upper half of the memory will not be executed. READ operations are always available.

If WP is tied to V_{SS}, normal memory operation is enabled, READ/WRITE over the entire memory array.

This feature allows the user to assign the upper half of the memory as ROM which can be protected against accidental programming writes. When WRITE is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

Device Operation

The NM24C32Uxxx supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving devices as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the NM24C32Uxxx is considered a slave in all applications.

CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH and reserved for indicating start and stop conditions. *Refer to Figures 2 and 3.*

START CONDITION

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The NM24C32Uxxx continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

STOP CONDITION

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the NM24C32Uxxx to place the device in the standby power mode.

Write Cycle Timing

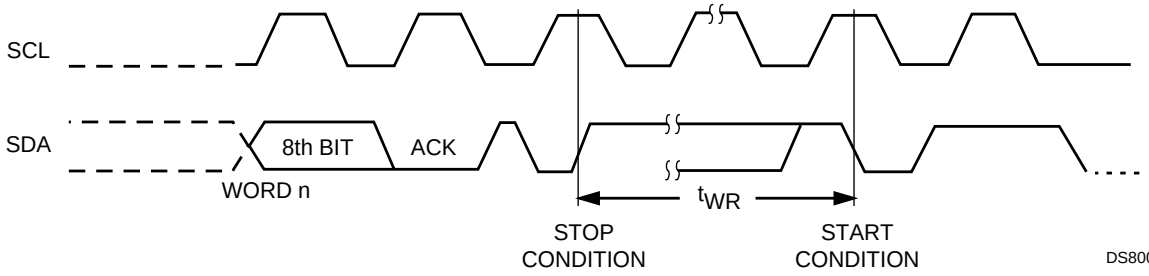
ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to *Figure 4.*

The NM24C32Uxxx device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the NM24C32Uxxx will respond with an acknowledge after the receipt of each subsequent eight bit word.

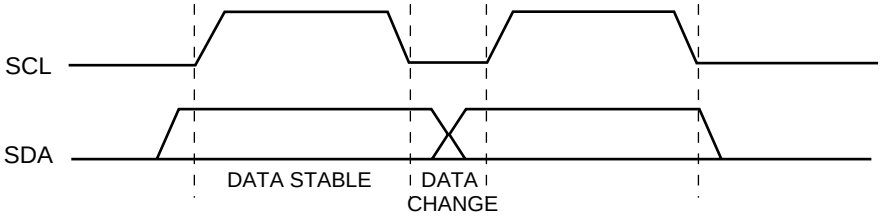
In the READ mode the NM24C32Uxxx slave will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to the standby power mode.

Write Cycle Timing (Figure 1)



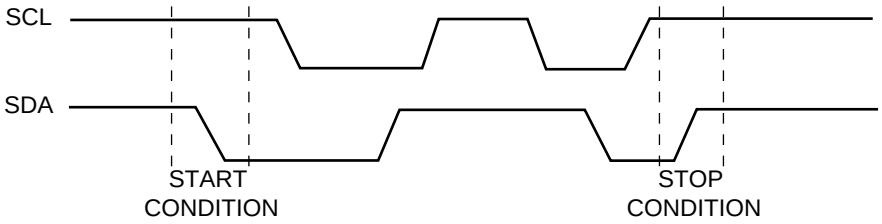
DS800011-4

Data Validity (Figure 2)



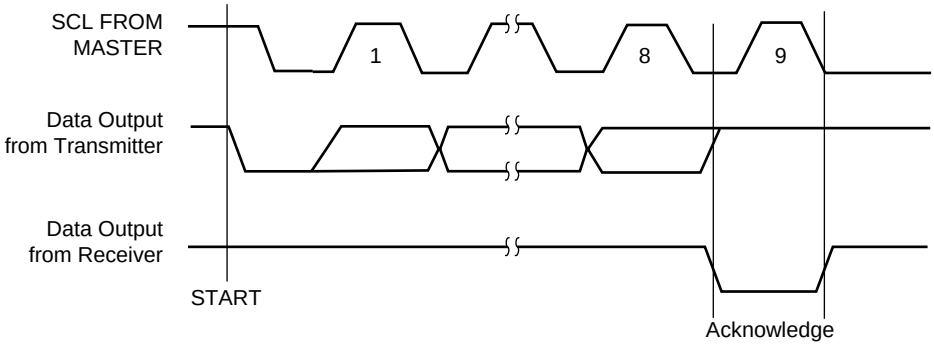
DS800011-5

Definition of Start and Stop (Figure 3)



DS800011-6

Acknowledge Response from Receiver (Figure 4)



DS800011-7

DEVICE ADDRESSING

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are those of the device type identifier. This is fixed as 1010 for all EEPROM devices.

The next three bits identifies the device address. Address from 000 to 111 are acceptable thus allowing up to eight devices to be connected to the IIC bus.

The last bit of the slave address defines whether a write or read condition is requested by the master. A "1" indicates that a READ operation is to be executed and a "0" initiates the WRITE mode.

A simple review: After the NM24C32Uxxx recognizes the start condition, the devices interfaced to the IIC bus wait for a slave address to be transmitted over the SDA line. If the transitted slave address matches an address of one of the devices, the designated slave pulls the line LOW with an acknowledge signal and awaits further transmissions.

Write Operations

BYTE WRITE

For a WRITE operation, two additional address bytes, with 12 active bits, are required after the SLAVE acknowledge to address the full memory array. The first byte indicates the high-order byte of the word address. Only the four least signicant bits can be changed, the other bits are pre-assigned the value "0". Following the acknowledgement from the first word address, the next byte indicates the low-order byte of the word address. Upon receipt of the word address, the NM24C32Uxxx responds with another acknowledge and waits for the next eight bits of data, again, responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the NM24C32Uxxx begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress, the device's inputs are disabled and the device will not respond to any requests from the master. Refer *Figure 5* for the Byte Write sequence.

PAGE WRITE

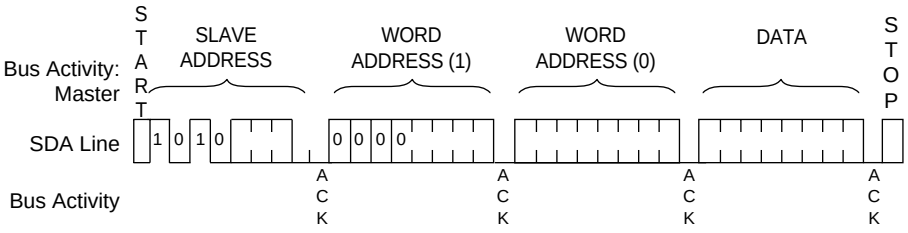
The NM24C32Uxxx is capable of thirty-two byte page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data word is transfered, the master can transmit up to thirty-one more words. After the receipt of each word, the device responds with an acknowledge.

After the receipt of each word, the internal address counter increments to the next address and the next SDA data is accepted. If the master should transmit more than thirty-two words prior to generating the stop condition, the address counter will "roll over" and the previous written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer *Figure 6* for the Page Write sequence.

Acknowledge Polling

Once the stop condition is isssued to indicate the end of the host's write operation, the NM24C32Uxxx initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the NM24C32Uxxx is still busy with the write operation, no ACK will be returned. If the device has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

Byte Write (Figure 5)



DS800011-8

Write Protection

Programming of the upper half of memory will not take place if the WP pin is connected to V_{CC}. The device will accept slave and word addresses; but if the memory accessed is write protected by the WP pin, the NM24C32Uxxx will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the stop condition is asserted.

Low V_{CC} Lockout

NM24C32UxHx (H option) protects against data corruption during programming by preventing any programming operations if V_{CC} drops below approximately 3.8V (V_{CC} Lockout trip level). This is accomplished by monitoring the "READ/WRITE" (R/$\overline{W}$) bit in the SLAVE address and if the R/W bit is "0," indicating a programming operation, the V_{CC} Lockout is activated. At that point, if the V_{CC} drops below the trip level, programming is inhibited and the device does not issue an ACK (the output stays high). To restate, the V_{CC} Lockout feature is active from the time a WRITE bit is received up to the time that the Master's STOP condition is received (the STOP condition turns on the V_{PP} internal high voltage). **Once programming has begun, the programming cycle cannot be interrupted except by removal of V_{CC}, which could result in data corruption.**

Read Operation

Read operations are initiated in the same manner as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to "1". There are three basic read operations: current address read, random read and sequential read.

CURRENT ADDRESS READ

Internally the NM24C32Uxxx contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n+1. Upon receipt of the slave address with R/$\overline{W}$ set to one, the NM24C32Uxxx issues an acknowledge and transmits the eight bit word. The master will not acknowledge the transfer but does generate a stop condition, and therefore discontinues transmission. Refer *Figure 7* for the Current Address Read sequence.

RANDOM READ

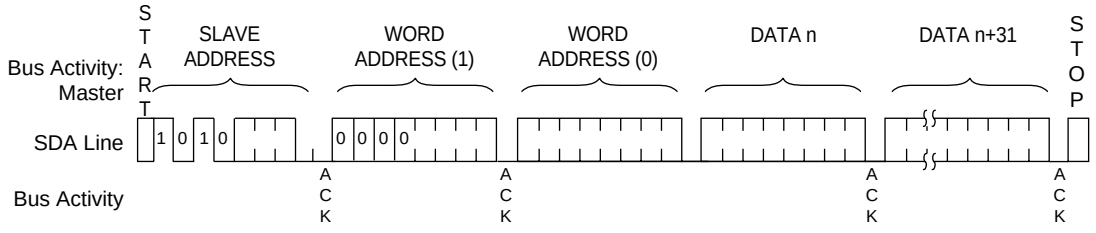
Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to "1", the master must first perform a "dummy" write operation. The master issues a start condition, slave address with the R/$\overline{W}$ bit set to "0" and then the word address it is to read from. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to "1". This will be followed by an acknowledge from the NM24C32Uxxx and then by the eight bit data. The master will not acknowledge the transfer but does generate the stop condition, and therefore the NM24C32Uxxx discontinues transmission. Refer *Figure 8* for the Random Read sequence.

SEQUENTIAL READ

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted in the same manner as the other read modes; however, the master now responds with an acknowledge, indicating it requires additional data. The NM24C32Uxxx continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge or by generating a stop condition.

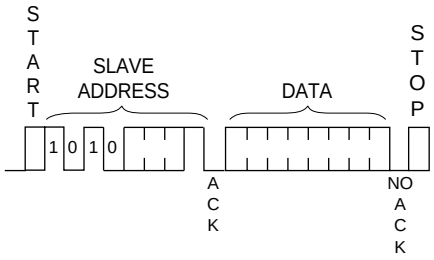
The data output is sequential, with the data from address n followed by the data n+1. The address counter for read operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. After the entire memory has been read, the counter "rolls over" and the NM24C32Uxxx continues to output data for each acknowledge received. Refer *Figure 9* for the Sequential Read sequence.

Page Write (Figure 6)



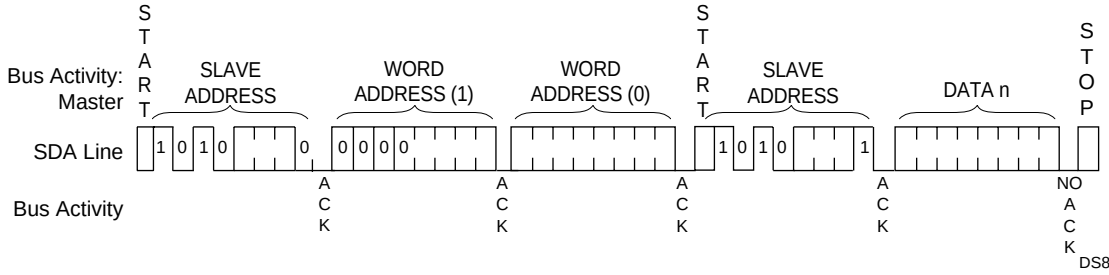
DS800011-9

Current Address Read (Figure 7)



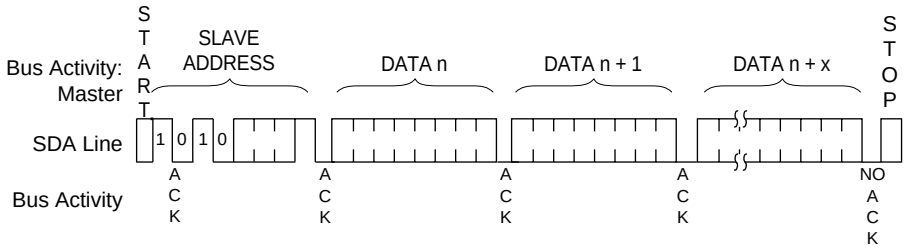
DS800011-10

Random Read (Figure 8)



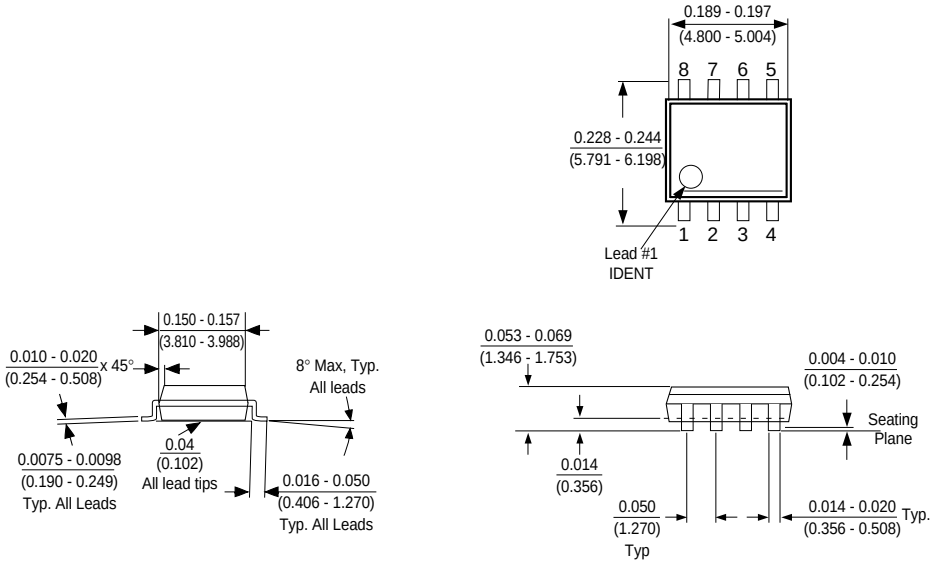
DS800011-11

Sequential Read (Figure 9)



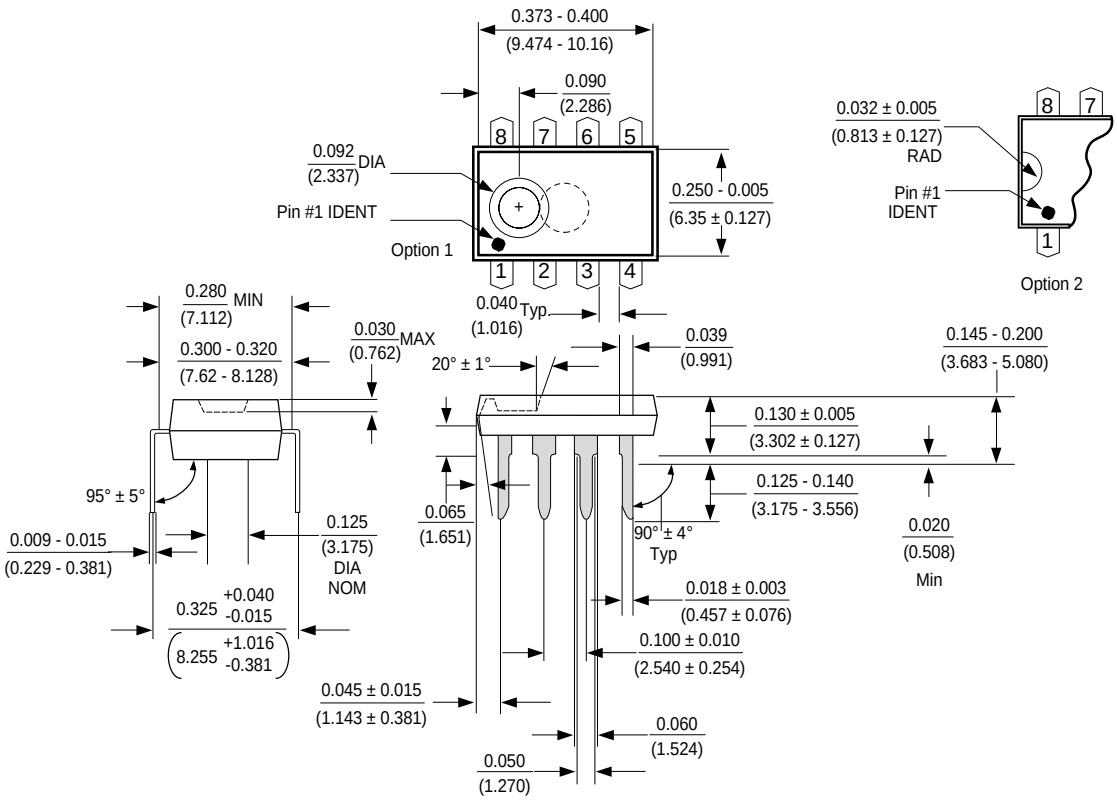
DS800011-12

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Small Out-Line Package (M8)
Order Number NM24C32UxxxM8 or NM24C32UxxxEM8
Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Order Number NM24C32UxxxN or NM24C32UxxxEN
Package Number N08E

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD
SEMICONDUCTOR™

PRELIMINARY
March 1999

NM24C65
64K-Bit Extended 2-Wire Bus Interface Serial EEPROM with Write Protect

General Description:

The NM24C65 devices are 65,536 bits of CMOS nonvolatile electrically erasable memory. These devices offer the designer different low voltage and low power options, and they conform to all in the Extended IIC 2-wire protocol. Furthermore, they are designed to minimize device pin count and simplify PC board layout requirements.

The upper half of the memory can be disabled (Write Protection) by connecting the WP pin to V_{CC}. This section of memory then becomes ROM.

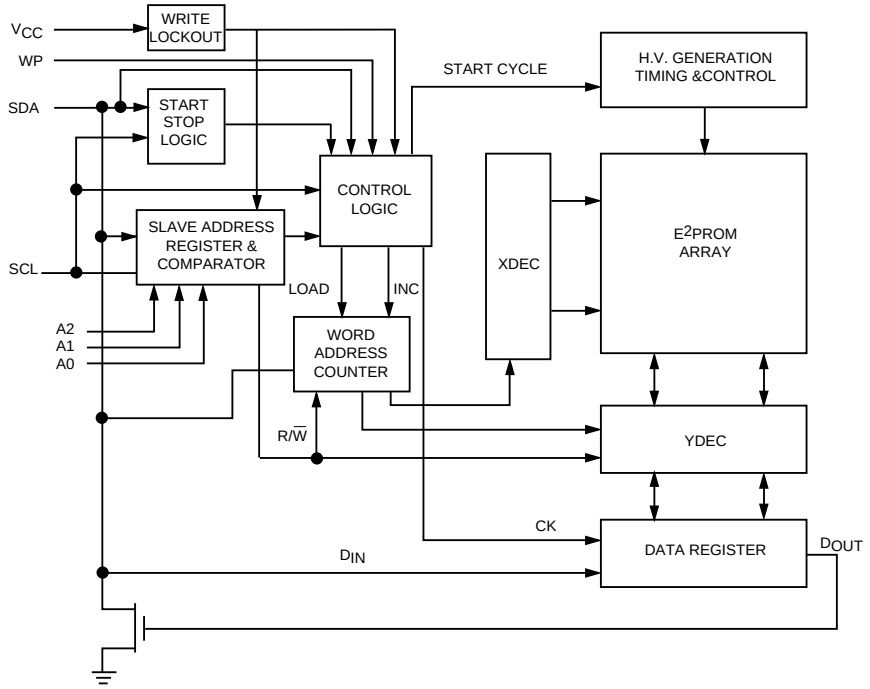
This communication protocol uses CLOCK (SCL) and DATA I/O (SDA) lines to synchronously clock data between the master (for example a microprocessor) and the slave EEPROM device(s).

Fairchild EEPROMs are designed and tested for applications requiring high endurance, high reliability, and low power consumption.

Features:

- Extended operating voltage 2.7V – 5.5V
- 400 KHz clock frequency (F) at 2.7V - 5.5V
- 200µA active current typical
  10µA standby current typical
  1µA standby typical (L)
  0.1µA standby typical (LZ)
- IIC compatible interface
  – Provides bidirectional data transfer protocol
- 32 byte page write mode
  – Minimizes total write time per byte
- Self timed write cycle
  Typical write cycle time of 6ms
- Hardware write protect for upper block
- Endurance: 1,000,000 data changes
- Data retention greater than 40 years
- Packages available: 8-pin SO, 8-pin DIP
- Low V_{CC} programming lockout (3.8V - on Standard V_{CC} devices only).

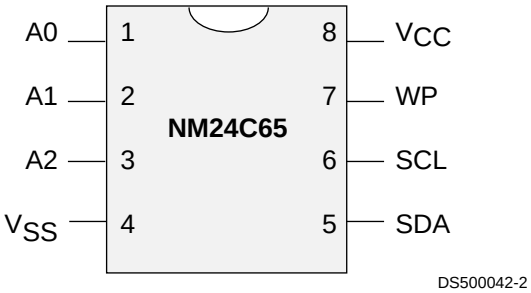
Block Diagram



DS500042-1

Connection Diagram

Dual-In-Line Package (N)
and 8-Pin SO Package (M8)



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Top View
See Package Number N08E and M08A

Pin Names

A0, A1, A2	Device Address Input
V_{SS}	Ground
SDA	Data I/O
SCL	Clock Input
WP	Write Protect
V_{CC}	Power Supply

Ordering Information

								Letter	Description
							Package	N	8-pin DIP
								M8	8-pin SO8
						Temp. Range		None	0 to 70°C
								V	-40 to +125°C
								E	-40 to +85°C
					Voltage Operating Range			Blank	4.5V to 5.5V
								L	2.7V to 4.5V
								LZ	2.7V to 4.5V and <1µA Standby Current
				SCL Clock Frequency				Blank	100KHz
								F	400KHz
			Density					65	64K with Write Protect
		C						C	CMOS
	Interface							24	IIC
NM								**NM**	**Fairchild Non-Volatile Memory**

Product Specifications

Absolute Maximum Ratings

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltages with Respect to Ground	6.5V to –0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min.

Operating Conditions

Ambient Operating Temperature	
NM24C65	0°C to +70°C
NM24C65E	-40°C to +85°C
NM24C65V	-40°C to +125°C
Positive Power Supply	
NM24C65	4.5V to 5.5V
NM24C65L	2.7V to 4.5V
NM24C65LZ	2.7V to 4.5V

Standard V_{CC} (4.5V to 5.5V) DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 KHz		0.2	1.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		10	50	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	1	µA
V_{IL}	Input Low Voltage		–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Low V_{CC} (2.7V to 4.5V) DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		0.2	1.0	mA
I_{SB}	Standby Current for L	V_{IN} = GND or V_{CC}		1	10	µA
(Note 1)	Standby Current for LZ	V_{IN} = GND or V_{CC}		0.1	1	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	1	µA
V_{IL}	Input Low Voltage		–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Capacitance T_A = +25°C, f = 100/400 KHz, V_{CC} = 5V (Note 2)

Symbol	Test	Conditions	Max	Units
$C_{I/O}$	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN}	Input Capacitance (A0, A1, A2, SCL)	V_{IN} = 0V	6	pF

Note 1: Typical values are for T_A = 25°C and nominal supply voltage (5V).

Note 2: This parameter is periodically sampled and not 100% tested.

AC Conditions of Test

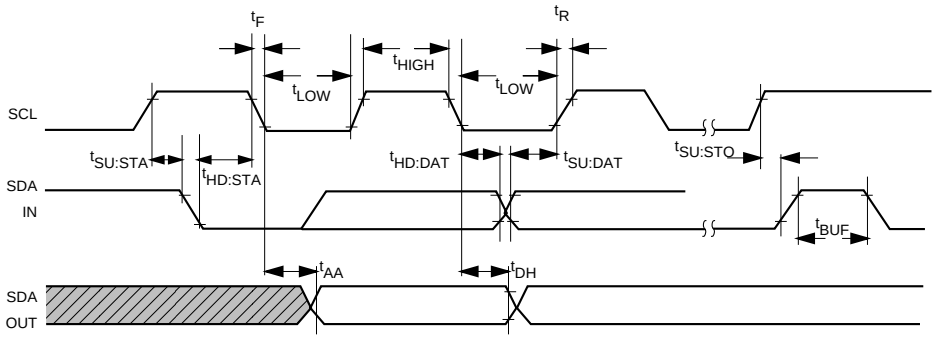
Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10 ns
Input & Output Timing Levels	V_{CC} x 0.5
Output Load	1 TTL Gate and C_L = 100 pF

Read and Write Cycle Limits (Standard and Low V_{CC} Range - 2.7V-5.5V)

Symbol	Parameter	100 KHz		400 KHz		Units
		Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		100		400	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs (Minimum V_{IN} Pulse width)		100		50	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	0.1	0.9	µs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		1.3		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		0.6		µs
t_{LOW}	Clock Low Period	4.7		1.5		µs
t_{HIGH}	Clock High Period	4.0		0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		µs
$t_{HD:DAT}$	Data in Hold Time	0		0		ns
$t_{SU:DAT}$	Data in Setup Time	250		100		ns
t_R	SDA and SCL Rise Time		1		0.3	µs
t_F	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		0.6		µs
t_{DH}	Data Out Hold Time	300		50		ns
t_{WR} (Note 3)	Write Cycle Time - NM24C65 - NM24C65L, NM24C65LZ		10 15		10 15	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the NM24C65 bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address

Bus Timing



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BACKGROUND INFORMATION (IIC Bus)

As mentioned, the IIC bus allows synchronous bidirectional communication between Transmitter/Receiver using the SCL (clock) and SDA (Data I/O) lines. All communication must be started with a valid START condition, concluded with a STOP condition and acknowledged by the Receiver with an ACKNOWLEDGE condition.

In addition, since the IIC bus is designed to support other devices such as RAM, EPROM, etc., the device type identifier string, or slave address, must follow the START condition. For EEPROMs, the first 4-bits of the slave address is '1010'. This is then followed by the device selection bits A2, A1 and A0.The final bit in the slave address determines the type of operation performed (READ/WRITE). A "1" signifies a READ while a "0" signifies a WRITE. The slave address is then followed by two bytes that define the word address, which is then followed by the data byte.

The EEPROMs on the IIC bus may be configured in any manner required, providing the total memory addressed does not exceed 4M bits in the Extended IIC protocol. EEPROM memory addressing is controlled by hardware configuring the A2, A1, and A0 pins (Device Address pins) with pull-up or pull-down resistors. ALL UNUSED PINS MUST BE GROUNDED (tied to V_{SS}).

Addressing an EEPROM memory location involves sending a command string with the following information:

[DEVICE TYPE]-[DEVICE ADDRESS]-[PAGE BLOCK ADDRESS]-[BYTE ADDRESS]

	Definitions
Word	8 bits (byte) of data
Page	32 sequential addresses (one byte each) that may be programmed during a "Page Write" programming cycle.
Master	Any IIC device CONTROLLING the transfer of data (such as a microcontroller).
Slave	Device being controlled (EEPROMS are always considered Slaves).
Transmitter	Device currently SENDING data on the bus (may be either a Master or Slave).
Receiver	Device currently receiving data on the bus (Master or Slave).

Pin Description

SERIAL CLOCK (SCL)

The SCL input is used to clock all data into and out of the device.

SERIAL DATA (SDA)

SDA is a biderectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

Device Address Inputs (A0, A1, A2)

Device address pins A0, A1, and A2 are connected to V_{CC} or V_{SS} to configure the EEPROM address for multiple device configuration. A total of eight different devices can be attached to the same SDA bus.

Write Protection (WP)

If WP is tied to V_{CC}, program WRITE operations onto the upper half of the memory will not be executed. READ operations are always available.

If WP is tied to V_{SS}, normal memory operation is enabled, READ/WRITE over the entire bit memory array.

This feature allows the user to assign the upper half of the memory as ROM which can be protected against accidental programming writes. When WRITE is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

Device Operation

The NM24C65xxx supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving devices as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the NM24C65xxx is considered a slave in all applications.

CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH and reserved for indicating start and stop conditions. *Refer to Figures 2 and 3.*

START CONDITION

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The NM24C65xxx continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

STOP CONDITION

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the NM24C65xxx to place the device in the standby power mode.

Write Cycle Timing

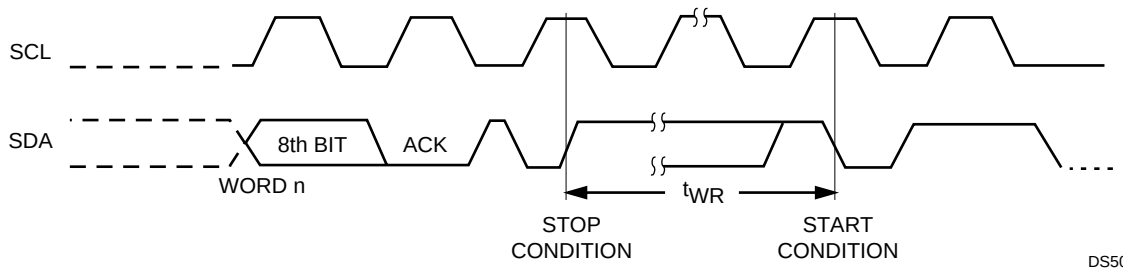
ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to *Figure 4*.

The NM24C65xxx device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the NM24C65xxx will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the READ mode the NM24C65xxx slave will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to the standby power mode.

Write Cycle Timing (Figure 1)



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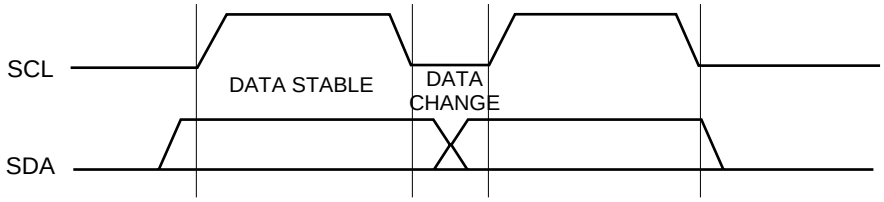
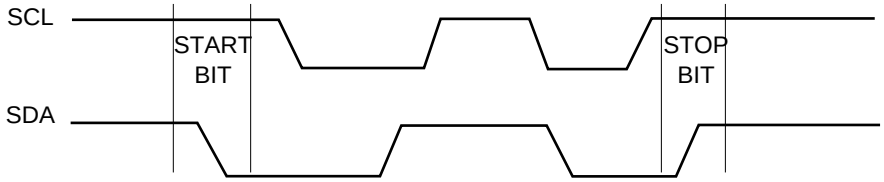
Data Validity (Figure 2)



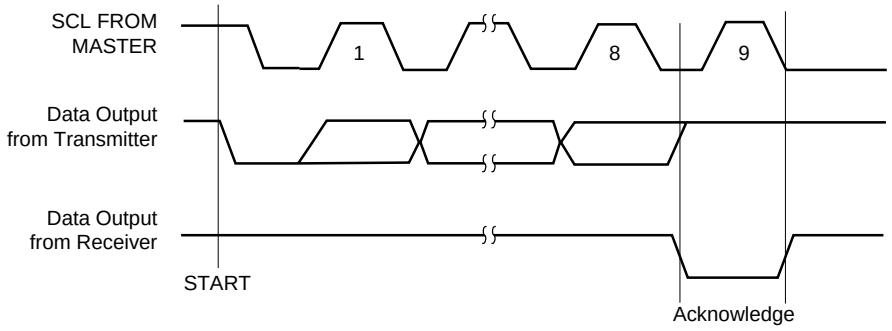
DS500042-5

Definition of Start and Stop (Figure 3)



DS500042-6

Acknowledge Response from Receiver (Figure 4)



DS500042-7

DEVICE ADDRESSING

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are those of the device type identifier. This is fixed as 1010 for all EEPROM devices.

The next three bits identifies the device address. Address from 000 to 111 are acceptable thus allowing up to eight devices to be connected to the IIC bus.

The last bit of the slave address defines whether a write or read condition is requested by the master. A "1" indicates that a READ operation is to be executed and a "0" initiates the WRITE mode.

A simple review: After the NM24C65xxx recognizes the start condition, the devices interfaced to the IIC bus waits for a slave address to be transmitted over the SDA line. If the transitted slave address matches an address of one of the devices, the designated slave pulls the line LOW with an acknowledge. signal and awaits further transmissions.

Write Operations

BYTE WRITE

For a WRITE operation, two additional address bytes, with 13 active bits, are required after the SLAVE acknowledge to address the full memory array. The first byte indicates the high-order byte of the word address. Only the five least signicant bits can be changed, the other bits are pre-assigned the value "0". Following the acknowledgement from the first word address, the next byte indicates the low-order byte of the word address. Upon receipt of the word address, the NM24C65xxx responds with another acknowledge and waits for the next eight bits of data, again, responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the NM24C65xxx begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress, the device's inputs are disabled and the device will not respond to any requests from the master. Refer to *Figure 5* for the address, acknowledge and data transfer sequence.

PAGE WRITE

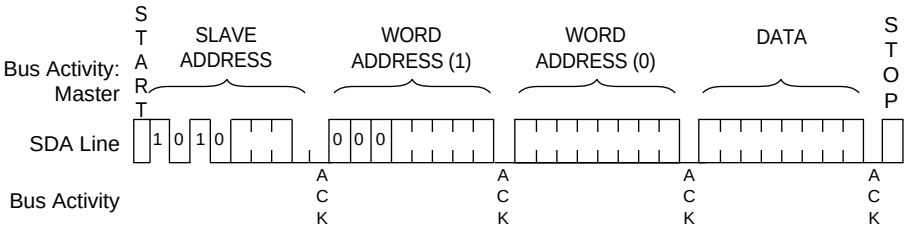
The NM24C65xxx is capable of thirty-two byte page write operation. It is initiated in the same manner as the byte write operation; but instead of termination the write cycle after the first data word is transfered, the master can transmit up to thirty-one more words. After the receipt of each word, the device responds with an acknowledge.

After the receipt of each word, the internal address counter increments to the next address and the next SDA data is accepted. If the master should transmit more than thirty-two words prior to generating the stop condition, the address counter will "roll over" and the previous written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to *Figure 6* for the address, acknowledge and data transfer sequence.

Acknowledge Polling

Once the stop condition is isssued to indicate the end of the host's write operation, the NM24C65xxx initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the NM24C65xxx is still busy with the write operation, no ACK will be returned. If the device has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

Byte Write (Figure 5)



DS500042-8

Write Protection

Programming of the upper half of memory will not take place if the WP pin is connected to V_{CC}. The device will accept slave and word addresses; but if the memory accessed is write protected by the WP pin, the NM24C65xxx will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the stop condition is asserted.

Low V_{CC} Lockout

NM24C65xxx provides data security against inadvertent writes that could potentially happen during the time the device is being powered on, powered down and brown out conditions by monitoring the V_{CC} voltage during a write cycle. Whenever a write cycle is started, the built-in circuitry starts to monitor the V_{CC} level throughout the duration of the write command sequence until the master issues the required STOP condition to start the actual internal write operation. If the sensed V_{CC} voltage is below 3.8V at any point during this monitoring period, the device prohibits the write operation and does not generate the ACK pulse. This low V_{CC} lockout feature is only available for standard 5V device.

Read Operation

Read operations are initiated in the same manner as write operations, with the exception that the R/W bit of the slave address is set to "1". There are three basic read operations: current address read, random read and sequential read.

CURRENT ADDRESS READ

Internally the NM24C65xxx contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n+1. Upon receipt of the slave address with R/W set to one, the NM24C65xxx issues an acknowledge and transmits the eight bit word. The master will not acknowledge acknowledge the transfer but does generate a stop condition, and therefore discontinues transmission. Refer to *Figure 7* for the sequence of address, acknowledge and data transfer.

RANDOM READ

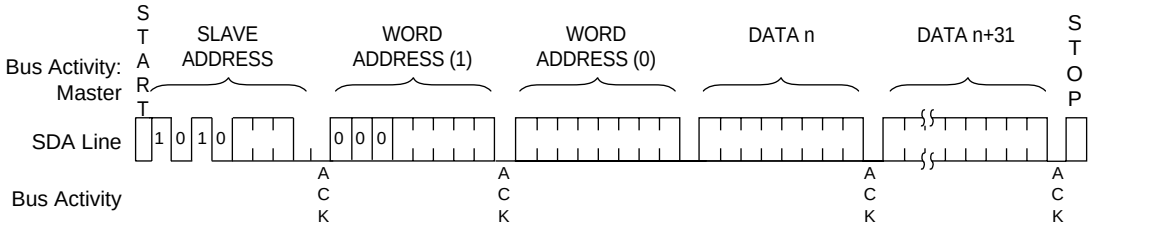
Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/W bit set to "1", the master must first perform a "dummy" write operation. The master issues a start condition, slave address and then the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/W bit set to "1". This will be followed by an acknowledge from the NM24C65xxx and then by the eight bit word. The master will not acknowledge the transfer but does generate the stop condition, and therefore the NM24C65xxx discontinues transmission. Refer to *Figure 8* for the address, acknowledge and data transfer sequence.

SEQUENTIAL READ

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted in the same manner as the other read modes; however, the master now responds with an acknowledge, indicating it requires additional data. The NM24C65xxx continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge or by generating a stop condition.

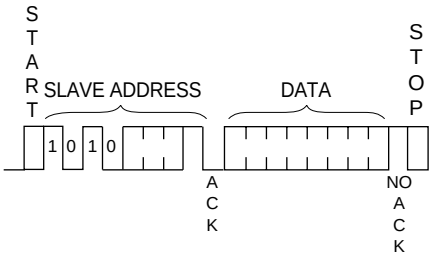
The data output is sequential, with the data from address n, followed by the data n+1. The address counter for read operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. After the entire memory has been read, the counter "rolls over" and the NM24C65xxx continues to output data for each acknowledge received. Refer to *Figure 9* for the address, acknowledge and data transfer sequence.

Page Write (Figure 6)



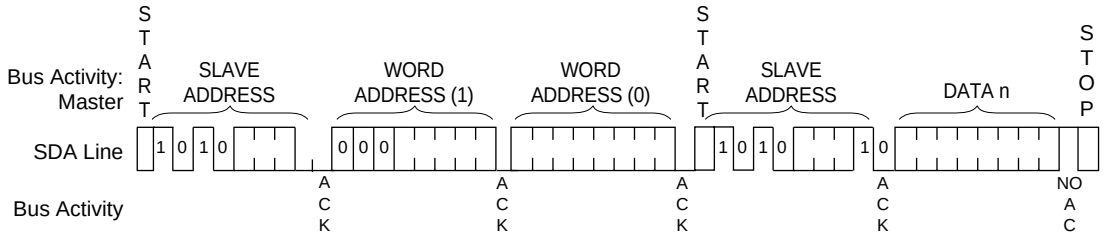
DS500042-9

Current Address Read (Figure 7)



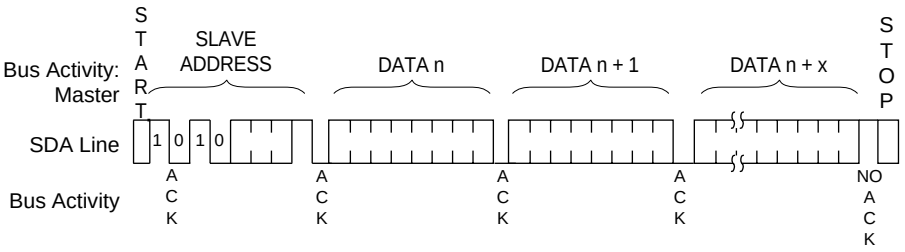
DS500042-10

Random Read (Figure 8)



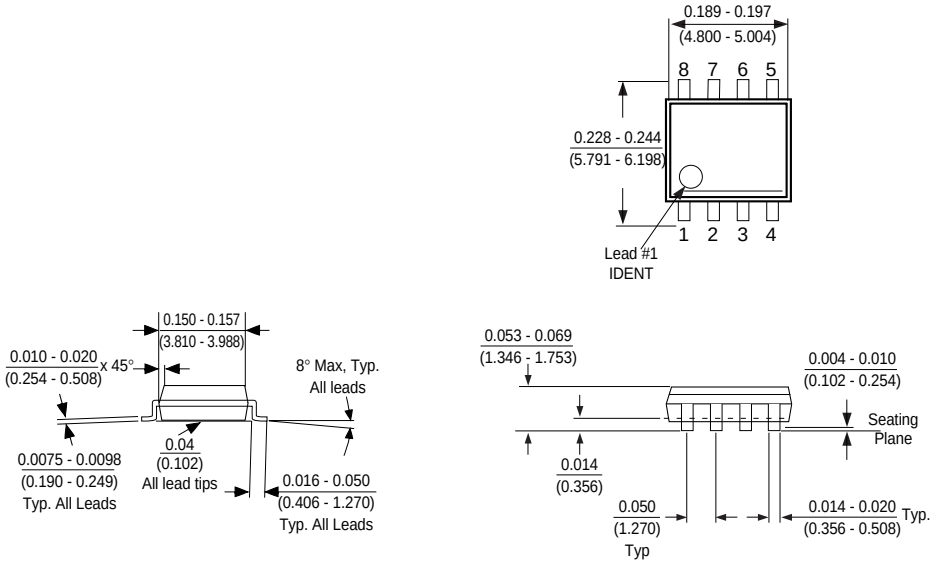
DS500042-11

Sequential Read (Figure 9)



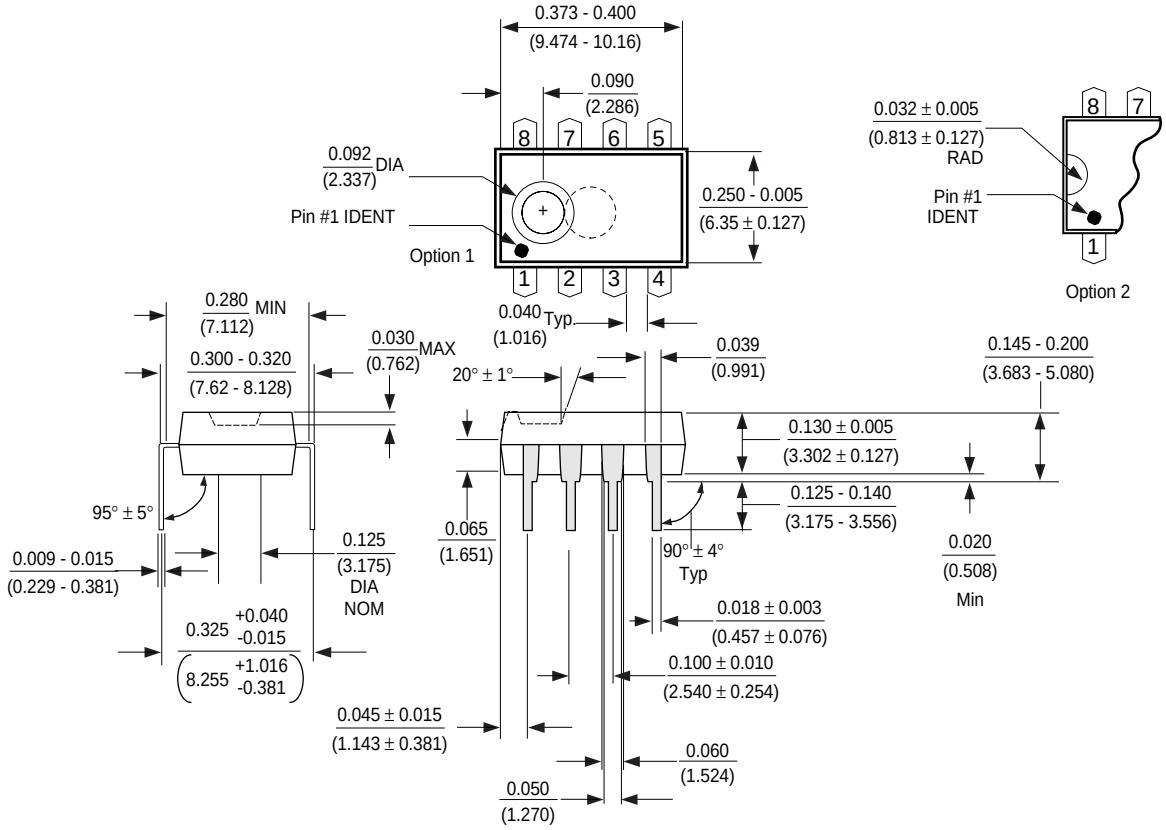
DS500042-12

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Small Out-Line Package (M8)
Order Number NM24C65xxxM8 or NM24C65xxxEM8
Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Order Number NM24C65xxxN or NM24C65xxxEN
Package Number N08E

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

PRELIMINARY

August 1999

NM24C65U
64K-Bit Serial EEPROM with Write Protect 2-Wire Bus Interface

General Description:

The NM24C65U is a 64K (65,536) bit serial interface CMOS EEPROM (Electrically Erasable Programmable Read-Only Memory). This device fully conforms to the **Extended** I²C™ 2-wire protocol which uses Clock (SCL) and Data I/O (SDA) pins to synchronously clock data between the "master" (for example a microprocessor) and the "slave" (the EEPROM device). In addition, the serial interface allows a minimal pin count packaging designed to simplify PC board layout requirements and offers the designer a variety of low voltage and low power options.

NM24C65U incorporates a hardware "Write Protect" feature, by which the upper half of the memory can be disabled against programming by connecting the WP pin to V_{CC}. This section of memory then effectively becomes a ROM (Read-Only Memory) and can no longer be programmed as long as WP pin is connected to V_{CC}.

Fairchild EEPROMs are designed and tested for applications requiring high endurance, high reliability and low power consumption for a continuously reliable non-volatile solution for all markets.

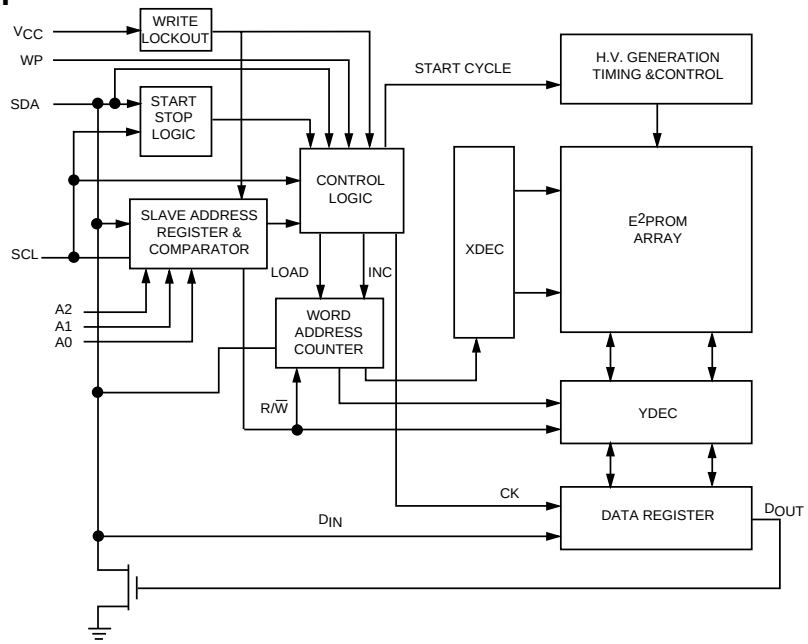
Functions

- I²C™ compatible interface
- 65,536 bits organized as 8,192 x 8
- 100 KHz or 400 KHz operation
- Extended 2.7V – 5.5V operating voltage
- Self timed programming cycle (6ms typical)
- "Programming complete" indicated by ACK polling
- Memory "Upper Block" Write Protect pin

Features

- The I²C™ interface allows the smallest I/O pincount of any EEPROM interface
- 32 byte page write mode to minimize total write time per byte
- Low V_{CC} programming lockout (3.8V)
  — **"H" option (Standard V_{CC} range) parts only**
- Typical 200µA active current (I_{CCA})
- Typical 1µA standby current (I_{SB}) for "L" devices and 0.1µA standby current for "LZ" devices
- Endurance: Up to 1,000,000 data changes
- Data retention greater than 40 years

Block Diagram

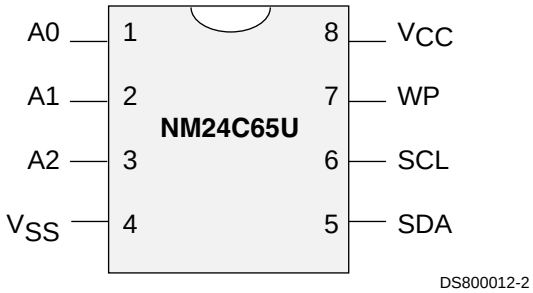


DS800012-1

I²C™ is a registered trademark of Philips Electronics N.V.

Connection Diagram

Dual-In-Line Package (N)
and 8-Pin SO Package (M8)



Top View
See Package Number N08E and M08A

Pin Names

A0, A1, A2	Device Address Input
V_{SS}	Ground
SDA	Data I/O
SCL	Clock Input
WP	Write Protect
V_{CC}	Power Supply

Ordering Information

NM 24 C XX U F LZ E XX

	Letter	Description
Package	N	8-Pin DIP
	M8	8-Pin SOIC
Temp. Range	None	0 to 70°C
	V	-40 to +125°C
	E	-40 to +85°C
Voltage Operating Range	Blank	4.5V to 5.5V
	L	2.7V to 5.5V
	LZ	2.7V to 5.5V and <1µA Standby Current
	H	4.5V to 5.5V and V_{CC} Lockout
SCL Clock Frequency	Blank	100KHz
	F	400KHz
	Ultralite	CS100UL Process
Density	65	64K with Write Protect
	C	CMOS
Interface	24	IIC
	NM	**Fairchild Non-Volatile Memory**

Product Specifications

Absolute Maximum Ratings

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltages with Respect to Ground	6.5V to –0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min.

Operating Conditions

Ambient Operating Temperature	
NM24C65U	0°C to +70°C
NM24C65UE	-40°C to +85°C
NM24C65UV	-40°C to +125°C
Positive Power Supply	
NM24C65U/NM24C65UH	4.5V to 5.5V
NM24C65UL	2.7V to 5.5V
NM24C65ULZ	2.7V to 5.5V

Standard V_{CC} (4.5V to 5.5V) DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 400 kHz f_{SCL} = 100 kHz		0.2	1.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		10	50	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	1	µA
V_{IL}	Input Low Voltage		–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Low V_{CC} (2.7V to 5.5V) DC Electrical Characteristics

Symbol	Parameter	Test Conditions		Limits			Units
				Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 400 KHz f_{SCL} = 100 KHz			0.2	1.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}	V_{CC} = 2.7V - 4.5V V_{CC} = 2.7V - 4.5V V_{CC} = 4.5V - 5.5V		1 0.1 10	10 1 50	µA µA µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}			0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}			0.1	1	µA
V_{IL}	Input Low Voltage			–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA				0.4	V

Capacitance T_A = +25°C, f = 100/400 KHz, V_{CC} = 5V (Note 2)

Symbol	Test	Conditions	Max	Units
$C_{I/O}$	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN}	Input Capacitance (A0, A1, A2, SCL)	V_{IN} = 0V	6	pF

Note 1: Typical values are for T_A = 25°C and nominal supply voltage (5V).

Note 2: This parameter is periodically sampled and not 100% tested.

AC Conditions of Test

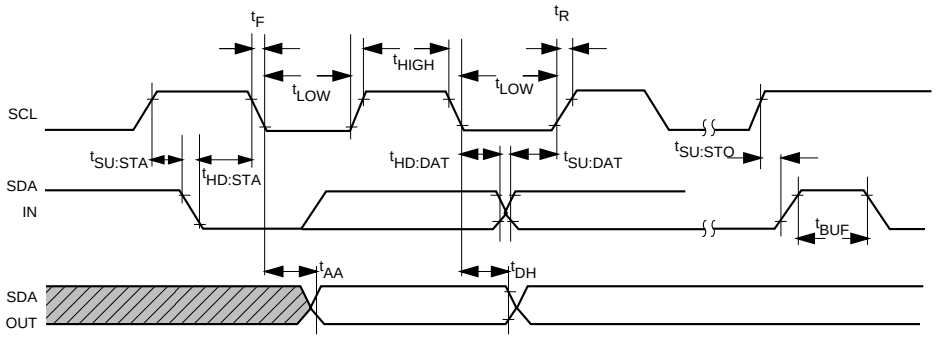
Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10 ns
Input & Output Timing Levels	V_{CC} x 0.5
Output Load	1 TTL Gate and C_L = 100 pF

Read and Write Cycle Limits (Standard and Low V_{CC} Range - 2.7V-5.5V)

Symbol	Parameter	100 KHz		400 KHz		Units
		Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		100		400	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs (Minimum V_{IN} Pulse width)		100		50	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	0.1	0.9	µs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		1.3		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		0.6		µs
t_{LOW}	Clock Low Period	4.7		1.5		µs
t_{HIGH}	Clock High Period	4.0		0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		µs
$t_{HD:DAT}$	Data in Hold Time	0		0		µs
$t_{SU:DAT}$	Data in Setup Time	250		100		ns
t_R	SDA and SCL Rise Time		1		0.3	µs
t_F	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		0.6		µs
t_{DH}	Data Out Hold Time	300		50		ns
t_{WR} (Note 3)	Write Cycle Time - NM24C65U - NM24C65UL, NM24C65ULZ		10 15		10 15	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the NM24C65U bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address

Bus Timing



DS800012-3

BACKGROUND INFORMATION (IIC Bus)

As mentioned, the IIC bus allows synchronous bidirectional communication between Transmitter/Receiver using the SCL (clock) and SDA (Data I/O) lines. All communication must be started with a valid START condition, concluded with a STOP condition and acknowledged by the Receiver with an ACKNOWLEDGE condition.

In addition, since the IIC bus is designed to support other devices such as RAM, EPROM, etc., the device type identifier string, or slave address, must follow the START condition. For EEPROMs, the first 4-bits of the slave address is '1010'. This is then followed by the device selection bits A2, A1 and A0.The final bit in the slave address determines the type of operation performed (READ/WRITE). A "1" signifies a READ while a "0" signifies a WRITE. The slave address is then followed by two bytes that define the word address, which is then followed by the data byte.

The EEPROMs on the IIC bus may be configured in any manner required, providing the total memory addressed does not exceed 4M bits in the Extended IIC protocol. EEPROM memory addressing is controlled by hardware configuring the A2, A1, and A0 pins (Device Address pins) with pull-up or pull-down resistors. ALL UNUSED PINS MUST BE GROUNDED (tied to V_{SS}).

Addressing an EEPROM memory location involves sending a command string with the following information:

[DEVICE TYPE]-[DEVICE ADDRESS]-[PAGE BLOCK ADDRESS]-[BYTE ADDRESS]

	Definitions
Word	8 bits (byte) of data
Page	32 sequential addresses (one byte each) that may be programmed during a "Page Write" programming cycle.
Master	Any IIC device CONTROLLING the transfer of data (such as a microcontroller).
Slave	Device being controlled (EEPROMS are always considered Slaves).
Transmitter	Device currently SENDING data on the bus (may be either a Master or Slave).
Receiver	Device currently RECEIVING data on the bus (Master or Slave).

Pin Description

SERIAL CLOCK (SCL)

The SCL input is used to clock all data into and out of the device.

SERIAL DATA (SDA)

SDA is a biderectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

Device Address Inputs (A0, A1, A2)

Device address pins A0, A1, and A2 are connected to V_{CC} or V_{SS} to configure the EEPROM address for multiple device configuration. A total of eight different devices can be attached to the same SDA bus.

Write Protection (WP)

If WP is tied to V_{CC}, program WRITE operations onto the upper half of the memory will not be executed. READ operations are always available.

If WP is tied to V_{SS}, normal memory operation is enabled, READ/WRITE over the entire bit memory array.

This feature allows the user to assign the upper half of the memory as ROM which can be protected against accidental programming writes. When WRITE is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

Device Operation

The NM24C65Uxxx supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving devices as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the NM24C65Uxxx is considered a slave in all applications.

CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH and reserved for indicating start and stop conditions. *Refer to Figures 2 and 3.*

START CONDITION

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The NM24C65Uxxx continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

STOP CONDITION

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the NM24C65Uxxx to place the device in the standby power mode.

Write Cycle Timing

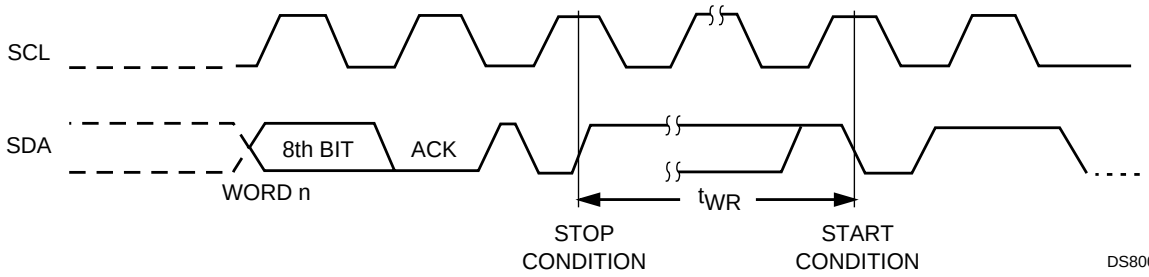
ACKNOWLEDGE

Acknowledge is a hardware convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to *Figure 4*.

The NM24C65Uxxx device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the NM24C65Uxxx will respond with an acknowledge after the receipt of each subsequent eight bit word.

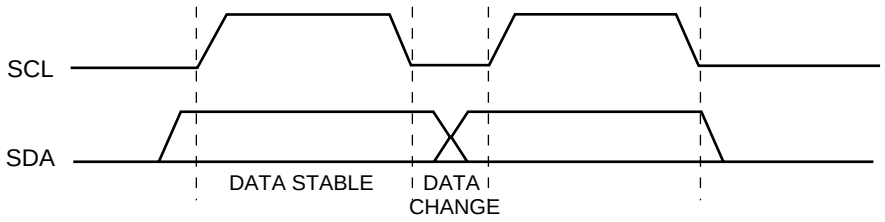
In the READ mode the NM24C65Uxxx slave will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to the standby power mode.

Write Cycle Timing (Figure 1)



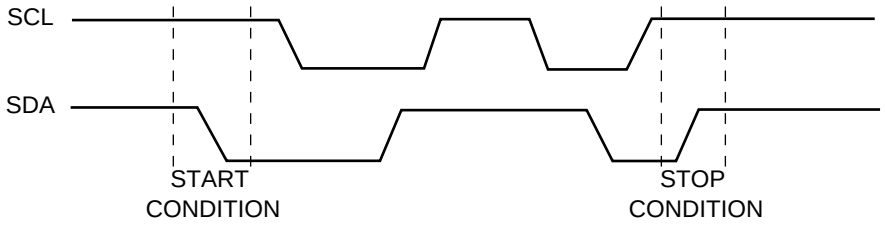
DS800012-4

Data Validity (Figure 2)



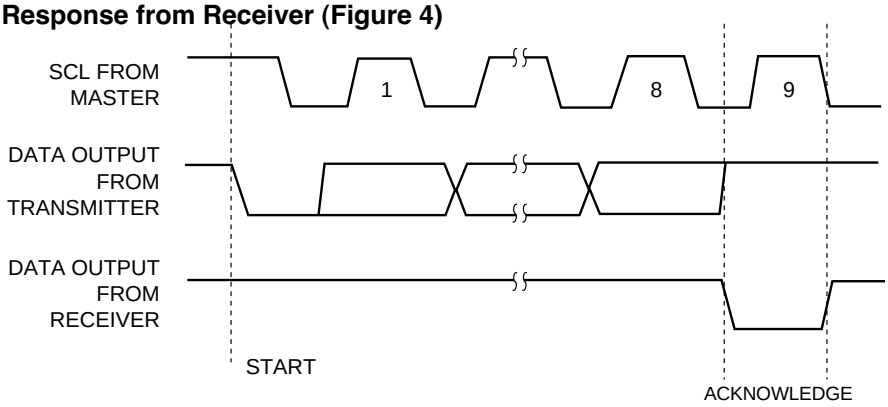
DS800012-5

Definition of Start and Stop (Figure 3)



DS800012-6

Acknowledge Response from Receiver (Figure 4)



DS800012-7

DEVICE ADDRESSING

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are those of the device type identifier. This is fixed as 1010 for all EEPROM devices.

The next three bits identifies the device address. Address from 000 to 111 are acceptable thus allowing up to eight devices to be connected to the IIC bus.

The last bit of the slave address defines whether a write or read condition is requested by the master. A "1" indicates that a READ operation is to be executed and a "0" initiates the WRITE mode.

A simple review: After the NM24C65Uxxx recognizes the start condition, the devices interfaced to the IIC bus wait for a slave address to be transmitted over the SDA line. If the transmitted slave address matches an address of one of the devices, the designated slave pulls the line LOW with an acknowledge signal and awaits further transmissions.

Write Operations

BYTE WRITE

For a WRITE operation, two additional address bytes, with 13 active bits, are required after the SLAVE acknowledge to address the full memory array. The first byte indicates the high-order byte of the word address. Only the five least signicant bits can be changed, the other bits are pre-assigned the value "0". Following the acknowledgement from the first word address, the next byte indicates the low-order byte of the word address. Upon receipt of the word address, the NM24C65Uxxx responds with another acknowledge and waits for the next eight bits of data, again, responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the NM24C65Uxxx begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress, the device's inputs are disabled and the device will not respond to any requests from the master. Refer *Figure 5* for the Byte Write sequence.

PAGE WRITE

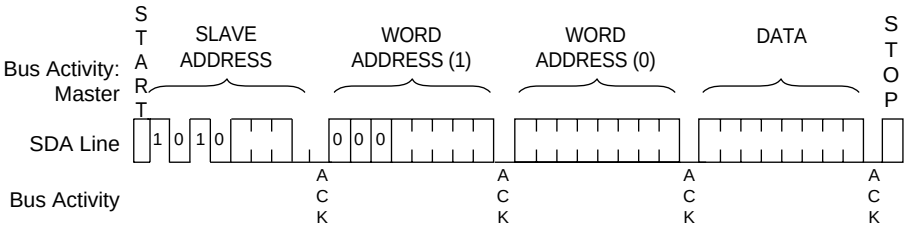
The NM24C65Uxxx is capable of thirty-two byte page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data word is transfered, the master can transmit up to thirty-one more words. After the receipt of each word, the device responds with an acknowledge.

After the receipt of each word, the internal address counter increments to the next address and the next SDA data is accepted. If the master should transmit more than thirty-two words prior to generating the stop condition, the address counter will "roll over" and the previous written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer *Figure 6* for the Page Write sequence.

Acknowledge Polling

Once the stop condition is isssued to indicate the end of the host's write operation, the NM24C65Uxxx initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the NM24C65Uxxx is still busy with the write operation, no ACK will be returned. If the device has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

Byte Write (Figure 5)



DS800012-8

Write Protection

Programming of the upper half of memory will not take place if the WP pin is connected to V_{CC}. The device will accept slave and word addresses; but if the memory accessed is write protected by the WP pin, the NM24C65Uxxx will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the stop condition is asserted.

Low V_{CC} Lockout

NM24C65UxHx (H option) protects against data corruption during programming by preventing any programming operations if V_{CC} drops below approximately 3.8V (V_{CC} Lockout trip level). This is accomplished by monitoring the "READ/WRITE" (R/$\overline{W}$) bit in the SLAVE address and if the R/$\overline{W}$ bit is "0," indicating a programming operation, the V_{CC} Lockout is activated. At that point, if the V_{CC} drops below the trip level, programming is inhibited and the device does not issue an ACK (the output stays high). To restate, the V_{CC} Lockout feature is active from the time a WRITE bit is received up to the time that the Master's STOP condition is received (the STOP condition turns on the V_{PP} internal high voltage). **Once programming has begun, the programming cycle cannot be interrupted except by removal of V_{CC}, which could result in data corruption.**

Read Operation

Read operations are initiated in the same manner as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to "1". There are three basic read operations: current address read, random read and sequential read.

CURRENT ADDRESS READ

Internally the NM24C65Uxxx contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n+1. Upon receipt of the slave address with R/$\overline{W}$ set to one, the NM24C65Uxxx issues an acknowledge and transmits the eight bit word. The master will not acknowledge acknowledge the transfer but does generate a stop condition, and therefore discontinues transmission. Refer *Figure 7* for the Current Address Read sequence.

RANDOM READ

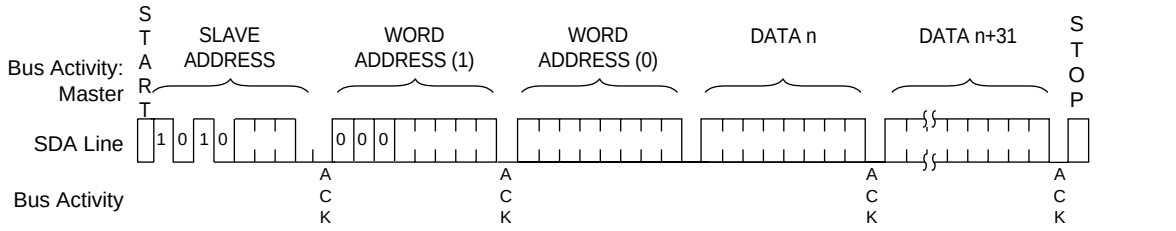
Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to "1", the master must first perform a "dummy" write operation. The master issues a start condition, slave address with the R/$\overline{W}$ bit set to "0" and then the word address it is to read from. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to "1". This will be followed by an acknowledge from the NM24C65Uxxx and then by the eight bit data. The master will not acknowledge the transfer but does generate the stop condition, and therefore the NM24C65Uxxx discontinues transmission. Refer *Figure 8* for the Random Read sequence.

SEQUENTIAL READ

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted in the same manner as the other read modes; however, the master now responds with an acknowledge, indicating it requires additional data. The NM24C65Uxxx continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge or by generating a stop condition.

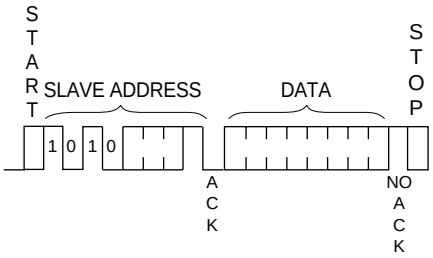
The data output is sequential, with the data from address n, followed by the data n+1. The address counter for read operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. After the entire memory has been read, the counter "rolls over" and the NM24C65Uxxx continues to output data for each acknowledge received. Refer *Figure 9* for the Sequential Read sequence.

Page Write (Figure 6)



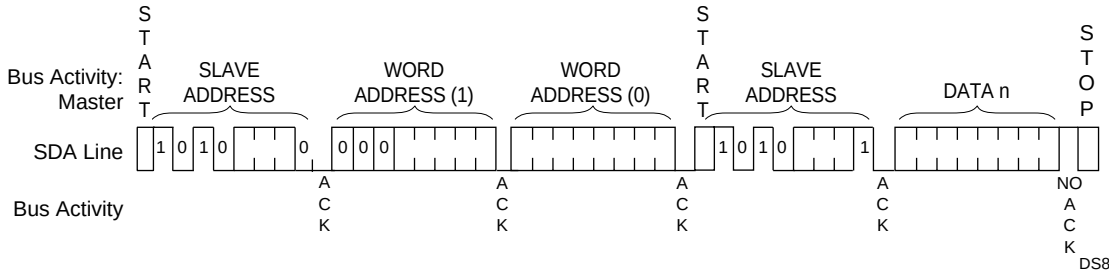
DS800012-9

Current Address Read (Figure 7)



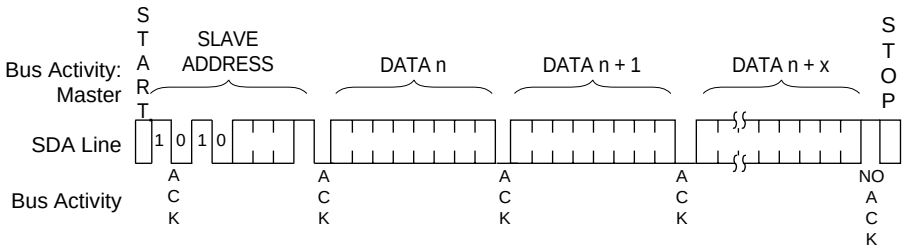
DS800012-10

Random Read (Figure 8)



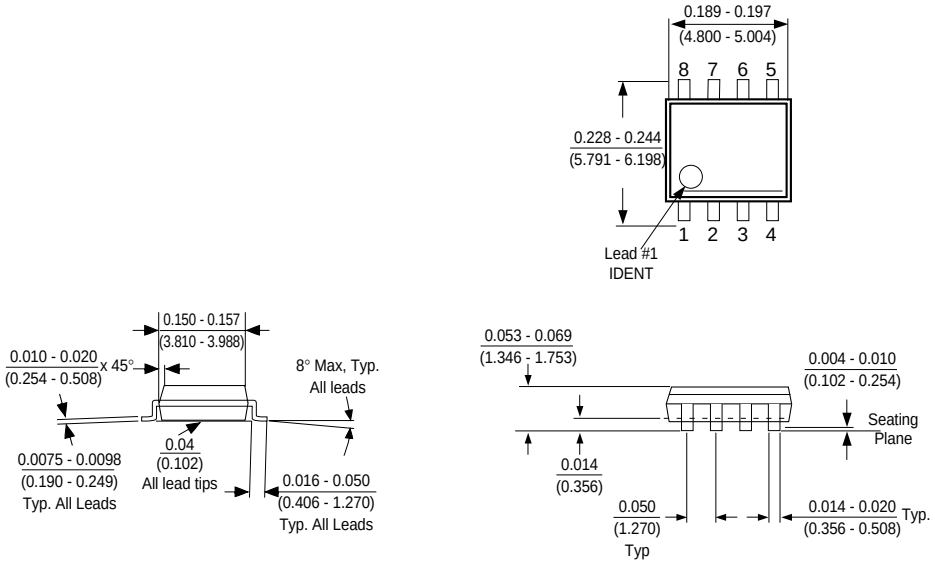
DS800012-11

Sequential Read (Figure 9)



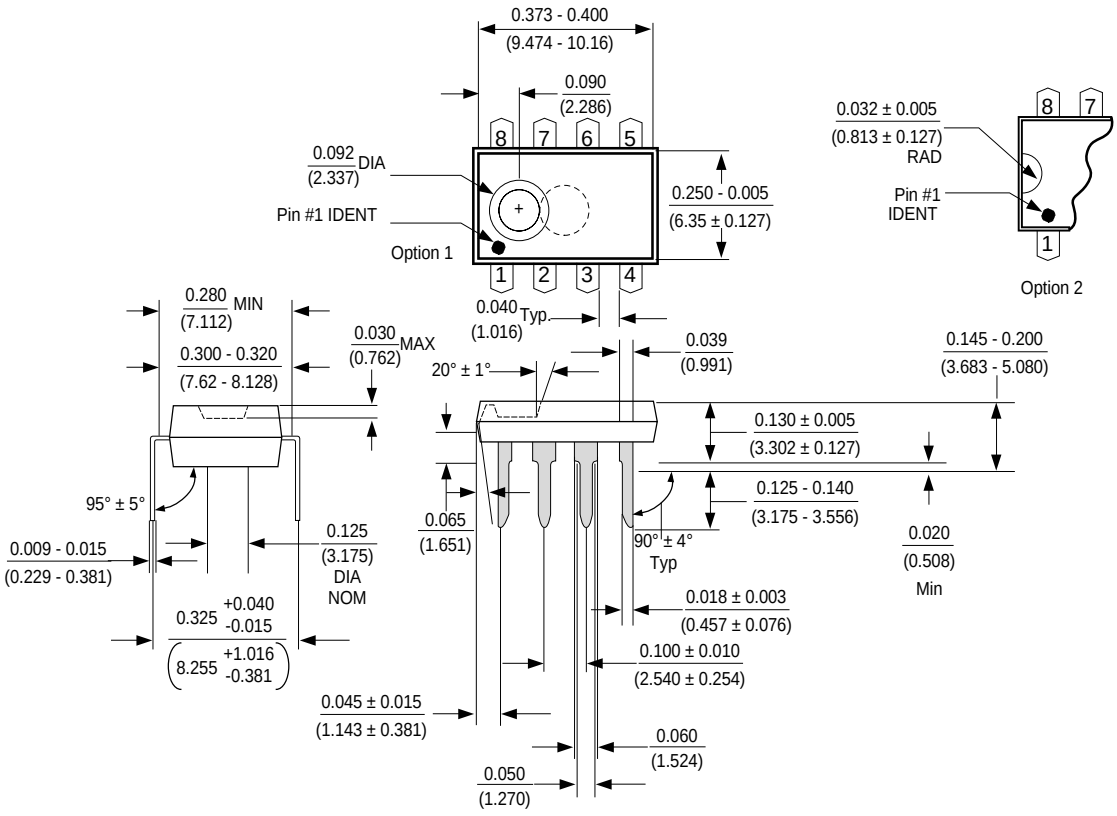
DS800012-12

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Small Out-Line Package (M8)
Order Number NM24C65UxxxM8 or NM24C65UxxxEM8
Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Order Number NM24C65UxxxN or NM24C65UxxxEN
Package Number N08E

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD
SEMICONDUCTOR™

PRELIMINARY
March 1999

NM24Wxx
2K/4K/8K/16K-Bit Standard 2-Wire Bus Interface Serial EEPROM with Full Array Write Protect

General Description

The NM24Wxx devices are 2048/4096/8192/16,384 bits, respectively, of CMOS non-volatile electrically erasable memory. These devices conform to all specifications in the IIC 2-wire protocol and are designed to minimize device pin count, and simplify PC board layout requirements.

The entire ememory can be disabled (Write Protected) by connecting the WP pin to V_{CC}. The memory then becomes unalterable unless WP is switched to V_{SS}.

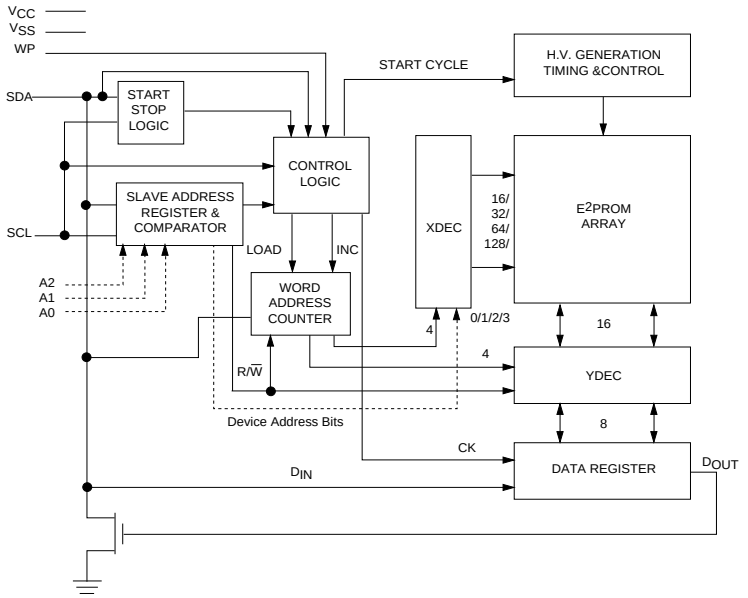
This communications protocol uses CLOCK (SCL) and DATA I/O (SDA) lines to synchronously clock data between the master (for example a microprocessor) and the slave EEPROM device(s). The Standard IIC protocol allows for a maximum of 16K of EEPROM memory which is supported by Fairchild's family in 2K, 4K, 8K, and 16K devices, allowing the user to configure the memory as the application requires with any combination of EEPROMs.

Fairchild EEPROMs are designed and tested for applications requiring high endurance, high reliability and low power consumption.

Features

- Hardware Write Protect for entire memory
- Low Power CMOS
  - 200µA active current typical
  - 10µA standby current typical
  - 1µA standby typical (L)
  - 0.1µA standby typical (LZ)
- IIC Compatible interface
  - — Provides bidirectional data transfer protocol
- Sixteen byte page write mode
  - — Minimizes total write time per byte
- Self timed write cycle
  - — Typical write cycle time of 6ms
- Endurance: 1,000,000 data changes
- Data retention greater than 40 years
- Packages available: 8-pin DIP, 8-pin SO, and 8-pin TSSOP
- Available in three temperature ranges
  - Commercial: 0° to +70°C
  - Extended (E): -40° to +85C
  - Automotive (V): -40° to +125°C

Block Diagram



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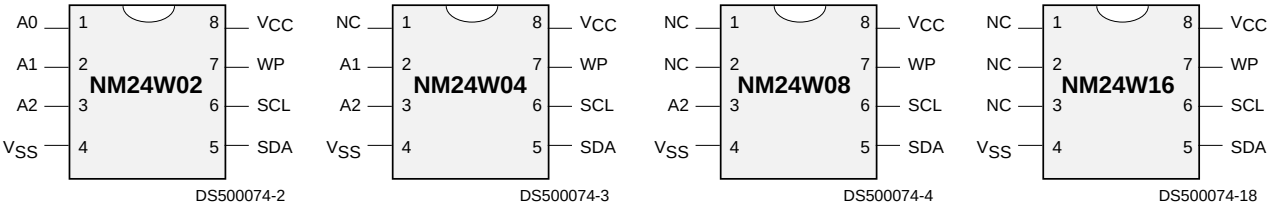
Connection Diagrams

Dual-In-Line Package (N), SO Package (M8), and TSSOP Package (MT8)



Top View
See Package Number N08E (N), M08A (M8), and MTC08 (MT8)

Pin Names	
A0,A1,A2	Device Address Inputs
V_{SS}	Ground
SDA	Data I/O
SCL	Clock Input
WP	Write Protect
V_{CC}	Power Supply
NC	No Connect

Ordering Information

NM 24 W XX LZ E XX

	Letter	Description
Package	N	8-Pin DIP
	M8	8-Pin SO8
	MT8	8-Pin TSSOP
Temp. Range	None	0 to 70°C
	E	-40 to +85°C
	V	-40°C to +125°C
Voltage Operating Range	Blank	4.5V to 5.5V
	L	2.7V to 4.5V
	LZ	2.7V to 4.5V and <1µA Standby Current
Density	02	2K
	04	4K
	08	8K
	16	16K
	W	Total Array Write Protect
Interface	24	IIC
	NM	**Fairchild Non-Volatile Memory**

Product Specifications

Absolute Maximum Ratings

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltages with Respect to Ground	6.5V to –0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min.

Operating Conditions

Ambient Operating Temperature	
NM24Wxx	0°C to +70°C
NM24WxxE	-40°C to +85°C
NM24WxxV	-40°C to +125°C
Positive Power Supply	
NM24Wxx	4.5V to 5.5V
NM24WxxL	2.7V to 4.5V
NM24WxxLZ	2.7V to 4.5V

Standard V_{CC} (4.5V to 5.5V) DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		0.2	1.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		10	50	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	1	µA
V_{IL}	Input Low Voltage		–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Low V_{CC} (2.7V to 5.5V) DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		0.2	1.0	mA
I_{SB}	Standby Current for L Standby Current for LZ	V_{IN} = GND or V_{CC} V_{IN} = GND or V_{CC}		1 0.1	10 1	µA µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	1	µA
V_{IL}	Input Low Voltage		–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Capacitance T_A = +25°C, f = 100/400 KHz, V_{CC} = 5V (Note 2)

Symbol	Test	Conditions	Max	Units
$C_{I/O}$	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN}	Input Capacitance (A0, A1, A2, SCL)	V_{IN} = 0V	6	pF

Note 1: Typical values are T_A = 25°C and nominal supply voltage (5V).

Note 2: This parameter is periodically sampled and not 100% tested.

AC Conditions of Test

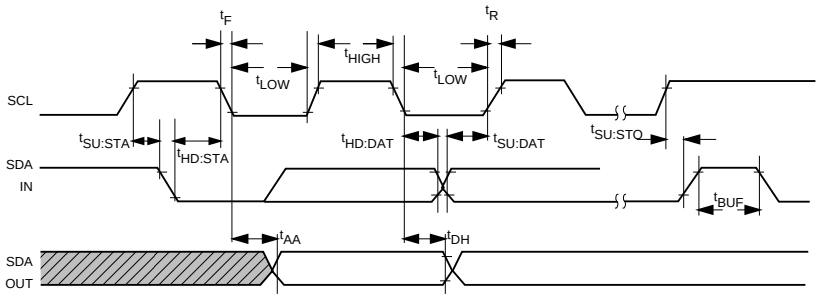
Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10 ns
Input & Output Timing Levels	V_{CC} x 0.5
Output Load	1 TTL Gate and C_L = 100 pF

Read and Write Cycle Limits (Standard and Low V_{CC} Range 2.7V - 4.5V)

Symbol	Parameter	100 KHz		400 KHz		Units
		Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		100		400	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs (Minimum V_{IN} Pulse width)		100		50	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	0.1	0.9	µs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		1.3		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		0.6		µs
t_{LOW}	Clock Low Period	4.7		1.5		µs
t_{HIGH}	Clock High Period	4.0		0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		µs
$t_{HD:DAT}$	Data in Hold Time	0		0		ns
$t_{SU:DAT}$	Data in Setup Time	250		100		ns
t_R	SDA and SCL Rise Time		1		0.3	µs
t_F	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		0.6		µs
t_{DH}	Data Out Hold Time	300		50		ns
t_{WR} (Note 3)	Write Cycle Time - NM24Wxx - NM24WxxL, NM24WxxLZ		10 15		10 15	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the NM24Wxx bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

Bus Timing



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Background Information (IIC Bus)

As mentioned, the IIC bus allows synchronous bidirectional communication between Transmitter/Receiver using the SCL (clock) and SDA (Data I/O) lines. All communication must be started with a valid START condition, concluded with a STOP condition and acknowledged by the Receiver with an ACKNOWLEDGE condition.

In addition, since the IIC bus is designed to support other devices such as RAM, EPROMs, etc., a devce type identifier string must follow the START condition. For EEPROMs, this 4-bit string is 1010 and is the first 4 bits in the slave address.

As shown below, the EEPROMs on the IIC bus may be configured in any manner required, and for the Standard IIC protocol, the total memory addressed can not exceed 16K (16,384 bits). EEPROM memory address programming is controlled by 2 methods:

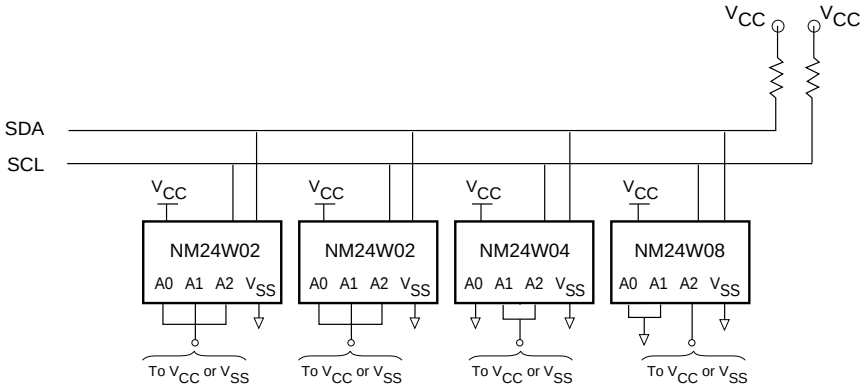
- Hardware configuring the A0, A1, and A2 pins (Device Address pins) with pull-up or pull-down to resistors. **All unused pins must be grounded** (tied to V_{SS}).
- Software addressing the required PAGE BLOCK within the device memory array (as sent in the Slave Address string).

Addressing an EEPROM memory location involves sending a command string with the following information:

[DEVICE TYPE]—[DEVICE ADDRESS]—[PAGE BLOCK ADDRESS]—[BYTE ADDRESS]

DEFINITIONS	
WORD	8 bits of data
PAGE	16 sequential addresses (one byte each) that may be programmed during a 'Page Write' programming cycle
PAGE BLOCK	2,048 (2K) bits organized into 16 pages of addressable memory. (8 bits) x (16 bytes) x (16 pages) = 2,048 bits
MASTER	Any IIC device CONTROLLING the transfer of data (such as a microprocessor)
SLAVE	Device being controlled (EEPROMs are always considered Slaves)
TRANSMITTER	Device currently SENDING data on the bus (may be either a Master or Slave).
RECEIVER	Device currently receiving data on the bus (Master or Slave)

Example of 16K of Memory on 2-Wire Bus



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Note: The SDA pull-up resistor is required due to the open-drain/open collector output of IIC bus devices.
The SCL pull-up resistor is recommended because of the normal SCL line inactive 'high' state.
It is recommended that the total line capacitance be less than 400pF.
Specific timing and addressing considerations are described in greater detail in the following sections.

Device	Address Pins			Memory Size	Number of Page Blocks
	A0	A1	A2		
NM24W02	ADR	ADR	ADR	2048 Bits	1
NM24W04	NC	ADR	ADR	4096 Bits	2
NM24W08	NC	NC	ADR	8192 Bits	4
NM24W16	NC	NC	NC	16,384 Bits	8

ADR is the hardware address (V_{CC}/1 or V_{SS}/0) of the device(s) used.

Pin Descriptions

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire–ORed with any number of open drain or open collector outputs.

Device Operation Inputs (A0, A1, A2)

Device address pins A0, A1, and A2 are connected to V_{CC} or V_{SS} to configure the EEPROM chip address. Table 1 shows the active pins across the NM24Wxx device family.

TABLE 1.

Device	A0	A1	A2	Effects of Addresses
NM24W02	ADR	ADR	ADR	2^3 = 8; 8*x(1x2K)**=16K
NM24W04	x	ADR	ADR	2^2 = 4; 4*x(2x2K)**=16K
NM24W08	x	x	ADR	2^1 = 2; 2*x(4x2K)**=16K
NM24W16	x	x	x	2^0 = 1; 1*x(8x2K)**=16K

* Max # of devices on bus
** Number of page blocks per density

WP Write Protection

If tied to V_{CC}, PROGRAM operations onto memory will not be executed. (Only READ operations are possible.) If tied to V_{SS}, normal operation is enabled (READ/WRITE over the entire memory is possible).

Device Operation

The NM24Wxx supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the NM24Wxx will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to *Figures 1* and *2.*

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The NM24Wxx continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Stop Condition

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the NM24Wxx to place the device in the standby power mode.

ACKNOWLEDGE

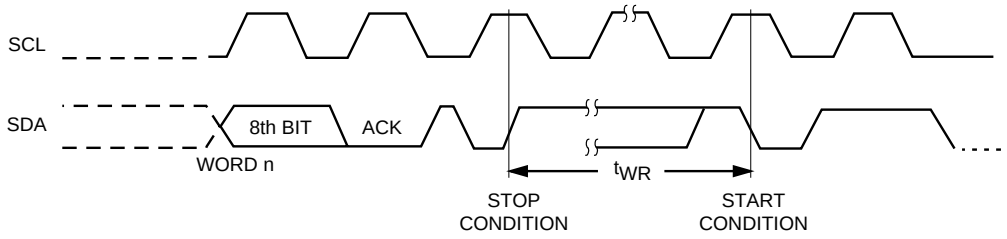
Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits.

During the ninth clock cycle the receiver will pull the SDA line to LOW to acknowledge that it received the eight bits of data. Refer to *Figure 3.*

The NM24Wxx device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the NM24Wxx will respond with an acknowledge after the receipt of each subsequent eight bit byte.

In the read mode the NM24Wxx slave will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to the standby power mode.

Write Cycle Timing



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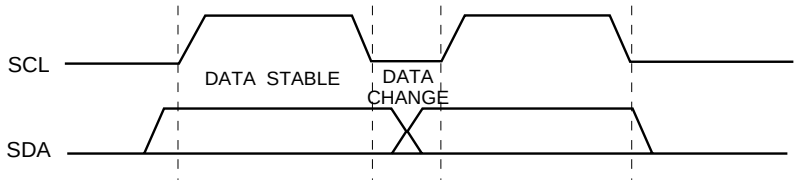
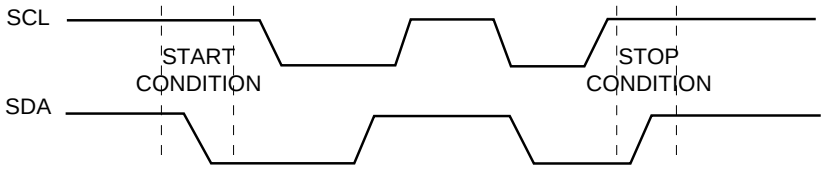
Data Validity (Figure 1)



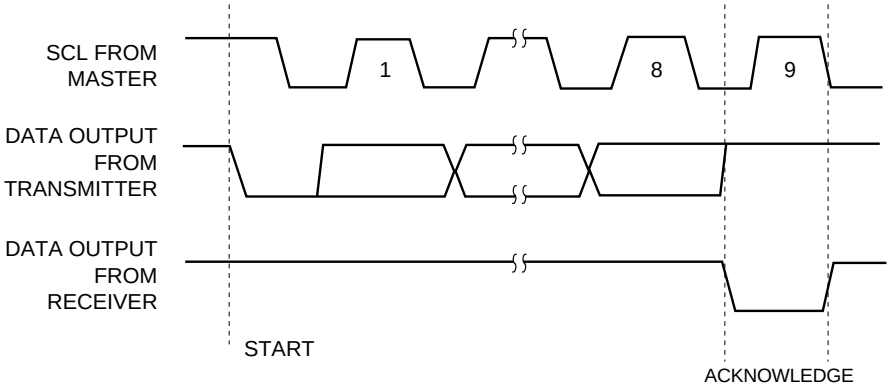
DS500074-8

Start and Stop Definition (Figure 2)



DS500074-9

Acknowledge Responses from Receiver (Figure 3)

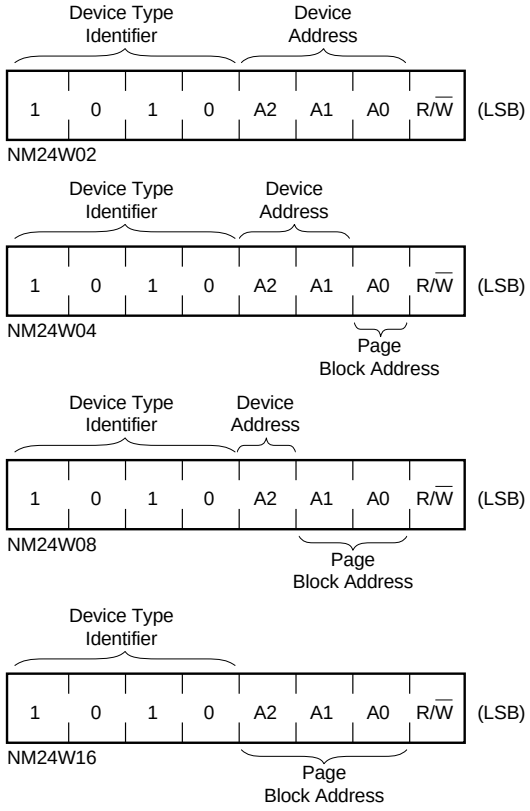


DS500074-10

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are those of the device type identifier (*see Figure 4)*. This is fixed as 1010 for all EEPROM devices.

Slave Addresses (Figure 4)



DS500074-11

All Standard IIC protocol EEPROMs use an internal protocol that defines a PAGE BLOCK size of 2K bits (for Byte addresses 00 through FF). Therefore, address bits A0, A1, or A2 (if designated 'P') are used to access a PAGE BLOCK in conjuction with the Byte address used to access any individual data byte.

Refer to the following table for Slave Address string details:

Device	A0	A1	A2	Page Blks	Page Block Addresses
NM24W02	A	A	A	1 (2K)	(None)
NM24W04	P	A	A	2 (4K)	0 1
NM24W08	P	P	A	4 (8K)	00 01 10 11
NM24W16	P	P	P	8 (16K)	000 001 010 011 100 101 110 111

Note: A: Refers to a hardware configured Device Address pin.
P: Refers to an internal PAGE BLOCK memory segment

The last bit of the slave address defines whether a write or read condition is requested by the master. A '1' indicates that a read operation is to be executed, and a '0' initiates the write mode.

A simple review: After the NM24Wxx recognizes the start condition, the devices interfaced to the IIC bus wait for a slave address to be transmitted over the SDA line. If the transmitted slave address matches an address of one of the devices, the designated slave pulls the line LOW with an acknowledge signal and awaits further transmissions.

Write Operations

Byte Write

For a write operation a second address field is required which is a word address that is comprised of eight bits and provides access to any one of the 256 words in the selected page of memory. Upon receipt of the word address the NM24Wxx responds with an acknowledge and waits for the next eight bits of data, again, responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the NM24Wxx begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the NM24Wxx inputs are disabled, and the device will not respond to any requests from the master. Refer to *Figure 5* for the address, acknowledge and data transfer sequence.

Page Write

The NM24Wxx is capable of a sixteen byte page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to fifteen more words. After the receipt of each word, the NM24Wxx will respond with an acknowledge.

After the receipt of each word, the internal address counter increments to the next address and the next SDA data is accepted.

If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will 'roll over' and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to *Figure 6* for the address, acknowledge, and data transfer sequence.

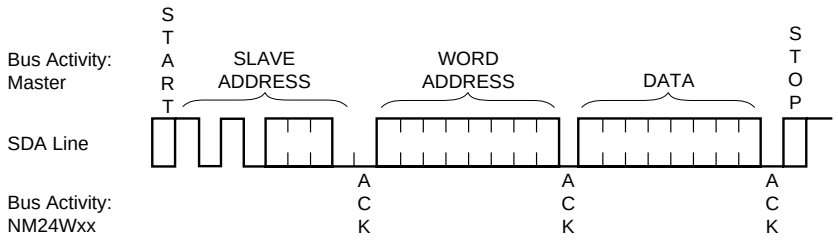
Acknowledge Polling

Once the stop condition is issued to indicate the end of the host's write operation the NM24Wxx initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the NM24Wxx is still busy with the write operation no ACK will be returned. If the NM24Wxx has completed the write operation an ACK will be returned and the host can then proceed with the next read or write operation.

Write Protection

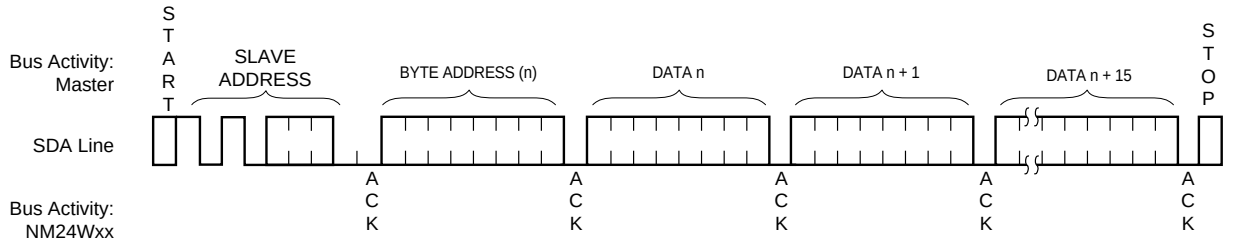
Programming of the memory will not take place if the WP pin of the NM24Wxx is connected to V_{CC}. The NM24Wxx will accept slave and word addresses; but if the memory accessed is write protected by the WP pin, the NM24Wxx will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the stop condition is asserted.

Byte Write (Figure 5)



DS500074-12

Page Write (Figure 6)



DS500074-13

Read Operations

Read operations are initiated in the same manner as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to a one. There are three basic read operations: current address read, random read, and sequential read.

Current Address Read

Internally the NM24Wxx contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ set to one, the NM24Wxx issues an acknowledge and transmits the eight bit word. The master will not acknowledge the transfer but does generate a stop condition, and therefore the NM24Wxx discontinues transmission. Refer to *Figure* 7 for the sequence of address, acknowledge and data transfer.

Random Read

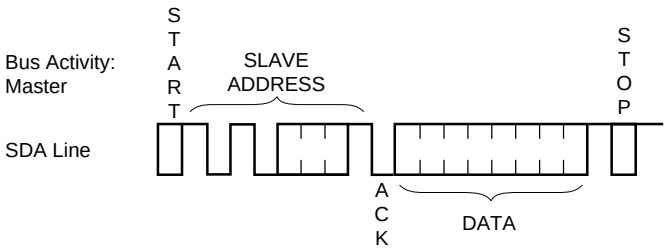
Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, slave address, R/$\overline{W}$ bit set to zero, and then the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the NM24Wxx and then by the eight bit word. The master will not acknowledge the transfer but does generate the stop condition, and therefore the NM24Wxx discontinues transmission. Refer to *Figure 8* for the address, acknowledge and data transfer sequence.

Sequential Read

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted in the same manner as the other read modes; however, the master now responds with an acknowledge, indicating it requires additional data. The NM24Wxx continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge or by generating a stop condition.

The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. After the entire memory has been read, the counter 'rolls over' and the NM24Wxx continues to output data for each acknowledge received. Refer to *Figure 9* for the address, acknowledge, and data transfer sequence.

Current Address Read (Figure 7)



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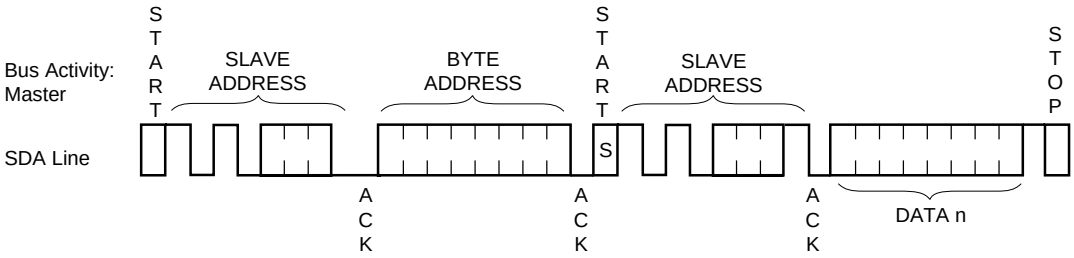
Random Read (Figure 8)



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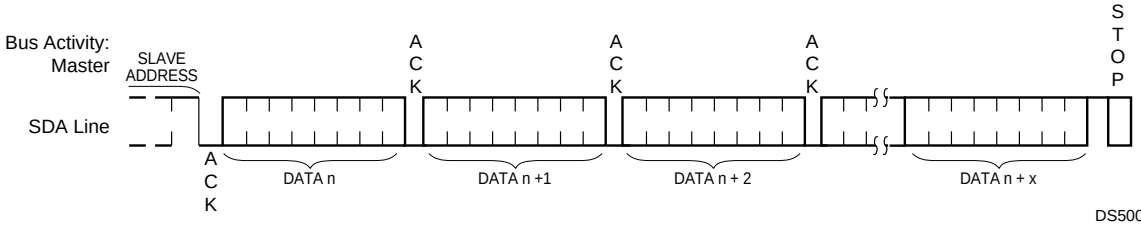
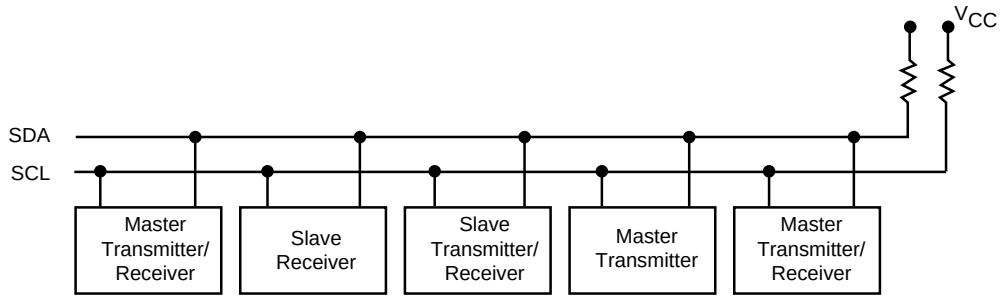
Sequential Read (Figure 9)



DS500074-16

Read Operations (Continued)

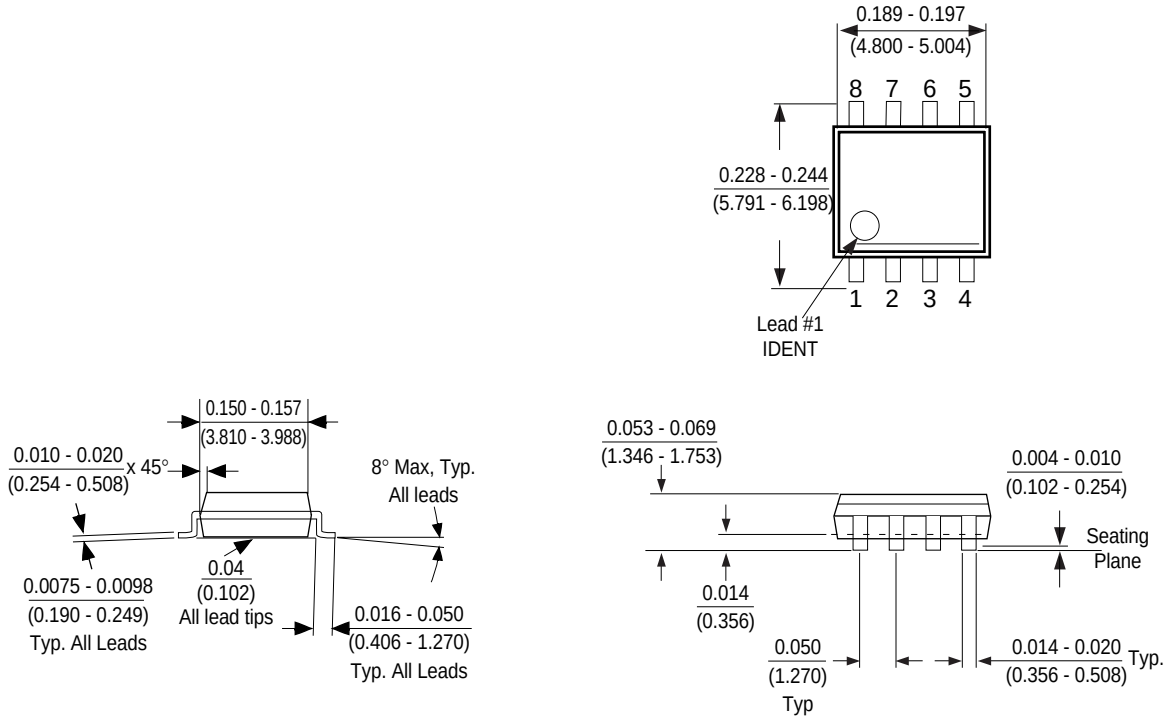
Typical System Configuration (Figure 11)



DS500074-17

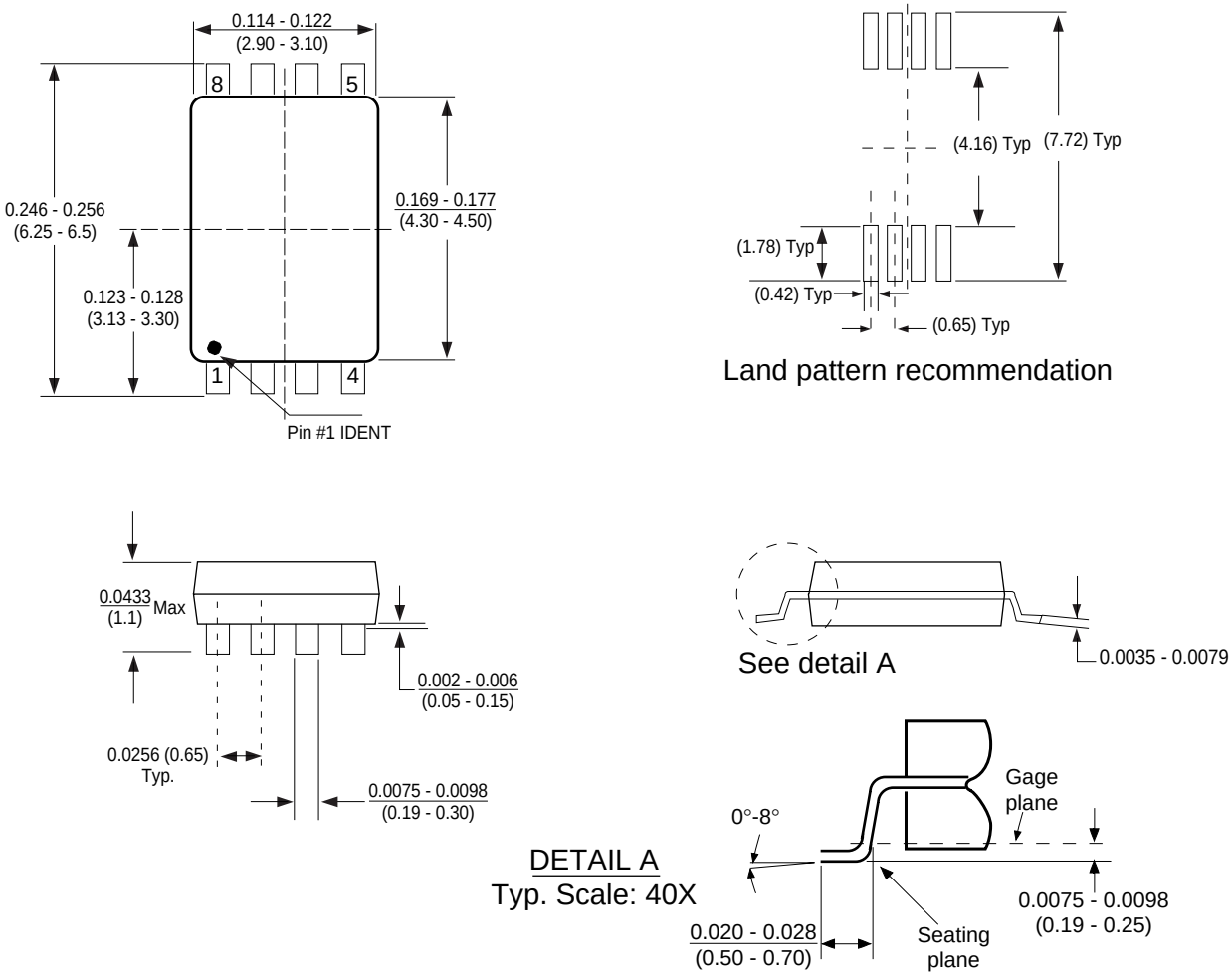
Note: Due to open drain configuration of SDA, a bus-level resistor is called for (Typical value = 4.7Ω)

Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin Molded Small Outline Package (M8)
Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted

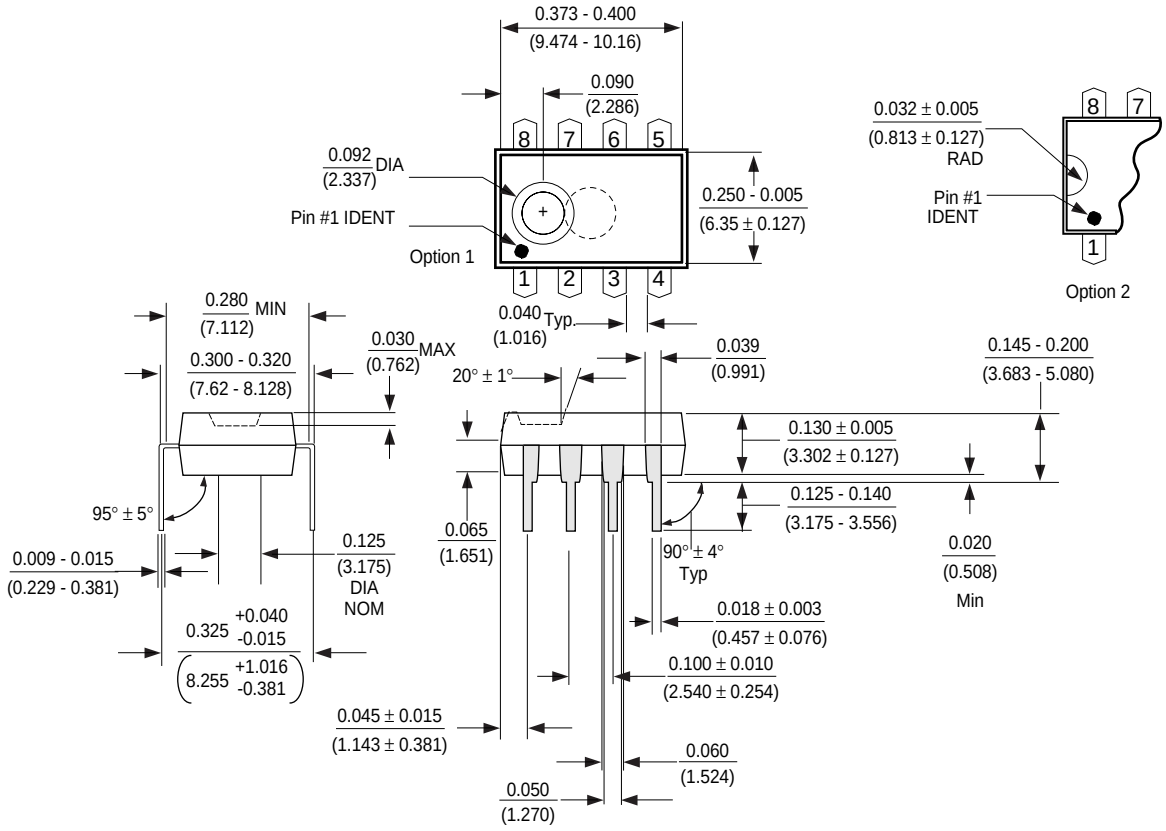


Notes: Unless otherwise specified

1. Reference JEDEC registration MO153. Variation AA. Dated 7/93

8-Pin Molded TSSOP, JEDEC
Package Number MTC08

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Package Number N08E

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FAIRCHILD
SEMICONDUCTOR™

March 1999

NM25C020
2K-Bit Serial CMOS EEPROM
(Serial Peripheral Interface (SPI) Synchronous Bus)

General Description

The NM25C020 is a 2048-bit CMOS EEPROM with an SPI compatible serial interface. The NM25C020 is designed for data storage in applications requiring both non-volatile memory and in-system data updates. This EEPROM is well suited for applications using the 68HC11 series of microcontrollers that support the SPI interface for high speed communication with peripheral devices via a serial bus to reduce pin count. The NM25C020 is implemented in Fairchild Semiconductor's floating gate CMOS process that provides superior endurance and data retention.

The serial data transmission of this device requires four signal lines to control the device operation: Chip Select ($\overline{CS}$), Clock (SCK), Data In (SI), and Serial Data Out (SO). All programming cycles are completely self-timed and do not require an erase before WRITE.

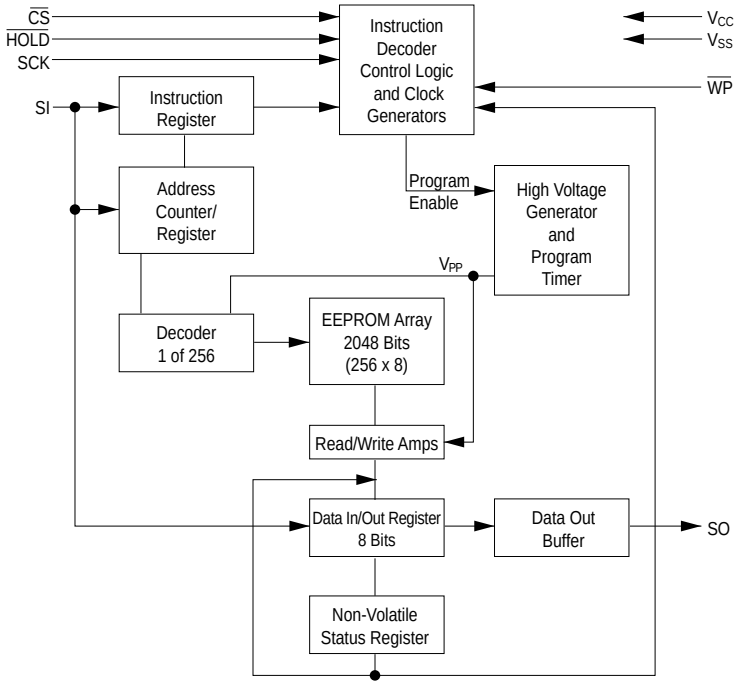
BLOCK WRITE protection is provided by programming the STATUS REGISTER with one of four levels of write protection. Additionally, separate WRITE enable and WRITE disable instructions are provided for data protection.

Hardware data protection is provided by the $\overline{WP}$ pin to protect against inadvertent programming. The $\overline{HOLD}$ pin allows the serial communication to be suspended without resetting the serial sequence.

Features

- 2.1 MHz clock rate @ 2.7V to 5.5V
- 2048 bits organized as 256 x 8
- Multiple chips on the same 3-wire bus with separate chip select lines
- Self-timed programming cycle
- Simultaneous programming of 1 to 4 bytes at a time
- Status register can be polled during programming to monitor READY/BUSY
- Write Protect ($\overline{WP}$) pin and write disable instruction for both hardware and software write protection
- Block write protect feature to protect against accidental writes
- Endurance: 1,000,000 data changes
- Data retention greater than 40 years
- Packages available: 8-pin DIP, 8-pin SO, or 8-pin TSSOP

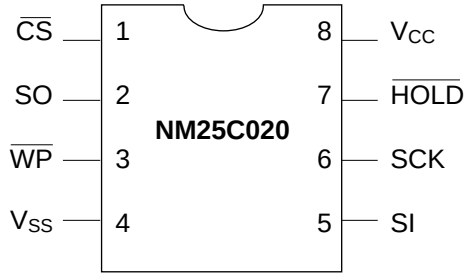
Block Diagram



DS012400-1

Connection Diagram

Dual-In-Line Package (N), SO Package (M8), and TSSOP Package (MT8)



DS012400-2

Top View
See Package Number N08E (N), M08A (M8), and MTC08 (MT8)

Pin Names

$\overline{CS}$	Chip Select Input
SO	Serial Data Output
$\overline{WP}$	Write Protect
V_{SS}	Ground
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{HOLD}$	Suspends Serial Data
V_{CC}	Power Supply

Ordering Information

NM 25 C XX LZ E XX

	Letter	Description
Package	N	8-pin DIP
	M8	8-pin SO
	MT8	8-pin TSSOP
Temp. Range	None	0 to 70°C
	V	-40 to +125°C
	E	-40 to +85°C
Voltage Operating Range	Blank	4.5V to 5.5V
	L	2.7V to 4.5V
	LZ	2.7V to 4.5V and <1µA Standby Current
Density/Mode	020	2K, mode 0
	C	CMOS technology
Interface	25	SPI
	NM	**Fairchild Nonvolatile Memory Prefix**

Standard Voltage 4.5 ≤ V_{CC} ≤ 5.5V Specifications

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM25C020	0°C to +70°C
NM25C020E	-40°C to +85°C
NM25C020V	-40°C to +125°C
Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics 4.5V ≤ V_{CC} ≤ 5.5V (unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Units
I_{CC}	Operating Current	$\overline{CS}$ = V_{IL}		3	mA
I_{CCSB}	Standby Current	$\overline{CS}$ = V_{CC}		50	µA
I_{IL}	Input Leakage	V_{IN} = 0 to V_{CC}	-1	+1	µA
I_{OL}	Output Leakage	V_{OUT} = GND to V_{CC}	-1	+1	µA
V_{IL}	CMOS Input Low Voltage		-0.3	V_{CC} * 0.3	V
V_{IH}	CMOS Input High Voltage		0.7 * V_{CC}	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -0.8 mA	V_{CC} - 0.8		V
f_{OP}	SCK Frequency			2.1	MHz
t_{RI}	Input Rise Time			2.0	µs
t_{FI}	Input Fall Time			2.0	µs
t_{CLH}	Clock High Time	(Note 2)	190		ns
t_{CLL}	Clock Low Time	(Note 2)	190		ns
t_{CSH}	Min $\overline{CS}$ High Time	(Note 3)	240		ns
t_{CSS}	$\overline{CS}$ Setup Time		240		ns
t_{DIS}	Data Setup Time		100		ns
t_{HDS}	$\overline{HOLD}$ Setup Time		90		ns
t_{CSN}	$\overline{CS}$ Hold Time		240		ns
t_{DIN}	Data Hold Time		100		ns
t_{HDN}	$\overline{HOLD}$ Hold Time		90		ns
t_{PD}	Output Delay	C_L = 200 pF		240	ns
t_{DH}	Output Hold Time		0		ns
t_{LZ}	$\overline{HOLD}$ to Output Low Z			100	ns
t_{DF}	Output Disable Time	C_L = 200 pF		240	ns
t_{HZ}	$\overline{HOLD}$ to Output High Z			100	ns
t_{WP}	Write Cycle Time	1–4 Bytes		10	ms

Capacitance T_A = 25°C, f = 2.1/1 MHz (Note 4)

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance	3	8	pF
C_{IN}	Input Capacitance	2	6	pF

AC Test Conditions

Output Load	C_L = 200 pF
Input Pulse Levels	0.1 * V_{CC} – 0.9 * V_{CC}
Timing Measurement Reference Level	0.3 * V_{CC} - .07 * V_{CC}

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The f_{OP} frequency specification specifies a minimum clock period of $1/f_{OP}$. Therefore, for every f_{OP} clock cycle, t_{CLH} + t_{CLL} must be equal to or greater than $1/f_{OP}$. For example, if the 2.1MHz period = 476ns and t_{CLH} = 190ns, t_{CLL} must be 286ns.

Note 3: $\overline{CS}$ must be brought high for a minimum of t_{CSH} between consecutive instruction cycles.

Note 4: This parameter is periodically sampled and not 100% tested.

Low Voltage 2.7V ≤ V_{CC} ≤ 4.5V Specifications

Absolute Maximum Ratings (Note 5)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM25C020L/LZ	0°C to +70°C
NM25C020LE/LZE	-40°C to +85°C
NM25C020LV	-40°C to +125°C
Power Supply (V_{CC})	2.7V–4.5V

DC and AC Electrical Characteristics 2.7V ≤ V_{CC} ≤ 4.5V (unless otherwise specified)

Symbol	Parameter	Part	Conditions	25C020L/LE 25C020LZ/LZE		25C020LV		Units
				Min.	Max.	Min	Max	
I_{CC}	Operating Current		$\overline{CS}$ = V_{IL}		3		3	mA
I_{CCSB}	Standby Current	L LZ	$\overline{CS}$ = V_{CC}		10 1		10 N/A	µA µA
I_{IL}	Input Leakage		V_{IN} = 0 to V_{CC}	-1	1	-1	1	µA
I_{OL}	Output Leakage		V_{OUT} = GND to V_{CC}	-1	1	-1	1	µA
V_{IL}	Input Low Voltage			-0.3	V_{CC} * 0.3	-0.3	V_{CC} * 0.3	V
V_{IH}	Input High Voltage			0.7 * V_{CC}	V_{CC} + 0.3	0.7 * V_{CC}	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage		I_{OL} = 0.8 mA		0.4		0.4	V
V_{OH}	Output High Voltage		I_{OH} = –0.8 mA	V_{CC} - 0.8		V_{CC} - 0.8		V
f_{OP}	SCK Frequency				1.0		1.0	MHz
t_{RI}	Input Rise Time				2.0		2.0	µs
t_{FI}	Input Fall Time				2.0		2.0	µs
t_{CLH}	Clock High Time		(Note 6)	410		410		ns
t_{CLL}	Clock Low Time		(Note 6)	410		410		ns
t_{CSH}	Min. $\overline{CS}$ High Time		(Note 7)	500		500		ns
t_{CSS}	$\overline{CS}$ Setup Time			500		500		ns
t_{DIS}	Data Setup Time			100		100		ns
t_{HDS}	$\overline{HOLD}$ Setup Time			240		240		ns
t_{CSN}	$\overline{CS}$ Hold Time			500		500		ns
t_{DIN}	Data Hold Time			100		100		ns
t_{HDN}	$\overline{HOLD}$ Hold Time			240		240		ns
t_{PD}	Output Delay		C_L = 200 pF		500		500	ns
t_{DH}	Output Hold Time			0		0		ns
t_{LZ}	$\overline{HOLD}$ Output Low Z				240		240	ns
t_{DF}	Output Disable Time		C_L = 200 pF		500		500	ns
t_{HZ}	$\overline{HOLD}$ to Output Hi Z				240		240	ns
t_{WP}	Write Cycle Time		1-4 Bytes		15		15	ms

Capacitance T_A = 25°C, f = 2.1/1 MHz (Note 8)

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance	3	8	pF
C_{IN}	Input Capacitance	2	6	pF

AC Test Conditions

Output Load	I_{OL} = 10 µA, I_{OH} = 10 µA
Input Pulse Levels	0.3V to 3.5V
Timing Measurement Reference Level	
Input	0.4V and 1.6V
Output	0.8V and 1.6V

Note 5: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

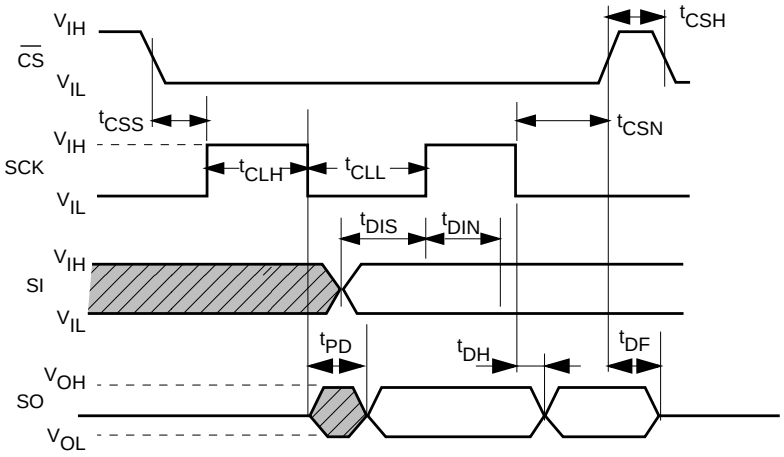
Note 6: The f_{OP} frequency specification specifies a minimum clock period of $1/f_{OP}$. Therefore, for every f_{OP} clock cycle, t_{CLH} + t_{CLL} must be equal to or greater than $1/f_{OP}$. For example, if the 2.1MHz period = 476ns and t_{CLH} = 190ns, t_{CLL} must be 286ns.

Note 7: $\overline{CS}$ must be brought high for a minimum of t_{CSH} between consecutive instruction cycles.

Note 8: This parameter is periodically sampled and not 100% tested.

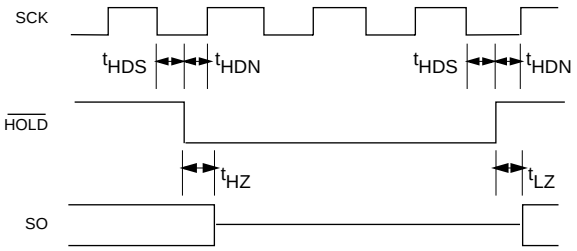
AC Test Conditions (Continued)

FIGURE 1. Synchronous Data Timing Diagram



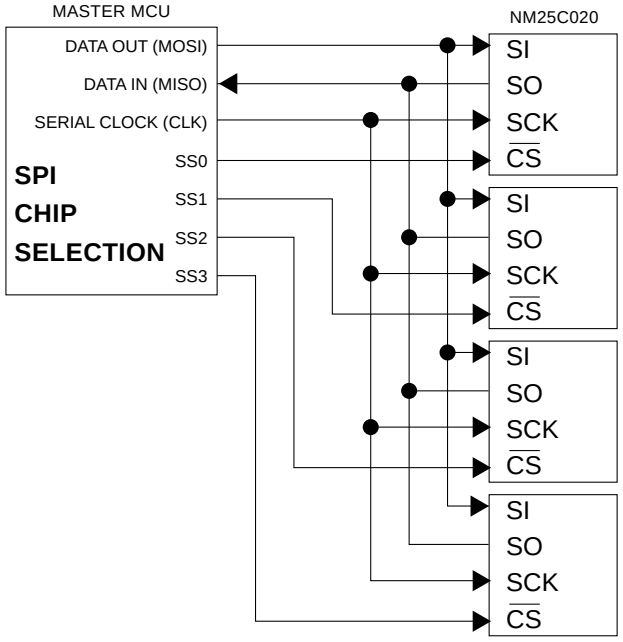
DS012400-3

FIGURE 2. HOLD Timing



DS012400-6

FIGURE 3. SPI Serial Interface



DS012400-4

Functional Description

TABLE 1. Instruction Set

Instruction Name	Instruction Opcode	Operation
WREN	00000110	Set Write Enable Latch
WRDI	00000100	Reset Write Enable Latch
RDSR	00000101	Read Status Register
WRSR	00000001	Write Status Register
READ	00000011	Read Data from Memory Array
WRITE	00000010	Write Data to Memory Array

MASTER: The device that generates the serial clock is designated as the master. The NM25C020 can never function as a master.

SLAVE: The NM25C020 always operates as a slave as the serial clock pin is always an input.

TRANSMITTER/RECEIVER: The NM25C020 has separate pins for data transmission (SO) and reception (SI).

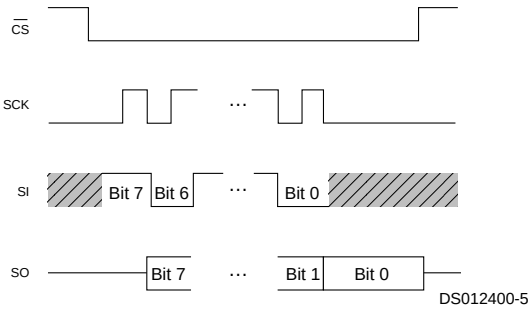
MSB: The Most Significant Bit is the first bit transmitted and received.

CHIP SELECT: The chip is selected when pin $\overline{CS}$ is low. When the chip is *not* selected, data will not be accepted from pin SI, and the output pin SO is in high impedance.

SERIAL OP-$\overline{CODE}$: The first byte transmitted after the chip is selected with CS going low contains the op-code that defines the operation to be performed.

PROTOCOL: When connected to the SPI port of a 68HC11 microcontroller, the NM25C020 accepts a clock phase of 0 and a clock polarity of 0. The SPI protocol for this device defines the byte transmitted on the SI and SO data lines for proper chip operation. See Figure 4.

FIGURE 4. SPI Protocol



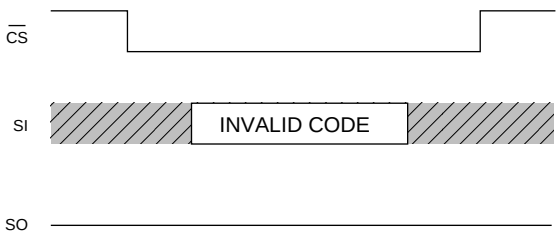
DS012400-5

Data is clocked in on the positive SCK edge and out on the negative SCK edge.

HOLD: The $\overline{HOLD}$ pin is used in conjunction with the $\overline{CS}$ to select the device. Once the device is selected and a serial sequence is underway, $\overline{HOLD}$ may be forced low to suspend further serial communication with the device without resetting the serial sequence. Note that $\overline{HOLD}$ must be brought low while the SCK pin is low. The device must remain selected during this sequence. To resume serial communication $\overline{HOLD}$ is brought high while the SCK pin is low. The SO pin is at a high impedance state during $\overline{HOLD}$.

INVALID OP-CODE: After an invalid code is received, no data is shifted into the NM25C020, and the SO data output pin remains high impedance until a new $\overline{CS}$ falling edge reinitializes the serial communication. See Figure 5.

FIGURE 5. Invalid Op-Code

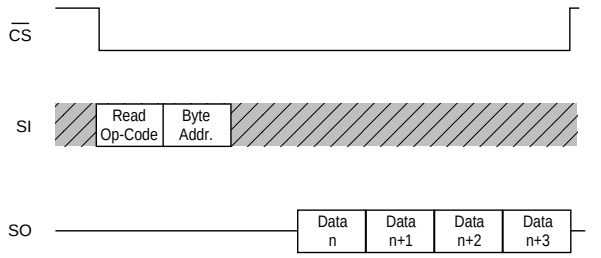


DS012400-7

Functional Description (Continued)

READ SEQUENCE: Reading the memory via the serial SPI link requires the following sequence. The $\overline{CS}$ line is pulled low to select the device. The READ op-code is transmitted on the SI line followed by the byte address (A7–A0) to be read. After this is done, data on the SI line becomes don't care. The data (D7–D0) at the address specified is then shifted out on the SO line. If only one byte is to be read, the $\overline{CS}$ line can be pulled back to the high level. It is possible to continue the READ sequence as the byte adress is automatically incremented and data will continue to be shifted out as clock pulses are continuously applied. When the highest address is reached (FF), the address counter rolls over to lowest address (000) allowing the entire memory to be read in one continuous READ cycle. See Figure 6.

FIGURE 6. Read Sequence



DS012400-8

READ STATUS REGISTER (RDSR) : The Read Status Register (RDSR) instruction provides access to the status register and is used to interrogate the READY/BUSY and WRITE ENABLE status of the chip. (Two non-volatile status register bits are used to select one of four levels of BLOCK WRITE PROTECTION.) The status register format is shown in Table 2.

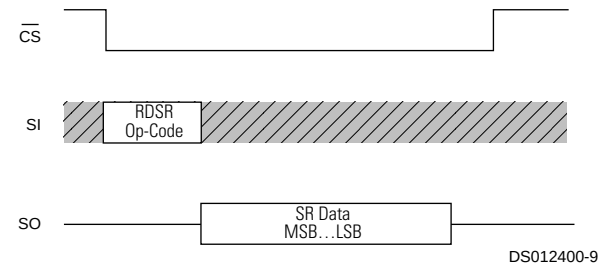
TABLE 2. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	BP1	BP0	WEN	$\overline{RDY}$

X = Don't Care

Status register Bit 0 = 0 ($\overline{RDY}$) indicates that the device is READY; Bit 0 = 1 indicates that a program cycle is in progress. Bit 1 = 0 (WEN) indicates that the device is not WRITE ENABLED; Bit 1 = 1 indicates that the device is WRITE ENABLED. Non-volatile status register Bits 2 and 3 (BP0 and BP1) indicate the level of BLOCK WRITE PROTECTION selected. The block write protection levels and corresponding status register control bits are shown in Table 3. **Note that if a RDSR instruction is executed during a programming cycle only the RDY bit is valid.** All other bits are 1s. See Figure 7.

FIGURE 7. Read Status



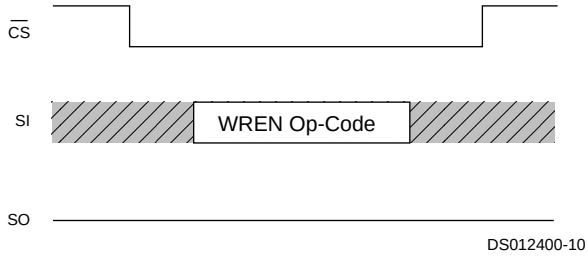
DS012400-9

TABLE 3. Block Write Protection Levels

Level	Status Register Bits		Array Address Protected
	BP1	BP0	
0	0	0	None
1	0	1	C0-FF
2	1	0	80-FF
3	1	1	00-FF

WRITE ENABLE (WREN): When V_{CC} is applied to the chip, it "powers up" in the write disable state. Therefore, all programming modes must be preceded by a WRITE ENABLE (WREN) instruction. **At the completion of a WRITE or WRSR cycle the device is automatically returned to the write disable state.** Note that a WRITE DISABLE (WRDI) instruction will also return the device to the write disable state. See Figure 8.

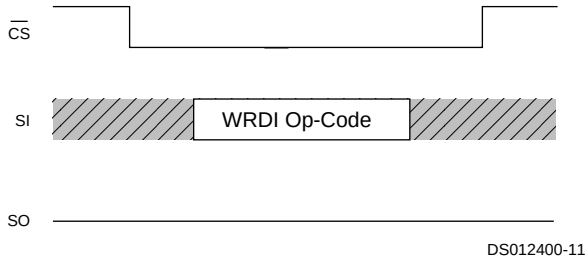
FIGURE 8. Write Enable



DS012400-10

WRITE DISABLE (WRDI): To protect against accidental data disturbance the WRITE DISABLE (WRDI) instruction disables all programming modes. See Figure 9.

FIGURE 9. Write Disable



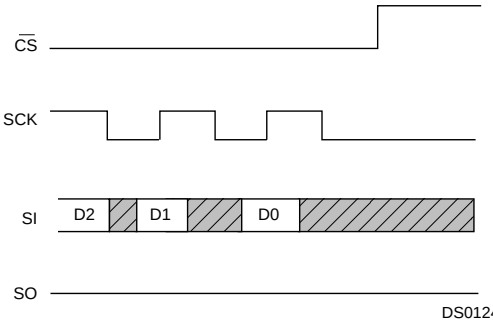
DS012400-11

WRITE SEQUENCE: **To program the device, the WRITE PROTECT ($\overline{WP}$) pin must be held high** and two separate instructions must be executed. The chip must first be write enabled via the WRITE ENABLE instruction and then a WRITE instruction must be executed. Moreover, the address of the memory location(s) to be programmed must be outside the protected address field selected by the Block Write Protection Level. See Table 3.

A WRITE command requires the following sequence. The $\overline{CS}$ line is pulled low to select the device, then the WRITE op-code is transmitted on the SI line followed by the byte address(A7–A0) and the corresponding data (D7-D0) to be written. **Programming will start after the $\overline{CS}$ pin is forced back to a high level.** Note that the LOW to HIGH transition of the $\overline{CS}$ pin must occur during the SCK low time immediately after clocking in the D0 data bit. See Figure 10.

Functional Description (Continued)

FIGURE 10. Write Sequence

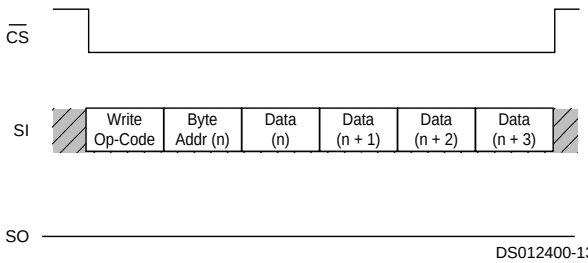


DS012400-12

The READY/BUSY status of the device can be determined by executing a READ STATUS REGISTER (RDSR) instruction. Bit 0 = 1 indicates that the WRITE cycle is still in progress and Bit 0 = 0 indicates that the WRITE cycle has ended. During the WRITE programming cycle (Bit 0 = 1) only the READ STATUS REGISTER instruction is enabled.

The NM25C020 is capable of a 4 byte PAGE WRITE operation. After receipt of each byte of data the two low order address bits are internally incremented by one. The seven high order bits of the address will remain constant. If the master should transmit more than 4 bytes of data, the address counter will "roll over," and the previously loaded data will be reloaded. See Figure 11.

FIGURE 11. 4 Byte Page Write



DS012400-13

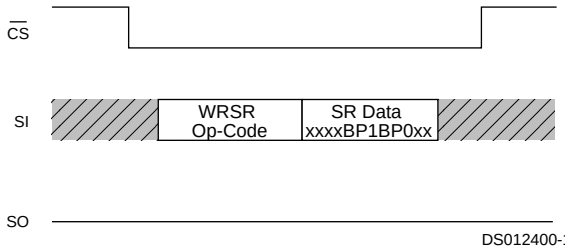
At the completion of a WRITE cycle the device is automatically returned to the write disable state.

If the device is not WRITE enabled, the device will ignore the WRITE instruction and return to the standby state when CS is forced high. A new CS falling edge is required to re-initialize the serial communication.

WRITE STATUS REGISTER (WRSR): The WRITE STATUS REGISTER (WRSR) instruction is used to program the non-volatile status register Bits 2 and 3 (BP0 and BP1). The WRITE PROTECT (WP) pin must be held high and two separate instructions must be executed. The chip must first be write enabled via the WRITE ENABLE instruction and then a WRSR instruction must be executed.

The WRSR command requires the following sequence. The CS line is pulled low to select the device and then the WRSR op-code is transmitted on the SI line followed by the data to be programmed. See Figure 12.

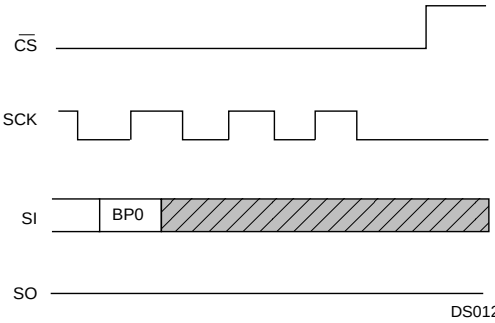
FIGURE 12. Write Status Register



DS012400-14

Note that the first four bits are don't care bits followed by BP1 and BP0 then two additional don't care bits. Programming will start after the CS pin is forced back to a high level. As in the WRITE instruction the LOW to HIGH transition of the CS pin must occur during the SCK low time immediately after clocking in the last don't care bit. See Figure 13.

FIGURE 13. Start WRSR Condition

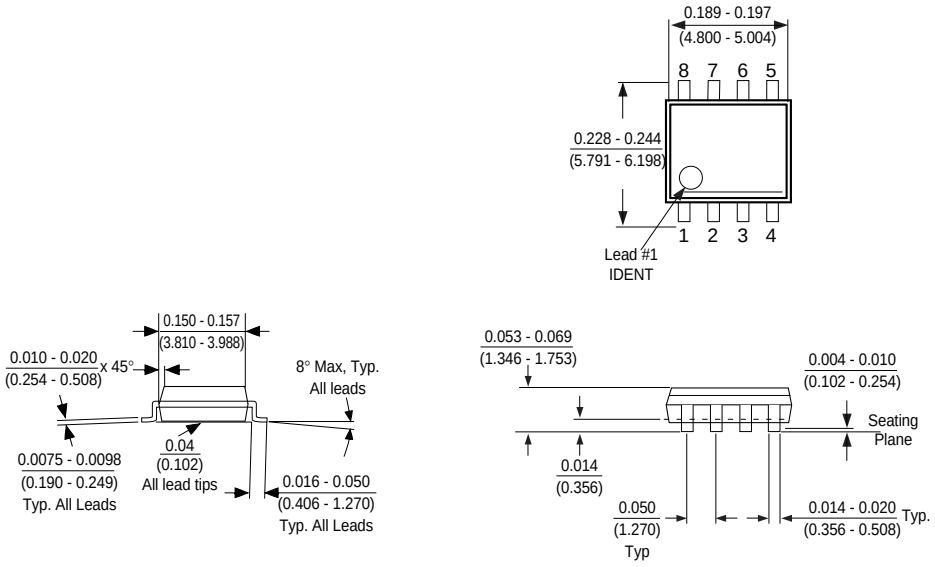


DS012400-15

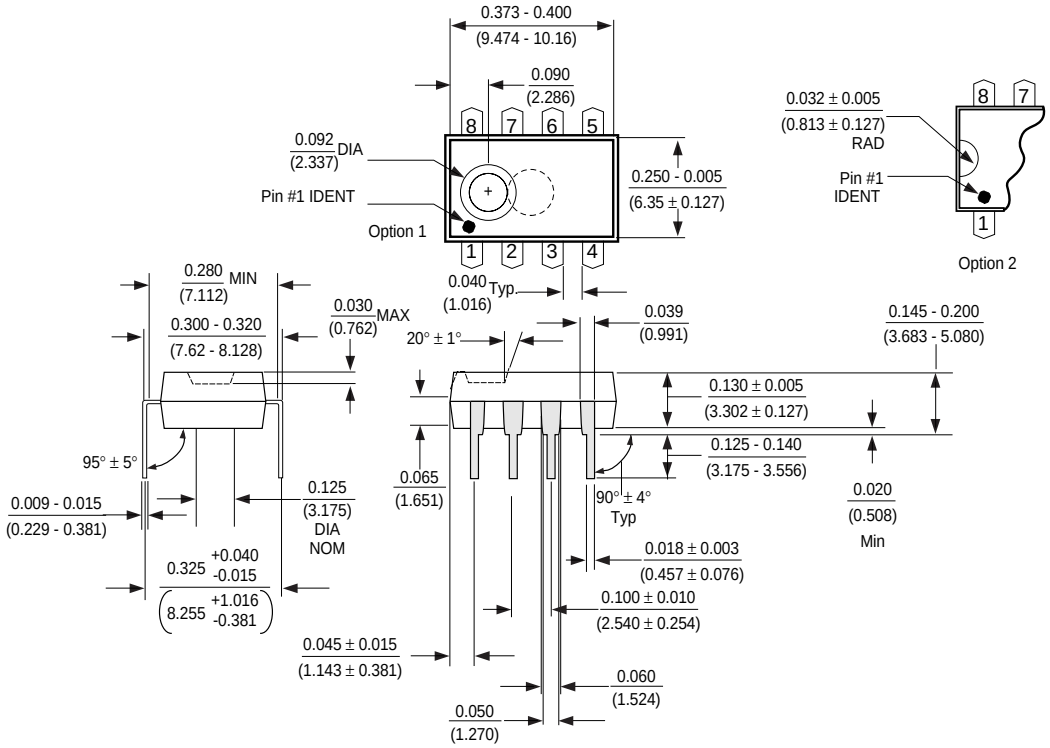
The READY/BUSY status of the device can be determined by executing a READ STATUS REGISTER (RDSR) instruction. Bit 0 = 1 indicates that the WRSR cycle is still in progress and Bit 0 = 0 indicates that the WRSR cycle has ended.

At the completion of a WRITE cycle the device is automatically returned to the write disable state.

Physical Dimensions inches (millimeters) unless otherwise noted

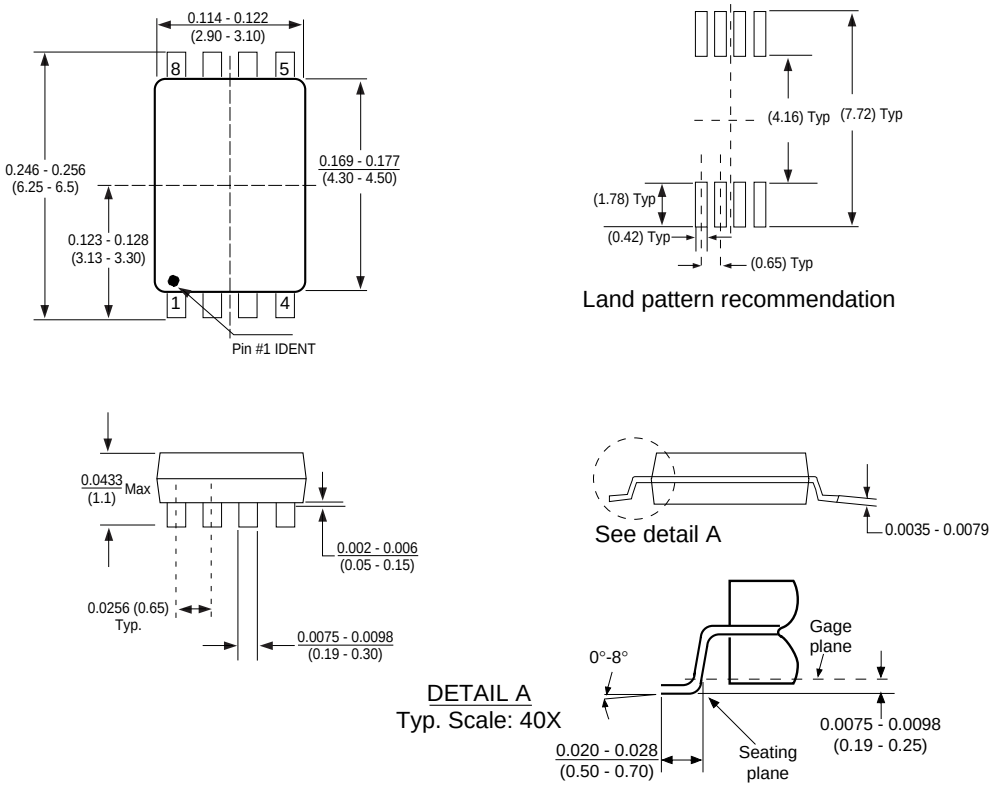


Molded Small Out-Line Package (M8)
Package Number M08A



Molded Dual-In-Line Package (N)
Package Number N08E

Physical Dimensions inches (millimeters) unless otherwise noted



Notes: Unless otherwise specified
1. Reference JEDEC registration MO153. Variation AA. Dated 7/93

8-Pin Molded TSSOP, JEDEC (MT8)
Package Number MTC08

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
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FAIRCHILD
SEMICONDUCTOR™

March 1999

NM25C040
4K-Bit Serial CMOS EEPROM
(Serial Peripheral Interface (SPI) Synchronous Bus)

General Description

The NM25C040 is a 4096-bit CMOS EEPROM with an SPI compatible serial interface. The NM25C040 is designed for data storage in applications requiring both non-volatile memory and in-system data updates. This EEPROM is well suited for applications using the 68HC11 series of microcontrollers that support the SPI interface for high speed communication with peripheral devices via a serial bus to reduce pin count. The NM25C040 is implemented in Fairchild Semiconductor's floating gate CMOS process that provides superior endurance and data retention.

The serial data transmission of this device requires four signal lines to control the device operation: Chip Select ($\overline{CS}$), Clock (SCK), Data In (SI), and Serial Data Out (SO). All programming cycles are completely self-timed and do not require an erase before WRITE.

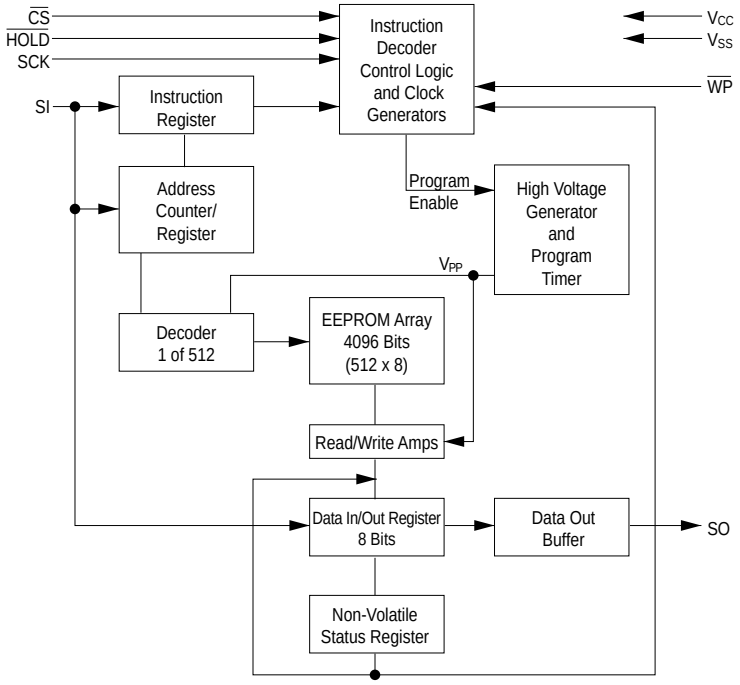
BLOCK WRITE protection is provided by programming the STATUS REGISTER with one of four levels of write protection. Additionally, separate WRITE enable and WRITE disable instructions are provided for data protection.

Hardware data protection is provided by the $\overline{WP}$ pin to protect against inadvertent programming. The $\overline{HOLD}$ pin allows the serial communication to be suspended without resetting the serial sequence.

Features

- 2.1 MHz clock rate @ 2.7V to 5.5V
- 4096 bits organized as 512 x 8
- Multiple chips on the same 3-wire bus with separate chip select lines
- Self-timed programming cycle
- Simultaneous programming of 1 to 4 bytes at a time
- Status register can be polled during programming to monitor READY/BUSY
- Write Protect ($\overline{WP}$) pin and write disable instruction for both hardware and software write protection
- Block write protect feature to protect against accidental writes
- Endurance: 1,000,000 data changes
- Data retention greater than 40 years
- Packages available: 8-pin DIP, 8-pin SO, or 8-pin TSSOP

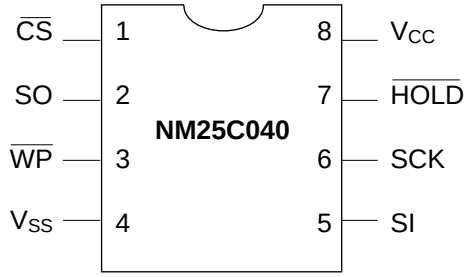
Block Diagram



DS012401-1

Connection Diagram

Dual-In-Line Package (N), SO Package (M8), and TSSOP Package (MT8)



DS012401-2

Top View
See Package Number N08E (N), M08A (M8), and MTC08 (MT8)

Pin Names

$\overline{CS}$	Chip Select Input
SO	Serial Data Output
$\overline{WP}$	Write Protect
V_{SS}	Ground
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{HOLD}$	Suspends Serial Data
V_{CC}	Power Supply

Ordering Information

NM 25 C XX LZ E XX

	Letter	Description
Package	N	8-pin DIP
	M8	8-pin SO
	MT8	8-pin TSSOP
Temp. Range	None	0 to 70°C
	V	-40 to +125°C
	E	-40 to +85°C
Voltage Operating Range	Blank	4.5V to 5.5V
	L	2.7V to 4.5V
	LZ	2.7V to 4.5V and <1µA Standby Current
Density/Mode	040	4K, mode 0
	C	CMOS technology
	W	Total Array write protect
Interface	25	SPI
	NM	**Fairchild Nonvolatile Memory Prefix**

Standard Voltage 4.5 ≤ V_{CC} ≤ 5.5V Specifications

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM25C040	0°C to +70°C
NM25C040E	-40°C to +85°C
NM25C040V	-40°C to +125°C
Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics 4.5V ≤ V_{CC} ≤ 5.5V (unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Units
I_{CC}	Operating Current	$\overline{CS}$ = V_{IL}		3	mA
I_{CCSB}	Standby Current	$\overline{CS}$ = V_{CC}		50	µA
I_{IL}	Input Leakage	V_{IN} = 0 to V_{CC}	-1	+1	µA
I_{OL}	Output Leakage	V_{OUT} = GND to V_{CC}	-1	+1	µA
V_{IL}	CMOS Input Low Voltage		-0.3	V_{CC} * 0.3	V
V_{IH}	CMOS Input High Voltage		0.7 * V_{CC}	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -0.8 mA	V_{CC} - 0.8		V
f_{OP}	SCK Frequency			2.1	MHz
t_{RI}	Input Rise Time			2.0	µs
t_{FI}	Input Fall Time			2.0	µs
t_{CLH}	Clock High Time	(Note 2)	190		ns
t_{CLL}	Clock Low Time	(Note 2)	190		ns
t_{CSH}	Min $\overline{CS}$ High Time	(Note 3)	240		ns
t_{CSS}	$\overline{CS}$ Setup Time		240		ns
t_{DIS}	Data Setup Time		100		ns
t_{HDS}	$\overline{HOLD}$ Setup Time		90		ns
t_{CSN}	$\overline{CS}$ Hold Time		240		ns
t_{DIN}	Data Hold Time		100		ns
t_{HDN}	$\overline{HOLD}$ Hold Time		90		ns
t_{PD}	Output Delay	C_L = 200 pF		240	ns
t_{DH}	Output Hold Time		0		ns
t_{LZ}	$\overline{HOLD}$ to Output Low Z			100	ns
t_{DF}	Output Disable Time	C_L = 200 pF		240	ns
t_{HZ}	$\overline{HOLD}$ to Output High Z			100	ns
t_{WP}	Write Cycle Time	1–4 Bytes		10	ms

Capacitance T_A = 25°C, f = 2.1/1 MHz (Note 4)

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance	3	8	pF
C_{IN}	Input Capacitance	2	6	pF

AC Test Conditions

Output Load	C_L = 200 pF
Input Pulse Levels	0.1 * V_{CC} – 0.9 * V_{CC}
Timing Measurement Reference Level	0.3 * V_{CC} - .07 * V_{CC}

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The f_{OP} frequency specification specifies a minimum clock period of $1/f_{OP}$. Therefore, for every f_{OP} clock cycle, t_{CLH} + t_{CLL} must be equal to or greater than $1/f_{OP}$. For example, if the 2.1MHz period = 476ns and t_{CLH} = 190ns, t_{CLL} must be 286ns.

Note 3: $\overline{CS}$ must be brought high for a minimum of t_{CSH} between consecutive instruction cycles.

Note 4: This parameter is periodically sampled and not 100% tested.

Low Voltage 2.7V ≤ V_{CC} ≤ 4.5V Specifications

Absolute Maximum Ratings (Note 5)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM25C040L/LZ	0°C to +70°C
NM25C040LE/LZE	-40°C to +85°C
NM25C040LV	-40°C to +125°C
Power Supply (V_{CC})	2.7V–4.5V

DC and AC Electrical Characteristics 2.7V ≤ V_{CC} ≤ 4.5V (unless otherwise specified)

				25C040L/LE 25C040LZ/ZE		25C040LV		
Symbol	**Parameter**	**Part**	**Conditions**	**Min.**	**Max.**	**Min**	**Max**	**Units**
I_{CC}	Operating Current		$\overline{CS}$ = V_{IL}		3		3	mA
I_{CCSB}	Standby Current	L LZ	$\overline{CS}$ = V_{CC}		10 1		10 N/A	µA µA
I_{IL}	Input Leakage		V_{IN} = 0 to V_{CC}	-1	1	-1	1	µA
I_{OL}	Output Leakage		V_{OUT} = GND to V_{CC}	-1	1	-1	1	µA
V_{IL}	Input Low Voltage			-0.3	V_{CC} * 0.3	-0.3	V_{CC} * 0.3	V
V_{IH}	Input High Voltage			V_{CC} * 0.7	V_{CC} + 0.3	V_{CC} * 0.7	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage		I_{OL} = 0.8 mA		0.4		0.4	V
V_{OH}	Output High Voltage		I_{OH} = –0.8 mA	V_{CC} - 0.8		V_{CC} - 0.8		V
f_{OP}	SCK Frequency				1.0		1.0	MHz
t_{RI}	Input Rise Time				2.0		2.0	µs
t_{FI}	Input Fall Time				2.0		2.0	µs
t_{CLH}	Clock High Time		(Note 6)	410		410		ns
t_{CLL}	Clock Low Time		(Note 6)	410		410		ns
t_{CSH}	Min. $\overline{CS}$ High Time		(Note 7)	500		500		ns
t_{CSS}	$\overline{CS}$ Setup Time			500		500		ns
t_{DIS}	Data Setup Time			100		100		ns
t_{HDS}	$\overline{HOLD}$ Setup Time			240		240		ns
t_{CSN}	$\overline{CS}$ Hold Time			500		500		ns
t_{DIN}	Data Hold Time			100		100		ns
t_{HDN}	$\overline{HOLD}$ Hold Time			240		240		ns
t_{PD}	Output Delay		C_L = 200 pF		500		500	ns
t_{DH}	Output Hold Time			0		0		ns
t_{LZ}	$\overline{HOLD}$ Output Low Z				240		240	ns
t_{DF}	Output Disable Time		C_L = 200 pF		500		500	ns
t_{HZ}	$\overline{HOLD}$ to Output Hi Z				240		240	ns
t_{WP}	Write Cycle Time		1-4 Bytes		15		15	ms

Capacitance T_A = 25°C, f = 2.1/1 MHz (Note 8)

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance	3	8	pF
C_{IN}	Input Capacitance	2	6	pF

AC Test Conditions

Output Load	C_L = 200pF
Input Pulse Levels	0.1 * V_{CC} - 0.9 * V_{CC}
Timing Measurement Reference Level	0.3 * V_{CC} - 0.7 * V_{CC}

Note 5: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

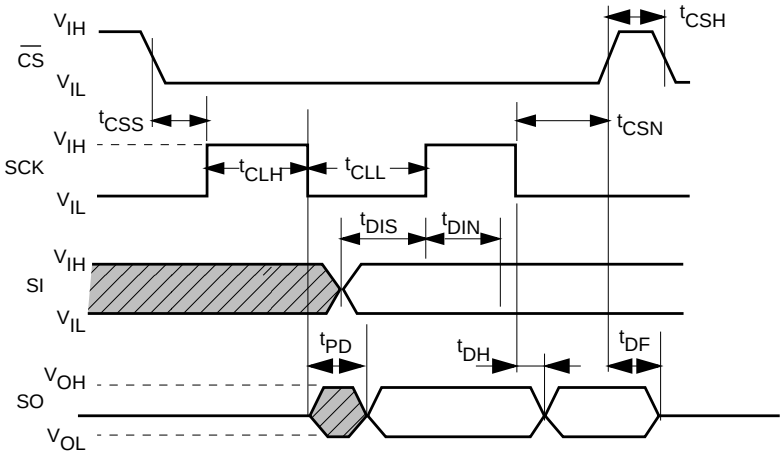
Note 6: The f_{OP} frequency specification specifies a minimum clock period of $1/f_{OP}$. Therefore, for every f_{OP} clock cycle, t_{CLH} + t_{CLL} must be equal to or greater than $1/f_{OP}$. For example, if the 2.1MHz period = 476ns and t_{CLH} = 190ns, t_{CLL} must be 286ns.

Note 7: $\overline{CS}$ must be brought high for a minimum of t_{CSH} between consecutive instruction cycles.

Note 8: This parameter is periodically sampled and not 100% tested.

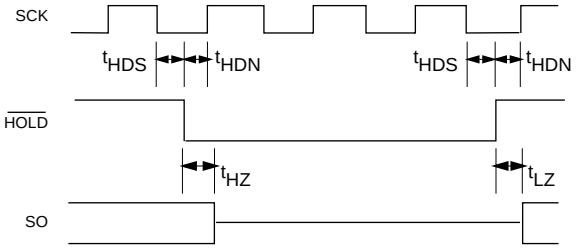
AC Test Conditions (Continued)

FIGURE 1. Synchronous Data Timing Diagram



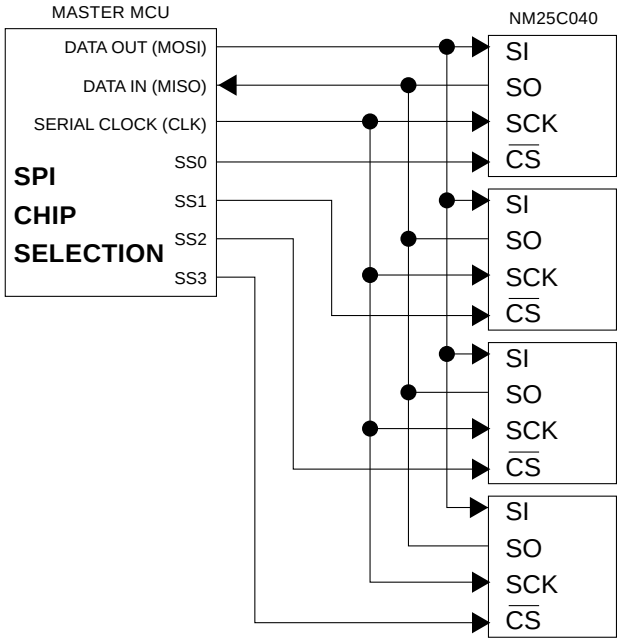
DS012401-3

FIGURE 2. HOLD Timing



DS012401-6

FIGURE 3. SPI Serial Interface



DS012401-4

Functional Description

TABLE 1. Instruction Set

Instruction Name	Instruction Opcode	Operation
WREN	00000110	Set Write Enable Latch
WRDI	00000100	Reset Write Enable Latch
RDSR	00000101	Read Status Register
WRSR	00000001	Write Status Register
READ	0000A011	Read Data from Memory Array
WRITE	0000A010	Write Data to Memory Array

Note: As the NM25C040 requires 9 address bits (4,096 ÷ 8 = 512 bytes = 2^9), the 9th bit (for R/$\overline{W}$ instructions) is inputted in the Instruction Set Byte in bit I_3. **This convention only applies to 4K SPI protocol.**

MASTER: The device that generates the serial clock is designated as the master. The NM25C040 can never function as a master.

SLAVE: The NM25C040 always operates as a slave as the serial clock pin is always an input.

TRANSMITTER/RECEIVER: The NM25C040 has separate pins for data transmission (SO) and reception (SI).

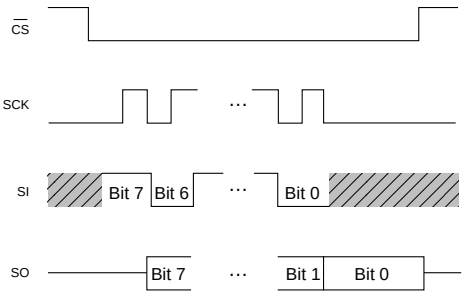
MSB: The Most Significant Bit is the first bit transmitted and received.

CHIP SELECT: The chip is selected when pin $\overline{CS}$ is low. When the chip is *not* selected, data will not be accepted from pin SI, and the output pin SO is in high impedance.

SERIAL OP-CODE: The first byte transmitted after the chip is selected with $\overline{CS}$ going low contains the op-code that defines the operation to be performed.

PROTOCOL: When connected to the SPI port of a 68HC11 microcontroller, the NM25C040 accepts a clock phase of 0 and a clock polarity of 0. The SPI protocol for this device defines the byte transmitted on the SI and SO data lines for proper chip operation. See Figure 4.

FIGURE 4. SPI Protocol



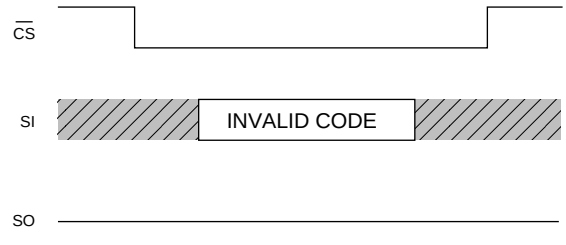
DS012401-5

Data is clocked in on the positive SCK edge and out on the negative SCK edge.

HOLD: The $\overline{HOLD}$ pin is used in conjunction with the $\overline{CS}$ to select the device. Once the device is selected and a serial sequence is underway, $\overline{HOLD}$ may be forced low to suspend further serial communication with the device without resetting the serial sequence. Note that $\overline{HOLD}$ must be brought low while the SCK pin is low. The device must remain selected during this sequence. To resume serial communication $\overline{HOLD}$ is brought high while the SCK pin is low. The SO pin is at a high impedance state during $\overline{HOLD}$.

INVALID OP-CODE: After an invalid code is received, no data is shifted into the NM25C040, and the SO data output pin remains high impedance until a new $\overline{CS}$ falling edge reinitializes the serial communication. See Figure 5.

FIGURE 5. Invalid Op-Code

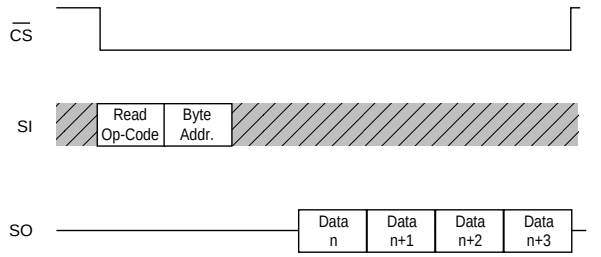


DS012401-7

Functional Description (Continued)

READ SEQUENCE: Reading the memory via the serial SPI link requires the following sequence. The $\overline{CS}$ line is pulled low to select the device. The READ op-code (which includes A8) is transmitted on the SI line followed by the byte address (A7–A0) to be read. After this is done, data on the SI line becomes don't care. The data (D7–D0) at the address specified is then shifted out on the SO line. If only one byte is to be read, the $\overline{CS}$ line can be pulled back to the high level. It is possible to continue the READ sequence as the byte adress is automatically incremented and data will continue to be shifted out. When the highest address is reached (1FF), the address counter rolls over to lowest address (000) allowing the entire memory to be read in one continuous READ cycle. See Figure 6.

FIGURE 6. Read Sequence



DS012401-8

READ STATUS REGISTER (RDSR) : The Read Status Register (RDSR) instruction provides access to the status register is used to interrogate the READY/BUSY and WRITE ENABLE status of the chip. Two non-volatile status register bits are used to select one of four levels of BLOCK WRITE PROTECTION. The status register format is shown in Table 2.

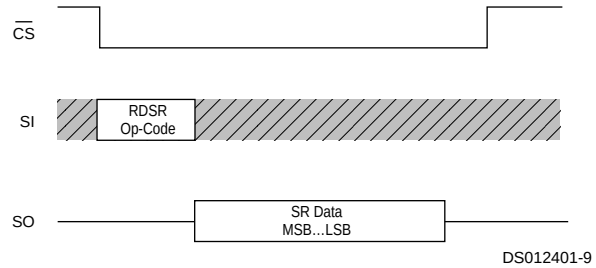
TABLE 2. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	BP1	BP0	WEN	$\overline{RDY}$

X = Don't Care.

Status register Bit 0 = 0 ($\overline{RDY}$) indicates that the device is READY; Bit 0 = 1 indicates that a program cycle is in progress. Bit 1 = 0 (WEN) indicates that the device is not WRITE ENABLED; Bit 1 = 1 indicates that the device is WRITE ENABLED. Non-volatile status register Bits 2 and 3 (BP0 and BP1) indicate the level of BLOCK WRITE PROTECTION selected. The block write protection levels and corresponding status register control bits are shown in Table 3. **Note that if a RDSR instruction is executed during a programming cycle only the $\overline{RDY}$ bit is valid. All other bits are 1s.** See Figure 7.

FIGURE 7. Read Status



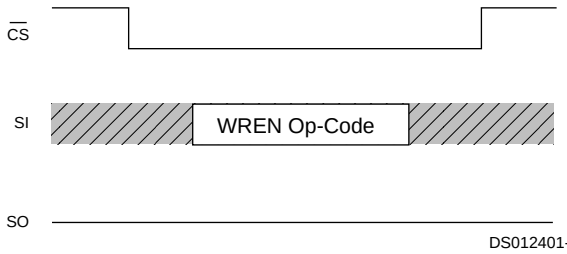
DS012401-9

TABLE 3. Block Write Protection Levels

Level	Status Register Bits		Array Address Protected
	BP1	BP0	
0	0	0	None
1	0	1	180-1FF
2	1	0	100-1FF
3	1	1	000-1FF

WRITE ENABLE (WREN): When V_{CC} is applied to the chip, it "powers up" in the write disable state. Therefore, all programming modes must be preceded by a WRITE ENABLE (WREN) instruction. At the completion of a WRITE or WRSR cycle the device is automatically returned to the write disable state. Note that a WRITE DISABLE (WRDI) instruction will also return the device to the write disable state. See Figure 8.

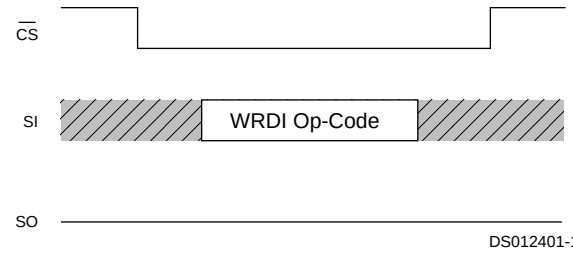
FIGURE 8. Write Enable



DS012401-10

WRITE DISABLE (WRDI): To protect against accidental data disturbance the WRITE DISABLE (WRDI) instruction disables all programming modes. See Figure 9.

FIGURE 9. Write Disable



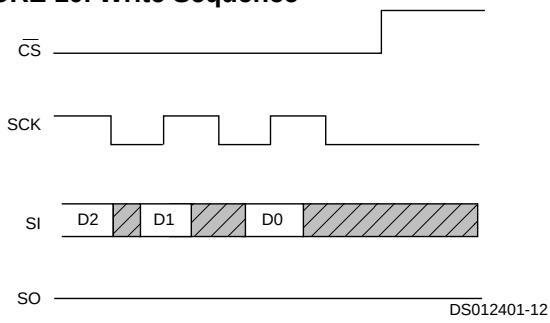
DS012401-11

WRITE SEQUENCE: To program the device, the WRITE PROTECT (WP) pin must be held high and two separate instructions must be executed. The chip must first be write enabled via the WRITE ENABLE instruction and then a WRITE instruction must be executed. Moreover, the address of the memory location(s) to be programmed must be outside the protected address field selected by the Block Write Protection Level. See Table 3.

A WRITE command requires the following sequence. The $\overline{CS}$ line is pulled low to select the device, then the WRITE op-code (which includes A8) is transmitted on the SI line followed by the high order address byte (A10-A8) and the byte address(A7–A0) and the corresponding data (D7-D0) to be written. Programming will start after the $\overline{CS}$ pin is forced back to a high level. Note that the LOW to HIGH transition of the $\overline{CS}$ pin must occur during the SCK low time immediately after clocking in the D0 data bit. See Figure 10.

Functional Description (Continued)

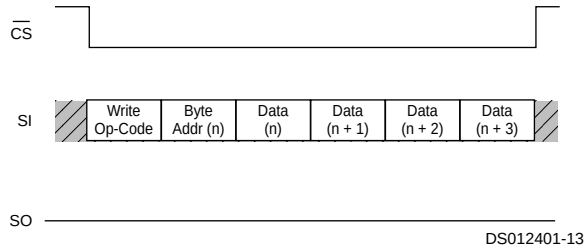
FIGURE 10. Write Sequence



The READY/BUSY status of the device can be determined by executing a READ STATUS REGISTER (RDSR) instruction. Bit 0 = 1 indicates that the WRITE cycle is still in progress and Bit 0 = 0 indicates that the WRITE cycle has ended. During the WRITE programming cycle (Bit 0 = 1) only the READ STATUS REGISTER instruction is enabled.

The NM25C040 is capable of a 4 byte PAGE WRITE operation. After receipt of each byte of data the two low order address bits are internally incremented by one. The seven high order bits of the address will remain constant. If the master should transmit more than 4 bytes of data, the address counter will "roll over," and the previously loaded data will be reloaded. See Figure 11.

FIGURE 11. 4 Byte Page Write



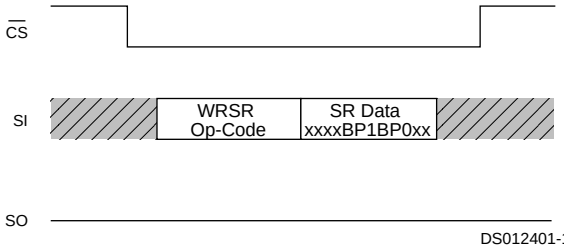
At the completion of a WRITE cycle the device is automatically returned to the write disable state.

If the device is not WRITE enabled, the device will ignore the WRITE instruction and return to the standby state when CS is forced high. A new CS falling edge is required to re-initialize the serial communication.

WRITE STATUS REGISTER (WRSR): The WRITE STATUS REGISTER (WRSR) instruction is used to program the non-volatile status register Bits 2 and 3 (BP0 and BP1). The WRITE PROTECT (WP) pin must be held high and two separate instructions must be executed. The chip must first be write enabled via the WRITE ENABLE instruction and then a WRSR instruction must be executed.

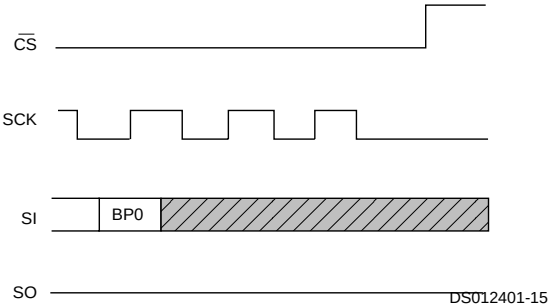
The WRSR command requires the following sequence. The CS line is pulled low to select the device and then the WRSR op-code is transmitted on the SI line followed by the data to be programmed. See Figure 12.

FIGURE 12. Write Status Register



Note that the first four bits are don't care bits followed by BP1 and BP0 then two additional don't care bits. Programming will start after the CS pin is forced back to a high level. As in the WRITE instruction the LOW to HIGH transition of the CS pin must occur during the SCK low time immediately after clocking in the last don't care bit. See Figure 13.

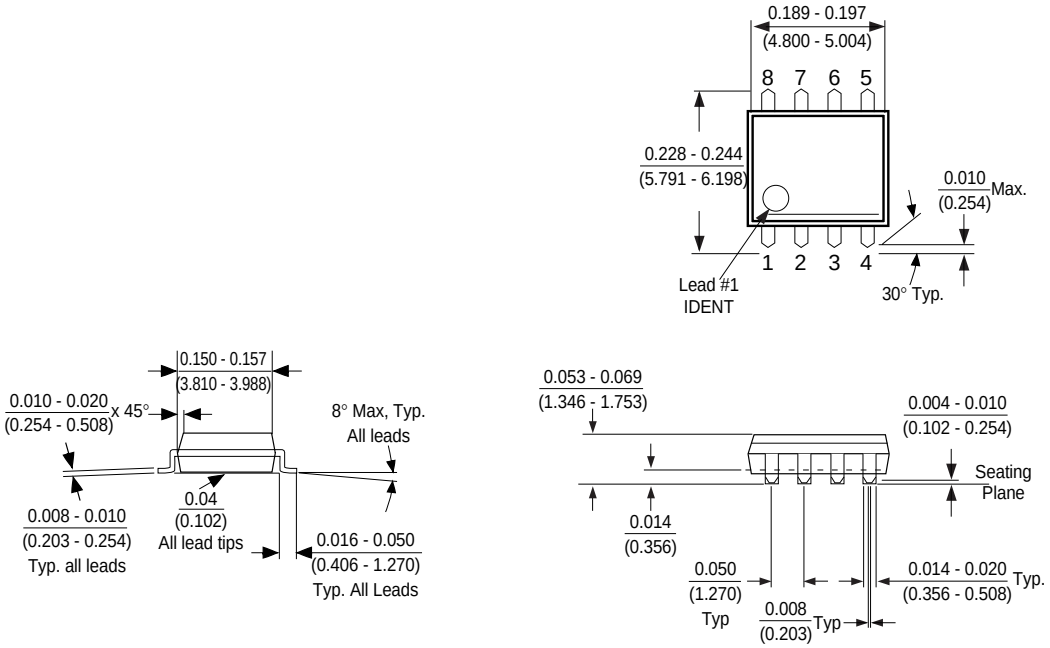
FIGURE 13. Start WRSR Condition



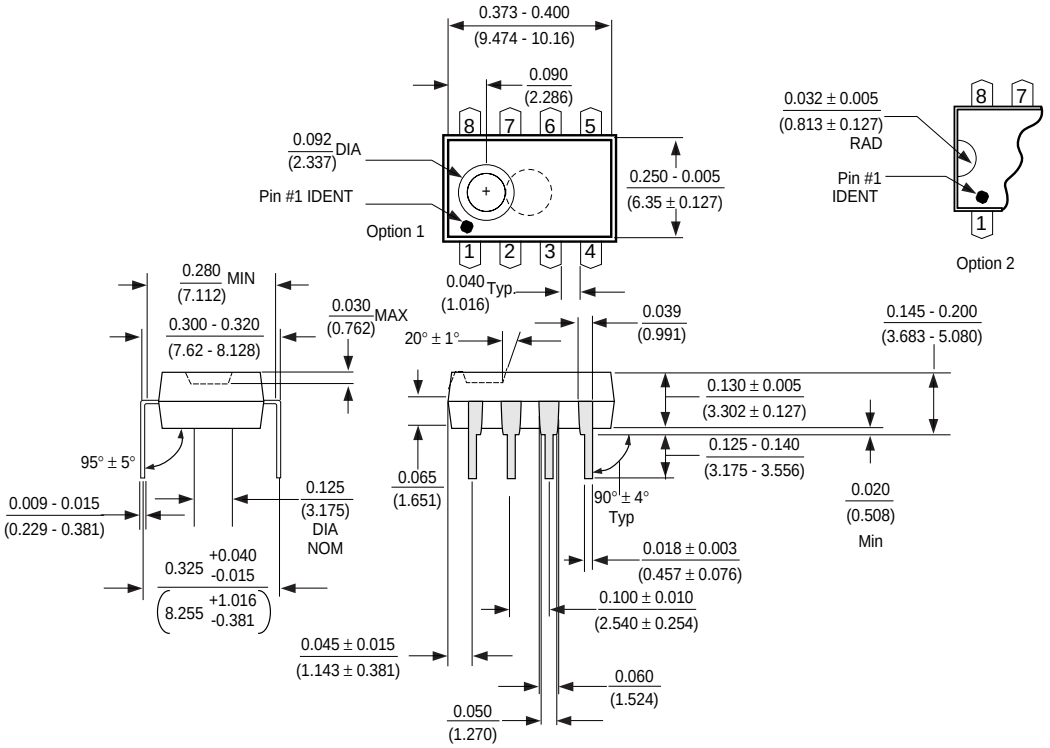
The READY/BUSY status of the device can be determined by executing a READ STATUS REGISTER (RDSR) instruction. Bit 0 = 1 indicates that the WRSR cycle is still in progress and Bit 0 = 0 indicates that the WRSR cycle has ended.

At the completion of a WRITE cycle the device is automatically returned to the write disable state.

Physical Dimensions inches (millimeters) unless otherwise noted

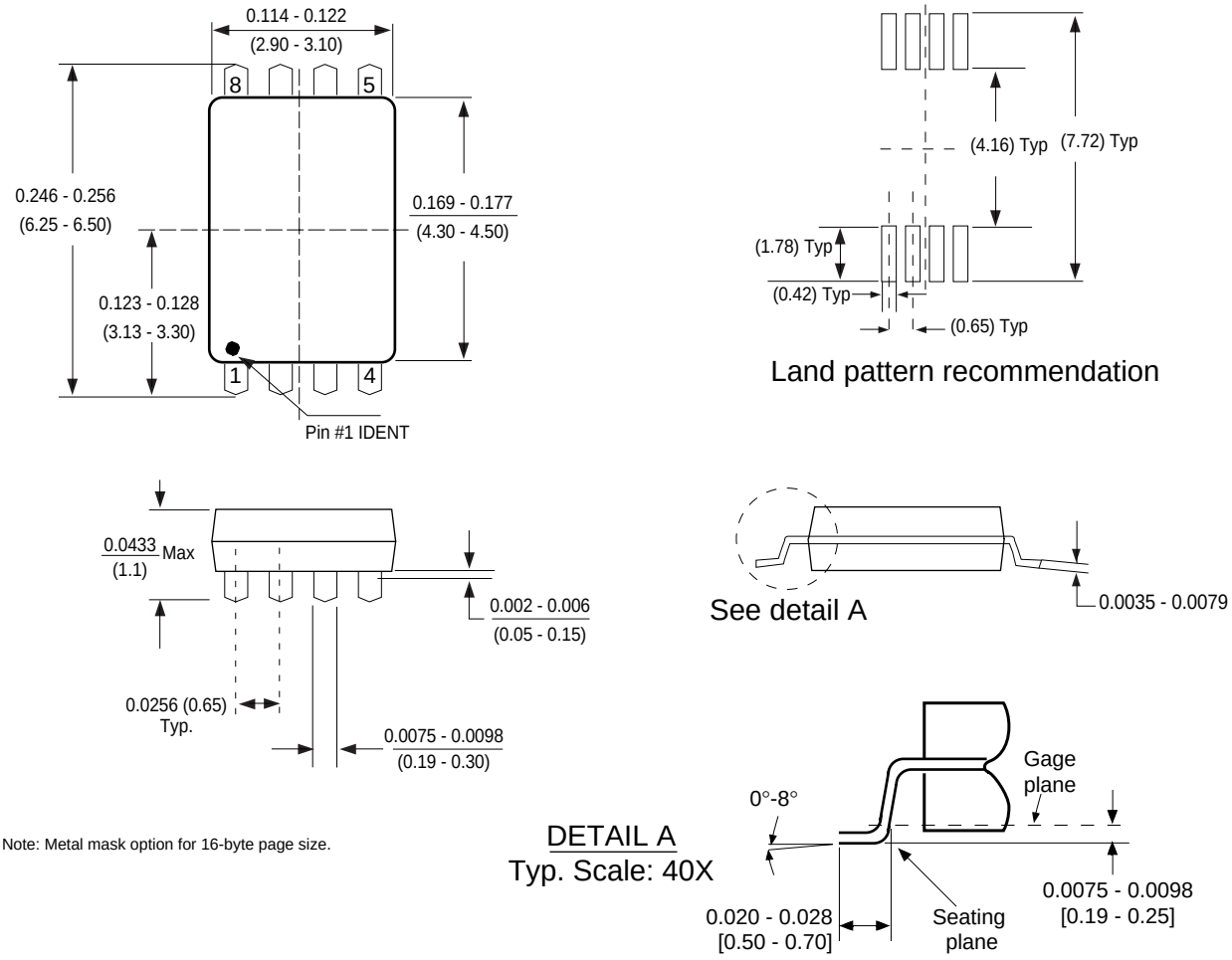


Molded Small Out-Line Package (M8)
Package Number M08A



Molded Dual-In-Line Package (N)
Package Number N08E

Physical Dimensions inches (millimeters) unless otherwise noted



Note: Metal mask option for 16-byte page size.

8-Pin Molded TSSOP, JEDEC (MT8)
Package Number MTC08

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
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FAIRCHILD
SEMICONDUCTOR™

March 1999

NM25C041
4K-Bit Serial Interface CMOS EEPROM (Serial Peripheral Interface (SPI™) Synchronous Bus)

General Description

The NM25C041 is a 4096-bit MODE 1 SPI (Serial Peripheral Interface) CMOS EEPROM which is designed for high-reliability non-volatile data storage applications. The SPI interface features a byte-wide format (all data is transferred in 8-bit words) to interface with the Motorola 68HC11 microprocessor, or equivalent, at a 2.1MHz clock transfer rate. (This interface is considered the fastest serial communication method.) This 4-wire SPI interface allows the end user full EEPROM functionality while keeping pin count and space requirements low for maximum PC board space utilization.

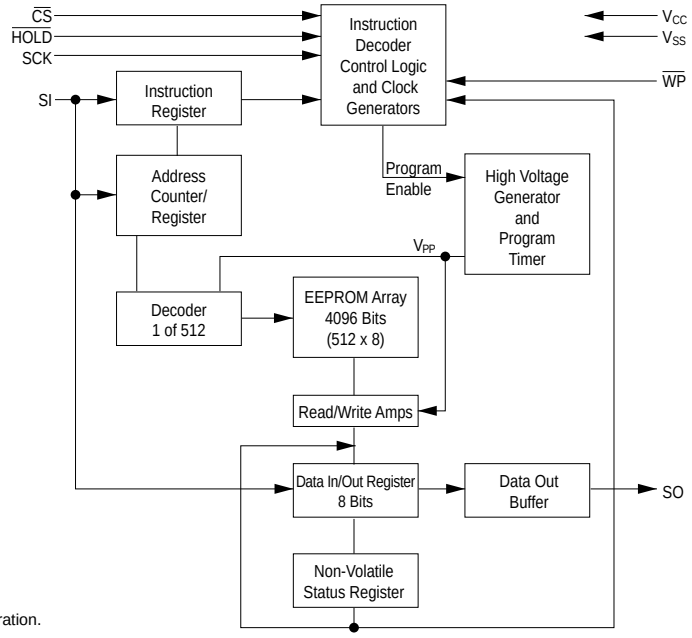
The SPI interface requires four I/O pins on each EEPROM device: Chip Select ($\overline{CS}$), Clock (SCK), Serial Data In (SI), and Serial Data Out (SO), as well as 2 other control pins: Write Protect ($\overline{WP}$) and HOLD ($\overline{HOLD}$). The Write Protect pin can be used to disable the Write operation and the $\overline{HOLD}$ pin is used to interrupt the SI datastream and place the device in a Hold state during microprocessor instruction generation. Please refer to the following diagrams and description for more details.

All programming cycles are completely self-timed and do not require an ERASE, or similar setup, before programming any cells. Programming can be performed in 3 modes, address (byte) write, page (4 addresses/bytes) write or **partial** page write. Furthermore, the EEPROM is provided with 4 levels of write protection wherein the data, once programmed, cannot be altered. This is controlled by the Status Register and is described in greater detail within this datasheet. In order to prevent spurious programming, the EEPROM has both a Write Enable command, which is immediately disabled after each programming operation, and a Write Protect (WP) pin, which must be pulled HIGH to program.

Features

- 2.1 MHz clock rate @ 2.7V to 5.5V
- 4096 bits organized as 512 x 8
- Multiple chips on the same 3 wire bus with separate chip select lines
- Self-timed programming cycle
- Simultaneous programming of 1 to 4 bytes at a time
- Status register can be polled during programming to monitor RDY/BUSY
- Both the Write Protect ($\overline{WP}$) pin and 'auto-write disable after programming' provides hardware and software write protection
- Block write protect feature to protect against accidental writes
- Endurance: 1,000,000 data changes
- Data retention greater than 40 years
- Packages available: 8-pin DIP and 8-pin SO

Block Diagram

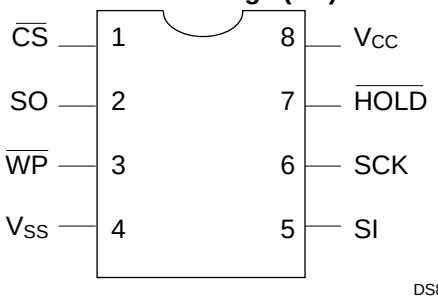


SPI™ is a trademark of Motorola Corporation.

DS800002-1

Connection Diagram

Dual-In-Line Package (N) and SO Package (M8)



DS800002-2

Top View

Pin Names

$\overline{CS}$	Chip Select Input
SO	Serial Data Output
$\overline{WP}$	Write Protect
V_{SS}	Ground
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{HOLD}$	Suspends Serial Data
V_{CC}	Power Supply

Ordering Information

NM 25 C XX LZ E XX

	Letter	Description
Package	N	8-pin DIP
	M8	8-pin SO
Temp. Range	None	0 to 70°C
	V	-40 to +125°C
	E	-40 to +85°C
Voltage Operating Range	Blank	4.5V to 5.5V
	L	2.7V to 4.5V
	LZ	2.7V to 4.5V and <1µA Standby Current
Density/Mode	041	4K, mode 1
	C	CMOS
Interface	25	SPI
	NM	**Fairchild Non-Volatile Memory**

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to -0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM25C041	0°C to +70°C
NM25C041E	-40°C to +85°C
NM25C041V	-40°C to +125°C
Power Supply (V_{CC})	
NM25C041	4.5V to 5.5V

DC and AC Electrical Characteristics $4.5V \le V_{CC} \le 5.5V$

Symbol	Parameter	Conditions	Min	Max	Units
I_{CC}	Operating Current	$\overline{CS} = V_{IL}$		3	mA
I_{CCSB}	Standby Current	$\overline{CS} = V_{CC}$		50	µA
I_{IL}	Input Leakage	V_{IN} = 0 to V_{CC}	-1	1	µA
I_{OL}	Output Leakage	V_{OUT} = GND to V_{CC}	-1	1	µA
V_{IL}	Input Low Voltage		-0.3	V_{CC} * 0.3	V
V_{IH}	Input High Voltage		0.7 * V_{CC}	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -0.8 mA	V_{CC} - 0.8		V
f_{OP}	SCK Frequency			2.1	MHz
t_{RI}	Input Rise Time			2.0	µs
t_{FI}	Input Fall Time			2.0	µs
t_{CLH}	Clock High Time	(Note 2)	190		ns
t_{CLL}	Clock Low Time	(Note 2)	190		ns
t_{CSH}	Min $\overline{CS}$ High Time	(Note 3)	240		ns
t_{CSS}	$\overline{CS}$ Setup Time		240		ns
t_{DIS}	Data Setup Time		100		ns
t_{HDS}	$\overline{HOLD}$ Setup Time		90		ns
t_{CSN}	$\overline{CS}$ Hold Time		240		ns
t_{DIN}	Data Hold Time		100		ns
t_{HDN}	$\overline{HOLD}$ Hold Time		90		ns
t_{PD}	Output Delay	C_L = 200 pF		240	ns
t_{DH}	Output Hold Time		0		ns
t_{LZ}	$\overline{HOLD}$ to Output Low Z			100	ns
t_{DF}	Output Disable Time	C_L = 200 pF		240	ns
t_{HZ}	$\overline{HOLD}$ to Output High Z			100	ns
t_{WP}	Write Cycle Time	1–4 Bytes		10	ms

Capacitance (Note 4) T_A = 25°C, f = 2.1/1 MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance	3	8	pF
C_{IN}	Input Capacitance	2	6	pF

AC Test Conditions

Output Load	C_L = 200 pF
Input Pulse Levels	0.1 * V_{CC} - 0.9 * V_{CC}
Timing Measurement Reference Level	0.3 * V_{CC} - 0.7 * V_{CC}

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The f_{OP} frequency specification specifies a minimum clock period of $1/f_{OP}$. Therefore, for every f_{OP} clock cycle, $t_{CLH} + t_{CLL}$ must be equal to or greater than $1/f_{OP}$. For example, if the 2.1MHz period = 476ns and t_{CLH} = 190ns, t_{CLL} must be 286ns.

Note 3: $\overline{CS}$ must be brought high for a minimum of t_{CSH} between consecutive instruction cycles.

Note 4: This parameter is periodically sampled and not 100% tested.

Low Voltage 2.7V ≤ V_{CC} ≤ 4.5V Specifications

Absolute Maximum Ratings (Note 5)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM25C041L/LZ	0°C to +70°C
NM25C041LE/LZE	-40°C to +85°C
NM25C041LV	-40°C to +125°C
Power Supply (V_{CC})	2.7V - 4.5V

DC and AC Electrical Characteristics 2.7V ≤ V_{CC} ≤ 4.5V

Symbol	Parameter	Conditions	25C041L/LE 25C041LZ/LZE		25C041LV		Units
			Min.	Max.	Min	Max	
I_{CC}	Operating Current	$\overline{CS}$ = V_{IL}		3		3	mA
I_{CCSB}	Standby Current L LZ	$\overline{CS}$ = V_{CC}		 10 1	µA	 10 N/A	
I_{IL}	Input Leakage	V_{IN} = 0 to V_{CC}	-1	1	-1	1	µA
I_{OL}	Output Leakage	V_{OUT} = GND to V_{CC}	-1	1	-1	1	µA
V_{IL}	Input Low Voltage		-0.3	V_{CC} * 0.3	-0.3	V_{CC} * 0.3	V
V_{IH}	Input High Voltage		0.7 * V_{CC}	V_{CC} + 0.3	0.7 * V_{CC}	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 0.8 mA		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –0.8 mA	V_{CC} - 0.8		V_{CC} - 0.8		V
f_{OP}	SCK Frequency			1.0		1.0	MHz
t_{RI}	Input Rise Time			2.0		2.0	µs
t_{FI}	Input Fall Time			2.0		2.0	µs
t_{CLH}	Clock High Time	(Note 6)	410		410		ns
t_{CLL}	Clock Low Time	(Note 6)	410		410		ns
t_{CSH}	Min. $\overline{CS}$ High Time	(Note 7)	500		500		ns
t_{CSS}	$\overline{CS}$ Setup Time		500		500		ns
t_{DIS}	Data Setup Time		100		100		ns
t_{HDS}	$\overline{HOLD}$ Setup Time		240		240		ns
t_{CSN}	$\overline{CS}$ Hold Time		500		500		ns
t_{DIN}	Data Hold Time		100		100		ns
t_{HDN}	$\overline{HOLD}$ Hold Time		240		240		ns
t_{PD}	Output Delay			500		500	ns
t_{DH}	Output Hold Time		0		0		ns
t_{LZ}	$\overline{HOLD}$ Output Low Z			240		240	ns
t_{DF}	Output Disable Time			500		500	ns
t_{HZ}	$\overline{HOLD}$ to Output Hi Z			240		240	ns
t_{WP}	Write Cycle Time	1-4 Bytes		15		15	ms

Capacitance T_A = 25°C, f = 2.1/1 MHz (Note 8)

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance	3	8	pF
C_{IN}	Input Capacitance	2	6	pF

AC Test Conditions

Output Load	C_L = 200 pF
Input Pulse Levels	0.1 * V_{CC} - 0.9 * V_{CC}
Timing Measurement Reference Level	0.3 * V_{CC} - 0.7 * V_{CC}

Note 5: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

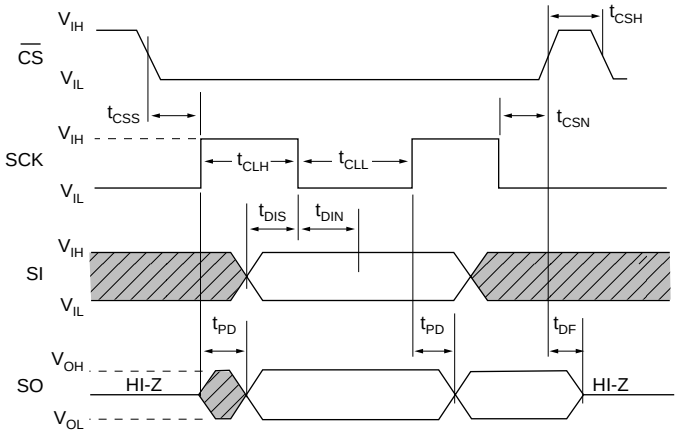
Note 6 : The f_{OP} frequency specification specifies a minimum clock period of $1/f_{OP}$. Therefore, for every f_{OP} clock cycle, t_{CLH} + t_{CLL} must be equal to or greater than $1/f_{OP}$. For example, if the 2.1MHz period = 476ns and t_{CLH} = 190ns, t_{CLL} must be 286ns.

Note 7: $\overline{CS}$ must be brought high for a minimum of t_{CSH} between consecutive instruction cycles.

Note 8: This parameter is periodically sampled and not 100% tested.

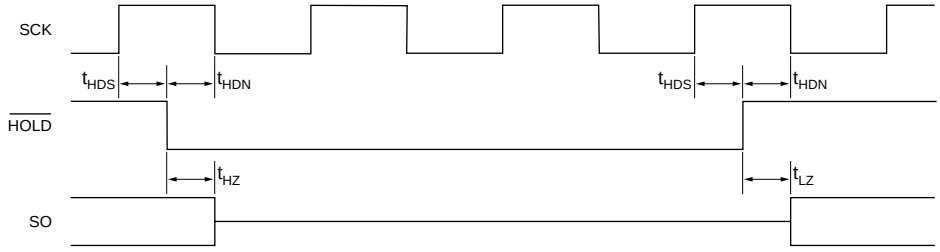
AC Test Conditions (Continued)

FIGURE 1. Synchronous Data Timing



DS800002-4

FIGURE 2. HOLD Timing



DS800002-6

Functional Description

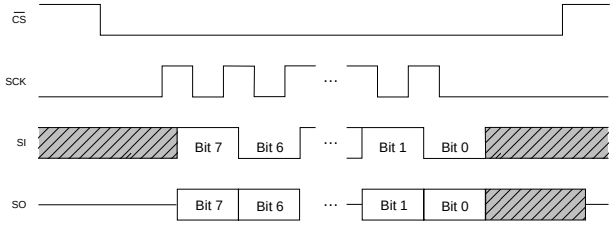
TABLE 1. Op Codes Table

Instruction Name	Instruction Opcode	Operation
WREN	0000 0110	Set Write Enable Latch
WRDI	0000 0100	Reset Write Enable Latch
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register
READ	0000 A011	Read Data from Memory Array
WRITE	0000 A010	Write Data to Memory Array

Note: As the NM25C040 requires 9 address bits (4,096 ÷ 8 = 512 bytes = 2^9), the 9th bit (for R/$\overline{W}$ instructions) is inputted in the Instruction Set Byte in bit I_3. **This convention only applies to 4K SPI protocol.**

The NM25C041 SPI device uses a $\overline{CS}$ functionality, so the device is selected when $\overline{CS}$ is LOW ($\overline{CS}$ is to be held HIGH during 'standby' periods and between instruction sets). As stated above, the SPI protocol defines this as a MODE 1 part, with a CLOCK PHASE 1 and CLOCK POLARITY 0. This means that the part is active with $\overline{CS}$ = 0 (V_{IL}), all INPUT data is latched into the device on the RISING edge of SCK and all OUTPUT data is clocked out on the FALLING edge of SCK.

FIGURE 3. SPI Protocol

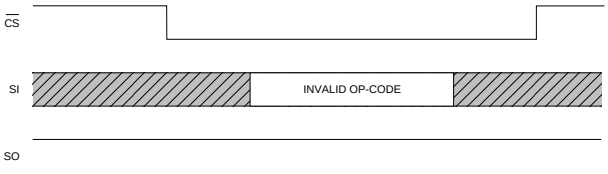


DS800002-5

The HOLD pin operation is used when the device is selected ($\overline{CS}$ LOW) and the application requires that the SI datastream be stopped and then restarted. The HOLD pin allows a fully 'static' operation, wherin the device may be put on HOLD by bringing the HOLD pin LOW (V_{IL}). During the HOLD state, SCK must be HIGH and $\overline{CS}$ must remain LOW (device selected). In order to resume EEPROM serial communication, HOLD must be again brought HIGH and the SCK/SI signals resumed. During the HOLD state, SO is tri-stated (high impedance).

As an additional protection against data corruption, the device is designed so that, if an invalid opcode is received, the device will not shift any further data into the SI latches and SO will remain tri-stated. In this case, $\overline{CS}$ must again be brought HIGH to re-initialize the device and a new opcode re-entered. See Figure 4.

FIGURE 4. Invalid Op-Code

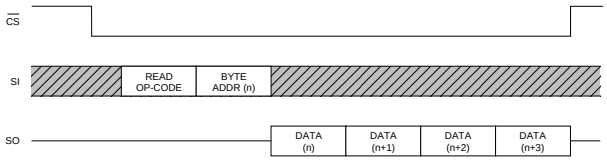


DS800002-7

READ STATUS REGISTER (RDSR): The Read Status Register (RDSR) instruction provides access to the status register which is used to interrogate the READY/BUSY and WRITE ENABLE status of the chip. Two non-volatile status register bits are used to select one of four levels of BLOCK WRITE PROTECTION. The status register format is shown in Table 2.

READ SEQUENCE: Reading the memory via the SPI link requires the following sequence. The $\overline{CS}$ line is pulled low to select the device. The READ op-code (which includes A8) is transmitted on the SI line followed by the byte address (A7–A0) to be read. After this is done, data on the SI line becomes don't care. The data (D7–D0) at the address specified is then shifted out on the SO line. If only one byte is to be read, the $\overline{CS}$ line can be pulled back to the high level. It is possible to continue the READ sequence as the byte address is automatically incremented and data will continue to be shifted out. When the highest address is reached (1FF), the address counter rolls over to lowest address (000) allowing the entire memory to be read in one continuous READ cycle. See Figure 5.

FIGURE 5. Read Sequence



DS800002-8

Functional Description (Continued)

TABLE 2. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	BP1	BP0	WEN	RDY

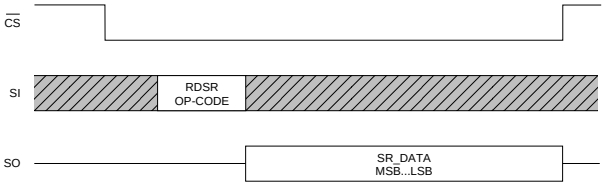
X = Don't Care

Status register Bit 0 = 0 ($\overline{RDY}$) indicates that the device is READY; Bit 0 = 1 indicates that a program cycle is in progress. Bit 1 = 0 (WEN) indicates that the device is not WRITE ENABLED; Bit 1 = 1 indicates that the device is WRITE ENABLED. Non-volatile status register Bits 2 and 3 (BP0 and BP1) indicate the level of BLOCK WRITE PROTECTION selected. The block write protection levels and corresponding status register control bits are shown in Table 3. **Note that if a RDSR instruction is executed during a programming cycle only the $\overline{RDY}$ bit is valid. All other bits are 1s.** See Figure 6.

TABLE 3. Block Write Protection Levels

Level	Status Register Bits		Array Address Protected
	BP1	BP0	
0	0	0	None
1	0	1	180–1FF
2	1	0	100–1FF
3	1	1	000–1FF

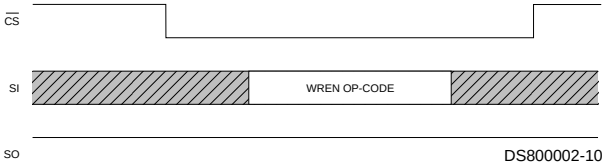
FIGURE 6. Read Status



DS800002-9

WRITE ENABLE (WREN): When V_{CC} is applied to the chip, it "powers up" in the write disable state. Therefore, all modes must be preceded by a WRITE ENABLE (WREN) instruction. Additionally the $\overline{WP}$ pin must be held high during a WRITE ENABLE instruction. At the completion of a WRITE or WRSR cycle the device is automatically turned to the write disable state. Note that a WRITE DISABLE (WRDI) instruction or forcing the $\overline{WP}$ pin low will also return the device to the write disable state. See Figure 7.

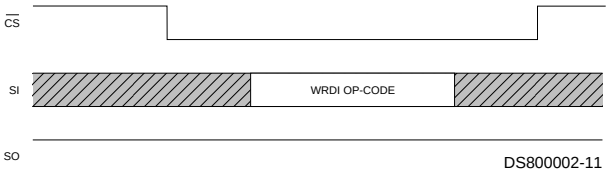
FIGURE 7. Write Enable



DS800002-10

WRITE DISABLE (WRDI): To protect against accidental data disturbance the WRITE DISABLE (WRDI) instruction disables all programming modes. The WRITE DISABLE instruction is independent of the status of the $\overline{WP}$ pin. See Figure 8.

FIGURE 8. Write Disable

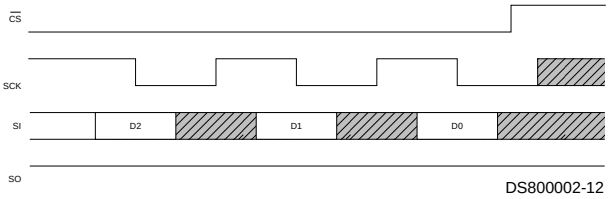


DS800002-11

WRITE SEQUENCE: To program the device the WRITE PROTECT ($\overline{WP}$) pin must be held high and two separate instructions must be executed. The chip must first be write enabled via the WRITE ENABLE instruction and then a WRITE instruction must be executed. Moreover, the address of the memory location(s) to be programmed must be outside the protected address field selected by the Block Write Protection Level. See Table 3.

A WRITE command requires the following sequence. The $\overline{CS}$ line is pulled low to select the device, then the WRITE op-code (which includes A8) is transmitted on the SI line followed by the byte address (A7–A0) and the corresponding pro-data (D7–D0) to be programmed. Programming will start after the $\overline{CS}$ pin is forced back to a high level. Note that the LOW to HIGH transition of the $\overline{CS}$ pin must occur during the SCK low time immediately after clocking in the D0 data bit. The READY/BUSY status of the device can be determined by executing a READ STATUS REGISTER (RDSR) instruction. Bit 0 = 1 indicates that the WRITE cycle is still in progress and Bit 0 = 0 indicates that the WRITE cycle has ended. During the WRITE programming cycle (Bit 0 = 1) only the READ STATUS REGISTER instruction is enabled.

FIGURE 9. Start WRITE Condition

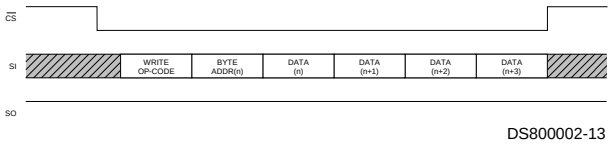


DS800002-12

Functional Description (Continued)

The NM25C041 is capable of a four byte PAGE WRITE operation. After receipt of each byte of data the two low order address bits are internally incremented by one. The seven high order bits of the address will remain constant. If the master should transmit more than four bytes of data, the address counter will "roll over", and the previously loaded data will be reloaded. See Figure 10.

FIGURE 10. 4 Page Byte Write



DS800002-13

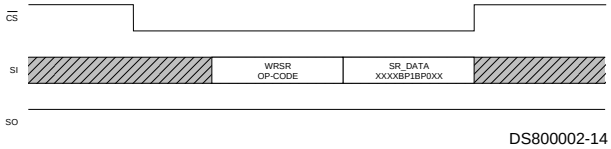
At the completion of a WRITE cycle the device is automatically returned to the write disable state.

If the WP pin is forced low or the device is not WRITE enabled, the device will ignore the WRITE instruction and return to the standby state when CS is forced high. A new CS falling edge is required to re-initialize the serial communication.

WRITE STATUS REGISTER (WRSR): The WRITE STATUS REGISTER (WRSR) instruction is used to program the non-volatile status register Bits 2 and 3 (BP0 and BP1). As in the WRITE mode the WRITE PROTECT (WP) pin must be held high and two separate instructions must be executed. The chip must first be write enabled via the WRITE ENABLE instruction and then a WRSR instruction must be executed.

The WRSR command requires the following sequence. The CS line is pulled low to select the device and then the WRSR op-code is transmitted on the SI line followed by the data to be programmed (see Figure 11).

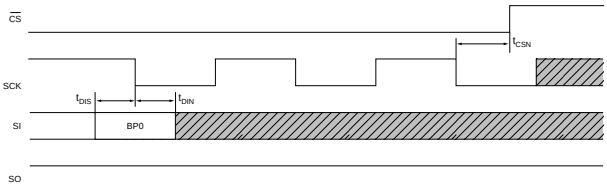
FIGURE 11. Write Status Register



DS800002-14

Note that the first four bits are don't care bits followed by BP1 and BP0 then two additional don't care bits. Programming will start after the CS pin is forced back to a high level. As in the WRITE instruction the LOW to HIGH transition of the CS pin must occur during the SCK low time immediately after clocking in the last don't care bit. See Figure 12.

FIGURE 12. Start WRSR Condition

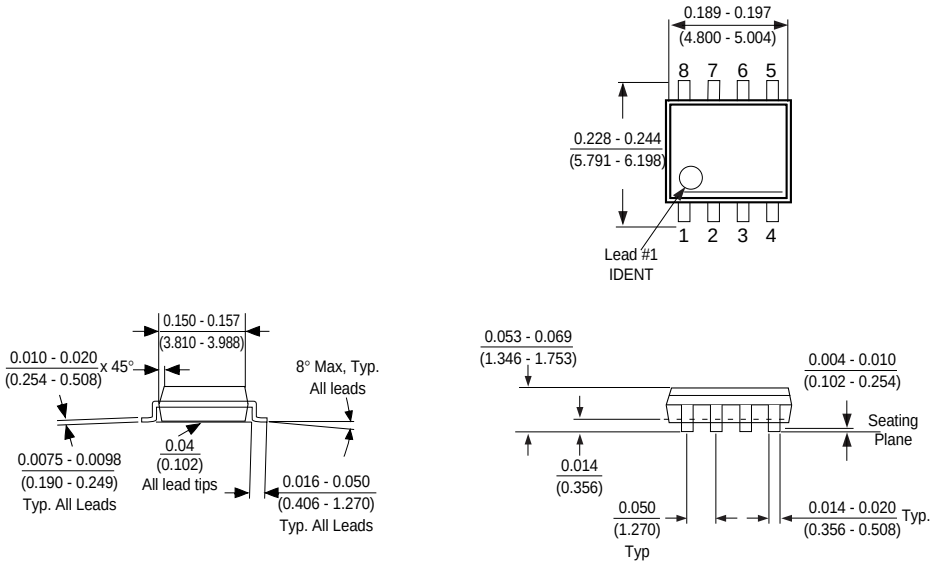


DS800002-15

The READY/BUSY status of the device can be determined by executing a READ STATUS REGISTER (RDSR) instruction. Bit 0 = 1 indicates that the WRSR cycle is still in progress and Bit 0 = 0 indicates that the WRSR cycle has ended.

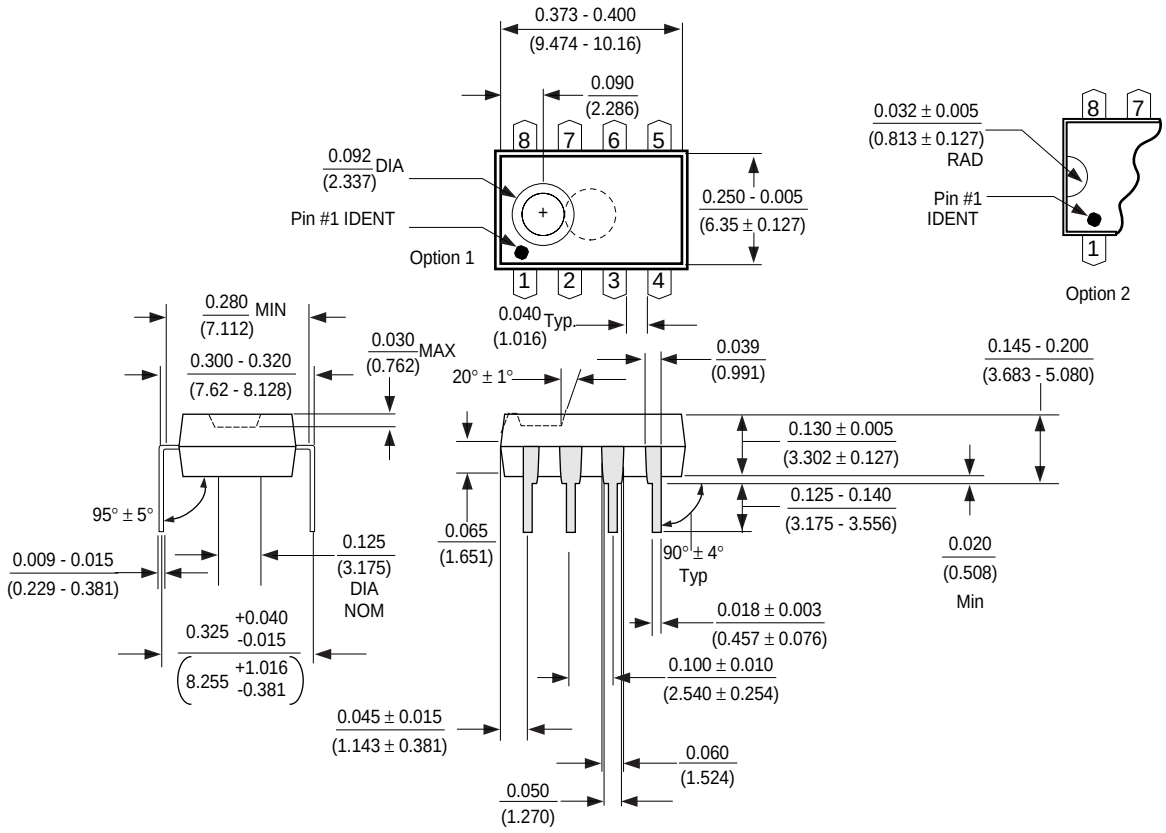
At the completion of a WRSR cycle the device is automatically returned to the write disable state.

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Small Out-Line Package (M8)
Order Number NM25C041M8
Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Order Number NM25C041N
Package Number N08E

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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March 1999

FAIRCHILD
SEMICONDUCTOR™

NM25C160
16K-Bit Serial CMOS EEPROM
(Serial Peripheral Interface (SPI) Synchronous Bus)

General Description

The NM25C160 is a 16,384-bit CMOS EEPROM with an SPI compatible serial interface. The NM25C160 is designed for data storage in applications requiring both non-volatile memory and in-system data updates. This EEPROM is well suited for applications using the 68HC11 series of microcontrollers that support the SPI interface for high speed communication with peripheral devices via a serial bus to reduce pin count. The NM25C160 is implemented in Fairchild Semiconductor's floating gate CMOS process that provides superior endurance and data retention.

The serial data transmission of this device requires four signal lines to control the device operation: Chip Select ($\overline{CS}$), Clock (SCK), Data In (SI), and Serial Data Out (SO). All programming cycles are completely self-timed and do not require an erase before WRITE.

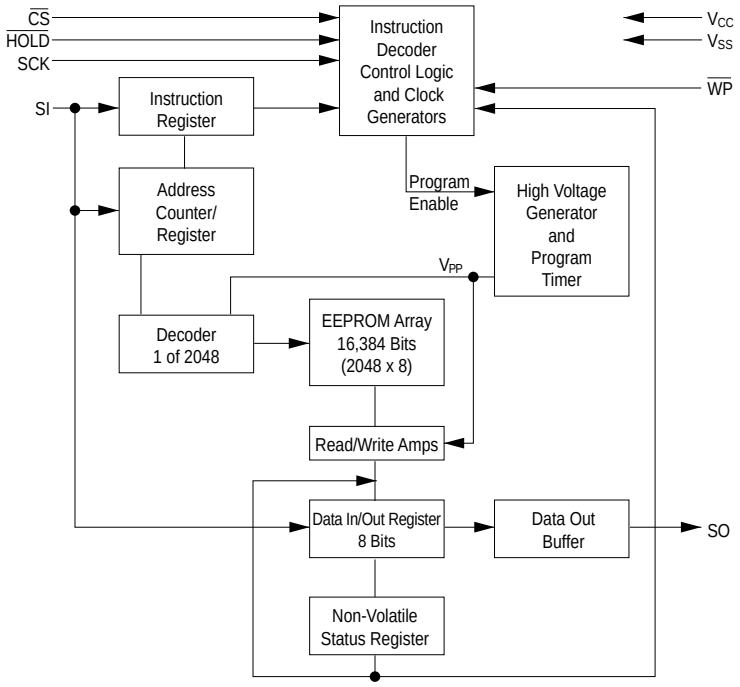
BLOCK WRITE protection is provided by programming the STATUS REGISTER with one of four levels of write protection. Additionally, separate WRITE enable and WRITE disable instructions are provided for data protection.

Hardware data protection is provided by the $\overline{WP}$ pin to protect against inadvertent programming. The $\overline{HOLD}$ pin allows the serial communication to be suspended without resetting the serial sequence.

Features

- 2.1 MHz clock rate @ 2.7V to 5.5V
- 16,384 bits organized as 2,048 x 8
- Multiple chips on the same 3-wire bus with separate chip select lines
- Self-timed programming cycle
- Simultaneous programming of 1 to 16 bytes at a time
- Status register can be polled during programming to monitor READY/BUSY
- Write Protect ($\overline{WP}$) pin and write disable instruction for both hardware and software write protection
- Block write protect feature to protect against accidental writes
- Endurance: 1,000,000 data changes
- Data retention greater than 40 years
- Packages available: 8-pin DIP, 8-pin SO, or 8-pin TSSOP

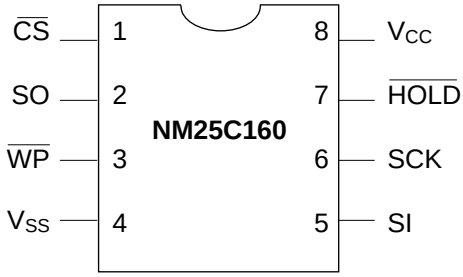
Block Diagram



DS012402-1

Connection Diagram

Dual-In-Line Package (N), SO Package (M8), and TSSOP Package (MT8)



DS012402-2

Top View
See Package Number N08E (N), M08A (M8), and MTC08 (MT8)

Pin Names

$\overline{CS}$	Chip Select Input
SO	Serial Data Output
$\overline{WP}$	Write Protect
V_{SS}	Ground
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{HOLD}$	Suspends Serial Data
V_{CC}	Power Supply

Ordering Information

NM 25 C XX LZ E XX

	Letter	Description
Package	N	8-pin DIP
	M8	8-pin SO
	MT8	8-pin TSSOP
Temp. Range	None	0 to 70°C
	V	-40 to +125°C
	E	-40 to +85°C
Voltage Operating Range	Blank	4.5V to 5.5V
	L	2.7V to 4.5V
	LZ	2.7V to 4.5V and <1µA Standby Current
Density/Mode	160	16K, mode 0
	C	CMOS technology
Interface	25	SPI
	NM	**Fairchild Nonvolatile Memory Prefix**

Standard Voltage 4.5 ≤ V_{CC} ≤ 5.5V Specifications

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM25C160	0°C to +70°C
NM25C160E	-40°C to +85°C
NM25C160V	-40°C to +125°C
Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics 4.5V ≤ V_{CC} ≤ 5.5V (unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Units
I_{CC}	Operating Current	$\overline{CS}$ = V_{IL}		3	mA
I_{CCSB}	Standby Current	$\overline{CS}$ = V_{CC}		50	µA
I_{IL}	Input Leakage	V_{IN} = 0 to V_{CC}	-1	+1	µA
I_{OL}	Output Leakage	V_{OUT} = GND to V_{CC}	-1	+1	µA
V_{IL}	CMOS Input Low Voltage		-0.3	V_{CC} * 0.3	V
V_{IH}	CMOS Input High Voltage		0.7 * V_{CC}	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -0.8 mA	V_{CC} - 0.8		V
f_{OP}	SCK Frequency			2.1	MHz
t_{RI}	Input Rise Time			2.0	µs
t_{FI}	Input Fall Time			2.0	µs
t_{CLH}	Clock High Time	(Note 2)	190		ns
t_{CLL}	Clock Low Time	(Note 2)	190		ns
t_{CSH}	Min $\overline{CS}$ High Time	(Note 3)	240		ns
t_{CSS}	$\overline{CS}$ Setup Time		240		ns
t_{DIS}	Data Setup Time		100		ns
t_{HDS}	$\overline{HOLD}$ Setup Time		90		ns
t_{CSN}	$\overline{CS}$ Hold Time		240		ns
t_{DIN}	Data Hold Time		100		ns
t_{HDN}	$\overline{HOLD}$ Hold Time		90		ns
t_{PD}	Output Delay	C_L = 200 pF		240	ns
t_{DH}	Output Hold Time		0		ns
t_{LZ}	$\overline{HOLD}$ to Output Low Z			100	ns
t_{DF}	Output Disable Time	C_L = 200 pF		240	ns
t_{HZ}	$\overline{HOLD}$ to Output High Z			100	ns
t_{WP}	Write Cycle Time	1–16 Bytes		10	ms

Capacitance T_A = 25°C, f = 2.1/1 MHz (Note 4)

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance	3	8	pF
C_{IN}	Input Capacitance	2	6	pF

AC Test Conditions

Output Load	C_L = 200 pF
Input Pulse Levels	0.1 * V_{CC} – 0.9 * V_{CC}
Timing Measurement Reference Level	0.3 * V_{CC} - 0.7 * V_{CC}

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The f_{OP} frequency specification specifies a minimum clock period of $1/f_{OP}$. Therefore, for every f_{OP} clock cycle, t_{CLH} + t_{CLL} must be equal to or greater than $1/f_{OP}$. For example, if the 2.1MHz period = 476ns and t_{CLH} = 190ns, t_{CLL} must be 286ns.

Note 3: $\overline{CS}$ must be brought high for a minimum of t_{CSH} between consecutive instruction cycles.

Note 4: This parameter is periodically sampled and not 100% tested.

Low Voltage 2.7V ≤ V_{CC} ≤ 4.5V Specifications

Absolute Maximum Ratings (Note 5)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM25C160L/LZ	0°C to +70°C
NM25C160LZ/LZE	-40°C to +85°C
NM25C160LV	-40°C to +125°C
Power Supply (V_{CC})	2.7V–4.5V

DC and AC Electrical Characteristics 2.7V ≤ V_{CC} ≤ 4.5V (unless otherwise specified)

Symbol	Parameter	Part	Conditions	25C160L/LE 25C160LZ/LZE		25C160LV		Units
				Min.	Max.	Min	Max	
I_{CC}	Operating Current		$\overline{CS}$ = V_{IL}		3		3	mA
I_{CCSB}	Standby Current	L LZ	$\overline{CS}$ = V_{CC}		10 1		10 N/A	µA µA
I_{IL}	Input Leakage		V_{IN} = 0 to V_{CC}	-1	1	-1	1	µA
I_{OL}	Output Leakage		V_{OUT} = GND to V_{CC}	-1	1	-1	1	µA
V_{IL}	Input Low Voltage			-0.3	V_{CC} * 0.3	-0.3	V_{CC} * 0.3	V
V_{IH}	Input High Voltage			0.7 * V_{CC}	V_{CC} + 0.3	0.7 * V_{CC}	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage		I_{OL} = 0.8 mA		0.4		0.4	V
V_{OH}	Output High Voltage		I_{OH} = –0.8 mA	V_{CC} - 0.8		V_{CC} - 0.8		V
f_{OP}	SCK Frequency				1.0		1.0	MHz
t_{RI}	Input Rise Time				2.0		2.0	µs
t_{FI}	Input Fall Time				2.0		2.0	µs
t_{CLH}	Clock High Time		(Note 6)	410		410		ns
t_{CLL}	Clock Low Time		(Note 6)	410		410		ns
t_{CSH}	Min. $\overline{CS}$ High Time		(Note 7)	500		500		ns
t_{CSS}	$\overline{CS}$ Setup Time			500		500		ns
t_{DIS}	Data Setup Time			100		100		ns
t_{HDS}	$\overline{HOLD}$ Setup Time			240		240		ns
t_{CSN}	$\overline{CS}$ Hold Time			500		500		ns
t_{DIN}	Data Hold Time			100		100		ns
t_{HDN}	$\overline{HOLD}$ Hold Time			240		240		ns
t_{PD}	Output Delay		C_L = 200 pF		500		500	ns
t_{DH}	Output Hold Time			0		0		ns
t_{LZ}	$\overline{HOLD}$ Output Low Z				240		240	ns
t_{DF}	Output Disable Time		C_L = 200 pF		500		500	ns
t_{HZ}	$\overline{HOLD}$ to Output Hi Z				240		240	ns
t_{WP}	Write Cycle Time		1-16 Bytes		15		15	ms

Capacitance T_A = 25°C, f = 2.1/1 MHz (Note 8)

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance	3	8	pF
C_{IN}	Input Capacitance	2	6	pF

AC Test Conditions

Output Load	I_{OL} = 10 µA, I_{OH} = 10 µA
Input Pulse Levels	0.3V to 3.5V
Timing Measurement Reference Level	
Input	0.4V and 1.6V
Output	0.8V and 1.6V

Note 5: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

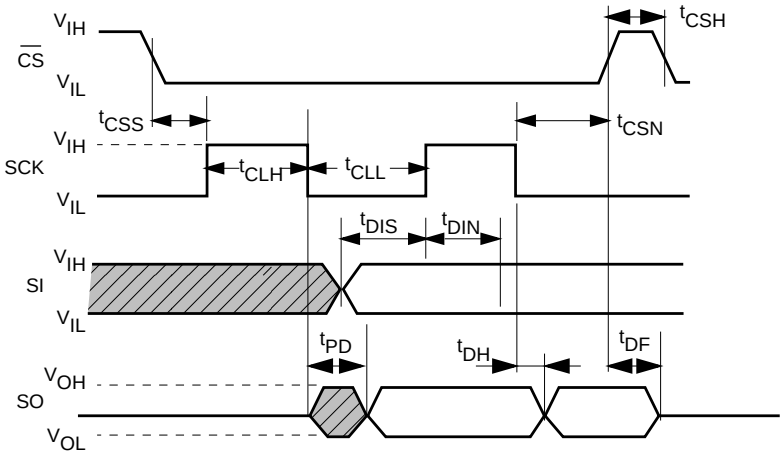
Note 6: The f_{OP} frequency specification specifies a minimum clock period of $1/f_{OP}$. Therefore, for every f_{OP} clock cycle, t_{CLH} + t_{CLL} must be equal to or greater than $1/f_{OP}$. For example, if the 2.1MHz period = 476ns and t_{CLH} = 190ns, t_{CLL} must be 286ns.

Note 7: $\overline{CS}$ must be brought high for a minimum of t_{CSH} between consecutive instruction cycles.

Note 8: This parameter is periodically sampled and not 100% tested.

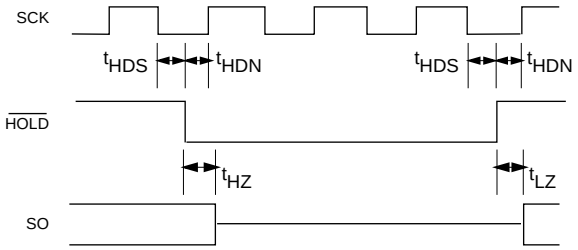
AC Test Conditions (Continued)

FIGURE 1. Synchronous Data Timing Diagram



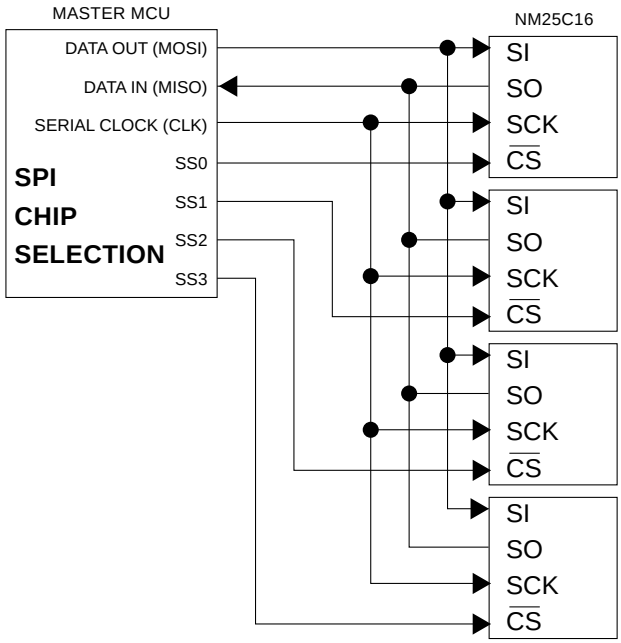
DS012402-3

FIGURE 2. HOLD Timing



DS012402-6

FIGURE 3. SPI Serial Interface



DS012402-4

Functional Description

TABLE 1. Instruction Set

Instruction Name	Instruction Opcode	Operation
WREN	00000110	Set Write Enable Latch
WRDI	00000100	Reset Write Enable Latch
RDSR	00000101	Read Status Register
WRSR	00000001	Write Status Register
READ	00000011	Read Data from Memory Array
WRITE	00000010	Write Data to Memory Array

MASTER: The device that generates the serial clock is designated as the master. The NM25C160 can never function as a master.

SLAVE: The NM25C160 always operates as a slave as the serial clock pin is always an input.

TRANSMITTER/RECEIVER: The NM25C160 has separate pins for data transmission (SO) and reception (SI).

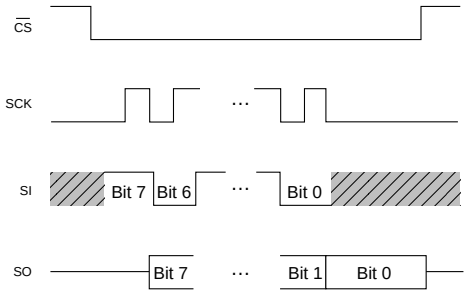
MSB: The Most Significant Bit is the first bit transmitted and received.

CHIP SELECT: The chip is selected when pin $\overline{CS}$ is low. When the chip is *not* selected, data will not be accepted from pin SI, and the output pin SO is in high impedance.

SERIAL OP-CODE: The first byte transmitted after the chip is selected with $\overline{CS}$ going low contains the op-code that defines the operation to be performed.

PROTOCOL: When connected to the SPI port of a 68HC11 microcontroller, the NM25C160 accepts a clock phase of 0 and a clock polarity of 0. The SPI protocol for this device defines the byte transmitted on the SI and SO data lines for proper chip operation. See Figure 4.

FIGURE 4. SPI Protocol



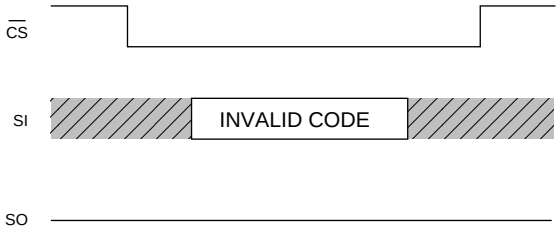
DS012402-5

Data is clocked in on the positive SCK edge and out on the negative SCK edge.

HOLD: The $\overline{HOLD}$ pin is used in conjunction with the $\overline{CS}$ to select the device. Once the device is selected and a serial sequence is underway, $\overline{HOLD}$ may be forced low to suspend further serial communication with the device without resetting the serial sequence. Note that $\overline{HOLD}$ must be brought low while the SCK pin is low. The device must remain selected during this sequence. To resume serial communication $\overline{HOLD}$ is brought high while the SCK pin is low. The SO pin is at a high impedance state during $\overline{HOLD}$.

INVALID OP-CODE: After an invalid code is received, no data is shifted into the NM25C160, and the SO data output pin remains high impedance until a new $\overline{CS}$ falling edge reinitializes the serial communication. See Figure 5.

FIGURE 5. Invalid Op-Code

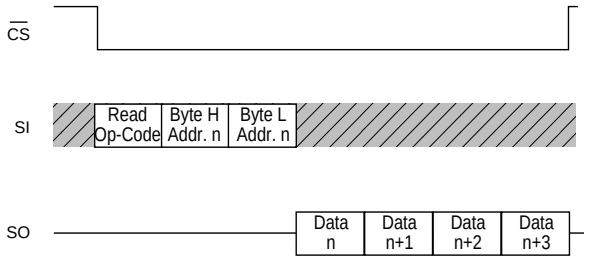


DS012402-7

Functional Description (Continued)

READ SEQUENCE: Reading the memory via the serial SPI link requires the following sequence. The $\overline{CS}$ line is pulled low to select the device. The READ op-code is transmitted on the SI line followed by the high order address byte (A10–A8), and the low order address byte (A7–A0). The leading three bits in the high order address byte will be ignored. After this is done, data on the SI line becomes don't care. The data (D7–D0) at the address specified is then shifted out on the SO line. If only one byte is to be read, the $\overline{CS}$ line can be pulled back to the high level. It is possible to continue the READ sequence as the byte adress is automatically incremented and data will continue to be shifted out. When the highest address is reached (7FF), the address counter rolls over to lowest address (000) allowing the entire memory to be read in one continuous READ cycle. See Figure 6.

FIGURE 6. Read Sequence



DS012402-8

READ STATUS REGISTER (RDSR) : The Read Status Register (RDSR) instruction provides access to the status register is used to interrogate the READY/BUSY and WRITE ENABLE status of the chip. Two non-volatile status register bits are used to select one of four levels of BLOCK WRITE PROTECTION. The status register format is shown in Table 2.

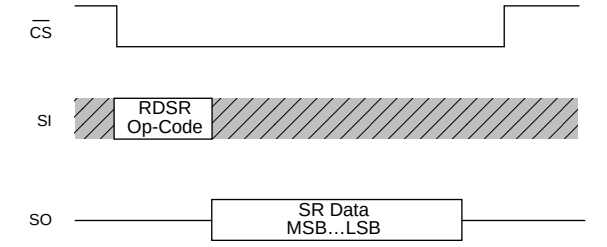
TABLE 2. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	BP1	BP0	WEN	$\overline{RDY}$

X = Don't Care

Status register Bit 0 = 0 ($\overline{RDY}$) indicates that the device is READY; Bit 0 = 1 indicates that a program cycle is in progress. Bit 1 = 0 (WEN) indicates that the device is not WRITE ENABLED; Bit 1 = 1 indicates that the device is WRITE ENABLED. Non-volatile status register Bits 2 and 3 (BP0 and BP1) indicate the level of BLOCK WRITE PROTECTION selected. The block write protection levels and corresponding status register control bits are shown in Table 3. **Note that if a RDSR instruction is executed during a programming cycle only the $\overline{RDY}$ bit is valid. All other bits are 1s.** See Figure 7.

FIGURE 7. Read Status



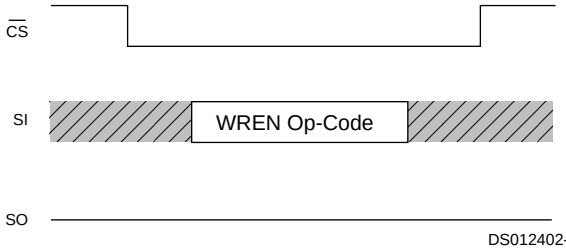
DS012402-9

TABLE 3. Block Write Protection Levels

Level	Status Register Bits		Array Address Protected
	BP1	BP0	
0	0	0	None
1	0	1	600-7FF
2	1	0	400-7FF
3	1	1	000-7FF

WRITE ENABLE (WREN): When V_{CC} is applied to the chip, it "powers up" in the write disable state. Therefore, all programming modes must be preceded by a WRITE ENABLE (WREN) instruction. At the completion of a WRITE or WRSR cycle the device is automatically returned to the write disable state. Note that a WRITE DISABLE (WRDI) instruction will also return the device to the write disable state. See Figure 8.

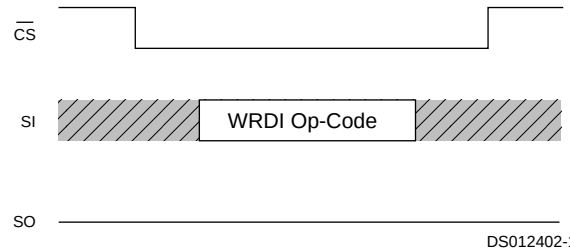
FIGURE 8. Write Enable



DS012402-10

WRITE DISABLE (WRDI): To protect against accidental data disturbance the WRITE DISABLE (WRDI) instruction disables all programming modes. See Figure 9.

FIGURE 9. Write Disable



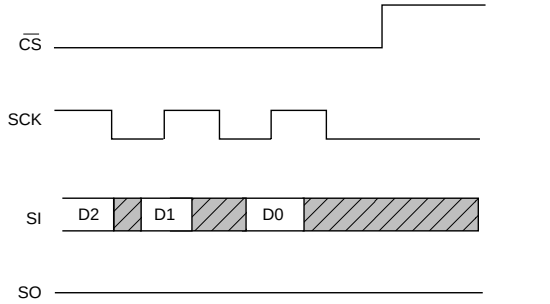
DS012402-11

WRITE SEQUENCE: To program the device, the WRITE PROTECT ($\overline{WP}$) pin must be held high and two separate instructions must be executed. The chip must first be write enabled via the WRITE ENABLE instruction and then a WRITE instruction must be executed. Moreover, the address of the memory location(s) to be programmed must be outside the protected address field selected by the Block Write Protection Level. See Table 3.

Functional Description (Continued)

A WRITE command requires the following sequence. The $\overline{CS}$ line is pulled low to select the device, then the WRITE op-code is transmitted on the SI line followed by the high order address byte (A10-A8) and the low order address byte (A7–A0). The leading five bits in the high order address byte will be ignored. The address is followed by the data (D7–D0) to be written. Programming will start after the $\overline{CS}$ pin is forced back to a high level. Note that the LOW to HIGH transition of the $\overline{CS}$ pin must occur during the SCK low time immediately after clocking in the D0 data bit. See Figure 10.

FIGURE 10. Write Sequence

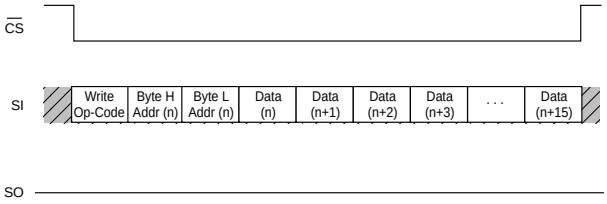


DS012402-12

The READY/BUSY status of the device can be determined by executing a READ STATUS REGISTER (RDSR) instruction. Bit 0 = 1 indicates that the WRITE cycle is still in progress and Bit 0 = 0 indicates that the WRITE cycle has ended. During the WRITE programming cycle (Bit 0 = 1) only the READ STATUS REGISTER instruction is enabled.

The NM25C160 is capable of a 16 byte PAGE WRITE operation. After receipt of each byte of data the four low order address bits are internally incremented by one. The seven high order bits of the address will remain constant. If the master should transmit more than 16 bytes of data, the address counter will "roll over," and the previously loaded data will be reloaded. See Figure 11.

FIGURE 11. 16 Byte Page Write



DS012402-13

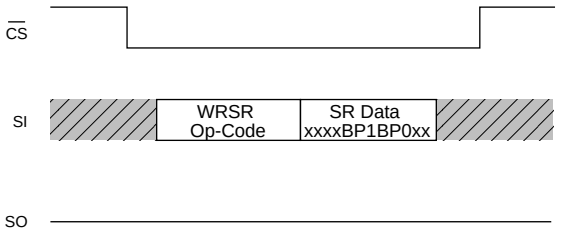
At the completion of a WRITE cycle the device is automatically returned to the write disable state.

If the device is not WRITE enabled, the device will ignore the WRITE instruction and return to the standby state when $\overline{CS}$ is forced high. A new $\overline{CS}$ falling edge is required to re-initialize the serial communication.

WRITE STATUS REGISTER (WRSR): The WRITE STATUS REGISTER (WRSR) instruction is used to program the non-volatile status register Bits 2 and 3 (BP0 and BP1). The WRITE PROTECT ($\overline{WP}$) pin must be held high and two separate instructions must be executed. The chip must first be write enabled via the WRITE ENABLE instruction and then a WRSR instruction must be executed.

The WRSR command requires the following sequence. The $\overline{CS}$ line is pulled low to select the device and then the WRSR op-code is transmitted on the SI line followed by the data to be programmed. See Figure 12.

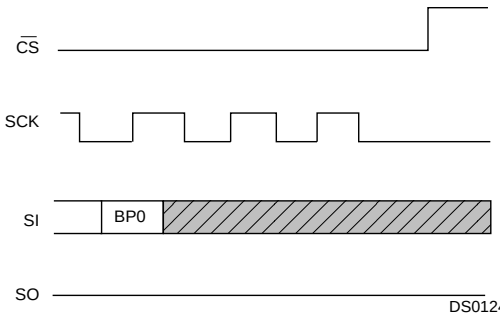
FIGURE 12. Write Status Register



DS012402-14

Note that the first four bits are don't care bits followed by BP1 and BP0 then two additional don't care bits. Programming will start after the $\overline{CS}$ pin is forced back to a high level. As in the WRITE instruction the LOW to HIGH transition of the $\overline{CS}$ pin must occur during the SCK low time immediately after clocking in the last don't care bit. See Figure 13.

FIGURE 13. Start WRSR Condition

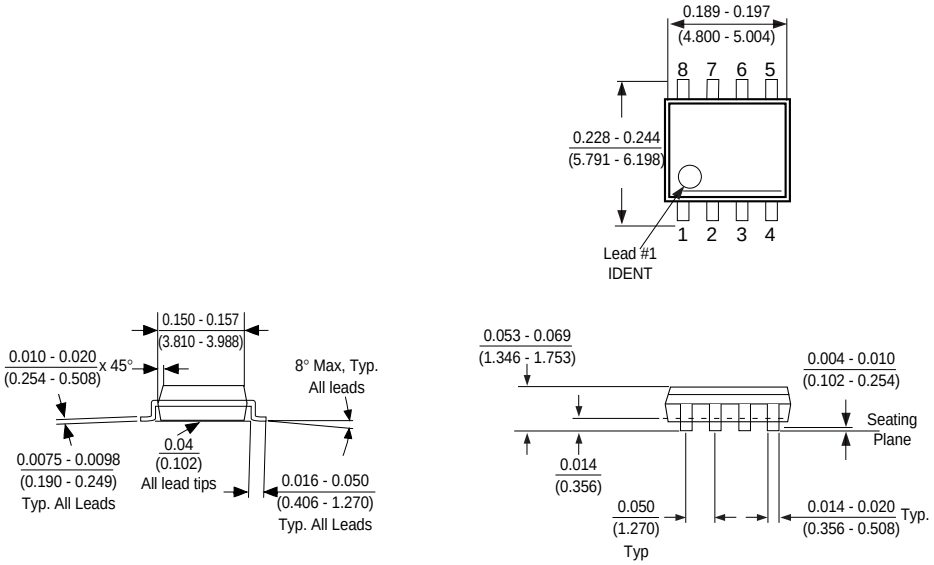


DS012402-15

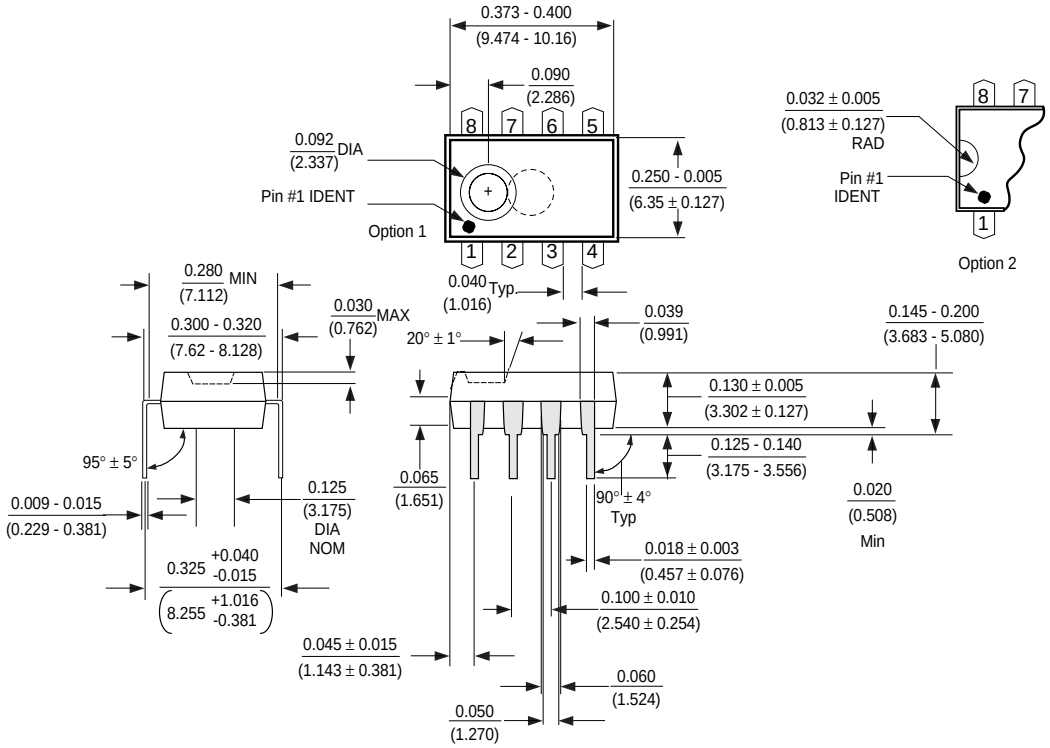
The READY/BUSY status of the device can be determined by executing a READ STATUS REGISTER (RDSR) instruction. Bit 0 = 1 indicates that the WRSR cycle is still in progress and Bit 0 = 0 indicates that the WRSR cycle has ended.

At the completion of a WRITE cycle the device is automatically returned to the write disable state.

Physical Dimensions inches (millimeters) unless otherwise noted

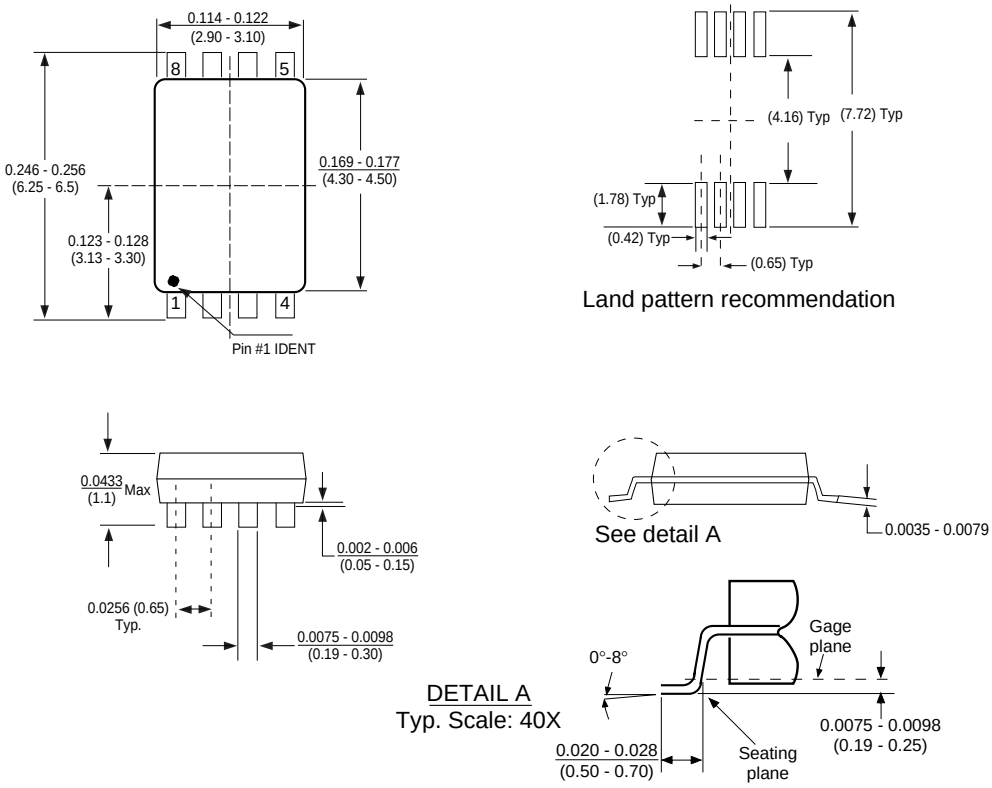


Molded Small Out-Line Package (M8)
Package Number M08A



Molded Dual-In-Line Package (N)
Package Number N08E

Physical Dimensions inches (millimeters) unless otherwise noted



Notes: Unless otherwise specified
1. Reference JEDEC registration MO153. Variation AA. Dated 7/93

8-Pin Molded TSSOP, JEDEC (MT8)
Package Number MTC08

Life Support Policy

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FAIRCHILD
SEMICONDUCTOR™

PRELIMINARY
March 1999

NM25C640
64K-Bit Serial CMOS EEPROM
(Serial Peripheral Interface (SPI) Synchronous Bus)

General Description

The NM25C640 is a 65,536-bit CMOS EEPROM with an SPI compatible serial interface. The NM25C640 is designed for data storage in applications requiring both non-volatile memory and in-system data updates. This EEPROM is well suited for applications using the 68HC11 series of microcontrollers that support the SPI interface for high speed communication with peripheral devices via a serial bus to reduce pin count. The NM25C640 is implemented in Fairchild Semiconductor's floating gate CMOS process that provides superior endurance and data retention.

The serial data transmission of this device requires four signal lines to control the device operation: Chip Select ($\overline{CS}$), Clock (SCK), Data In (SI), and Serial Data Out (SO). All programming cycles are completely self-timed and do not require an erase before WRITE.

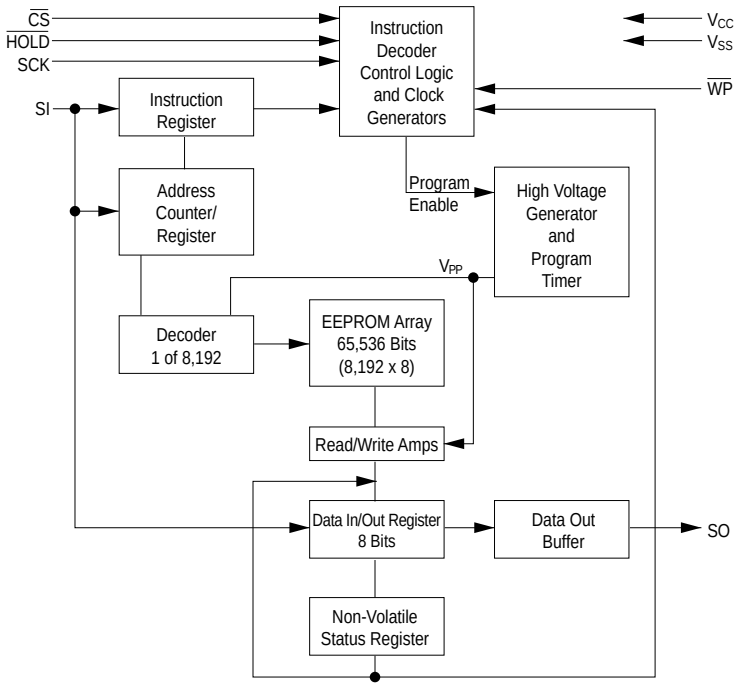
BLOCK WRITE protection is provided by programming the STATUS REGISTER with one of four levels of write protection. Additionally, separate WRITE enable and WRITE disable instructions are provided for data protection.

Hardware data protection is provided by the $\overline{WP}$ pin to protect against inadvertent programming. The $\overline{HOLD}$ pin allows the serial communication to be suspended without resetting the serial sequence.

Features

- 2.75 MHz clock rate @ 4.5V to 5.5V
  2.1 MHz @ 2.7V to 4.5V
- 65,536 bits organized as 8,192 x 8
- Multiple chips on the same 3-wire bus with separate chip select lines
- Self-timed programming cycle
- Simultaneous programming of 1 to 32 bytes at a time
- Status register can be polled during programming to monitor READY/BUSY
- Write Protect ($\overline{WP}$) pin and write disable instruction for both hardware and software write protection
- Block write protect feature to protect against accidental writes
- Endurance: 1,000,000 data changes
- Data retention greater than 40 years
- Packages available: 8-pin DIP or 8-Pin SO

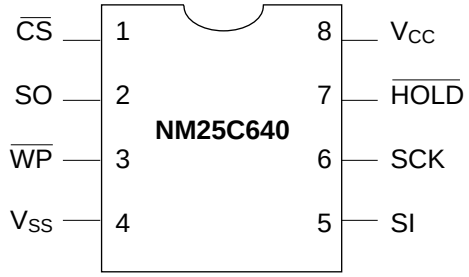
Block Diagram



DS500041-1

Connection Diagram

**Dual-In-Line Package (N)
and SO Package (M8)**



DS500041-2

Top View

Pin Names

$\overline{CS}$	Chip Select Input
SO	Serial Data Output
$\overline{WP}$	Write Protect
V_{SS}	Ground
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{HOLD}$	Suspends Serial Data
V_{CC}	Power Supply

Ordering Information

		Letter	Description
NM 25 C XX LZ E XX	**Package**	N	8-Pin DIP
		M8	8-Pin SO
	Temp. Range	None	0 to 70°C
		V	-40 to +125°C
		E	-40 to +85°C
	Voltage Operating Range	Blank	4.5V to 5.5V
		L	2.7V to 4.5V
		LZ	2.7V to 4.5V and <1µA Standby Current
	Density/Mode	640	64K, mode 0
		C	CMOS
	Interface	25	SPI
		NM	**Fairchild Nonvolatile Memory**

Standard Voltage 4.5 ≤ V_{CC} ≤ 5.5V Specifications

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM25C640	0°C to +70°C
NM25C640E	-40°C to +85°C
NM25C640V	-40°C to +125°C
Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics 4.5V ≤ V_{CC} ≤ 5.5V (unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Units
I_{CC}	Operating Current	$\overline{CS}$ = V_{IL}		3	mA
I_{CCSB}	Standby Current	$\overline{CS}$ = V_{CC}		50	µA
I_{IL}	Input Leakage	V_{IN} = 0 to V_{CC}	-1	+1	µA
I_{OL}	Output Leakage	V_{OUT} = GND to V_{CC}	-1	+1	µA
V_{IL}	CMOS Input Low Voltage		-0.3	V_{CC} * 0.3	V
V_{IH}	CMOS Input High Voltage		V_{CC} * 0.7	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -0.8 mA	V_{CC} - 0.8		V
f_{OP}	SCK Frequency			2.75	MHz
t_{RI}	Input Rise Time			2.0	µs
t_{FI}	Input Fall Time			2.0	µs
t_{CLH}	Clock High Time	(Note 2)	155		ns
t_{CLL}	Clock Low Time	(Note 2)	155		ns
t_{CSH}	Min $\overline{CS}$ High Time	(Note 3)	240		ns
t_{CSS}	$\overline{CS}$ Setup Time		176		ns
t_{DIS}	Data Setup Time		50		ns
t_{HDS}	$\overline{HOLD}$ Setup Time		90		ns
t_{CSN}	$\overline{CS}$ Hold Time		155		ns
t_{DIN}	Data Hold Time		50		ns
t_{HDN}	$\overline{HOLD}$ Hold Time		90		ns
t_{PD}	Output Delay	C_L = 200 pF		135	ns
t_{DH}	Output Hold Time		0		ns
t_{LZ}	$\overline{HOLD}$ to Output Low Z			240	ns
t_{DF}	Output Disable Time	C_L = 200 pF		290	ns
t_{HZ}	$\overline{HOLD}$ to Output High Z			240	ns
t_{WP}	Write Cycle Time	1–32 Bytes		10	ms

Capacitance T_A = 25°C, f = 2.1/1 MHz (Note 4)

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance	3	8	pF
C_{IN}	Input Capacitance	2	6	pF

AC Test Conditions

Output Load	C_L = 200 pF
Input Pulse Levels	0.1 * V_{CC} – 0.9 * V_{CC}
Timing Measurement Reference Level	0.3 * V_{CC} - 0.7 • V_{CC}

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The f_{OP} frequency specification specifies a minimum clock period of $1/f_{OP}$. Therefore, for every f_{OP} clock cycle, t_{CLH} + t_{CLL} must be equal to or greater than $1/f_{OP}$. For example, if the 2.1MHz period = 476ns and t_{CLH} = 190ns, t_{CLL} must be 286ns.

Note 3: $\overline{CS}$ must be brought high for a minimum of t_{CSH} between consecutive instruction cycles.

Note 4: This parameter is periodically sampled and not 100% tested.

Low Voltage 2.7V ≤ V_{CC} ≤ 4.5V Specifications

Absolute Maximum Ratings (Note 5)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM25C640L/LZ	0°C to +70°C
NM25C640LZ/LZE	-40°C to +85°C
NM25C640LV	-40°C to +125°C
Power Supply (V_{CC})	2.7V–4.5V

DC and AC Electrical Characteristics 2.7V ≤ V_{CC} ≤ 4.5V (unless otherwise specified)

Symbol	Parameter	Part	Conditions	25C640L/LE 25C640LZ/LZE		25C640LV		Units
				Min.	Max.	Min	Max	
I_{CC}	Operating Current		$\overline{CS}$ = V_{IL}		3		3	mA
I_{CCSB}	Standby Current	L LZ	$\overline{CS}$ = V_{CC}		10 1		10 N/A	µA µA
I_{IL}	Input Leakage		V_{IN} = 0 to V_{CC}	-1	1	-1	1	µA
I_{OL}	Output Leakage		V_{OUT} = GND to V_{CC}	-1	1	-1	1	µA
V_{IL}	Input Low Voltage			-0.3	0.3 * V_{CC}	-0.3	0.3 * V_{CC}	V
V_{IH}	Input High Voltage			0.7 * V_{CC}	V_{CC} + 0.3	0.7 * V_{CC}	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage		I_{OL} = 1.6 mA		0.4		0.4	V
V_{OH}	Output High Voltage		I_{OH} = –0.8 mA	V_{CC} - 0.8		V_{CC} - 0.8		V
f_{OP}	SCK Frequency				2.1		1.0	MHz
t_{RI}	Input Rise Time				2.0		2.0	µs
t_{FI}	Input Fall Time				2.0		2.0	µs
t_{CLH}	Clock High Time		(Note 6)	190		410		ns
t_{CLL}	Clock Low Time		(Note 6)	190		410		ns
t_{CSH}	Min. $\overline{CS}$ High Time		(Note 7)	240		500		ns
t_{CSS}	$\overline{CS}$ Setup Time			240		500		ns
t_{DIS}	Data Setup Time			100		100		ns
t_{HDS}	$\overline{HOLD}$ Setup Time			90		240		ns
t_{CSN}	$\overline{CS}$ Hold Time			240		500		ns
t_{DIN}	Data Hold Time			100		100		ns
t_{HDN}	$\overline{HOLD}$ Hold Time			90		240		ns
t_{PD}	Output Delay		C_L = 200 pF		240		500	ns
t_{DH}	Output Hold Time			0		0		ns
t_{LZ}	$\overline{HOLD}$ Output Low Z				100		240	ns
t_{DF}	Output Disable Time		C_L = 200 pF		240		500	ns
t_{HZ}	$\overline{HOLD}$ to Output Hi Z				100		240	ns
t_{WP}	Write Cycle Time		1-32 Bytes		15		15	ms

Capacitance T_A = 25°C, f = 2.1/1 MHz (Note 8)

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance	3	8	pF
C_{IN}	Input Capacitance	2	6	pF

AC Test Conditions

Output Load	C_L = 200pF
Input Pulse Levels	0.1 * V_{CC} - 0.9 * V_{CC}
Timing Measurement Reference Level	0.3 * V_{CC} - 0.7 * V_{CC}

Note 5: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

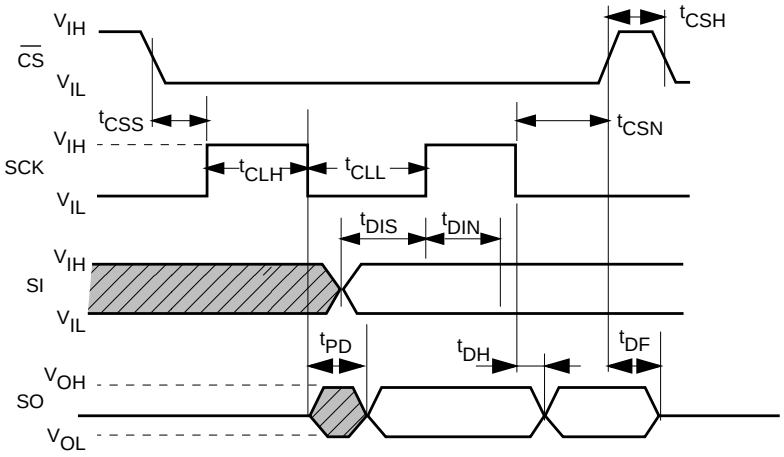
Note 6: The f_{OP} frequency specification specifies a minimum clock period of $1/f_{OP}$. Therefore, for every f_{OP} clock cycle, t_{CLH} + t_{CLL} must be equal to or greater than $1/f_{OP}$. For example, if the 2.1MHz period = 476ns and t_{CLH} = 190ns, t_{CLL} must be 286ns.

Note 7: $\overline{CS}$ must be brought high for a minimum of t_{CSH} between consecutive instruction cycles.

Note 8: This parameter is periodically sampled and not 100% tested.

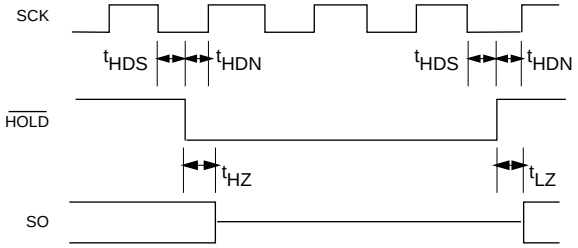
AC Test Conditions (Continued)

FIGURE 1. Synchronous Data Timing Diagram



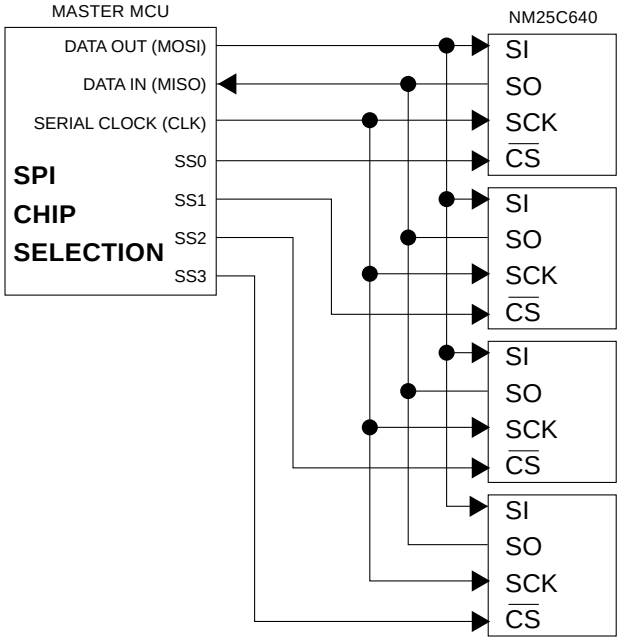
DS500041-3

FIGURE 2. Hold Timing



DS500041-6

FIGURE 3. SPI Serial Interface



DS500041-4

Functional Description

TABLE 1. Instruction Set

Instruction Name	Instruction Opcode	Operation
WREN	00000110	Set Write Enable Latch
WRDI	00000100	Reset Write Enable Latch
RDSR	00000101	Read Status Register
WRSR	00000001	Write Status Register
READ	00000011	Read Data from Memory Array
WRITE	00000010	Write Data to Memory Array

MASTER: The device that generates the serial clock is designated as the master. The NM25C640 can never function as a master.

SLAVE: The NM25C640 always operates as a slave as the serial clock pin is always an input.

TRANSMITTER/RECEIVER: The NM25C640 has separate pins for data transmission (SO) and reception (SI).

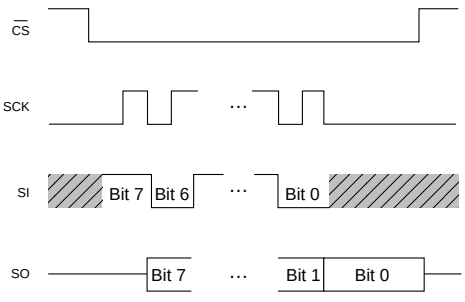
MSB: The Most Significant Bit is the first bit transmitted and received.

CHIP SELECT: The chip is selected when pin $\overline{CS}$ is low. When the chip is *not* selected, data will not be accepted from pin SI, and the output pin SO is in high impedance.

SERIAL OP-CODE: The first byte transmitted after the chip is selected with $\overline{CS}$ going low contains the op-code that defines the operation to be performed.

PROTOCOL: When connected to the SPI port of a 68HC11 microcontroller, the NM25C640 accepts a clock phase of 0 and a clock polarity of 0. The SPI protocol for this device defines the byte transmitted on the SI and SO data lines for proper chip operation. See Figure 4.

FIGURE 4. SPI Protocol



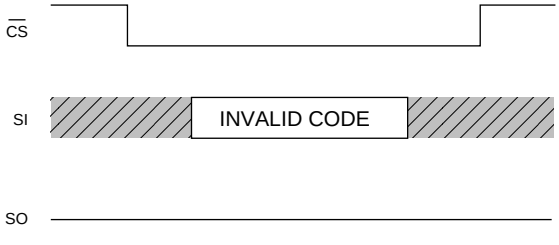
DS500041-5

Data is clocked in on the positive SCK edge and out on the negative SCK edge.

HOLD: The $\overline{HOLD}$ pin is used in conjunction with the $\overline{CS}$ to select the device. Once the device is selected and a serial sequence is underway, $\overline{HOLD}$ may be forced low to suspend further serial communication with the device without resetting the serial sequence. Note that $\overline{HOLD}$ must be brought low while the SCK pin is low. The device must remain selected during this sequence. To resume serial communication $\overline{HOLD}$ is brought high while the SCK pin is low. The SO pin is at a high impedance state during $\overline{HOLD}$.

INVALID OP-CODE: After an invalid code is received, no data is shifted into the NM25C640, and the SO data output pin remains high impedance until a new $\overline{CS}$ falling edge reinitializes the serial communication. See Figure 5 .

FIGURE 5. Invalid Op-Code

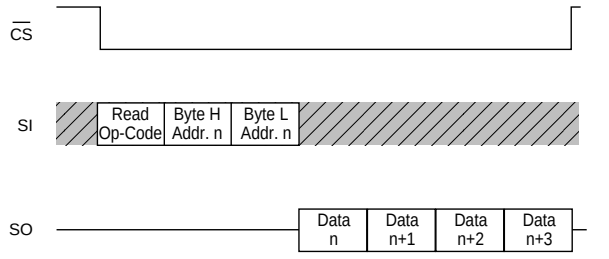


DS500041-7

Functional Description (Continued)

READ SEQUENCE: Reading the memory via the serial SPI link requires the following sequence. The $\overline{CS}$ line is pulled low to select the device. The READ op-code is transmitted on the SI line followed by the high order address byte (A12–A8), and the low order address byte (A7–A0). The leading three bits in the high order address byte will be ignored. After this is done, data on the SI line becomes don't care. The data (D7–D0) at the address specified is then shifted out on the SO line. If only one byte is to be read, the $\overline{CS}$ line can be pulled back to the high level. It is possible to continue the READ sequence as the byte adress is automatically incremented and data will continue to be shifted out. When the highest address is reached (1FFF), the address counter rolls over to lowest address (000) allowing the entire memory to be read in one continuous READ cycle. See Figure 6.

FIGURE 6. Read Sequence



READ STATUS REGISTER (RDSR) : The Read Status Register (RDSR) instruction provides access to the status register is used to interrogate the READY/BUSY and WRITE ENABLE status of the chip. Two non-volatile status register bits are used to select one of four levels of BLOCK WRITE PROTECTION. The status register format is shown in Table 2.

TABLE 2. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	BP1	BP0	WEN	$\overline{RDY}$

X = Don't Care.

Status register Bit 0 = 0 ($\overline{RDY}$) indicates that the device is READY; Bit 0 = 1 indicates that a program cycle is in progress. Bit 1 = 0 (WEN) indicates that the device is not WRITE ENABLED; Bit 1 = 1 indicates that the device is WRITE ENABLED. Non-volatile status register Bits 2 and 3 (BP0 and BP1) indicate the level of BLOCK WRITE PROTECTION selected. The block write protection levels and corresponding status register control bits are shown in Table 3. **Note that if a RDSR instruction is executed during a programming cycle only the RDY bit is valid. All other bits are 1s.** See Figure 7.

FIGURE 7. Read Status

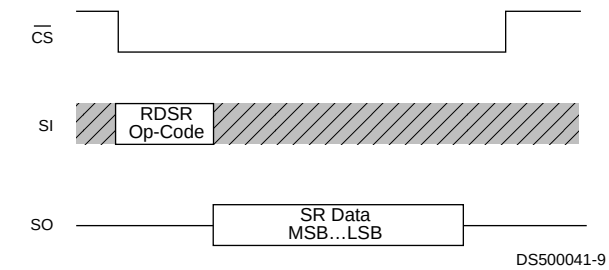
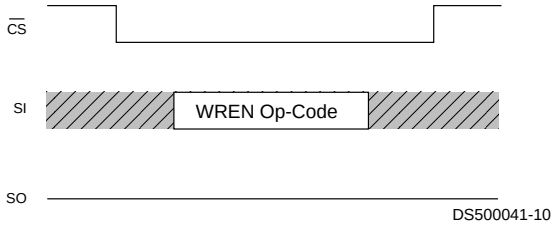


TABLE 3. Block Write Protection Levels

Level	Status Register Bits		Array Address Protected
	BP1	BP0	
0	0	0	None
1	0	1	1800-1FFF
2	1	0	1000-1FFF
3	1	1	0000–1FFF

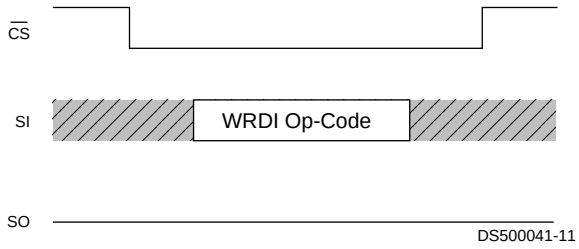
WRITE ENABLE (WREN): When V_{CC} is applied to the chip, it "powers up" in the write disable state. Therefore, all programming modes must be preceded by a WRITE ENABLE (WREN) instruction. Additionally, the WP must be held high during a write engble instruction. At the completion of a WRITE or WRSR cycle the device is automatically returned to the write disable state. Note that a WRITE DISABLE (WRD) instruction will also return the device to the write disable state. See Figure 8.

FIGURE 8. Write Enable



WRITE DISABLE (WRDI): To protect against accidental data disturbance the WRITE DISABLE (WRDI) instruction disables all programming modes. See Figure 9.

FIGURE 9. Write Disable

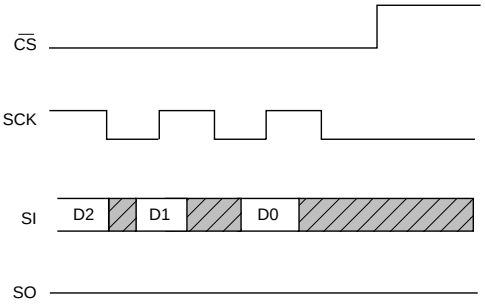


Functional Description (Continued)

WRITE SEQUENCE: To program the device, the WRITE PROTECT ($\overline{WP}$) pin must be held high and two separate instructions must be executed. The chip must first be write enabled via the WRITE ENABLE instruction and then a WRITE instruction must be executed. Moreover, the address of the memory location(s) to be programmed must be outside the protected address field selected by the Block Write Protection Level. See Table 3.

A WRITE command requires the following sequence. The $\overline{CS}$ line is pulled low to select the device, then the WRITE op-code is transmitted on the SI line followed by the high order address byte (A12-A8) and the low order address byte (A7–A0). The leading five bits in the high order address byte will be ignored. The address is followed by the data (D7–D0) to be written. Programming will start after the $\overline{CS}$ pin is forced back to a high level. Note that the LOW to HIGH transition of the $\overline{CS}$ pin must occur during the SCK low time immediately after clocking in the D0 data bit. See Figure 10.

FIGURE 10. End of WRITE Sequence

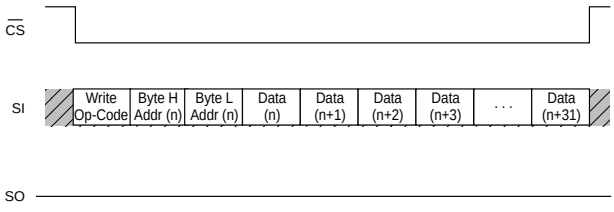


DS500041-12

The READY/BUSY status of the device can be determined by executing a READ STATUS REGISTER (RDSR) instruction. Bit 0 = 1 indicates that the WRITE cycle is still in progress and Bit 0 = 0 indicates that the WRITE cycle has ended. During the WRITE programming cycle (Bit 0 = 1) only the READ STATUS REGISTER instruction is enabled.

The NM25C640 is capable of a 32 byte PAGE WRITE operation. After receipt of each byte of data the five low order address bits are internally incremented by one. The eight high order bits of the address will remain constant. If the master should transmit more than 32 bytes of data, the address counter will "roll over," and the previously loaded data will be reloaded. See Figure 11.

FIGURE 11. 32 Byte Page Write



DS500041-13

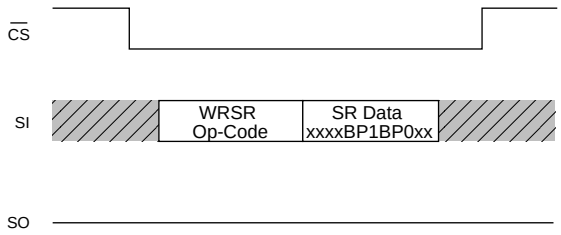
At the completion of a WRITE cycle the device is automatically returned to the write disable state.

If the device is not WRITE enabled, the device will ignore the WRITE instruction and return to the standby state when CS is forced high. A new CS falling edge is required to re-initialize the serial communication.

WRITE STATUS REGISTER (WRSR): The WRITE STATUS REGISTER (WRSR) instruction is used to program the non-volatile status register Bits 2 and 3 (BP0 and BP1). The WRITE PROTECT (WP) pin must be held high and two separate instructions must be executed. The chip must first be write enabled via the WRITE ENABLE instruction and then a WRSR instruction must be executed.

The WRSR command requires the following sequence. The CS line is pulled low to select the device and then the WRSR op-code is transmitted on the SI line followed by the data to be programmed. See Figure 12.

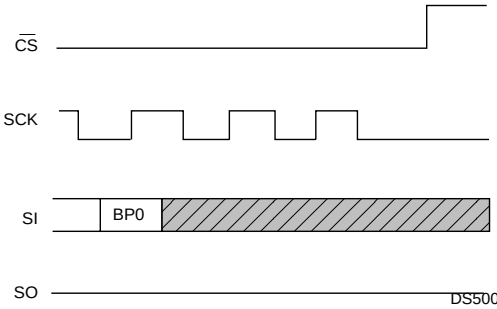
FIGURE 12. Write Status Register



DS500041-14

Note that the first four bits are don't care bits followed by BP1 and BP0 then two additional don't care bits. Programming will start after the CS pin is forced back to a high level. As in the WRITE instruction the LOW to HIGH transition of the CS pin must occur during the SCK low time immediately after clocking in the last don't care bit. See Figure 13.

FIGURE 13. Start WRSR Condition

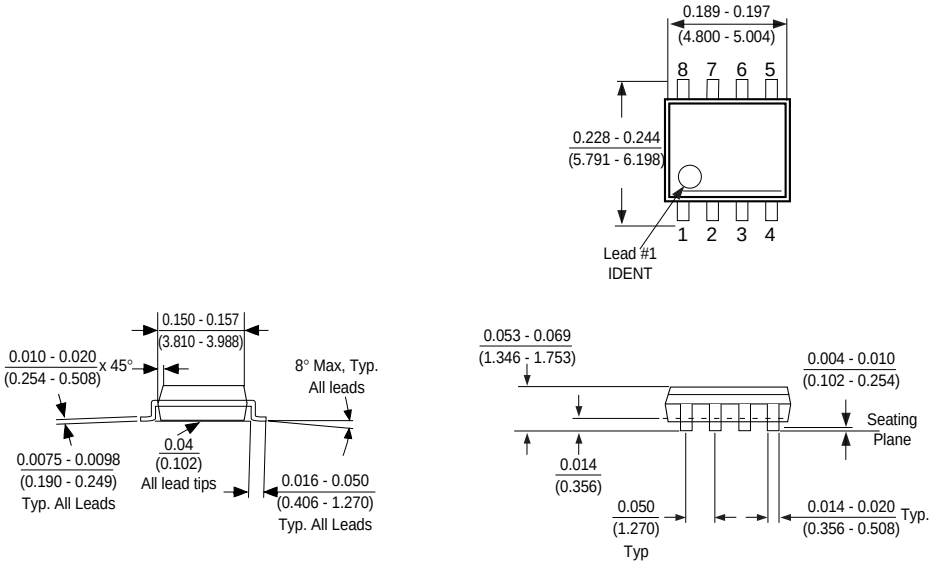


DS500041-15

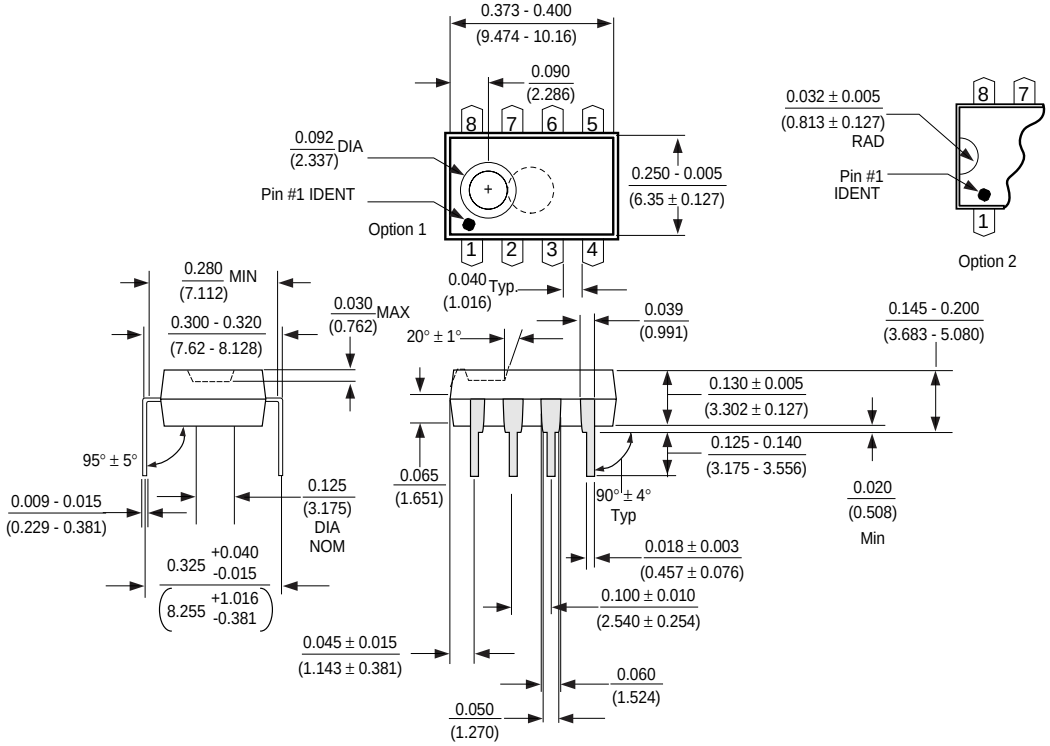
The READY/BUSY status of the device can be determined by executing a READ STATUS REGISTER (RDSR) instruction. Bit 0 = 1 indicates that the WRSR cycle is still in progress and Bit 0 = 0 indicates that the WRSR cycle has ended.

At the completion of a WRITE cycle the device is automatically returned to the write disable state.

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Small Out-Line Package (M8)
Package Number M08A



Molded Dual-In-Line Package (N)
Package Number N08E

Life Support Policy

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD
SEMICONDUCTOR™

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NM25C020
2048-Bit Serial CMOS EEPROM
(Serial Peripheral Interface (SPI) Synchronous Bus)

General Description

The NM25C020 is a 2048-bit CMOS EEPROM with an SPI compatible serial interface. The NM25C020 is designed for data storage in applications requiring both non-volatile memory and in-system data updates. This EEPROM is well suited for applications using the 68HC11 series of microcontrollers that support the SPI interface for high speed communication with peripheral devices via a serial bus to reduce pin count. The NM25C020 is implemented in Fairchild Semiconductor's floating gate CMOS process that provides superior endurance and data retention.

The serial data transmission of this device requires four signal lines to control the device operation: Chip Select ($\overline{CS}$), Clock (SCK), Data In (SI), and Serial Data Out (SO). All programming cycles are completely self-timed and do not require an erase before WRITE.

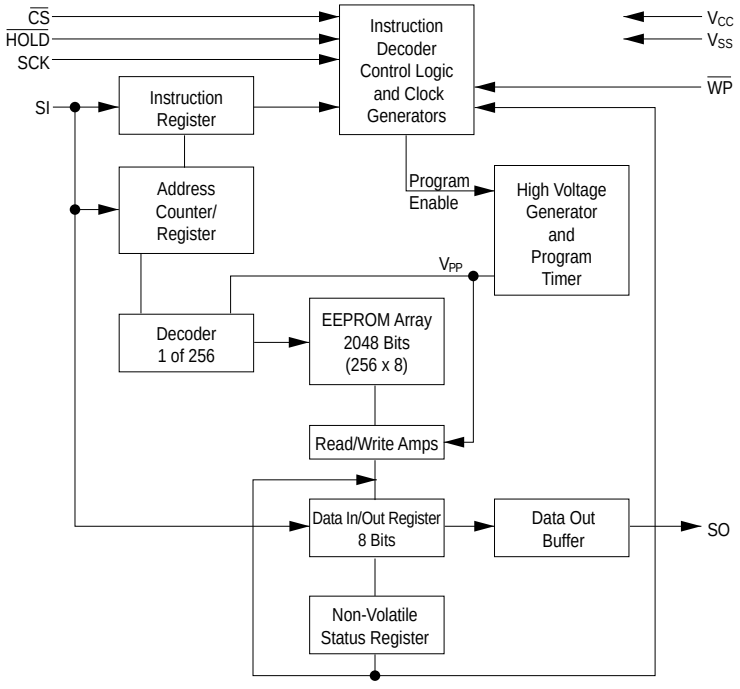
BLOCK WRITE protection is provided by programming the STATUS REGISTER with one of four levels of write protection. Additionally, separate WRITE enable and WRITE program disable instructions are provided for data protection.

Hardware data protection is provided by the $\overline{WP}$ pin to protect against accidental data changes. The $\overline{HOLD}$ pin allows the serial communication to be suspended without resetting the serial sequence.

Features

- 2.1 MHz clock rate @ 2.7V to 5.5V
- 2048 bits organized as 256 x 8
- Multiple chips on the same 3-wire bus with separate chip select lines
- Self-timed programming cycle
- Simultaneous programming of 1 to 4 bytes at a time
- Status register can be polled during programming to monitor READY/BUSY
- Write Protect ($\overline{WP}$) pin and write disable instruction for both hardware and software write protection
- Block write protect feature to protect against accidental writes
- Endurance: 1,000,000 data changes
- Data retention greater than 40 years
- Packages available: 8-pin DIP, 8-pin SO, or 8-pin TSSOP

Block Diagram



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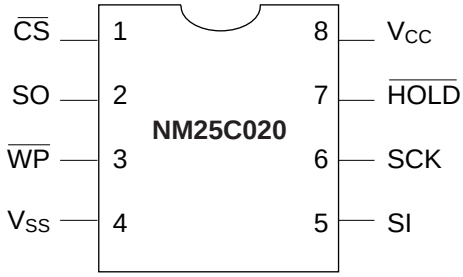
Connection Diagram

Dual-In-Line Package (N), SO Package (M8), and TSSOP Package (MT8)



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Top View
See Package Number N08E (N), M08A (M8), and MTC08 (MT8)

Pin Names

$\overline{CS}$	Chip Select Input
SO	Serial Data Output
$\overline{WP}$	Write Protect
V_{SS}	Ground
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{HOLD}$	Suspends Serial Data
V_{CC}	Power Supply

Ordering Information

NM 25 C XX LZ E XX

	Letter	Description
Package	N	8-pin DIP
	M8	8-pin SO
	MT8	8-pin TSSOP
Temp. Range	None	0 to 70°C
	V	-40 to +125°C
	E	-40 to +85°C
Voltage Operating Range	Blank	4.5V to 5.5V
	L	2.7V to 5.5V
	LZ	2.7V to 5.5V and <1µA Standby Current
Density	020	2K, mode 0
	C	CMOS technology
Interface	25	SPI - 3 Wire
	NM	**Fairchild Nonvolatile Memory Prefix**

Standard Voltage 4.5 ≤ V_{CC} ≤ 5.5V Specifications

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM25C020	0°C to +70°C
NM25C020E	-40°C to +85°C
NM25C020V	-40°C to +125°C
Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics 4.5V ≤ V_{CC} ≤ 5.5V (unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Units
I_{CC}	Operating Current	$\overline{CS}$ = V_{IL}		3	mA
I_{CCSB}	Standby Current	$\overline{CS}$ = V_{CC}		50	µA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}	-1	+1	µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}	-1	+1	µA
V_{IL}	CMOS Input Low Voltage		-0.3	0.8	V
V_{IH}	CMOS Input High Voltage		2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -0.8 mA	V_{CC} - 0.8		V
f_{OP}	SCK Frequency			2.1	MHz
t_{RI}	Input Rise Time			2.0	µs
t_{FI}	Input Fall Time			2.0	µs
t_{CLH}	Clock High Time	(Note 2)	190		ns
t_{CLL}	Clock Low Time	(Note 2)	190		V
t_{CSH}	Min $\overline{CS}$ High Time	(Note 3)	240		ns
t_{CSS}	$\overline{CS}$ Setup Time		240		ns
t_{DIS}	Data Setup Time		100		ns
t_{HDS}	$\overline{HOLD}$ Setup Time		90		ns
t_{CSN}	$\overline{CS}$ Hold Time		240		ns
t_{DIN}	Data Hold Time		100		ns
t_{HDN}	$\overline{HOLD}$ Hold Time		90		ns
t_{PD}	Output Delay from Clock Low	C_L = 200 pF		240	ns
t_{DH}	Output Hold Time		0		ns
t_{LZ}	$\overline{HOLD}$ to Output Low Z			100	ns
t_{DF}	Output Disable Time	C_L = 200 pF		240	ns
t_{HZ}	$\overline{HOLD}$ to Output High Z			100	ns
t_{WP}	Write Cycle Time	1–4 Bytes		10	ms

Capacitance T_A = 25°C, f = 1 MHz (Note 4)

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance	3	8	pF
C_{IN}	Input Capacitance	2	6	pF

AC Test Conditions

Output Load	C_L = 200 pF
Input Pulse Levels	0.1 * V_{CC} – 0.9 * V_{CC}
Timing Measurement Reference Level	0.3 * V_{CC} - .07 * V_{CC}

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SCK frequency specification specifies a minimum clock period of 476 ns; therefore, in an SCK clock cycle, t_{CLH} +t_{CLL} must be greater than or equal to 476 ns. For example, if t_{CLL} = 190 ns, then the minimum t_{CLH} = 286 ns in order to meet the SCK frequency specification.

Note 3: $\overline{CS}$ must be brought high for a minimum of 240 ns (t_{CSH}) between consecutive instruction cycles.

Note 4: This parameter is periodically sampled and not 100% tested.

Low Voltage 2.7V ≤ V_{CC} ≤ 5.5V Specifications

Absolute Maximum Ratings (Note 5)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM25C020L/LZ	0°C to +70°C
NM25C020LE/LZE	-40°C to +85°C
NM25C020LV	-40°C to +125°C
Power Supply (V_{CC})	2.7V–5.5V

DC and AC Electrical Characteristics 2.7V ≤ V_{CC} ≤ 5.5V (unless otherwise specified)

Symbol	Parameter	Part	Conditions	25C020E		25C020V		Units
				Min.	Max.	Min	Max	
I_{CC}	Operating Current		$\overline{CS}$ = V_{IL}		3		3	mA
I_{CCSB}	Standby Current	L LZ	$\overline{CS}$ = V_{CC}		10 1		10 N/A	µA µA
I_{IL}	Input Leakage		V_{IN} = 0 to V_{CC}	-1	1	-1	1	µA
I_{OL}	Output Leakage		V_{OUT} = GND to V_{CC}	-1	1	-1	1	µA
V_{IL}	Input Low Voltage			-0.3	0.8	-0.3	0.8	V
V_{IH}	Input High Voltage			2	V_{CC} + 0.3	2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage		I_{OL} = 2.1 mA		0.4		0.4	V
V_{OH}	Output High Voltage		I_{OH} = –0.8 mA	V_{CC} - 0.8		V_{CC} - 0.8		V
f_{OP}	SCK Frequency				2.1		2.1	MHz
t_{RI}	Input Rise Time				2.0		2.0	µs
t_{FI}	Input Fall Time				2.0		2.0	µs
t_{CLH}	Clock High Time		(Note 6)	190		190		ns
t_{CLL}	Clock Low Time		(Note 6)	190		190		ns
t_{CSH}	Min. $\overline{CS}$ High Time		(Note 7)	240		240		ns
t_{CSS}	$\overline{CS}$ Setup Time			240		240		ns
t_{DIS}	Data Setup Time			100		100		ns
t_{HDS}	$\overline{HOLD}$ Setup Time			90		90		ns
t_{CSN}	$\overline{CS}$ Hold Time			240		240		ns
t_{DIN}	Data Hold Time			100		100		ns
t_{HDN}	$\overline{HOLD}$ Hold Time			90		90		ns
t_{PD}	Output Delay from Clock Low		C_L = 200 pF		240		240	ns
t_{DH}	Output Hold Time			0		0		ns
t_{LZ}	$\overline{HOLD}$ Output Low Z				100		100	ns
t_{DF}	Output Disable Time		C_L = 200 pF		240		240	ns
t_{HZ}	$\overline{HOLD}$ to Output Hi Z				100		100	ns
t_{WP}	Write Cycle Time		1-4 Bytes		10		10	ms

Capacitance T_A = 25°C, f = 1 MHz (Note 8)

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance	3	8	pF
C_{IN}	Input Capacitance	2	6	pF

AC Test Conditions

Output Load	I_{OL} = 10 µA, I_{OH} = 10 µA
Input Pulse Levels	0.3V to 3.5V
Timing Measurement Reference Level	
Input	0.4V and 1.6V
Output	0.8V and 1.6V

Note 5: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

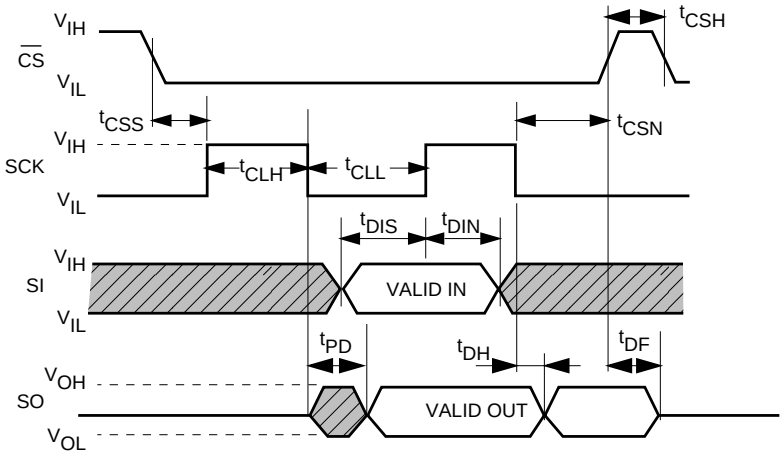
Note 6: Minimum Clock period. Specified minimum clock period for SCK frequency varies with temperature range. Extended temperature range ("E"), the minimum clock period is 476ns. In the automotive temperature range, the minimum clock period is 1000ns. For example, using the extended temperature range minimum, if t_{CLL} = 190ns, the minimum t_{CLH} is 286ns (190ns + 286ns = 476ns).

Note 7: $\overline{CS}$ must be brought high for a minimum of 250 ns (t_{CSH}) between consecutive instruction cycles.

Note 8: This parameter is periodically sampled and not 100% tested.

AC Test Conditions (Continued)

Synchronous Data Timing Diagram (Figure 1)



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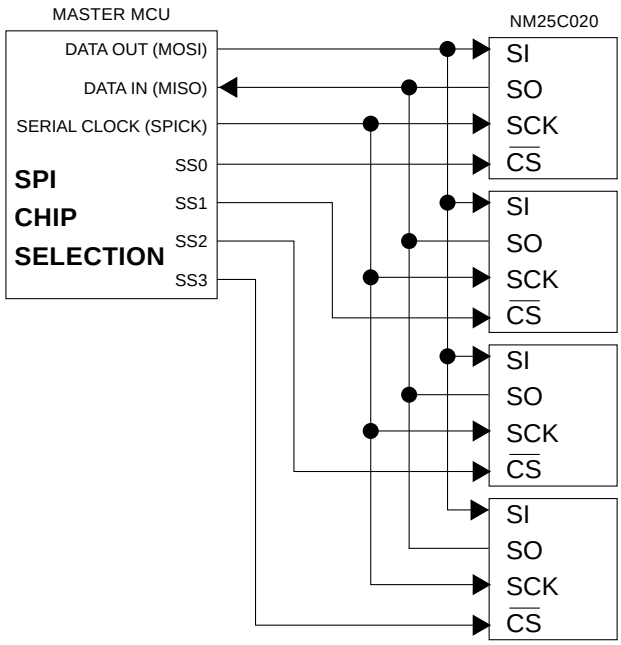
SPI Serial Interface (Figure 2)



DS012400-4

Functional Description

MASTER: The device that generates the serial clock is designated as the master. The NM25C020 can never function as a master.

SLAVE: The NM25C020 always operates as a slave as the serial clock pin is always an input.

TRANSMITTER/RECEIVER: The NM25C020 has separate pins for data transmission (SO) and reception (SI).

MSB: The Most Significant Bit is the first bit transmitted and received.

CHIP SELECT: The chip is selected when pin $\overline{CS}$ is low. When the chip is *not* selected, data will not be accepted from pin SI, and the output pin SO is in high impedance.

SERIAL OP-CODE: The first byte transmitted after the chip is selected with $\overline{CS}$ going low contains the op-code that defines the operation to be performed.

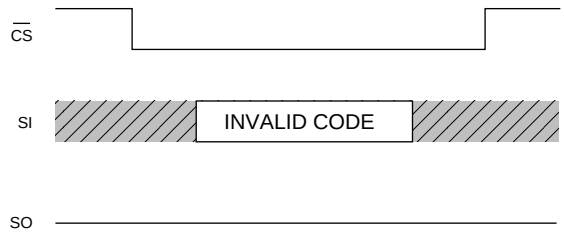
PROTOCOL: When connected to the SPI port of a 68HC11 microcontroller, the NM25C020 accepts a clock phase of 0 and a clock polarity of 0. The SPI protocol for this device defines the byte transmitted on the SI and SO data lines for proper chip operation. See Figure 4.

Data is clocked in on the positive SCK edge and out on the negative SCK edge.

HOLD: The $\overline{HOLD}$ pin is used in conjunction with the $\overline{CS}$ to select the device. Once the device is selected and a serial sequence is underway, $\overline{HOLD}$ may be forced low to suspend further serial communication with the device without resetting the serial sequence. Note that $\overline{HOLD}$ must be brought low while the SCK pin is low. The device must remain selected during this sequence. To resume serial communication $\overline{HOLD}$ is brought high while the SCK pin is low. Pins SI, SCK and SO are at a high impedance state during $\overline{HOLD}$. See Figure 5.

INVALID OP-CODE: After an invalid code is received, no data is shifted into the NM25C020, and the SO data output pin remains high impedance until a new $\overline{CS}$ falling edge reinitializes the serial communication. See Figure 3.

Invalid Op-Code (Figure 3)



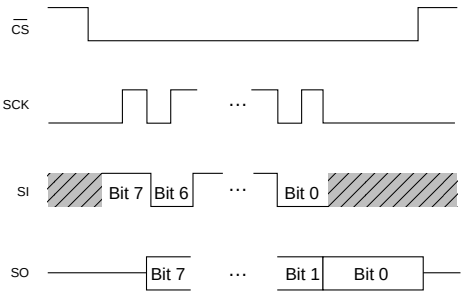
DS012400-7

Instruction Set (Table 1)

Instruction Name	Instruction Format	Operation
WREN	00000110	Set Write Enable Latch
WRDI	00000100	Reset Write Enable Latch
RDSR	00000101	Read Status Register
WRSR	00000001	Write Status Register
READ	00000011	Read Data from Memory Array
WRITE	00000010	Write Data to Memory Array

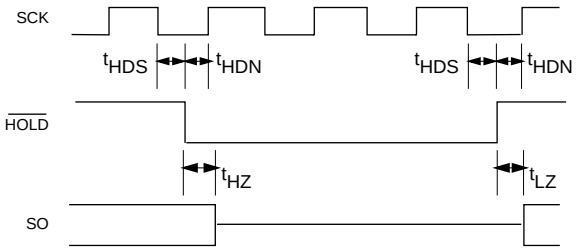
Functional Description (Continued)

SPI Protocol (Figure 4)



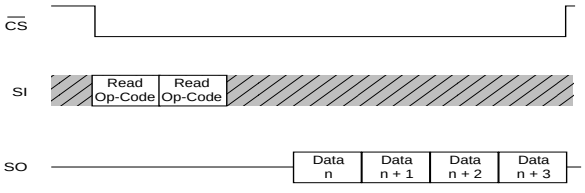
DS012400-5

HOLD Timing (Figure 5)



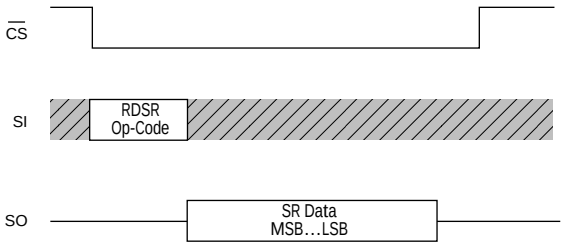
DS012400-6

Read Sequence (Figure 6)



DS012400-8

Read Status (Figure 7)



DS012400-9

Functional Description (Continued)

READ SEQUENCE: (One or More Bytes): Reading the memory via the serial SPI link requires the following sequence. The $\overline{CS}$ line is pulled low to select the device. The READ op-code is transmitted on the SI line followed by the byte address (A7–A0) to be read. After this is done, data on the SI line becomes don't care. The data (D7–D0) at the address specified is then shifted out on the SO line. If only one byte is to be read, the $\overline{CS}$ line can be pulled back to the high level. It is possible to continue the READ sequence as the byte adress is automatically incremented and data will continue to be shifted out. When the highest address is reached (FF), the address counter rolls over to lowest address (000) allowing the entire memory to be read in one continuous READ cycle. See Figure 6.

READ STATUS REGISTER (RDSR) : The Read Status Register (RDSR) instruction provides access to the status register is used to interrogate the READY/BUSY and WRITE ENABLE status of the chip. Two non-volatile status register bits are used to select one of four levels of BLOCK WRITE PROTECTION. The status register format is shown in Table 2.

Status Register Format (Table 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	1	1	BP1	BP0	WEN	$\overline{RDY}$

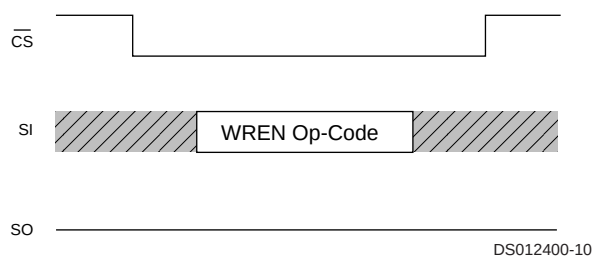
Status register Bit 0 = 0 ($\overline{RDY}$) indicates that the device is READY; Bit 0 = 1 indicates that a program cycle is in progress. Bit 1 = 0 (WEN) indicates that the device is not WRITE ENABLED; Bit 1 = 1 indicates that the device is WRITE ENABLED. Non-volatile status register Bits 2 and 3 (BP0 and BP1) indicate the level of BLOCK WRITE PROTECTION selected. The block write protection levels and corresponding status register control bits are shown in Table 3. Note that if a RDSR instruction is executed during a programming cycle only the $\overline{RDY}$ bit is valid. All other bits are 1s. See Figure 7.

Block Write Protection Levels (Table 3)

Level	Status Register Bits		Array Address Protected
	BP1	BP0	
0	0	0	None
1	0	1	C0-FF
2	1	0	80-FF
3	1	1	00-FF

WRITE ENABLE (WREN): When V_{CC} is applied to the chip, it "powers up" in the write disable state. Therefore, all programming modes must be preceded by a WRITE ENABLE (WREN) instruction. At the completion of a WRITE or WRSR cycle the device is automatically returned to the write disable state. Note that a WRITE DISABLE (WRDI) instruction will also return the device to the write disable state. See Figure 8.

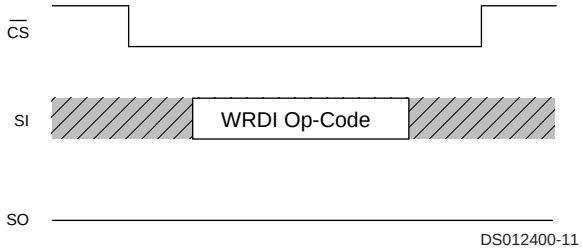
Write Enable (Figure 8)



DS012400-10

WRITE DISABLE (WRDI): To protect against accidental data disturbance the WRITE DISABLE (WRDI) instruction disables all programming modes. See Figure 9.

Write Disable (Figure 9)



DS012400-11

WRITE SEQUENCE: To program the device, the WRITE PROTECT ($\overline{WP}$) pin must be held high and two separate instructions must be executed. The chip must first be write enabled via the WRITE ENABLE instruction and then a WRITE instruction must be executed. Moreover, the address of the memory location(s) to be programmed must be outside the protected address field selected by the Block Write Protection Level. See Table 3.

A WRITE command requires the following sequence. The $\overline{CS}$ line is pulled low to select the device, then the WRITE op-code is transmitted on the SI line followed by the byte address(A7–A0) and the corresponding data (D7-D0) to be written. Programming will start after the $\overline{CS}$ pin is forced back to a high level. Note that the LOW to HIGH transition of the $\overline{CS}$ pin must occur during the SCK low time immediately after clocking in the D0 data bit. See Figure 10.

The READY/BUSY status of the device can be determined by executing a READ STATUS REGISTER (RDSR) instruction. Bit 0 = 1 indicates that the WRITE cycle is still in progress and Bit 0 = 0 indicates that the WRITE cycle has ended. During the WRITE programming cycle (Bit 0 = 1) only the READ STATUS REGISTER instruction is enabled.

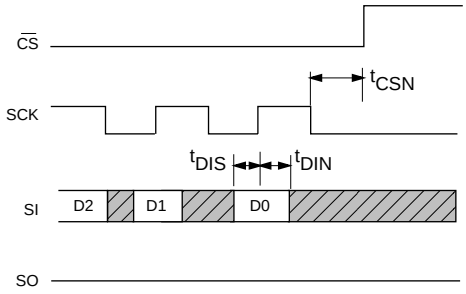
The NM25C020 is capable of a 4 byte PAGE WRITE operation. After receipt of each byte of data the two low order address bits are internally incremented by one. The seven high order bits of the address will remain constant. If the master should transmit more than 4 bytes of data, the address counter will "roll over," and the previously loaded data will be reloaded. See Figure 11.

At the completion of a WRITE cycle the device is automatically returned to the write disable state.

If the device is not WRITE enabled, the device will ignore the WRITE instruction and return to the standby state when $\overline{CS}$ is forced high. A new $\overline{CS}$ falling edge is required to re-initialize the serial communication.

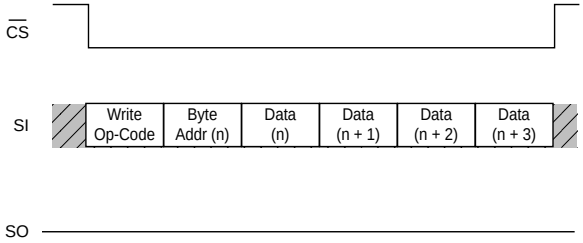
Functional Description (Continued)

Write Sequence (Figure 10)



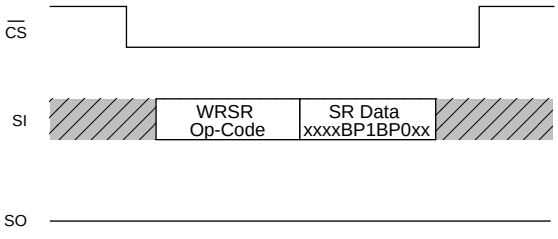
DS012400-12

Start Write Condition (Figure 11)



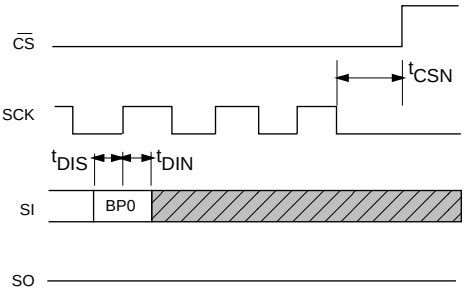
DS012400-13

Write Status Register (Figure 12)



DS012400-14

Start WRSR Condition (Figure 13)



DS012400-15

WRITE STATUS REGISTER (WRSR): The WRITE STATUS REGISTER (WRSR) instruction is used to program the non-volatile status register Bits 2 and 3 (BP0 and BP1). The WRITE PROTECT ($\overline{WP}$) pin must be held high and two separate instructions must be executed. The chip must first be write enabled via the WRITE ENABLE instruction and then a WRSR instruction must be executed.

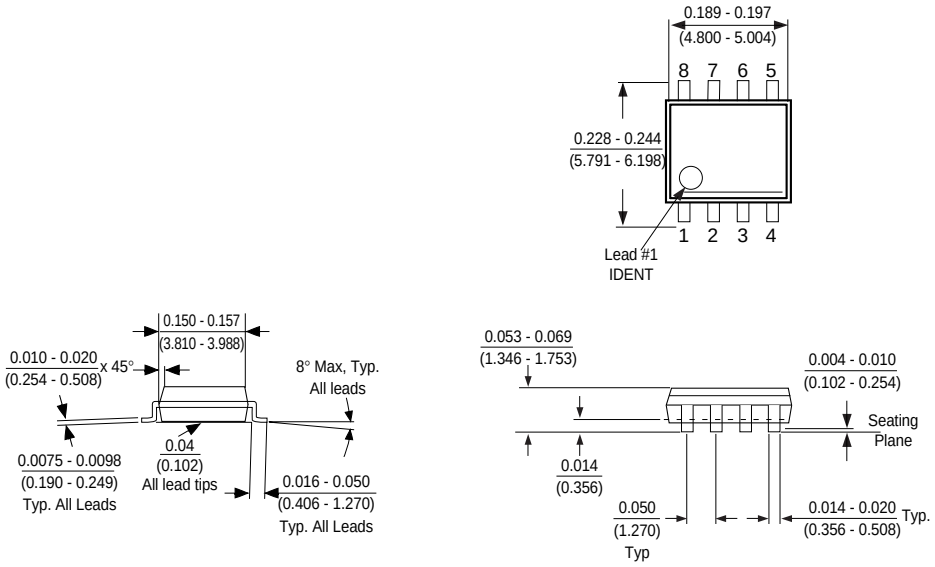
The WRSR command requires the following sequence. The $\overline{CS}$ line is pulled low to select the device and then the WRSR op-code is transmitted on the SI line followed by the data to be programmed. See Figure 12.

Note that the first four bits are don't care bits followed by BP1 and BP0 then two additional don't care bits. Programming will start after the $\overline{CS}$ pin is forced back to a high level. As in the WRITE instruction the LOW to HIGH transition of the $\overline{CS}$ pin must occur during the SCK low time immediately after clocking in the last don't care bit. See Figure 13.

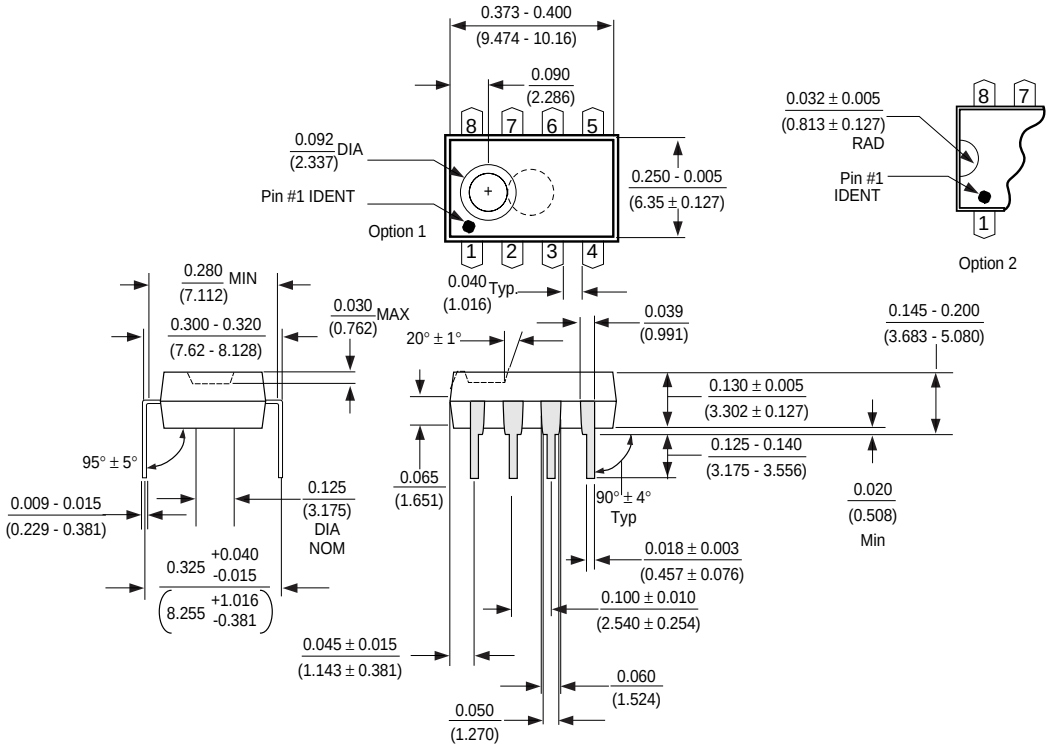
The READY/BUSY status of the device can be determined by executing a READ STATUS REGISTER (RDSR) instruction. Bit 0 = 1 indicates that the WRSR cycle is still in progress and Bit 0 = 0 indicates that the WRSR cycle has ended.

At the completion of a WRITE cycle the device is automatically returned to the write disable state.

Physical Dimensions inches (millimeters) unless otherwise noted

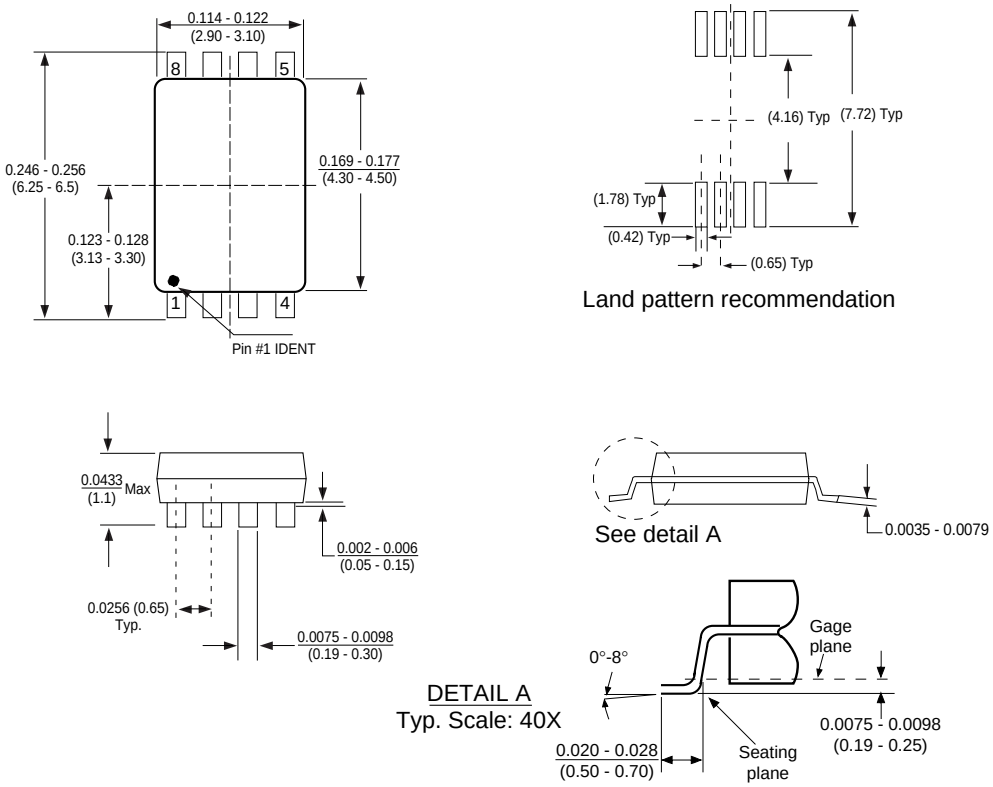


Molded Small Out-Line Package (M8)
Package Number M08A



Molded Dual-In-Line Package (N)
Package Number N08E

Physical Dimensions inches (millimeters) unless otherwise noted



Notes: Unless otherwise specified
1. Reference JEDEC registration MO153. Variation AA. Dated 7/93

8-Pin Molded TSSOP, JEDEC (MT8)
Package Number MTC08

Life Support Policy

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FAIRCHILD
SEMICONDUCTOR™

July 1998

NM25C040
4096-Bit Serial CMOS EEPROM
(Serial Peripheral Interface (SPI) Synchronous Bus)

General Description

The NM25C040 is a 4096-bit CMOS EEPROM with an SPI compatible serial interface. The NM25C040 is designed for data storage in applications requiring both non-volatile memory and in-system data updates. This EEPROM is well suited for applications using the 68HC11 series of microcontrollers that support the SPI interface for high speed communication with peripheral devices via a serial bus to reduce pin count. The NM25C040 is implemented in Fairchild Semiconductor's floating gate CMOS process that provides superior endurance and data retention.

The serial data transmission of this device requires four signal lines to control the device operation: Chip Select ($\overline{CS}$), Clock (SCK), Data In (SI), and Serial Data Out (SO). All programming cycles are completely self-timed and do not require an erase before WRITE.

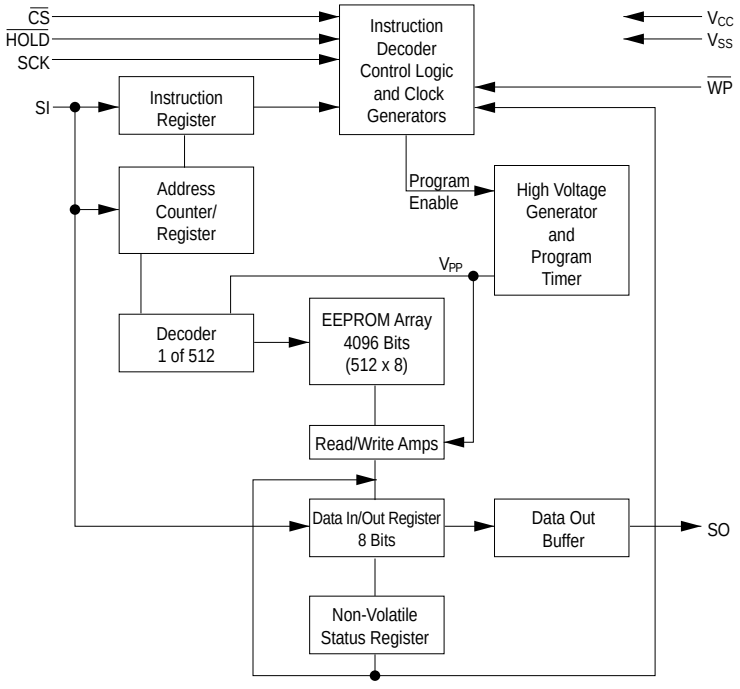
BLOCK WRITE protection is provided by programming the STATUS REGISTER with one of four levels of write protection. Additionally, separate WRITE enable and WRITE program disable instructions are provided for data protection.

Hardware data protection is provided by the $\overline{WP}$ pin to protect against accidental data changes. The $\overline{HOLD}$ pin allows the serial communication to be suspended without resetting the serial sequence.

Features

- 2.1 MHz clock rate @ 2.7V to 5.5V
- 4096 bits organized as 512 x 8
- Multiple chips on the same 3-wire bus with separate chip select lines
- Self-timed programming cycle
- Simultaneous programming of 1 to 4 bytes at a time
- Status register can be polled during programming to monitor READY/BUSY
- Write Protect ($\overline{WP}$) pin and write disable instruction for both hardware and software write protection
- Block write protect feature to protect against accidental writes
- Endurance: 1,000,000 data changes
- Data retention greater than 40 years
- Packages available: 8-pin DIP, 8-pin SO, or 8-pin TSSOP

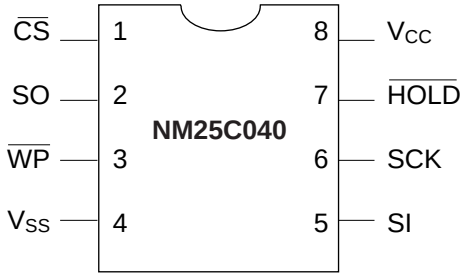
Block Diagram



DS012401-1

Connection Diagram

Dual-In-Line Package (N), SO Package (M8), and TSSOP Package (MT8)



DS012401-2

Top View
See Package Number N08E (N), M08A (M8), and MTC08 (MT8)

Pin Names

$\overline{CS}$	Chip Select Input
SO	Serial Data Output
$\overline{WP}$	Write Protect
V_{SS}	Ground
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{HOLD}$	Suspends Serial Data
V_{CC}	Power Supply

Ordering Information

NM 25 C XX LZ E XX

	Letter	Description
Package	N	8-pin DIP
	M8	8-pin SO
	MT8	8-pin TSSOP
Temp. Range	None	0 to 70°C
	V	-40 to +125°C
	E	-40 to +85°C
Voltage Operating Range	Blank	4.5V to 5.5V
	L	2.7V to 5.5V
	LZ	2.7V to 5.5V and <1µA Standby Current
Density	040	4K, mode 0
	C	CMOS technology
Interface	25	SPI - 3 Wire
	NM	**Fairchild Nonvolatile Memory Prefix**

Standard Voltage 4.5 ≤ V_{CC} ≤ 5.5V Specifications

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM25C040	0°C to +70°C
NM25C040E	-40°C to +85°C
NM25C040V	-40°C to +125°C
Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics 4.5V ≤ V_{CC} ≤ 5.5V (unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Units
I_{CC}	Operating Current	$\overline{CS}$ = V_{IL}		3	mA
I_{CCSB}	Standby Current	$\overline{CS}$ = V_{CC}		50	µA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}	-1	+1	µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}	-1	+1	µA
V_{IL}	CMOS Input Low Voltage		-0.3	0.8	V
V_{IH}	CMOS Input High Voltage		2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -0.8 mA	V_{CC} - 0.8		V
f_{OP}	SCK Frequency			2.1	MHz
t_{RI}	Input Rise Time			2.0	µs
t_{FI}	Input Fall Time			2.0	µs
t_{CLH}	Clock High Time	(Note 2)	190		ns
t_{CLL}	Clock Low Time	(Note 2)	190		V
t_{CSH}	Min $\overline{CS}$ High Time	(Note 3)	240		ns
t_{CSS}	$\overline{CS}$ Setup Time		240		ns
t_{DIS}	Data Setup Time		100		ns
t_{HDS}	$\overline{HOLD}$ Setup Time		90		ns
t_{CSN}	$\overline{CS}$ Hold Time		240		ns
t_{DIN}	Data Hold Time		100		ns
t_{HDN}	$\overline{HOLD}$ Hold Time		90		ns
t_{PD}	Output Delay from Clock Low	C_L = 200 pF		240	ns
t_{DH}	Output Hold Time		0		ns
t_{LZ}	$\overline{HOLD}$ to Output Low Z			100	ns
t_{DF}	Output Disable Time	C_L = 200 pF		240	ns
t_{HZ}	$\overline{HOLD}$ to Output High Z			100	ns
t_{WP}	Write Cycle Time	1–4 Bytes		10	ms

Capacitance T_A = 25°C, f = 1 MHz (Note 4)

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance	3	8	pF
C_{IN}	Input Capacitance	2	6	pF

AC Test Conditions

Output Load	C_L = 200 pF
Input Pulse Levels	0.1 * V_{CC} – 0.9 * V_{CC}
Timing Measurement Reference Level	0.3 * V_{CC} - 0.7 * V_{CC}

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SCK frequency specification specifies a minimum clock period of 476 ns; therefore, in an SCK clock cycle, t_{CLH} +t_{CLL} must be greater than or equal to 476 ns. For example, if t_{CLL} = 190 ns, then the minimum t_{CLH} = 286 ns in order to meet the SCK frequency specification.

Note 3: $\overline{CS}$ must be brought high for a minimum of 240 ns (t_{CSH}) between consecutive instruction cycles.

Note 4: This parameter is periodically sampled and not 100% tested.

Low Voltage 2.7V ≤ V_{CC} ≤ 5.5V Specifications

Absolute Maximum Ratings (Note 5)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM25C040L/LZ	0°C to +70°C
NM25C040LE/LZE	-40°C to +85°C
NM25C040LV	-40°C to +125°C
Power Supply (V_{CC})	2.7V–5.5V

DC and AC Electrical Characteristics 2.7V ≤ V_{CC} ≤ 5.5V (unless otherwise specified)

Symbol	Parameter	Part	Conditions	25C040LE		25C040LV		Units
				Min.	Max.	Min	Max	
I_{CC}	Operating Current		$\overline{CS}$ = V_{IL}		3		3	mA
I_{CCSB}	Standby Current	L LZ	$\overline{CS}$ = V_{CC}		10 1		10	µA µA
I_{IL}	Input Leakage		V_{IN} = 0 to V_{CC}	-1	1	-1	1	µA
I_{OL}	Output Leakage		V_{OUT} = GND to V_{CC}	-1	1	-1	1	µA
V_{IL}	Input Low Voltage			-0.3	V_{CC} * 0.3	-0.3	V_{CC} * 0.3	V
V_{IH}	Input High Voltage			V_{CC} * 0.7	V_{CC} + 0.3	V_{CC} * 0.7	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage		I_{OL} = 2.1 mA		0.4		0.4	V
V_{OH}	Output High Voltage		I_{OH} = –0.8 mA	V_{CC} - 0.8		V_{CC} - 0.8		V
f_{OP}	SCK Frequency				2.1		1.0	MHz
t_{RI}	Input Rise Time				2.0		2.0	µs
t_{FI}	Input Fall Time				2.0		2.0	µs
t_{CLH}	Clock High Time		(Note 6)	190		410		ns
t_{CLL}	Clock Low Time		(Note 6)	190		410		ns
t_{CSH}	Min. CS High Time		(Note 7)	240		500		ns
t_{CSS}	CS Setup Time			240		500		ns
t_{DIS}	Data Setup Time			100		100		ns
t_{HDS}	$\overline{HOLD}$ Setup Time			90		500		ns
t_{CSN}	CS Hold Time			240		500		ns
t_{DIN}	Data Hold Time			100		100		ns
t_{HDN}	HOLD Hold Time			90		240		ns
t_{PD}	Output Delay from Clock Low		C_L = 200 pF		240		240	ns
t_{DH}	Output Hold Time			0		0		ns
t_{LZ}	HOLD Output Low Z				100		240	ns
t_{DF}	Output Disable Time		C_L = 200 pF		240		500	ns
t_{HZ}	HOLD to Output Hi Z				100		240	ns
t_{WP}	Write Cycle Time		1-4 Bytes		10		10	ms

Capacitance T_A = 25°C, f = 1 MHz (Note 8)

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance	3	8	pF
C_{IN}	Input Capacitance	2	6	pF

AC Test Conditions

Output Load	C_L = 200pF
Input Pulse Levels	0.1 * V_{CC} - 0.9 * V_{CC}
Timing Measurement Reference Level	0.3 * V_{CC} - 0.7 * V_{CC}

Note 5: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

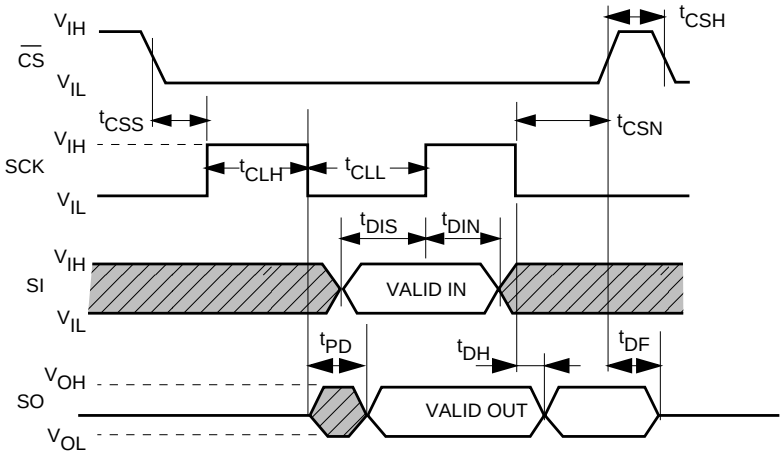
Note 6: Minimum Clock period. Specified minimum clock period for SCK frequency varies with temperature range. Extended temperature range ("E"), the minimum clock period is 476ns (2.1MHz). In the automotive temperature range, the minimum clock period is 1000ns (1MHz). For example, using the extended temperature range minimum, if t_{CLL} = 190ns, the minimum t_{CLH} is 286ns (190ns + 286ns = 476ns).

Note 7: $\overline{CS}$ must be brought high for a minimum of 250 ns (t_{CSH}) between consecutive instruction cycles.

Note 8: This parameter is periodically sampled and not 100% tested.

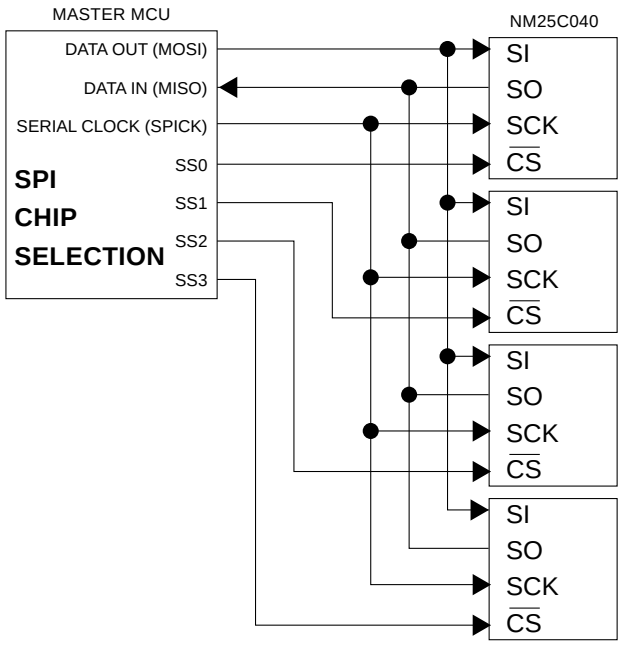
AC Test Conditions (Continued)

Synchronous Data Timing Diagram (Figure 1)



DS012401-3

SPI Serial Interface (Figure 2)



DS012401-4

Functional Description

MASTER: The device that generates the serial clock is designated as the master. The NM25C040 can never function as a master.

SLAVE: The NM25C040 always operates as a slave as the serial clock pin is always an input.

TRANSMITTER/RECEIVER: The NM25C040 has separate pins for data transmission (SO) and reception (SI).

MSB: The Most Significant Bit is the first bit transmitted and received.

CHIP SELECT: The chip is selected when pin $\overline{CS}$ is low. When the chip is *not* selected, data will not be accepted from pin SI, and the output pin SO is in high impedance.

SERIAL OP-CODE: The first byte transmitted after the chip is selected with $\overline{CS}$ going low contains the op-code that defines the operation to be performed.

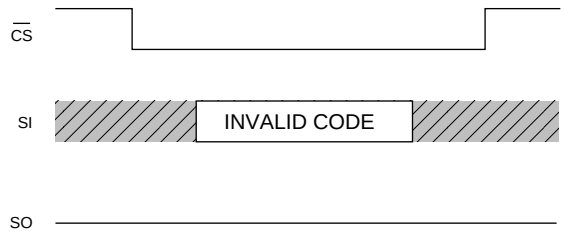
PROTOCOL: When connected to the SPI port of a 68HC11 microcontroller, the NM25C040 accepts a clock phase of 0 and a clock polarity of 0. The SPI protocol for this device defines the byte transmitted on the SI and SO data lines for proper chip operation. See Figure 4.

Data is clocked in on the positive SCK edge and out on the negative SCK edge.

HOLD: The $\overline{HOLD}$ pin is used in conjunction with the $\overline{CS}$ to select the device. Once the device is selected and a serial sequence is underway, $\overline{HOLD}$ may be forced low to suspend further serial communication with the device without resetting the serial sequence. Note that $\overline{HOLD}$ must be brought low while the SCK pin is low. The device must remain selected during this sequence. To resume serial communication $\overline{HOLD}$ is brought high while the SCK pin is low. Pins SI, SCK and SO are at a high impedance state during $\overline{HOLD}$. See Figure 5.

INVALID OP-CODE: After an invalid code is received, no data is shifted into the NM25C040, and the SO data output pin remains high impedance until a new $\overline{CS}$ falling edge reinitializes the serial communication. See Figure 3.

Invalid Op-Code (Figure 3)



DS012401-7

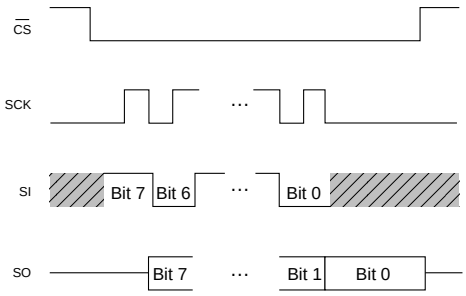
Instruction Set (Table 1)

Instruction Name	Instruction Format	Operation
WREN	0000X110	Set Write Enable Latch
WRDI	0000X100	Reset Write Enable Latch
RDSR	0000X101	Read Status Register
WRSR	0000X001	Write Status Register
READ	0000A011	Read Data from Memory Array
WRITE	0000A010	Write Data to Memory Array

Note: "A" represents MSB address bit A8
"X" = don't care

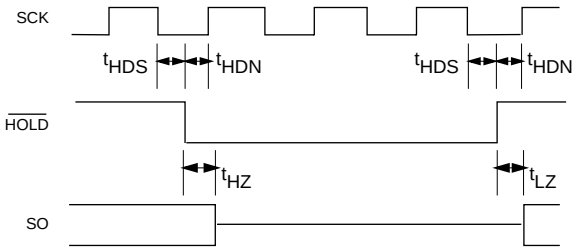
Functional Description (Continued)

SPI Protocol (Figure 4)



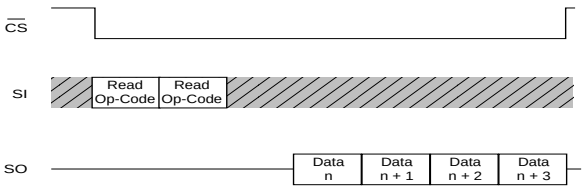
DS012401-5

HOLD Timing (Figure 5)



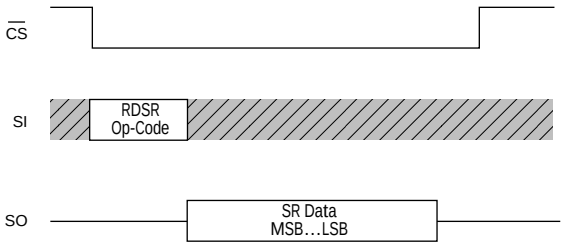
DS012401-6

Read Sequence (Figure 6)



DS012401-8

Read Status (Figure 7)



DS012401-9

Functional Description (Continued)

READ SEQUENCE: (One or More Bytes): Reading the memory via the serial SPI link requires the following sequence. The $\overline{CS}$ line is pulled low to select the device. The READ op-code (which includes A8) is transmitted on the SI line followed by the byte address (A7–A0) to be read. After this is done, data on the SI line becomes don't care. The data (D7–D0) at the address specified is then shifted out on the SO line. If only one byte is to be read, the $\overline{CS}$ line can be pulled back to the high level. It is possible to continue the READ sequence as the byte adress is automatically incremented and data will continue to be shifted out. When the highest address is reached (1FF), the address counter rolls over to lowest address (000) allowing the entire memory to be read in one continuous READ cycle. See Figure 6.

READ STATUS REGISTER (RDSR) : The Read Status Register (RDSR) instruction provides access to the status register is used to interrogate the READY/BUSY and WRITE ENABLE status of the chip. Two non-volatile status register bits are used to select one of four levels of BLOCK WRITE PROTECTION. The status register format is shown in Table 2.

Status Register Format (Table 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	1	1	BP1	BP0	WEN	$\overline{RDY}$

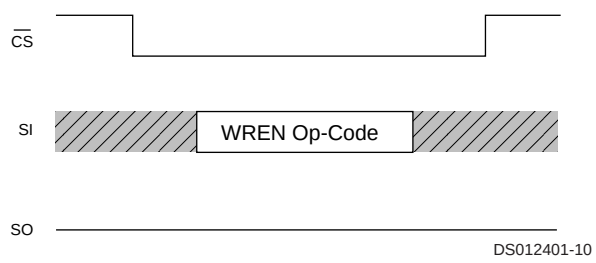
Status register Bit 0 = 0 ($\overline{RDY}$) indicates that the device is READY; Bit 0 = 1 indicates that a program cycle is in progress. Bit 1 = 0 (WEN) indicates that the device is not WRITE ENABLED; Bit 1 = 1 indicates that the device is WRITE ENABLED. Non-volatile status register Bits 2 and 3 (BP0 and BP1) indicate the level of BLOCK WRITE PROTECTION selected. The block write protection levels and corresponding status register control bits are shown in Table 3. Note that if a RDSR instruction is executed during a programming cycle only the $\overline{RDY}$ bit is valid. All other bits are 1s. See Figure 7.

Block Write Protection Levels (Table 3)

Level	Status Register Bits		Array Address Protected
	BP1	BP0	
0	0	0	None
1	0	1	180-1FF
2	1	0	100-1FF
3	1	1	000-1FF

WRITE ENABLE (WREN): When V_{CC} is applied to the chip, it "powers up" in the write disable state. Therefore, all programming modes must be preceded by a WRITE ENABLE (WREN) instruction. At the completion of a WRITE or WRSR cycle the device is automatically returned to the write disable state. Note that a WRITE DISABLE (WRDI) instruction will also return the device to the write disable state. See Figure 8.

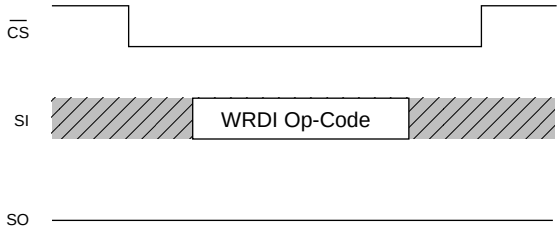
Write Enable (Figure 8)



DS012401-10

WRITE DISABLE (WRDI): To protect against accidental data disturbance the WRITE DISABLE (WRDI) instruction disables all programming modes. See Figure 9.

Write Disable (Figure 9)



DS012401-11

WRITE SEQUENCE: To program the device, the WRITE PROTECT ($\overline{WP}$) pin must be held high and two separate instructions must be executed. The chip must first be write enabled via the WRITE ENABLE instruction and then a WRITE instruction must be executed. Moreover, the address of the memory location(s) to be programmed must be outside the protected address field selected by the Block Write Protection Level. See Table 3.

A WRITE command requires the following sequence. The $\overline{CS}$ line is pulled low to select the device, then the WRITE op-code (which includes A8) is transmitted on the SI line followed by the byte address (A7-A0) and the corresponding data (D7-D0) to be written. Programming will start after the $\overline{CS}$ pin is forced back to a high level. Note that the LOW to HIGH transition of the $\overline{CS}$ pin must occur during the SCK low time immediately after clocking in the D0 data bit. See Figure 10.

The READY/BUSY status of the device can be determined by executing a READ STATUS REGISTER (RDSR) instruction. Bit 0 = 1 indicates that the WRITE cycle is still in progress and Bit 0 = 0 indicates that the WRITE cycle has ended. During the WRITE programming cycle (Bit 0 = 1) only the READ STATUS REGISTER instruction is enabled.

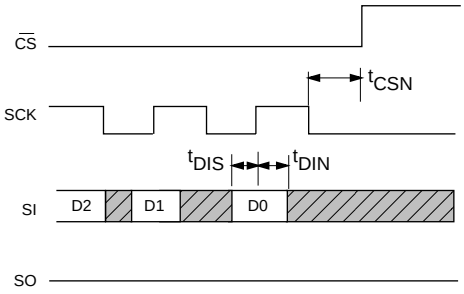
The NM25C040 is capable of a 4 byte PAGE WRITE operation. After receipt of each byte of data the two low order address bits are internally incremented by one. The seven high order bits of the address will remain constant. If the master should transmit more than 4 bytes of data, the address counter will "roll over," and the previously loaded data will be reloaded. See Figure 11.

At the completion of a WRITE cycle the device is automatically returned to the write disable state.

If the device is not WRITE enabled, the device will ignore the WRITE instruction and return to the standby state when $\overline{CS}$ is forced high. A new $\overline{CS}$ falling edge is required to re-initialize the serial communication. See Figure 11.

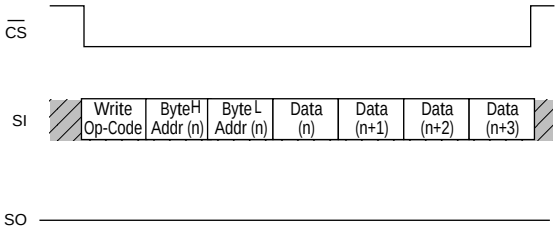
Functional Description (Continued)

Write Sequence (Figure 10)



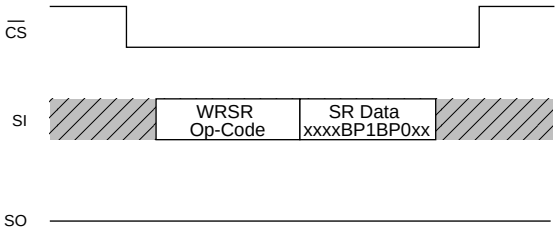
DS012401-12

Start Write Condition (Figure 11)



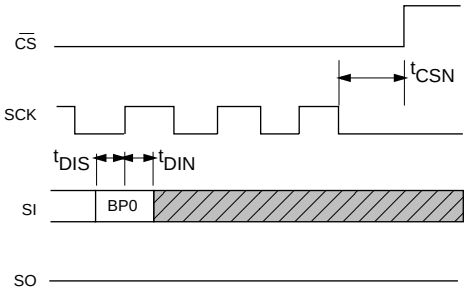
DS012401-13

Write Status Register (Figure 12)



DS012401-14

Start WRSR Condition (Figure 13)



DS012401-15

WRITE STATUS REGISTER (WRSR): The WRITE STATUS REGISTER (WRSR) instruction is used to program the non-volatile status register Bits 2 and 3 (BP0 and BP1). The WRITE PROTECT ($\overline{WP}$) pin must be held high and two separate instructions must be executed. The chip must first be write enabled via the WRITE ENABLE instruction and then a WRSR instruction must be executed.

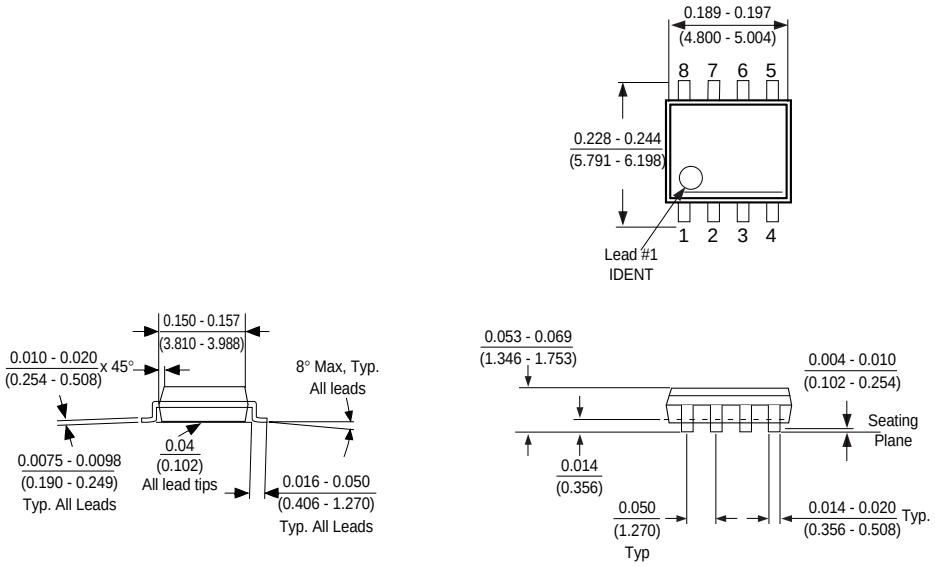
The WRSR command requires the following sequence. The $\overline{CS}$ line is pulled low to select the device and then the WRSR op-code is transmitted on the SI line followed by the data to be programmed. See Figure 12.

Note that the first four bits are don't care bits followed by BP1 and BP0 then two additional don't care bits. Programming will start after the $\overline{CS}$ pin is forced back to a high level. As in the WRITE instruction the LOW to HIGH transition of the $\overline{CS}$ pin must occur during the SCK low time immediately after clocking in the last don't care bit. See Figure 13.

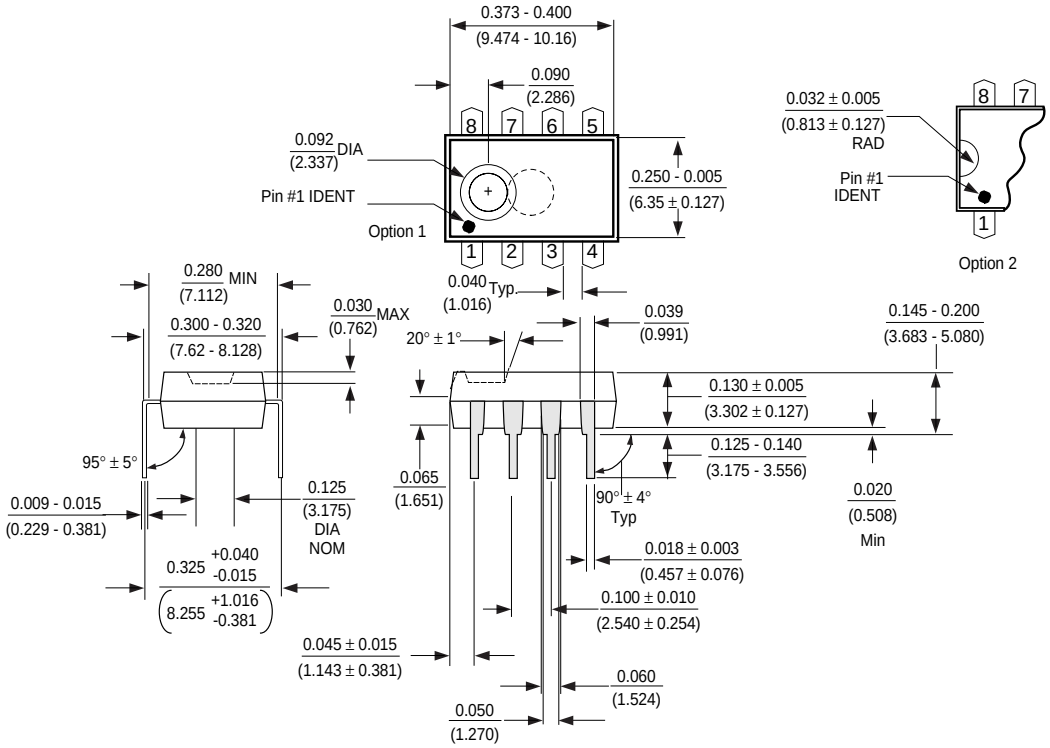
The READY/BUSY status of the device can be determined by executing a READ STATUS REGISTER (RDSR) instruction. Bit 0 = 1 indicates that the WRSR cycle is still in progress and Bit 0 = 0 indicates that the WRSR cycle has ended.

At the completion of a WRITE cycle the device is automatically returned to the write disable state.

Physical Dimensions inches (millimeters) unless otherwise noted

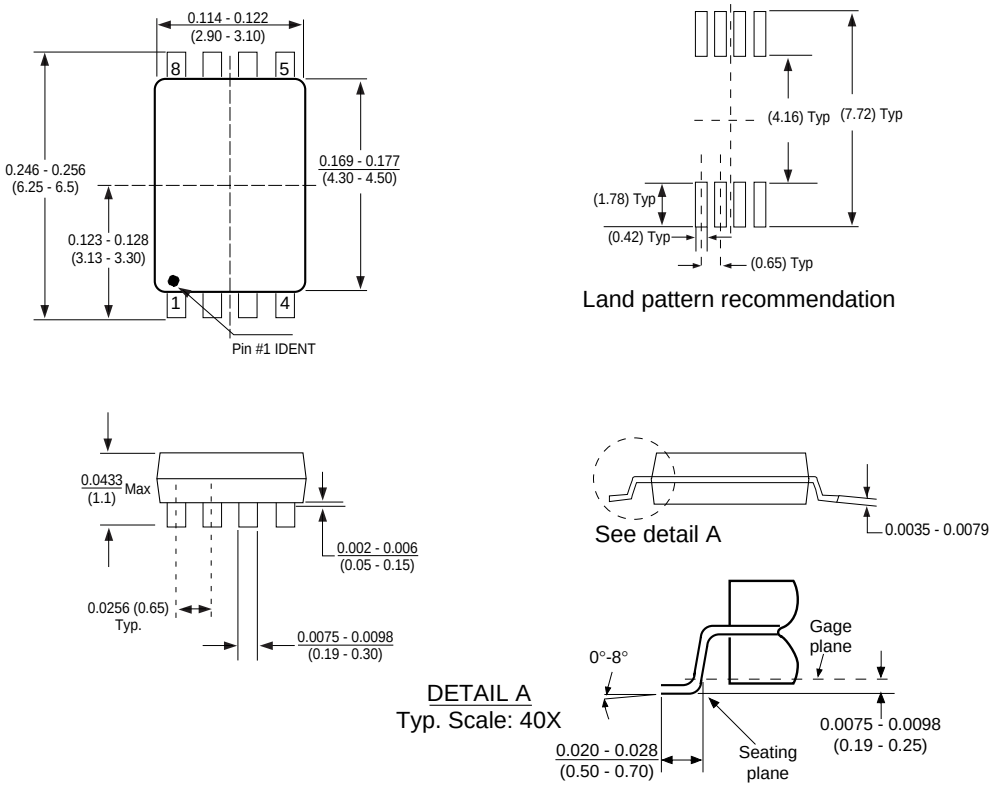


Molded Small Out-Line Package (M8)
Package Number M08A



Molded Dual-In-Line Package (N)
Package Number N08E

Physical Dimensions inches (millimeters) unless otherwise noted



Notes: Unless otherwise specified
1. Reference JEDEC registration MO153. Variation AA. Dated 7/93

8-Pin Molded TSSOP, JEDEC (MT8)
Package Number MTC08

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

October 1998

NM27C010
1,048,576-Bit (128K x 8) High Performance CMOS EPROM

General Description

The NM27C010 is a high performance, 1,048,576-bit Electrically Programmable UV Erasable Read Only Memory. It is organized as 128K-words of 8 bits each. Its pin-compatibility with byte-wide JEDEC EPROMs enables upgrades through 8 Mbit EPROMs. The "Don't Care" feature during read operations allows memory expansions from 1M to 8M bits with no printed circuit board changes.

The NM27C010 can directly replace lower density 28-pin EPROMs by adding an A16 address line and V_{CC} jumper. During the normal read operation $\overline{PGM}$ and V_{PP} are in a "Don't Care" state which allows higher order addresses, such as A17, A18, and A19 to be connected without affecting the normal read operation. This allows memory upgrades to 8M bits without hardware changes. The NM27C010 is also offered in a 32-pin plastic DIP with the same upgrade path.

The NM27C010 provides microprocessor-based systems extensive storage capacity for large portions of operating system and application software. Its 70 ns access time provides no-wait-state operation with high-performance CPUs. The NM27C010 offers a single chip solution for the code storage requirements of 100% firmware-based equipment. Frequently-used software routines are quickly executed from EPROM storage, greatly enhancing system utility.

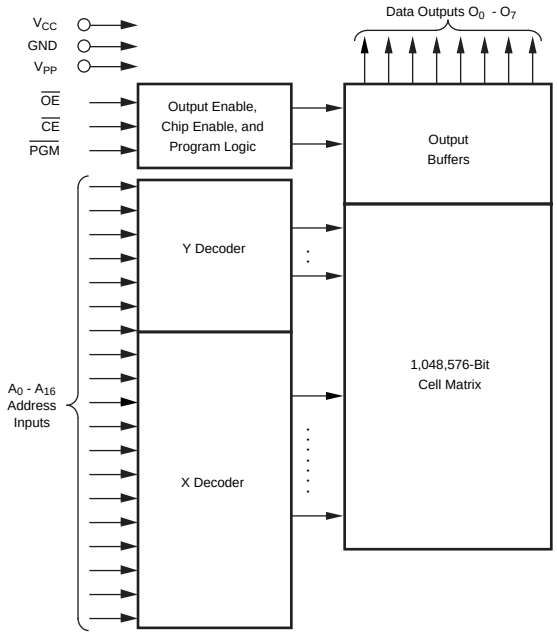
The NM27C010 is manufactured using Fairchild's advanced CMOS AMG™ EPROM technology.

The NM27C010 is one member of a high density EPROM Family which range in densities up to 4 Megabit.

Features

- High performance CMOS
  - —70 ns access time
- Fast turn-off for microprocessor compatibility
- Simplified upgrade path
  - —V_{PP} and PGM are "Don't Care" during normal read operation
- Manufacturers identification code
- Fast programming
- JEDEC standard pin configurations
  - —32-pin PDIP package
  - —32-pin PLCC package
  - —32-pin CERDIP package

Block Diagram



DS010798-1

Connection Diagrams

DIP PIN CONFIGURATIONS

27C080	27C040	27C020	27C512	27C256	DIP NM27C010			27C256	27C512	27C020	27C040	27C080
A_{19}	XX/V_{PP}	XX/V_{PP}			XX/V_{PP}	1	32			V_{CC}	V_{CC}	V_{CC}
A_{16}	A_{16}	A_{16}			A_{16}	2	31			$XX/\overline{PGM}$	A_{18}	A_{18}
A_{15}	A_{15}	A_{15}	A_{15}	V_{PP}	A_{15}	3	30	V_{CC}	V_{CC}	A_{17}	A_{17}	A_{17}
A_{12}	A_{12}	A_{12}	A_{12}	A_{12}	A_{12}	4	29	A_{14}	A_{14}	A_{14}	A_{14}	A_{14}
A_7	A_7	A_7	A_7	A_7	A_7	5	28	A_{13}	A_{13}	A_{13}	A_{13}	A_{13}
A_6	A_6	A_6	A_6	A_6	A_6	6	27	A_8	A_8	A_8	A_8	A_8
A_5	A_5	A_5	A_5	A_5	A_5	7	26	A_9	A_9	A_9	A_9	A_9
A_4	A_4	A_4	A_4	A_4	A_4	8	25	A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
A_3	A_3	A_3	A_3	A_3	A_3	9	24	$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_2	A_2	A_2	A_2	A_2	A_2	10	23	A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
A_1	A_1	A_1	A_1	A_1	A_1	11	22	$\overline{CE}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}/\overline{PGM}$
A_0	A_0	A_0	A_0	A_0	A_0	12	21	O_7	O_7	O_7	O_7	O_7
O_0	O_0	O_0	O_0	O_0	O_0	13	20	O_6	O_6	O_6	O_6	O_6
O_1	O_1	O_1	O_1	O_1	O_1	14	19	O_5	O_5	O_5	O_5	O_5
O_2	O_2	O_2	O_2	O_2	O_2	15	18	O_4	O_4	O_4	O_4	O_4
GND	GND	GND	GND	GND	GND	16	17	O_3	O_3	O_3	O_3	O_3

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Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the NM27C010 pins.

Commercial Temperature Range

(0°C to +70°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C010 Q, V, N 70	70
NM27C010 Q, V, N 90	90
NM27C010 Q, V, N 120	120
NM27C010 Q, V, N 150	150

Extended Temperature Range

(-40°C to +85°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C010 QE, VE, NE 70	70
NM27C010 QE, VE, NE 90	90
NM27C010 QE, VE, NE 120	120
NM27C010 QE, VE, NE 150	150

Package Types: NM27C010 Q, N, V XXX

Q = Quartz-Windowed Ceramic DIP package

V = PLCC package

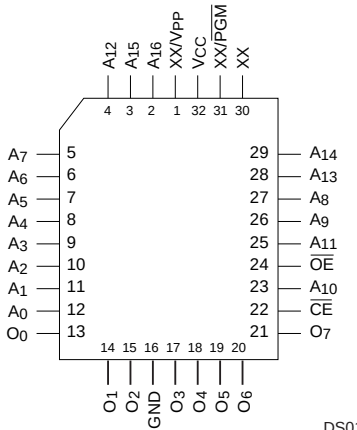
N = Plastic DIP package

- All packages conform to JEDEC standard.
- All versions are guaranteed to function at slower speeds.

Pin Names

A0–A16	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)

PLCC Pin Configuration



DS010798-3

Top View

Absolute Maximum Ratings (Note 1)

Storage Temperature	-65°C to +150°C
All Input Voltages Except A9 with Respect to Ground (Note 10)	-0.6V to +7V
V_{PP} and A9 with Respect to Ground	-0.6V to +14V
V_{CC} Supply Voltage with Respect to Ground	-0.6V to +7V
ESD Protection	>2000V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} + 1.0V to GND - 0.6V

Operating Range

Range	Temperature	V_{CC}	Tolerance
Commercial	0°C to +70°C	+5V	±10%
Extended	-40°C to +85°C	+5V	±10%

DC Read Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	Test Conditions		Min	Max	Units
V_{IL}	Input Low Level			-0.5	0.8	V
V_{IH}	Input High Level			2.0	V_{CC} +1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -2.5 mA		3.5		V
I_{SB1}	V_{CC} Standby Current (CMOS)	$\overline{CE} = V_{CC} \pm 0.3V$			100	µA
I_{SB2}	V_{CC} Standby Current (TTL)	$\overline{CE} = V_{IH}$			1	mA
I_{CC}	V_{CC} Active Current	$\overline{CE} = \overline{OE} = V_{IL}$ I/O = 0 mA	f = 5 MHz		30	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$			10	µA
V_{PP}	V_{PP} Read Voltage			V_{CC} - 0.7	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5 or GND		-1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND		-10	10	µA

AC Read Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	70		90		120		150		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		70		90		120		150	
t_{CE}	$\overline{CE}$ to Output Delay		70		90		120		150	
t_{OE}	$\overline{OE}$ to Output Delay		35		40		50		50	
t_{DF} (Note 2)	Output Disable to Output Float		30		35		35		45	ns
t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		0		

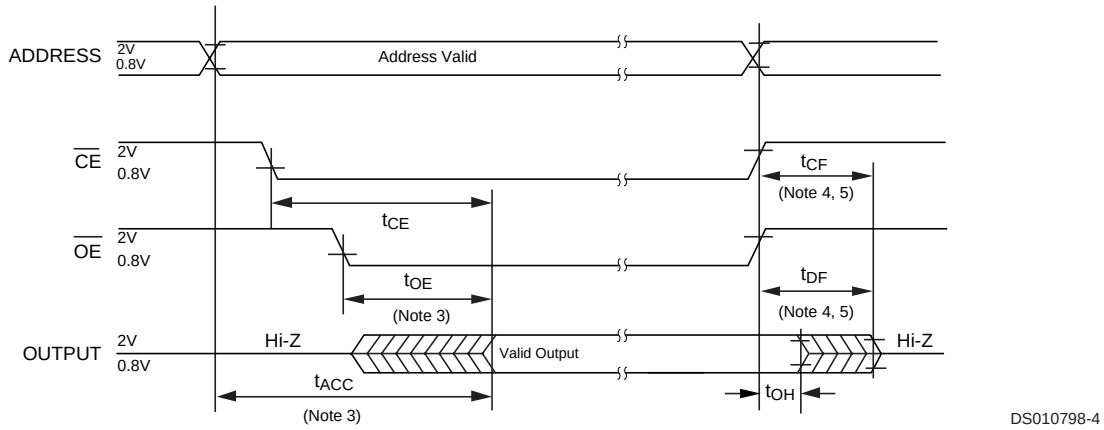
Capacitance T_A = +25°C, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	6	15	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	10	15	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Note 6), (Note 7), and (Note 9)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE®, the measured V_{OH1} (DC) - 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: I_{OL} = 1.6 mA, I_{OH} = -400 µA.
C_L: 100 pF includes fixture capacitance.

Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to -2.0V for 20 ns Max.

Programming Characteristics (Note 11), (Note 12), (Note 13), and (Note 14)

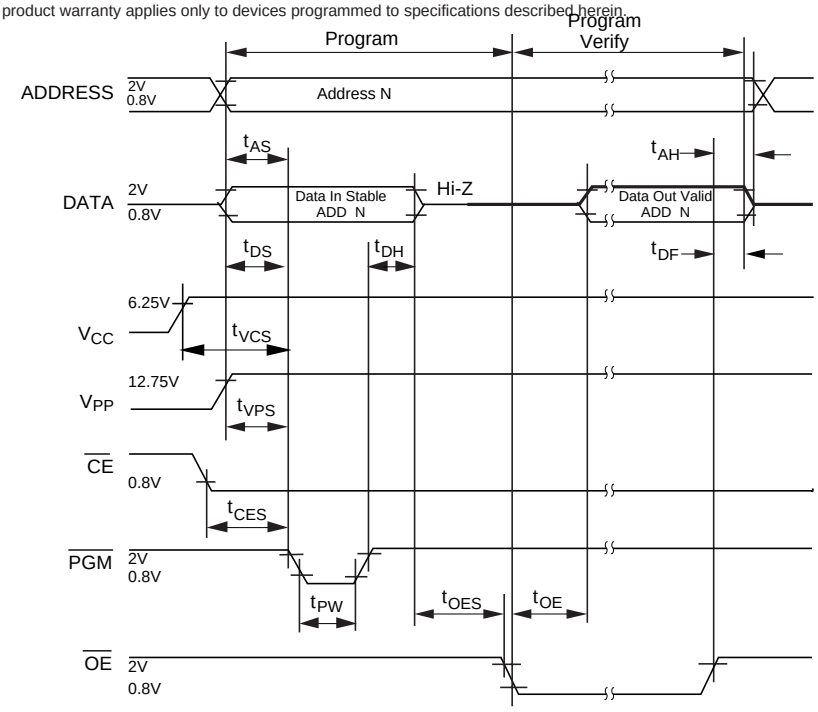
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			µs
t_{OES}	$\overline{OE}$ Setup Time		1			µs
t_{CES}	$\overline{CE}$ Setup Time	$\overline{OE}$ = V_{IH}	1			µs
t_{DS}	Data Setup Time		1			µs
t_{VPS}	V_{PP} Setup Time		1			µs
t_{VCS}	V_{CC} Setup Time		1			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		1			µs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE}$ = V_{IL}	0		60	ns
t_{PW}	Program Pulse Width		45	50	105	µs

Programming Characteristics (Note 11), (Note 12), (Note 13), and (Note 14) (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IL}$			15	mA
I_{CC}	V_{CC} Supply Current				20	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.2	6.5	6.75	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

Programming Waveforms (Note 13)

Note 11: Fairchild's standard product warranty applies only to devices programmed to specifications described herein.



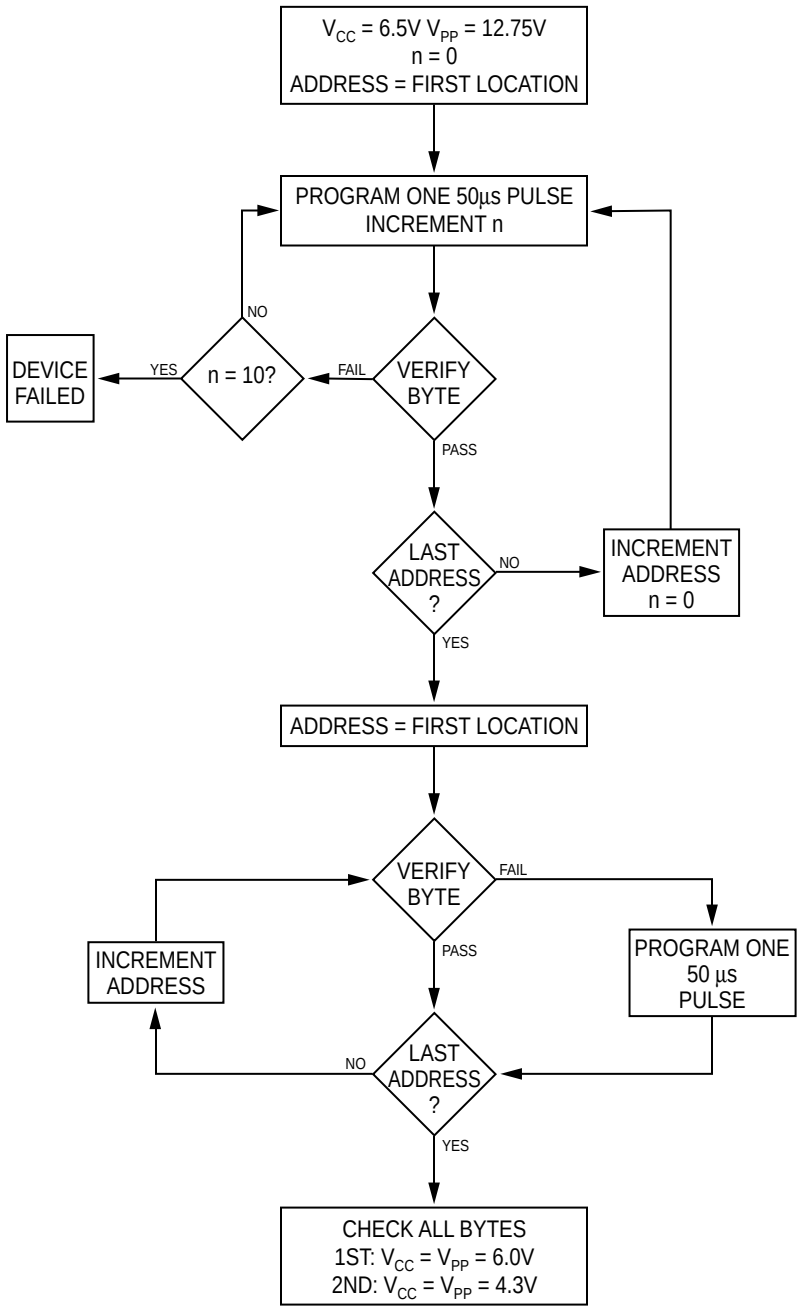
DS010798-5

Note 12: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 13: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 µF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 14: During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

Turbo Programming Algorithm Flow Chart



Note: The standard National Semiconductor Algorithm may also be used but it will have longer programming time.

DS010798-6

FIGURE 1.

Functional Description

DEVICE OPERATION

The six modes of operation of the EPROM are listed in Table 1. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.5V during the three programming modes, and at 5V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from 165 mW to 0.55 mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the $\overline{OE}$ input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Tying

Because the EPROM is usually used in larger memory arrays, Fairchild has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

1. the lowest possible memory power dissipation, and
2. complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on the V_{PP} or A9 pin will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 µF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the Turbo Programming Algorithm shown in Figure 1. Each Address is programmed with a series of 50 µs pulses until it verifies good, up to a maximum of 10 pulses. Most memory cells will program with a single 50 µs pulse.

The EPROM must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled EPROM.

Program Inhibit

Programming multiple EPROM's in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel EPROM may be common. A TTL low level program pulse applied to an EPROM's $\overline{PGM}$ input with $\overline{CE}$ at V_{IL} and V_{PP} at 12.75V will program that EPROM. A TTL high level $\overline{CE}$ input inhibits the other EPROM's from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC}, except during programming and program verify.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's indentification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table 2, specifically identifies the manufacturer and device type. The code for the NM27C010 is "8F86", where "8F" designates that it is made by Fairchild Semiconductor, and "86" designates a 1 Megabit (128K x 8) part.

The code is accessed by applying 12V ±0.5V to address pin A9. Addresses A1–A8, A10–A16, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O0–07. Proper code access is only guaranteed at 25°C ± 5°C.

Functional Description (Continued)

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å – 4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increases as the square of the distance from the lamp. (if distance is doubled the erasure time increases by factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

MODE SELECTION

The modes of operation of the NM27C010 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 for device signature.

TABLE 1. Modes Selection

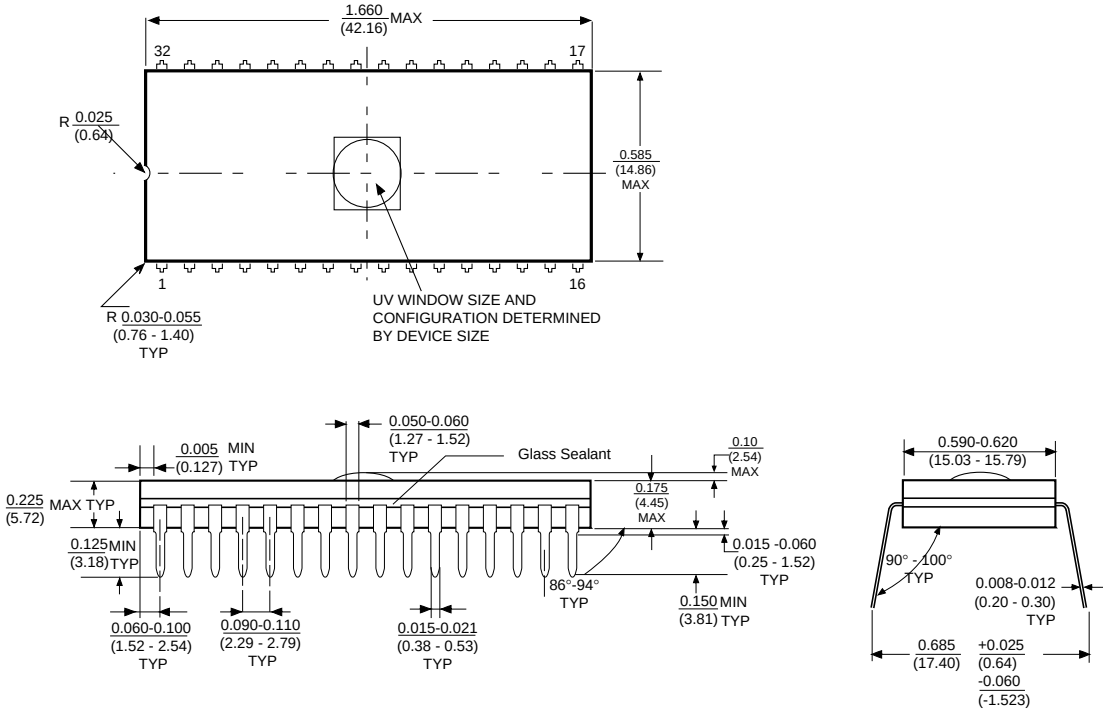
Mode \ Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X (Note 15)	X	5.0V	D_{OUT}
Output Disable	X	V_{IH}	X	X	5.0V	High Z
Standby	V_{IH}	X	X	X	5.0V	High Z
Programming	V_{IL}	V_{IH}	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	X	X	12.75V	6.25V	High Z

Note 15: X can be V_{IL} or V_{IH}.

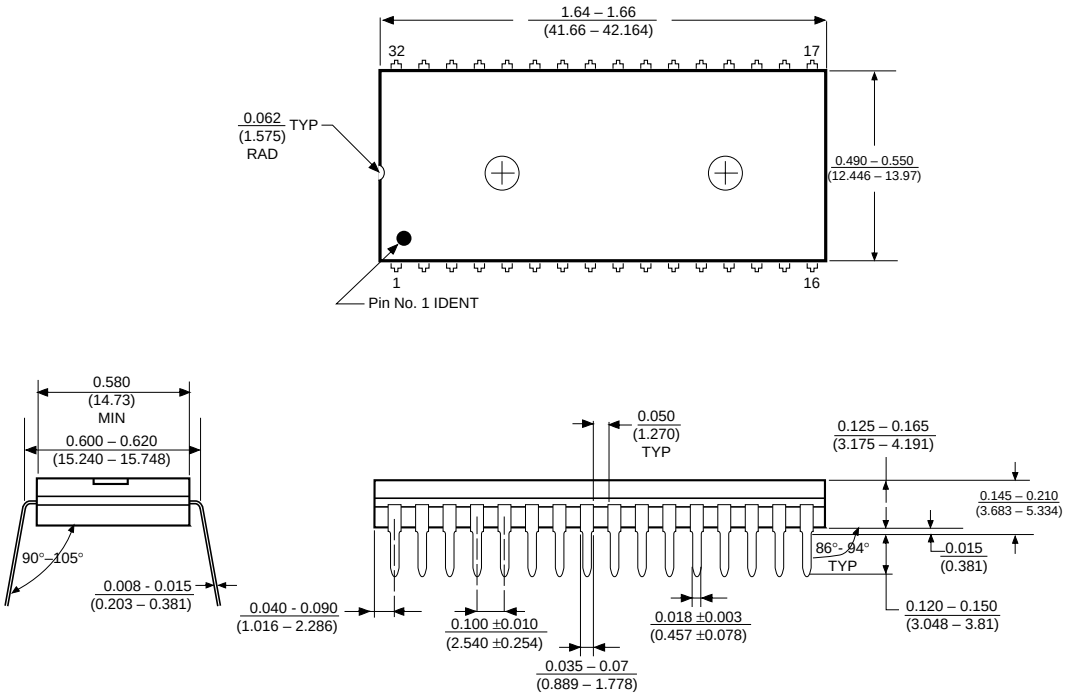
TABLE 2. Manufacturer's Identification Code

Pins	A0 (12)	A9 (26)	O7 (21)	O6 (20)	O5 (19)	O4 (18)	O3 (17)	O2 (15)	O1 (14)	O0 (13)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	1	0	0	0	0	1	1	0	86

Physical Dimensions inches (millimeters) unless otherwise noted

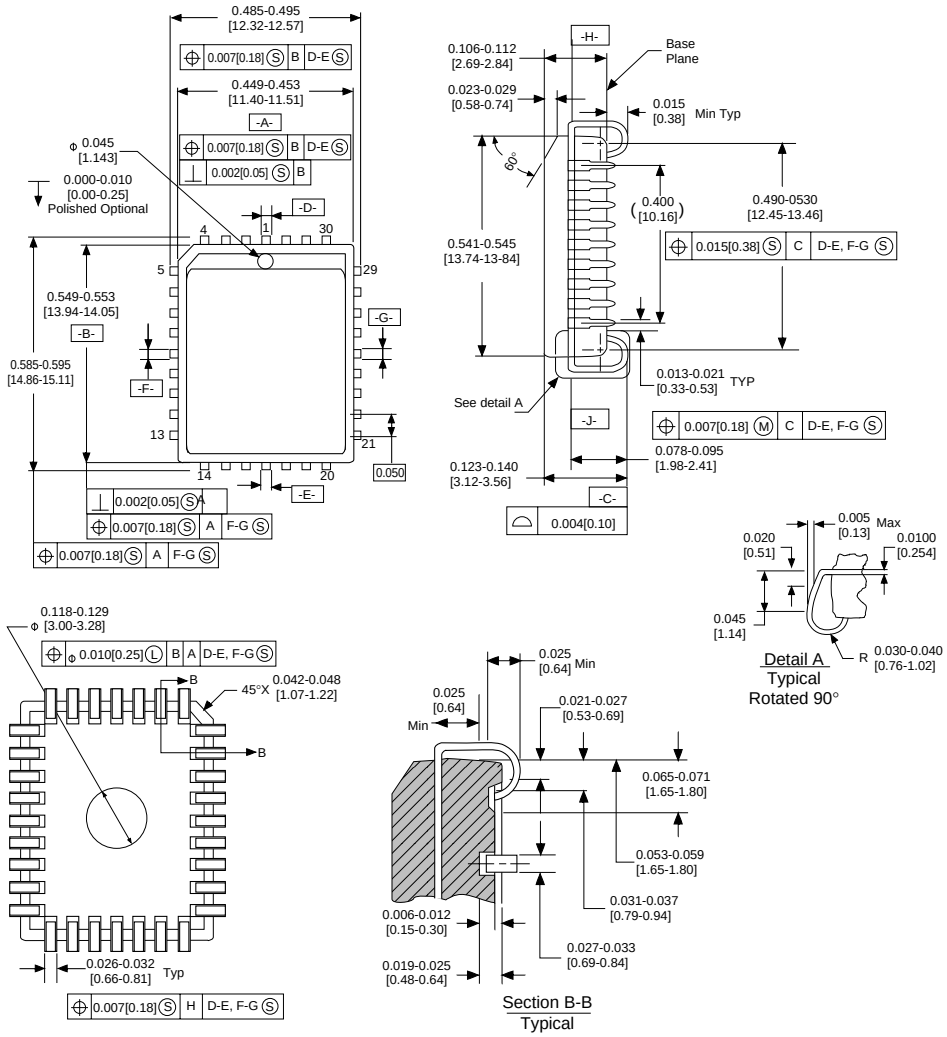


32-Lead EPROM Ceramic Dual-In-Line Package (Q)
Order Number NM27C010QXXX
Package Number J32AQ



32-Lead Molded Dual-In-Line Package (N)
Order Number NM27C010NXXX
Package Number

Physical Dimensions inches (millimeters) unless otherwise noted



32-Lead PLCC Package
Order Number NM27C010VXXX
Package Number VA32A

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

July 1998

NM27C020
2,097,152-Bit (256K x 8) UV Erasable CMOS EPROM

General Description

The NM27C020 is a high speed 2 Megabit CMOS UV-EPROM manufactured on Fairchild's advanced sub-micron technology. Utilizing the AMG architecture, this advanced CMOS process delivers high speeds while consuming low power.

The NM27C020 provides microprocessor-based systems extensive storage capacity for large portions of operating systems and application software. Its 100ns access time provides no-wait-state operation with high-performance CPUs.

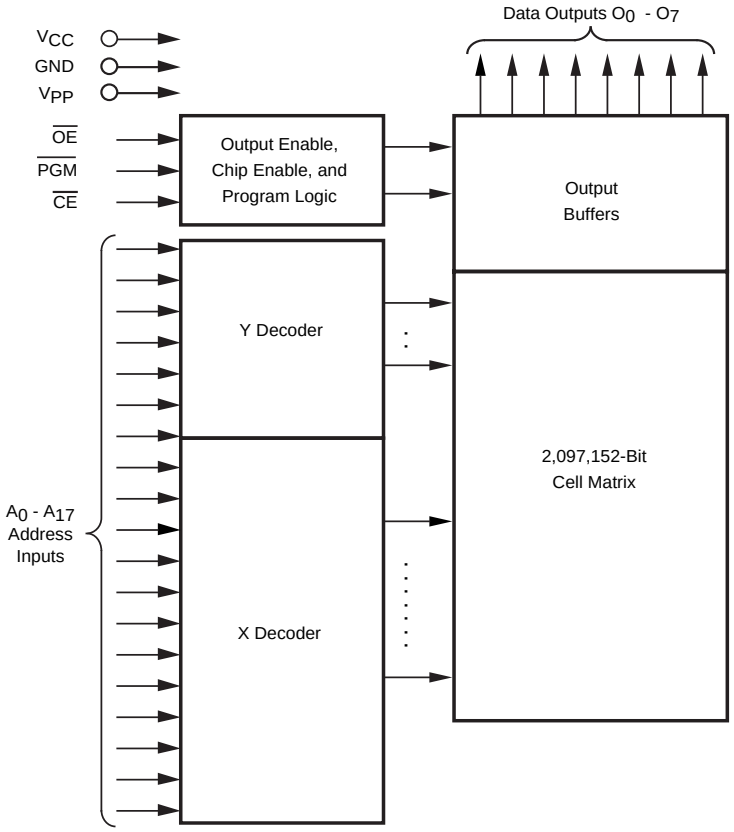
The NM27C020 offers a single chip solution for the code storage requirements of 100% firmware-based equipment. Frequently-used software routines are quickly executed from EPROM storage, greatly enhancing system utility.

The NM27C020 is manufactured using Fairchild's advanced CMOS AMG EPROM technology, and is one member of a high density Fairchild EPROM series family which range in densities up to 4Mb.

Features

- High performance CMOS
  - 100 ns access time
- Simplified upgrade path
  - —V_{PP} and PGM are "Don't Care" during normal read operation
- Manufacturers identification code
- JEDEC Standard Pin Configuration
  - 32-pin CERDIP package
  - 32-pin PLCC package
  - 32-pin PDIP package

Block Diagram



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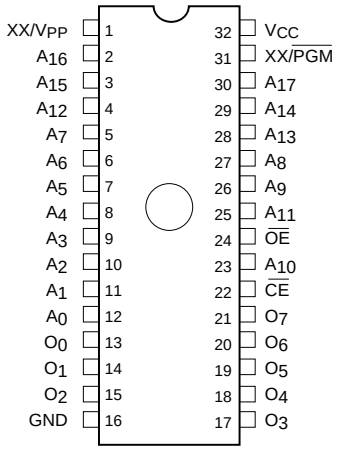
Connection Diagrams

27C080	27C040	27C010	27C512	27C256
A19	XX/V_{PP}	XX/V_{PP}		
A16	A16	A16		
A15	A15	A15	A15	V_{PP}
A12	A12	A12	A12	A12
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O0	O0	O0	O0	O0
O1	O1	O1	O1	O1
O2	O2	O2	O2	O2
GND	GND	GND	GND	GND



27C256	27C512	27C010	27C040	27C080
		V_{CC}	V_{CC}	V_{CC}
		XX/PGM	A18	A18
V_{CC}	V_{CC}	XX	A17	A17
A14	A14	A14	A14	A14
A13	A13	A13	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
A11	A11	A11	A11	A11
OE	OE/V_{PP}	OE	OE	OE/V_{PP}
A10	A10	A10	A10	A10
CE/PGM	CE/PGM	CE/PGM	CE	CE/PGM
O7	O7	O7	O7	O7
O6	O6	O6	O6	O6
O5	O5	O5	O5	O5
O4	O4	O4	O4	O4
O3	O3	O3	O3	O3

Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the NM27C020 pins.

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Commercial Temperature Range (0°C to +70°C) V_{CC} = 5V ±10%

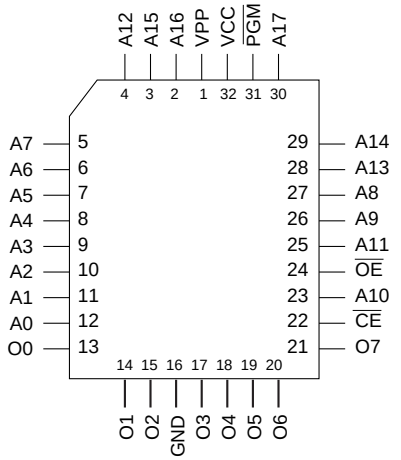
Parameter/Order Number	Access Time (ns)
NM27C020 Q, V, N 100	100
NM27C020 Q, V, N 120	120
NM27C020 Q, V, N 150	150

All versions are guaranteed to function at slower speeds.

Extended Temperature Range (-40°C to +85°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C020 QE, VE, TE, NE 120	120
NM27C020 QE, VE, TE, NE 150	150

PLCC Pin Configuration



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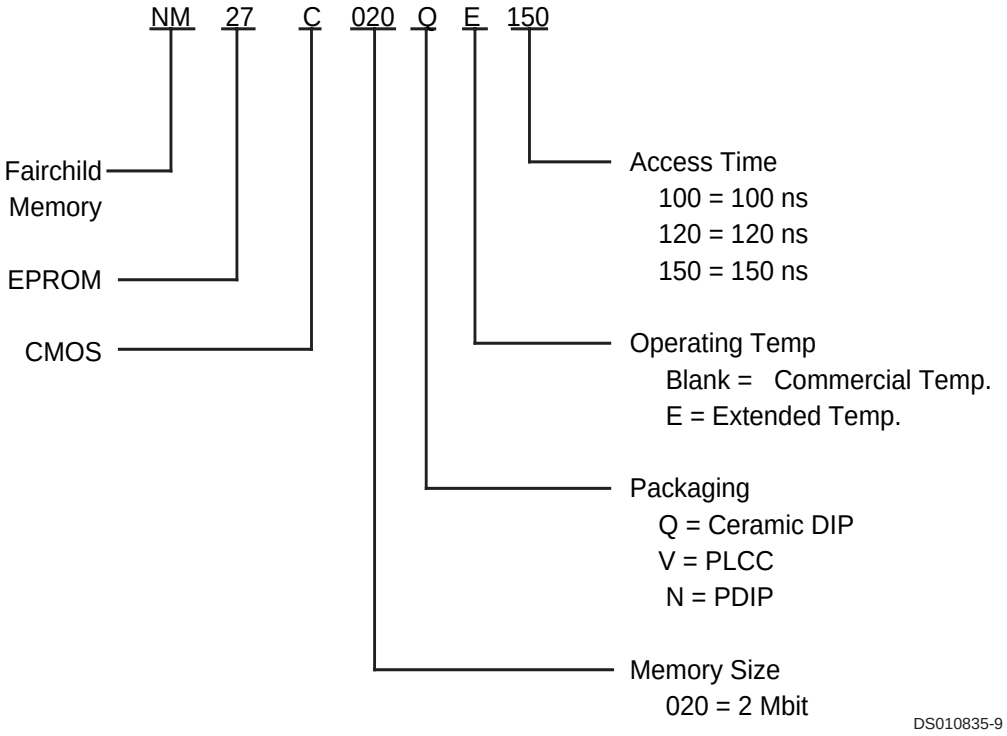
Top View

Pin Names

A0 –A17	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0 –O7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)

Connection Diagrams (Continued)

Ordering Information



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Absolute Maximum Ratings (Note 1)

Storage Temperature	-65°C to +125°C
All Input Voltage Except A9 with Respect to Ground (Note 13)	-0.6V to +7V
V_{PP} and A9 with Respect to Ground	-0.6V to +14V
V_{CC} Supply Voltage with Respect to Ground	-0.6V to +7V
ESD Protection	>2000V
All Output Voltages with Respect to Ground (Note 13)	V_{CC} + 10V to GND -0.6V

Operating Range

Range	Temperature	V_{CC}	Tolerance
Commercial	0°C to +70°C	+5V	±10
Industrial	-40°C to +85°C	+5V	±10%

DC Read Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	Test Conditions		Min	Max	Units
V_{IL}	Input Low Level			-0.5	0.8	V
V_{IH}	Input High Level			2.0	V_{CC} +1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			-0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA		3.5		V
I_{SB1} (Note 4)	V_{CC} Standby Current (CMOS)	$\overline{CE} = V_{CC} \pm 0.3V$			100	µA
I_{SB2}	V_{CC} Standby Current (TTL)	$\overline{CE} = V_{IH}$			1	mA
I_{CC} (Note 2)	V_{CC} Active Current	$\overline{CE}$, $\overline{OE} = V_{IL}$ I/O = 0 mA, f = 5 MHz Inputs = V_{IH} or V_{IL}	Commercial Industrial		30 30	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$			10	µA
VPP	V_{PP} Read Voltage			VCC - 0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5 or GND		-1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND		-10	10	µA

AC Read Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	100		120		150		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		100		120		150	ns
t_{CE}	$\overline{CE}$ to Output Delay		100		120		150	ns
t_{OE}	$\overline{OE}$ to Output Delay		40		45		50	ns
t_{DF} (Note 3)	Output Disable to Output Float		40		45		50	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		ns

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

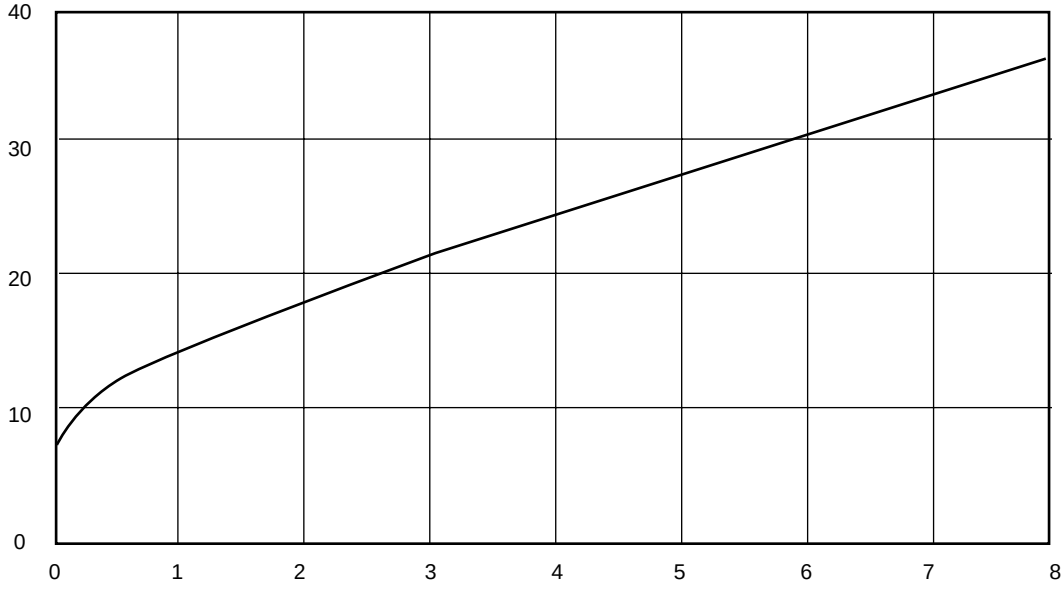
Note 2: The supply current is the sum of I_{CC} and I_{PP}. The maximum current value is with Outputs O0 to O7 unloaded.

Note 3: This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven-see timing diagram.

Note 4: CMOS inputs: V_{IL} = GND 10.3V, $V_{IH} = V_{CC}$ 10.3V.

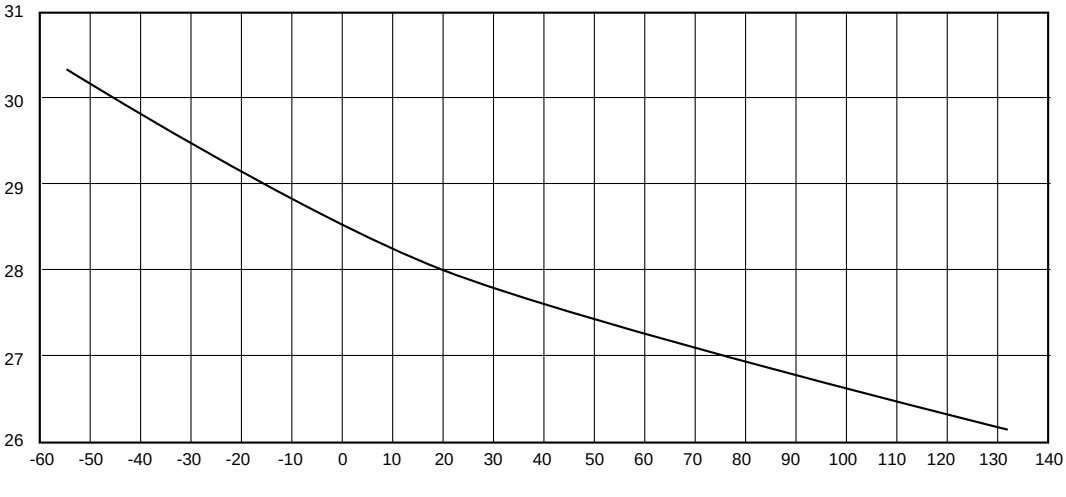
AC Read Characteristics (Continued)

I_{CC} vs. Frequency



Frequency (MHz)

I_{CC} vs. Temperature



Temperature (IC)

Capacitance T_A = +25°C, f = 1 MHz (Note 5)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	9	15	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	15	pF

AC Test Conditions

Output Load 1 TTL Gate and C_L = 100 pF (Note 11)

Input Rise and Fall Times ≤5 ns

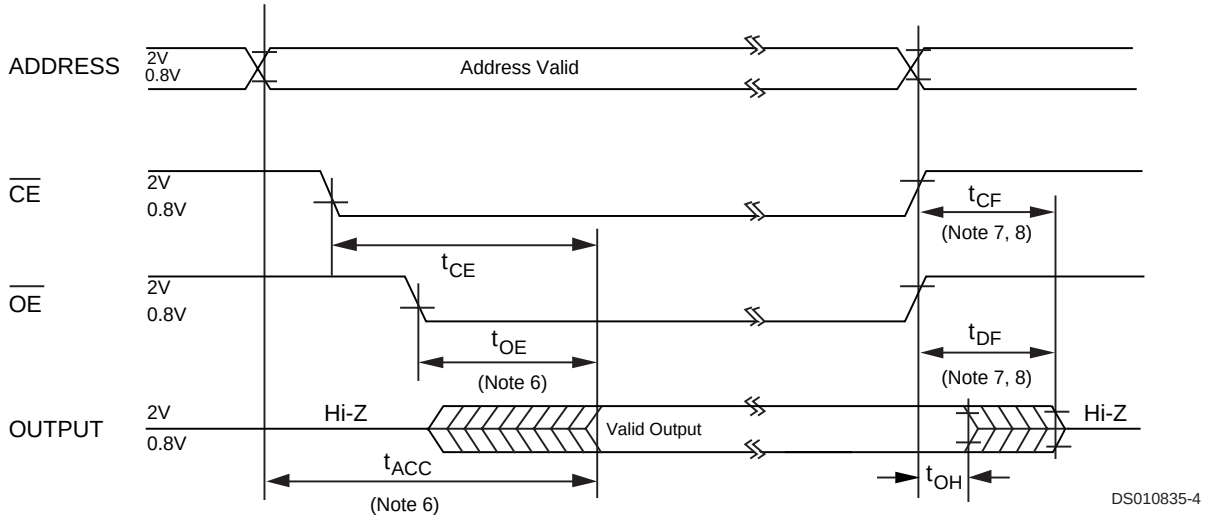
Input Pulse Levels 0.45V to 2.4V

Timing Measurement Reference Level (Note 13)

Inputs 0.8V and 2V

Outputs 0.8V and 2V

AC Waveforms (Notes 9, 10, 12)



Note 5: This parameter is only sampled and is not 100% tested.

Note 6: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 7: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE®, the measured V_{OH1} (DC) - 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 8: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 9: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 MF ceramic capacitor be used on every device between V_{CC} and GND.

Note 10: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 11: 1 TTL Gate: I_{OL} = 1.6 mA, I_{OH} = -400 µA.
C_L: 100 pF includes fixture capacitance.

Note 12: V_{PP} may be connected to V_{CC} except during programming.

Note 13: Inputs and outputs can undershoot to -2.0V for 20 ns Max.

Programming Characteristics (Notes 14, 15, 16, 17)

Symbol	Parameter	Condition	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			µs
t_{OES}	$\overline{OE}$ Setup Time		1			µs
t_{CES}	$\overline{CE}$ Setup Time	$\overline{OE} = V_{IH}$	1			µs
t_{DS}	Data Setup Time		1			µs
t_{VPS}	V_{PP} Setup Time		1			µs
t_{VCS}	V_{CC} Setup Time		1			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		1			µs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		45	50	105	µs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IL}$			15	mA
I_{CC}	V_{CC} Supply Current				20	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.25	6.5	6.75	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

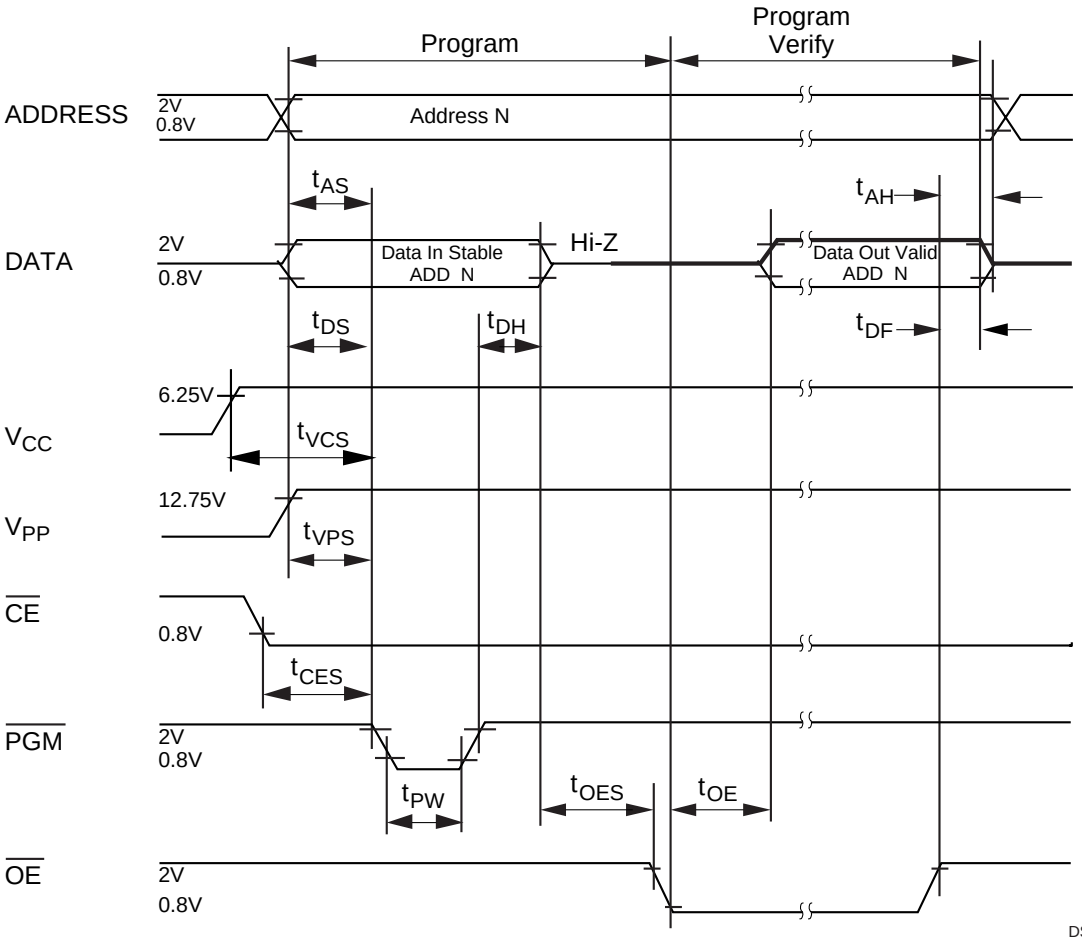
Note 14: Fairchild's standard product warranty applies only to devices programmed to specifications described herein.

Note 15: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 16: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 µF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 17: During power up the $\overline{PGM}$ pin must be brought high (≥V IH) either coincident with or before power is applied to V PP .

Programming Waveforms (Note 16)



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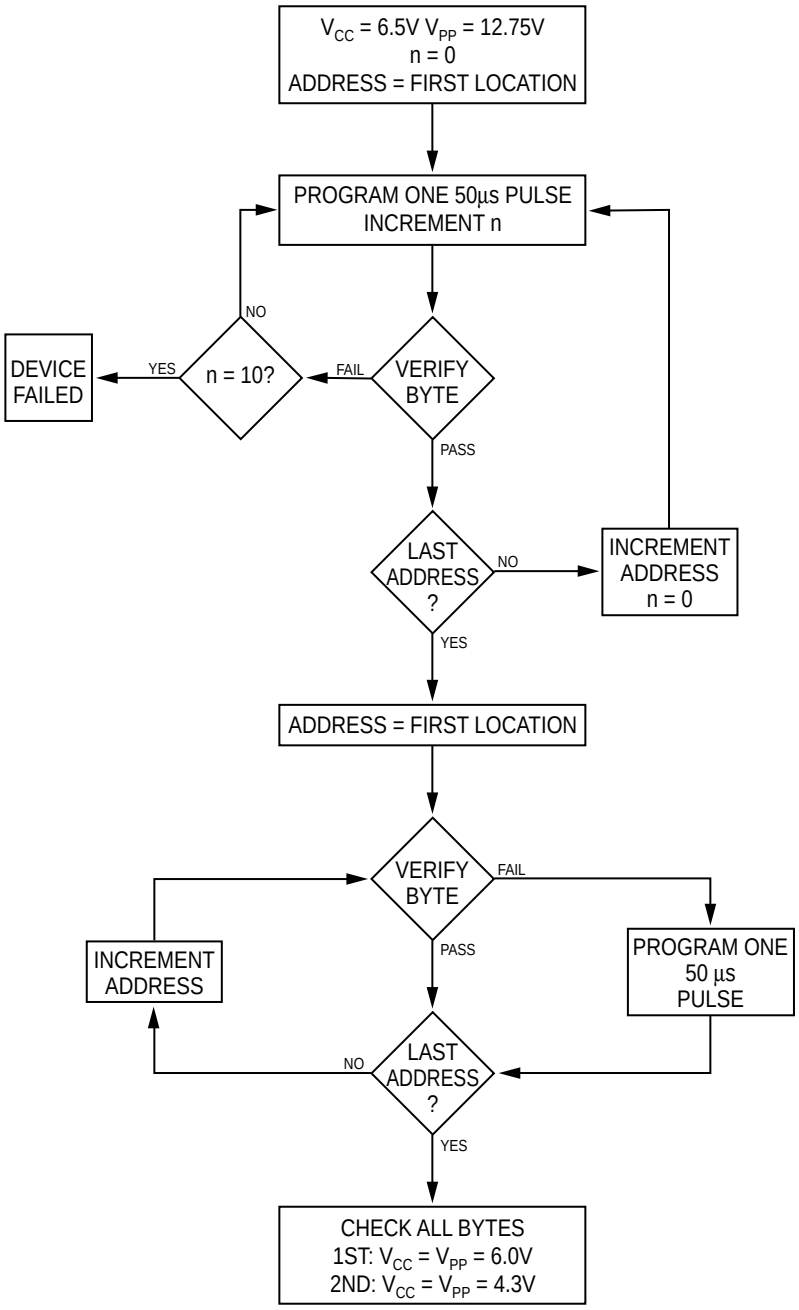
Turbo Programming Algorithm Flow Chart



Note: The standard National Semiconductor Algorithm may also be used but it will have longer programming time.

DS010835-6

FIGURE 1.

Functional Description

DEVICE OPERATION

The six modes of operation of the device are listed in Table 1. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.5V during the three programming modes, and at 5V in the other three modes.

Read Mode

The part has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from 220 mW to 0.55 mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because the part is usually used in larger memory arrays, Fairchild has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

1. the lowest possible memory power dissipation, and
2. complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all selected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the device.

Initially, and after each erasure, all bits of the device are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The part is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 µF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the Turbo Programming Algorithm shown in Figure 1. Each Address is programmed with a series of 50 µs pulses until it verifies good, up to a maximum of 10 pulses. Most memory cells will program with a single 50 µs pulse. (The standard National Semiconductor Algorithm may also be used but it will have longer programming time.) The EPROM must not be programmed with a DC signal applied to the $\overline{PGM}$ input. Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the PGM input programs the paralleled EPROM.

MODE SELECTION

The modes of operation of the NM27C020 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 for device signature.

TABLE 1. Modes Selection

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X (Note 18)	X	5.0V	D_{OUT}
Output Disable	X	V_{IH}	X	X	5.0V	H igh Z
Standby	V_{IH}	X	X	X	5.0V	High Z
Programming	V_{IL}	V_{IH}	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	X	X	12.75V	6.25V	High Z

Note 18: X can be V_{IL} or V_{IH}.

Functional Description (Continued)

Program Inhibit

Programming multiple EPROM's in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$) of the parallel EPROM may be common. A TTL low level program pulse applied to an EPROM's $\overline{CE}$ with V_{PP} at 12.75V will program that EPROM. A TTL high level $\overline{CE}$ input inhibits the other EPROM's from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC}, except during programming and program verify.

MANUFACTURER'S IDENTIFICATION CODE

The part has a manufacturer's indentification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table 2, specifically identifies the manufacturer and device type. The code for the NM27C020 is "8F8E," where "8F" designates that it is made by Fairchild Semiconductor, and "8E" designates a 2 Megabit byte-wide part.

The code is accessed by applying 12V ±0.5V to address pin A9. Addresses and control pins are held at V_{IL}, except A0. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O0 –07 . Proper code access is only guaranteed at 25°C ± 5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å – 4000Å range. After programming, opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15W-sec/cm^2. The device should be placed within 1 inch of the lamp tubes during erasure. The device should be placed within 1 inch of the lamp tubes during erasure.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increases as the square of the distance from the lamp. (if distance is doubled the erasure time increases by factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components and even system designs have been erroneously suspected when incomplete erasure was the problem.

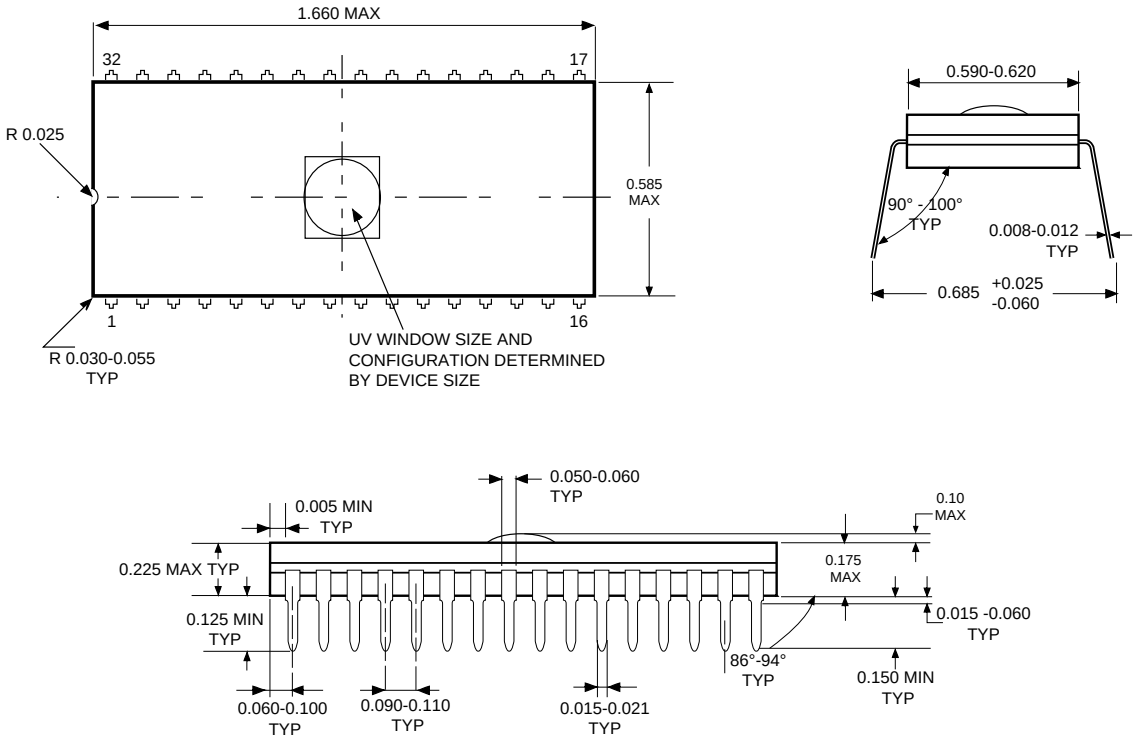
SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE 2. Manufacturer's Identification Code

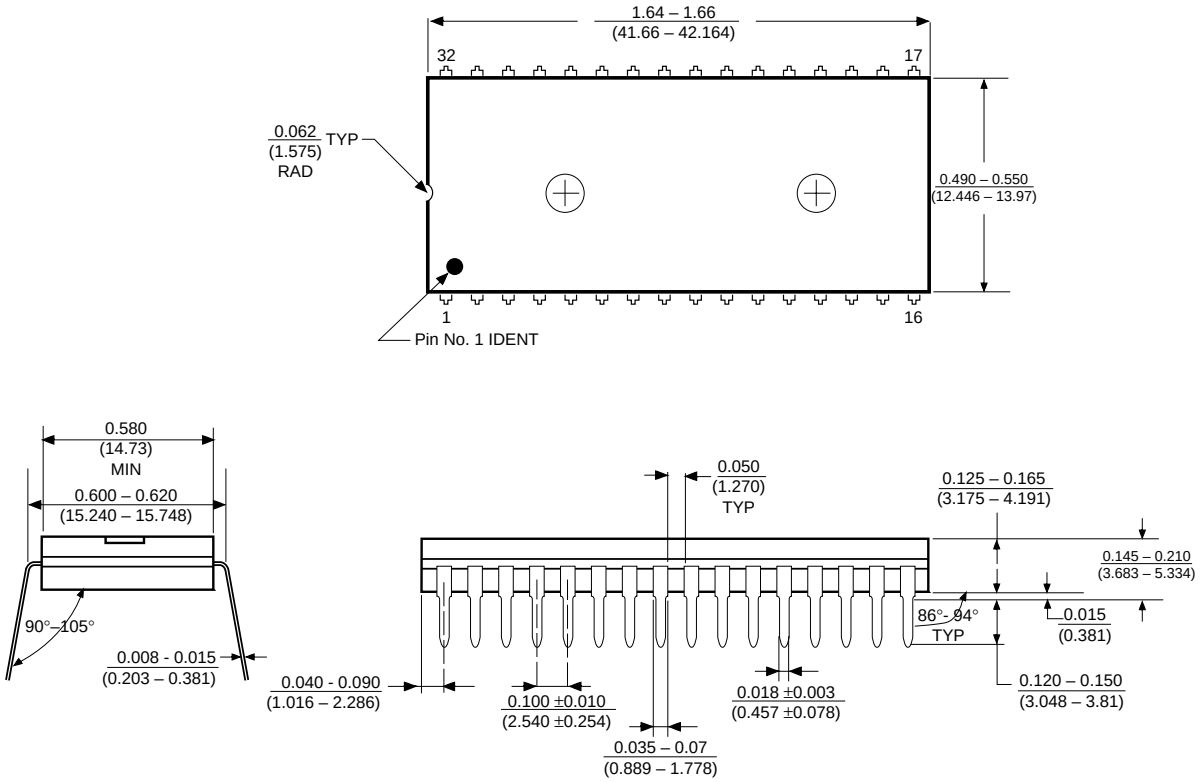
Pins	A0 (12)	A9 (26)	O7 (21)	O6 (19)	O5 (18)	O4 (17)	O3 (16)	O2 (15)	O1 (14)	O0 (13)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	0	0	0	0	0	1	1	1	07

Physical Dimensions inches (millimeters) unless otherwise noted



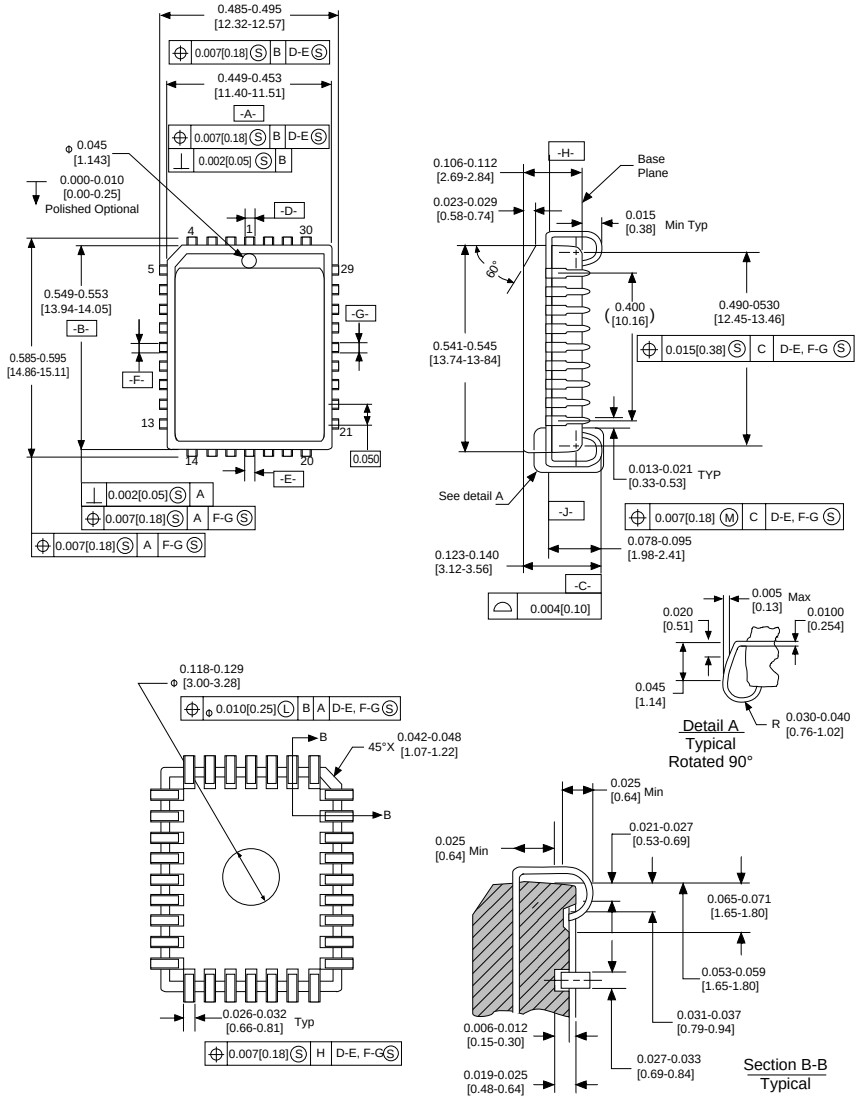
32-Lead EPROM Ceramic Dual-In-Line Package (Q)
Order Number NM27C020Q
Package Number J32AQ

Physical Dimensions inches (millimeters) unless otherwise noted



32-Lead PDIP Package
Order Number NM27C020N

Physical Dimensions inches (millimeters) unless otherwise noted



32-Lead PLCC Package
Order Number NM27C020V
Package Number VA32A

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

February 1999

NM27C040
4,194,304-Bit (512K x 8) High Performance CMOS EPROM

General Description

The NM27C040 is a high performance, 4,194,304-bit Electrically Programmable UV Erasable Read Only Memory. It is organized as 512K words of 8 bits each. Its pin-compatibility with byte-wide JEDEC EPROMs enables upgrades through 8 Mbit EPROMs. The "Don't Care" feature on V_{PP} during read operations allows memory expansions from 1M to 8 Mbits with no printed circuit board changes.

The NM27C040 provides microprocessor-based systems extensive storage capacity for large portions of operating system and application software. Its 120ns access time provides high speed operation with high-performance CPUs. The NM27C040 offers a single chip solution for the code storage requirements of 100% firmware-based equipment. Frequently used software routines are quickly executed from EPROM storage, greatly enhancing system utility.

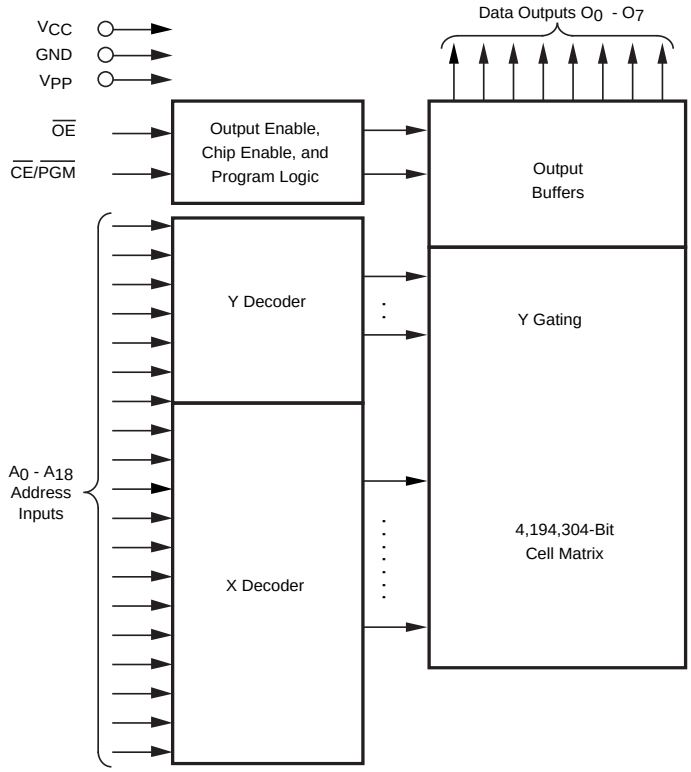
The NM27C040 is manufactured using Fairchild's advanced CMOS AMG™ EPROM technology.

Features

- High performance CMOS
  - —120, 150ns access time*
- Simplified upgrade path
  - —V_{PP} is a "Don't Care" during normal read operation
- Manufacturer's identification code
- JEDEC standard pin configuration
  - —32-pin PDIP
  - —32-pin PLCC
  - —32-pin CERDIP

***Note:** New revision meets 70ns. Please check with factory for availability.

Block Diagram



DS010836-1

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Connection Diagrams

27C080	27C020	27C010				27C010	27C020	27C080
A_{19}	XX/V_{PP}	XX/V_{PP}	XX/V_{PP}	1	32	V_{CC}	V_{CC}	V_{CC}	V_{CC}
A_{16}	A_{16}	A_{16}	A_{16}	2	31	A_{18}	$XX/\overline{PGM}$	$XX/\overline{PGM}$	A_{18}
A_{15}	A_{15}	A_{15}	A_{15}	3	30	A_{17}	NC	A_{17}	A_{17}
A_{12}	A_{12}	A_{12}	A_{12}	4	29	A_{14}	A_{14}	A_{14}	A_{14}
A_7	A_7	A_7	A_7	5	28	A_{13}	A_{13}	A_{13}	A_{13}
A_6	A_6	A_6	A_6	6	27	A_8	A_8	A_8	A_8
A_5	A_5	A_5	A_5	7	26	A_9	A_9	A_9	A_9
A_4	A_4	A_4	A_4	8	25	A_{11}	A_{11}	A_{11}	A_{11}
A_3	A_3	A_3	A_3	9	24	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_2	A_2	A_2	A_2	10	23	A_{10}	A_{10}	A_{10}	A_{10}
A_1	A_1	A_1	A_1	11	22	$\overline{CE}/\overline{PGM}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}/PGM$
A_0	A_0	A_0	A_0	12	21	O_7	O_7	O_7	O_7
O_0	O_0	O_0	O_0	13	20	O_6	O_6	O_6	O_6
O_1	O_1	O_1	O_1	14	19	O_5	O_5	O_5	O_5
O_2	O_2	O_2	O_2	15	18	O_4	O_4	O_4	O_4
GND	GND	GND	GND	16	17	O_3	O_3	O_3	O_3

NM27C040

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Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the NM27C040 pin.

Commercial Temperature Range (0°C to +70°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C040 Q, N, V 120	120
NM27C040 Q, N, V 150	150

Pin Names

A0–A18	Addresses
$\overline{CE}/\overline{PGM}$	Chip Enable/Program
$\overline{OE}$	Output Enable
O0–O7	Outputs
XX	Don't Care (During Read)

Extended Temperature Range (-40°C to +85°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C040 QE, NE, VE 150	150

Package Types: NM27C040 Q, N,V XXX

Q = Quartz-Windowed Ceramic DIP

N = Plastic DIP

V = PLCC

- All packages conform to the JEDEC standard.
- All versions are guaranteed to function for slower speeds.

Absolute Maximum Ratings (Note 1)

Storage Temperature	-65°C to +150°C
All Input Voltages except A9 with Respect to Ground	-0.6V to +7V
V_{PP} and A9 with Respect to Ground	-0.6V to +14V
V_{CC} Supply Voltage with Respect to Ground	-0.6V to +7V
ESD Protection	>2000V
All Output Voltages with Respect to Ground	V_{CC} +1.0V to GND - 0.6V

Operating Range

Range	Temperature	V_{CC}	Tolerance
Commercial	0°C to +70°C	+5V	±10%
Industrial	-40°C to +85°C	+5V	±10%

Read Operation

DC Electrical Characteristics Over operating range with $V_{PP} = V_{CC}$

Symbol	Parameter	Test Conditions		Min	Max	Units
V_{IL}	Input Low Level			-0.5	0.8	V
V_{IH}	Input High Level			2.0	V_{CC} +1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -2.5 mA		3.5		V
I_{SB1}	V_{CC} Standby Current (CMOS)	$\overline{CE} = V_{CC} \pm 0.3V$			100	µA
I_{SB2}	V_{CC} Standby Current	$\overline{CE} = V_{IH}$			1	mA
I_{CC}	V_{CC} Active Current	$\overline{CE} = \overline{OE} = V_{IL}$, I/O = 0 mA	f=5 MHz		30	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$			10	µA
V_{PP}	V_{PP} Read Voltage			V_{CC} - 0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or GND		-1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND		-10	10	µA

AC Electrical Characteristics Over operating range with $V_{PP} = V_{CC}$

Symbol	Parameter	120		150		Units
		Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		120		150	ns
t_{CE}	$\overline{CE}$ to Output Delay		120		150	
t_{OE}	$\overline{OE}$ to Output Delay		50		50	
t_{DF} (Note 2)	Output Disable to Output Float		45		55	
t_{OH} (Note 2)	Output Hold from Addresses $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		

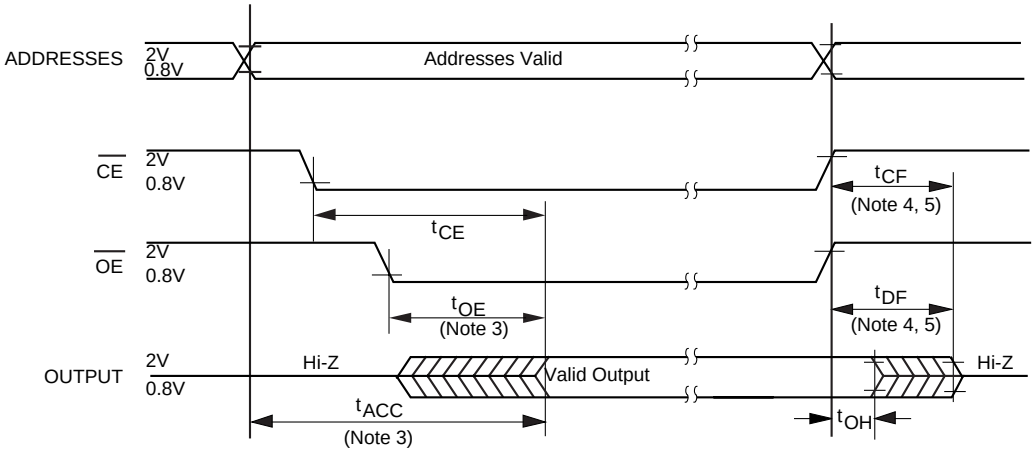
Capacitance T_A = +25°C, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	9	15	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	15	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level (Note 10)	
Inputs	0.8V and 2V
Outputs`	0.8V and 2V

AC Waveforms (Notes 6, 7, 9)



DS010836-4

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE®, the measured V_{OH1} (DC) - 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND.

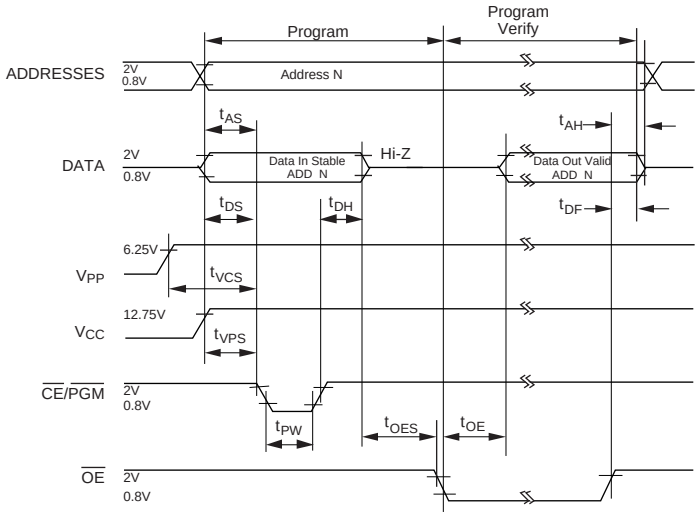
Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: I_{OL} = 1.6 mA, I_{OH} = -400 µA.
C_L: 100 pF includes fixture capacitance.

Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to -2.0V for 20 ns Max.

Programming Waveform (Note 13)



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Programming Characteristics (Notes 11, 12, 13, 14)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			µs
t_{OES}	$\overline{OE}$ Setup Time		1			µs
t_{DS}	Data Setup Time		1			µs
t_{VPS}	V_{PP} Setup Time		1			µs
t_{VCS}	V_{CC} Setup Time		1			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		1			µs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE}/\overline{PGM}$ = X	0		60	ns
t_{PW}	Program Pulse Width		45	50	105	µs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE}/\overline{PGM}$ = X			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE}/\overline{PGM}$ = V_{IL}			30	mA
I_{CC}	V_{CC} Supply Current				30	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.25	6.5	6.75	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage		-0.1	0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

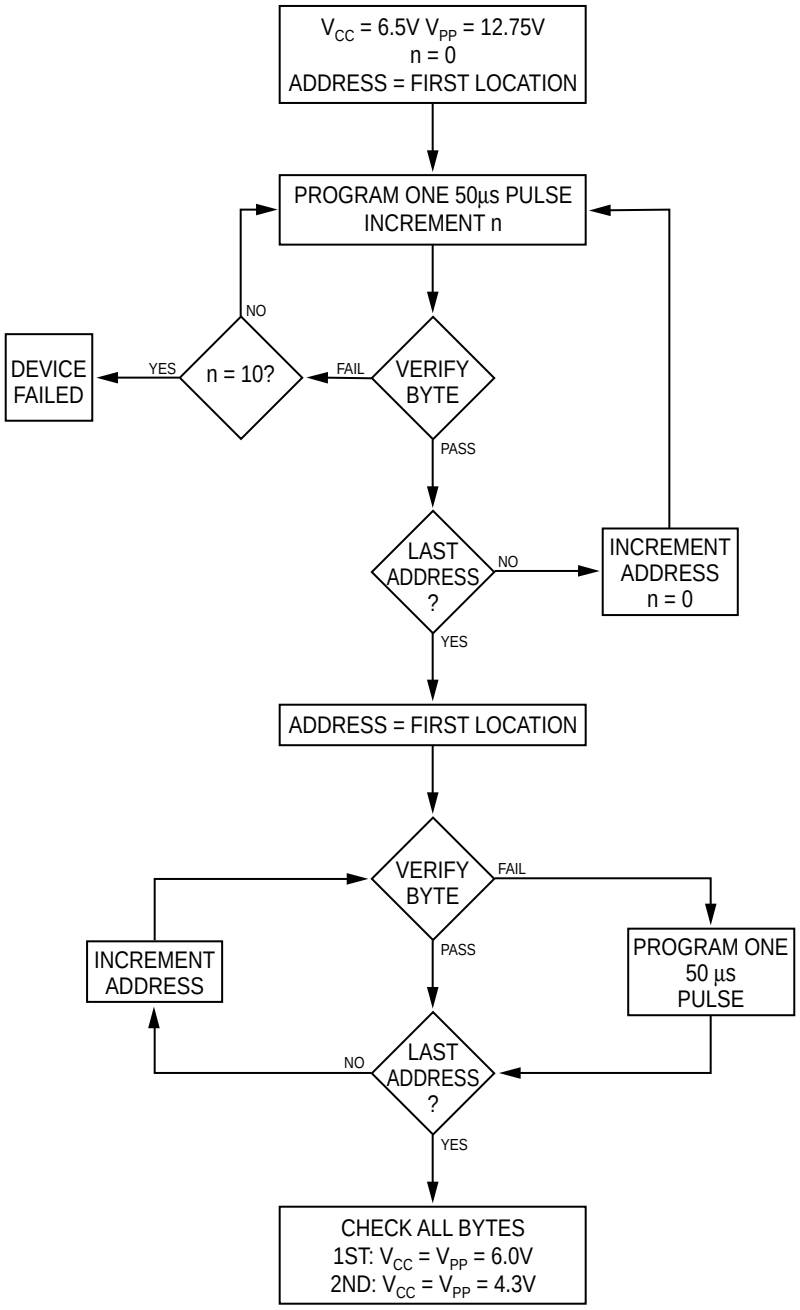
Note 11: Fairchild's standard product warranty applies only to devices programmed to specifications described herein.

Note 12: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 13: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 µF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 14: During power up the $\overline{CE}/\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

Turbo Programming Algorithm Flow Chart



DS010836-6

Note: The standard National Semiconductor algorithm may also be used with it will have longer programming time.

FIGURE 1.

Functional Description

DEVICE OPERATION

The six modes of operation of the EPROM are listed in Table 1. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$/PGM) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t$\overline{OE}$ after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$/$\overline{PGM}$ has been low and addresses have been stable for at least t_{ACC} -t_{OE}.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from of 65 mW to 0.55 mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$/PGM input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the $\overline{OE}$ input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Typing

Because the EPROM is usually used in larger memory arrays, Fairchild has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

1. the lowest possible memory power dissipation, and
2. complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$/$\overline{PGM}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 µF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{CE}$/$\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the Turbo Programming Algorithm shown in Figure 1. Each Address is programmed with a series of 50 µs pulses until it verifies good, up to a maximum of 10 pulses. Most memory cells will program with a single 50 µs pulse. (The standard National Semiconductor Algorithm may also be used but it will have longer programming time.)

The EPROM must not be programmed with a DC signal applied to the $\overline{CE}$/$\overline{PGM}$ input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the pro-gramming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$/$\overline{PGM}$ input programs the paralleled EPROM.

Program Inhibit

Programming multiple EPROMs in parallel with different data is also easily accomplished. Except for $\overline{CE}$/$\overline{PGM}$ all like in-puts (including $\overline{OE}$) of the parallel EPROMs may be com-mon. A TTL low level program pulse applied to an EPROM's $\overline{CE}$/$\overline{PGM}$ input with V_{PP} at 12.75V will program that EPROM. A TTL high level $\overline{CE}$/$\overline{PGM}$ input inhibits the other EPROMs from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC}, except during programming and program verify.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table 2, specifically identifies the manufacturer and device type. The code for NM27C040 is "8F08", where "8F" designates that it is made by Fairchild Semiconductor, and "08" designates a 4 Megabit (512K x 8) part.

The code is accessed by applying 12V ±0.5V to address pin A9. Addresses A1–A8, A10–A18, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O0 –O7 . Proper code access is only guaranteed at 25°C ± 5°C.

Functional Description (Continued)

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity X exposure time) for erasure should be minimum of 15W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increase as the square of the distance from the lamp. (If distance is doubled the erasure time increases by factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent of the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

Mode Selection

The modes of operation of the NM27C040 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 for device signature.

TABLE 1. Modes Selection

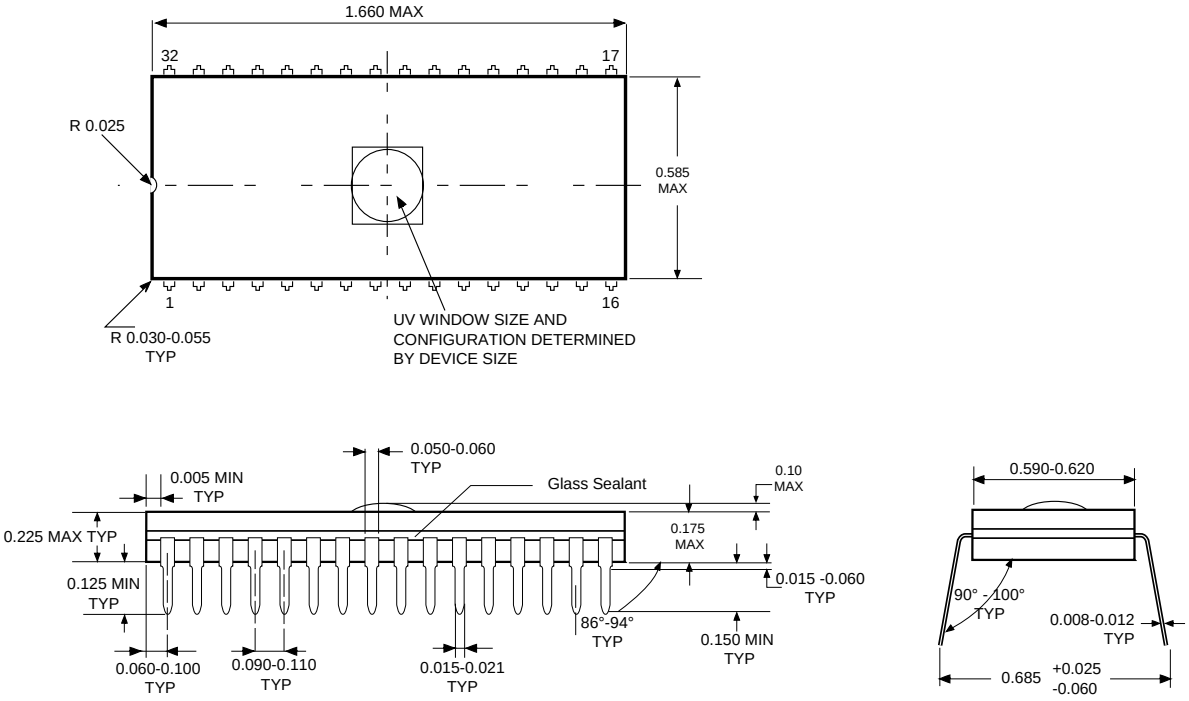
Mode \ Pins	$\overline{CE}/\overline{PGM}$	$\overline{OE}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X (Note 15)	5.0V	D_{OUT}
Output Disable	X	V_{IH}	X	5.0V	High Z
Standby	V_{IH}	X	X	5.0V	High Z
Programming	V_{IL}	V_{IH}	12.75V	6.25V	D_{IN}
Program Verify	X	V_{IL}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	12.75V	6.25V	High Z

Note 15: X can be V_{IL} or V_{IH}

TABLE 2. Manufacturer's Identification Code

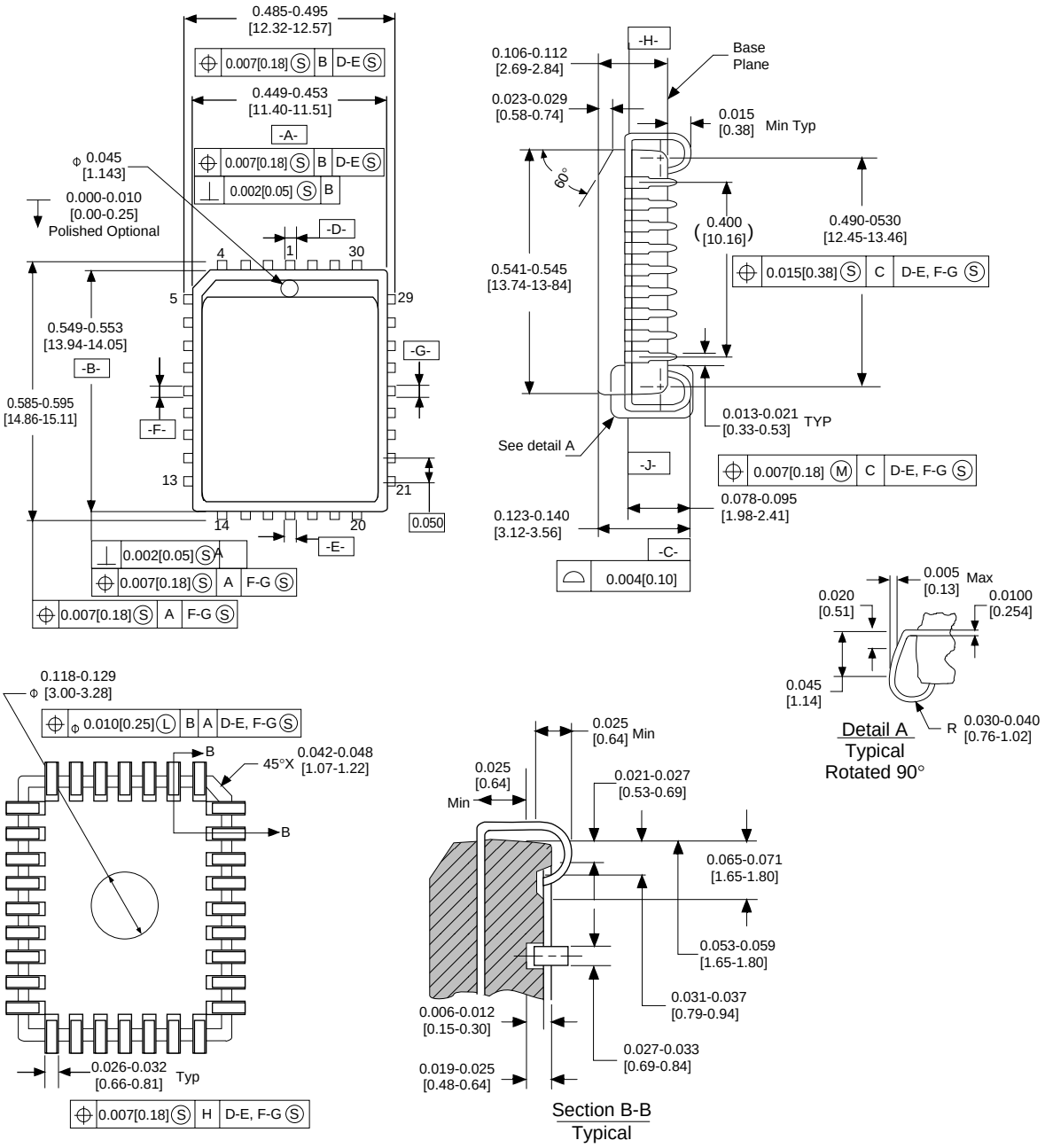
Pins	A0 (12)	A9 (26)	O7 (21)	O6 (20)	O5 (19)	O4 (18)	O3 (17)	O2 (15)	O1 (14)	O0 (13)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	0	0	0	0	1	0	0	0	08

Physical Dimensions inches (millimeters) unless otherwise noted



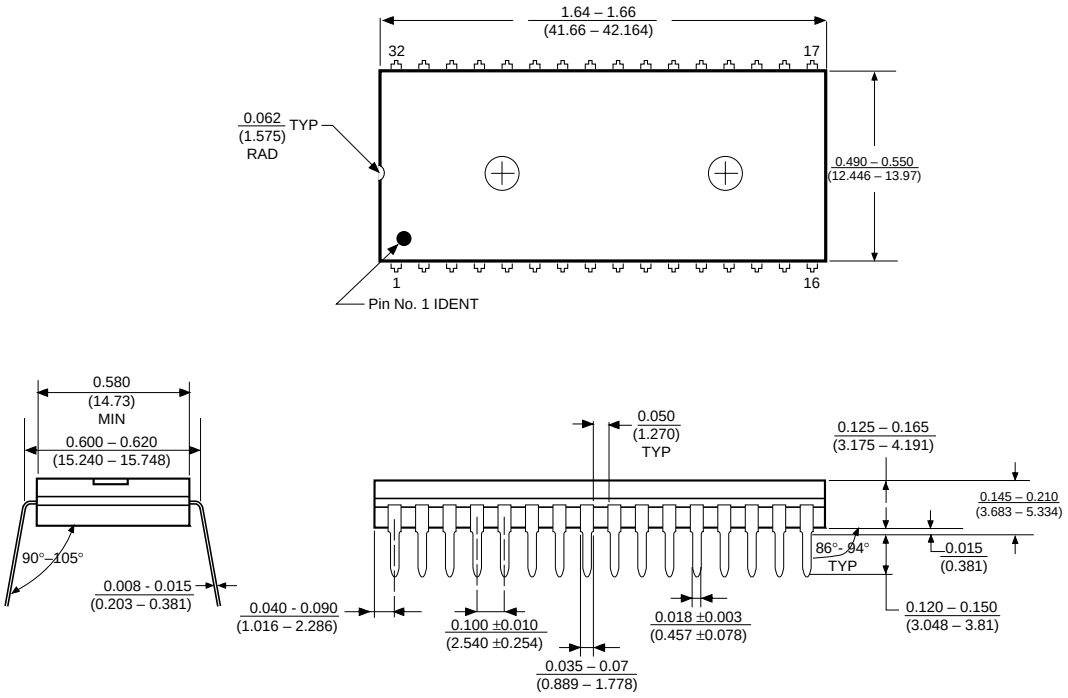
32-Lead EPROM Ceramic Dual-In-Line Package (Q)
Order Number NM27C040QXXX
Package Number J32AQ

Physical Dimensions inches (millimeters) unless otherwise noted



32-Lead PLCC Package (V)
Order Number NM27C040VXXX
Package Number VA32A

Physical Dimensions inches (millimeters) unless otherwise noted



32-Lead PDIP Package
Order Number NM27C040NXXX

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

July 1998

NM27C128
131,072-Bit (16K x 8) High Performance CMOS EPROM

General Description

The NM27C128 is a high performance 128K UV Erasable Electrically Programmable Read Only Memory. It is manufactured with Fairchild's latest CMOS split gate EPROM technology which enables it to operate at speeds as fast as 90 ns access time over the full operating range.

The NM27C128 provides microprocessor-based systems extensive storage capacity for large portions of operating system and application software. Its 90 ns access time provides high speed operation with high-performance CPUs. The NM27C128 offers a single chip solution for the code storage requirements of 100% firmware-based equipment. Frequently-used software routines are quickly executed from EPROM storage, greatly enhancing system utility.

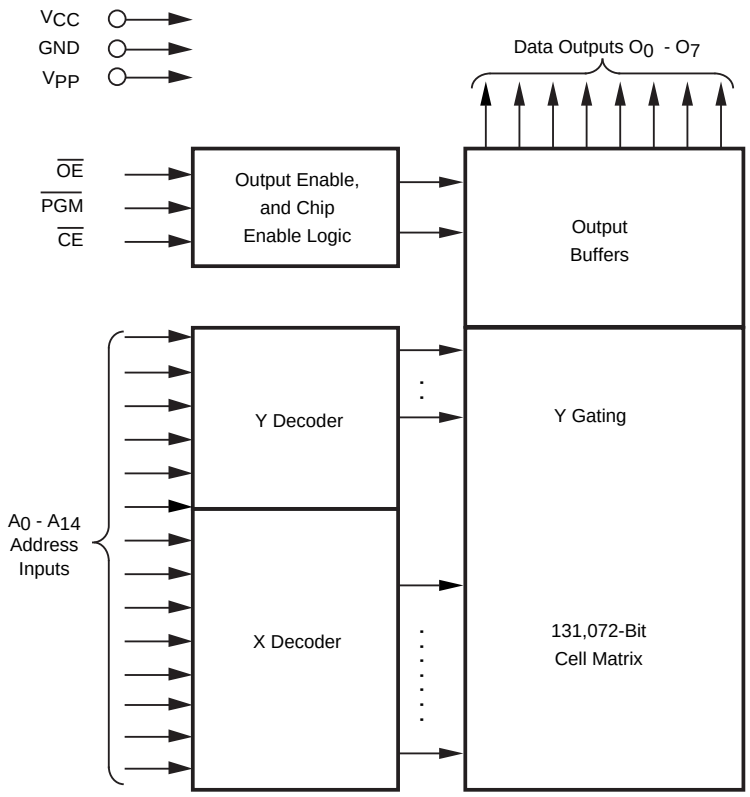
The NM27C128 is configured in the standard EPROM pinout which provides an easy upgrade path for systems which are currently using standard EPROMs.

The NM27C128 is one member of a high density EPROM Family which range in densities up to 4 Mb.

Features

- High performance CMOS
  - —90 ns access time
- Fast turn-off for microprocessor compatibility
- JEDEC standard pin configuration
  - —28-pin PDIP package
  - —32-pin chip carrier
  - —28-pin CERDIP package
- Drop-in replacement for 27C128 or 27128
- 40% faster programming time with Fairchild's turbo algorithm

Block Diagram



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Connection Diagrams

27C080	27C040	27C020	27C010	27C512	27C256
A19	V_{PP}	V_{PP}	V_{PP}		
A16	A16	A16	A16		
A15	A15	A15	A15	A15	V_{PP}
A12	A12	A12	A12	A12	A12
A7	A7	A7	A7	A7	A7
A6	A6	A6	A6	A6	A6
A5	A5	A5	A5	A5	A5
A4	A4	A4	A4	A4	A4
A3	A3	A3	A3	A3	A3
A2	A2	A2	A2	A2	A2
A1	A1	A1	A1	A1	A1
A0	A0	A0	A0	A0	A0
O0	O0	O0	O0	O0	O0
O1	O1	O1	O1	O1	O1
O2	O2	O2	O2	O2	O2
GND	GND	GND	GND	GND	GND

DIP
NM27C128

V_{PP}	1	28	V_{CC}
A12	2	27	$\overline{PGM}$
A7	3	26	A13
A6	4	25	A8
A5	5	24	A9
A4	6	23	$\overline{A11}$
A3	7	22	$\overline{OE}$
A2	8	21	A10
A1	9	20	$\overline{CE}$
A0	10	19	O7
O0	11	18	O6
O1	12	17	O5
O2	13	16	O4
GND	14	15	O3

27C256	27C512	27C010	27C020	27C040	27C080
		V_{CC}	V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	$\overline{PGM}$	A18	A18
V_{CC}	V_{CC}	XX	XX	A17	A17
A14	A14	A14	A14	A14	A14
A13	A13	A13	A13	A13	A13
A8	A8	A8	A8	A8	A8
A9	A9	A9	A9	A9	A9
A11	A11	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A10	A10	A10	A10	A10	A10
$\overline{CE}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}/\overline{PGM}$
O7	O7	O7	O7	O7	O7
O6	O6	O6	O6	O6	O6
O5	O5	O5	O5	O5	O5
O4	O4	O4	O4	O4	O4
O3	O3	O3	O3	O3	O3

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Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the NM27C128 pins.

Commercial Temp. Range (0°C to +70°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C128 Q, N, V 90	90
NM27C128 Q, N, V 120	120
NM27C128 Q, N, V 150	150
NM27C128 Q, N, V 200	200

Pin Names

Symbol	Description
A0–A13	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O7	Outputs
$\overline{PGM}$	Program
NC	No Connect

Extended Temp. Range (-40°C to +85°C) V_{cc} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C128 QE, NE, VE 120	120
NM27C128 QE, NE, VE 150	150
NM27C128 QE, NE, VE 200	200

Note: Surface mount PLCC package available for commercial and extended temperature ranges only.

Package Types: NM27C128 Q, N, V XXX

Q = Quartz-Windowed Ceramic DIP

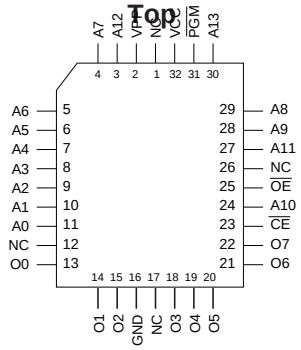
N = Plastic OTP DIP

V = Surface-Mount PLCC

- All packages conform to the JEDEC standard.
- All versions are guaranteed to function for slower speeds.

PLCC

Top



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Absolute Maximum Ratings (Note 1)

Storage Temperature	-65°C to +150°C
All Input Voltages except A9 with Respect to Ground	-0.6V to +7V
V_{PP} and A9 with Respect to Ground	-0.7V to +14V
V_{CC} Supply Voltage with Respect to Ground	-0.6V to +7V
ESD Protection	> 2000V
All Output Voltages with Respect to Ground	V_{CC} + 1.0V to GND -0.6V

Operating Range

Range	Temperature	V_{CC}
Comm'l	0°C to +70°C	+5V ±10%
Industrial	-40°C to +85°C	+5V ±10%

Read Operation

DC Electrical Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IL}	Input Low Level		-0.5	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} +1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -2.5 mA	3.5		V
I_{SB1}	V_{CC} Standby Current (CMOS)	$\overline{CE} = V_{CC} \pm 0.3V$ V_{IL} = GND ± 0.3V, $V_{IH} = V_{CC} \pm 0.3V$		100	µA
I_{SB2}	V_{CC} Standby Current (T^2L)	$\overline{CE} = V_{IH}$		1	mA
I_{CC1}	V_{CC} Active Current, T^2L Inputs	$\overline{CE} = \overline{OE} = V_{IL}$, f = 5 MHz I/O = 0 mA		35	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$		10	µA
V_{PP}	V_{PP} Read Voltage		GND	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or GND	-1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND	-10	10	µA

AC Electrical Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	90		120		150		200		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		90		120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay		90		120		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay		50		50		50		50	ns
t_{CF} (Note 2)	$\overline{CE}$ High to Output Float		30		30		45		55	ns
t_{DF} (Note 2)	$\overline{OE}$ High to Output Float		35		35		45		55	ns
t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		0		ns

Capacitance T_A = +25°C, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	6	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	9	12	pF

AC Test Conditions

Output Load 1 TTL Gate and C_L = 100 pF (Note 8)

Input Rise and Fall Times ≤ 5 ns

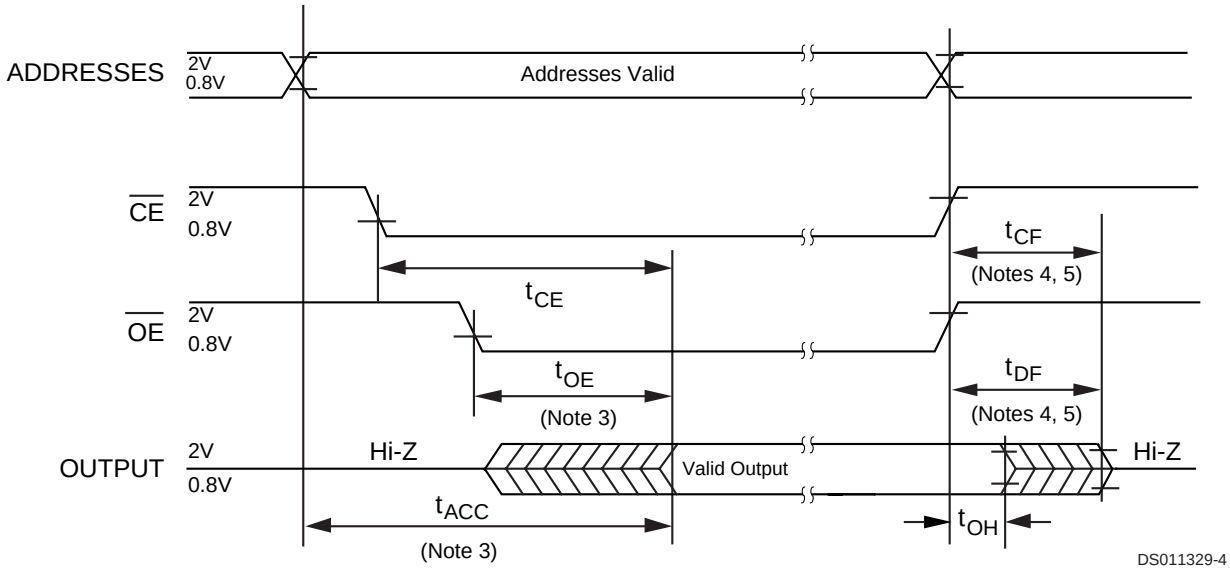
Input Pulse Levels 0.45 to 2.4V

Timing Measurement Reference Level (Note 10)

Inputs 0.8V and 2.0V

Outputs 0.8V and 2.0V

AC Waveforms (Notes 6, 7, 9)



Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: OE may be delayed up to t_{ACC} - t_{OE} after the falling edge of CE without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE®, the measured V_{OH1} (DC) - 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: TTL Gate: I_{OL} = 1.6 mA, I_{OH} = -400 µA.
C_L = 100 pF includes fixture capacitance.

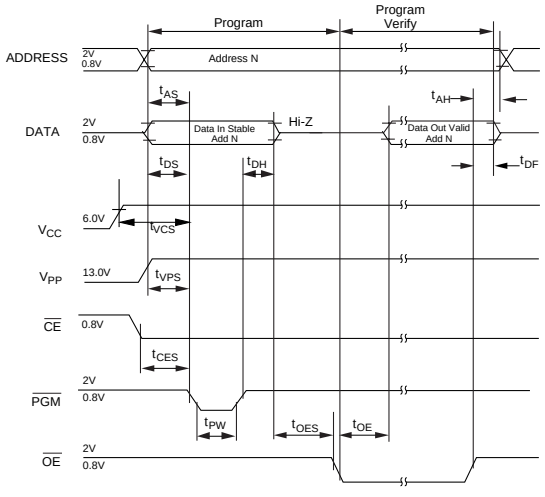
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to -2.0V for 20 ns Max.

Programming Characteristics (Notes 11, 12, 13, 14)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			µs
t_{OES}	$\overline{OE}$ Setup Time		1			µs
t_{CES}	$\overline{CE}$ Setup Time	$\overline{OE} = V_{IH}$	1			µs
t_{VPS}	V_{PP} Setup Time		1			µs
t_{VCS}	V_{CC} Setup Time		1			µs
t_{DS}	Data Setup Time		1			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		1			µs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		45	50	105	µs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				50	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.25	6.5	6.75	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

Programming Waveforms (Note 13)



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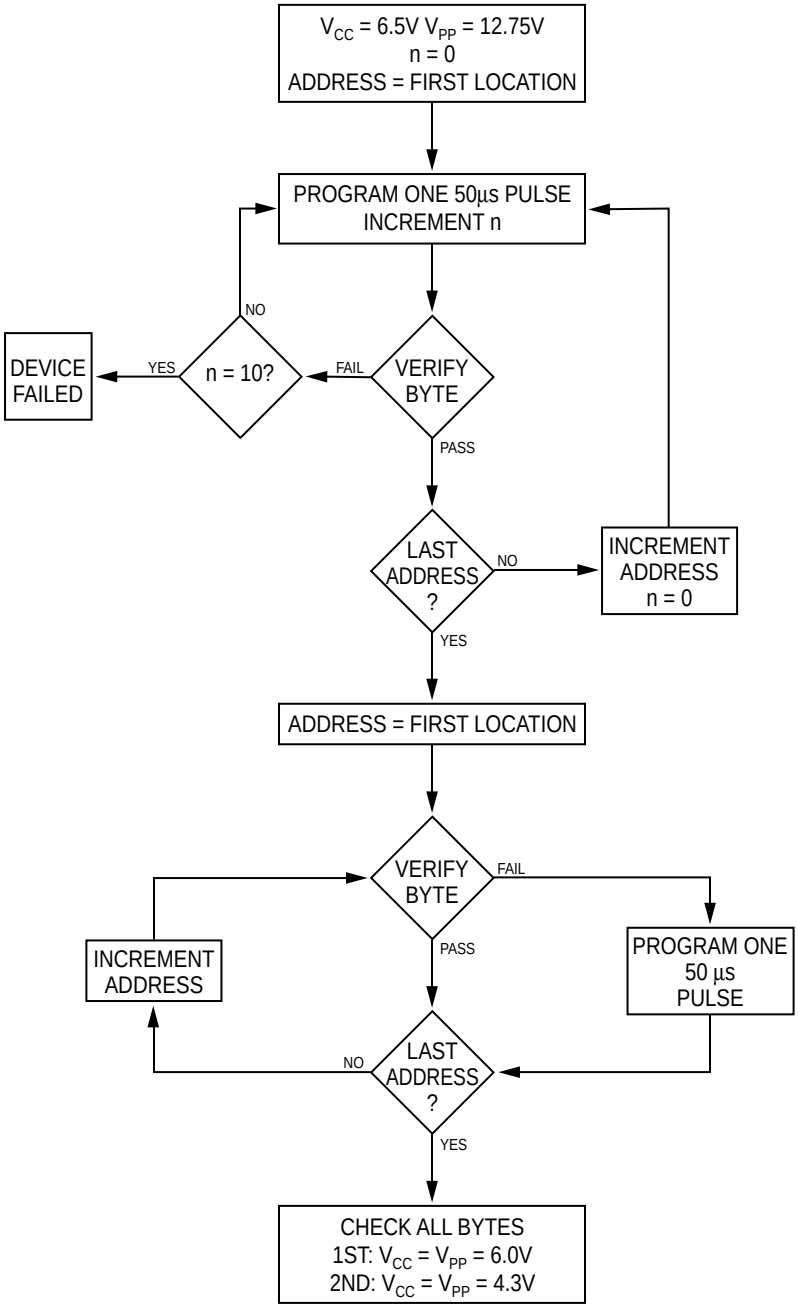
Note 11: Fairchild's standard product warranty applies to devices programmed to specifications described herein.

Note 12: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 13: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 µF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 14: During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

Turbo Programming Algorithm Flow Chart



Note: The standard National Semiconductor algorithm may also be used but it will have longer programming time.

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FIGURE 1.

Functional Description

DEVICE OPERATION

The six modes of operation of the EPROM are listed in Table 1. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.5V during the three programming modes, and at 5V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from 220 mW to 0.55 mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the $\overline{OE}$ input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Typing

Because the EPROM is usually used in larger memory arrays, Fairchild has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

1. the lowest possible memory power dissipation, and
2. complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the V_{PP} power supply is at 12.75V, $\overline{CE}$ is at V_{IL}, and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 µF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the Turbo Programming Algorithm shown in Figure 1. Each Address is programmed with a series of 50 µs pulses until it verifies good, up to a maximum of 10 pulses. Most memory cells will program with a single 50 µs pulse. (The standard National Semiconductor algorithm may also be used but it will have longer programming time.)

The EPROM must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirments. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the PGM input programs the paralleled EPROM.

Program Inhibit

Programming multiple EPROMs in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$) of the parallel EPROMs may be common. A TTL low level program pulse applied to an EPROM's $\overline{CE}$ input with V_{PP} at 12.75V will program that EPROM. A TTL high level $\overline{CE}$ input inhibits the other EPROMs from being programmed.

Functional Description (Continued)

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC}, except during programming and program verify.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table 2, specifically identifies the manufacture and device type. The code for NM27C128 is "8F83", where "8F" designates that it is made by Fairchild Semiconductor, and "83" designates a 128K part.

The code is accessed by applying 12V ±0.5V to address pin A9. Addresses A1–A8, A10–A13, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O0 –O7 . Proper code access is only guaranteed at 25°C to ±5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å – 4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table 1 shows the minimum EPROM erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increases as the square of the distance from the lamp (if distance is doubled the erasure time increases by factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent of the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

Mode Selection

The modes of operation of NM27C128 listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 for device signature.

TABLE 1. Modes Selection

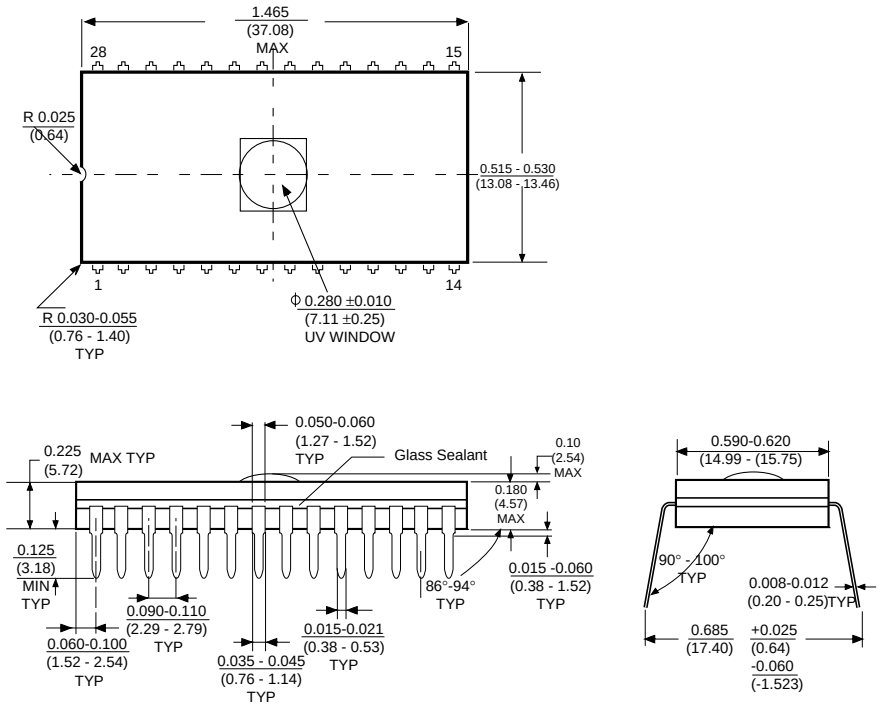
Mode \ Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	5.0V	D_{OUT}
Output Disable	X	V_{IH}	V_{IH}	V_{CC}	5.0V	High-Z
Standby	V_{IH}	X	X	V_{CC}	5.0V	High-Z
Programming	V_{IL}	V_{IH}	V_{IL}	12.75V	6.5V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	12.75V	6.5V	D_{OUT}
Program Inhibit	V_{IH}	X	X	12.75V	6.5V	High-Z

Note 15: X can be V_{IL} or V_{IH}.

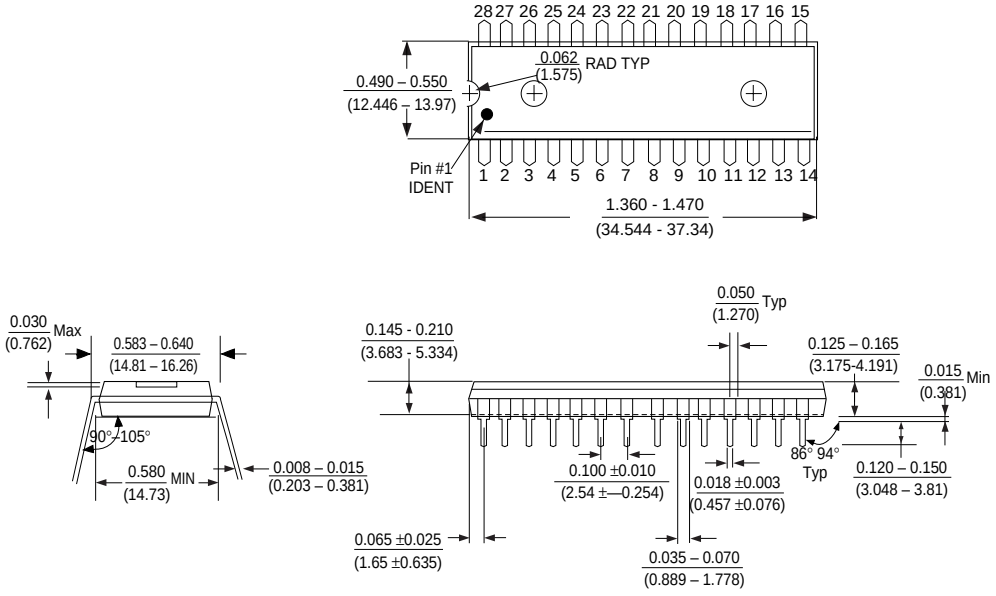
TABLE 2. Manufacturer's Identification Code

Pins	A0 (10)	A9 (24)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	1	0	0	0	0	0	1	1	83

Physical Dimensions inches (millimeters) unless otherwise noted

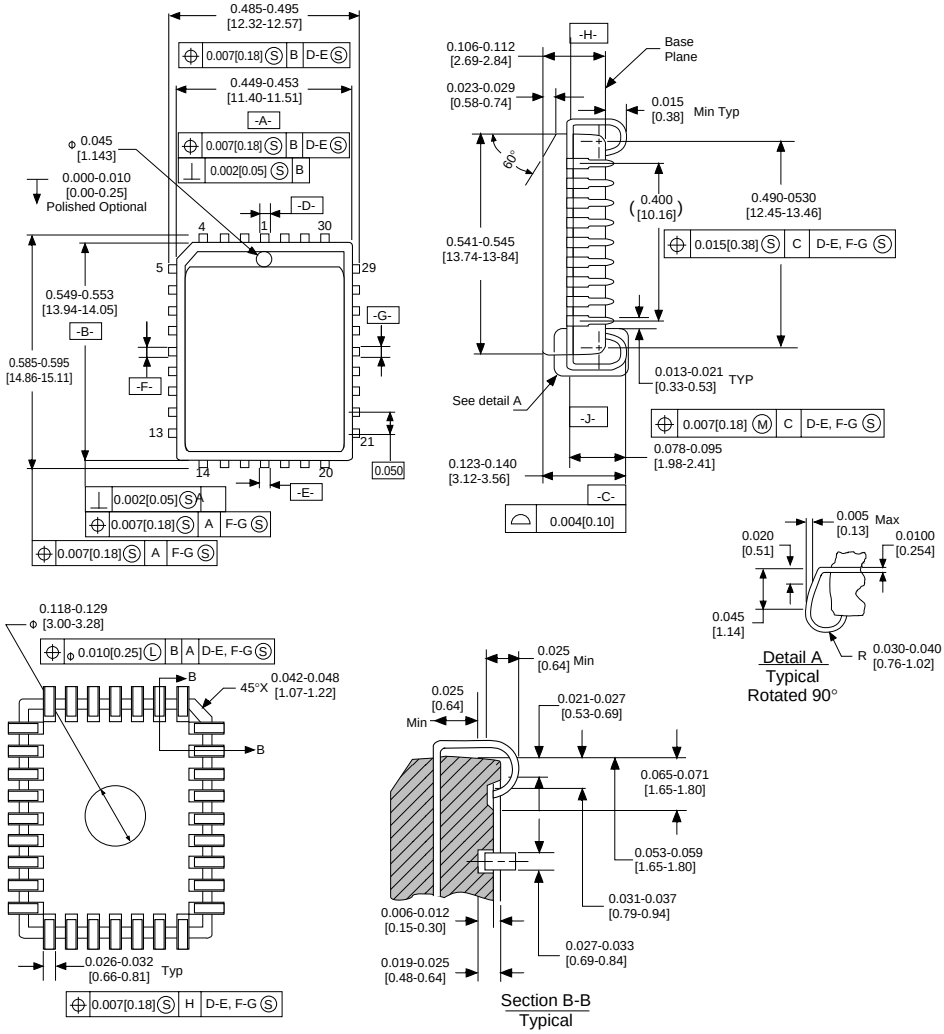


UV Window Cavity Dual-In-Line CerDIP Package (JQ)
Order Number NM27C128QXXX
Package Number J28CQ (C)



28-Lead Plastic One-Time-Programmable Dual-In-Line Package
Order Number NM27C128NXXX
Package Number N28B

Physical Dimensions inches (millimeters) unless otherwise noted



32-Lead Plastic Leaded Chip Carrier (PLCC)
Order Number NM27C128VXXX
Package Number VA32A

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

July 1998

NM27C210
1,048,576-Bit (64K x 16) High Performance CMOS EPROM

General Description

The NM27C210 is a high performance Electrically Programmable UV erasable ROM (EPROM). It contains 1,048,576 bits configured as 64K x 16 bit. It is offered in both erasable versions for prototyping and early production applications as well as non-erasable, plastic packaged versions that are ideal for high volume and automated assembly applications.

The NM27C210 operates from a single 5 volt ±10% supply in the read mode.

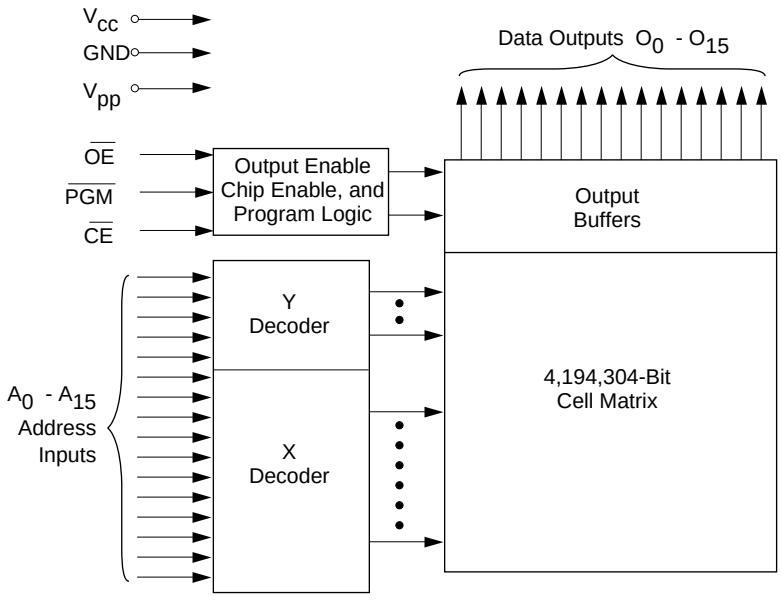
The NM27C210 is offered in both DIP and surface mount packages. The DIP package is a 40-pin dual-in-line ceramic with a quartz window to allow erasing. The surface mount package is a 44-pin PLCC that is offered in OTP.

This EPROM is manufactured using Fairchild's proprietary AMG™ EPROM technology for an excellent combination of speed and economy while providing excellent reliability.

Features

- High performance CMOS
  - —90 ns access time
- Fast turn-off for microprocessor compatibility
- Simplified upgrade path
  - —V_{PP} and $\overline{PGM}$ are "Don't Care" during normal read operation
- Compatible with 27210 and 27C210 EPROMs
- Manufacturer's identification code
- Fast programming
- JEDEC standard pin configuration
  - —40-pin CDIP package
  - —40-pin PDIP package
  - —44-pin PLCC package

Block Diagram



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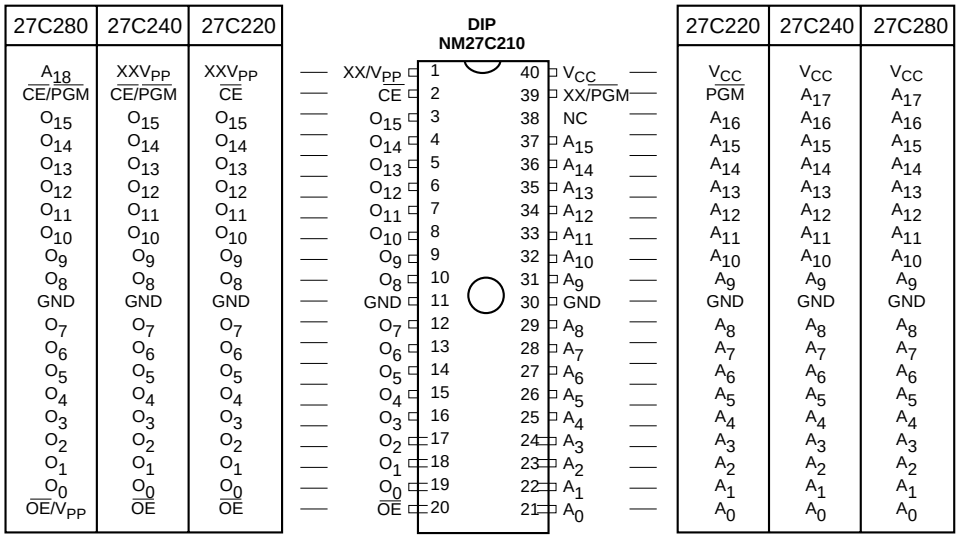
AMG™ is a trademark of WSI, Inc.

Connection Diagrams

DIP PIN CONFIGURATIONS



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Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the NM27C210 pins.

Commercial Temperature Range (0°C to +70°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C210 Q, V, N 90	90
NM27C210 Q, V, N 120	120
NM27C210 Q, V, N 150	150

Industrial Temperature Range (-40°C to +85°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C210 QE, VE, NE 120	120
NM27C210 QE, VE, NE 150	150

Package Types: NM27C210 Q, V, N XXX

Q = Quartz-Windowed Ceramic DIP package

N = Plastic DIP package

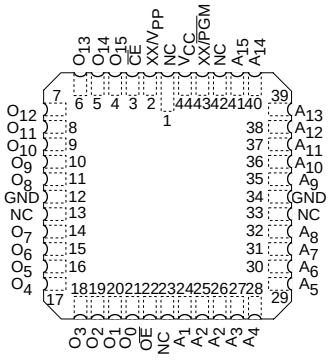
V = PLCC package

- All packages conform to JEDEC standard.
- All versions are guaranteed to function in slower applications.

Pin Names

A0–A15	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O15	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)
NC	No Connect

PLCC Pin Configuration



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Top View

Absolute Maximum Ratings (Note 1)

Storage Temperature	-65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	-0.6V to +7V
V_{PP} and A9 with Respect to Ground	-0.6V to +14V
V_{CC} Supply Voltage with Respect to Ground	-0.6V to +7V
ESD Protection	>2000V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} + 1.0V to GND - 0.6V

Operating Range

Range	Temperature	V_{CC}	Tolerance
Commercial	0°C to +70°C	+5V	±10%
Industrial	-40°C to +85°C	+5V	±10%

DC Read Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	Test Conditions		Min	Max	Units
V_{IL}	Input Low Level			-0.5	0.8	V
V_{IH}	Input High Level			2.0	V_{CC} +1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -2.5 mA		3.5		V
I_{SB1}	V_{CC} Standby Current (CMOS)	$\overline{CE} = V_{CC} \pm 0.3V$			100	µA
I_{SB2}	V_{CC} Standby Current	$\overline{CE} = V_{IH}$			1	mA
I_{CC}	V_{CC} Active Current	$\overline{CE} = \overline{OE} = V_{IL}$, I/O = 0 mA	f = 5 MHz		40	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$			10	µA
I_{LI}	Input Load Current	V_{IN} = 5.5 or GND		-1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND		-10	10	µA

AC Read Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	90		120		150		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		90		120		150	ns
t_{CE}	$\overline{CE}$ to Output Delay		90		120		150	
t_{OE}	$\overline{OE}$ to Output Delay		50		50		50	
t_{DF} (Note 2)	Output Disable to Output Float		30		35		45	
t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		

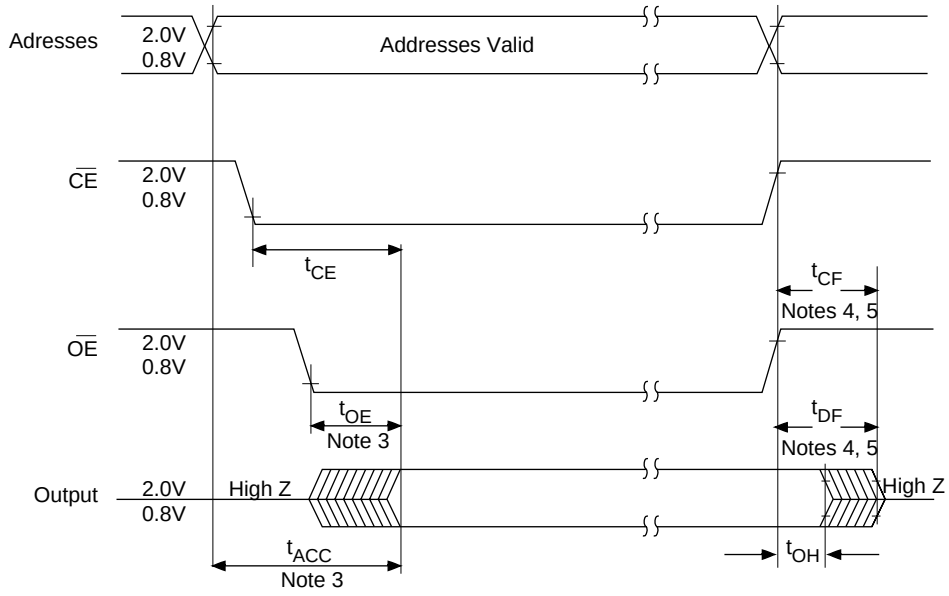
Capacitance (Note 2) T_A = +25°C, f = 1 MHz

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	12	20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	13	20	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Note 6) , (Note 7) , (Note 9)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE®, the measured V_{OH1} (DC) - 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: I_{OL} = 1.6 mA, I_{OH} = -400 µA.
C_L: 100 pF includes fixture capacitance.

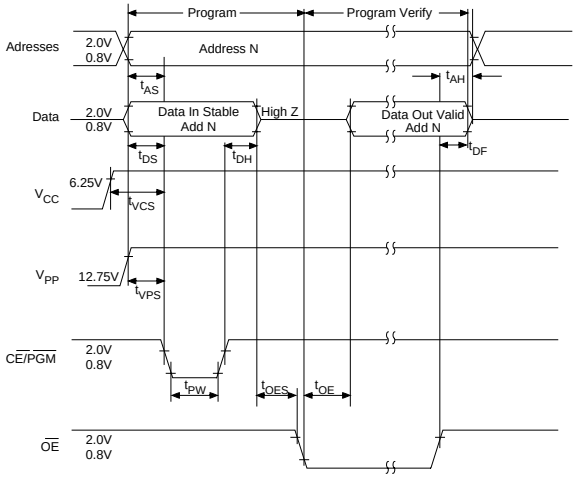
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to -2.0V for 20 ns Max.

Programming Characteristics (Note 11), (Note 12), (Note 13), (Note 14), and (Note 15)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			µs
t_{OES}	$\overline{OE}$ Setup Time		1			µs
t_{CES}	$\overline{CE}$ Setup Time	$\overline{OE} = V_{IH}$	1			µs
t_{DS}	Data Setup Time		1			µs
t_{VPS}	V_{PP} Setup Time		1			µs
t_{VCS}	V_{CC} Setup Time		1			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		1			µs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		45	50	105	µs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IL}$			40	mA
I_{CC}	V_{CC} Supply Current				50	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.25	6.5	6.75	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

Programming Waveforms (Note 13)



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Note 11: Fairchild's standard product warranty applies only to devices programmed to specifications described herein.

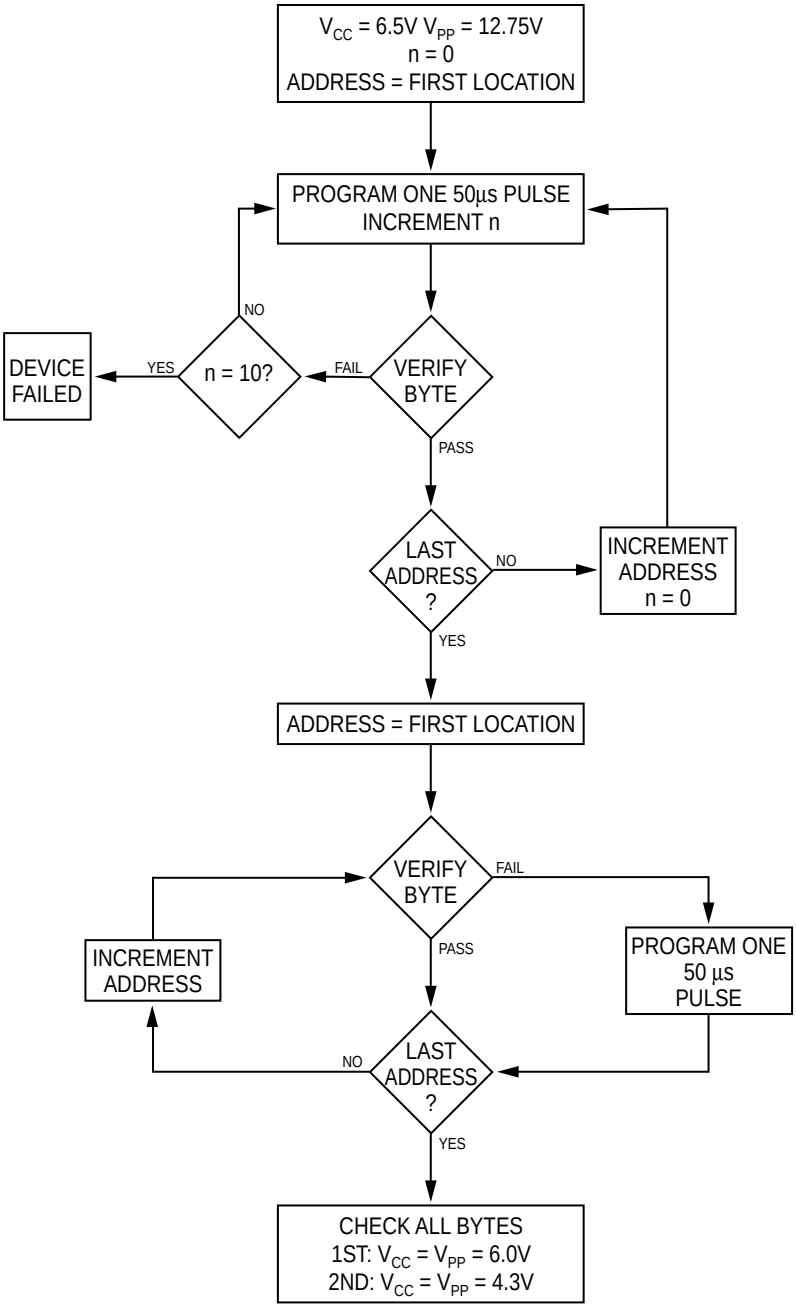
Note 12: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 13: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 µF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 14: Programming and program verify are tested with the turbo Program Algorithm, at typical power supply voltages and timings.

Note 15: During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

Turbo Programming Algorithm Flow Chart



DS011093-6

Note: The standard National Semiconductor algorithm may also be used but it will have longer programming time.

FIGURE 1.

Functional Description

DEVICE OPERATION

The six modes of operation of the EPROM are listed in Table 1. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.5V during the three programming modes, and at 5V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from 200 mW to 0.5 mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the $\overline{OE}$ input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Tying

Because the EPROM is usually used in larger memory arrays, Fairchild has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

1. the lowest possible memory power dissipation, and
2. complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on the V_{PP} or A9 pin will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 µF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 16 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the Turbo Programming Algorithm shown in Figure 1. Each Address is programmed with a series of 50 µs pulses until it verifies good, up to a maximum of 10 pulses. Most memory cells will program with a single 50 µs pulse. (The standard National Semiconductor Algorithm may also be used but it will have longer programming time).

The EPROM must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled EPROM.

Program Inhibit

Programming multiple EPROM's in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel EPROM may be common. A TTL low level program pulse applied to an EPROM's $\overline{PGM}$ input with $\overline{CE}$ at V_{IL} and V_{PP} at 12.75V will program that EPROM. A TTL high level $\overline{CE}$ input inhibits the other EPROM's from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC}, except during programming and program verify.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table 2, specifically identifies the manufacturer and device type. The code for the NM27C210 is "8FD6", where "8F" designates that it is made by Fairchild Semiconductor, and "D6" designates a 1 Megabit (64K x 16) part.

The code is accessed by applying 12V ±0.5V to address pin A9 . Addresses A1 –A8, A10 –A 15 , and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held

Functional Description (Continued)

at V_{IH} for the device code. The code is read on the lower eight data pins, O0 –07 . Proper code access is only guaranteed at 25°C ± 5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å – 4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increases as the square of the distance from the lamp (if distance is doubled the erasure time increases by factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

MODE SELECTION

The modes of operation of the NM27C210 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 for device signature.

TABLE 1. Modes Selection

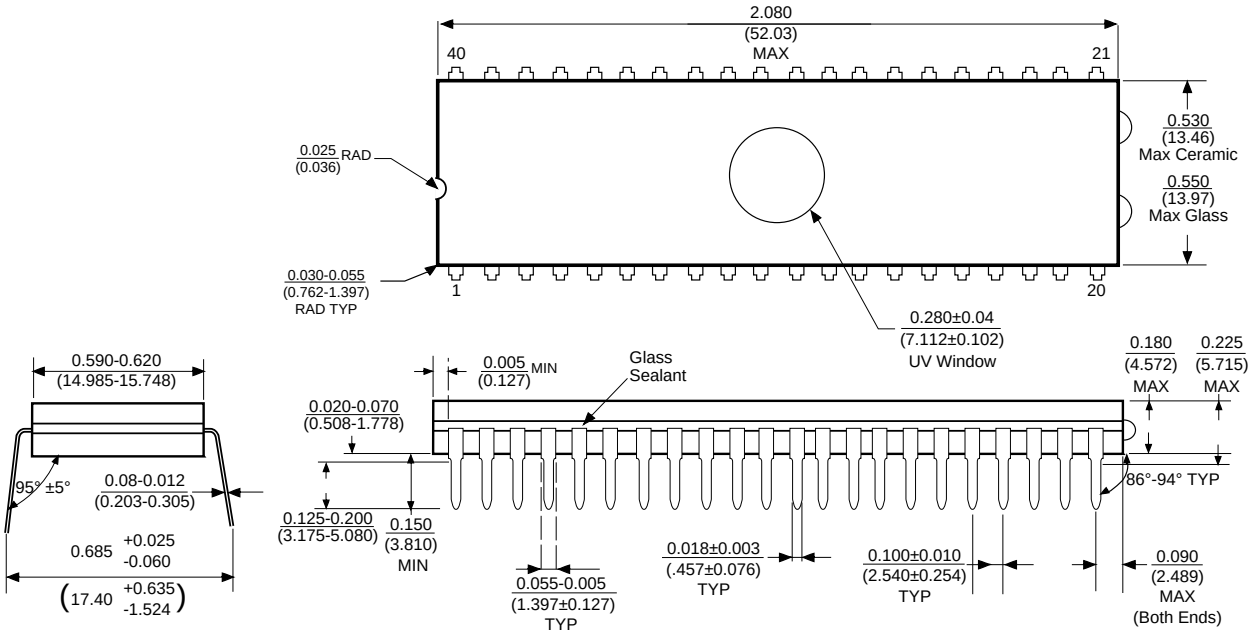
Pins / Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X (Note 16)	X	5.0V	D_{OUT}
Output Disable	X	V_{IH}	X	X	5.0V	High Z
Standby	V_{IH}	X	X	X	5.0V	High Z
Programming	V_{IL}	V_{IH}	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	X	X	12.75V	6.25V	High Z

Note 16: X can be V_{IL} or V_{IH}.

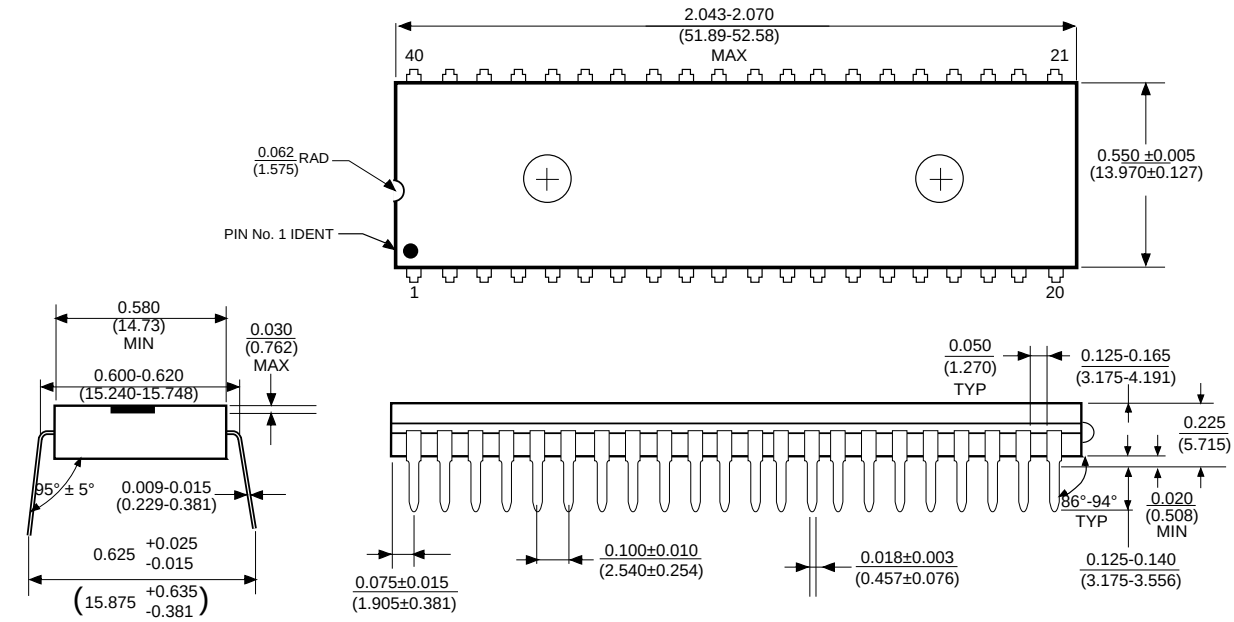
TABLE 2. Manufacturer's Identification Code

Pins	A0 (21)	A9 (31)	O7 (12)	O6 (13)	O5 (14)	O4 (15)	O3 (16)	O2 (17)	O1 (18)	O0 (19)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	1	1	0	1	0	1	1	0	D6

Physical Dimensions inches (millimeters) unless otherwise noted

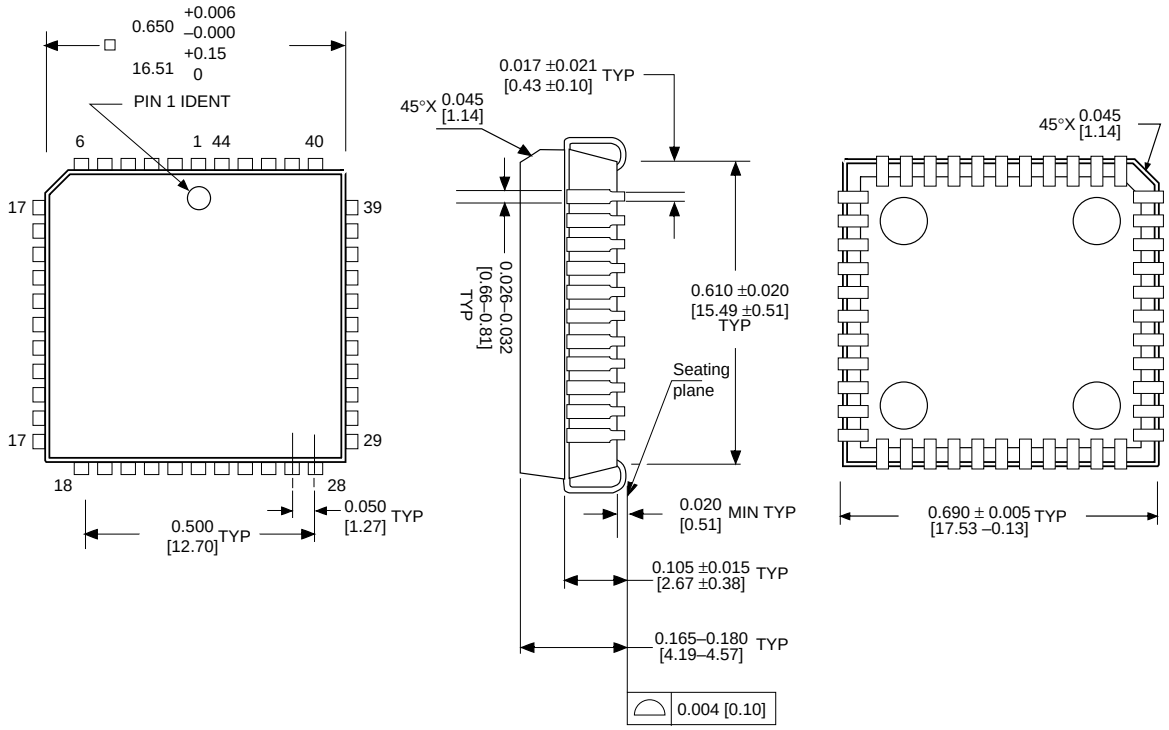


40-Lead EPROM Ceramic Dual-In-Line Package (Q)
Order Number NM27C210QXXX
Package Number J40BQ



40-Lead Molded Dual-In-Line Package (N)
Order Number NM27C210NXXX
Package Number N40A

Physical Dimensions inches (millimeters) unless otherwise noted



44-Lead Plastic Chip Carrier (V)
Order Number NM27C210VXXX
Package Number V44A

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

July 1998

NM27C240
4,194,304-Bit (256k x 16) High Performance CMOS EPROM

General Description

The NM27C240 is a high performance Electrically Programmable UV erasable ROM (EPROM). It contains 4,194,304 bits configured as 256k x 16 bits. It is offered in both erasable versions for prototyping and early production applications as well as non-erasable, plastic packaged versions that are ideal for high volume and automated assembly applications.

The NM27C240 operates from a single 5V ±10% supply in the read mode.

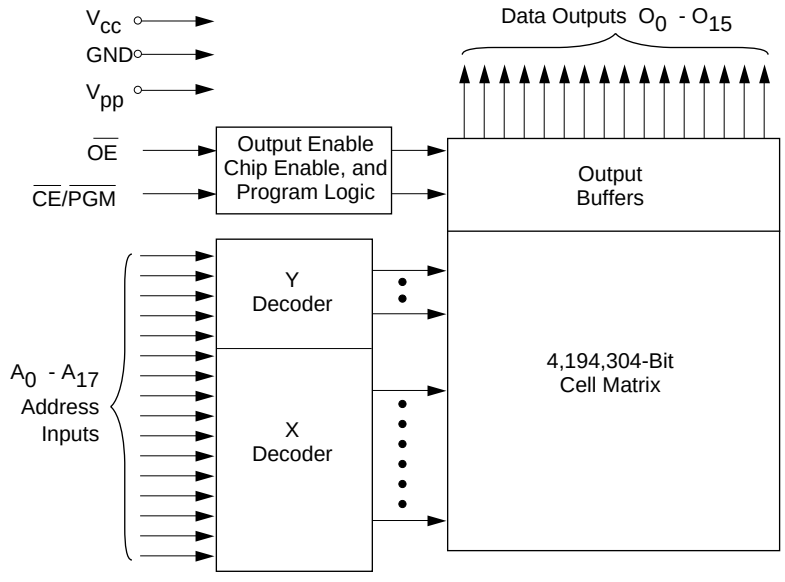
The NM27C240 is offered in both DIP and surface mount packages. The DIP package is a 40-pin dual-in-line ceramic with a quartz window to allow erasing. The surface mount package is a 44-pin PLCC that is offered in OTP.

This EPROM is manufactured using Fairchild's proprietary AMG™ EPROM technology for an excellent combination of speed and economy while providing excellent reliability.

Features

- High performance CMOS
  - —100 ns access time
- Fast turn-off for microprocessor compatibility
- Simplified upgrade path
  - —V_{PP} and PGM are "Don't Care" during normal read operation
- Compatible with 27240 and 27C240 EPROMs
- JEDEC standard pin configuration
  - —40-pin DIP package
  - —44-pin PLCC package
- Manufacturer's identification code
- Fast programming algorithm

Block Diagram



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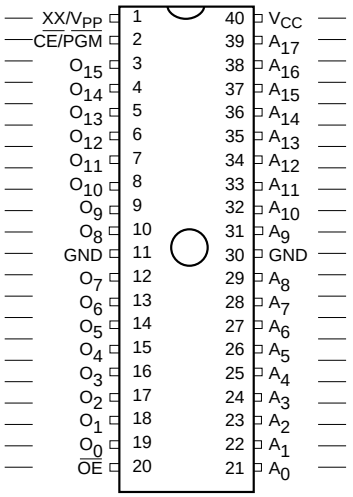
AMG™ is a trademark of WSI, Inc.

Connection Diagrams

DIP PIN CONFIGURATIONS

27C280	27C220	27C210
A_{18}	XXV_{PP}	XXV_{PP}
$\overline{CE}/\overline{PGM}$	$\overline{CE}$	$\overline{CE}$
O_{15}	O_{15}	O_{15}
O_{14}	O_{14}	O_{14}
O_{13}	O_{13}	O_{13}
O_{12}	O_{12}	O_{12}
O_{11}	O_{11}	O_{11}
O_{10}	O_{10}	O_{10}
O_9	O_9	O_9
O_8	O_8	O_8
GND	GND	GND
O_7	O_7	O_7
O_6	O_6	O_6
O_5	O_5	O_5
O_4	O_4	O_4
O_3	O_3	O_3
O_2	O_2	O_2
O_1	O_1	O_1
O_0	O_0	O_0
$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$

DIP
NM27C240



27C210	27C220	27C280
V_{CC}	V_{CC}	V_{CC}
XX/PGM	$\overline{PGM}$	A_{17}
NC	A_{16}	A_{16}
A_{15}	A_{15}	A_{15}
A_{14}	A_{14}	A_{14}
A_{13}	A_{13}	A_{13}
A_{12}	A_{12}	A_{12}
A_{11}	A_{11}	A_{11}
A_{10}	A_{10}	A_{10}
A_9	A_9	A_9
GND	GND	GND
A_8	A_8	A_8
A_7	A_7	A_7
A_6	A_6	A_6
A_5	A_5	A_5
A_4	A_4	A_4
A_3	A_3	A_3
A_2	A_2	A_2
A_1	A_1	A_1
A_0	A_0	A_0

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Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the NM27C240 pins.

Commercial Temperature Range

(0°C to +70°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C240 Q, V, N 100	100
NM27C240 Q, V, N 120	120
NM27C240 Q, V, N 150	150

Note: Surface mount PLCC package available for commercial and extended temperature ranges only.

Package types: NM27C240 Q, V, N XXX

Q = Quartz-Windowed Ceramic DIP Package

V = PLCC Package

N = Plastic DIP Package

• All packages conform to JEDEC standard.

• All versions are guaranteed to function in slower applications.

Pin Names

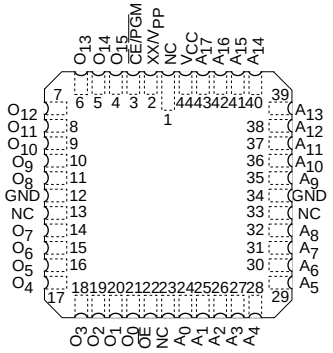
A0–A15	Addresses
$\overline{CE}/\overline{PGM}$	Chip Enable/Program
$\overline{OE}$	Output Enable
O0–O15	Outputs
XX	Don't Care (During Read)
NC	No Connect

Extended Temperature Range

(-40° to +85°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C240 QE, VE, NE 120	120
NM27C240 QE, VE, NE 150	150

PLCC Pin Configuration



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Top View

Absolute Maximum Ratings (Note 1)

Storage Temperature	-65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	-0.6V to +7V
V_{PP} and A9 with Respect to Ground	-0.6V to +14V
V_{CC} Supply Voltage with Respect to Ground	-0.6V to +7V
ESD Protection	>2000V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} + 1.0V to GND - 0.6V

Operating Range

Range	Temperature	V_{CC}	Tolerance
Commercial	0°C to +70°C	+5V	±10%
Industrial	-40V°C to +85°C	+5V	±10%

DC Read Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	Conditions		Min	Max	Units
V_{IL}	Input Low Level			-0.5	0.8	V
V_{IH}	Input High Level			2.0	V_{CC} +1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -2.5 mA		3.5		V
I_{SB1}	V_{CC} Standby Current (CMOS)	$\overline{CE} = V_{CC} \pm 0.3V$			100	µA
I_{SB2}	V_{CC} Standby Current (TTL)	$\overline{CE} = V_{IH}$			1	mA
I_{CC}	V_{CC} Active Current	$\overline{CE} = \overline{OE} = V_{IL}$, I/O = 0 mA	f=5 MHz		40	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$			10	µA
I_{LI}	Input Load Current	V_{IN} = 5.5V or GND		-1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND		-10	10	µA

AC Read Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	100		120		150		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		100		120		150	ns
t_{CE}	$\overline{CE}$ to Output Delay		100		120		150	
t_{OE}	$\overline{OE}$ to Output Delay		50		50		50	
t_{DF} (Note 2)	Output Disable to Output Float		35		35		45	
t_{OH} (Note 2)	Output Hold from Addresses $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		

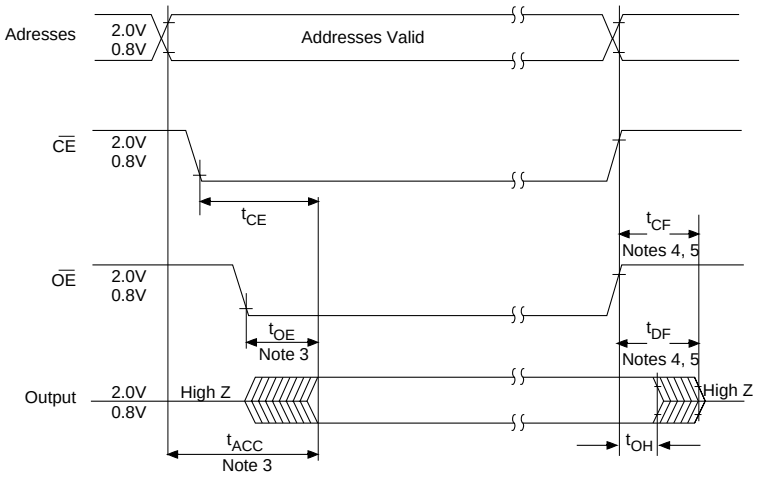
Capacitance T_A = +25˚C, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	12	20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	13	20	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7) (Note 9)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE®, the measured V_{OH1} (DC) - 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: I_{OL} = 1.6 mA, I_{OH} = -400 µA. C_L: 100 pF includes fixture capacitance.

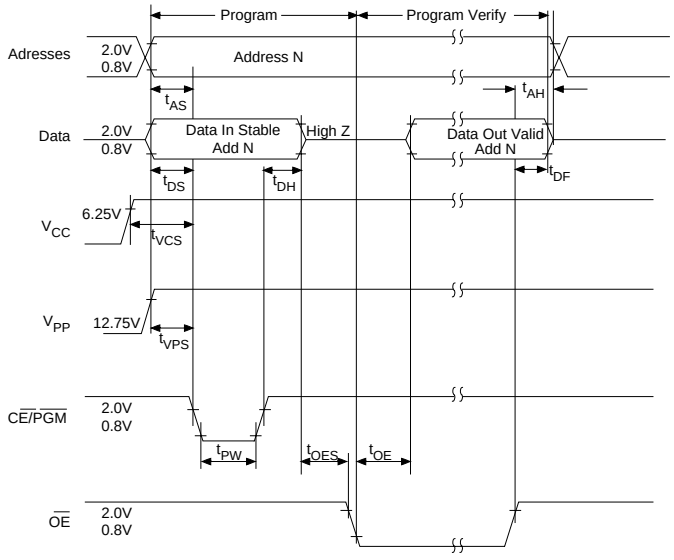
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to -2.0V for 20 ns Max.

DC Electrical Characteristics (Notes 11, 12, 13, 14)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			µs
t_{OES}	$\overline{OE}$ Setup Time		1			µs
t_{DS}	Data Setup Time		1		2.4	µs
t_{VPS}	V_{PP} Setup Time		1			µs
t_{VCS}	V_{CC} Setup Time		1			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		1			µs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		45	50	105	µs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				30	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.25	6.5	6.75	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

Programming Waveforms (Note 13)



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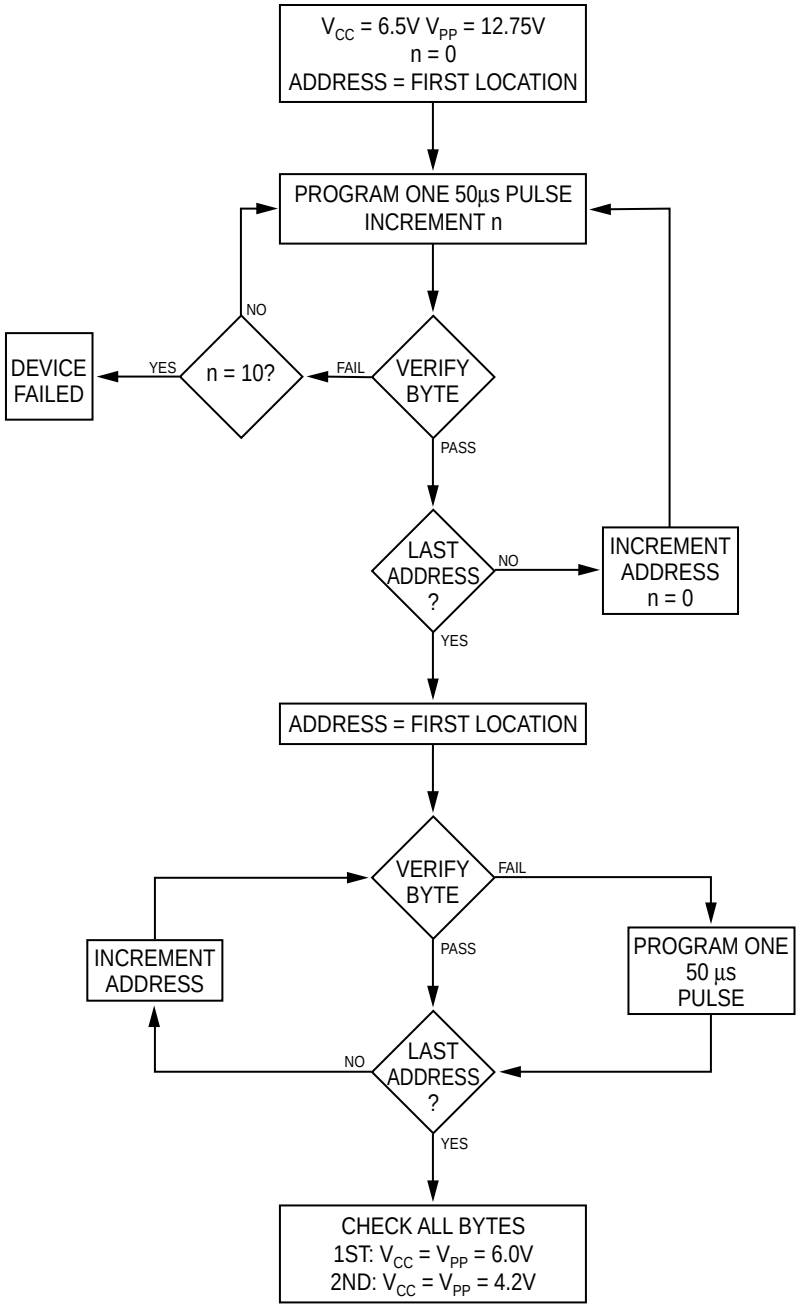
Note 11: Fairchild's standard product warranty applies only to devices programmed to specifications described herein.

Note 12: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 13: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 µF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 14: During power up the $\overline{CE}/\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

Turbo Programming Algorithm Flow Chart



DS011949-6

Note: The standard National Semiconductor algorithm may also be used but it will have longer programming time.

FIGURE 1.

Functional Description

DEVICE OPERATION

The six modes of operation of the EPROM are listed in Table 1. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. V_{CC} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.5V during the three programming modes, and at 5V in the other three modes.

Mode Selection

The modes of operation of the NM27C240 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 for device signature.

TABLE 1. Modes Selection

Mode	Pins				Outputs
	CE/ PGM	OE	V_{PP}	V_{CC}	
Read	V_{IL}	V_{IL}	X	5.0V	D_{OUT}
Output Disable	X	V_{IH}	X	5.0V	High Z
Standby	V_{IH}	X	X	5.0V	High Z
Programming	V_{IL}	V_{IH}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	X	12.75V	6.25V	High Z

Note 15: X can be V_{IL} or V_{IH}.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of the device selection. Assuming that the addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The EPROM standby mode reduces the active power dissipation by over 99%, from 165 mW to 0.55 mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the $\overline{OE}$ input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Tying

Because the EPROM is usually used in larger memory arrays, Fairchild has provided a 2-line control function that accommodates this use of multiple connections. The 2-line control function allows for:

1. the lowest possible memory power dissipation, and
2. the complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on the V_{PP} or A9 pin will damage the EPROM.

Initially, and after erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 µF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 16 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, and active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the Turbo Programming Algorithm shown in Figure 1. Each Address is programmed with a series of 50 µs pulses until it verifies good, up to a maximum of 10 pulses. Most memory cells will program with a single 50 µs pulse. (The standard National Semiconductor algorithm may also be used but it will have longer programming time.)

The EPROM must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled EPROM.

Program Inhibit

Programming multiple EPROM's in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel EPROM may be common. A TTL low level program pulse applied to an EPROM's $\overline{PGM}$ input with $\overline{CE}$ at V_{IL} and V_{PP} at 12.75V will program that EPROM. A TTL high level $\overline{CE}$ input inhibits the other EPROM's from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC}, except during programming and program verify.

Functional Description (Continued)

After Programming

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

Manufacturer's Identification Code

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The manufacturer's identification code, shown in Table 2, specifically identifies the manufacturer and device type. The code for the NM27C240 is "8FEE", where "8F" designates that it is made by Fairchild Semiconductor, and "EE" designates a 4 Megabit (256k x 16) part.

The code is accessed by applying 12V ±0.5% to address pin A9. Addresses A1–A8, A10–A15, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the lower eight data pins, O0–O7. Proper code access is only guaranteed at 25°C ±5°C.

Erasure Characteristics

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity x exposure time) for erasure should be minimum of 15W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increases as the square of the distance from the lamp (if distance is doubled the erasure time increases by factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make sure full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

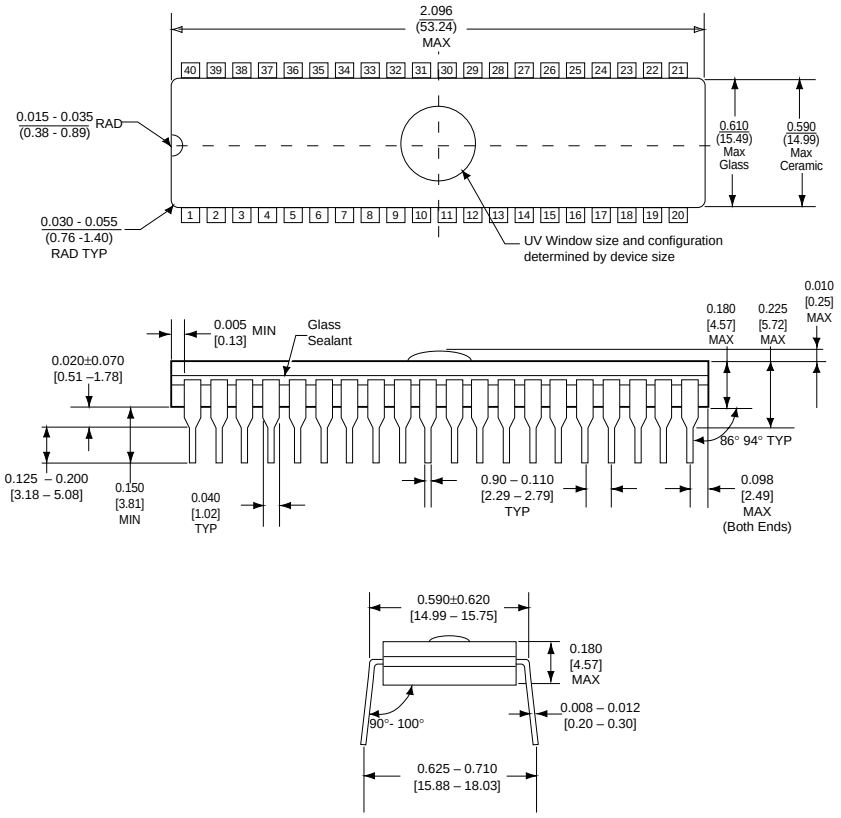
System Consideration

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

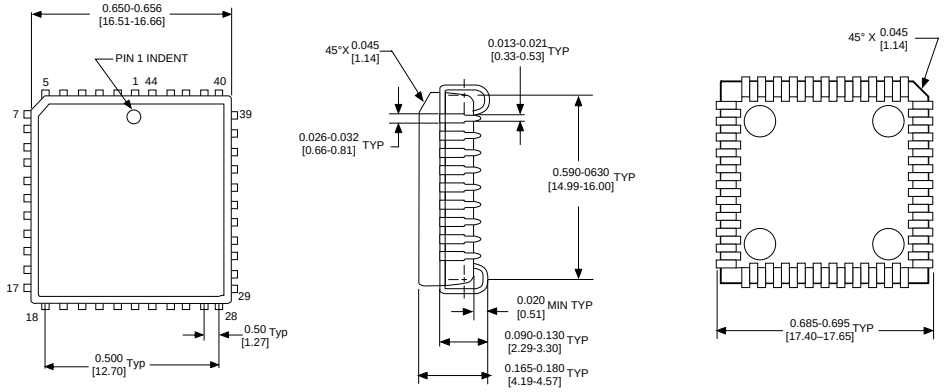
TABLE 2. Manufacturer's Identification Code

Pins	A0 (21)	A9 (31)	O7 (12)	O6 (13)	O5 (14)	O4 (15)	O3 (16)	O2 (17)	O1 (18)	O0 (19)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	1	1	1	0	1	1	1	0	EE

Physical Dimensions inches (millimeters) unless otherwise noted

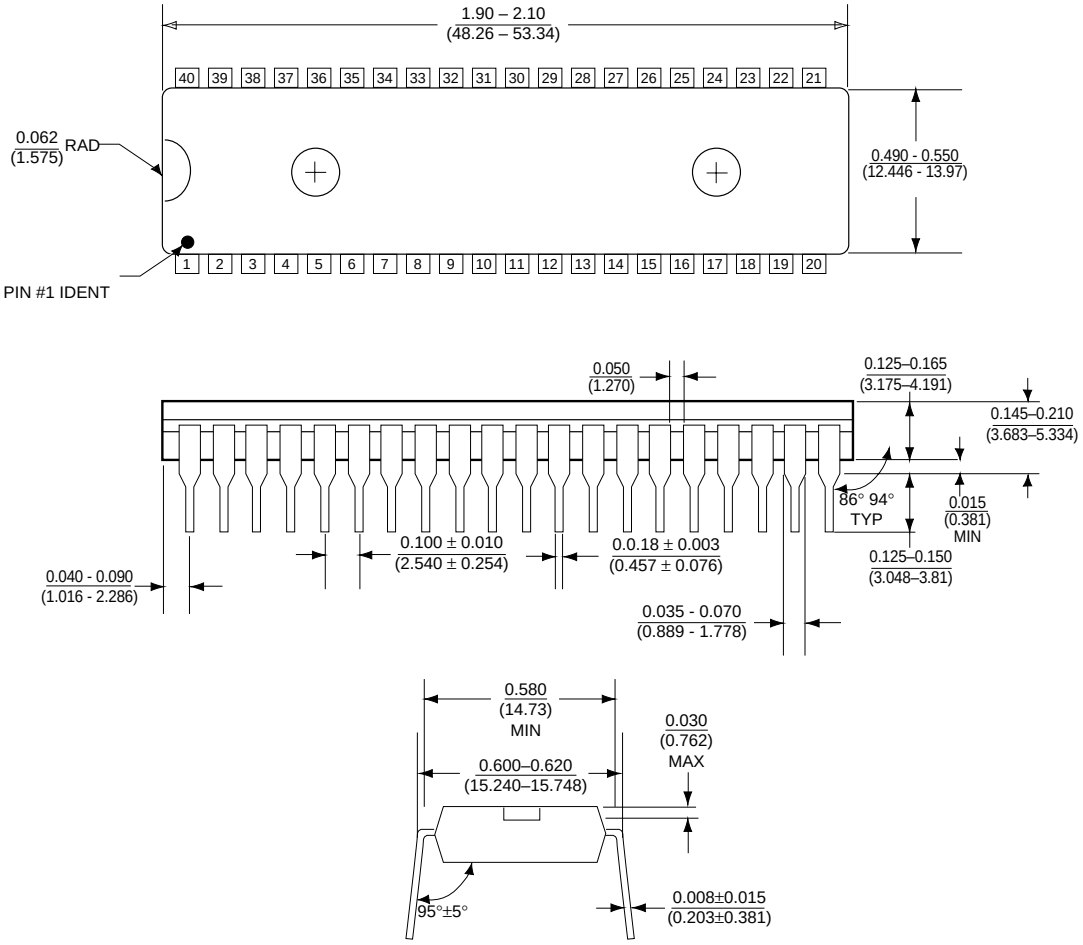


40-Lead Ceramic Dual-In-Line Package (Q)
Order Number NM27C240Qxxx
Package Number J40BQ



44-Lead Plastic Chip Carrier (V)
Order Number NM27C240Vxxx
Package Number V44A

Physical Dimensions inches (millimeters) unless otherwise noted



40-Lead Plastic Molded Dual-In-Line (N)
Order Number NM27C240Nxxx

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

July 1998

NM27C256
262,144-Bit (32K x 8) High Performance CMOS EPROM

General Description

The NM27C256 is a 256K Electrically Programmable Read Only Memory. It is manufactured in Fairchild's latest CMOS split gate EPROM technology which enables it to operate at speeds as fast as 90 ns access time over the full operating range.

The NM27C256 provides microprocessor-based systems extensive storage capacity for large portions of operating system and application software. Its 90 ns access time provides high speed operation with high-performance CPUs. The NM27C256 offers a single chip solution for the code storage requirements of 100% firmware-based equipment. Frequently-used software routines are quickly executed from EPROM storage, greatly enhancing system utility.

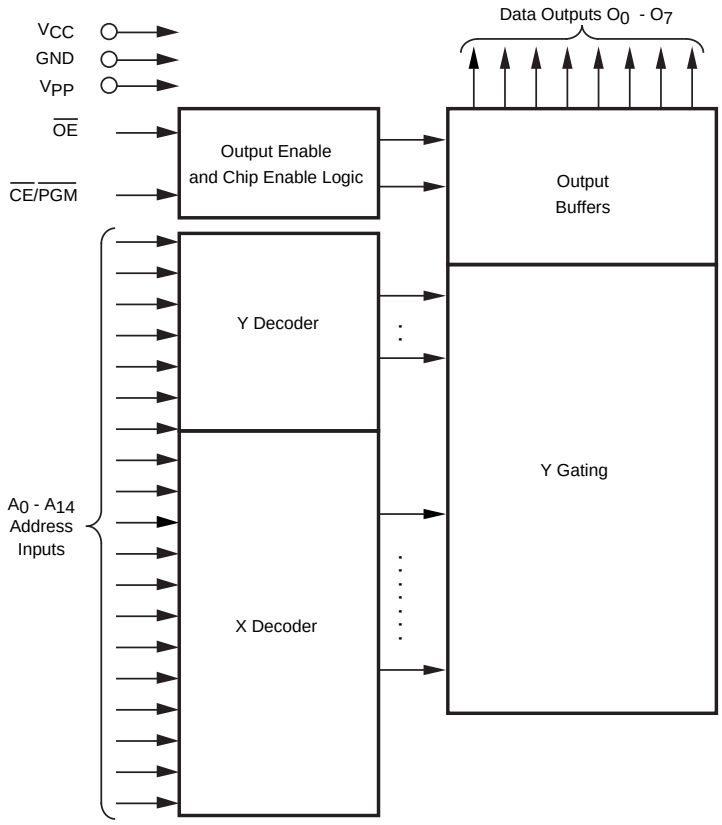
The NM27C256 is configured in the standard EPROM pinout which provides an easy upgrade path for systems which are currently using standard EPROMs.

The NM27C256 is one member of a high density EPROM Family which range in densities up to 4 Mb.

Features

- High performance CMOS
  - —90 ns access time
- JEDEC standard pin configuration
  - — 28-pin PDIP package
  - — 32-pin chip carrier
  - — 28-pin CERDIP package
- Drop-in replacement for 27C256 or 27256
- Manufacturer's identification code

Block Diagram



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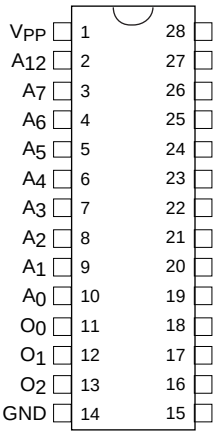
Connection Diagrams

27C080	27C040	27C020	27C010	27C512
A_{19}	XX/V_{PP}	XX/V_{PP}	XX/V_{PP}	
A_{16}	A_{16}	A_{16}	A_{16}	
A_{15}	A_{15}	A_{15}	A_{15}	A_{15}
A_{12}	A_{12}	A_{12}	A_{12}	A_{12}
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

DIP
NM27C256



27C512	27C010	27C020	27C040	27C080
	V_{CC}	V_{CC}	V_{CC}	V_{CC}
	XX/$\overline{PGM}$	XX/$\overline{PGM}$	A_{18}	A_{18}
V_{CC}	XX	A_{17}	A_{17}	A_{17}
A_{14}	A_{14}	A_{14}	A_{14}	A_{14}
A_{13}	A_{13}	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9
A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$/V_{PP}	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$/V_{PP}
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$/$\overline{PGM}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$/$\overline{PGM}$	$\overline{CE}$/$\overline{PGM}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the NM27C256 pins.

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Commercial Temp. Range (0°C to +70°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C256 Q, N, V 90	90
NM27C256 Q, N, V 100	100
NM27C256 Q, N, V 120	120
NM27C256 Q, N, V 150	150
NM27C256 Q, N, V 200	200

Extended Temp. Range (-40°C to +85°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C256 QE, NE, VE 120	120
NM27C256 QE, NE, VE 150	150
NM27C256 QE, NE, VE 200	200

Note: Surface mount PLCC package available for commercial and extended temperature ranges only.

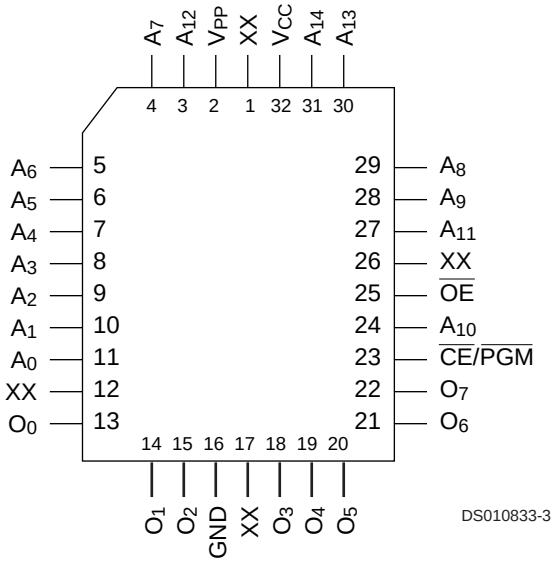
Package Types: NM27C256 Q, N, V XXX
- Q = Quartz-Windowed Ceramic DIP
- N = Plastic OTP DIP
- V = Surface-Mount PLCC

- All Packages conform to the JEDEC standard.
- All versions are guaranteed to function for slower speeds.

Pin Names

Symbol	Description
A0–A14	Addresses
$\overline{CE}$/$\overline{PGM}$	Chip Enable/Program
$\overline{OE}$	Output Enable
O0–O7	Outputs
XX	Don't Care (during Read)

PLCC



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Top

Absolute Maximum Ratings (Note 1)

Storage Temperature	-65°C to +150°C
All Input Voltages except A9 with Respect to Ground	-0.6V to +7V
V_{PP} and A9 with Respect to Ground	-0.7V to +14V
V_{CC} Supply Voltage with Respect to Ground	-0.6V to +7V
ESD Protection	> 2000V
All Output Voltages with Respect to Ground	V_{CC} + 1.0V to GND -0.6V

Operating Range

Range	Temperature	V_{CC}
Comm'l	0°C to +70°C	+5V ±10%
Industrial	-40°C to +85°C	+5V ±10%

Read Operation

DC Electrical Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IL}	Input Low Level		-0.5	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} +1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -2.5 mA	3.5		V
I_{SB1} (Note 11)	V_{CC} Standby Current (CMOS)	$\overline{CE}$ = V_{CC} ±0.3V		100	µA
I_{SB2}	V_{CC} Standby Current (TTL)	$\overline{CE}$ = V_{IH}		1	mA
I_{CC1}	V_{CC} Active Current TTL Inputs	$\overline{CE}$ = $\overline{OE}$ = V_{IL},f=5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		35	mA
I_{PP}	V_{PP} Supply Current	V_{PP} = V_{CC}		10	µA
V_{PP}	V_{PP} Read Voltage		V_{CC} - 0.7	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or GND	-1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND	-10	10	µA

AC Electrical Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	90		100		120		150		200		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		90		100		120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay		90		100		120		150		200	
t_{OE}	$\overline{OE}$ to Output Delay		35		50		50		50		50	
t_{DF} (Note 2)	Output Disable to Output Float		30		30		35		45		45	
t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		0		0		

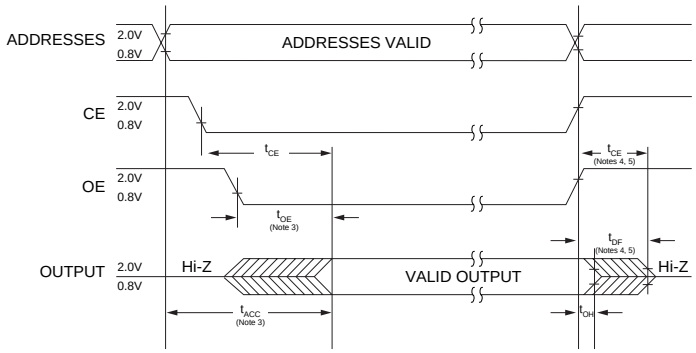
Capacitance (Note 2) T_A = +25˚C, f = 1 MHz

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	6	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	9	12	pF

AC Test Conditions

Output Load	1 TTL Gate and CL = 100 pF (Note 8)
Input Rise and Fall Times	≤ 5 ns
Input Pulse Levels	0.45 to 2.4V
Timing Measurement Reference Level (Note 10)	
Inputs	0.8V and 2.0V
Outputs	0.8V and 2.0V

AC Waveforms (Note 6) (Note 7) (Note 9)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE®, the measured V_{OH1} (DC) - 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: TTL Gate: I_{OL} = 1.6 mA, I_{OH} = -400 µA.
C_L = 100 pF includes fixture capacitance.

Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to -2.0V for 20 ns Max.

Note 11: CMOS inputs: V_{IL} = GND ±0.3V, V_{IH} = V_{CC} ±0.3V.

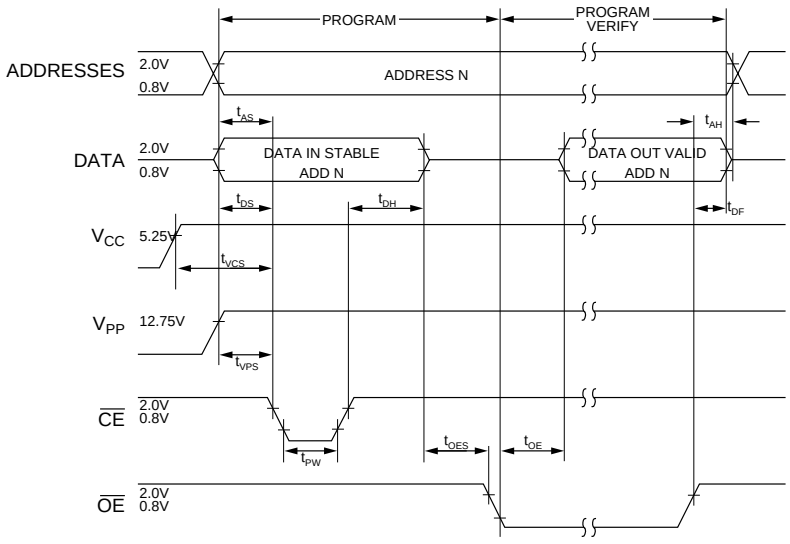
Programming Characteristics (Note 12) (Note 13) (Note 14) (Note 15)

Symbol	Parameter	Conditions	Min	Typ	Max	Units

Programming Characteristics (Note 12) (Note 13) (Note 14) (Note 15) (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			µs
t_{OES}	$\overline{OE}$ Setup Time		1			µs
t_{VPS}	V_{PP} Setup Time		1			µs
t_{VCS}	V_{CC} Setup Time		1			µs
t_{DS}	Data Setup Time		1			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		1			µs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		45	50	105	µs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				50	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.25	6.5	6.75	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

Programming Waveforms (Note 14)



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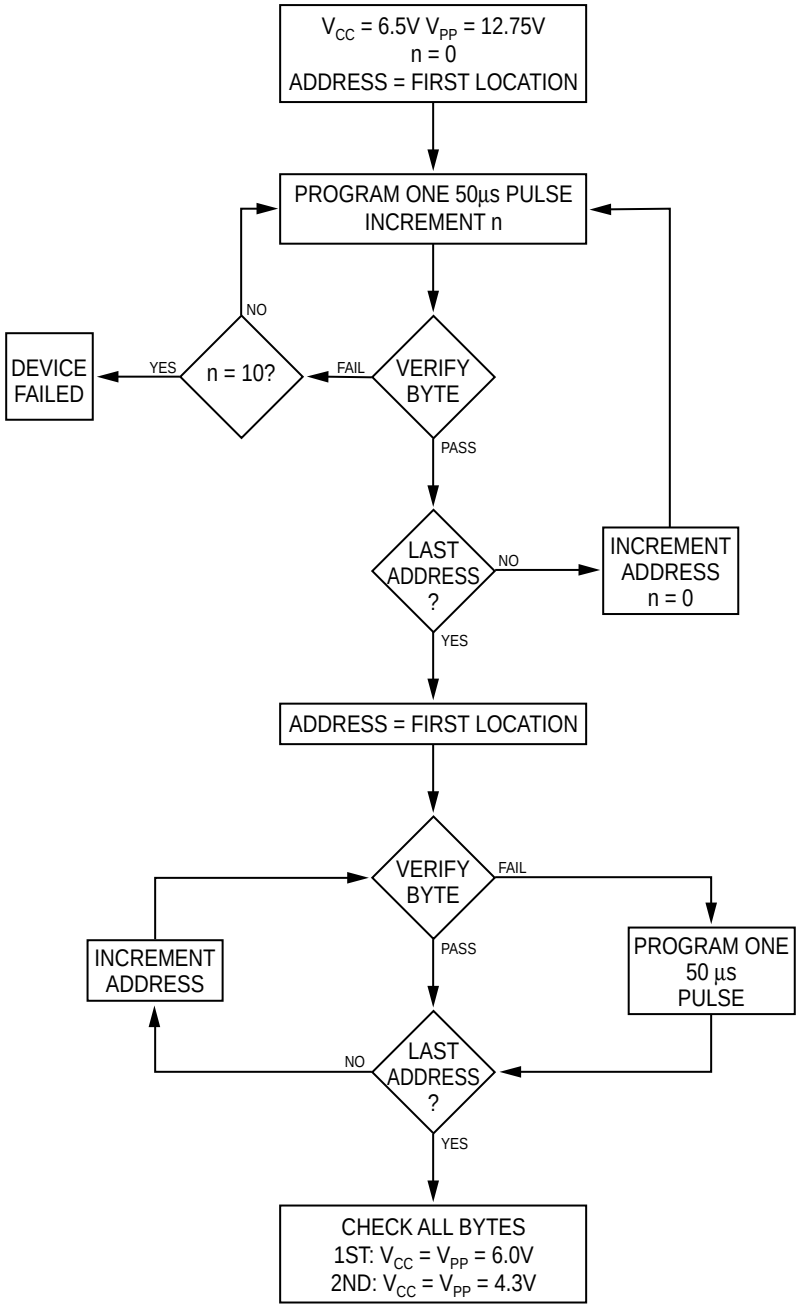
Note 12: Fairchild's standard product warranty applies to devices programmed to specifications described herein.

Note 13: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 14: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 µF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 15: During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

Turbo Programming Algorithm Flow Chart



Note: The standard National Semiconductor algorithm may also be used but it will have longer programming time.

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FIGURE 1.

Functional Description

DEVICE OPERATION

The six modes of operation of the EPROM are listed in Table 1. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.5V during the three programming modes, and at 5V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$/$\overline{PGM}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$/$\overline{PGM}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from 385 mW to 0.55 mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$/$\overline{PGM}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the $\overline{OE}$ input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Typing

Because the EPROM is usually used in larger memory arrays, Fairchild has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

1. the lowest possible memory power dissipation, and
2. complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$/$\overline{PGM}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 µF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{CE}$/$\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the Turbo Programming Algorithm shown in Figure 1. Each Address is programmed with a series of 50 µs pulses until it verifies good, up to a maximum of 10 pulses. Most memory cells will program with a single 50 µs pulse. (The standard National Semiconductor Algorithm may also be used but it will have longer programming time.)

The EPROM must not be programmed with a DC signal applied to the $\overline{CE}$/$\overline{PGM}$ input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirments. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$/$\overline{PGM}$ input programs the paralleled EPROM.

Program Inhibit

Programming multiple EPROMs in parallel with different data is also easily accomplished. Except for $\overline{CE}$/$\overline{PGM}$, all like inputs (including $\overline{OE}$) of the parallel EPROMs may be common. A TTL low level program pulse applied to an EPROM's CE/PGM input with V_{PP} at 12.75V will program that EPROM. A TTL high level $\overline{CE}$/$\overline{PGM}$ input inhibits the other EPROMs from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC}, except during programming and program verify.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table 2, specifically identifies the manufacturer and device type. The code for NM27C256 is "8F04", where "8F" designates that it is made by Fairchild Semiconductor, and "04" designates a 256K part.

The code is accessed by applying 12V ±0.5V to address pin A9. Addresses A1–A8, A10–A16, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O0 –O7. Proper code access is only guaranteed at 25°C to ±5°C.

Functional Description (Continued)

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increases as the square of the distance from the lamp (if distance is doubled the erasure time increases by factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, $I_{CC,}$ has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent of the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

Mode Selection

The modes of operation of NM27C256 listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 for device signature.

TABLE 1. Modes Selection

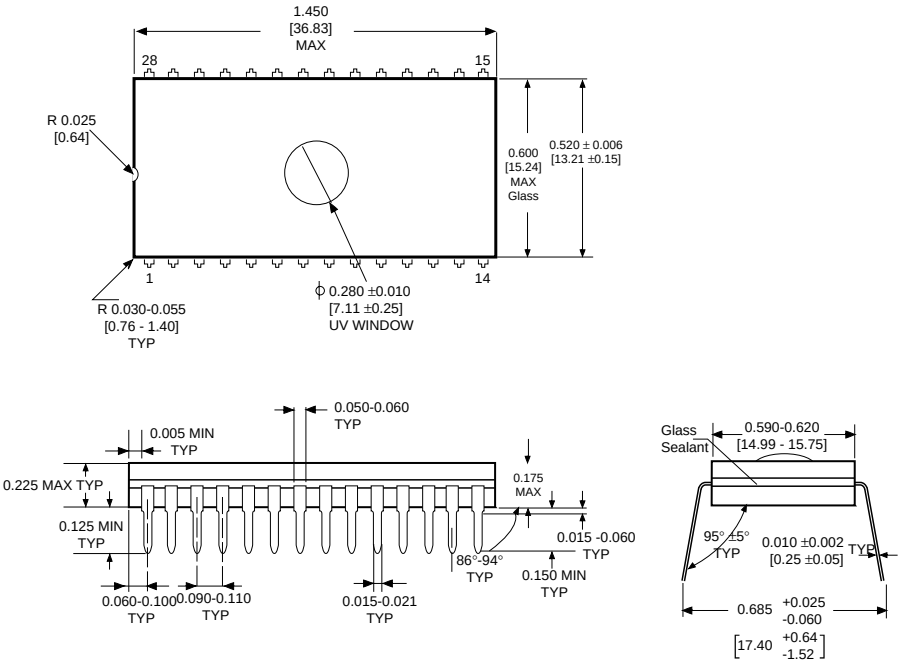
Pins / Mode	$\overline{CE}/\overline{PGM}$	$\overline{OE}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{CC}	5.0V	D_{OUT}
Output Disable	X (Note 16)	V_{IH}	V_{CC}	5.0V	High-Z
Standby	V_{IH}	X	V_{CC}	5.0V	High-Z
Programming	V_{IL}	VIH	12.75V	6.25V	D_{IN}
Program Verify	V_{IH}	V_{IL}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	12.75V	6.25V	High-Z

Note 16: X can be V_{IL} or V_{IH}.

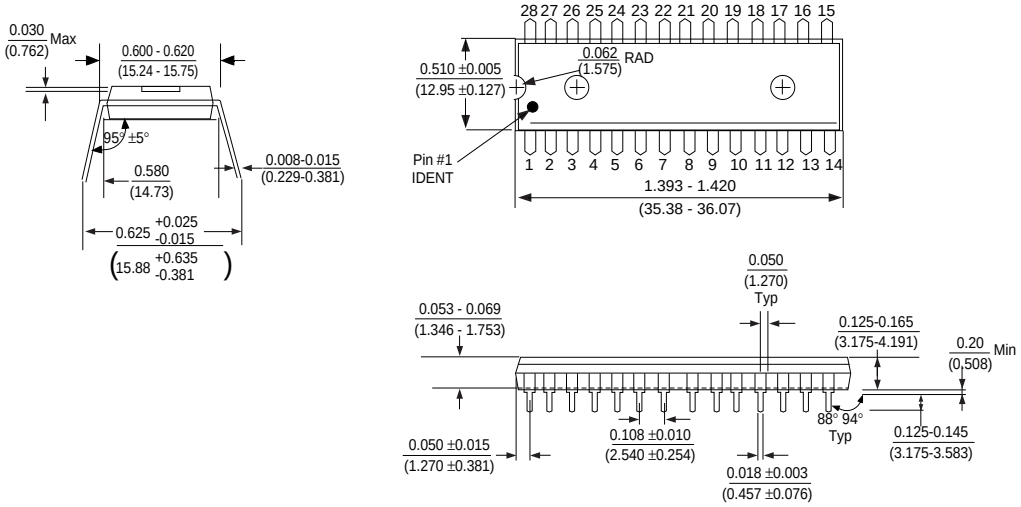
TABLE 2. Manufacturer's Identification Code

Pins	A0 (10)	A9 (24)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	0	0	0	0	0	1	0	0	04

Physical Dimensions inches (millimeters) unless otherwise noted

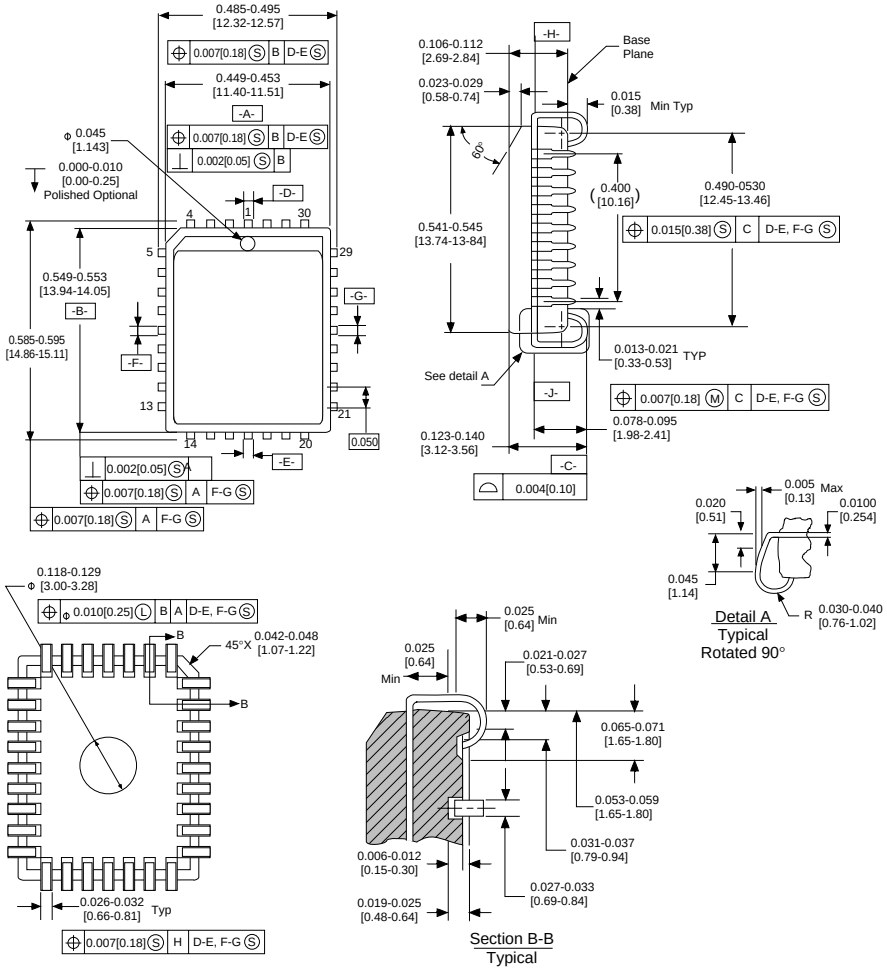


UV Window Cavity Dual-In-Line CerDIP Package (Q)
Order Number NM27C256QXXX
Package Number J28AQ



28-Lead Plastic One-Time-Programmable Dual-In-Line Package
Order Number NM27C256NXXX
Package Number N28B

Physical Dimensions inches (millimeters) unless otherwise noted



32-Lead Plastic Leaded Chip Carrier (PLCC)
Order Number NM27C256VXXX
Package Number VA32A

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

July 1998

NM27C512
524,288-Bit (64K x 8) High Performance CMOS EPROM

General Description

The NM27C512 is a high performance 512K UV Erasable Electrically Programmable Read Only Memory (EPROM). It is manufactured using Fairchild's proprietary CMOS AMG™ EPROM technology for an excellent combination of speed and economy while providing excellent reliability.

The NM27C512 provides microprocessor-based systems storage capacity for portions of operating system and application software. Its 90 ns access time provides no wait-state operation with high-performance CPUs. The NM27C512 offers a single chip solution for the code storage requirements of 100% firmware-based equipment. Frequently-used software routines are quickly executed from EPROM storage, greatly enhancing system utility.

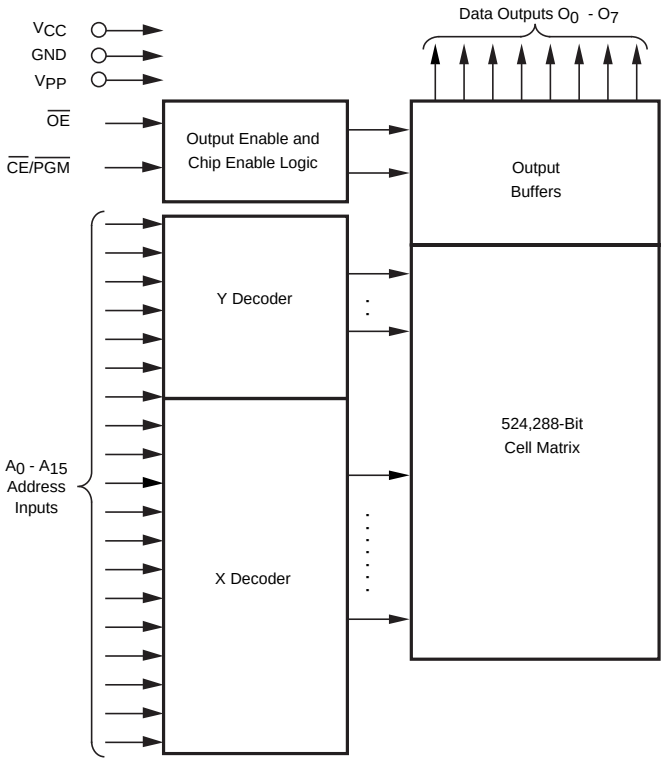
The NM27C512 is configured in the standard JEDEC EPROM pinout which provides an easy upgrade path for systems which are currently using standard EPROMs.

The NM27C512 is one member of a high density EPROM Family which range in densities up to 4 Megabit.

Features

- High performance CMOS
  - — 90 ns access time
- Fast turn-off for microprocessor compatibility
- Manufacturers identification code
- JEDEC standard pin configuration
  - — 28-pin PDIP package
  - — 32-pin chip carrier
  - — 28-pin CERDIP package

Block Diagram



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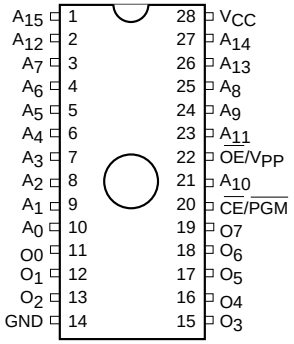
AMG is a trademark of WSI, Inc.

Connection Diagrams

27C080	27C040	27C020	27C010	27C256
A_{19}	XX/V_{PP}	XX/V_{PP}	XX/V_{PP}	
A_{16}	A_{16}	A_{16}	A_{16}	
A_{15}	A_{15}	A_{15}	A_{15}	V_{PP}
A_{12}	A_{12}	A_{12}	A_{12}	A_{12}
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

DIP
NM27C512



27C256	27C010	27C020	27C040	27C080
	V_{CC}	V_{CC}	V_{CC}	V_{CC}
	XX/PGM	XX/PGM	A_{18}	A_{18}
V_{CC}	XX	A_{17}	A_{17}	A_{17}
A_{14}	A_{14}	A_{14}	A_{14}	A_{14}
A_{13}	A_{13}	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9
A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A10	A10	A10	A10	A10
$\overline{CE/PGM}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE/PGM}$	$\overline{CE/PGM}$
O7	O7	O7	O7	O7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O4	O4	O4	O4	O4
O_3	O_3	O_3	O_3	O_3

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Compatible EPROM pin configurations are shown in the blocks adjacement to the NM27C512 pins.

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Access Time (ns)
NM27C512 Q, N, V 90	90
NM27C512 Q, N, V 120	120
NM27C512 Q, N, V 150	150

Industrial Temp Range (-40°C to +85°C)

Parameter/Order Number	Access Time (ns)
NM27C512 QE, NE, VE 120	120
NM27C512 QE, NE, VE 150	150

Q = Quartz-Windowed Ceramic DIP Package

N = Plastic DIP Package

V = PLCC Package

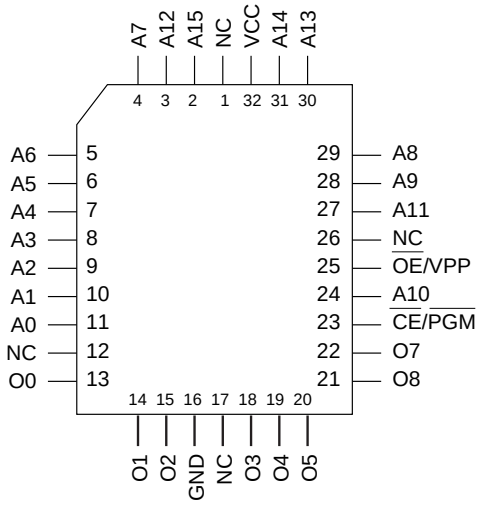
• All packages conform to the JEDEC standard.

• All versions are guaranteed to function for slower speeds.

Pin Names

A0–A15	Addresses
$\overline{CE}/\overline{PGM}$	Chip Enable/Program
$\overline{OE}$	Output Enable
O0–O7	Outputs
NC	Don't Care (During Read)

PLCC



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Absolute Maximum Ratings (Note 1)

Storage Temperature	-65°C to +150°C
All Input Voltages Except A9 with Respect to Ground	-0.6V to +7V
V_{PP} and A9 with Respect to Ground	-0.7V to +14V
V_{CC} Supply Voltage with Respect to Ground	-0.6V to +7V
ESD Protection (MIL Std. 883, Method 3015.2)	>2000V
All Output Voltages with Respect to Ground	V_{CC} + 1.0V to GND -0.6V

Operating Range

Range	Temperature	V_{CC}	Tolerance
Commercial	0°C to +70°C	+5V	±10%
Industrial	-40°C to +85°C	+5V	±10%

Read Operation

DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IL}	Input Low Level		-0.5	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} +1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -2.5 mA	3.5		V
I_{SB1}	V_{CC} Standby Current (CMOS)	$\overline{CE}$ = V_{CC} ±0.3V		100	µA
I_{SB2}	V_{CC} Standby Current	$\overline{CE}$ = V_{IH}		1	mA
I_{CC1}	V_{CC} Active Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, f = 5 MHz		40	mA
I_{CC2}	V_{CC} Active Current CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA C, E Temp Ranges		35	mA
I_{PP}	V_{PP} Supply Current	V_{PP} = V_{CC}		10	µA
V_{PP}	V_{PP} Read Voltage		V_{CC} - 0.7	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or GND	-1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND	-10	10	µA

AC Electrical Characteristics

Symbol	Parameter	90		120		150		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		90		120		150	ns
t_{CE}	$\overline{CE}$ to Output Delay		90		120		150	
t_{OE}	$\overline{OE}$ to Output Delay		40		50		50	
t_{DF}	Output Disable to Output Float		35		25		45	
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		

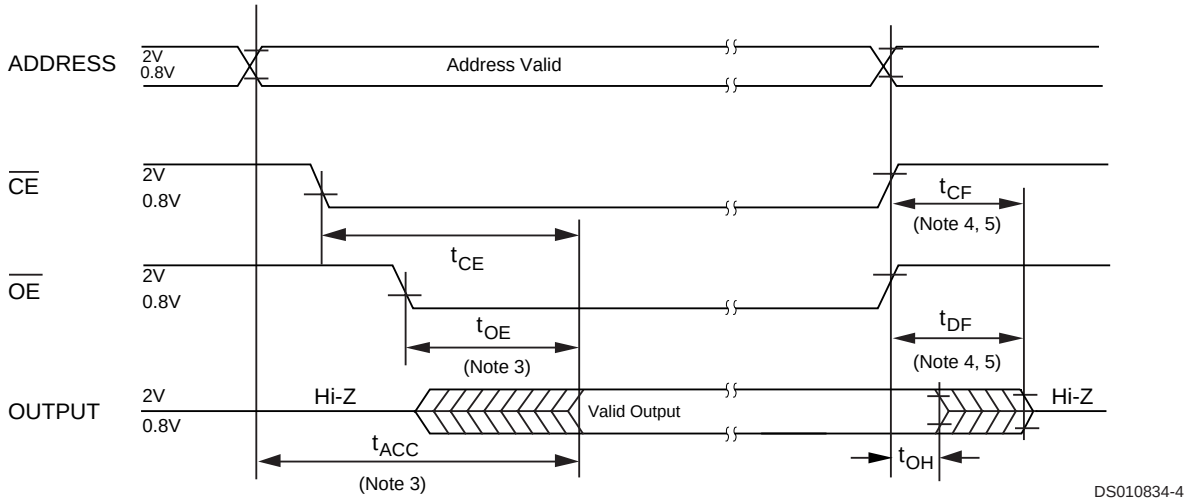
Capacitance T_A = +25°C, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN1}	Input Capacitance except $\overline{OE}/V_{PP}$	V_{IN} = 0V	6	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	9	12	pF
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance	V_{IN} = 0V	20	25	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level (Note 9)	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7)



Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) - 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

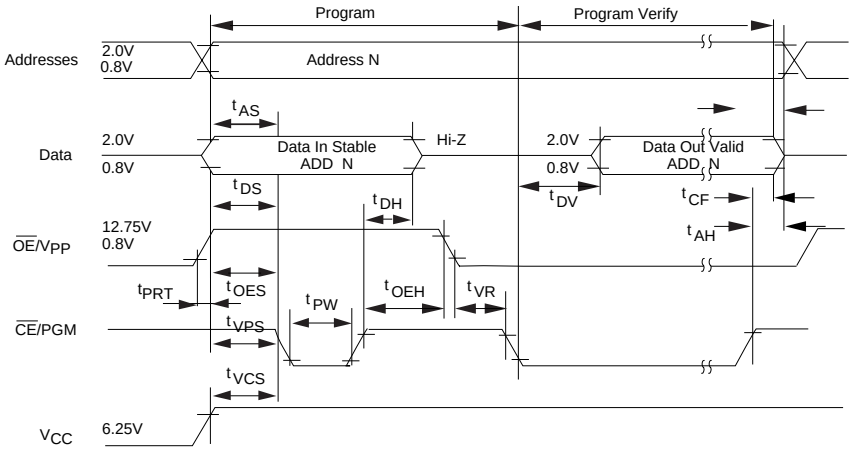
Note 8: 1 TTL Gate: I_{OL} = 1.6 mA, I_{OH} = -400 µA. C_L: 100 pF includes fixture capacitance.

Note 9: Inputs and outputs can undershoot to -2.0V for 20 ns Max.

Programming Characteristics (Note 10) and (Note 11)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			µs
t_{OES}	$\overline{OE}$ Setup Time		1			µs
t_{DS}	Data Setup Time		1			µs
t_{VCS}	V_{CC} Setup Time		1			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		1			µs
t_{CF}	Chip Enable to Output Float Delay	$\overline{OE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		45	50	105	µs
t_{OEH}	$\overline{OE}$ Hold Time		1			µs
t_{DV}	Data Valid from $\overline{CE}$	$\overline{OE} = V_{IL}$			250	ns
t_{PRT}	$\overline{OE}$ Pulse Rise Time during Programming		50			ns
t_{VR}	V_{PP} Recovery Time		1			µs
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{PP}$			30	mA
I_{CC}	V_{CC} Supply Current				50	mA
T_R	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.25	6.5	6.75	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0	0.45	V
V_{IH}	Input High Voltage		2.4	4		V
t_{IN}	Input Timing Reference Voltage		0.8		2	V
t_{OUT}	Output Timing Reference Voltage		0.8		2	V

Programming Waveforms



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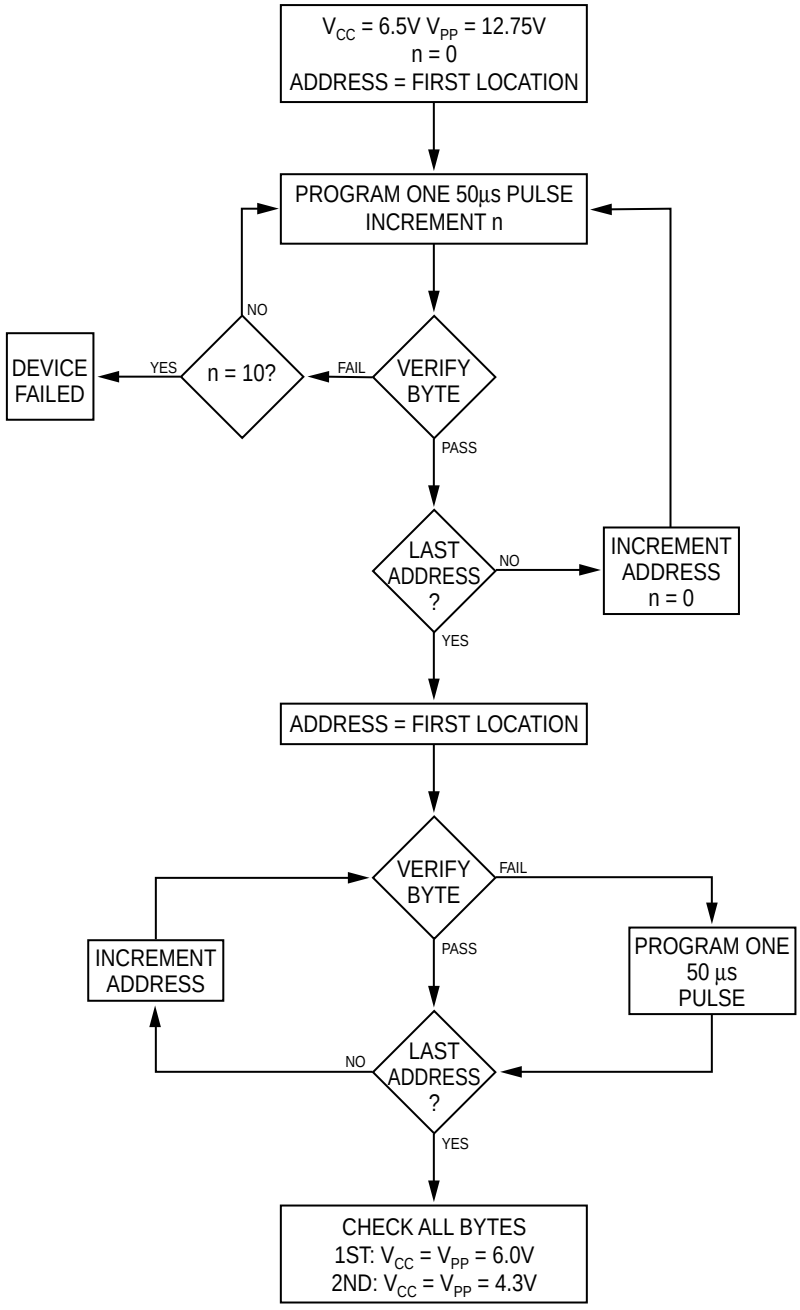
Note 10: Fairchild's standard product warranty applies to devices programmed to specifications described herein.

Note 11: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 12: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 µF capacitor is required across V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Turbo Programming Algorithm Flow Chart



Note: The standard National Semiconductor algorithm may also be used but it will take longer programming time.

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FIGURE 1.

Functional Description

DEVICE OPERATION

The six modes of operation of the EPROM are listed in Table1. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and $\overline{OE}/V_{PP}$. The $\overline{OE}/V_{PP}$ power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.5V during the three programming modes, and at 5V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$/PGM) is the power control and should be used for device selection. Output Enable ($\overline{OE}/V_{PP}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from 220 mW to 0.55 mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$/PGM input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the $\overline{OE}$ input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Typing

Because the EPROM is usually used in larger memory arrays, Fairchild has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

1. the lowest possible memory power dissipation, and
2. complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$/PGM be decoded and used as the primary device selecting function, while $\overline{OE}/V_{PP}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus.

This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 22 ($\overline{OE}/V_{PP}$) will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the $\overline{OE}/V_{PP}$ is at 12.75V. It is required that at least a 0.1 µF capacitor be placed across V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{CE}$/PGM input. A program pulse must be applied at each address location to be programmed.

The EPROM is programmed with the Turbo Programming Algorithm shown in Figure 1. Each Address is programmed with a series of 50 µs pulses until it verifies good, up to a maximum of 10 pulses. Most memory cells will program with a single 50 µs pulse. (The standard National Semiconductor Algorithm may also be used but it will have longer programming time.)

The EPROM must not be programmed with a DC signal applied to the $\overline{CE}$/PGM input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$/PGM input programs the paralleled EPROM.

Program Inhibit

Programming multiple EPROMs in parallel with different data is also easily accomplished. Except for $\overline{CE}$/PGM all like inputs (including $\overline{OE}/V_{PP}$) of the parallel EPROMs may be common. A TTL low level program pulse applied to an EPROM's $\overline{CE}$/PGM input with $\overline{OE}/V_{PP}$ at 12.75V will program that EPROM. A TTL high level $\overline{CE}$/PGM input inhibits the other EPROMs from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified T_{DV} after the falling edge of $\overline{CE}$.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table 2, specifically identifies the manufacturer and device type. The code for NM27C512 is "8F85", where "8F" designates that it is made by Fairchild Semiconductor, and "85" designates a 512K part.

The code is accessed by applying 12V ±0.5V to address pin A9. Addresses A1–A8, A10–A16, and all control pins

Functional Description (Continued)

are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O0 –O 7 . Proper code access is only guaranteed at 25°C ±5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity x exposure time) for erasure should be minimum of 15W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increases as the square of the distance from the lamp (if distance is doubled the erasure time increases by factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

Mode Selection

The modes of operation of the NM27C512 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels excepts for V_{PP} and A9 for device signature.

TABLE 1. Mode Selection

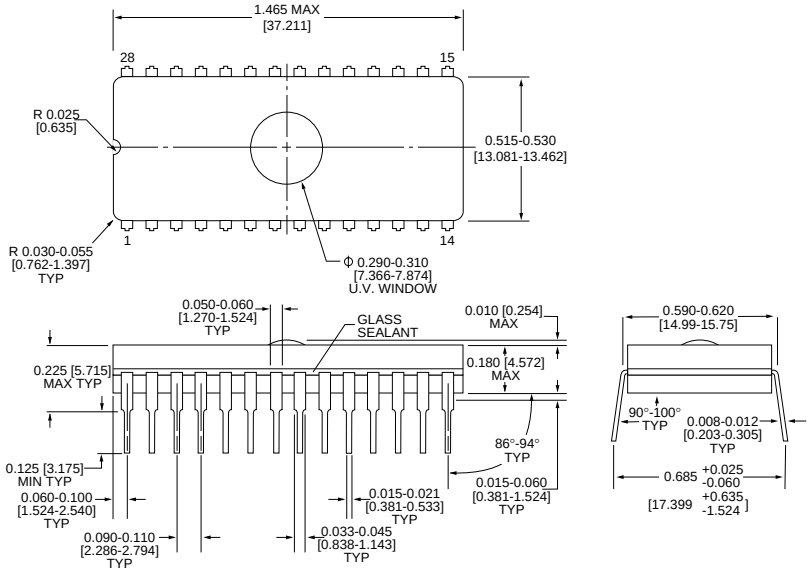
Mode \ Pins	$\overline{CE}/\overline{PGM}$	$\overline{OE}/V_{PP}$	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	5.0V	D_{OUT}
Output Disable	X (Note 13)	V_{IH}	5.0V	High Z
Standby	V_{IH}	X	5.0V	High Z
Programming	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	6.25V	D_{OUT}
Program Inhibit	V_{IH}	12.75V	6.25V	High Z

Note 13: X can be V_{IL} or V_{IH}.

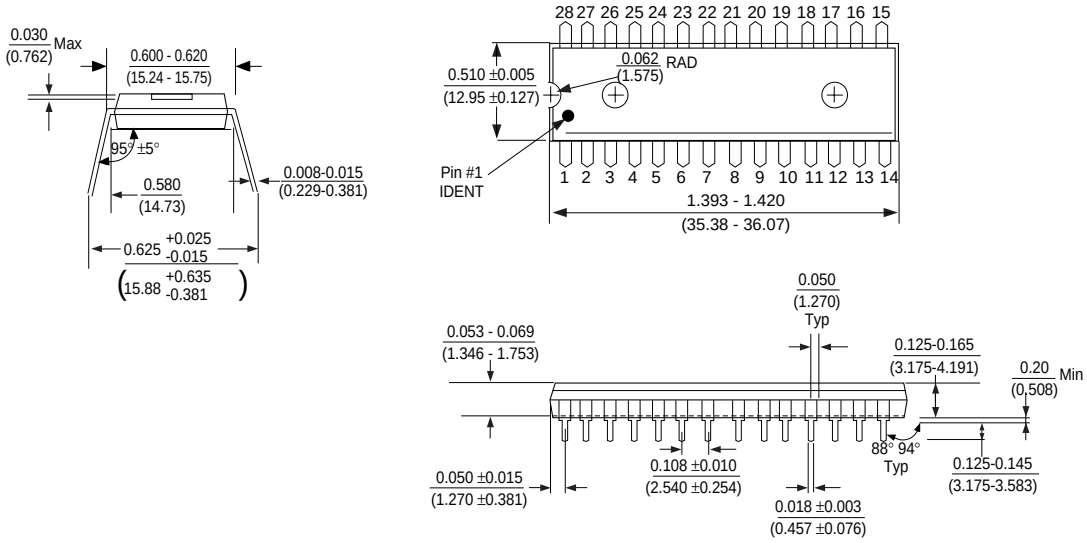
TABLE 2. Manufacturer's Identification Code

Pins	A0 (10)	A9 (24)	07 (19)	06 (18)	05 (17)	04 (16)	03 (15)	02 (13)	01 (12)	00 (11)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	1	0	0	0	0	1	0	1	85

Physical Dimensions inches (millimeters) unless otherwise noted

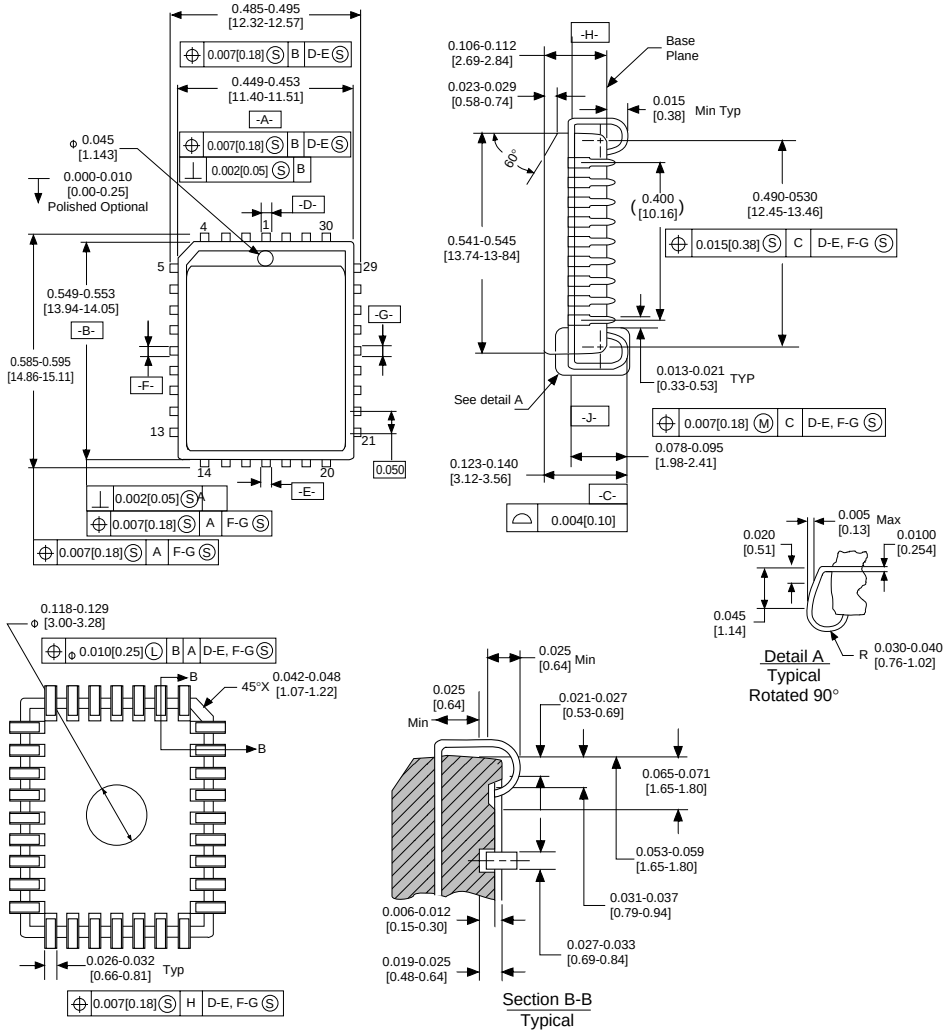


UV Window Cavity Dual-In-Line Cerdip Package (JQ)
Order Number NM27C512Q
Package Number J28CQ



28-Lead Plastic One-Time-Programmable Dual-In-Line
Order Number NM27C512N
Package Number N28B

Physical Dimensions inches (millimeters) unless otherwise noted



32-Lead Plastic Leaded Chip Carrier (PLCC)
Order Number NM27C512V
Package Number VA32A

Life Support Policy

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

July 1998

NM27C520
524,288-Bit (64K x 8) Multiplexed Addresses/Outputs OTP CMOS EPROM

General Description

The NM27C520 is a high performance 512K CMOS one-time programmable read only memory (EPROM) manufactured using Fairchild's proprietary CMOS AMG™ EPROM technology for an excellent combination of speed and economy while providing excellent reliability. It incorporates latches for the 8 lower order address bits to multiplex with the 8 data bits. This minimizes chip count, reduces cost, and simplifies the design of multiplexed bus systems.

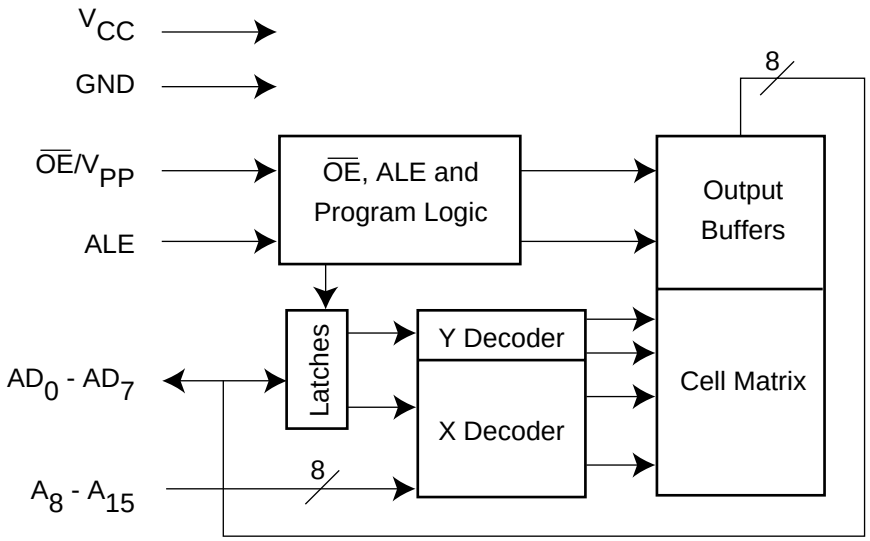
The NM27C520 provides microprocessor-based systems storage capacity for portions of operating system and application software. Its 90ns access time provides no wait-state operation with high-performance CPUs. The NM27C520 offers a single chip solution for the code storage requirements of 100% firmware-based equipment. Frequently-used software routines are quickly executed from EPROM storage, greatly enhancing system utility.

The NM27C520 is one member of a high density EPROM Family which range in densities up to 4 Megabit.

Features

- 8-Bit multiplexed Addresses/Outputs
- High performance CMOS —
  - 90 ns access time
- Fast turn-off for microprocessor compatibility
- Manufacturers identification code
- JEDEC Standard Pin Configuration
  - 20-Lead SOIC package

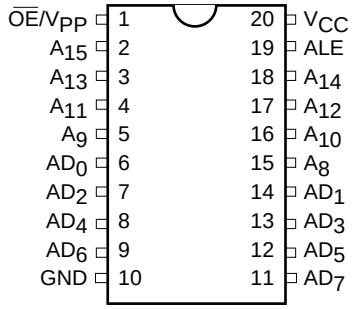
Block Diagram



DS800001-1

AMG™ is a trademark of WSI, Inc.

Connection Diagram



DS800001-2

SOIC Top View

Pin Names

	Addresses/Outputs
AD_0-AD_7	Address/Data
A_8-A_{15}	Address
ALE	Address Latch Enable
OE/V_{PP}	Output Enable

Commercial Temp. Range (0°C to + 70°C)

V_{CC} = 5V ± 10%

Parameter/Order Number	Access Time (ns) (Note 1)
NM27C520M 90	90

Industrial Temp. Range (-40°C to + 85°C)

V_{CC} = 5V ± 10%

Parameter/Order Number	Access Time (ns) (Note 1)
NM27C520ME 90	90

Note 1: All versions are guaranteed to function for slower speeds.

Package Type:

M=Wide Bodied SOIC

Absolute Maximum Ratings (Note 2)

Storage Temperature	-65°C to +150°C
All Input Voltage except A9 with Respect to Ground	-2.0V to +7V
V_{PP} and A9 with Respect to Ground	-2.0V to +14V
V_{CC} Supply Voltage with Respect to Ground	-0.6V to +7V
ESD Protection (MIL Std. 883, Method 3015.2)	>2000V
All Output Voltages with Respect to Ground	V_{CC} +1.0V to GND -0.6V

Operating Range

Range	Temperature	V_{CC}	Tolerance
Commercial	0°C to +70°C	+5V	±10%
Industrial	-40°C to +85°C	+5V	±10%

Read Operation

DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400µA	2.4		V
I_{CC}	V_{CC} Active Current	I_{OUT} = 0 mA, f = 5 MHz		20	mA
I_{CC2}	V_{CC} Standby Current	ALE = V_{IH}		2	mA
I_{PP}	V_{PP} Supply Current	V_{PP} = V_{CC}		10	µA
V_{PP}	V_{PP} Read Voltage		V_{CC} - 0.7	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or GND	-1	1	µA
I_{LI2}	Input Load Current A13	V_{IN} = 5.5V or GND	-100	100	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND	-5	5	µA

Read Operation

AC Electrical Characteristics

Symbol	Parameter	Min	Max	Units
t_{ACC}	Address to Output Delay		90	ns
t_{ALE}	Address Latch Enable Width	45		ns
t_{OE}	OE to Output Delay		35	ns
t_{DF}	Output Disable to Output Float		25	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, whichever Occurred First	0		ns
t_{AS}	Address Setup Time	15		ns
t_{AH}	Address Hold Time	15		ns

Capacitance T_A = +25°C, f = 1 MHz (Note 3)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

AC Test Conditions

Output Load 1 TTL Gate and CL = 100 pF (Note 9)

Input Rise and Fall Times ≤ 20 ns (10% to 90%)

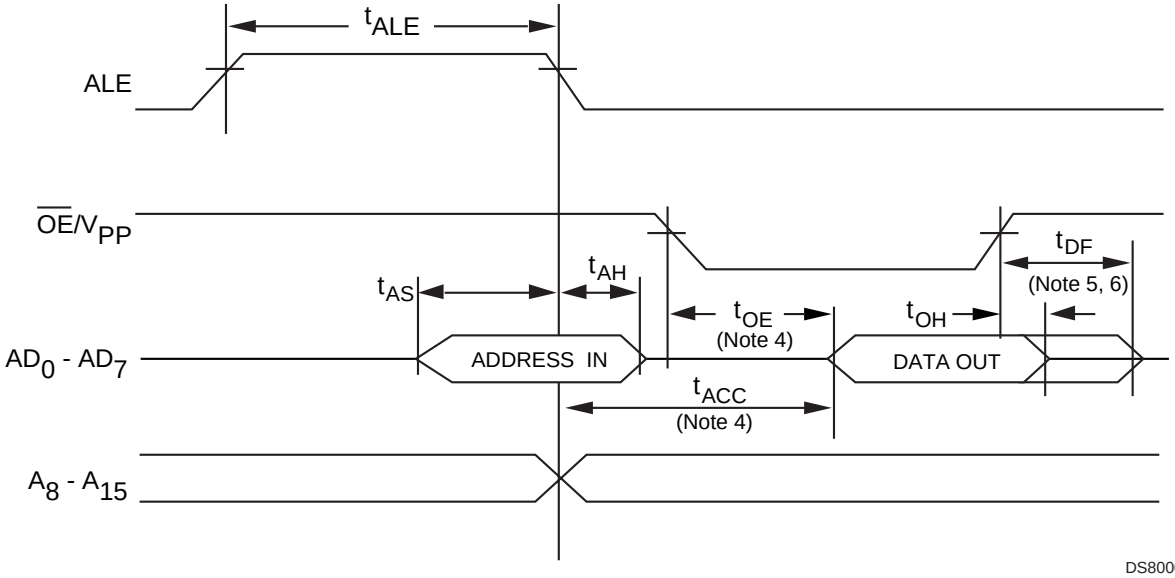
Input Pulse Levels 0.45V to 2.4V

Timing Measurement Reference Level (Note 9)

Inputs 0.8V and 2.0V

Outputs 0.8V and 2.0V

AC Waveforms for Read Operation (Notes 7 and 8)



DS800001-3

Note 2: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 3: This parameter is only sampled and is not 100% tested.

Note 4: $\overline{OE}$ may be delayed up to t_{ACC}- t_{OE} after the falling edge of ALE without impacting t_{ACC}.

Note 5: The t_{DF} and t_{CF} compare level is determined as follows:

High to TRI-STATE, the measured V_{OH1} (DC) -0.10V;

Low to TRI-STATE, the measured V_{OL1} (DC) +0.10V.

Note 6: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 7: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND.

Note 8: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 9: 1 TTL Gate: I_{OL} = 1.6 mA, I_{OH} = -400 µA.

C_L: 100 pF includes fixture capacitance.

Note 10: Inputs and outputs can undershoot to -2.0V for 20 ns Max.

DC Programming Characteristics (Notes 11 & 12)

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 2.5V$, $\overline{OE}/V_{PP} = 13.0 \pm 0.25V$ (Note 13)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Level		-0.6		0.8	V
V_{IH}	Input High Level		2.0		V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4			V
I_{CC}	V_{CC} Supply Current				25	mA
I_{CC2}	V_{CC} Standby Current	ALE = V_{IL}			2.5	mA
I_{PP}	$\overline{OE}/V_{PP}$ Current	ALE = V_{IH}			25	mA
I_{LI}	Input Load Current	$V_{IN} = V_{IL}$ or V_{IH}	-10		10	µA
I_{LI2}	Input Load Current A13	$V_{IN} = V_{IL}$ or V_{IH}	-100		100	µA

AC Programming Characteristics (Notes 11 & 12)

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 2.5V$, $\overline{OE}/V_{PP} = 13.0 \pm 0.25V$ (Note 13)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t_{ALE}	Address Latch Enable Width		500			ns
t_{LAS}	Latched Address Setup Time		100			ns
t_{LAH}	Latched Address Hold Time		100			ns
t_{AS}	Address Setup Time		2			µs
t_{AH}	Address Hold Time		2			µs
t_{DS}	Data Setup Time		2			µs
t_{DH}	Data Hold Time		2			µs
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time		2			µs
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time		2			µs
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time during Programming		50			ns
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time		2			µs
t_{PW}	Program Pulse Width		45	50	105	µs
t_{VCS}	V_{CC} Setup Time		2			µs
t_{LP}	ALE Low to $\overline{OE}/V_{PP}$ High Voltage Delay		2			µs
t_{OE}	Data Valid from $\overline{OE}/V_{PP}$			150		ns
t_{DFP}	$\overline{OE}/V_{PP}$ High to Output Float Delay (Note 14)		0	130		ns

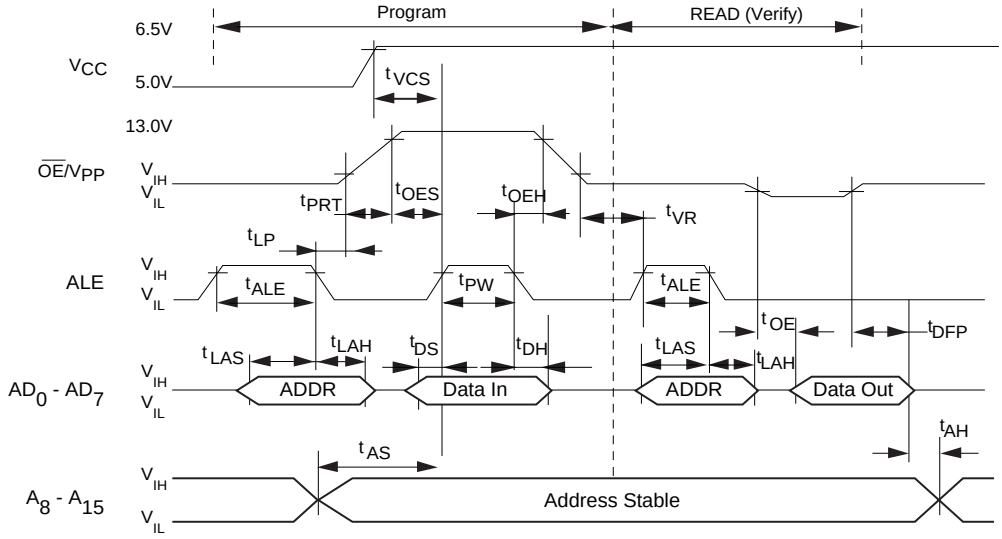
Note 11: Fairchild's standard product warranty applies only to devices programmed to specifications described herein.

Note 12: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 13: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 µF capacitor is required across V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 14: This parameter is not 100% tested. Output Float is defined as the point where data is no longer driven. See timing diagram (page 6).

Programming Waveforms

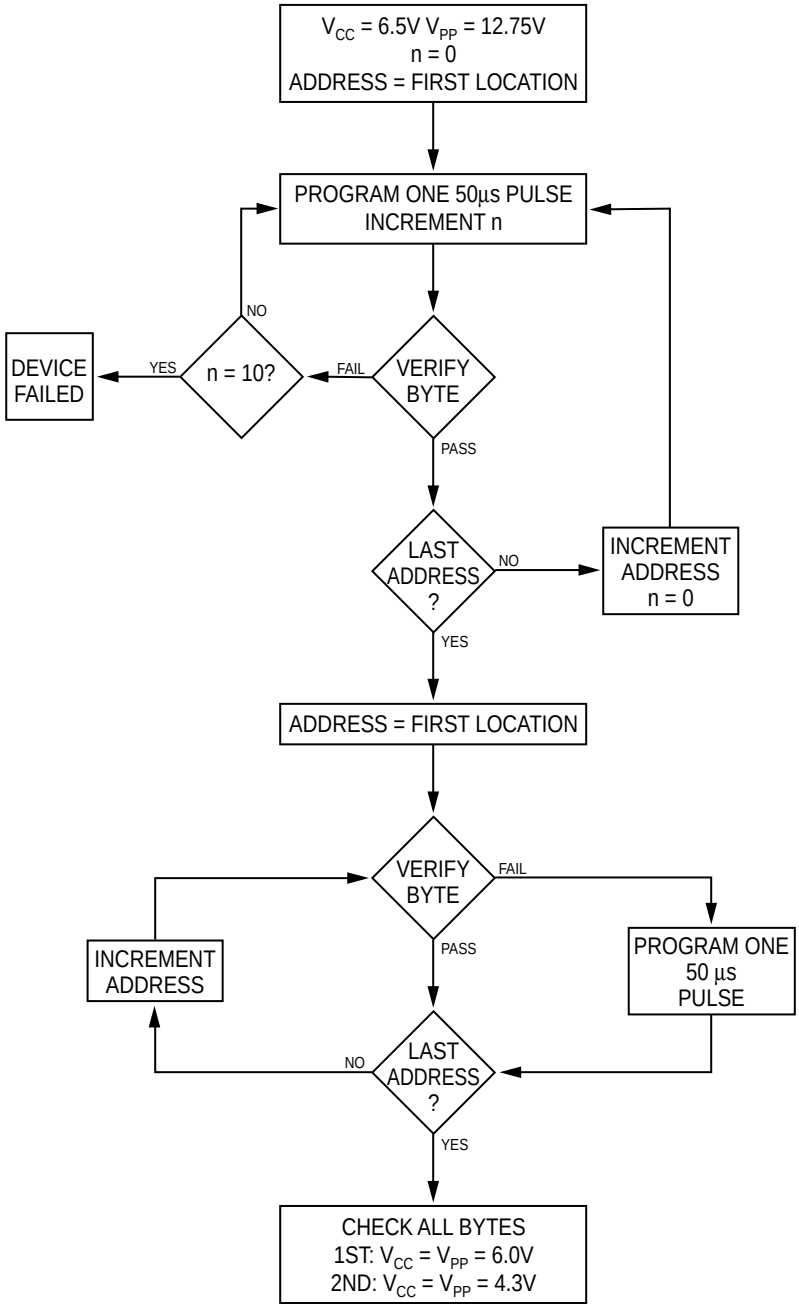


DS800001-4

Note 15: The input timing reference is 0.8V for V_{IL} and 2.0V for V_{IH}.

Note 16: t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

Turbo Programming Algorithm Flow Chart



DS800001-5

Figure 1

Functional Description

DEVICE OPERATION

The six modes of operation of the EPROM are listed in Table 1. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and $\overline{OE}/V_{PP}$. The $\overline{OE}/V_{PP}$ power supply must be at 12.75V during the two programming modes, and must be at 5V in the other four modes. The V_{CC} power must be at 6.5V during the two programming modes, and at 5V in the other four modes.

Read Mode

The NM27C520 has two control pins which are used to read data on the output pins. Address Latch Enable (ALE) is pulsed to read address pins AD_0 - AD_7. On the falling edge of this pulse, the data on these pins are latched into memory. When the address pins A_8 - A_{15} are stable and output enable ($\overline{OE}$) is low, the data contained in the desired address location is gated to pins AD_0 - AD_7. Address access time (t_{ACC}) is either the time delay from address latch enable, or the time delay from when the address pins A_8 - A_{15} are stable, which ever happens last. Output Enable ($\overline{OE}/V_{PP}$) is the output control and should be used to drive data to the output pins.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 90%, from 110mW to less than 11mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the ALE input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the $\overline{OE}$ input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Typing

Because the EPROM is usually used in larger memory arrays, Fairchild has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

1. the lowest possible memory power dissipation, and
2. complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that ALE be decoded and used as the primary device selecting function, while $\overline{OE}/V_{PP}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus.

This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 ($\overline{OE}/V_{PP}$) will damage the EPROM.

Initially, all bits of the EPROM are in the “1’s” state. Data is introduced by selectively programming “0’s” into the desired bit locations. Although only "0’s" will be programmed, both “1’s” and “0’s” can be presented in the data word. It is not possible to change a “0” to a “1”.

The EPROM is in the programming mode when the $\overline{OE}/V_{PP}$ power supply is at 12.75V. It is required that at least a 0.1 µF capacitor be placed across V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Programming mode can be accomplished after a TTL high pulse is applied to the ALE input latching in the addresses AD_0 - AD_7 by its falling edge. Once addresses A_8 - A_{15} are stable, the $\overline{OE}/V_{PP}$ power supply is set to 12.75V and a TTL high pulse is again applied to the ALE input. In order to program the entire memory array, a program pulse must be applied at each address location in this same manner.

The EPROM is programmed with the Turbo Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 50 µs pulses until it verifies good, up to a maximum of 10 pulses. Most memory cells will program with a single 50 µs pulse.

The EPROM must not be programmed with a DC signal applied to the ALE input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A high level TTL pulse applied to the ALE input programs the paralleled EPROM.

Program Inhibit

Programming multiple EPROM's in parallel with different data is also easily accomplished. Except for ALE all like inputs (including $\overline{OE}/V_{PP}$) of the parallel EPROM may be common. A TTL high level program pulse applied to an EPROM’s ALE input with $\overline{OE}/V_{PP}$ at 12.75V will program that EPROM. A TTL low level ALE input inhibits the other EPROMs from being programmed.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer’s identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer’s Identification code, shown in Table 2, specifically identifies the manufacture and device type. The code for NM27C520 is '8F9D', where '8F' designates that it is made by Fairchild Semiconductor, and '9D' designates the 520 part.

The code is accessed by applying 12V ± 0.5V to address pin A_9. Addresses AD_1 - A_8, A_{10}-A_{16}, and all control pins are held at V_{IL}.

Address pin A_8 is held at V_{IL} for the manufacturer’s code, and held at V_{IH} for the device code. The code is read on the eight data pins, AD_0- AD_7. Proper code access is only guaranteed at 25°C ± 5°C.

Mode Selection

The modes of operation of the NM27C520 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A_9 for device signature.

Table 1. Mode Selection

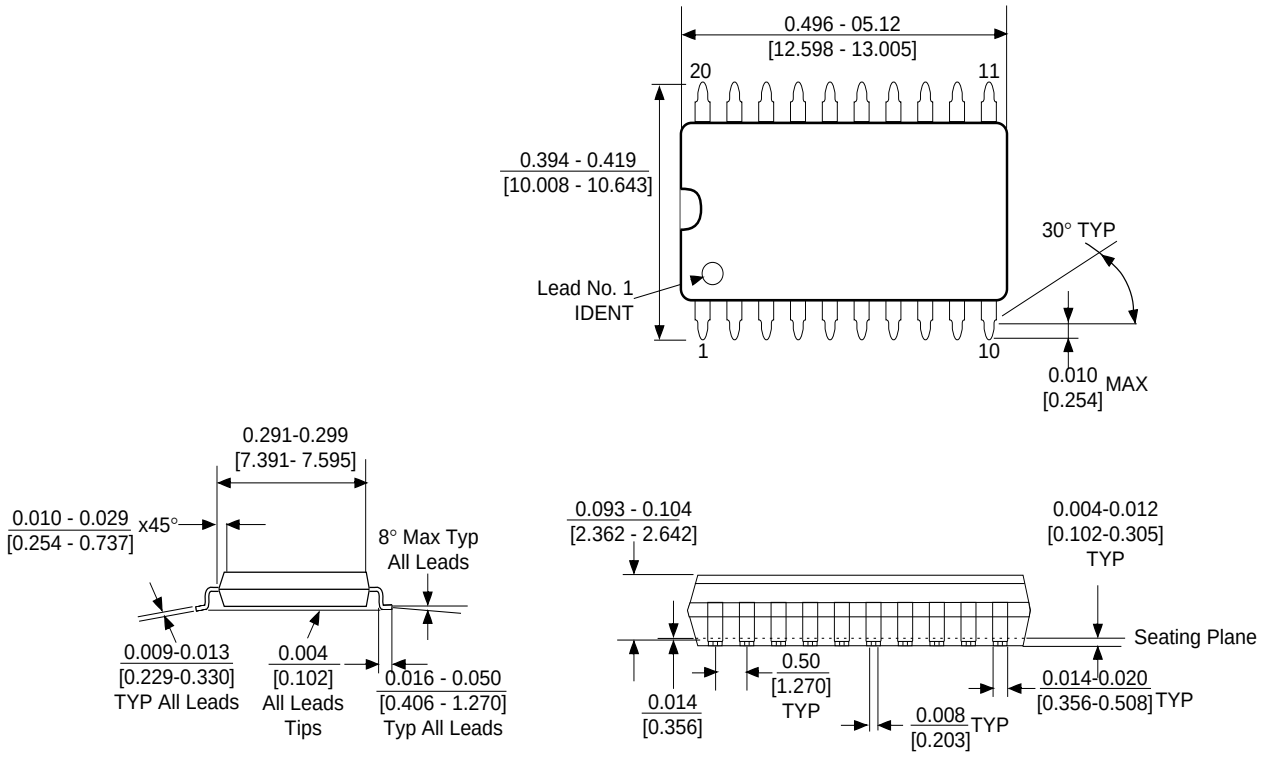
Mode \ Pins	ALE	$\overline{OE}/V_{PP}$	A_8 - A_{15}	AD_0 - AD_7
Read	V_{IL}	V_{IL}	A_{IN}	D_{OUT}
Output Disable	V_{IL}/V_{IH}	V_{IH}	A_{IN}	High Z/A_{IN}
Standby	V_{IH}	X	A_{IN}	A_{IN}
Address Latch Enable	⎺_	V_{IH}	A_{IN}	A_{IN}
Programming	V_{IH}	12.75V	A_{IN}	D_{IN}
Program Inhibit	V_{IL}	12.75V	A_{IN}	High Z

Note 17: ⎺_ = High to Low Transition, A_{IN} = Address In, D_{OUT} = Data Out, D_{IN} = Data In

Table 2. Manufacturer's Identification Code

Mode \ Pins	A_9	A_8	AD_7	AD_6	AD_5	AD_4	AD_3	AD_2	AD_1	AD_0	Hex Data
Manufacturer Code	V_{PP}	0	1	0	0	0	1	1	1	1	8F
Device Code	V_{PP}	1	1	0	0	1	1	1	0	1	9D

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead (0.300" Wide) Molded Small Outline Package, JEDEC
Order Number NM27C520
Package Number M20B

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

July 1998

NM27LV010
1,048,576-Bit (128k x 8) Low Voltage EPROM

General Description

The NM27LV010 is a high performance Low Voltage Electrically Programmable Read Only Memory. It is manufactured using Fairchild's AMG™ EPROM technology. This technology allows the part to operate at speeds as fast as 200 ns.

This Low Voltage and Low Power EPROM is designed with power sensitive hand held and portable battery products in mind. This allows for code storage of firmware for applications like notebook computers, palm top computers, cellular phones, and HDD.

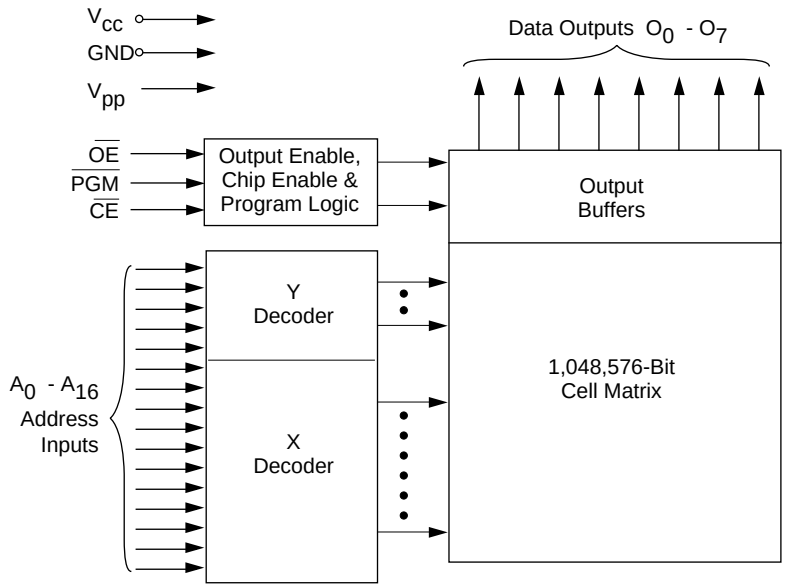
Small outline packages are just as critical to portable applications as Low Voltage and Low Power.

The NM27LV010 is one member of Fairchild's growing Low Voltage product Family.

Features

- 3.0V to 3.6V operation
- 200 ns access time
- Low current operation
  - —8 mA I_{CC} active current @ 5 MHz (typ.)
  - —20µA I_{CC} standby current @ 5 MHz (typ.)
- Ultra low power operation
  - —66 µW standby power @ 3.3V
  - —50 mW active power @ 3.3V
- Surface mount package options|
  - —32-pin TSOP
  - —32-pin PLCC

Block Diagram



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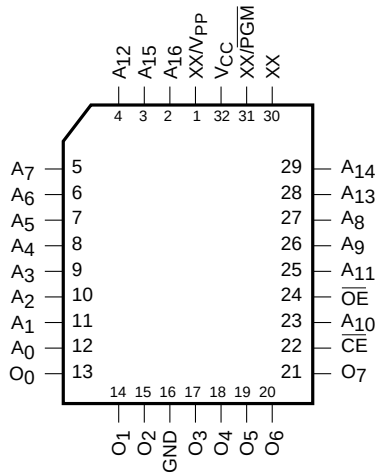
Connection Diagrams

PLCC Pin Configuration



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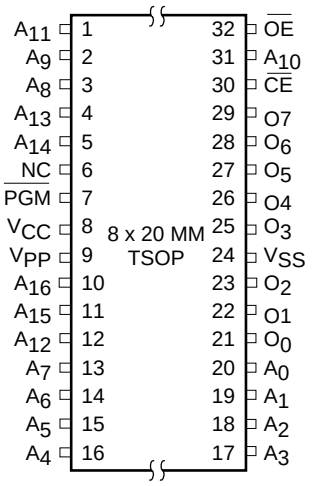
Top View

TSOP Pin Configuration



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Top View

Commercial Temperature Range (0°C to +70°C) V_{CC} = 3.3 ± 0.3

Parameter/Order Number	Access Time (ns)
NM27LV010 V, T 200	200
NM27LV010 V, T 250	250

Pin Names

A0–A16	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)
V_{PP}	Programming Voltage

Industrial Temperature Range (-40°C to +85°C) V_{CC} = 3.3 ± 0.3

Parameter/Order Number	Access Time (ns)
NM27LV010 VE, TE	200
NM27LV010 VE, TE	250

Package Types: NM27LV010 V, T

V = PLCC

T = TSOP

- All packages conform to the JEDEC standard.
- All versions are guaranteed to function for slower speeds.
- Consult the Fairchild Sales office on new released products and packages.
- Consult the Fairchild representative for custom products for your specific application.

Absolute Maximum Ratings (Note 1)

Storage Temperature	-65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	-0.6V to +7V
V_{PP} and A9 with Respect to Ground	-0.6V to +14V
V_{CC} Supply Voltage with Respect to Ground	-0.6V to +7V
ESD Protection	>2000V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} + 1.0V to GND - 0.6V

Operating Range

Range	Temperature	V_{CC}	Tolerance
Commercial	0°C to +70°C	3.3V	±0.3V
Industrial	-40°C to +85°C	3.3V	±0.3V

DC Electrical Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IL}	Input Low Level		-0.3	0.7	V
V_{IH}	Input High Level		2.0	V_{CC} + 0.3	V
V_{OL1}	Output Low Voltage (TTL)	I_{OL} = 2.0 mA		0.4	V
V_{OH1}	Output High Voltage (TTL)	I_{OH} = -2.0 mA	2.4		V
V_{OL2}	Output Low Voltage	I_{OL} = 100 µA		0.2	V
V_{OH2}	Output High Voltage (CMOS)	I_{OH} = -100 µA	V_{CC} - 0.3		
I_{SB1}	V_{CC} Standby Current (CMOS)	$\overline{CE} = V_{CC} \pm 0.3V$		50	µA
I_{SB2}	V_{CC} Standby Current (TTL)	$\overline{CE} = V_{IH}$		100	µA
I_{CC}	V_{CC} Active Current	$\overline{CE} = \overline{OE} = V_{IL}$, f = 5 MHz I/O = 0 µA		15	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$		10	µA
V_{PP}	V_{PP} Read Voltage		V_{CC} - 0.7	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 3.0V or GND		1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 3.0V or GND	-1	10	µA

AC Electrical Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	200		250		Units
		Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay		200		250	
t_{OE}	$\overline{OE}$ to Output Delay		70		75	
t_{DF} (Note 2)	Output Disable to Output Float		50		50	
t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		

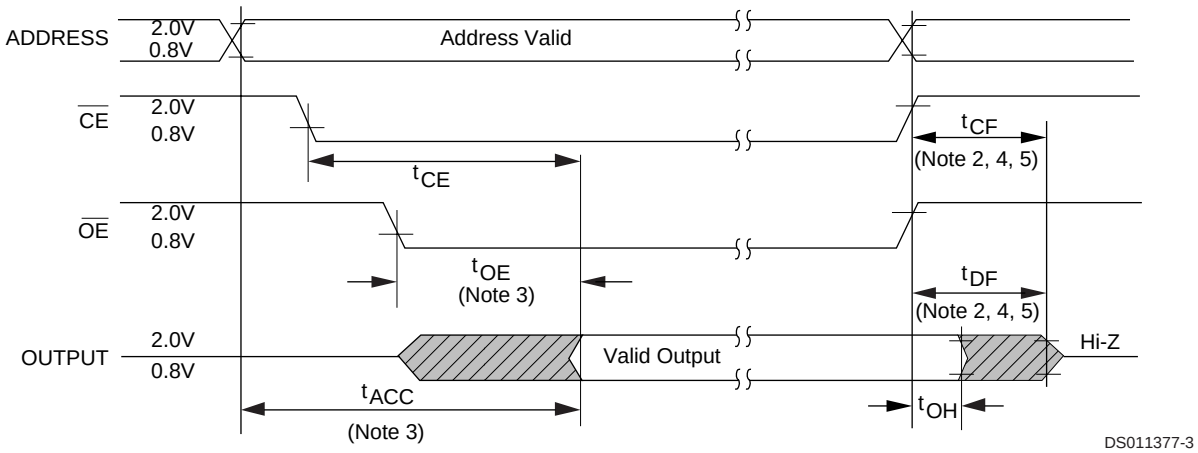
Capacitance (Note 2) T_A = +25°C, 1 = 1 MHz

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	9	15	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	15	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Note 6) , (Note 7) , and (Note 9)



Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operations sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE®, the measured V_{OH1} (DC) - 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.2 µF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: I_{OL} = 1.6 mA, I_{OH} = -400 µA.
C_L: 100pF includes fixture capacitance.

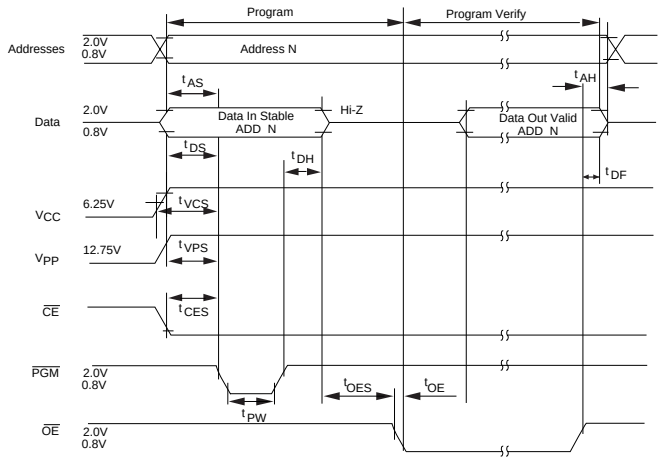
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to -2.0V for 20 ns Max.

Programming Characteristics (Note 11), (Note 12), (Note 13) and (Note 14)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			µs
t_{OES}	$\overline{OE}$ Setup Time		1			µs
t_{CES}	$\overline{CE}$ Setup Time		1			µs
t_{DS}	Data Setup Time		1			µs
t_{VPS}	V_{PP} Setup Time		1			µs
t_{VCS}	V_{CC} Setup Time		1			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		1			µs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE}/\overline{PGM} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		45	50	105	µs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE}/\overline{PGM} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE}/\overline{PGM} = V_{IL}$			20	mA
I_{CC}	V_{CC} Supply Current				20	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.25	6.5	6.75	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

Programming Waveform (Note 13)



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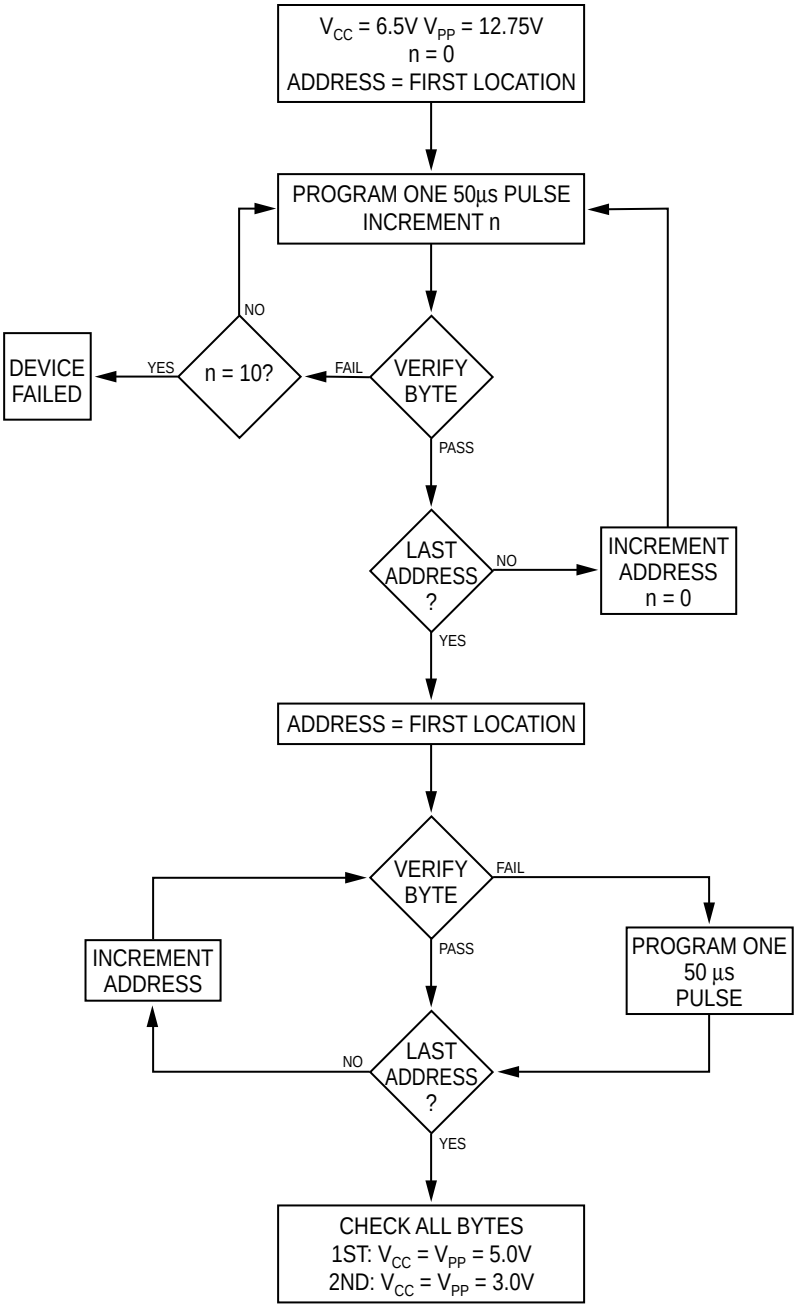
Note 11: Fairchild's standard product warranty applies to devices programmed to specifications described herein.

Note 12: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removedfrom a board with voltage applied to V_{PP} or V_{CC}.

Note 13: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 µF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 14: During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

LV Turbo Programming Algorithm Flow Chart



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Note: The standard National Semiconductor algorithm may also be used but it will have longer programming time.

FIGURE 1.

Functional Description

DEVICE OPERATION

The six modes of operation of the EPROM are listed in Table 1. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 3.3V in the other three modes. The V_{CC} power supply must be at 6.5V during the three programming modes, and at 3.3V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from 50 mW to 0.17 mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the $\overline{OE}$ input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Tying

Because the EPROM is usually used in larger memory arrays, Fairchild has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

1. the lowest possible memory power dissipation, and
2. complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 µF capacitor be placed across V_{PP} and V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the LV Turbo Programming Algorithm shown in Figure 1. Each Address is programmed with a series of 50 µs pulses until it verifies good, up to a maximum of 10 pulses. Most memory cells will program with a single 50 µs pulse. (The standard National Semiconductor Algorithm may also be used, but it will have longer programming time.)

The EPROM must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled EPROM.

Program Inhibit

Programming multiple EPROM's in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel EPROM may be common. A TTL low level program pulse applied to an EPROM's $\overline{PGM}$ input with $\overline{CE}$ at V_{IL} and V_{PP} at 12.75V will program that EPROM. A TTL high level $\overline{CE}$ input inhibits the other EPROM's from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 6.25V. V_{PP} must be at V_{CC}, except during programming and program verify.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table 2, specifically identifies the manufacturer and device type. The code for the NM27LV010 is "8F86", where "8F" designates that it is made by Fairchild Semiconductor, and "86" designates a 1 Megabit (128k x 8) part.

The code is accessed by applying 12V ±0.5V to address pin A9. Addresses A1–A8, A10–A16, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the lower eight data pins, O0–07. Proper code access is only guaranteed at 25°C ± 5°C.

Functional Description (Continued)

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å – 4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 30W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increases as the square of the distance from the lamp (if distance is doubled the erasure time increases by factor of 4). Lamps lose intensity as they age. When a lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

Mode Selection

The modes of operation of the NM27LV010 are listed in Table 1. A single 3.3V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 for device signature.

TABLE 1. Modes Selection

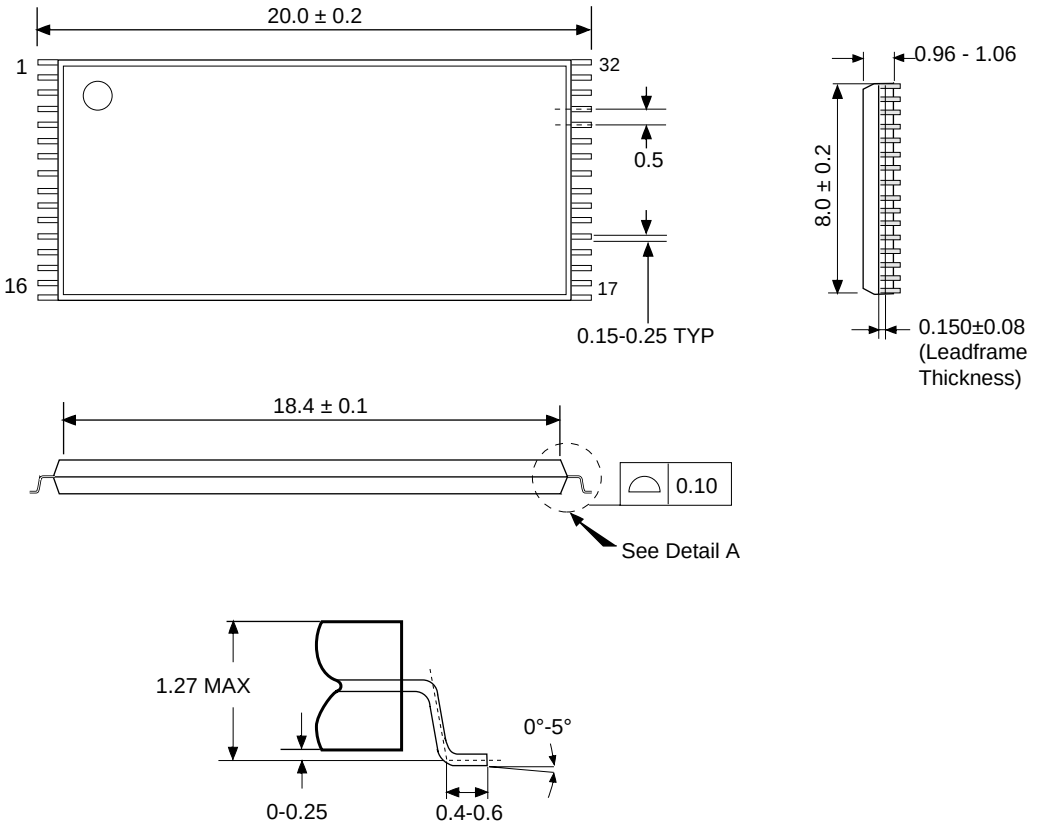
Mode \ Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X	V_{CC}	3.3V	D_{OUT}
Output Disable	X (Note 15)	V_{IH}	X	V_{CC}	3.3V	High Z
Standby	V_{IH}	X	X	V_{CC}	3.3V	High Z
Programming	V_{IL}	V_{IH}	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	12.75V	12.75V	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	X	12.75V	6.25V	High Z

Note 15: X can be V_{IL} or V_{IH} .

TABLE 2. Manufacturer's Identification Code

Pins	A0 (12)	A9 (26)	O7 (21)	O6 (20)	O5 (19)	O4 (18)	O3 (17)	O2 (15)	O1 (14)	O0 (13)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	1	0	0	0	0	1	1	0	86

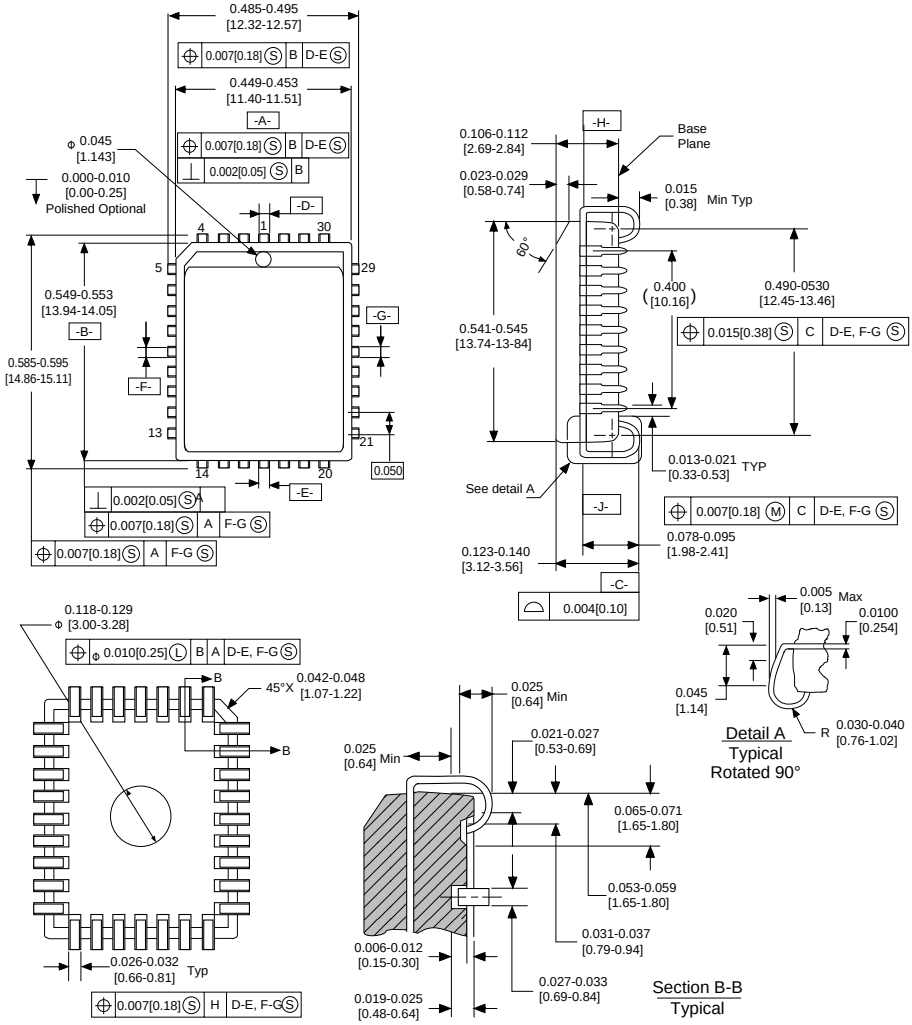
Physical Dimensions inches (millimeters) unless otherwise noted



DETAIL A
Typical

32-Lead TSOP Package (T)
Order Number NM27LV010TXXX
Package Number MBH32A

Physical Dimensions inches (millimeters) unless otherwise noted



32-Lead PLCC Package
Order Number NM27LV010VXXX
Package Number VA32A

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

July 1998

NM27LV010B
1,048,576-Bit (128k x 8) Low Voltage EPROM

General Description

The NM27LV010B is a high performance Low Voltage Electrically Programmable Read Only Memory. It is manufactured using Fairchild's split gate AMG™ EPROM technology. This technology allows the part to operate at speeds as fast as 250 ns over industrial temperatures (-40°C to +85°C).

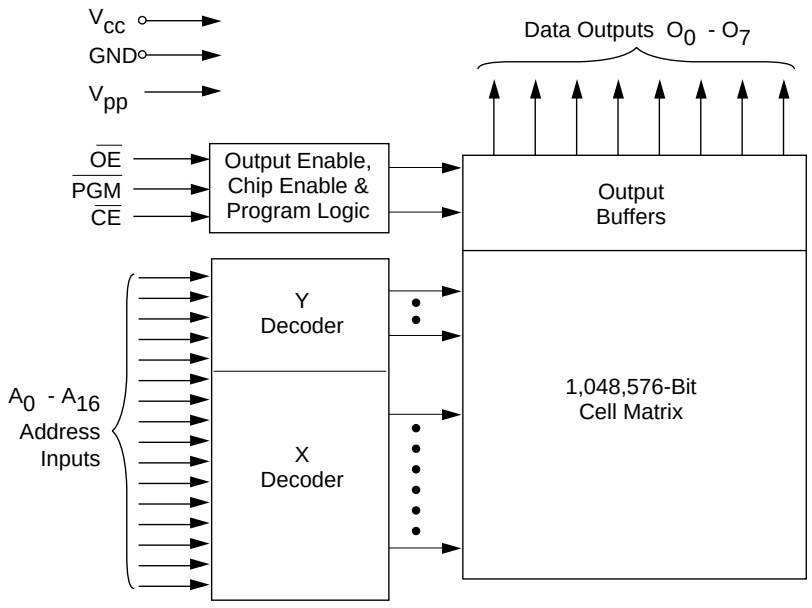
This Low Voltage and Low Power EPROM is designed with power sensitive hand held and portable battery products in mind. This allows for code storage of firmware for applications like notebook computers, palm top computers, cellular phones, and HDD.

The NM27LV010B is one member of Fairchild's growing Low Voltage product family.

Features

- 2.7V to 3.3V operation
- 200 ns access time
- Low current operation
  - —8 mA I_{CC} Active Current @ 5 MHz (Typ)
  - —15μA I_{CC} Standby Current @ 5 MHz (Typ)
- Ultra low power operation
  - —50 μW Standby Power @ 3.3V (Typ)
  - —27 mW Active Power @ 3.3V (Typ)
- 32-pin TSOP Package

Block Diagram



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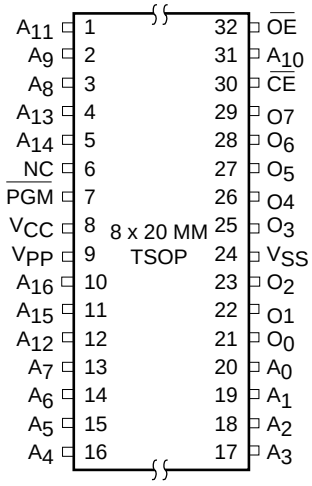
Connection Diagrams

TSOP Pin Configuration



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Top View

Commercial Temperature Range (0°C to +70°C) V_{CC} = 2.7V-3.6V

Parameter/Order Number	Access Time (ns)
NM27LV010BT 200	200
NM27LV010BT 250	250

Pin Names

A0–A16	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)
V_{PP}	Programming Voltage

Industrial Temperature Range (-40°C to +85°C) V_{CC} = 2.7V–3.6V

Parameter/Order Number	Access Time (ns)
NM27LV010BTE	250

Package Type: NM27LV010B T

T = TSOP Package

- All packages conform to JEDEC standard.
- All versions are guaranteed to function at slower speeds.
- Consult your Fairchild Semiconductor sales office for new released products and packages.
- Consult your Fairchild Semiconductor representative for custom products for your specific application.

Absolute Maximum Ratings (Note 1)

Storage Temperature -65°C to +150°C

All Input Voltage except A9 with Respect to Ground -0.6V to +7V

V_{PP} and A9 with Respect to Ground -0.7V to +14V

V_{CC} Supply Voltage with Respect to Ground -0.6V to +7V

ESD Protection >2000V

All Output Voltages with Respect to Ground (Note 10) V_{CC} + 1.0V to GND - 0.6V

Operating Range

Range	Temperature	V_{CC}	Tolerance
Commercial	0°C to +70°C	2.7V–3.3V	
Industrial	-40°C to +85°C	2.7V–3.3V	

DC Read Characteristics (Over Operating Range with $V_{PP} = V_{CC}$)

Symbol	Parameter	Conditions	Min	Max	Units
V_{IL}	Input Low Level		-0.3	0.6	V
V_{IH}	Input High Level		2.0	V_{CC} + 0.3	V
V_{OL1}	Output Low Voltage (TTL)	I_{OL} = 2.1 mA		0.4	V
V_{OH1}	Output High Voltage (TTL)	I_{OH} = -400 µA	2.2		V
V_{OL2}	Output Low Voltage	I_{OL} = 100 µA		0.2	V
V_{OH2}	Output High Voltage (CMOS)	I_{OH} = 100 µA	V_{CC} - 0.3		V
I_{SB1}	V_{CC} Standby Current (CMOS)	$\overline{CE}$ = 2.7V–3.6V		50	µA
I_{SB2}	V_{CC} Standby Current (TTL)	$\overline{CE} = V_{IH}$		100	µA
I_{CC}	V_{CC} Active Current	$\overline{CE} = \overline{OE} = V_{IL}$, I/O = 0 µA; f = 5 MHz		15	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$		10	µA
I_{LI}	Input Load Current	V_{IN} = 3.0V or GND		1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 3.3V or GND	-1	10	µA

AC Read Characteristics (Over Operating Range with $V_{PP} = V_{CC}$)

Symbol	Parameter	200		250		Units
		Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay		70		75	ns
t_{DF}	Output Disable to Output Float (Note 2)		50		50	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First (Note 2)	0		0		ns

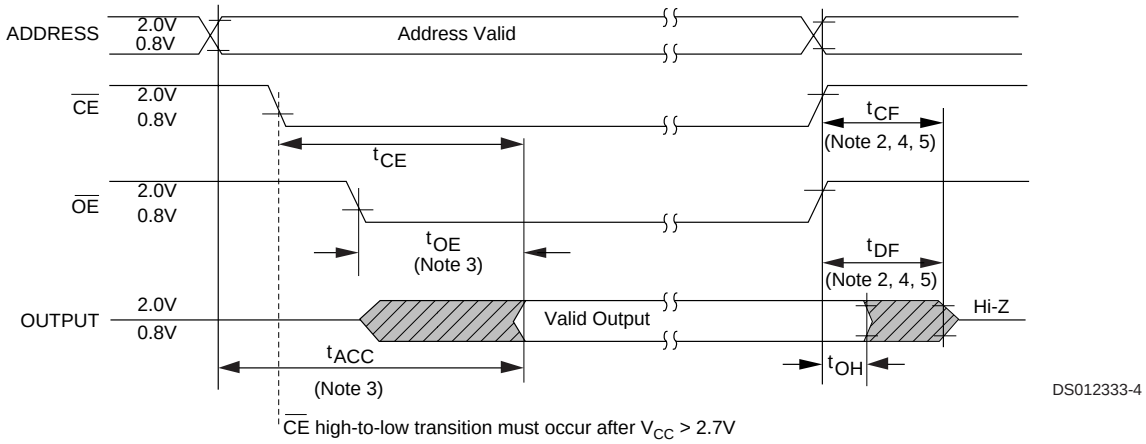
Capacitance T_A = +25°C, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN1}	Input Capacitance	V_{IN} = 0V	9	15	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	15	pF

AC Test Conditions

Output Load:	1 TTL Gate and C_L = 100 pF (Note 8)
Input Rise and Fall Times:	≤5 ns
Input Pulse Levels:	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs:	0.8V and 2V
Outputs:	0.8V and 2V

AC Waveforms (Note 6) (Note 7) (Note 9)



$\overline{CE}$ high-to-low transition must occur after V_{CC} > 2.7V

*After power-up (stable V_{CC}), a high-to-low transition of $\overline{CE}$ is required before the first byte of data is read.

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows: High to TRI-STATE®, the measured V_{OH1} (DC) - 0.10V; Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: I_{OL} = 1.6 mA, I_{OH} = -400 µA. C_L: 100 pF includes fixture capacitance.

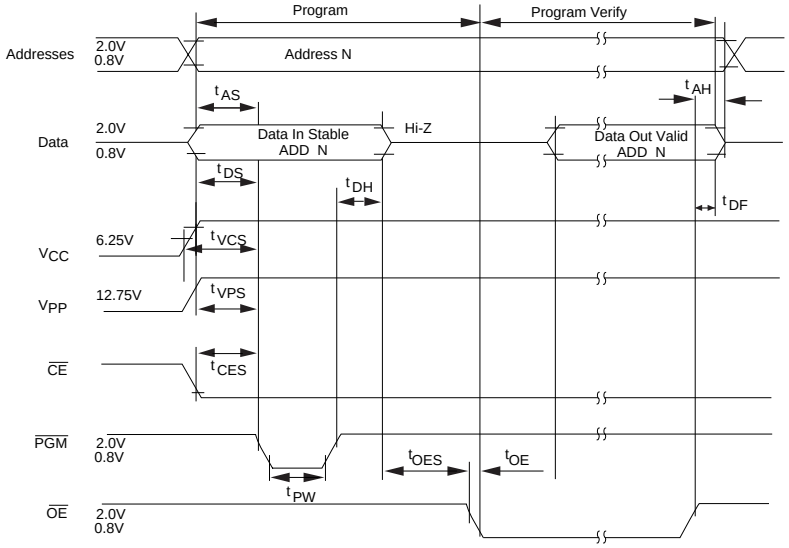
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to -2.0V for 20 ns max.

Programming Characteristics (Note 11) (Note 12) (Note 13) (Note 14)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			µs
t_{OES}	$\overline{OE}$ Setup Time		1			µs
t_{CES}	$\overline{CE}$ Setup Time		1			
t_{DS}	Data Setup Time		1			µs
t_{VPS}	V_{PP} Setup Time		1			
t_{VCS}	V_{CC} Setup Time		1			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		1			µs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE}/\overline{PGM} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		45	50	55	µs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE}/\overline{PGM} = V_{IL}$			100	µs
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE}/\overline{PGM} = V_{IL}$			20	mA
I_{CC}	V_{CC} Supply Current			20	mA	
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.25	6.5	6.75	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0	0.45	V
V_{IH}	Input High Voltage		2.4	4		V
t_{IN}	Input Timing Reference Voltage		0.8		2	V
t_{OUT}	Output Timing Reference Voltage		0.8		2	V

Programming Waveform (Note 13)



DS012333-5

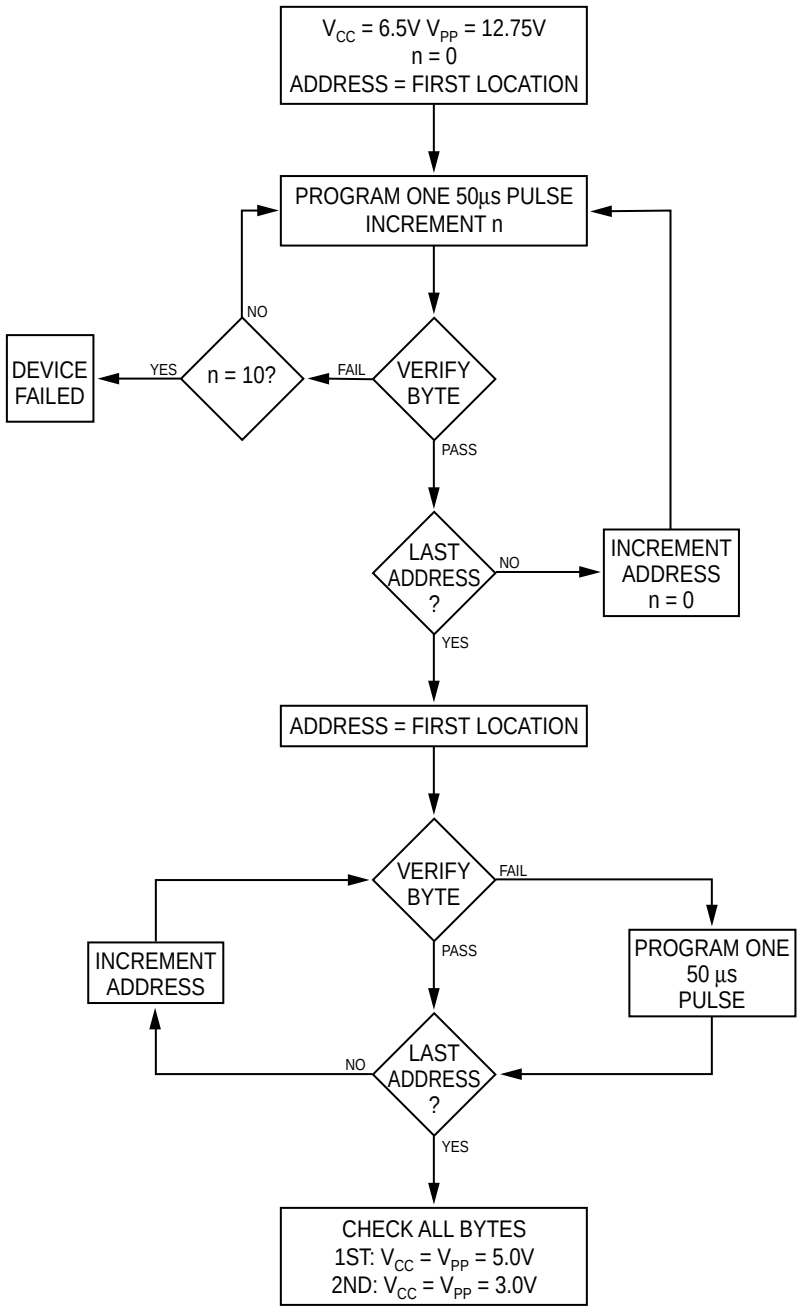
Note 11: Fairchild's standard product warranty applies only to devices programmed to specifications described herein.

Note 12: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 13: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 µF capacitor is required across V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 14: During power up, the $\overline{PGM}$ pin must be brought high (V_{IH}) either coincident with or before power is applied to V_{PP}.

LV Turbo Programming Algorithm Flow Chart



DS012333-6

Note: The standard National Semiconductor algorithm may also be used but it will have longer programming time.

FIGURE 1.

Functional Description

DEVICE OPERATION

The six modes of operation of the EPROM are listed in Table 1. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 3.3V in the other three modes. The V_{CC} power must be at 6.5V during the three programming modes, and at 3.3V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from 45 mW to 0.15 mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the $\overline{OE}$ input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Tying

Because the EPROM is usually used in larger memory arrays, Fairchild has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

1. the lowest possible memory power dissipation, and
2. complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all selected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 22 (V_{PP}) will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the V_{PP} power supply is at 12.75V and OE is at V_{IH}. It is required that at least a 0.1 µF capacitor be placed across V_{CC} to GND to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the LV Turbo Programming Algorithm shown in Figure 1. Each address is programmed with a series of 50 µs pulses until it verifies good, up to a maximum of 10 pulses. Most memory cells will program with a single 50 µs pulse. (The standard National Semiconductor Algorithm may also be used, but it will have longer programming time.)

The EPROM must not be programmed with a DC signal applied to the PGM input.

Programming multiple EPROMs in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the PGM input programs the paralleled EPROM.

Program Inhibit

Programming multiple EPROMs in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$ and PGM) of the parallel EPROM may be common. A TLL low level program pulse applied to an EPROM's $\overline{PGM}$ input with $\overline{CE}$ at V_{IL} and V_{PP} at 12.75V will program that EPROM. A TTL high level $\overline{CE}$ input inhibits the other EPROMs from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 6.25V. V_{PP} must be at V_{CC} except during programming and program verify.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The manufacturer's identification code, shown in Table 2, specifically identifies the manufacture and device type. The code for NM27LV010B is "8F86", where "8F" designates that it is made by Fairchild Semiconductor, and "86" designates a 1 Mbit (128k x 8) part.

The code is accessed by applying 12V ± 0.5V to address pin A9. Addresses A1–A8, A10–A16 and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code and held at V_{IH} for the device code. The code is read on the eight data pins, O0–O7. Proper code access is only guaranteed at 25°C ± 5°C.

Functional Description (Continued)

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å – 4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 30 Wsec/cm^2.

The EPROM should be placed within one inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increases at the square of the distance from the lamp (if distance is doubled the erasure time increases by factor of four). Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

Mode Selection

The modes of operation of the NM27LV010B are listed below. All inputs are TTL levels except for V_{PP} and A9 for device signature.

Modes Selection

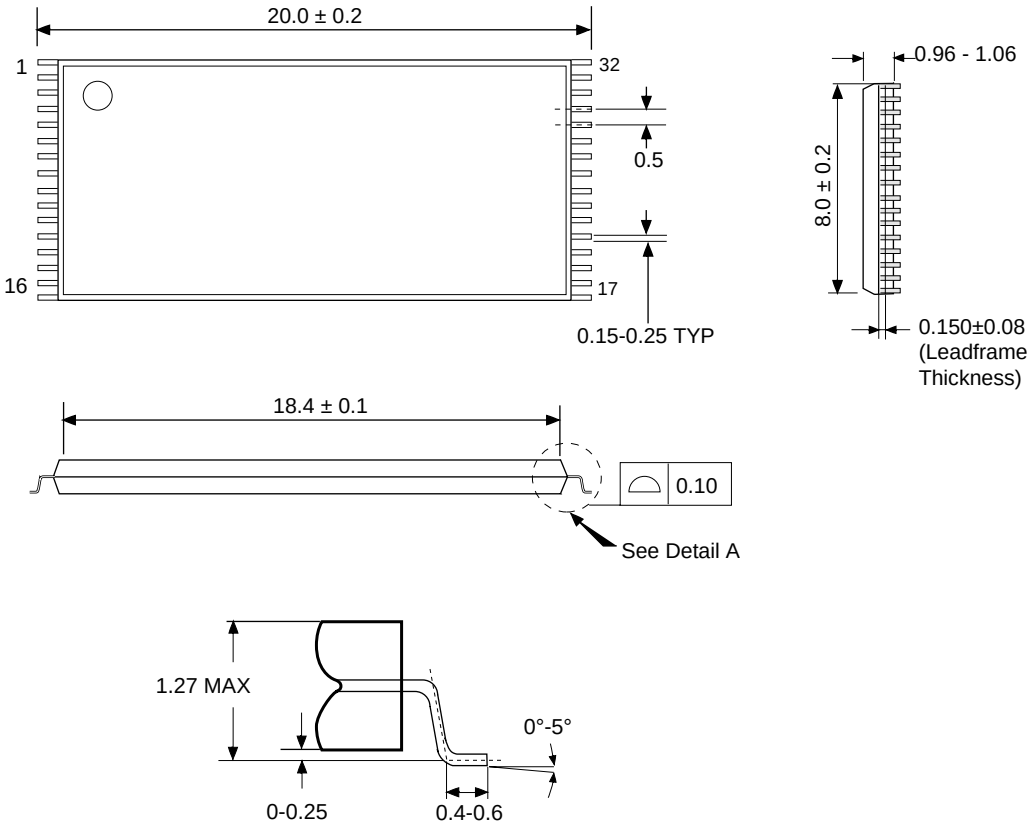
Mode \ Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X	V_{CC}	3.3V	D_{OUT}
Output Disable	X	V_{IH}	X	V_{CC}	3.3V	High Z
Standby	V_{IH}	X	X	V_{CC}	3.3V	High Z
Programming	V_{IL}	V_{IH}	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	12.75V	12.75V	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	X	12.75V	6.25V	High Z

X can be V_{IL} or V_{IH}

Manufacturer's Identification Code

Pins	A0 (12)	A9 (26)	O7 (21)	O6 (20)	O5 (19)	O4 (18)	O3 (17)	O2 (15)	O1 (14)	O0 (13)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	1	0	0	0	0	1	1	0	86

Physical Dimensions inches (millimeters) unless otherwise noted



DETAIL A
Typical

32-Lead TSOP Package (T)
Order Number NM27LV010BTXXX
Package Number MBH32A

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

July 1998

NM27LV210
1,048,576-Bit (64K x 16) Low Voltage EPROM

General Description

The NM27LV210 is a high performance Low Voltage Electrical Programmable read only memory. It is manufactured using Fairchild's latest EPROM technology. This technology allows the part to operate at high speeds.

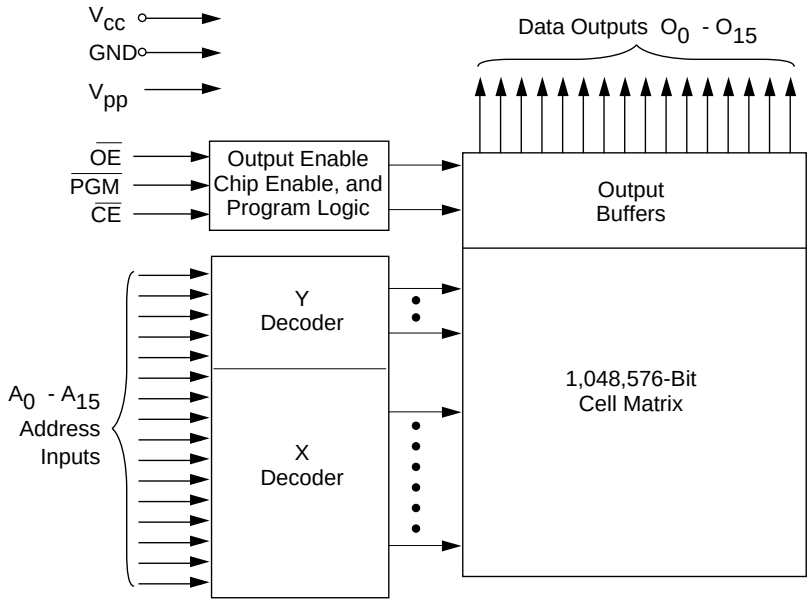
This Low Voltage and Low Power EPROM is designed with power sensitive hand held and portable battery products in mind. This allows for code storage of firmware for applications like notebook computers, palm top computers, cellular phones, and HDD.

The NM27LV210 is one member of Fairchild's growing Low Voltage product family.

Features

- 3.0V to 3.6V operation
- 200 ns, 250 ns maximum access time
- Low current operation
  - —20mA I_{CC} active current @ 5 MHz
  - —50µA I_{CC} standby current @ 5 MHz
- Ultra low power operation
  - —60 µA standby power @ 3.3V
  - —50 mW active power @ 3.3V
- Surface mount package option
  - —44-Pin PLCC

Block Diagram



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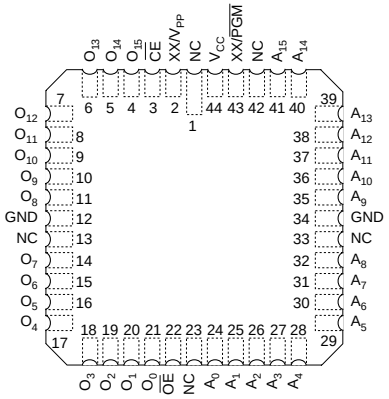
Connection Diagrams

PLCC Pin Configuration



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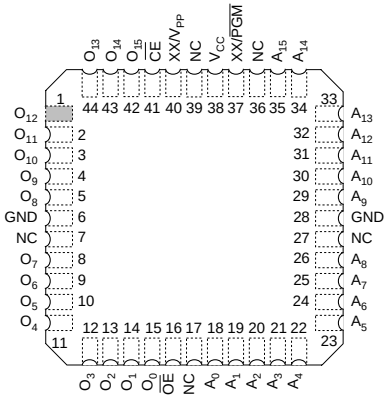
Top View



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Commercial Temperature Range

(0°C to +70°C) V_{CC} = 3.3V ± 0.3

Parameter/Order Number	Access Time (ns)
NM27LV210 V 200	200
NM27LV210 V 250	250

Pin Names

A0–A15	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O15	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)
NC	No Connect
V_{PP}	Programming Voltage

Extended Temperature Range

(-40°C to +85°C) V_{CC} = 3.3V ±0.3

Parameter/Order Number	Access Time (ns)
NM27LV210 VE 250	250

- All packages conform to JEDEC standard.
- All versions are guaranteed to function in slower applications.
- Consult the FSC representative for newly released products/ packages.

Absolute Maximum Ratings (Note 2)

Storage Temperature	-65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 12)	-0.6V to +7V
V_{PP} and A9 with Respect to Ground	-0.6V to +14V
V_{CC} Supply Voltage with Respect to Ground	-0.6V to +7V
ESD Protection	>2000V
All Output Voltages with Respect to Ground (Note 11)	V_{CC} + 1.0V to GND - 0.6V

Operating Range

Range	Temperature	V_{CC}	Tolerance
Commercial	0°C to +70°C	3.3	±0.3
Extended	-40°C to +85°C	3.3	±0.3

DC Read Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IL}	Input Low Level		-0.3	0.7	V
V_{IH}	Input High Level		2.0	V_{CC} + 0.3	V
V_{OL1}	Output Low Voltage (TTL)			0.4	V
V_{OH1}	Output High Voltage (TTL)		2.4		V
V_{OL2}	Output Low Voltage (CMOS)			0.2	V
V_{OH2}	Output High Voltage (CMOS)		V_{CC} - 0.3		V
I_{SB1}	V_{CC} Standby Current (TTL)	$\overline{CE} = V_{IH}$		150	µA
I_{SB2}	V_{CC} Standby Current (CMOS)	$\overline{CE} = V_{CC}$ ±0.3V		50	µA
I_{CC}	V_{CC} Active Current	$\overline{CE} = \overline{OE} = V_{IL}$, I/O = 0 µA, f = 5 MHz		20	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$		10	µA
I_{LI}	Input Load Current	V_{IN} = 3.3 or GND	-1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 3.3V or GND	-1	10	µA

AC Read Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	200		250		Units
		Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		200		250	
t_{CE}	$\overline{CE}$ to Output Delay		200		250	
t_{OE}	$\overline{OE}$ to Output Delay		70		75	
t_{DF} (Note 3)	Output Disable to Output Float	0	50	0	60	ns
t_{OH} (Note 3)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		

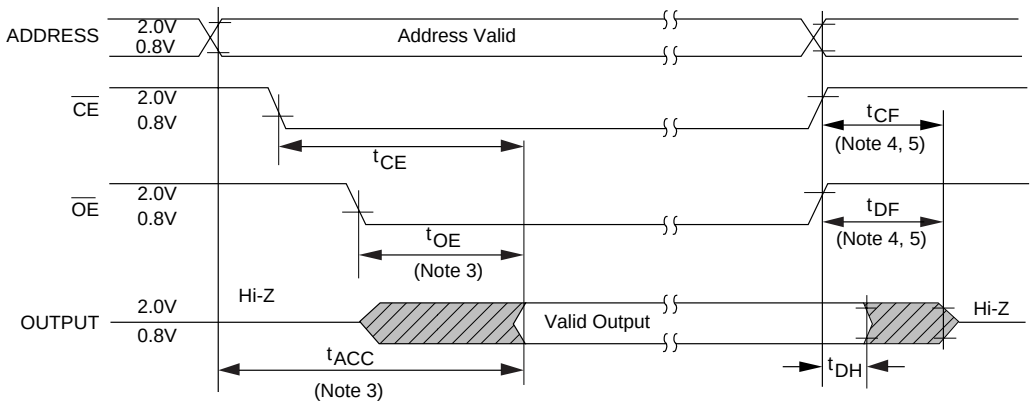
Capacitance (Note 3) T_A = +25˚C, f = 1 MHz

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	12	20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	13	20	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF (Note 9)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Note 7) (Note 8) (Note 10)



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Note 2: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 3: This parameter is only sampled and is not 100% tested.

Note 4: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 5: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE™, the measured V_{OH1} (DC) - 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 6: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 7: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND.

Note 8: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 9: 1 TTL Gate: I_{OL} = 1.6 mA, I_{OH} = -400 µA.
C_L: 100 pF includes fixture capacitance.

Note 10: V_{PP} may be connected to V_{CC} except during programming.

Note 11: Inputs and outputs can undershoot to -2.0V for 20 ns Max.

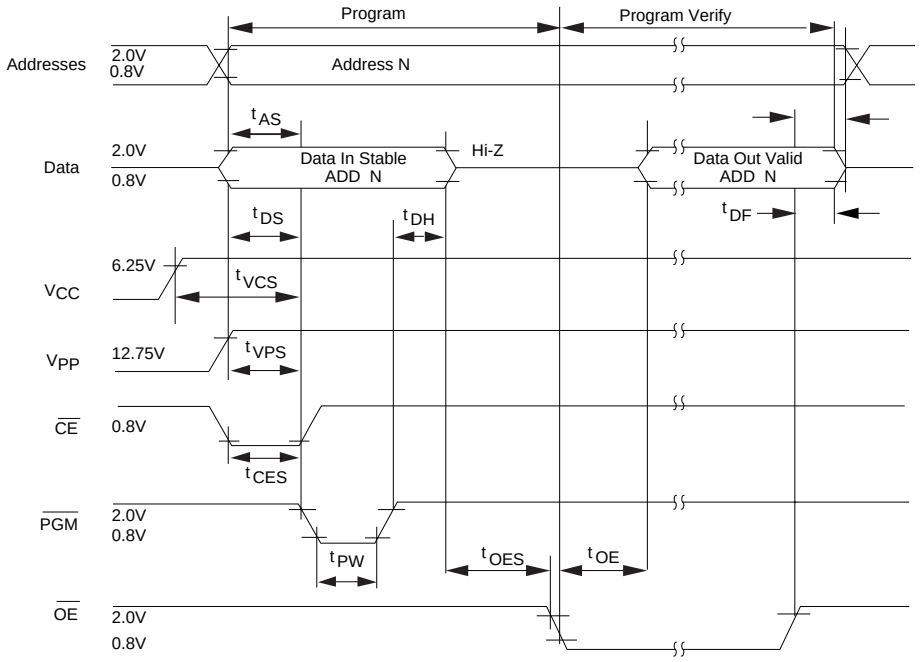
Programming Characteristics (Note 12) (Note 13) (Note 14) (Note 15)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			µs
t_{OES}	$\overline{OE}$ Setup Time		1			µs
t_{CES}	$\overline{CE}$ Setup Time	$\overline{OE} = V_{IH}$	1			µs
t_{DS}	Data Setup Time		1			µs
t_{VPS}	V_{PP} Setup Time		1			µs
t_{VCS}	V_{CC} Setup Time		1			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		1			µs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		60	ns

Programming Characteristics (Note 12) (Note 13) (Note 14) (Note 15) (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PW}	Program Pulse Width		45	50	105	µs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IL}$			40	mA
I_{CC}	V_{CC} Supply Current				50	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.25	6.5	6.75	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

Programming Waveforms (Note 14)



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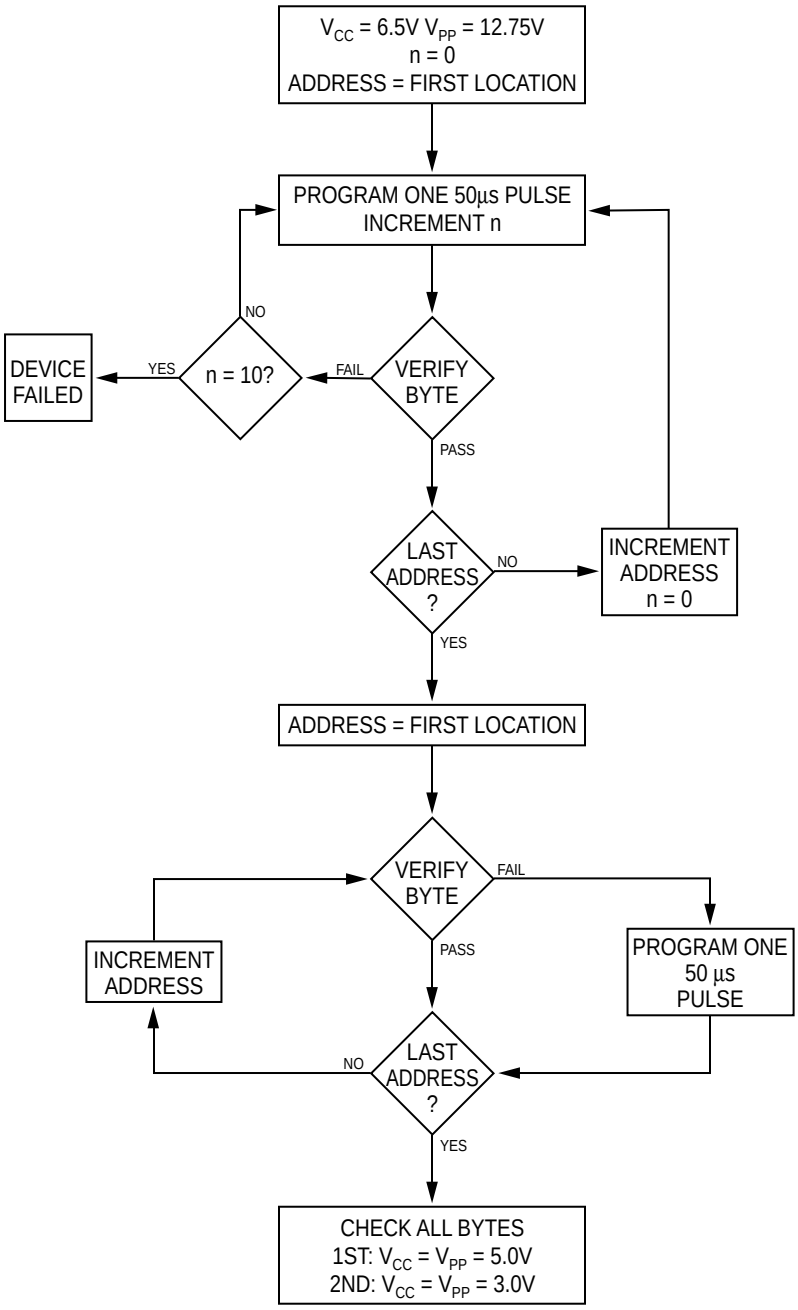
Note 12: Fairchild's standard product warranty applies only to devices programmed to specifications described herein.

Note 13: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 14: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 µF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 15: During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

Turbo LV Programming Algorithm Flow Chart



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Note: The standard National Semiconductor algorithm may also be used but it will have longer programming time.

FIGURE 1.

Functional Description

DEVICE OPERATION

The six modes of operation of the EPROM are listed in . It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 3.3V in the other three modes. The V_{CC} power supply must be at 6.5V during the three programming modes, and at 3.3V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from 66 mW to 66 µW. The EPROM is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the $\overline{OE}$ input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Tying

Because the EPROM is usually used in larger memory arrays, Fairchild has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

1. the lowest possible memory power dissipation, and
2. complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on the V_{PP} or A9 pin will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 µF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 16 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the Turbo Programming Algorithm shown in Figure 1. Each Address is programmed with a series of 50 µs pulses until it verifies good, up to a maximum of 10 pulses. Most memory cells will program with a single 50 µs pulse. (The standard National Semiconductor Algorithm may also be used but it will have longer programming time.)

The EPROM must not be programmed with a DC signal applied to the PGM input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled EPROM.

Functional Description (Continued)

MODE SELECTION

The modes of operation of the NM27LV210 are listed in Table 1. A single power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 for device signature.

TABLE 1. Modes Selection

Pins / Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X (Note 16)	X	3.3V	D_{OUT}
Output Disable	X	V_{IH}	X	X	3.3V	High Z
Standby	V_{IH}	X	X	X	3.3V	High Z
Programming	V_{IL}	V_{IH}	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	X	X	12.75V	6.25V	High Z

Note 16: X can be V_{IL} or V_{IH}.

Program Inhibit

Programming multiple EPROM's in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel EPROM may be common. A TTL low level program pulse applied to an EPROM's $\overline{PGM}$ input with $\overline{CE}$ at V_{IL} and V_{PP} at 12.75V will program that EPROM. A TTL high level $\overline{CE}$ input inhibits the other EPROM's from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 6.25V. V_{PP} must be at V_{CC}, except during programming and program verify.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table 2, specifically identifies the manufacturer and device type. The code for the NM27LV210 is "8FD6", where "8F" designates that it is made by Fairchild Semiconductor, and "D6" designates a 1 Megabit (64K x 16) part.

The code is accessed by applying 12V ±0.5V to address pin A9 . Addresses A1 –A8 ,A10 –A15 , and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the lower eight data pins, O0 –07 . Proper code access is only guaranteed at 25°C ± 5°C.

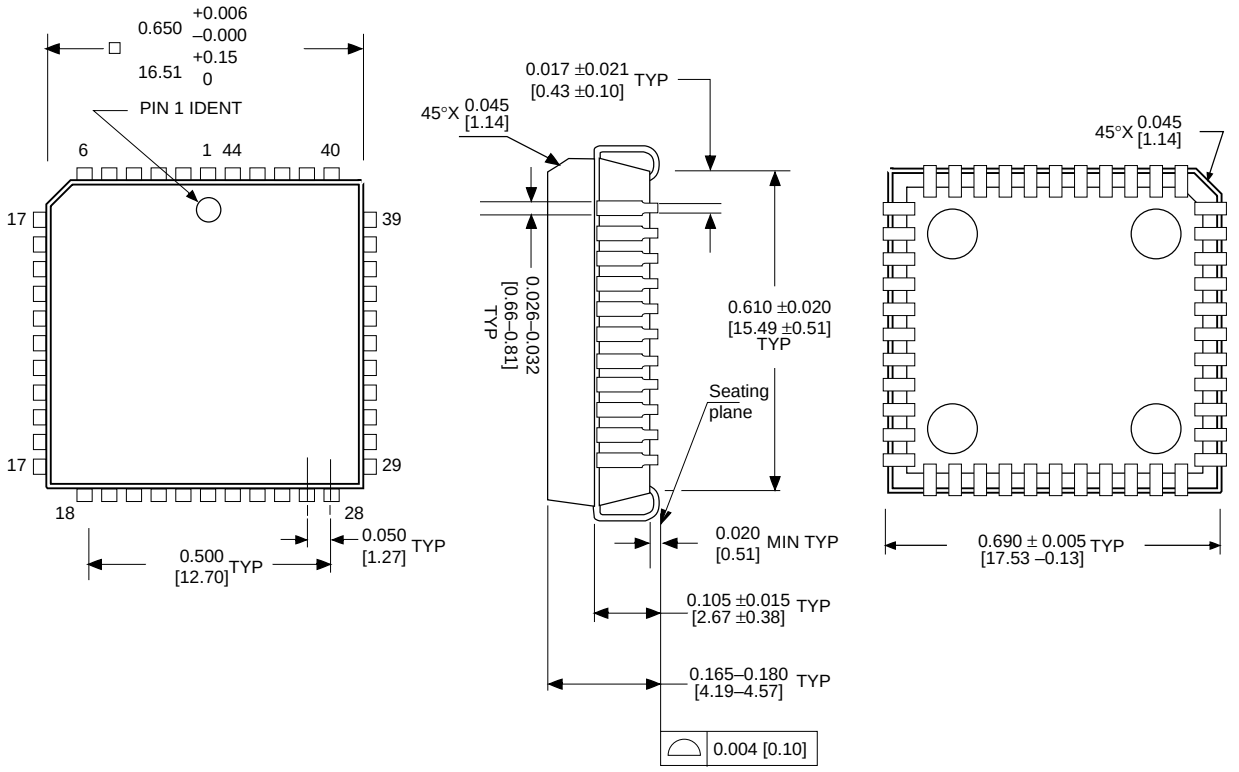
SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE 2. Manufacturer's Identification Code

Pins	A0 (21)	A9 (31)	O7 (12)	O6 (13)	O5 (14)	O4 (15)	O3 (16)	O2 (17)	O1 (18)	O0 (19)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	1	1	0	1	0	1	1	0	D6

Physical Dimensions inches (millimeters) unless otherwise noted



44-Lead Plastic Chip Carrier (V)
Order Number NM27LV210XXX
Package Number V44A

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

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March 1999

FAIRCHILD SEMICONDUCTOR™

NM34C02
2K-Bit Standard 2-Wire Bus Interface

Designed with Permanent Write-Protection for First 128 Bytes for Serial Presence Detect Application on Memory Modules

General Description

The NM34C02 is 2048 bits of CMOS non-volatile electrically erasable memory. It is designed to support Serial Presence Detect circuitry in memory modules. This communications protocol uses CLOCK (SCL) and DATA I/O (SDA) lines to synchronously clock data between the master (for example a microprocessor) and the slave EEPROM device(s).

The contents of the non-volatile memory allows the CPU to determine the capacity of the module and the electrical characteristics of the memory devices it contains. This will enable "plug and play" capability as the module is read and PC main memory resources utilized through the memory controller.

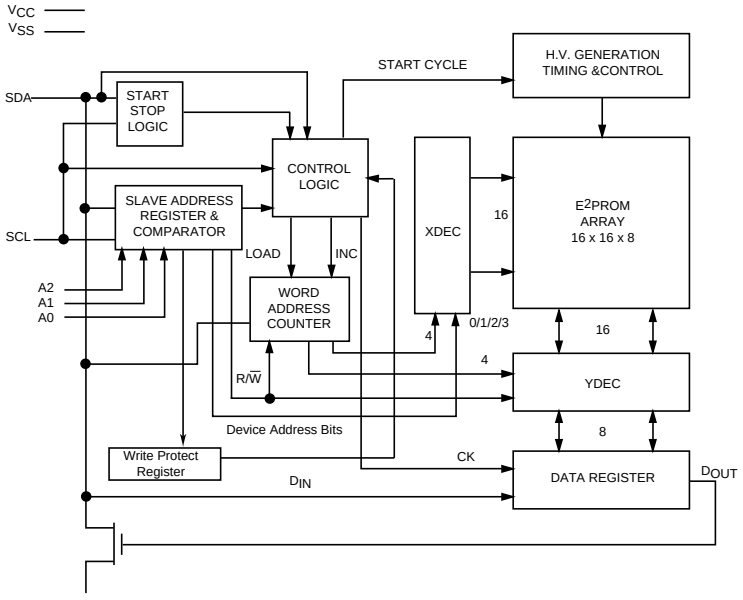
The first 128 bytes of the memory of the NM34C02 can be permanently Write Protected by writing to the "WRITE PROTECT" Register. Write Protect implementation details are described under the section titled **Addressing the WP Register**.

The NM34C02 is available in a JEDEC standard TSSOP package for low profile memory modules for systems requiring efficient space utilization such as in a notebook computer. Two options are available: L - Low Voltage and LZ - Low Power, allowing the part to be used in systems where battery life is of primary importance.

Features

- Extended Operating Voltage: 2.7V-5.5V
- Write-Protection for first 128 bytes
- 200 µA active current typical
  - 10 µA standby current typical
  - 1.0 µA standby current typical (L)
  - 0.1 µA standby current typical (LZ)
- IIC compatible interface
  - Provides bidirectional data transfer protocol
- Sixteen byte page write mode
  - Minimizes total write time per byte
- Self timed write cycle
  - Typical write cycle time of 6ms
- Endurance: 1,000,000 data changes
- Data retention greater than 40 years
- Packages available: 8-pin TSSOP and 8-pin SO

Block Diagram



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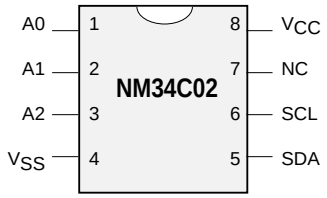
Connection Diagram

SO (M8) and TSSOP (MT8) Package



DS012821-2

Top View
See Package Number
M08A and MTC08

Pin Names	
A0,A1,A2	Device Address Inputs
V_{SS}	Ground
SDA	Data I/O
SCL	Clock Input
NC	No Connection
V_{CC}	Power Supply

Ordering Information

NM34C02 XX X X

Package
M8 = 8 pin SOIC
MT8 = 8 pin TSSOP

Temperature Range
Blank = 0°C to +70°C
E = -40°C to +85°C

Voltage Range
Blank = 4.5V to 5.5V
L = 2.7V to 4.5V
LZ = 2.7V to 4.5V and < 1μA standby current

Device
2K IIC Serial EEPROM

DS012821-21

Product Specifications

Absolute Maximum Ratings

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltages with Respect to Ground	6.5V to –0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min.

Operating Conditions

Ambient Operating Temperature	
NM34C02	0°C to +70°C
NM34C02E	-40°C to +85°C
Positive Power Supply	
NM34C02	4.5V to 5.5V
NM34C02L	2.7V to 4.5V
NM34C02LZ	2.7V to 4.5V

Standard V_{CC} (4.5V to 5.5V) DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		0.2	1.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		10	50	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	1	µA
V_{IL}	Input Low Voltage		–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Low V_{CC} (2.7V to 5.5V) DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		0.2	1.0	mA
I_{SB}	Standby Current for L Standby Current for LZ	V_{IN} = GND or V_{CC} V_{IN} = GND or V_{CC}		1 0.1	10 1	µA µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	1	µA
V_{IL}	Input Low Voltage		–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Capacitance T_A = +25°C, f = 100/400 KHz, V_{CC} = 5V (Note 2)

Symbol	Test	Conditions	Max	Units
$C_{I/O}$	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN}	Input Capacitance (A0, A1, A2, SCL)	V_{IN} = 0V	6	pF

Note 1: Typical values are T_A = 25°C and nominal supply voltage (5V).

Note 2: This parameter is periodically sampled and not 100% tested.

AC Conditions of Test

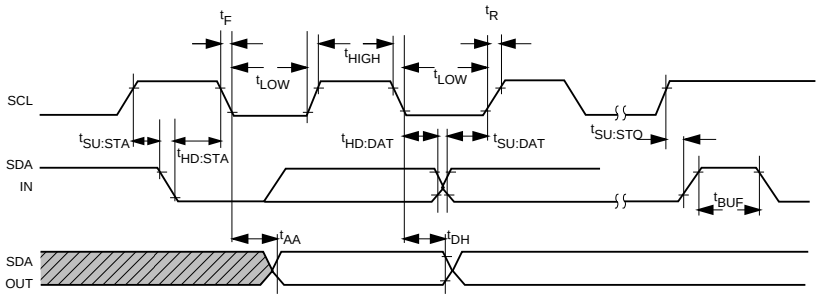
Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10 ns
Input & Output Timing Levels	V_{CC} x 0.5
Output Load	1 TTL Gate and C_L = 100 pF

Read and Write Cycle Limits (Standard and Low V_{CC} Range 2.7V - 4.5V)

Symbol	Parameter	100 KHz		400 KHz		Units
		Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		100		400	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs (Minimum V_{IN} Pulse width)		100		50	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	0.1	0.9	µs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		1.3		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		0.6		µs
t_{LOW}	Clock Low Period	4.7		1.5		µs
t_{HIGH}	Clock High Period	4.0		0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		µs
$t_{HD:DAT}$	Data in Hold Time	0		0		µs
$t_{SU:DAT}$	Data in Setup Time	250		100		ns
t_R	SDA and SCL Rise Time		1		0.3	µs
t_F	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		0.6		µs
t_{DH}	Data Out Hold Time	300		50		ns
t_{WR} (Note 3)	Write Cycle Time - NM34C02 - NM34C02L, NM34C02LZ		10 15		10 15	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the NM34C02 bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

Bus Timing



DS012821-4

Background Information (IIC Bus)

As mentioned, the IIC bus allows synchronous bidirectional communication between Transmitter/Receiver using the SCL (clock) and SDA (Data I/O) lines. All communication must be started with a valid START condition, concluded with a STOP condition and acknowledged by the Receiver with an ACKNOWLEDGE condition.

In addition, since the IIC bus is designed to support other devices such as RAM, EPROMs, etc., a device type identifier string must follow the START condition. For EEPROMs, this 4-bit string is 1010. Also refer the **Addressing the WP Register** section.

As shown below, although the EEPROMs on the IIC bus may be configured in any manner required, the total memory addressed can not exceed 16K (16,384 bits) on the Standard IIC protocol. EEPROM memory address programming is controlled by 2 methods:

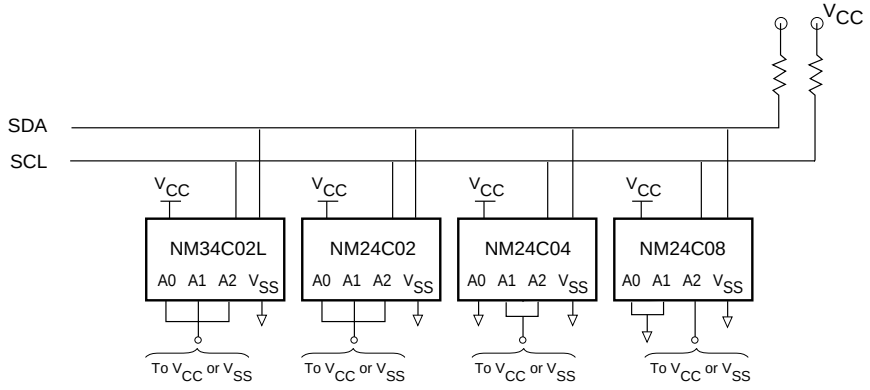
- Hardware configuring the A0, A1, and A2 pins (Device Address pins) with pull-up or pull-down resistors. **All unused pins must be grounded** (tied to V_{SS}).
- Software addressing the required PAGE BLOCK within the device memory array (as sent in the Slave Address string).

Addressing an EEPROM memory location involves sending a command string with the following information:

[DEVICE TYPE]—[DEVICE ADDRESS]—[PAGE BLOCK ADDRESS]—[BYTE ADDRESS]

DEFINITIONS	
BYTE	8 bits of data
PAGE	16 sequential addresses (one byte each) that may be programmed during a 'Page Write' programming cycle
PAGE BLOCK	2,048 (2K) bits organized into 16 pages of addressable memory. (8 bits) x (16 bytes) x (16 pages) = 2,048 bits
MASTER	Any IIC device CONTROLLING the transfer of data (such as a microprocessor)
SLAVE	Device being controlled (EEPROMs are always considered Slaves)
TRANSMITTER	Device currently SENDING data on the bus (may be either a Master or Slave).
RECEIVER	Device currently receiving data on the bus (Master or Slave)

Example of 16K of Memory on 2-Wire Bus



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Note: The SDA pull-up resistor is required due to the open-drain/open collector output of IIC bus devices
The SCL pull-up resistor is recommended because of the normal SCL line inactive 'high' state.
It is recommended that the total line capacitance be less than 400pF.
Specific timing and addressing considerations are described in greater detail in the following sections.

Device	Address Pins			Memory Size	Number of Page Blocks
	A0	A1	A2		
NM34C02	ADR	ADR	ADR	2048 Bits	1

Pin Descriptions

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire–ORed with any number of open drain or open collector outputs.

Device Operation Inputs (A0, A1, A2)

Device address pins A0, A1, and A2 are connected to V_{CC} or V_{SS} to configure the EEPROM chip address. Table A shows the active pins across the NM34C02 device family.

Table 1.

Device	A0	A1	A2	Effects of Addresses
NM34C02L	ADR	ADR	ADR	8 devices max.

Device Operation

The NM34C02 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the NM34C02 will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to *Figures 1* and *2.*

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The NM34C02 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Stop Condition

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the NM34C02 to place the device in the standby power mode.

ACKNOWLEDGE

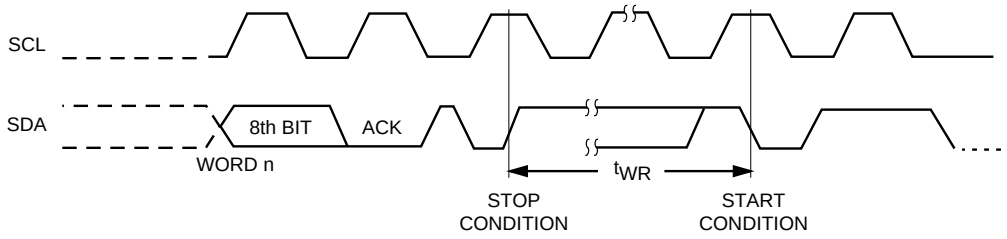
Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits.

During the ninth clock cycle the receiver will pull the SDA line to LOW to acknowledge that it received the eight bits of data. Refer to *Figure 3.*

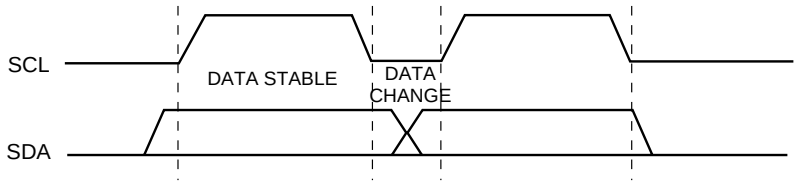
The NM34C02 device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the NM34C02 will respond with an acknowledge after the receipt of each subsequent eight bit byte.

In the Read mode the NM34C02 slave will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to the standby power mode.

Write Cycle Timing

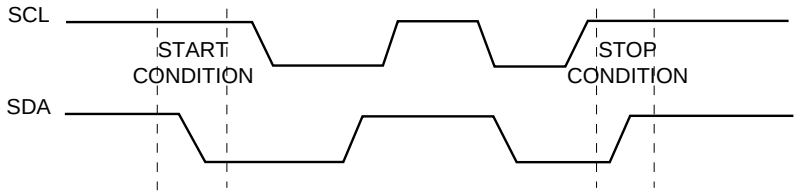


DS012821-6



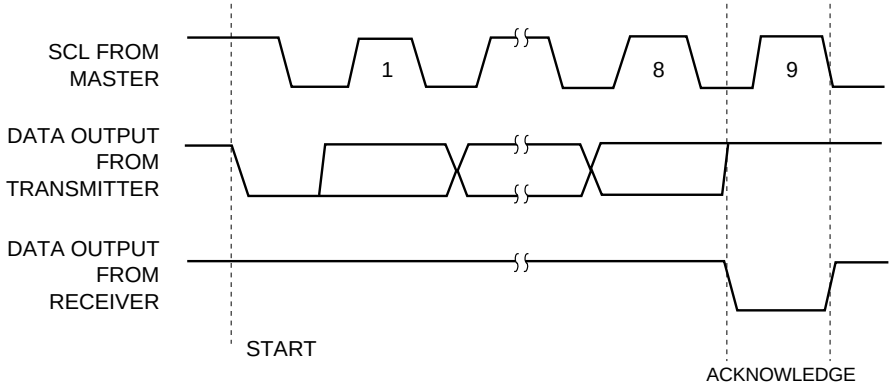
DS012821-7

Data Validity (Figure 1).



DS012821-8

Start and Stop Definition (Figure 2).



DS012821-9

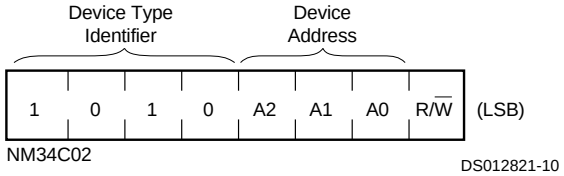
Acknowledge Responses from Receiver (Figure 3).

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are those of the device type identifier (*see Figure 4).* This is fixed as 1010 for all EEPROM devices.

All IIC EEPROMs use an internal protocol that defines a PAGE BLOCK size of 2K bits (for Byte addresses 00 through FF).

Device Addressing (Continued)



Slave Addresses (Figure 4).

Refer to the following table for Slave Address string details:

Device	A0	A1	A2	Page Blocks	Page Block Addresses
NM34C02	A	A	A	1 (2K)	(None)

Write Operations

The last bit of the slave address defines whether a write or read condition is requested by the master. A '1' indicates that a read operation is to be executed, and a '0' initiates the write mode.

A simple review: After the NM34C02 recognizes the start condition, the devices interfaced to the IIC bus wait for a slave address to be transmitted over the SDA line. If the transmitted slave address matches an address of one of the devices, the designated slave pulls the line LOW with an acknowledge signal and awaits further transmissions.

Byte Write

For a write operation a second address field is required which is a byte address that is comprised of eight bits and provides access to any one of the 256 bytes in the selected page block of memory. Upon receipt of the byte address the NM34C02 responds with an acknowledge and waits for the next eight bits of data, again, responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the NM34C02 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the NM34C02 inputs are disabled, and the device will not respond to any requests from the master. Refer to *Figure 5* for the address, acknowledge and data transfer sequence.

Page Write

The NM34C02 is capable of a sixteen byte page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data byte is transferred, the master can transmit up to fifteen more bytes. After the receipt of each byte, the NM34C02 will respond with an acknowledge.

After the receipt of each byte, the internal address counter increments to the next address and the next SDA data is accepted. If the master should transmit more than sixteen bytes prior to generating the stop condition, the address counter will 'roll over' and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to *Figure 6* for the address, acknowledge, and data transfer sequence.

Acknowledge Polling

Once the stop condition is issued to indicate the end of the host's write operation the NM34C02 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the NM34C02 is still busy with the write operation no ACK will be returned. If the NM34C02 has completed the write operation an ACK will be returned and the host can then proceed with the next read or write operation.

Software Write Protect

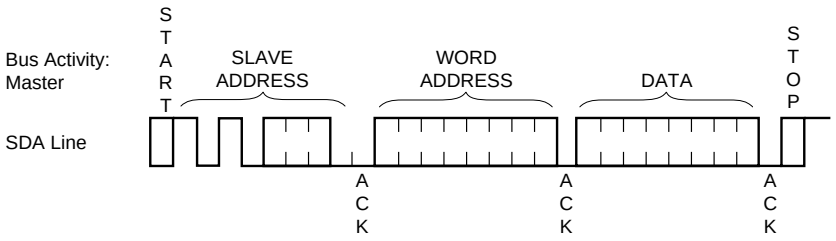
Write protection on the NM34C02 protects the first 128 bytes of the EEPROM memory. Write protection is implemented through a seperate register called the WRITE PROTECT (WP) Register and writing to this WP register permanently WRITE protects the memory. **This WP register is a "one-time-only-write" register. Once this register is written, it cannot be erased. After the first WRITE to this register, all future access' to this register are ignored as if an invalid IIC cycle occured.** To write protect, the user must perform a byte write to the WP register. This will permanently disable programming to the first 128 bytes of memory.

Addressing the WP Register

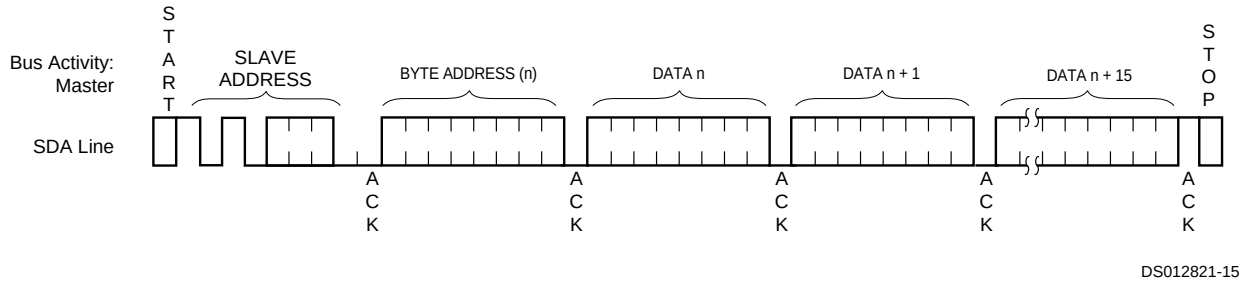
Addressing the WP register is very similar to accessing any memory array with the following difference:

Instead of the conventional "1010" IIC device address, the unused IIC device address "0110" is used to access just the WP register. Device address "1010" will be used for all the typical memory array access. With this difference in place, accessing the WP register is same as a typical IIC byte write cycle as described under "Write Operations" section. All timing information and waveform details remain the same. The "Byte Address" and the "Data" fields of the Byte write cycle serve as place holders and can be of any value (Don't Care). Refer to *Figure 7*.

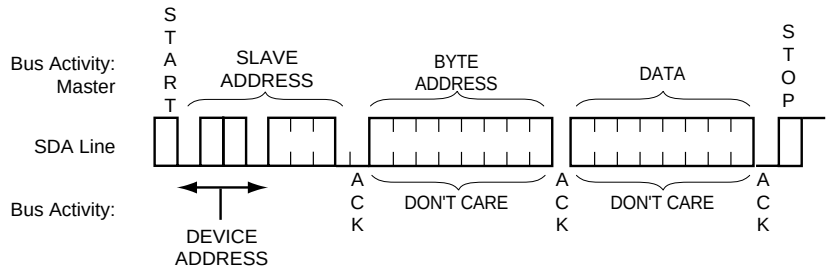
Write Protect Scheme (Continued)



Byte Write (Figure 5).



Page Write (Figure 6).



WP Register Write (Figure 7).

Read Operations

Read operations are initiated in the same manner as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to a one. There are three basic read operations: current address read, random read, and sequential read.

CURRENT ADDRESS READ

Internally the NM34C02 contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ set to one, the NM34C02 issues an acknowledge and transmits the data byte. The master will not acknowledge the transfer but does generate a stop condition, and therefore the NM34C02 discontinues transmission. Refer to *Figure* 8 for the sequence of address, acknowledge and data transfer.

RANDOM READ

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, slave address, R/$\overline{W}$ bit set to zero, and then the word address to be read. After the Slave word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the NM34C02 and then by the eight bit word. The master will not acknowledge the transfer but does generate the stop condition, and therefore the NM34C02 discontinues transmission. Refer to *Figure 9* for the address, acknowledge and data transfer sequence.

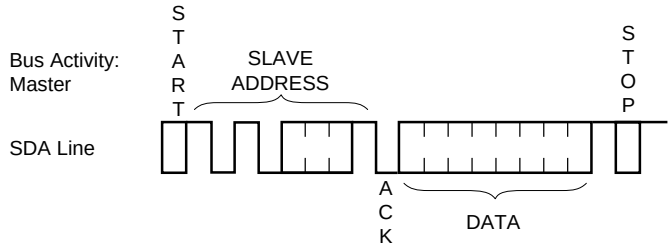
SEQUENTIAL READ

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted in the same manner as the other read modes; however, the master now responds with an acknowledge, indicating it requires additional data. The NM34C02 continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge or by generating a stop condition.

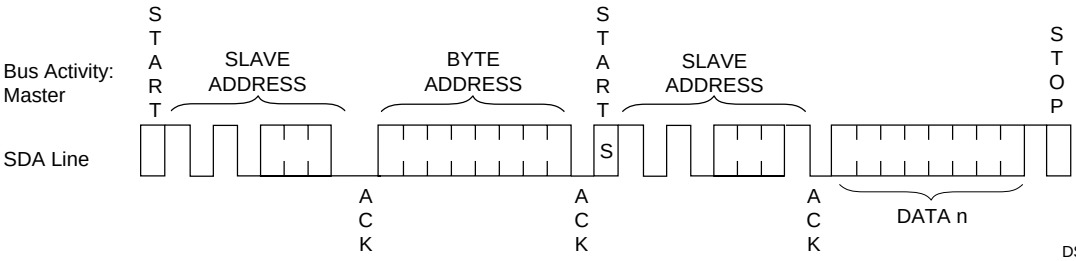
The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read

Read Operations (Continued)

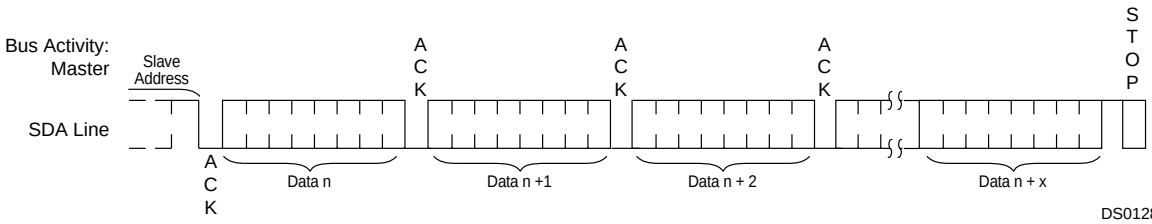
operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. After the entire memory has been read, the counter 'rolls over' and the NM34C02 continues to output data for each acknowledge received. Refer to *Figure 10* for the address, acknowledge, and data transfer sequence.



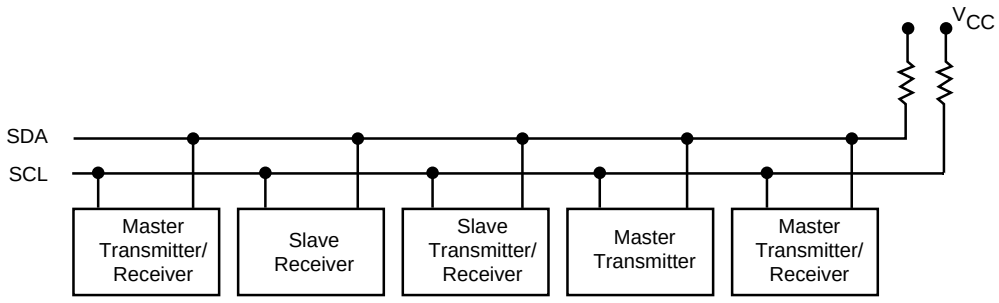
Current Address Read (Figure 8).



Random Read (Figure 9).



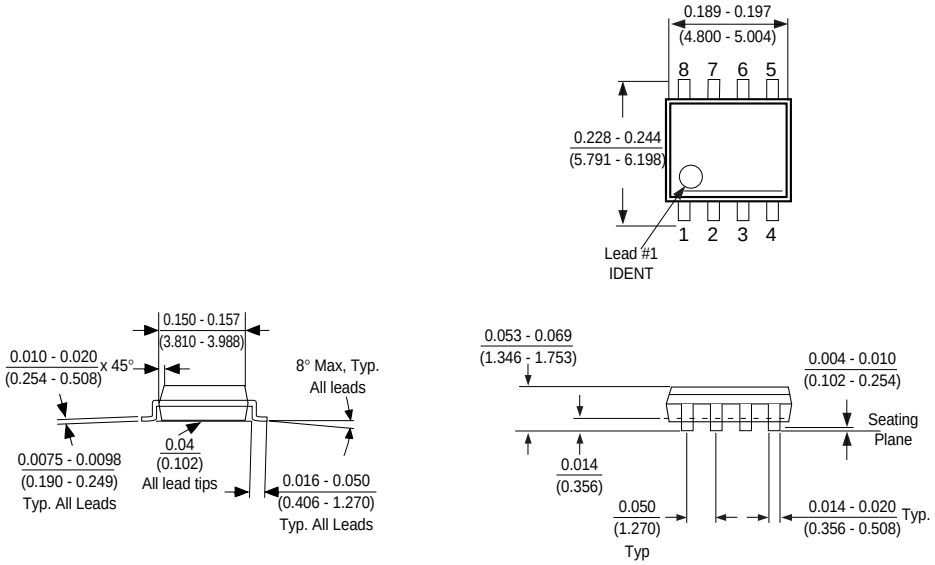
Sequential Read (Figure 10).



Note: Due to open drain configuration of SDA, a bus-level resistor is called for (Typical value = 4.7Ω)

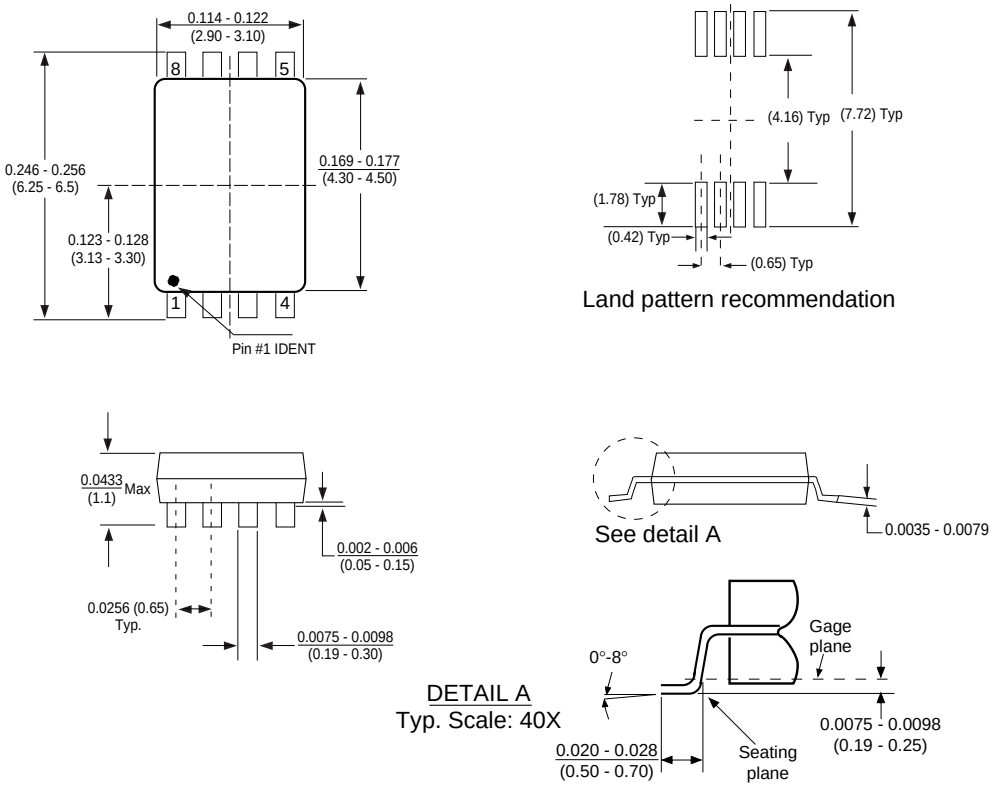
Typical System Configuration (Figure 11).

Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin Molded Small Outline Package (M8)
Order Number NM34C02LM8/LZM8
Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted



Notes: Unless otherwise specified
1. Reference JEDEC registration MO153. Variation AA. Dated 7/93

8-Pin Molded TSSOP, JEDEC (MT8)
Order Number NM34C02LMT8/LZMT8
Package Number MTC08

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March 1999

FAIRCHILD SEMICONDUCTOR™

NM34W02
2K-Bit Standard 2-Wire Bus Interface Serial EEPROM with Full Array Write Protect

Designed with Permanent Write-Protection for First 128 Bytes for Serial Presence Detect Application on Memory Modules (PC100 Compliant)

General Description

The NM34W02 is 2048 bits of CMOS non-volatile electrically erasable memory. This device is specifically designed to support Serial Presence Detect circuitry in memory modules. This communications protocol uses CLOCK (SCL) and DATA I/O (SDA) lines to synchronously clock data between the master (for example a microprocessor) and the slave EEPROM device(s).

The contents of the non-volatile memory allows the CPU to determine the capacity of the module and the electrical characteristics of the memory devices it contains. This will enable "plug and play" capability as the module is read and PC main memory resources utilized through the memory controller.

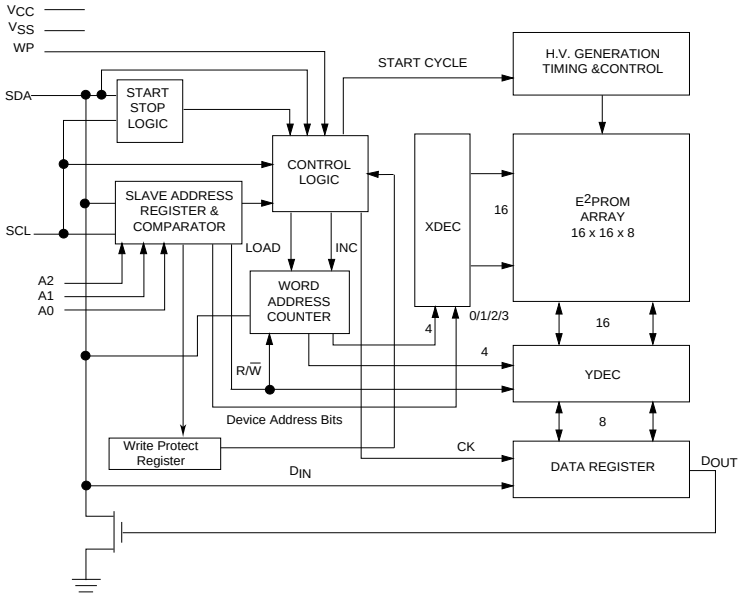
The first 128 bytes of the memory of the NM34W02 can be permanently Write Protected by writing to the "WRITE PROTECT" Register. Write Protect implementation details are described under the section titled **Addressing the WP Register**. In addition, like the NM24Wxx product family, the entire memory array can be write-protected through "WP" pin.

The NM34W02 is available in a JEDEC standard TSSOP package for low profile memory modules for systems requiring efficient space utilization such as in a notebook computer. Two options are available: L - Low Voltage and LZ - Low Power, allowing the part to be used in systems where battery life is of primary importance.

Features

- PC100 Compliant
- Extended Operating Voltage: 2.7V-5.5V
- Software Write-Protection for first 128 bytes
- Hardware Write-Protection for entire memory array
- 200 µA active current typical
  - 1.0 µA standby current typical (L)
  - 0.1 µA standby current typical (LZ)
- IIC compatible interface
  - Provides bidirectional data transfer protocol
- Sixteen byte page write mode
  - Minimizes total write time per byte
- Self timed write cycle
  - Typical write cycle time of 6ms
- Endurance: 1,000,000 data changes
- Data retention greater than 40 years
- Packages available: 8-pin TSSOP and 8-pin SO
- Temperature Ranges: Commercial and Extended

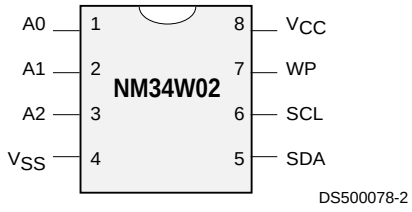
Block Diagram



DS500078-1

Connection Diagram

SO (M8) and TSSOP (MT8) Package



Top View
See Package Number
M08A and MTC08

Pin Names	
A0,A1,A2	Device Address Inputs
V_{SS}	Ground
SDA	Data I/O
SCL	Clock Input
WP	Write Protect
V_{CC}	Power Supply

Ordering Information

NM 34 W 02 LZ E XX

	Letter	Description
Package	M8	8-Pin SO8
	MT8	8-Pin TSSOP
Temp. Range	None	0 to 70°C
	E	-40 to +85°C
Voltage Operating Range	Blank	4.5V to 5.5V
	L	2.7V to 4.5V
	LZ	2.7V to 4.5V and <1µA Standby Current
Density	02	2K
	W	Full Array Write Protect
Interface	34	IIC
	NM	**Fairchild Non-Volatile Memory**

Product Specifications

Absolute Maximum Ratings

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltages with Respect to Ground	6.5V to –0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min.

Operating Conditions

Ambient Operating Temperature	
NM34W02	0°C to +70°C
NM34W02E	-40°C to +85°C
Positive Power Supply	
NM34W02	4.5V to 5.5V
NM34W02L	2.7V to 4.5V
NM34W02LZ	2.7V to 4.5V

Standard V_{CC} (4.5V to 5.5V) DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		0.2	1.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		10	50	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	1	µA
V_{IL}	Input Low Voltage		–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Low V_{CC} (2.7V to 5.5V) DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		0.2	1.0	mA
I_{SB}	Standby Current for L Standby Current for LZ	V_{IN} = GND or V_{CC} V_{IN} = GND or V_{CC}		1 0.1	10 1	µA µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	1	µA
V_{IL}	Input Low Voltage		–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Capacitance T_A = +25°C, f = 100/400 KHz, V_{CC} = 5V (Note 2)

Symbol	Test	Conditions	Max	Units
$C_{I/O}$	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN}	Input Capacitance (A0, A1, A2, SCL)	V_{IN} = 0V	6	pF

Note 1: Typical values are T_A = 25°C and nominal supply voltage (5V).

Note 2: This parameter is periodically sampled and not 100% tested.

AC Conditions of Test

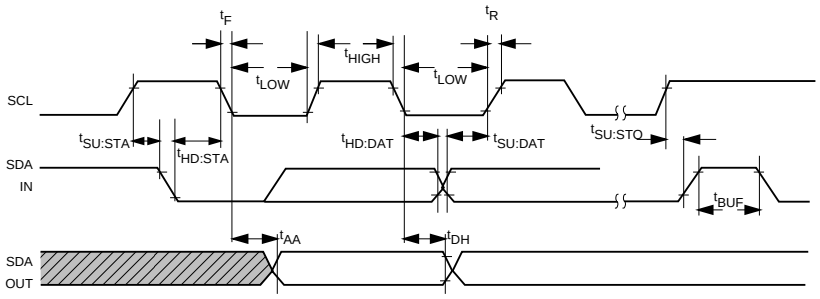
Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10 ns
Input & Output Timing Levels	V_{CC} x 0.5
Output Load	1 TTL Gate and C_L = 100 pF

Read and Write Cycle Limits (Standard and Low V_{CC} Range 2.7V - 5.5V)

Symbol	Parameter	100 KHz		400 KHz		Units
		Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		100		400	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs (Minimum V_{IN} Pulse width)		100		50	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	0.1	0.9	µs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		1.3		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		0.6		µs
t_{LOW}	Clock Low Period	4.7		1.5		µs
t_{HIGH}	Clock High Period	4.0		0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		µs
$t_{HD:DAT}$	Data in Hold Time	0		0		ns
$t_{SU:DAT}$	Data in Setup Time	250		100		ns
t_R	SDA and SCL Rise Time		1		0.3	µs
t_F	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		0.6		µs
t_{DH}	Data Out Hold Time	300		50		ns
t_{WR} (Note 3)	Write Cycle Time - NM34W02 - NM34W02L, NM34W02LZ		10 15		10 15	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the NM34W02 bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

Bus Timing



DS500078-5

Background Information (IIC Bus)

As mentioned, the IIC bus allows synchronous bidirectional communication between Transmitter/Receiver using the SCL (clock) and SDA (Data I/O) lines. All communication must be started with a valid START condition, concluded with a STOP condition and acknowledged by the Receiver with an ACKNOWLEDGE condition.

In addition, since the IIC bus is designed to support other devices such as RAM, EPROMs, etc., a device type identifier string must follow the START condition. For EEPROMs, this 4-bit string is 1010. Also refer the **Addressing the WP Register** section.

As shown below, although the EEPROMs on the IIC bus may be configured in any manner required, the total memory addressed can not exceed 16K (16,384 bits) on the Standard IIC. EEPROM memory address programming is controlled by 2 methods:

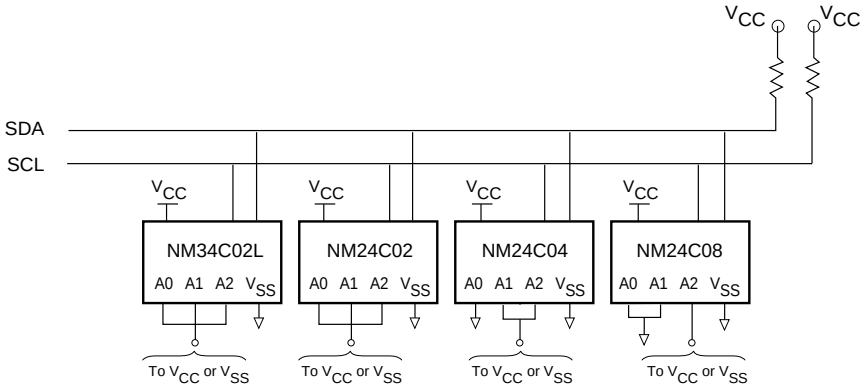
- Hardware configuring the A0, A1, and A2 pins (Device Address pins) with pull-up or pull-down to V_{CC} or V_{SS}. **All unused pins must be grounded** (tied to V_{SS}).
- Software addressing the required PAGE BLOCK within the device memory array (as sent in the Slave Address string).

Addressing an EEPROM memory location involves sending a command string with the following information:

[DEVICE TYPE]—[DEVICE ADDRESS]—[PAGE BLOCK ADDRESS]—[BYTE ADDRESS]

DEFINITIONS	
BYTE	8 bits of data
PAGE	16 sequential addresses (one byte each) that may be programmed during a 'Page Write' programming cycle
PAGE BLOCK	2,048 (2K) bits organized into 16 pages of addressable memory. (8 bits) x (16 bytes) x (16 pages) = 2,048 bits
MASTER	Any IIC device CONTROLLING the transfer of data (such as a microprocessor)
SLAVE	Device being controlled (EEPROMs are always considered Slaves)
TRANSMITTER	Device currently SENDING data on the bus (may be either a Master or Slave).
RECEIVER	Device currently receiving data on the bus (Master or Slave)

Example of 16K of Memory on 2-Wire Bus



DS500078-6

Note: The SDA pull-up resistor is required due to the open-drain/open collector output of IIC bus devices.
The SCL pull-up resistor is recommended because of the normal SCL line inactive 'high' state.
It is recommended that the total line capacitance be less than 400pF.
Specific timing and addressing considerations are described in greater detail in the following sections.

Device	Address Pins			Memory Size	Number of Page Blocks
	A0	A1	A2		
NM34W02	ADR	ADR	ADR	2048 Bits	1

Pin Descriptions

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire–ORed with any number of open drain or open collector outputs.

Device Operation Inputs (A0, A1, A2)

Device address pins A0, A1, and A2 are connected to V_{CC} or V_{SS} to configure the EEPROM chip address. Table A shows the active pins across the NM34W02 device family.

Table 1.

Device	A0	A1	A2	Effects of Addresses
NM34W02	ADR	ADR	ADR	8 devices max.

Device Operation

The NM34W02 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the NM34W02 will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to *Figures 1* and *2.*

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The NM34W02 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Stop Condition

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the NM34W02 to place the device in the standby power mode.

ACKNOWLEDGE

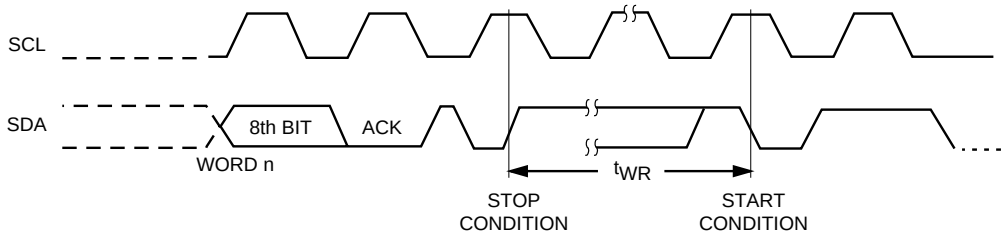
Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits.

During the ninth clock cycle the receiver will pull the SDA line to LOW to acknowledge that it received the eight bits of data. Refer to *Figure 3.*

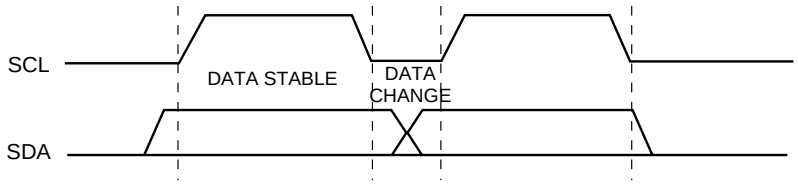
The NM34W02 device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the NM34W02 will respond with an acknowledge after the receipt of each subsequent eight bit byte.

In the Read mode the NM34W02 slave will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to the standby power mode.

Write Cycle Timing

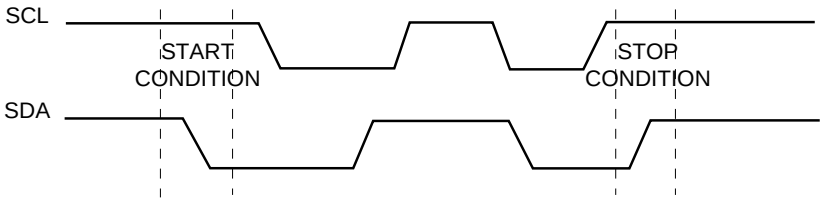


DS500078-7



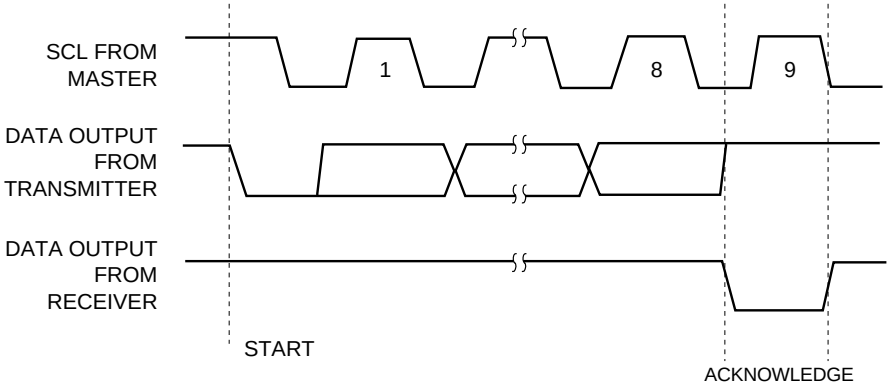
DS500078-8

Data Validity (Figure 1).



DS500078-9

Start and Stop Definition (Figure 2).



DS500078-10

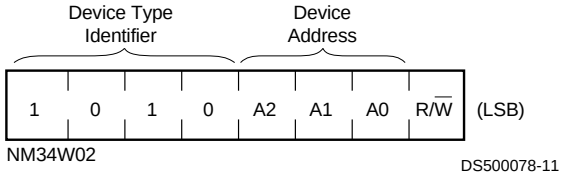
Acknowledge Responses from Receiver (Figure 3).

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are those of the device type identifier (*see Figure 4).* This is fixed as 1010 for all EEPROM devices.

All IIC EEPROMs use an internal protocol that defines a PAGE BLOCK size of 2K bits (for Byte addresses 00 through FF).

Device Addressing (Continued)



Slave Addresses (Figure 4).

Refer to the following table for Slave Address string details:

Device	A0	A1	A2	Page Blocks	Page Block Addresses
NM34W02	A	A	A	1 (2K)	(None)

Write Operations

The last bit of the slave address defines whether a write or read condition is requested by the master. A '1' indicates that a read operation is to be executed, and a '0' initiates the write mode.

A simple review: After the NM34W02 recognizes the start condition, the devices interfaced to the IIC bus wait for a slave address to be transmitted over the SDA line. If the transmitted slave address matches an address of one of the devices, the designated slave pulls the line LOW with an acknowledge signal and awaits further transmissions.

Byte Write

For a write operation a second address field is required which is a byte address that is comprised of eight bits and provides access to any one of the 256 bytes in the selected page block of memory. Upon receipt of the byte address the NM34W02 responds with an acknowledge and waits for the next eight bits of data, again, responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the NM34W02 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the NM34W02 inputs are disabled, and the device will not respond to any requests from the master. Refer to *Figure 5* for the address, acknowledge and data transfer sequence.

Page Write

The NM34W02 is capable of a sixteen byte page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data byte is transferred, the master can transmit up to fifteen more bytes. After the receipt of each byte, the NM34W02 will respond with an acknowledge.

After the receipt of each byte, the internal address counter increments to the next address and the next SDA data is accepted. If the master should transmit more than sixteen bytes prior to generating the stop condition, the address counter will 'roll over' and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to *Figure 6* for the address, acknowledge, and data transfer sequence.

Acknowledge Polling

Once the stop condition is issued to indicate the end of the host's write operation the NM34W02 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the NM34W02 is still busy with the write operation no ACK will be returned. If the NM34W02 has completed the write operation an ACK will be returned and the host can then proceed with the next read or write operation.

Software Write Protect

Software write protection on the NM34W02 protects the first 128 bytes of the EEPROM memory. Software write protection is implemented through a seperate register called the WRITE PROTECT (WP) Register and writing to this WP register permanently WRITE protects the memory. **This WP register is a "one-time-only-write" register. Once this register is written, it cannot be erased. After the first WRITE to this register, all future access' to this register are ignored as if an invalid IIC cycle occured.** To write protect, the user must perform a byte write to the WP register. This will permanently disable programming to the first 128 bytes of memory.

Addressing the WP Register

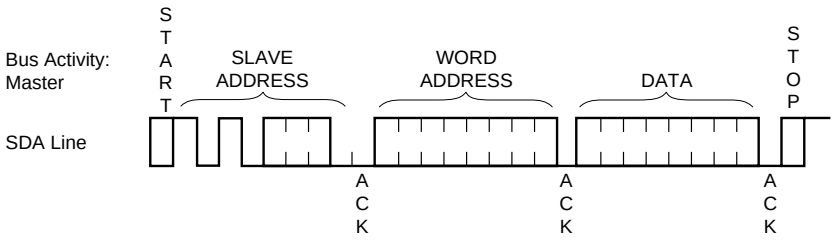
Addressing the WP register is very similar to accessing any memory array with the following difference:

Instead of the conventional "1010" IIC device address, the unused IIC device address "0110" is used to access just the WP register. Device address "1010" will be used for all the typical memory array access. With this difference in place, accessing the WP register is same as a typical IIC byte write cycle as described under "Write Operations" section. All timing information and waveform details remain the same. The "Byte Address" and the "Data" fields of the Byte write cycle serve as place holders and can be of any value (Don't Care). Refer to *Figure 7*.

Hardware Write Protect

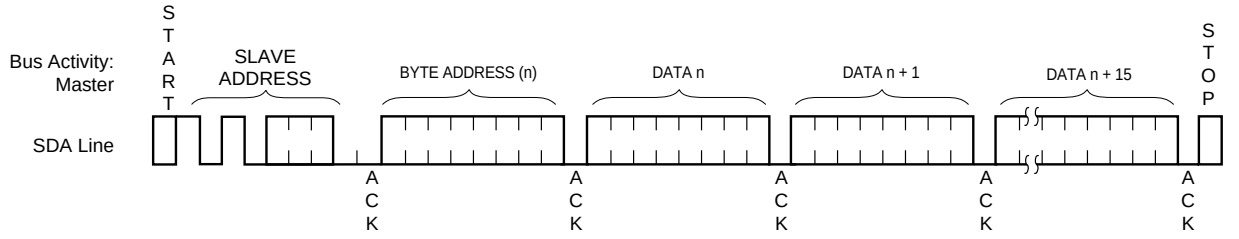
Programming of the memory will not take place if the WP pin of the NM34W02 is connected to V_{CC}, regardless of whether the software write protect register has been implemented or not. The NM34W02 will accept slave and word addresses; but if the memory accessed is write protected by the WP pin, the NM34W02 will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the stop condition is asserted. (Note: if the WP pin is set to V_{CC}, it will prevent the software write protect register from being written.)

Write Protect Scheme (Continued)



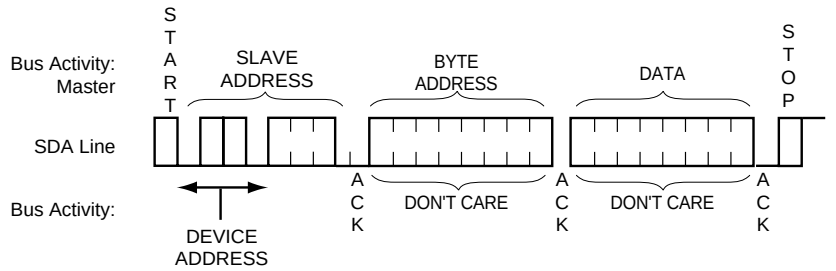
DS500078-15

Byte Write (Figure 5).



DS500078-16

Page Write (Figure 6).



DS500078-17

WP Register Write (Figure 7).

Read Operations

Read operations are initiated in the same manner as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to a one. There are three basic read operations: current address read, random read, and sequential read.

CURRENT ADDRESS READ

Internally the NM34W02 contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ set to one, the NM34W02 issues an acknowledge and transmits the data byte. The master will not acknowledge the transfer but does generate a stop condition, and therefore the NM34W02 discontinues transmission. Refer to *Figure* 8 for the sequence of address, acknowledge and data transfer.

RANDOM READ

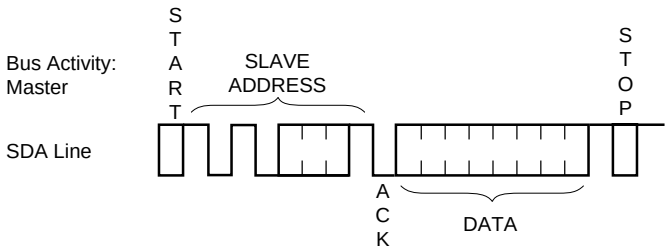
Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, slave address, R/$\overline{W}$ bit set to zero, and then the word address to be read. After the slave word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the NM34W02 and then by the eight bit word. The master will not acknowledge the transfer but does generate the stop condition, and therefore the NM34W02 discontinues transmission. Refer to *Figure 9* for the address, acknowledge and data transfer sequence.

SEQUENTIAL READ

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted in the same manner as the other read modes; however, the master now responds with an acknowledge, indicating it requires additional data. The NM34W02 continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge or by generating a stop condition.

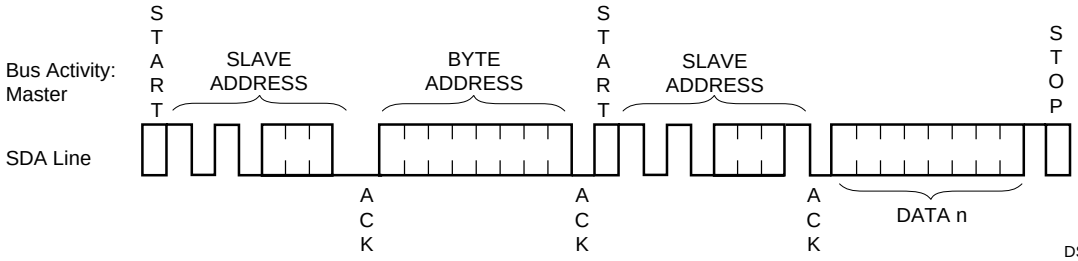
The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. After the entire memory has been read, the counter 'rolls over' and the NM34W02 continues to output data for each acknowledge received. Refer to *Figure 10* for the address, acknowledge, and data transfer sequence.

Current Address Read (Figure 8)



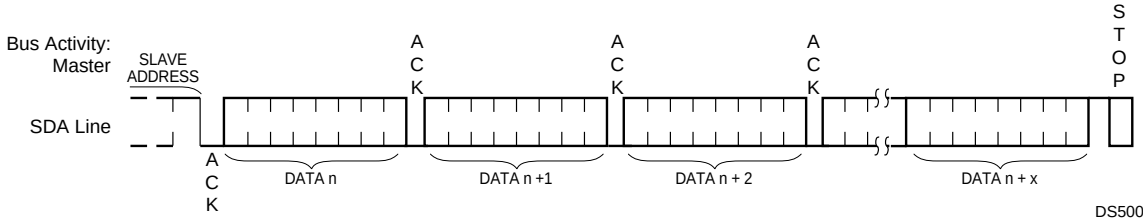
DS500078-18

Random Read (Figure 9)



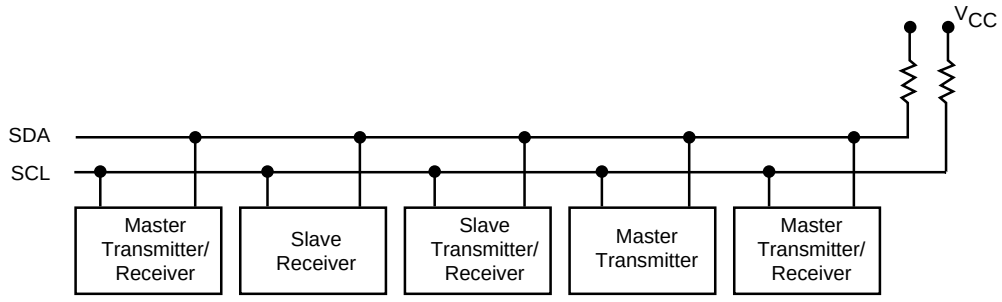
DS500078-19

Sequential Read (Figure 10)



DS500078-20

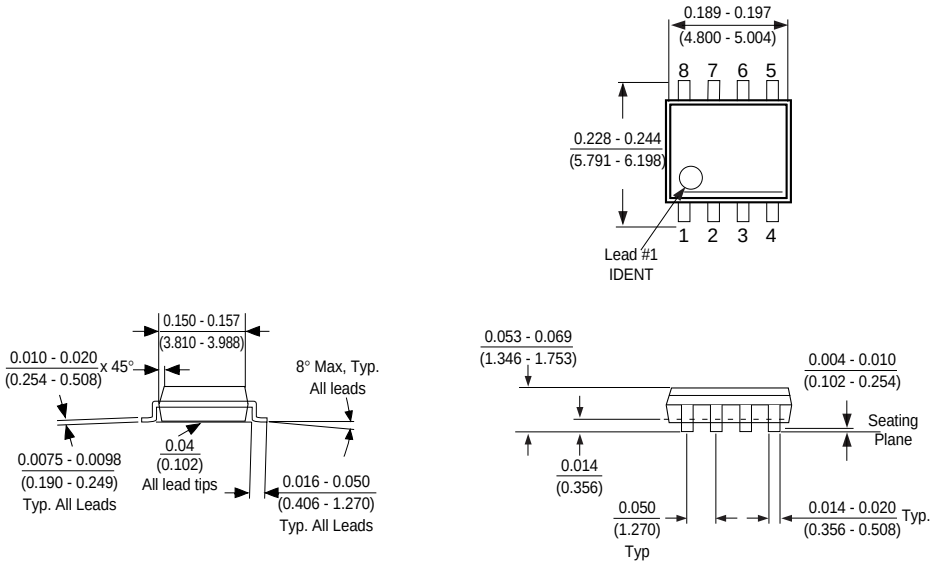
Typical System Configuration (Figure 11)



DS500078-21

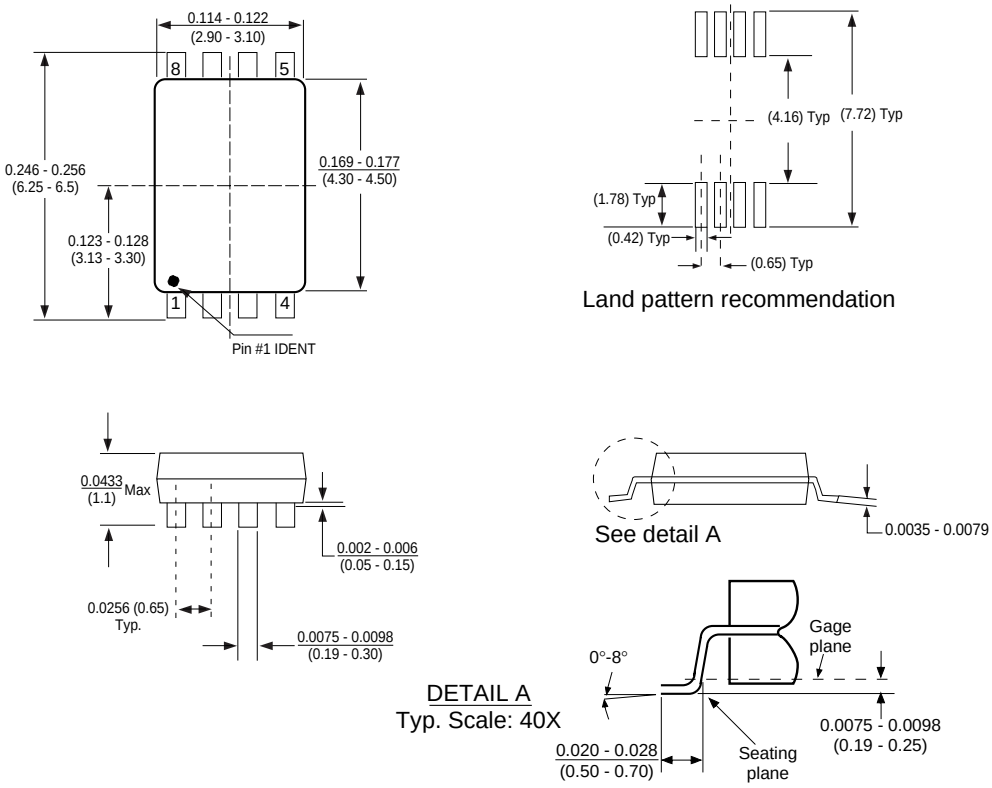
Note: Due to open drain configuration of SDA, a bus-level resistor is called for (Typical value = 4.7Ω)

Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin Molded Small Outline Package (M8)
Order Number NM34W02LM8/LZM8
Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted



Notes: Unless otherwise specified
1. Reference JEDEC registration MO153. Variation AA. Dated 7/93

8-Pin Molded TSSOP, JEDEC (MT8)
Order Number NM34W02LMT8/LZMT8
Package Number MTC08

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

March 1999

NM93C06
256-Bit Serial CMOS EEPROM (MICROWIRE™ Bus Interface)

General Description

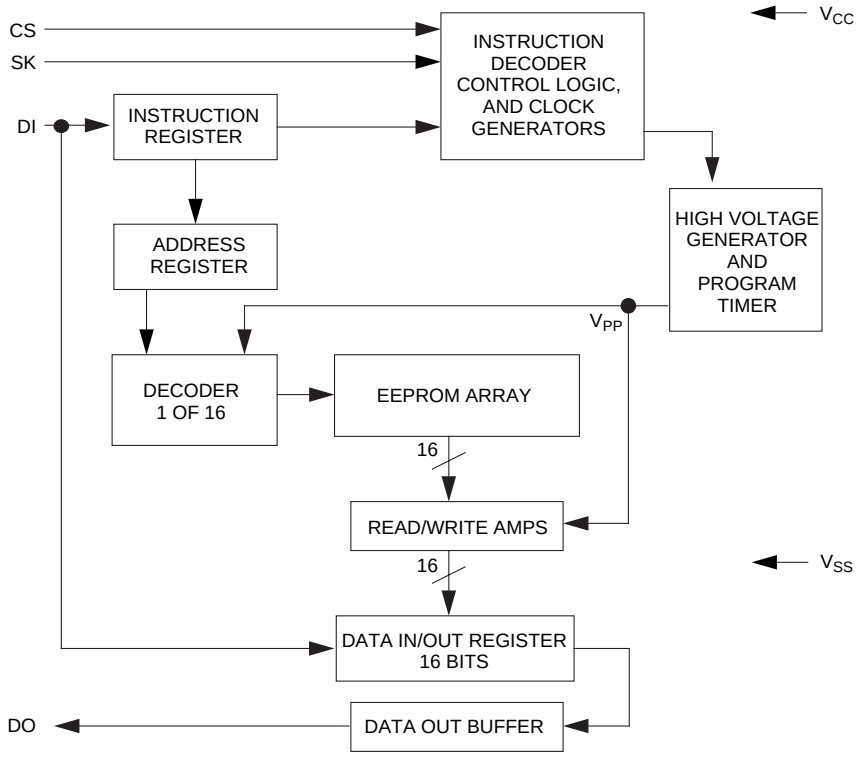
The NM93C06 devices are 256 bits of CMOS non-volatile electrically erasable memory divided into 16 16-bit registers. They are fabricated using Fairchild Semiconductor's floating-gate CMOS process for high reliability, high endurance and low power consumption. These memory devices are available in an 8-pin SOIC or 8-pin TSSOP package for small space considerations.

The serial interface that operates these EEPROMs is MICROWIRE compatible for simple interface to standard microcontrollers and microprocessors. There are 7 instructions which control this device: Read, Write Enable, Erase, Erase All, Write, Write All, and Write Disable. The ready/busy status is available on the DO pin to indicate the completion of a programming cycle.

Features

- Device status during programming mode
- Typical active current of 200µA
  10µA standby current typical
  1µA standby current typical (L)
  0.1µA standby current typical (LZ)
- No erase required before write
- Reliable CMOS floating gate technology
- 2.7V to 5.5V operation in all modes
- MICROWIRE compatible serial I/O
- Self-timed programming cycle
- 40 years data retention
- Endurance: 1,000,000 data changes
- Packages available: 8-pin SO, 8-pin DIP, 8-pin TSSOP

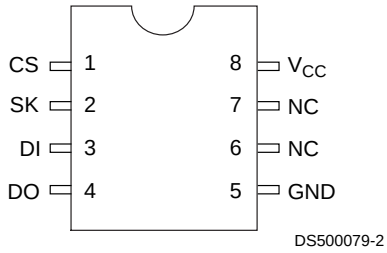
Block Diagram



DS500079-1

Connection Diagrams

Dual-In-Line Package (N),
8-Pin SO (M8) and 8-Pin TSSOP (MT8)



Top View
See Package Number
N08E, M08A and MTC08

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply

Ordering Information

NM	93	C	XX	LZ	E	XX		Letter	Description
							Package	N	8-Pin DIP
								M8	8-Pin SO8
								MT8	8-Pin TSSOP
							Temp. Range	None	0 to 70°C
								V	-40 to +125°C
								E	-40 to +85°C
							Voltage Operating Range	Blank	4.5V to 5.5V
								L	2.7V to 4.5V
								LZ	2.7V to 4.5V and <1µA Standby Current
							Density	06	256 bit
								C	CMOS
								CS	Data protect and sequential read
							Interface	93	MICROWIRE
								NM	**Fairchild Non-Volatile Memory**

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Range

Ambient Operating Temperature	
NM93C06	0°C to +70°C
NM93C06E	-40°C to +85°C
NM93C06V	-40°C to +125°C
Power Supply (V_{CC})	4.5V to 5.5V

Standard V_{CC} (4.5V to 5.5V) DC and AC Electrical Characteristics

Symbol	Parameter	Part Number	Conditions	Min.	Max.	Units
I_{CCA}	Operating Current		CS = V_{IH}, SK = 1MHz		1	mA
I_{CCS}	Standby Current		CS = V_{IL}		50	µA
I_{IL} I_{OL}	Input Leakage Output Leakage		V_{IN} = 0V to V_{CC} (Note 2)		±1	µA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			-0.1 2	0.8 V_{CC} +1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage		I_{OL} = 2.1mA I_{OH} = -400 µA	 2.4	0.4	V V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage		I_{OL} = 10 µA I_{OH} = -10 µA	 V_{CC} -0.2	0.2	V V
f_{SK}	SK Clock Frequency		(Note 3)	0	1	MHz
t_{SKH}	SK High Time	NM93C06 NM93C06E/V		250 300		ns
t_{SKL}	SK Low Time			250		ns
t_{SKS}	SK Setup Time		SK must be at V_{IL} for t_{SKS} before CS goes high	50		ns
t_{CS}	Minimum CS Low Time		(Note 4)	250		ns
t_{CSS}	CS Setup Time			50		ns
t_{DH}	DO Hold Time			70		ns
t_{DIS}	DI Setup Time	NM93C06 NM93C06E/V		100 200		ns
t_{CSH}	CS Hold Time			0		ns
t_{DIH}	DI Hold Time			20		ns
t_{PD1}	Output Delay to "1"				500	ns
t_{PD0}	Output Delay to "0"				500	ns
t_{SV}	CS to Status Valid				500	ns
t_{DF}	CS to DO in TRI-STATE		CS = V_{IL}		100	ns
t_{WP}	Write Cycle Time				10	ms

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Range

Ambient Operating Temperature	
NM93C06L/LZ	0°C to +70°C
NM93C06LE/LZE	-40°C to +85°C
NM93C06LV/LZV	-40°C to +125°C
Power Supply (V_{CC})	2.7V to 4.5V

Low V_{CC} (2.7V to 4.5V) DC and AC Electrical Characteristics

Symbol	Parameter	Part Number	Conditions	Min.	Max.	Units
I_{CCA}	Operating Current		CS = V_{IH}, SK = 250KHz		1	mA
I_{CCS}	Standby Current L LZ		CS = V_{IL}		 10 1	 µA µA
I_{IL} I_{OL}	Input Leakage Output Leakage		V_{IN} = 0V to V_{CC} (Note 2)		±1	µA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			-0.1 0.8 V_{CC}	0.15 V_{CC} V_{CC} +1	V
V_{OL} V_{OH}	Output Low Voltage Output High Voltage		I_{OL} = 10 µA I_{OH} = -10 µA	 0.9 V_{CC}	0.1 V_{CC}	V V
f_{SK}	SK Clock Frequency		(Note 3)	0	250	KHz
t_{SKH}	SK High Time			1		µs
t_{SKL}	SK Low Time			1		µs
t_{SKS}	SK Setup Time		SK must be at V_{IL} for t_{SKS} before CS goes high	0.2		µs
t_{CS}	Minimum CS Low Time		(Note 4)	1		µs
t_{CSS}	CS Setup Time			0.2		µs
t_{DH}	DO Hold Time			70		ns
t_{DIS}	DI Setup Time			0.4		µs
t_{CSH}	CS Hold Time			0		ns
t_{DIH}	DI Hold Time			0.4		µs
t_{PD1}	Output Delay to "1"				2	µs
t_{PD0}	Output Delay to "0"				2	µs
t_{SV}	CS to Status Valid				1	µs
t_{DF}	CS to DO in TRI-STATE		CS = V_{IL}		0.4	µs
t_{WP}	Write Cycle Time				15	ms

Capacitance T_A = 25°C, f = 1 MHz (Note 5)

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical leakage values are in the 20nA range.

Note 3: The shortest allowable SK clock period = $1/f_{SK}$ (as shown under the f_{SK} parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both t_{SKH} and t_{SKL} limits must be observed. Therefore, it is not allowable to set $1/f_{SK} = t_{SKHminimum} + t_{SKLminimum}$ for shorter SK cycle time operation.

Note 4: CS (Chip Select) must be brought low (to V_{IL}) for an interval of t_{CS} in order to reset all internal device registers (device reset) prior to beginning another opcode cycle. (This is shown in the opcode diagram on the following page.)

Note 5: This parameter is periodically sampled and not 100% tested.

AC Test Conditions

V_{CC} Range	V_{IL}/V_{IH} Input Levels	V_{IL}/V_{IH} Timing Level	V_{OL}/V_{OH} Timing Level	I_{OL}/I_{OH}
2.7V ≤ V_{CC} ≤ 5.5V (Extended Voltage Levels)	.03V/1.8V	1.0V	0.8V/1.5V	±10µA
4.5V ≤ V_{CC} ≤ 5.5V (TTL Levels)	0.4V/2.4V	1.0V/2.0V	0.4V/2.4V	-2.1mA/0.4mA
Output Load: 1 TTL Gate (C_L = 100 pF)				

Functional Description

The NM93C06 device has 7 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 6-bit address for register selection.

Read (READ):

The READ instruction outputs serial data on the D0 pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

Write Enable (WEN):

When V_{CC} is applied to the part, it 'powers-up' in the Write Disable (WDS) state. Therefore, all programming modes must be preceded by a Write Enable (WEN) instruction. Once a Write Enable instruction is executed, programming remains enabled until aWrite Disable (WDS) instruction is executed or V_{CC} is removed from the part.

Erase (ERASE):

The ERASE instruction will program all bits in the specified register to the logical "1" state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum time of t_{CS}. DO = logical "0" indicates that the register, at the address specified in the instruction, has been erased, and the part is ready for another instruction.

Write (WRITE):

The WRITE instruction is followed by the address and 16 bits of data to be written into the specified address. After the last bit of data is put in the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. The D0 pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of t_{CS}. D0 = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Erase All (ERAL):

The ERAL instruction will simultaneously program all registers in the memory array and set each bit to the logical "1" state. The Erase All cycle is identical to the ERASE cycle except for the different op-code. As in the ERASE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval.

Write All (WRALL):

The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval.

Write Disable (WDS):

To protect against accidental data disturb, the WDS instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

Note: The Fairchild CMOS EEPROMs do not require an "ERASE" or "ERASE ALL" operation prior to the "WRITE" and "WRITE ALL" instructions. The "ERASE" and "ERASE ALL" instructions are included to maintain compatibility with earlier technology EEPROMs.

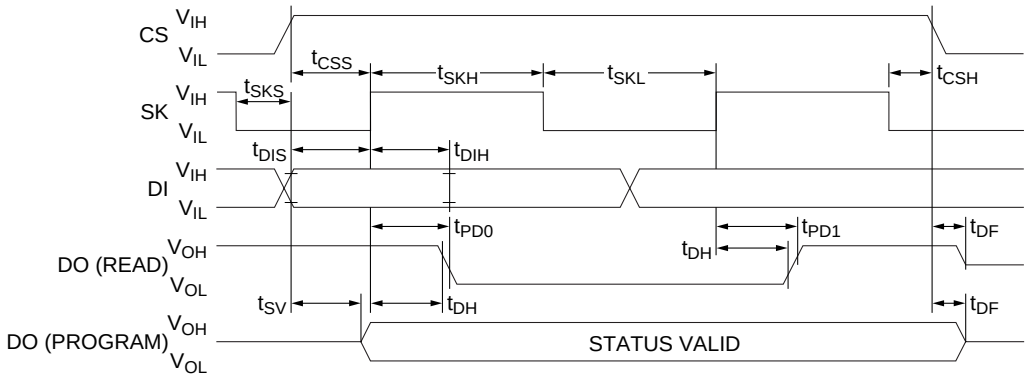
Instruction Set for the NM93C06

Instruction	SB	Op. Code	Address	Data	Comments
READ	1	10	00 A3 A2 A1 A0		Reads data stored in memory, at specified address.
WEN	1	00	11xxxx		Write enable must precede all programming modes.
ERASE	1	11	00 A3 A2 A1 A0		Erase selected register.
WRITE	1	01	00 A3 A2 A1 A0	D15-D0	Writes selected register.
ERAL	1	00	10xxxx		Erases all registers.
WRALL	1	00	01xxxx	D15-D0	Writes all registers.
WDS	1	00	00xxxx		Disables all programming instructions.

Note: Address bits A5 and A4 should be set to '0' for READ, ERASE and WRITE instructions.

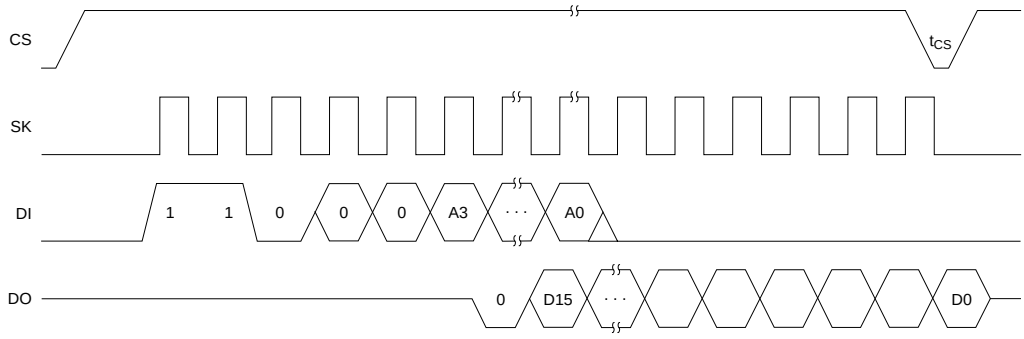
Timing Diagrams

Synchronous Data Timing



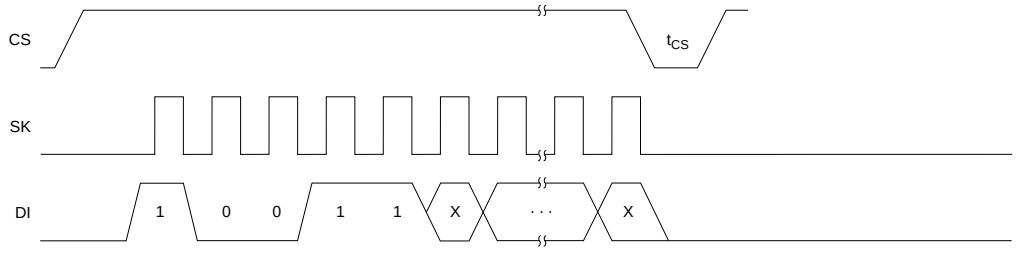
DS500079-4

READ



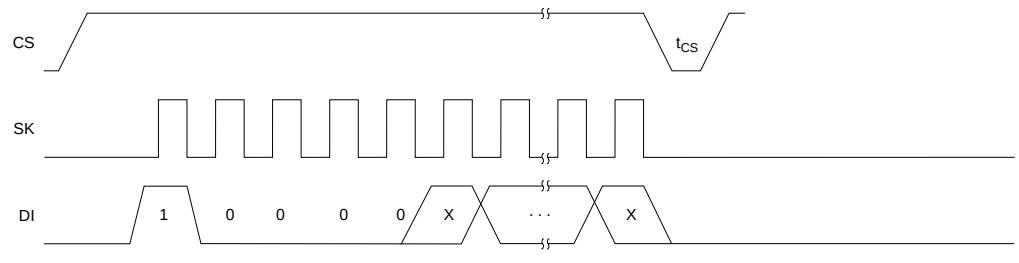
DS500079-5

WEN



DS500079-6

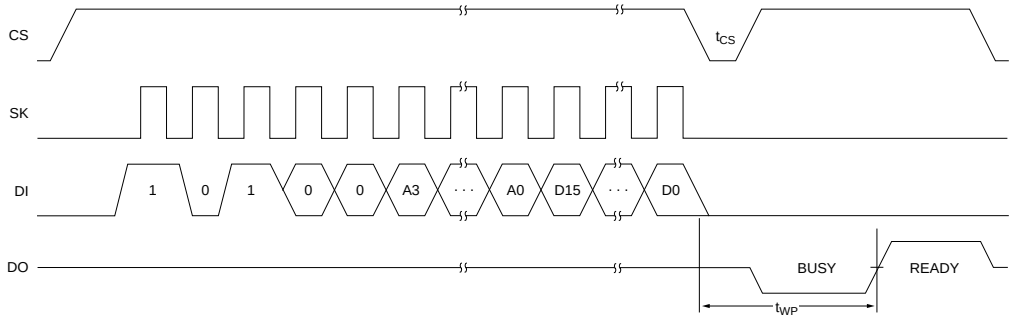
WDS



DS500079-7

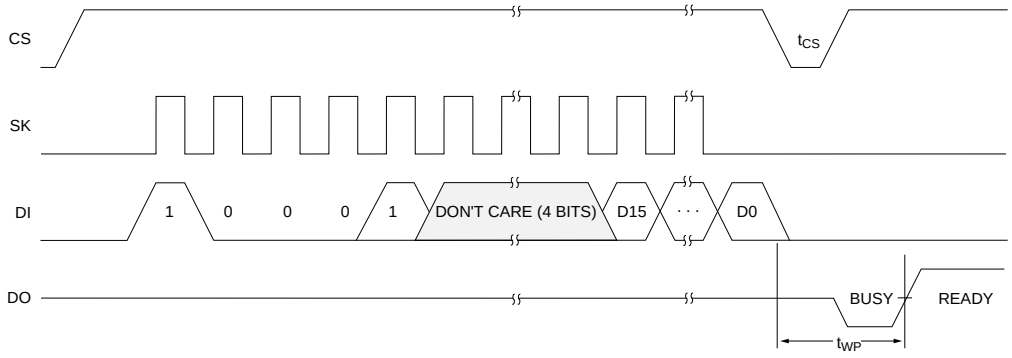
Timing Diagrams (Continued)

WRITE



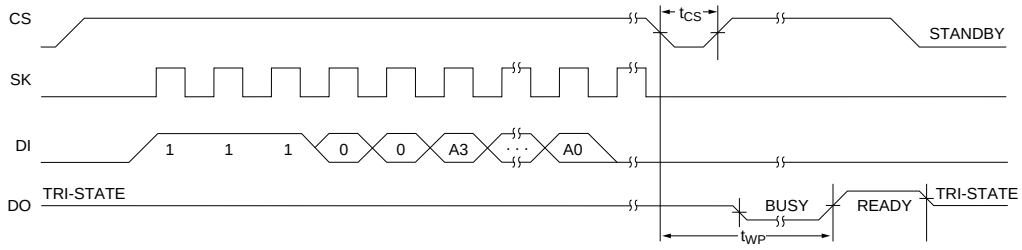
DS500079-8

WRALL



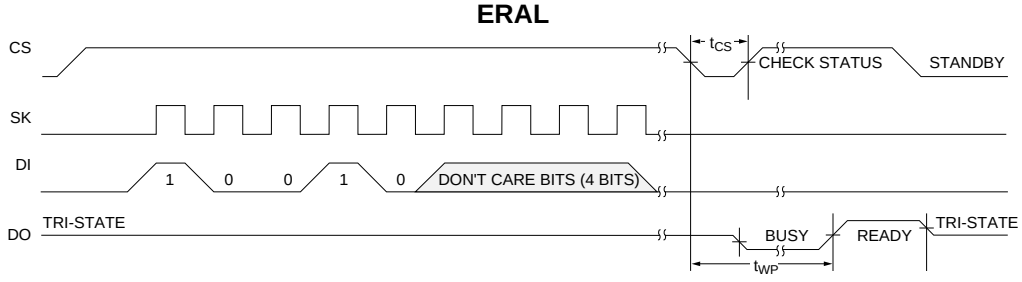
DS500079-9

ERASE



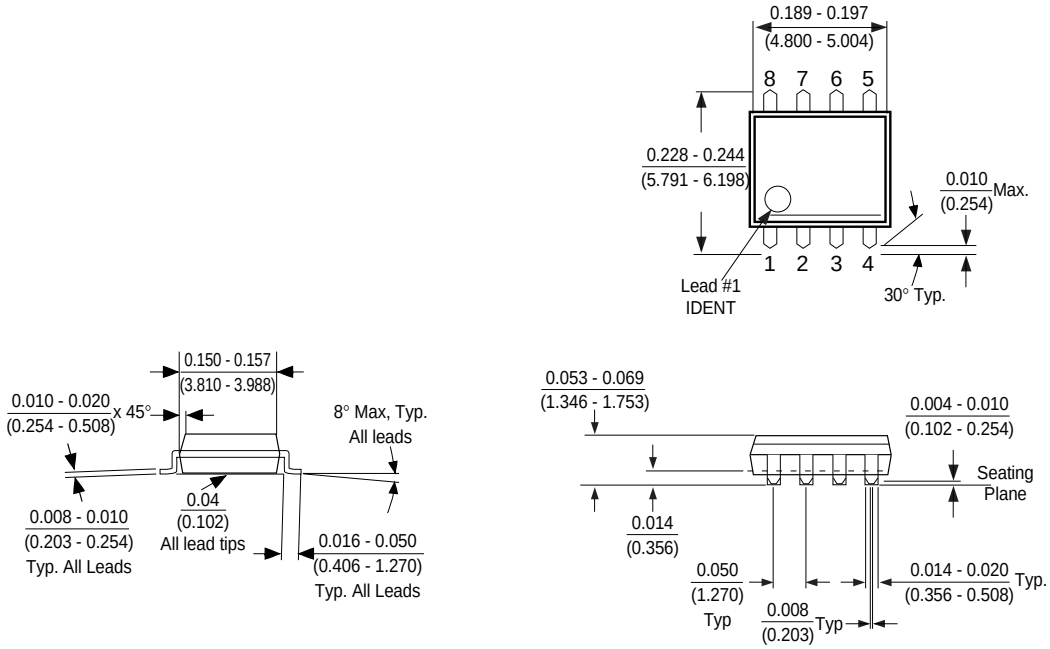
DS500079-10

ERAL

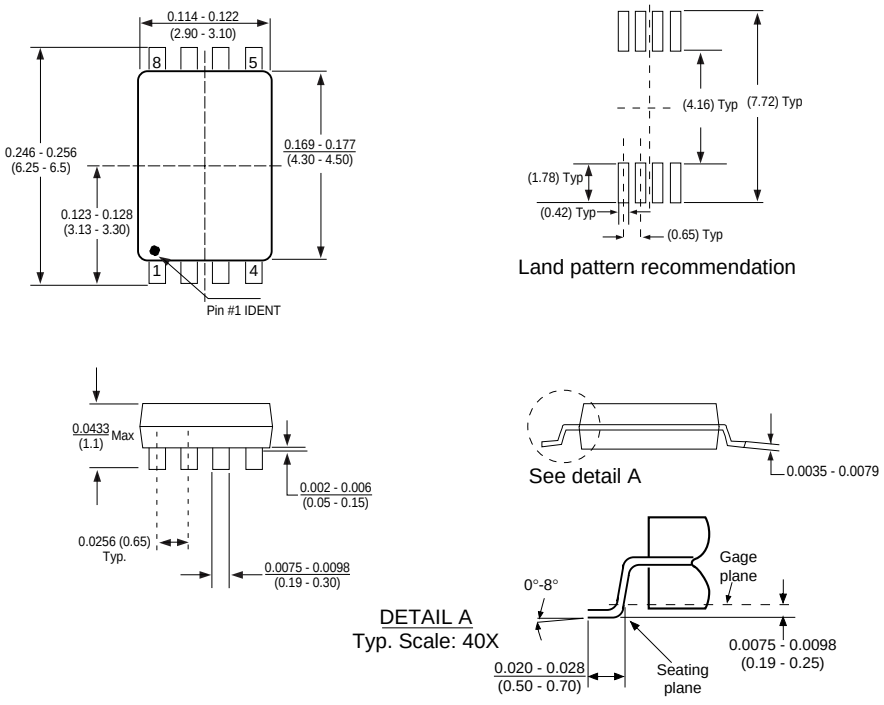


DS500079-11

Physical Dimensions inches (millimeters) unless otherwise noted



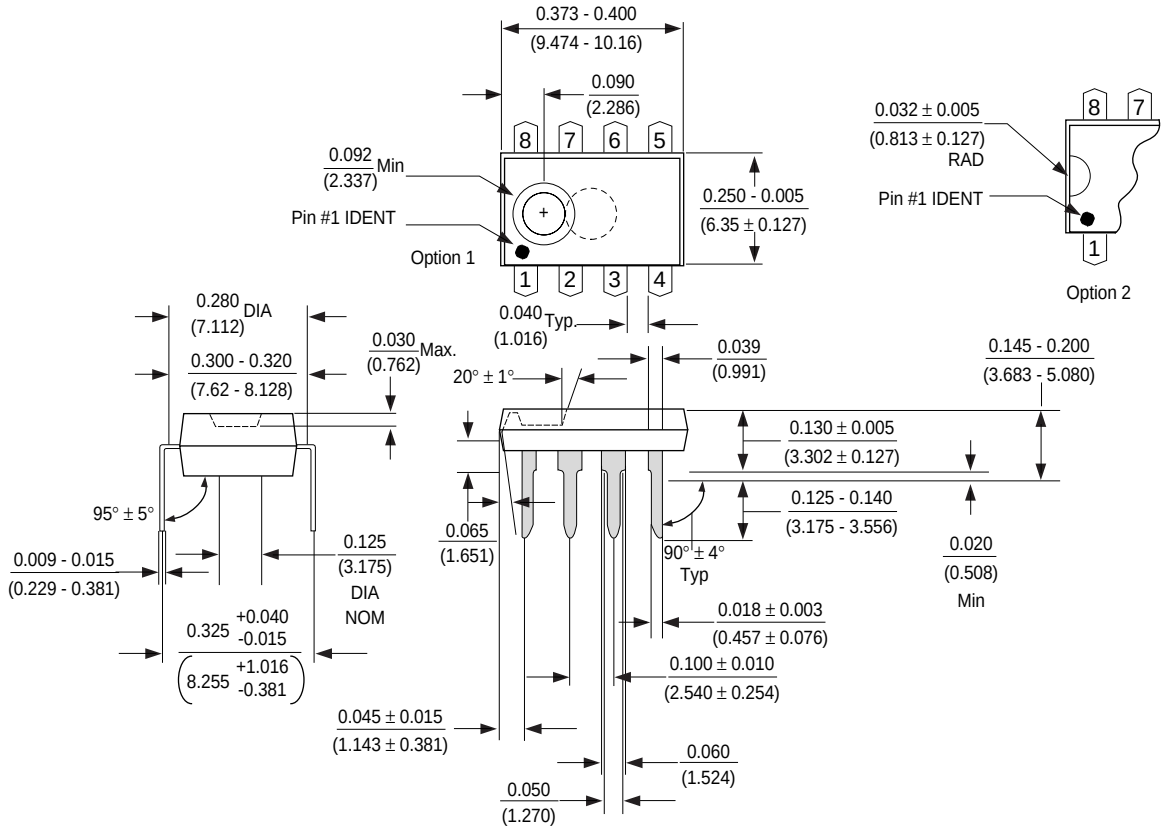
Molded Small Out-Line Package (M8)
Package Number M08A



Notes: Unless otherwise specified
1. Reference JEDEC registration MO153. Variation AA. Dated 7/93

8-Pin Molded TSSOP, JEDEC (MT8)
Package Number MTC08

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Package Number N08E

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

March 1999

NM93C46
1K-Bit Serial CMOS EEPROM (MICROWIRE™ Bus Interface)

General Description

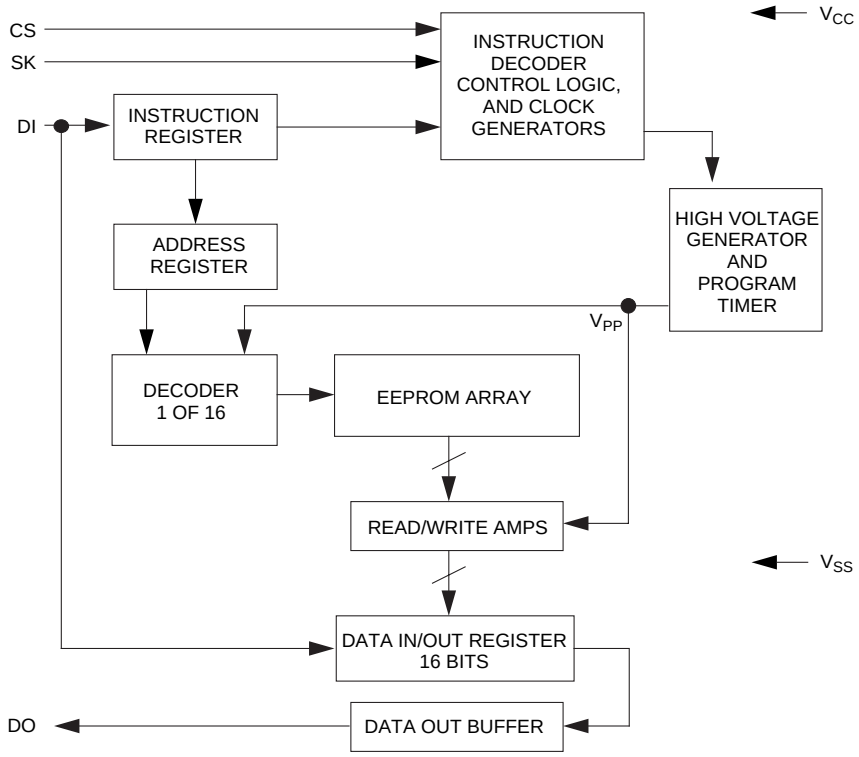
The NM93C46 devices are 1024 bits of CMOS non-volatile electrically erasable memory divided into 64 16-bit registers. They are fabricated using Fairchild Semiconductor's floating-gate CMOS process for high reliability, high endurance and low power consumption. These memory devices are available in an 8-pin SOIC or 8-pin TSSOP package for small space considerations.

The serial interface that operates these EEPROMs is MICROWIRE compatible for simple interface to standard microcontrollers and microprocessors. There are 7 instructions which control this device: Read, Write Enable, Erase, Erase All, Write, Write All, and Write Disable. The ready/busy status is available on the DO pin to indicate the completion of a programming cycle.

Features

- Device status during programming mode
- Typical active current of 200µA
  10µA standby current typical
  1µA standby current typical (L)
  0.1µA standby current typical (LZ)
- No erase required before write
- Reliable CMOS floating gate technology
- 2.7V to 5.5V operation in all modes
- MICROWIRE compatible serial I/O
- Self-timed programming cycle
- 40 years data retention
- Endurance: 1,000,000 data changes
- Packages available: 8-pin SO, 8-pin DIP, 8-pin TSSOP

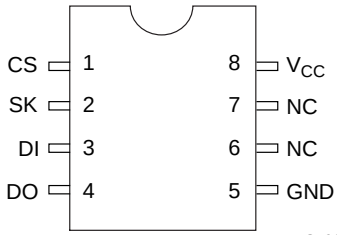
Block Diagram



DS500080-1

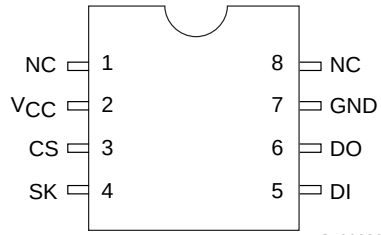
Connection Diagrams

Dual-In-Line Package (N), 8-Pin SO (M8) and 8-Pin TSSOP (MT8)



DS500080-2

Rotated Die (93C46T)



DS500080-12

Top View
See Package Number N08E, M08A and MTC08

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply

Ordering Information

NM 93 C XX T LZ E XX

	Letter	Description
Package	N	8-Pin DIP
	M8	8-Pin SO8
	MT8	8-Pin TSSOP
Temp. Range	None	0 to 70°C
	V	-40 to +125°C
	E	-40 to +85°C
Voltage Operating Range	Blank	4.5V to 5.5V
	L	2.7V to 4.5V
	LZ	2.7V to 4.5V and <1µA Standby Current
	Blank	Normal Pin Out
	T	Rotated Die Pin Out
Density	46	1K
	C	CMOS
	CS	Data protect and sequential read
Interface	93	MICROWIRE
	NM	**Fairchild Non-Volatile Memory**

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Range

Ambient Operating Temperature	
NM93C46	0°C to +70°C
NM93C46E	-40°C to +85°C
NM93C46V	-40°C to +125°C
Power Supply (V_{CC})	4.5V to 5.5V

Standard V_{CC} (4.5V to 5.5V) DC and AC Electrical Characteristics

Symbol	Parameter	Part Number	Conditions	Min.	Max.	Units
I_{CCA}	Operating Current		CS = V_{IH}, SK = 1MHz		1	mA
I_{CCS}	Standby Current		CS = V_{IL}		50	µA
I_{IL} I_{OL}	Input Leakage Output Leakage		V_{IN} = 0V to V_{CC} (Note 2)		±1	µA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			-0.1 2	0.8 V_{CC} +1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage		I_{OL} = 2.1mA I_{OH} = -400 µA	 2.4	0.4	V V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage		I_{OL} = 10 µA I_{OH} = -10 µA	 V_{CC} -0.2	0.2	V V
f_{SK}	SK Clock Frequency		(Note 3)	0	1	MHz
t_{SKH}	SK High Time	NM93C46 NM93C46E/V		250 300		ns
t_{SKL}	SK Low Time			250		ns
t_{SKS}	SK Setup Time		SK must be at V_{IL} for t_{SKS} before CS goes high	50		ns
t_{CS}	Minimum CS Low Time		(Note 4)	250		ns
t_{CSS}	CS Setup Time			50		ns
t_{DH}	DO Hold Time			70		ns
t_{DIS}	DI Setup Time	NM93C46 NM93C46E/V		100 200		ns
t_{CSH}	CS Hold Time			0		ns
t_{DIH}	DI Hold Time			20		ns
t_{PD1}	Output Delay to "1"				500	ns
t_{PD0}	Output Delay to "0"				500	ns
t_{SV}	CS to Status Valid				500	ns
t_{DF}	CS to DO in TRI-STATE		CS = V_{IL}		100	ns
t_{WP}	Write Cycle Time				10	ms

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Range

Ambient Operating Temperature	
NM93C46L/LZ	0°C to +70°C
NM93C46LE/LZE	-40°C to +85°C
NM93C46LV/LZV	-40°C to +125°C
Power Supply (V_{CC})	2.7V to 4.5V

Low V_{CC} (2.7V to 4.5V) DC and AC Electrical Characteristics

Symbol	Parameter	Part Number	Conditions	Min.	Max.	Units
I_{CCA}	Operating Current		CS = V_{IH}, SK = 250KHz		1	mA
I_{CCS}	Standby Current L LZ		CS = V_{IL}		 10 1	 µA µA
I_{IL} I_{OL}	Input Leakage Output Leakage		V_{IN} = 0V to V_{CC} (Note 2)		±1	µA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			-0.1 0.8 V_{CC}	0.15 V_{CC} V_{CC} +1	V
V_{OL} V_{OH}	Output Low Voltage Output High Voltage		I_{OL} = 10 µA I_{OH} = -10 µA	 0.9 V_{CC}	0.1 V_{CC}	V V
f_{SK}	SK Clock Frequency		(Note 3)	0	250	KHz
t_{SKH}	SK High Time			1		µs
t_{SKL}	SK Low Time			1		µs
t_{SKS}	SK Setup Time		SK must be at V_{IL} for t_{SKS} before CS goes high	0.2		µs
t_{CS}	Minimum CS Low Time		(Note 4)	1		µs
t_{CSS}	CS Setup Time			0.2		µs
t_{DH}	DO Hold Time			70		ns
t_{DIS}	DI Setup Time			0.4		µs
t_{CSH}	CS Hold Time			0		ns
t_{DIH}	DI Hold Time			0.4		µs
t_{PD1}	Output Delay to "1"				2	µs
t_{PD0}	Output Delay to "0"				2	µs
t_{SV}	CS to Status Valid				1	µs
t_{DF}	CS to DO in TRI-STATE		CS = V_{IL}		0.4	µs
t_{WP}	Write Cycle Time				15	ms

Capacitance T_A = 25°C, f = 1 MHz (Note 5)

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

AC Test Conditions

V_{CC} Range	V_{IL}/V_{IH} Input Levels	V_{IL}/V_{IH} Timing Level	V_{OL}/V_{OH} Timing Level	I_{OL}/I_{OH}
2.7V ≤ V_{CC} ≤ 5.5V (Extended Voltage Levels)	.03V/1.8V	1.0V	0.8V/1.5V	±10µA
4.5V ≤ V_{CC} ≤ 5.5V (TTL Levels)	0.4V/2.4V	1.0V/2.0V	0.4V/2.4V	-2.1mA/0.4mA
Output Load: 1 TTL Gate (C_L = 100 pF)				

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical leakage values are in the 20nA range.

Note 3: The shortest allowable SK clock period = $1/f_{SK}$ (as shown under the f_{SK} parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both t_{SKH} and t_{SKL} limits must be observed. Therefore, it is not allowable to set $1/f_{SK} = t_{SKHminimum} + t_{SKLminimum}$ for shorter SK cycle time operation.

Note 4: CS (Chip Select) must be brought low (to V_{IL}) for an interval of t_{CS} in order to reset all internal device registers (device reset) prior to beginning another opcode cycle. (This is shown in the opcode diagram on the following page.)

Note 5: This parameter is periodically sampled and not 100% tested.

Functional Description

The NM93C46 device has 7 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 6-bit address for register selection.

Read (READ):

The READ instruction outputs serial data on the D0 pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

Write Enable (WEN):

When V_{CC} is applied to the part, it 'powers-up' in the Write Disable (WDS) state. Therefore, all programming modes must be preceded by a Write Enable (WEN) instruction. Once a Write Enable instruction is executed, programming remains enabled until aWrite Disable (WDS) instruction is executed or V_{CC} is removed from the part.

Erase (ERASE):

The ERASE instruction will program all bits in the specified register to the logical "1" state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum time of t_{CS}. DO = logical "0" indicates that the register, at the address specified in the instruction, has been erased, and the part is ready for another instruction.

Write (WRITE):

The WRITE instruction is followed by the address and 16 bits of data to be written into the specified address. After the last bit of data is put in the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. The D0 pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of t_{CS}. D0 = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Erase All (ERAL):

The ERAL instruction will simultaneously program all registers in the memory array and set each bit to the logical "1" state. The Erase All cycle is identical to the ERASE cycle except for the different op-code. As in the ERASE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval.

Write All (WRALL):

The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval.

Write Disable (WDS):

To protect against accidental data disturb, the WDS instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

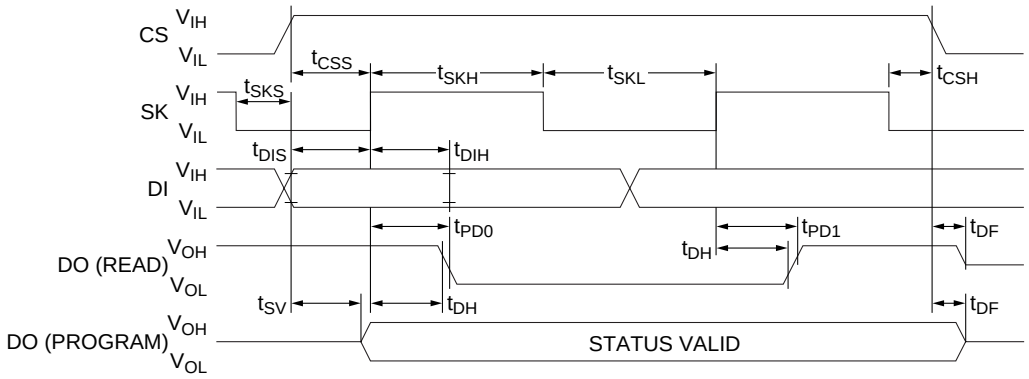
Note: The Fairchild CMOS EEPROMs do not require an "ERASE" or "ERASE ALL" operation prior to the "WRITE" and "WRITE ALL" instructions. The "ERASE" and "ERASE ALL" instructions are included to maintain compatibility with earlier technology EEPROMs.

Instruction Set for the NM93C46

Instruction	SB	Op. Code	Address	Data	Comments
READ	1	10	A5-A0		Reads data stored in memory, at specified address.
WEN	1	00	11xxxx		Write enable must precede all programming modes.
ERASE	1	11	A5-A0		Erase selected register.
WRITE	1	01	A5-A0	D15-D0	Writes selected register.
ERAL	1	00	10xxxx		Erases all registers.
WRALL	1	00	01xxxx	D15-D0	Writes all registers.
WDS	1	00	00xxxx		Disables all programming instructions.

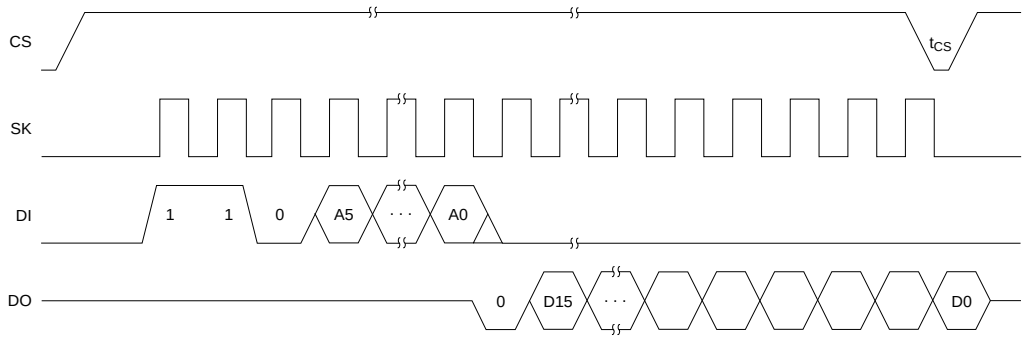
Timing Diagrams

Synchronous Data Timing



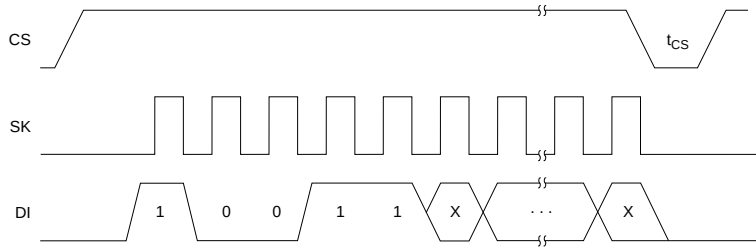
DS500080-4

READ



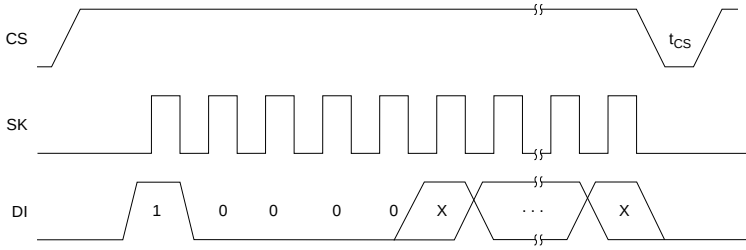
DS500080-5

WEN



DS500080-6

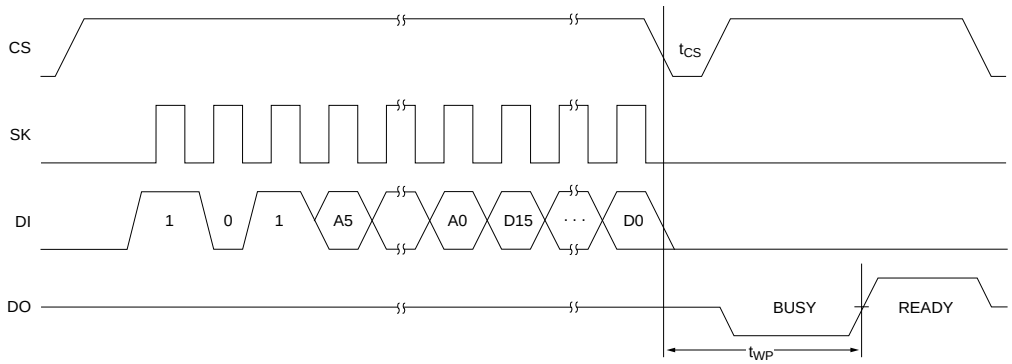
WDS



DS500080-7

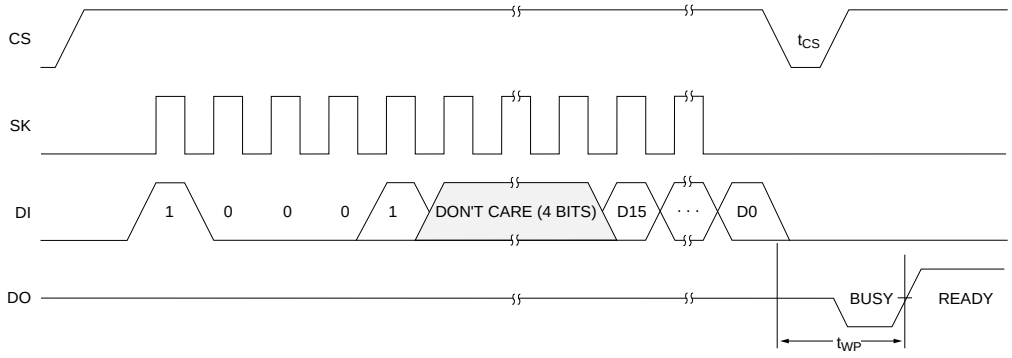
Timing Diagrams (Continued)

WRITE



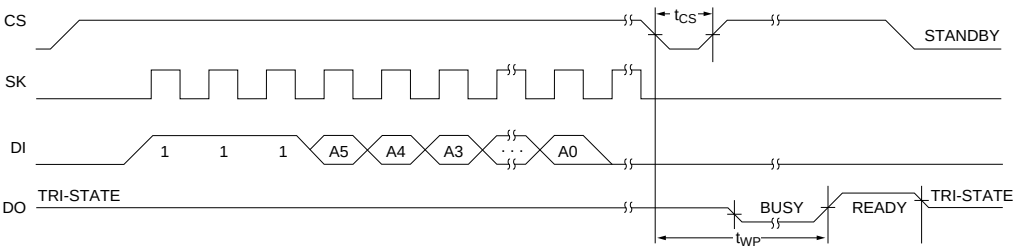
DS500080-8

WRALL



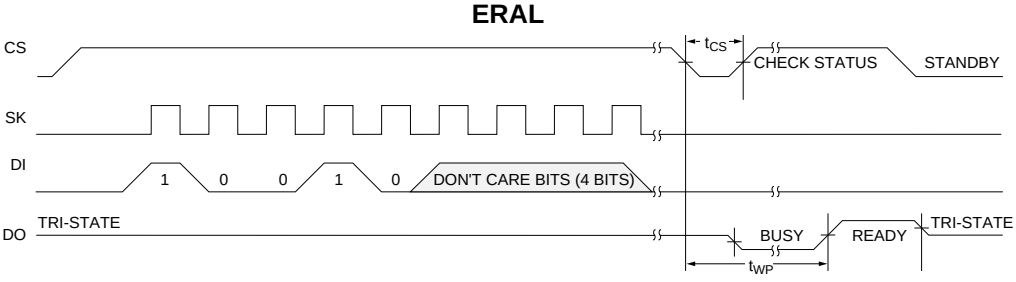
DS500080-9

ERASE



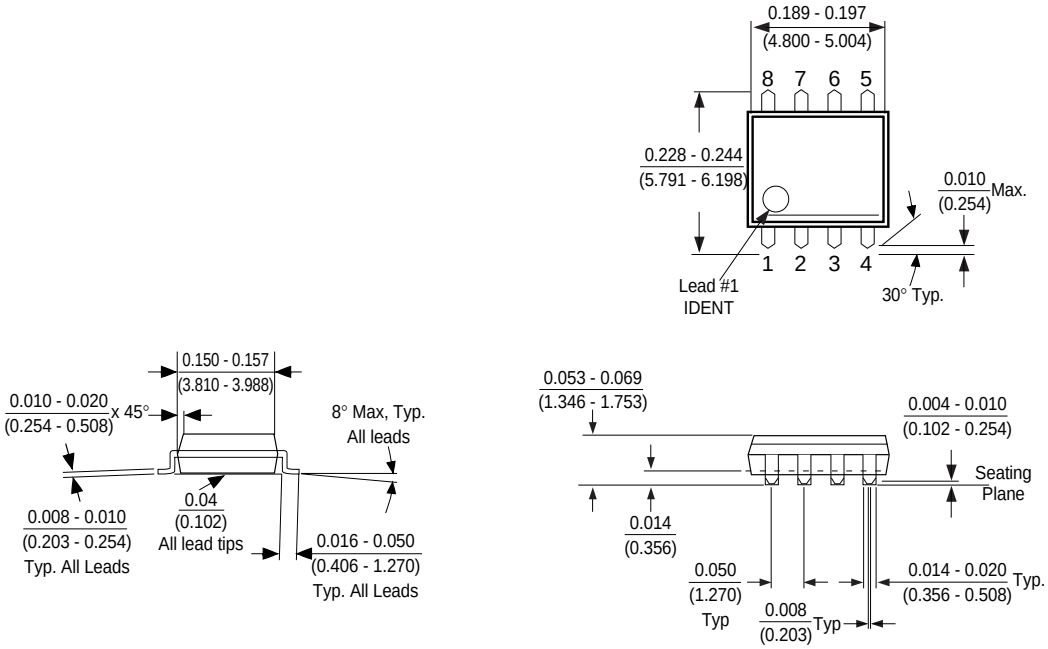
DS500080-10

ERAL

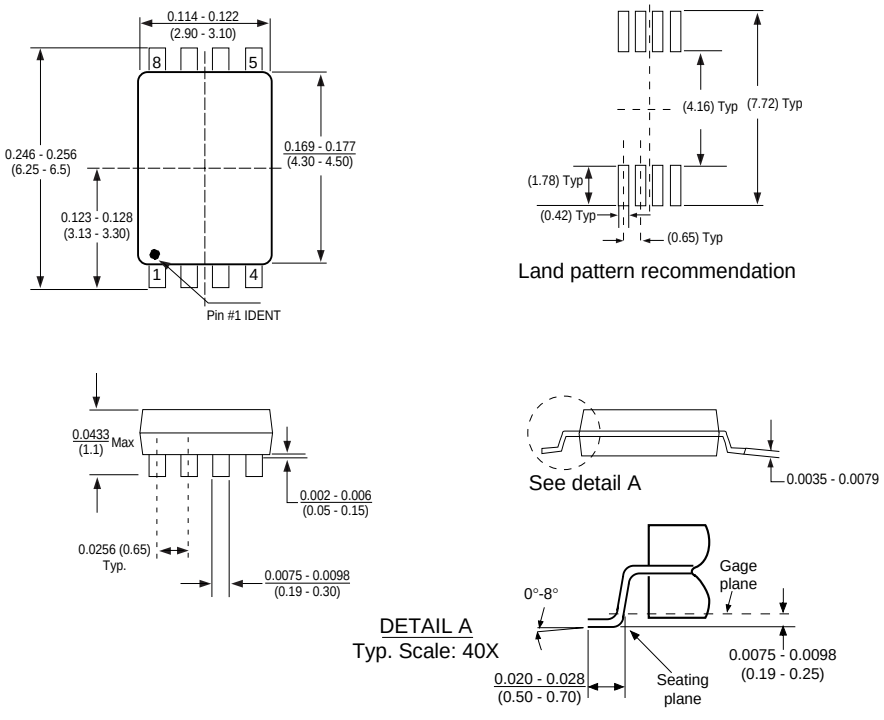


DS500080-11

Physical Dimensions inches (millimeters) unless otherwise noted



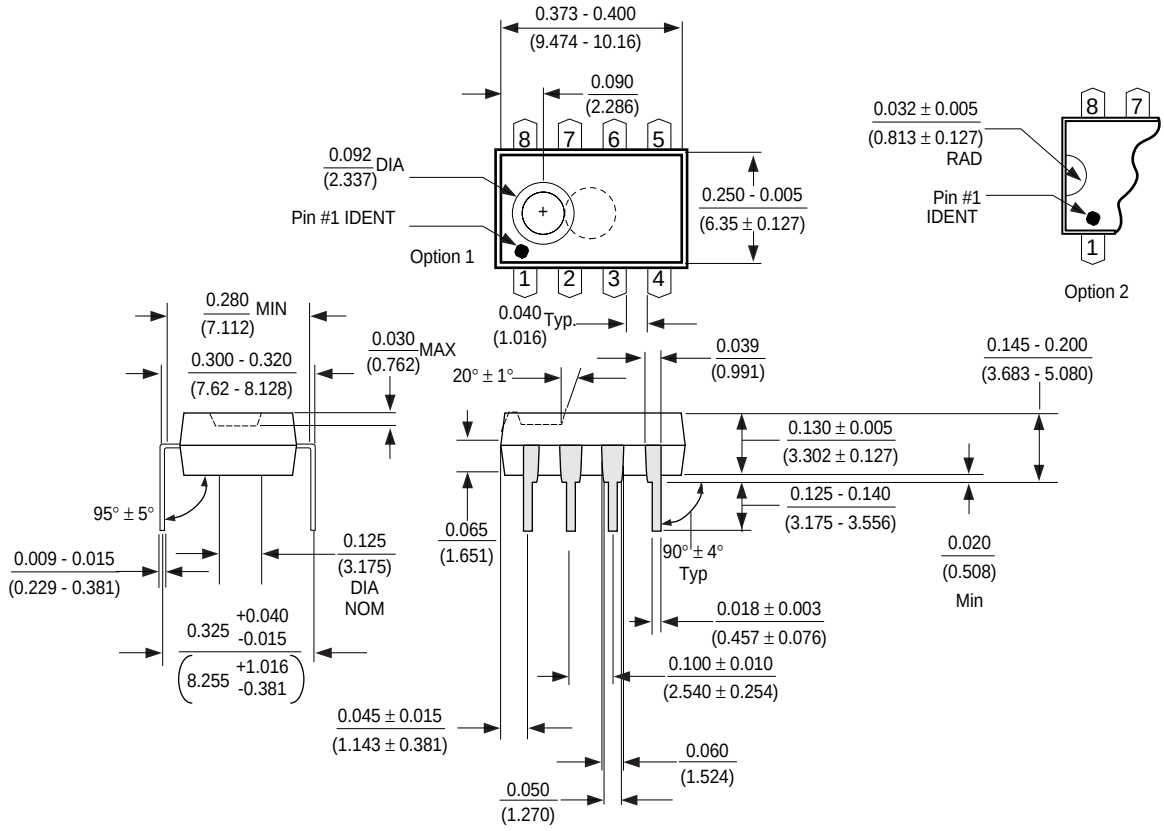
Molded Small Out-Line Package (M8)
Package Number M08A



Notes: Unless otherwise specified
1. Reference JEDEC registration MO153. Variation AA. Dated 7/93

8-Pin Molded TSSOP, JEDEC (MT8)
Package Number MTC08

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Package Number N08E

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

March 1999

NM93C46A
1K-Bit Serial CMOS EEPROM (MICROWIRE™ Synchronous Bus)

General Description

The NM93C46A is 1,024 bits of CMOS nonvolatile, electrically erasable memory available as either 64 16-bit registers or 128 8-bit registers. (The organization is determined by the status of the ORG input.) This is fabricated using Fairchild Semiconductor's floating gate CMOS process for high reliability, high endurance, and low power consumption. The NM93C46A is available in 8-pin DIP, SO and TSSOP packages for space considerations.

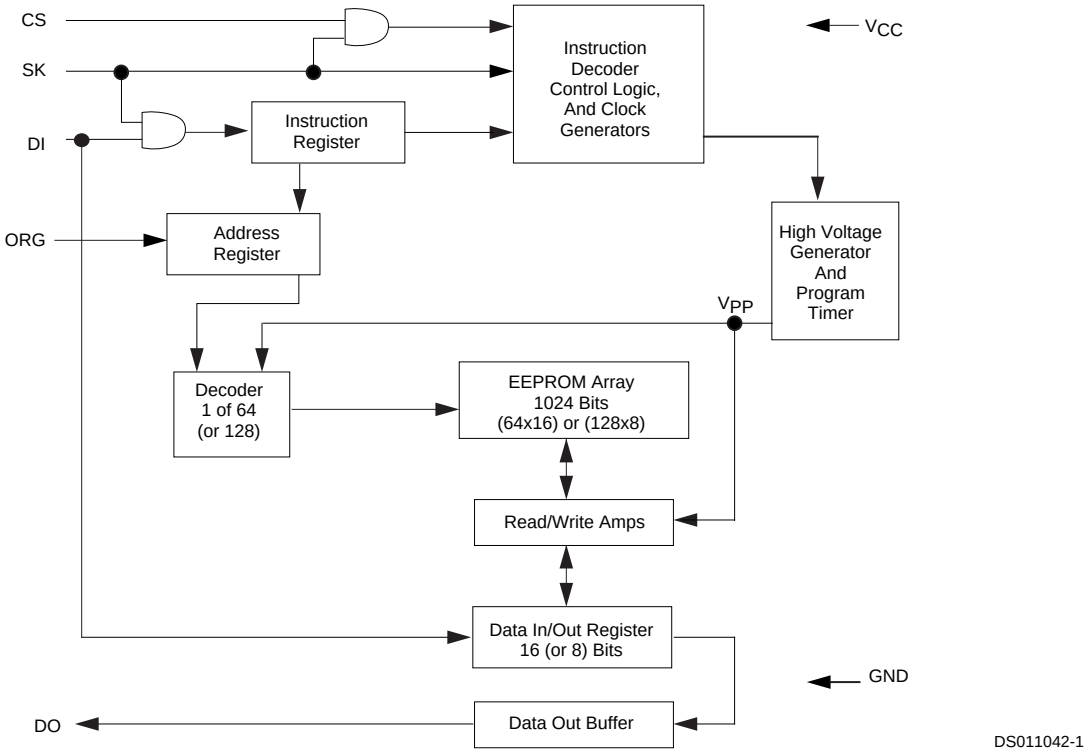
The EEPROM is MICROWIRE compatible for simple interfacing to a wide variety of microcontrollers and microprocessors. There are 7 instructions that operate the NM93C46A: Read, Erase/Write Enable, Erase, Write, Erase/Write Disable, Write All, and Erase All.

The NM93C46A defaults to the 64 x 16 configuration if the ORG pin (Pin 6) is left floating, as it is internally pulled up to V_{CC}.

Features

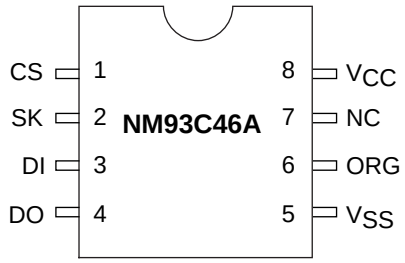
- 2.7V to 5.5V operation in all modes
- Typical active current 200μA
  10 μA standby current typical
  1 μA standby current typical (L)
  0.1 μA standby current typical (LZ)
- Self-timed programming cycle
- Device status indication during programming mode
- No erase required before write
- Reliable CMOS floating gate technology
- MICROWIRE compatible serial I/O
- 40 years data retention
- Endurance: 1,000,000 data changes
- Packages available: 8-pin TSSOP, 8-pin SO, 8-pin DIP

Block Diagram



Connection Diagrams

Dual-In-Line Package (N), 8-Pin SO Package (M8) and 8-Pin TSSOP Package (MT8)

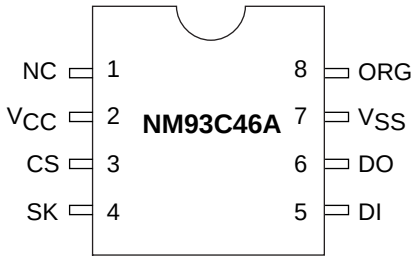


DS011042-2

Top View

See Package Number N08E, M08A and MTC08

Rotated Die (93C46AT)



Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V_{SS}	Ground
ORG	Memory Organizational Select
NC	No Connect
V_{CC}	Positive Power Supply

Ordering Information

NM 93 C XX A T LZ E XX

		Letter	Description
Package		N	8-Pin DIP
		M8	8-Pin SO8
		MT8	8-Pin TSSOP
Temp. Range		None	0 to 70°C
		V	-40 to +125°C
		E	-40 to +85°C
Voltage Operating Range		Blank	4.5V to 5.5V
		L	2.7V to 4.5V
		LZ	2.7V to 4.5V and <1µA Standby Current
		Blank	Normal Pin Out
		T	Rotated Die Pin Out
		A	x8 or x16 Configuration
Density		46	1K
		C	CMOS
		CS	Data protect and sequential read
Interface		93	MICROWIRE
		NM	**Fairchild Non-Volatile Memory**

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltages: with Respect to Ground	V_{CC} +1 to -0.3V
Lead Temperature (Soldering, 10 Seconds)	+300°C
EDS Rating	2000V

Operating Range

Ambient Operating Temperature	
NM93C46A	0°C to +70°C
NM93C46AE	-40°C to +85°C
NM93C46AV	-40°C to +125°C
Power Supply (V_{CC})	4.5V to 5.5V

Standard V_{CC} (4.5V to .5V) DC and AC Electrical Characteristics

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CCA}	Operating Current		CS = V_{IH} ,SK=1 MHz		1	mA
I_{CCS}	Standby Current		CS = 0V, ORG = V_{CC} or NC		50	µA
I_{IL}	Input Leakage		V_{IN} = 0V to V_{CC} (Note 2)	-1	1	µA
I_{ILO}	Input Leakage ORG Pin		ORG tied to V_{CC} ORG tied to V_{SS} (Note 3)	-1 -2.5	1 2.5	µA
I_{OL}	Output Leakage		V_{IN} = 0V to V_{CC}	-1	1	µA
V_{IL}	Input Low Voltage			-0.1	0.8	V
V_{IH}	Input High Voltage			2	V_{CC} +1	V
V_{OL1}	Output Low Voltage		I_{OL} = 2.1 mA		0.4	V
V_{OH1}	Output High Voltage		I_{OH} = -400 µA	2.4		V
V_{OL2}	Output Low Voltage		I_{OL} = 10 µA		0.2	V
V_{OH2}	Output High Voltage		I_{OL} = -10 µA	V_{CC} - 0.2		V
f_{SK}	SK Clock Frequency		(Note 4)	0	1	MHz
t_{SKH}	SK High Time	NM93C46A		250		ns
		NM93C46AE/V		300		
t_{SKL}	SK Low Time			250		ns
t_{SKS}	SK Setup Time		SK must be at V_{IL} for t_{SKS} before CS goes high	50		ns
t_{CS}	Minimum CS		(Note 5)	250		ns
t_{CSS}	CS Setup Time			50		ns
t_{DH}	DO Hold Time			70		ns
t_{DIS}	DI Setup Time	NM93C46A		100		ns
		NM93C46AE/V		200		
t_{CSH}	CS Hold Time			0		ns
t_{DIH}	DI Hold Time			20		ns
t_{PD1}	Output Delay to “1”				500	ns
t_{PD0}	Output Delay to “0”				500	ns
t_{SV}	CS to Status Valid				500	ns
t_{DF}	CS to DO in TRI-STATE ®		CS = V_{IL}		100	ns
t_{WP}	Write Cycle Time				10	ms

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Range

Ambient Operating Temperature	
NM93C46AL/LZ	0°C to +70°C
NM93C46ALE/LZE	-40°C to +85°C
NM93C46A LV/LZV	-40°C to +125°C
Power Supply (V_{CC})	2.7V to 4.5V

Low V_{CC} (2.7V to 4.5V) DC and AC Electrical Characteristics

Symbol	Parameter	Part Number	Conditions	Min.	Max.	Units
I_{CCA}	Operating Current		CS = V_{IH}, SK = 250KHz		1	mA
I_{CCS}	Standby Current L LZ		CS = V_{IL}		 10 1	 µA µA
I_{IL}	Input Leakage		V_{IN} = 0V to V_{CC} (Note 2)		±1	µA
I_{ILO}	Input Leakage ORG Pin		ORG tied to V_{CC} ORG tied to V_{SS} (Note 3)	-1 -2.5	1 2.5	µA
I_{OL}	Output Leakage		V_{IN} = 0V to V_{CC}		±1	µA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			-0.1 0.8 V_{CC}	0.15 V_{CC} V_{CC} +1	V
V_{OL} V_{OH}	Output Low Voltage Output High Voltage		I_{OL} = 10 µA I_{OH} = -10 µA	 0.9 V_{CC}	0.1 V_{CC}	V V
f_{SK}	SK Clock Frequency		(Note 4)	0	250	KHz
t_{SKH}	SK High Time			1		µs
t_{SKL}	SK Low Time			1		µs
t_{SKS}	SK Setup Time		SK must be at V_{IL} for t_{SKS} before CS goes high	0.2		µs
t_{CS}	Minimum CS Low Time		(Note 5)	1		µs
t_{CSS}	CS Setup Time			0.2		µs
t_{DH}	DO Hold Time			70		ns
t_{DIS}	DI Setup Time			0.4		µs
t_{CSH}	CS Hold Time			0		ns
t_{DIH}	DI Hold Time			0.4		µs
t_{PD1}	Output Delay to "1"				2	µs
t_{PD0}	Output Delay to "0"				2	µs
t_{SV}	CS to Status Valid				1	µs
t_{DF}	CS to DO in TRI-STATE		CS = V_{IL}		0.4	µs
t_{WP}	Write Cycle Time				15	ms

Capacitance T_A = 25°C, f = 1 MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical leakage values are in the 20 nA range.

Note 3: The ORG pin may draw > 1 µA when in the x8 mode ude to an internal pull-up transistor.

Note 4: The shortest allowable SK clock period = $1/f_{SK}$ (as shown under the f_{SK} f_{SK} parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both t_{SKH} and t_{SKL} limits must be observed. Therefore, it is not allowable to set $1/f_{SK} = t_{SKHminimum} + t_{SKLminimum}$ for shorter SK cycle time operation.

Note 5: CS (Chip Select) must be brought low (to V_{IL}) for an interval of t_{CS} in order to reset all internal device registers (device reset) prior to beginning another opcode cycle. (This is shown in the opcode diagrams in the following pages.)

AC Test Conditions

V_{CC} Range	V_{IL}/V_{IH} Input Levels	V_{IL}/V_{IH} Timing Level	V_{OL}/V_{OH} Timing Level	I_{OL}/I_{OH}
2.7V ≤ V_{CC} ≤ 5.5V (Extended Voltage Levels)	.03V/1.8V	1.0V	0.8V/1.5V	±10µA
4.5V ≤ V_{CC} ≤ 5.5V (TTL Levels)	0.4V/2.4V	1.0V/2.0V	0.4V/2.4V	-2.1mA/0.4mA
Output Load: 1 TTL Gate (C_L = 100 pF)				

MICROWIRE I/O Pin Description

Chip Select (CS):

This pin enables and disables the MICROWIRE device and performs 3 general functions:

1. When in the low state, the MICROWIRE device is disabled and the output tri-stated (high impedance). If this pin is brought high (rising edge active), all internal registers are reset and the device is enabled, allowing MICROWIRE communication via DI/DO pins. To restate, the CS pin must be held high during all device communication and opcode functions. If the CS pin is brought low, all functions will be disabled and reset when CS is brought high again. The exception to this is when a programming cycle is initiated (see 2 and 3). Again, all activity on the CS, DI and DO pins is ignored until CS is brought high.
2. After entering all required opcode and address data, bringing CS low initiates the (asynchronous) programming cycle.
3. When programming is in progress, the Data-Out pin will display the programming status as either BUSY (DO low) or READY (DO high) when CS is brought high. (Again, the output will be tri-stated when CS is low.) To restate, during programming, the CS pin may be brought high and low any number of times to view the programming status without affect the programming operation. Once programming is completed (Output in READY state), the output is 'cleared' (returned to normal tri-state condition) by clocking in a Start Bit. After the Start Bit is clocked in, the output will return to a tri-stated condition. When clocked in, this Start Bit can be the first bit in a command string, or CS can be brought low again to reset all internal circuits.

Serial Clock (SK):

This pin is the clock input (rising edge active) for clocking in all opcodes and data on the DI pin and clocking out all data on the DO pin.However, this pin has no effect on the asynchronous programming cycle (see the CS pin section) as the BUSY/READY status is a function of the CS pin only.

Data-In (DI):

All serial communication ***into*** the device is performed using this input pin (rising edge active). In order to avoid false Start Bits, or related issues, it is advised to keep the DI pin in the low state unless actually clocking in data bits (Start Bit, Opcode, Address or incoming data bits to be programmed). Please note that the first '1' clocked into the device (after CS is brought high) is seen as a Start Bit and the beginning of a serial command string, so caution must be observed when bringing CS high.

Data-Out (DO):

All serial communication **out of** the device (READ opcode) is performed using this output pin (rising edge active) as well as indicating the READY/BUSY status duting the asynchronous programming cycle. Note that, during READ operations, the output data is clocked **out** after the last address bit (A0) is clocked in. If a 3-wire application is required (where DI and DO are tied together), sections in AN-758, or related application notes, must be followed for correct operation.

Organization (ORG):

This pin controls the device architecture (8-bit data word vs. 16-bit data word). If the ORG pin is brought to V_{CC}, the device is configured with a 16-bit data word and if the ORG pin is brought to V_{SS} (Ground), the device is configured with an 8-bit data word (refer to other sections for details of both configurations). If the ORG pin is left floating, the device will default to a 16-bit data word.

Instruction Set for the NM93C46A

ORG Pin Logic	Memory	
	Configuration	# of Address Bits
0	128 x 8	7 Bits
1	64 x 16	6 Bits

64 by 16-Bit Organization (NM93C46A when ORG = V_{CC} or NC)

Instruction	SB	OP-Code 2 Bits	Address 6 Bits	Data 16 Bits	Comments
READ	1	10	A5–A0		Read data stored in selected registers.
EWEN	1	00	11XXXX		Enables programming modes.
EWDS	1	00	00XXXX		Disables all programming modes.
ERASE	1	11	A5–A0		Erases selected register.
WRITE	1	01	A5–A0	D15–D0	Writes data pattern D15–D0 into selected register.
ERAL	1	00	10XXXX		Erases all registers.
WRAL	1	00	01XXXX	D15–D0	Writes data pattern D15–D0 into all registers.

128 by 8-Bit Organization (NM93C46A when ORG = GND)

Instruction	SB	OP-Code 2 Bits	Address 7 Bits	Data 8 Bits	Comments
READ	1	10	A6–A0		Read data stored in selected registers.
EWEN	1	00	11XXXXX		Enables programming modes.
EWDS	1	00	00XXXXX		Disables all programming modes.
ERASE	1	11	A6–A0		Erases selected register.
WRITE	1	01	A6–A0	D7–D0	Writes data pattern D7–D0 into selected register.
ERAL	1	00	10XXXXX		Erases all registers.
WRAL	1	00	01XXXXX	D7–D0	Writes data pattern D7–D0 into all registers.

Functional Description

Programming:

1. Programming is initiated by clocking in the Start Bit, Opcode bits, Address bits and the 8/16 data bits (refer to the ORG pin section).
2. Programming is started by bringing the CS pin low. Once the programming cycle is started, it cannot be stopped. (Bringing V_{CC} low will stop any programming, but will also result in data corruption.)
3. The status of the programming cycle (BUSY or READY) is observed by bringing the CS pin high and observing the output state. If the output is LOW, the device is still programming (BUSY). If the output is HIGH, the programming cycle has been completed and the device is ready for the next operation. Note that the output will be tri-stated each time CS is brought low and the R/B status will be shown each time CS is brought high.
4. After programming, the READY state (output HIGH) can be reset and the output tri-stated by clocking in a single Start Bit. This Start Bit can be the first bit in a command string, or CS can be brought low again to reset all internal circuits. In any case, clocking in a '1' bit will tri-state the output.

Read (READ):

The READ instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a serial-out shift register. A dummy bit (logical 0) precedes the serial data output string. Output data changes are initiated by a low to high transition of SK after the last address bit (A0) is clocked in.

Erase/Write Enable (EWEN):

When V_{CC} is applied to the part, it “powers up” in the Erase/Write Disable (EWDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once an Erase/Write Enable instruction is executed, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} is removed from the part.

Functional Description (Continued)

Erase/Write Disable (EWDS):

To protect against accidental data overwrites, the Erase/Write Disable (EWDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the EVEN and EWDS instructions.

Erase (ERASE):

The ERASE instruction will program all bits in the specified register to the logical “1” state. Please refer to the Programming section for details.

Write (WRITE):

The WRITE instruction is followed by 16 bits of data (or 8 bits of data when using the NM93C46A in the x8 organization) to be written into the specified address. Please refer to the Programming section for details.

Erase All (ERAL):

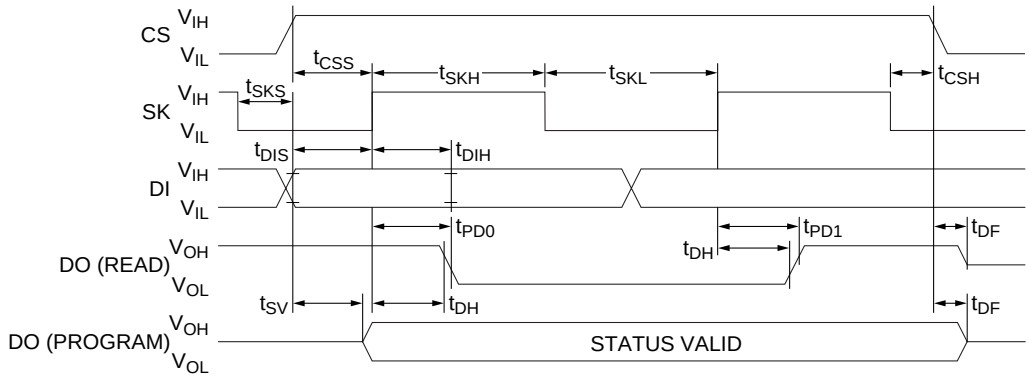
The ERAL instruction will simultaneously program all registers in the memory array to the logical “1” state.

Write All (WRAL):

The WRAL instruction will simultaneously program all registers with the data pattern specified in the instruction.

Timing Diagrams for the NM93C46A

Synchronous Data Timing



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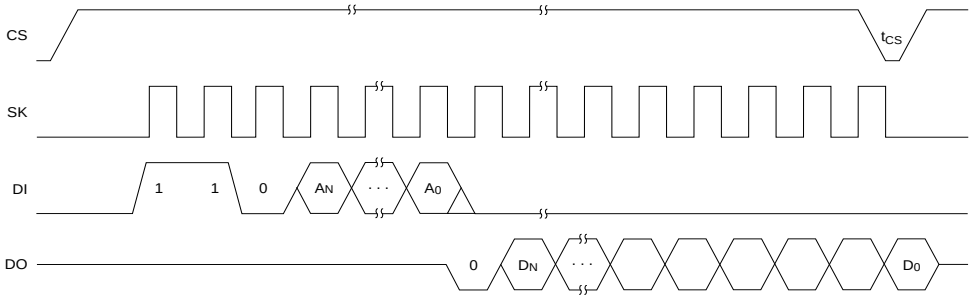
Timing Diagrams for the NM93C46A (Continued)

Key for Timing Diagrams
Organization of Address and Data Fields for NM93C46A

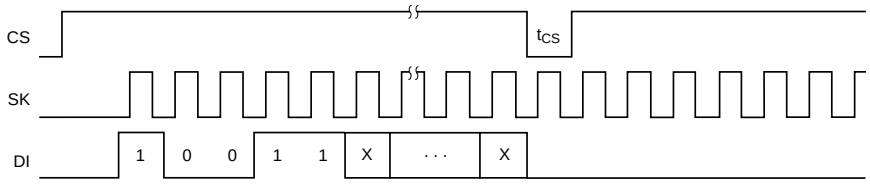
ORG Pin	Organization	A_N	D_N
V_{CC} or NC	64 x 16	A5	D15
V_{SS}	128 x 8	A6	D7

READ



DS011042-5

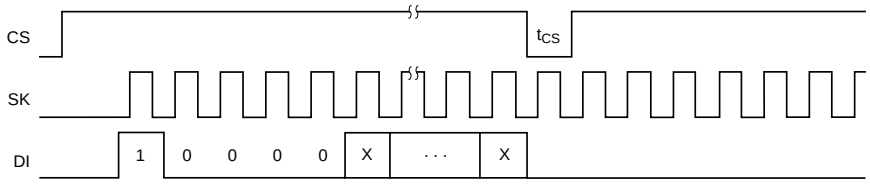
EWEN
DO = TRI-STATE



ORG = V_{CC}, 4 X'S
ORG = V_{SS}, 5 X'S

DS011042-6

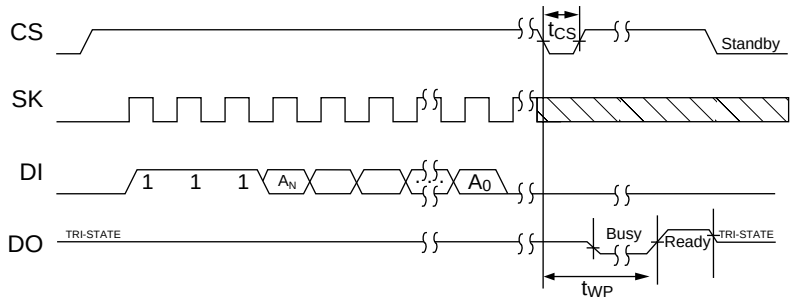
EWDS
DO = TRI-STATE



ORG = V_{CC}, 4 X'S
ORG = V_{SS}, 5 X'S

DS011042-7

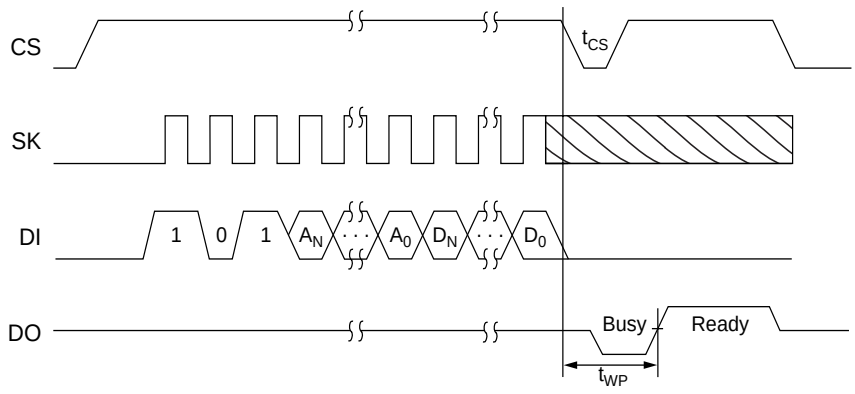
ERASE



DS011042-8

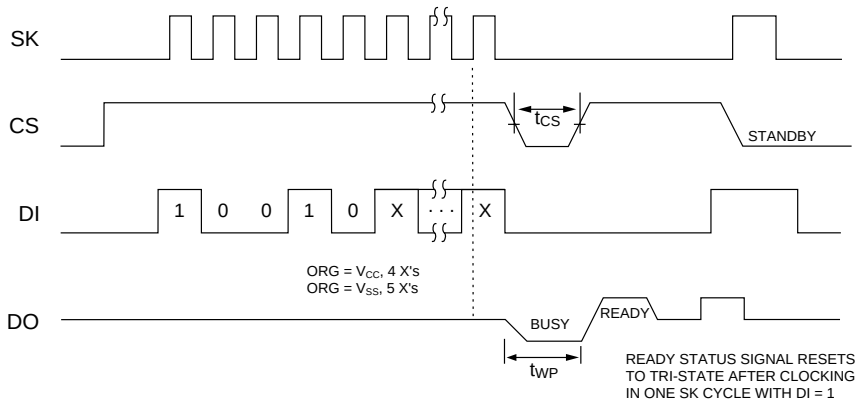
Timing Diagrams for the NM93C46A (Continued)

WRITE



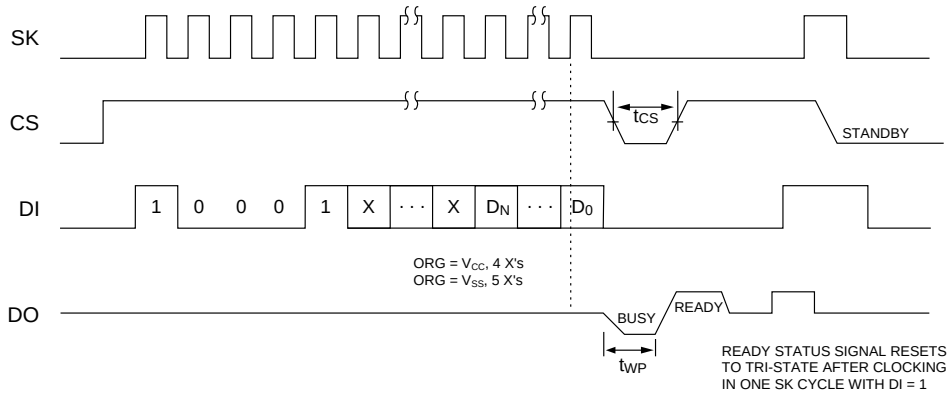
DS011042-9

ERAL



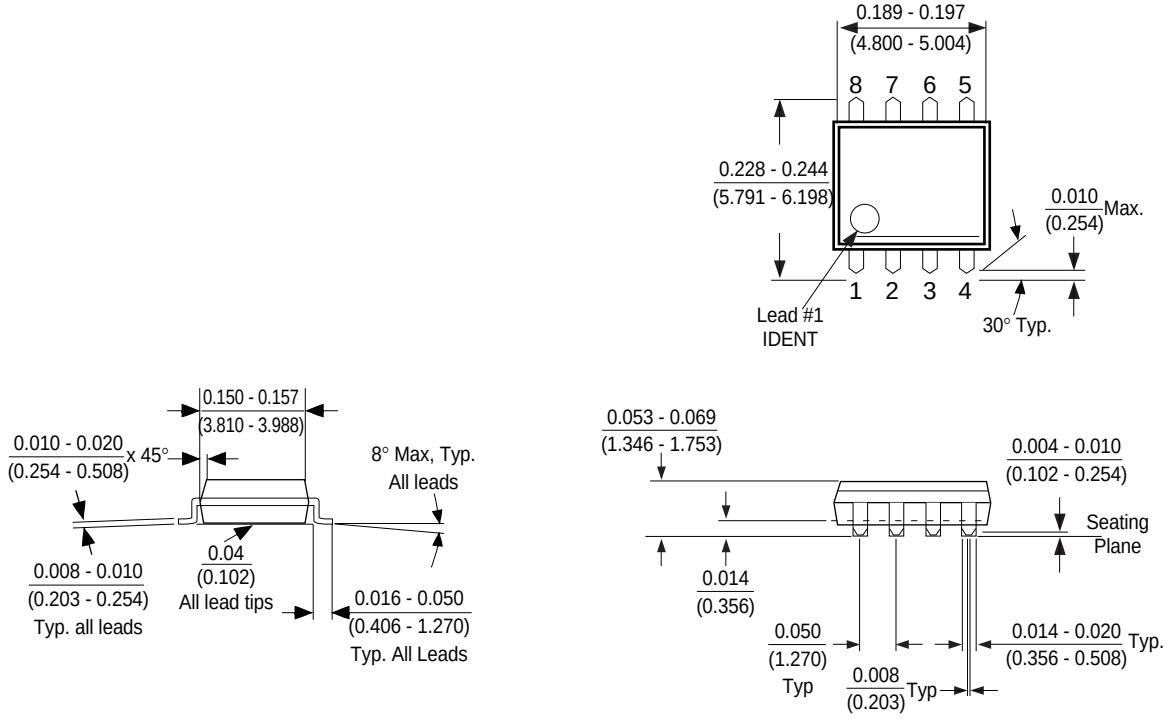
DS011042-10

WRAL



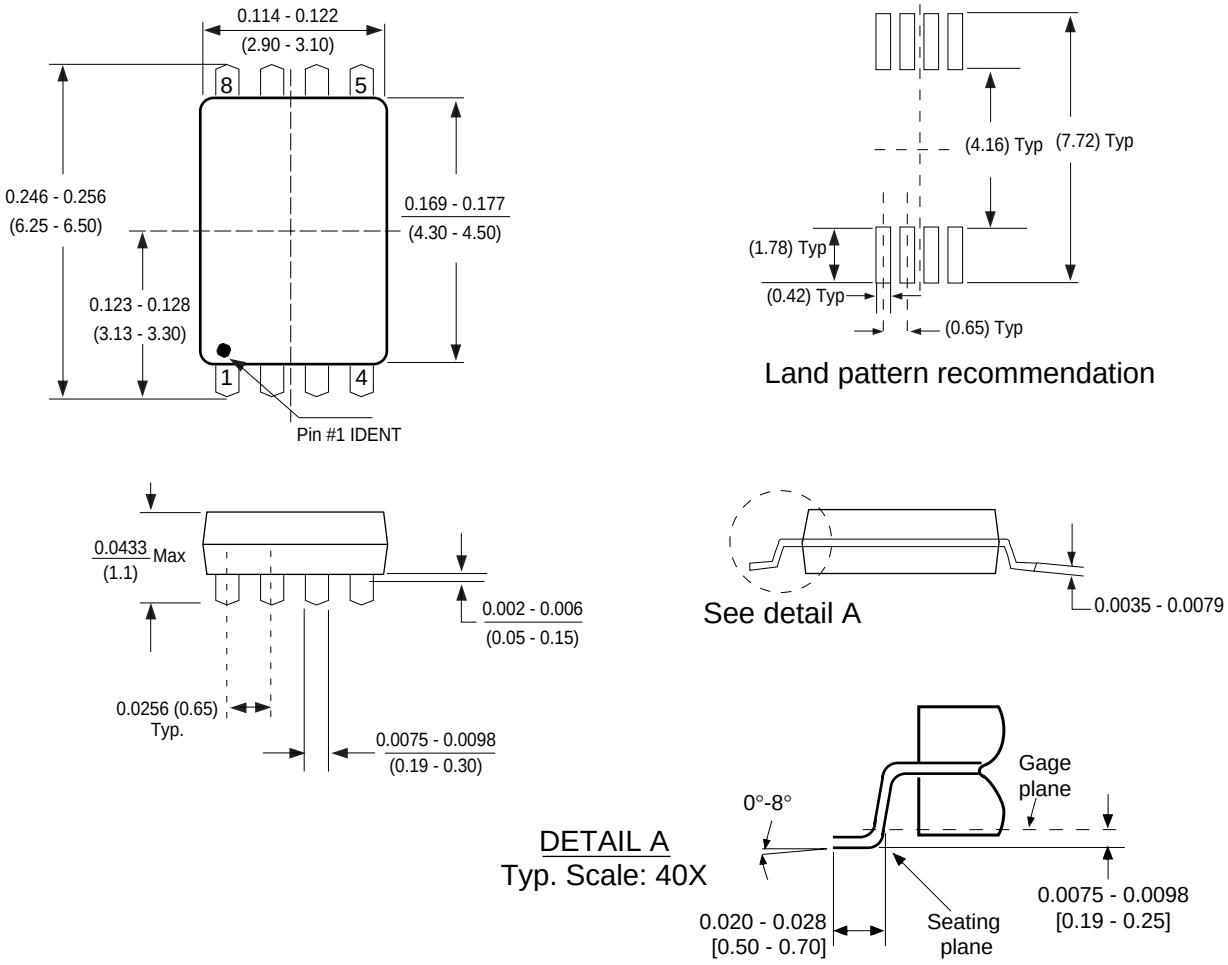
DS011042-11

Physical Dimensions inches (millimeters) unless otherwise noted



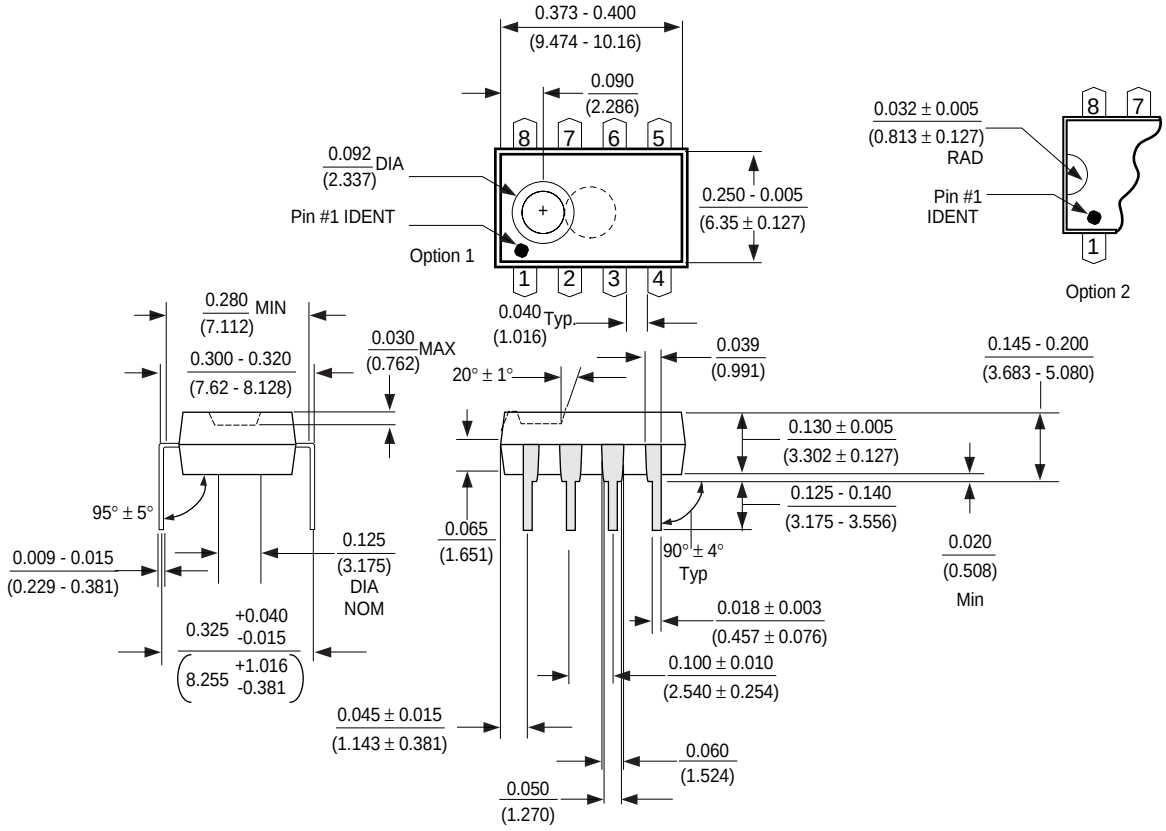
Molded Small Outline Package (M8)
Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin Molded TSSOP, JEDEC (MT8)
Package Number MTC08

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Package Number N08E

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

March 1999

NM93C56
2K-Bit Serial CMOS EEPROM (MICROWIRE™ Bus Interface)

General Description

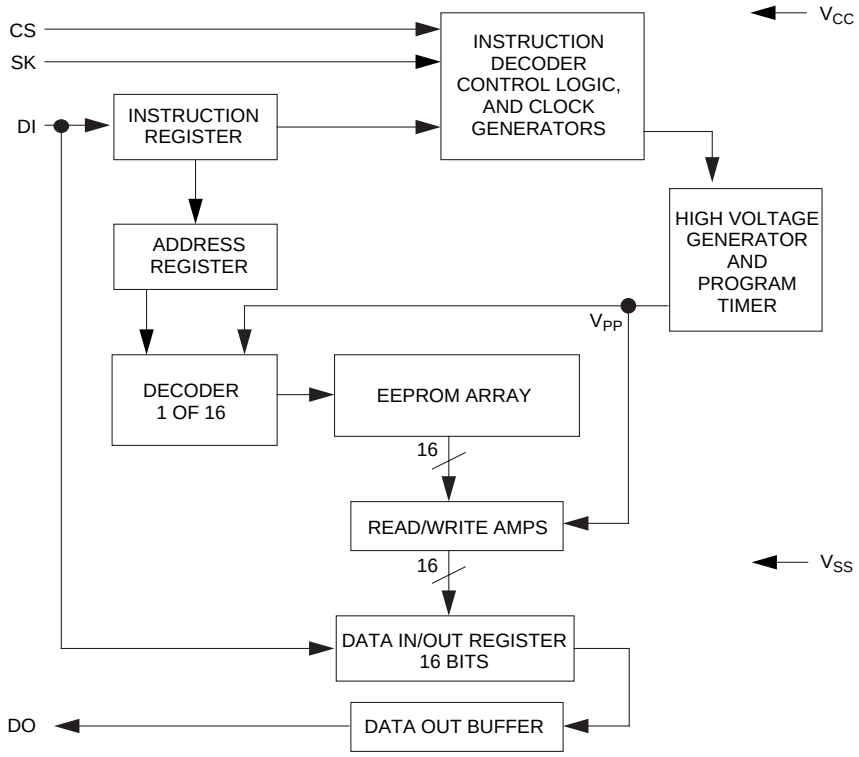
The NM93C56 devices are 2048 bits of CMOS non-volatile electrically erasable memory divided into 128 16-bit registers. They are fabricated using Fairchild Semiconductor's floating-gate CMOS process for high reliability, high endurance and low power consumption. These memory devices are available in an 8-pin SOIC or 8-pin TSSOP package for small space considerations.

The serial interface that operates this EEPROM is MICROWIRE compatible for simple interface to standard microcontrollers and microprocessors. There are 7 instructions which control this device: Read, Write Enable, Erase, Erase All, Write, Write All, and Write Disable. The ready/busy status is available on the DO pin to indicate the completion of a programming cycle.

Features

- Device status during programming mode
- Typical active current of 200µA
  10µA standby current typical
  1µA standby current typical (L)
  0.1µA standby current typical (LZ)
- No erase required before write
- Reliable CMOS floating gate technology
- 2.7V to 5.5V operation in all modes
- MICROWIRE compatible serial I/O
- Self-timed programming cycle
- 40 years data retention
- Endurance: 1,000,000 data changes
- Packages available: 8-pin SO, 8-pin DIP, 8-pin TSSOP

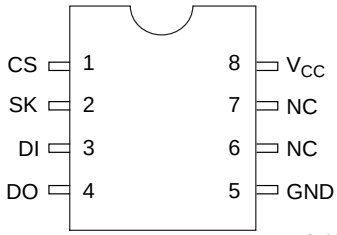
Block Diagram



DS500081-1

Connection Diagrams

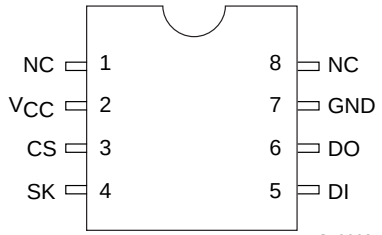
Dual-In-Line Package (N), 8-Pin SO (M8) and 8-Pin TSSOP (MT8)



DS500081-2

Top View
See Package Number
N08E, M08A and MTC08

Rotated Die (93C56T)



DS500081-12

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply

Ordering Information

NM 93 C XX T LZ E XX

	Letter	Description
Package	N	8-Pin DIP
	M8	8-Pin SO8
	MT8	8-Pin TSSOP
Temp. Range	None	0 to 70°C
	V	-40 to +125°C
	E	-40 to +85°C
Voltage Operating Range	Blank	4.5V to 5.5V
	L	2.7V to 4.5V
	LZ	2.7V to 4.5V and <1µA Standby Current
	Blank	Normal Pin Out
	T	Rotated Die Pin Out
Density	56	2K
	C	CMOS
	CS	Data protect and sequential read
Interface	93	MICROWIRE
	NM	**Fairchild Non-Volatile Memory**

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Range

Ambient Operating Temperature	
NM93C56	0°C to +70°C
NM93C56E	-40°C to +85°C
NM93C56V	-40°C to +125°C
Power Supply (V_{CC})	4.5V to 5.5V

Standard V_{CC} (4.5V to 5.5V) DC and AC Electrical Characteristics

Symbol	Parameter	Part Number	Conditions	Min.	Max.	Units
I_{CCA}	Operating Current		CS = V_{IH}, SK = 1MHz		1	mA
I_{CCS}	Standby Current		CS = V_{IL}		50	µA
I_{IL} I_{OL}	Input Leakage Output Leakage		V_{IN} = 0V to V_{CC} (Note 2)		±1	µA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			-0.1 2	0.8 V_{CC} +1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage		I_{OL} = 2.1mA I_{OH} = -400 µA	 2.4	0.4	V V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage		I_{OL} = 10 µA I_{OH} = -10 µA	 V_{CC} -0.2	0.2	V V
f_{SK}	SK Clock Frequency		(Note 3)	0	1	MHz
t_{SKH}	SK High Time	NM93C56 NM93C56E/V		250 300		ns
t_{SKL}	SK Low Time			250		ns
t_{SKS}	SK Setup Time		SK must be at V_{IL} for t_{SKS} before CS goes high	50		ns
t_{CS}	Minimum CS Low Time		(Note 4)	250		ns
t_{CSS}	CS Setup Time			50		ns
t_{DH}	DO Hold Time			70		ns
t_{DIS}	DI Setup Time	NM93C56 NM93C56E/V		100 200		ns
t_{CSH}	CS Hold Time			0		ns
t_{DIH}	DI Hold Time			20		ns
t_{PD1}	Output Delay to "1"				500	ns
t_{PD0}	Output Delay to "0"				500	ns
t_{SV}	CS to Status Valid				500	ns
t_{DF}	CS to DO in TRI-STATE		CS = V_{IL}		100	ns
t_{WP}	Write Cycle Time				10	ms

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Range

Ambient Operating Temperature	
NM93C56L/LZ	0°C to +70°C
NM93C56LE/LZE	-40°C to +85°C
NM93C56LV/LZV	-40°C to +125°C
Power Supply (V_{CC})	2.7V to 4.5V

Low V_{CC} (2.7V to 4.5V) DC and AC Electrical Characteristics

Symbol	Parameter	Part Number	Conditions	Min.	Max.	Units
I_{CCA}	Operating Current		CS = V_{IH}, SK = 250KHz		1	mA
I_{CCS}	Standby Current L LZ		CS = V_{IL}		 10 1	 µA µA
I_{IL} I_{OL}	Input Leakage Output Leakage		V_{IN} = 0V to V_{CC} (Note 2)		±1	µA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			-0.1 0.8 V_{CC}	0.15 V_{CC} V_{CC} +1	V
V_{OL} V_{OH}	Output Low Voltage Output High Voltage		I_{OL} = 10 µA I_{OH} = -10 µA	 0.9 V_{CC}	0.1 V_{CC}	V V
f_{SK}	SK Clock Frequency		(Note 3)	0	250	KHz
t_{SKH}	SK High Time			1		µs
t_{SKL}	SK Low Time			1		µs
t_{SKS}	SK Setup Time		SK must be at V_{IL} for t_{SKS} before CS goes high	0.2		µs
t_{CS}	Minimum CS Low Time		(Note 4)	1		µs
t_{CSS}	CS Setup Time			0.2		µs
t_{DH}	DO Hold Time			70		ns
t_{DIS}	DI Setup Time			0.4		µs
t_{CSH}	CS Hold Time			0		ns
t_{DIH}	DI Hold Time			0.4		µs
t_{PD1}	Output Delay to "1"				2	µs
t_{PD0}	Output Delay to "0"				2	µs
t_{SV}	CS to Status Valid				1	µs
t_{DF}	CS to DO in TRI-STATE		CS = V_{IL}		0.4	µs
t_{WP}	Write Cycle Time				15	ms

Capacitance T_A = 25°C, f = 1 MHz (Note 5)

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical leakage values are in the 20nA range.

Note 3: The shortest allowable SK clock period = $1/f_{SK}$ (as shown under the f_{SK} parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both t_{SKH} and t_{SKL} limits must be observed. Therefore, it is not allowable to set $1/f_{SK} = t_{SKH minimum} + t_{SKL minimum}$ for shorter SK cycle time operation.

Note 4: CS (Chip Select) must be brought low (to V_{IL}) for an interval of t_{CS} in order to reset all internal device registers (device reset) prior to beginning another opcode cycle. (This is shown in the opcode diagram on the following page.)

Note 5: This parameter is periodically sampled and not 100% tested.

AC Test Conditions

V_{CC} Range	V_{IL}/V_{IH} Input Levels	V_{IL}/V_{IH} Timing Level	V_{OL}/V_{OH} Timing Level	I_{OL}/I_{OH}
2.7V ≤ V_{CC} ≤ 5.5V (Extended Voltage Levels)	.03V/1.8V	1.0V	0.8V/1.5V	±10µA
4.5V ≤ V_{CC} ≤ 5.5V (TTL Levels)	0.4V/2.4V	1.0V/2.0V	0.4V/2.4V	-2.1mA/0.4mA
Output Load: 1 TTL Gate (C_L = 100 pF)				

Functional Description

The NM93C56 device has 7 instructions as described below. Note that the MSB of any instruction is a “1” and is viewed as a start bit in the interface sequence. The next 10 bits carry the op code and the 8-bit address for register selection.

Read (READ):

The READ instruction outputs serial data on the D0 pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

Write Enable (WEN):

When V_{CC} is applied to the part, it 'powers-up' in the Write Disable (WDS) state. Therefore, all programming modes must be preceded by a Write Enable (WEN) instruction. Once a Write Enable instruction is executed, programming remains enabled until aWrite Disable (WDS) instruction is executed or V_{CC} is removed from the part.

Erase (ERASE):

The ERASE instruction will program all bits in the specified register to the logical “1” state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum time of t_{CS}. DO = logical “0” indicates that the register, at the address specified in the instruction, has been erased, and the part is ready for another instruction.

Write (WRITE):

The WRITE instruction is followed by the address and 16 bits of data to be written into the specified address. After the last bit of data is put in the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. The D0 pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of t_{CS}. D0 = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Erase All (ERAL):

The ERAL instruction will simultaneously program all registers in the memory array and set each bit to the logical “1” state. The Erase All cycle is identical to the ERASE cycle except for the different op-code. As in the ERASE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval.

Write All (WRALL):

The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval.

Write Disable (WDS):

To protect against accidental data disturb, the WDS instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

Note: The Fairchild CMOS EEPROMs do not require an "ERASE" or "ERASE ALL" operation prior to the "WRITE" and "WRITE ALL" instructions. The "ERASE" and "ERASE ALL" instructions are included to maintain compatibility with earlier technology EEPROMs.

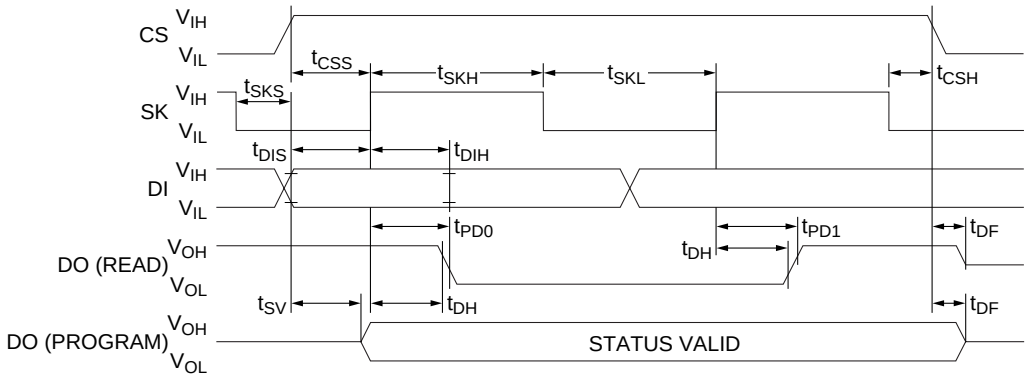
Instruction Set for the NM93C56

Instruction	SB	Op. Code	Address	Data	Comments
READ	1	10	A7-A0		Reads data stored in memory, at specified address.
WEN	1	00	11xxxxxx		Write enable must precede all programming modes.
ERASE	1	11	A7-A0		Erase selected register.
WRITE	1	01	A7-A0	D15-D0	Writes selected register.
ERAL	1	00	10xxxxxx		Erases all registers.
WRALL	1	00	01xxxxxx	D15-D0	Writes all registers.
WDS	1	00	00xxxxxx		Disables all programming instructions.

Note: A7 is "don't care" bit, but must be included in the address string.

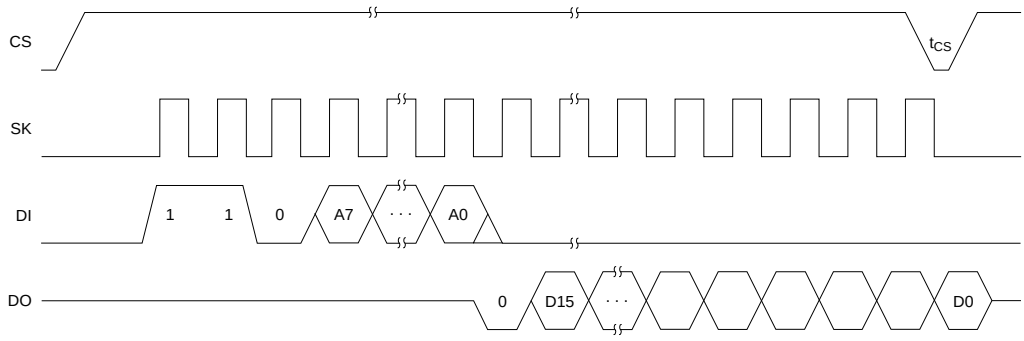
Timing Diagrams

Synchronous Data Timing



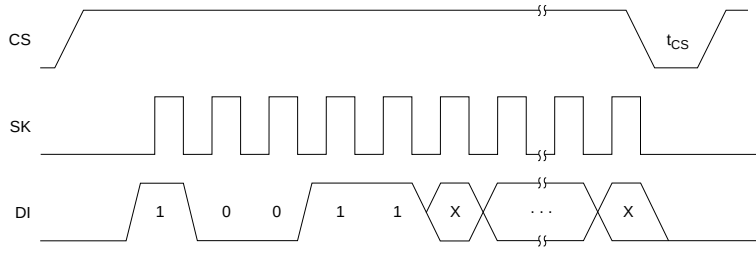
DS500081-4

READ



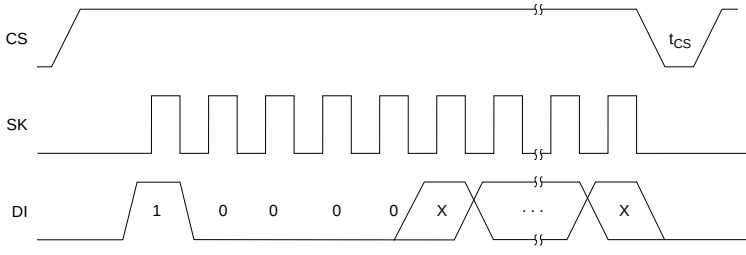
DS500081-5

WEN



DS500081-6

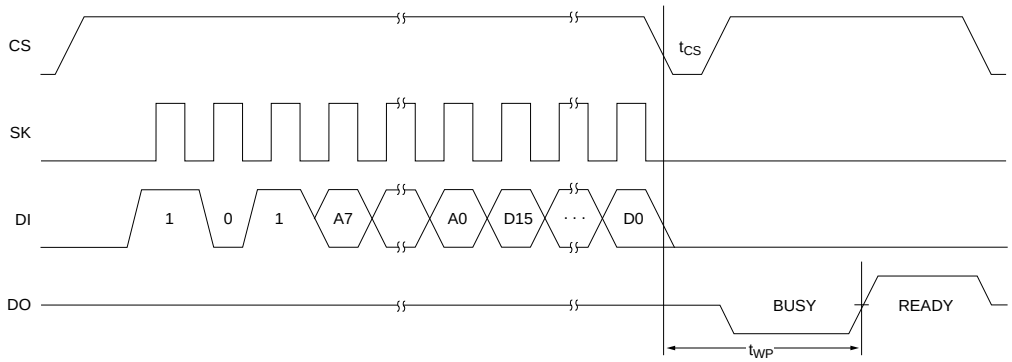
WDS



DS500081-7

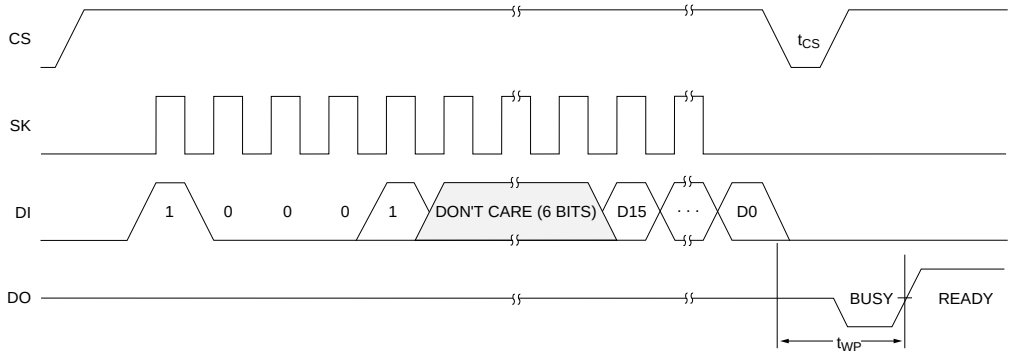
Timing Diagrams (Continued)

WRITE



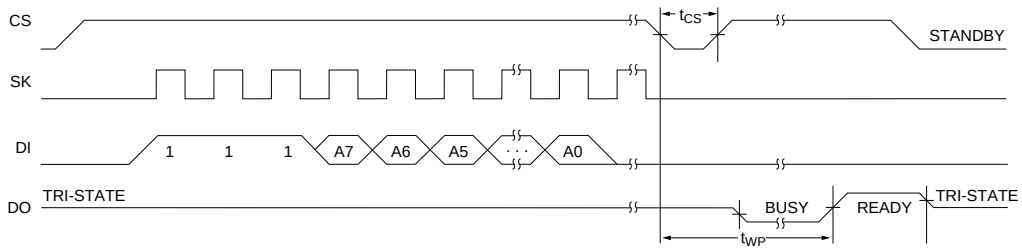
DS500081-8

WRALL



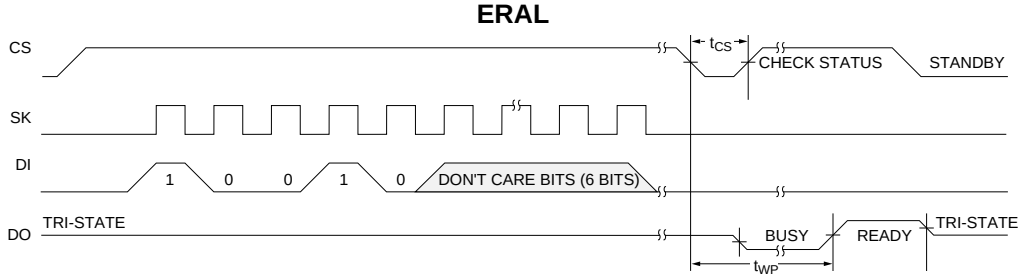
DS500081-9

ERASE



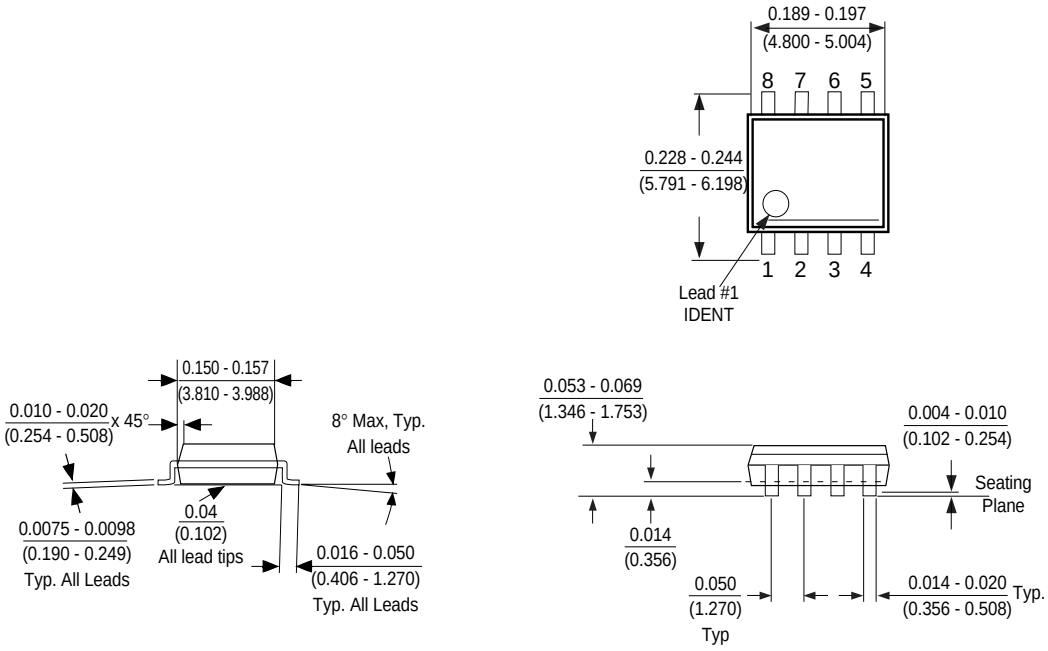
DS500081-10

ERAL

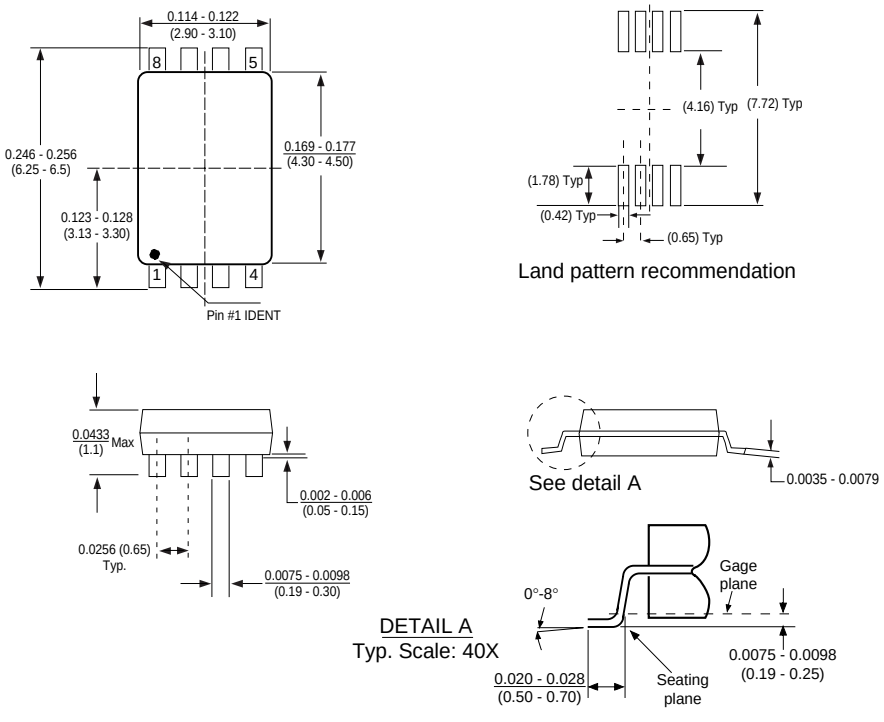


DS500081-11

Physical Dimensions inches (millimeters) unless otherwise noted



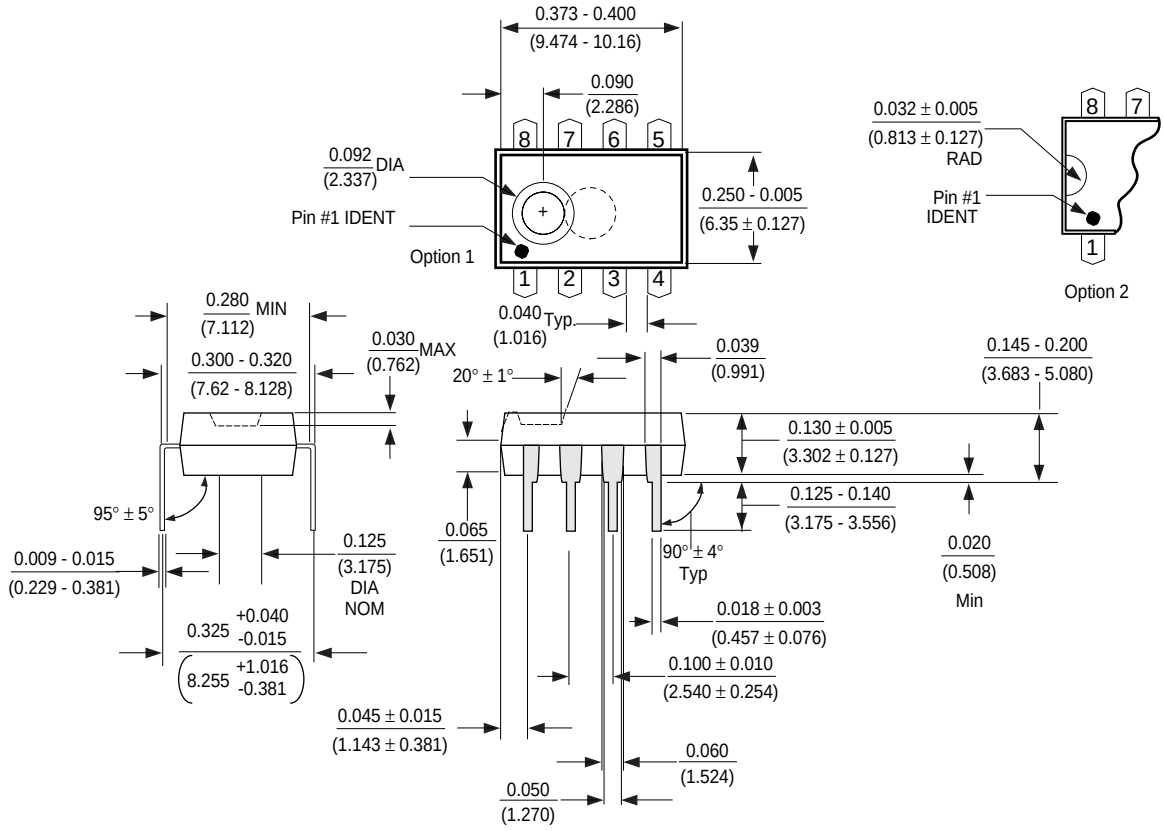
Molded Small Out-Line Package (M8)
Package Number M08A



Notes: Unless otherwise specified
1. Reference JEDEC registration MO153. Variation AA. Dated 7/93

8-Pin Molded TSSOP, JEDEC (MT8)
Package Number MTC08

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Package Number N08E

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

March 1999

NM93C56A
2K-Bit Serial CMOS EEPROM (MICROWIRE™ Synchronous Bus)

General Description

The NM93C56A is 2,048 bits of CMOS non-volatile, electrically erasable memory user organized as either 128 16-bit registers or 256 8-bit registers. The user organization is determined by the status of the ORG input. The memory device is fabricated using Fairchild Semiconductor's floating gate CMOS process for high reliability, high endurance and low power consumption. The NM93C56A is available in both 8-pin SO and TSSOP packages for space considerations.

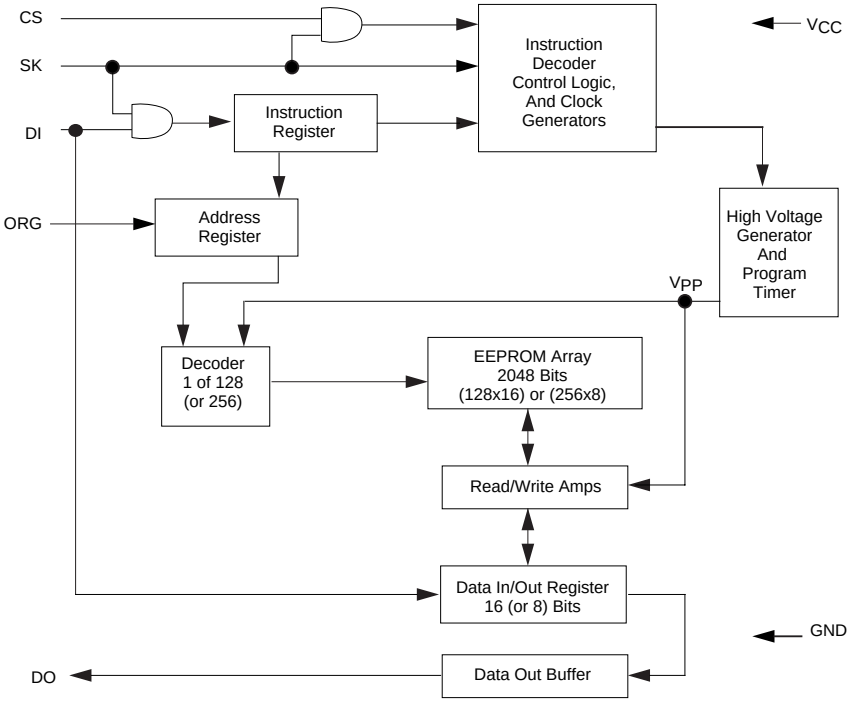
The EEPROM is MICROWIRE compatible for simple interfacing to a wide variety of microcontrollers and microprocessors. There are 7 instructions that operate the NM93C56A: Read, Erase/Write Enable, Erase, Write, Erase/Write Disable, Write All, and Erase All.

The NM93C56A defaults to the 128 x 16 configuration if the ORG pin (Pin 6) is left floating, as it is internally pulled up to V_{CC}.

Features

- 2.7V to 5.5V operation in all modes
- Typical active current 200µA
  10 µA standby current typical
  1 µA standby current typical (L)
  0.1 µA standby current typical (LZ)
- Self-timed programming cycle
- Device status indication during programming mode
- No erase required before write
- Reliable CMOS floating gate technology
- MICROWIRE compatible serial I/O
- 40 years data retention
- Endurance: 1,000,000 data changes
- Packages available: 8-Pin TSSOP, 8-pin SO, 8-pin DIP

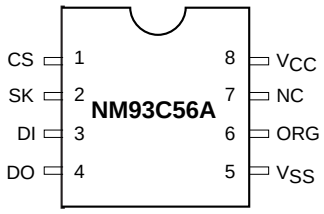
Block Diagram



DS012509-1

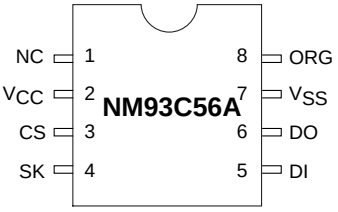
Connection Diagram

Dual-In-Line Package (N)
8-Pin SO Package (M8)
and 8-Pin TSSOP Package (MT8)



DS012509-2

Rotated Die
(93C56AT)



Top View
See Package Number N08E, M08A and MTC08

Pin Names

Pin	Description
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V_{SS}	Ground
ORG	Memory Organization Select
NC	No Connect
V_{CC}	Positive Power Supply

Ordering Information

NM 93 C XX A T LZ E XX

		Letter Description
Package	N	8-Pin DIP
	M8	8-Pin SO8
	MT8	8-Pin TSSOP
Temp. Range	None	0 to 70°C
	V	-40 to +125°C
	E	-40 to +85°C
Voltage Operating Range	Blank	4.5V to 5.5V
	L	2.7V to 4.5V
	LZ	2.7V to 4.5V and <1µA Standby Current
	Blank	Normal Pin Out
	T	Rotated Die Pin Out
	A	x8 or x16 Configuration
Density	56	2K
	C	CMOS
	CS	Data protect and sequential read
Interface	93	MICROWIRE
	NM	**Fairchild Non-Volatile Memory**

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltages with Respect to Ground	V_{CC} +1 to -0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93C56A	0°C to +70°C
NM93C56AE	-40°C to +85°C
NM93C56AV	-40°C to +125°C
Power Supply (V_{CC}) Range	4.5V to 5.5V

DC and AC Electrical Characteristics $4.5V \le V_{CC} \le 5.5V$

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CCA}	Operating Current		CS = V_{IH} SK = 1 MHz		1	mA
I_{CCS}	Standby Current		CS = 0V ORG = V_{CC} or NC		50	µA
I_{IL}	Input Leakage		V_{IN} = 0V to V_{CC} (Note 2)	-1	1	µA
I_{ILO}	Input Leakage ORG Pin		ORG Tied to V_{CC} ORG Tied to V_{SS} (Note 3)	-1 -2.5	1 2.5	µA
I_{OL}	Output Leakage		V_{IN} = 0V to V_{CC}	-1	1	µA
V_{IL}	Input Low Voltage			-0.1	0.8	V
V_{IH}	Input High Voltage			2	V_{CC} +1	V
V_{OL1}	Output Low Voltage		I_{OL} = 2.1 mA		0.4	V
V_{OH1}	Output High Voltage		I_{OH} = -400 µA	2.4		V
V_{OL2}	Output Low Voltage		I_{OL} = 10 µA		0.2	V
V_{OH2}	Output High Voltage		I_{OL} = -10 µA	V_{CC} -0.2		V
f_{SK}	SK Clock Frequency		(Note 4)	0	1	MHz
t_{SKH}	SK High Time	NM93C56A NM93C56AE		250 300		ns
t_{SKL}	SK Low Time			250		ns
t_{SKS}	SK Setup Time		SK must be at V_{IL} for t_{SKS} before CS goes high	50		ns
t_{CS}	Minimum CS Low Time		(Note 5)	250		ns
t_{CSS}	CS Set-Up Time			50		ns
t_{DH}	D0 Hold Time			70		ns
t_{DIS}	DI Set-Up Time	NM93C56A NM93C56AE/V		100 200		ns
t_{CSH}	CS Hold Time			0		ns
t_{DIH}	DI Hold Time			20		ns
t_{PD1}	Output Delay to “1”				500	ns
t_{PD0}	Output Delay to “0”				500	ns
t_{SV}	CS to Status Valid				500	ns
t_{DF}	CS to DO in TRI-STATE®				100	ns
t_{WP}	Write Cycle Time				10	ms

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Range

Ambient Operating Temperature	
NM93C56AL/LZ	0°C to +70°C
NM93C56ALE/LZE	-40°C to +85°C
NM93C56A LV/LZV	-40°C to +125°C
Power Supply (V_{CC})	2.7V to 4.5V

Low V_{CC} (2.7V to 4.5V) DC and AC Electrical Characteristics

Symbol	Parameter	Part Number	Conditions	Min.	Max.	Units
I_{CCA}	Operating Current		CS = V_{IH}, SK = 250KHz		1	mA
I_{CCS}	Standby Current L LZ		CS = V_{IL}		 10 1	 µA µA
I_{IL}	Input Leakage		V_{IN} = 0V to V_{CC} (Note 2)		±1	µA
I_{ILO}	Input Leakage ORG Pin		ORG tied to V_{CC} ORG tied to V_{SS} (Note 3)	-1 -2.5	1 2.5	µA
I_{OL}	Output Leakage		V_{IN} = 0V to V_{CC}		±1	µA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			-0.1 0.8 V_{CC}	0.15 V_{CC} V_{CC} +1	V
V_{OL} V_{OH}	Output Low Voltage Output High Voltage		I_{OL} = 10 µA I_{OH} = -10 µA	 0.9 V_{CC}	0.1 V_{CC}	V V
f_{SK}	SK Clock Frequency		(Note 4)	0	250	KHz
t_{SKH}	SK High Time			1		µs
t_{SKL}	SK Low Time			1		µs
t_{SKS}	SK Setup Time		SK must be at V_{IL} for t_{SKS} before CS goes high	0.2		µs
t_{CS}	Minimum CS Low Time		(Note 5)	1		µs
t_{CSS}	CS Setup Time			0.2		µs
t_{DH}	DO Hold Time			70		ns
t_{DIS}	DI Setup Time			0.4		µs
t_{CSH}	CS Hold Time			0		ns
t_{DIH}	DI Hold Time			0.4		µs
t_{PD1}	Output Delay to "1"				2	µs
t_{PD0}	Output Delay to "0"				2	µs
t_{SV}	CS to Status Valid				1	µs
t_{DF}	CS to DO in TRI-STATE		CS = V_{IL}		0.4	µs
t_{WP}	Write Cycle Time				15	ms

Capacitance T_A = 25°C, f = 1 MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical leakage values are in the 20 nA range.

Note 3: The ORG pin may draw > 1 µA when in the x8 mode ude to an internal pull-up transistor.

Note 4: The shortest allowable SK clock period = $1/f_{SK}$ (as shown under the f_{SK} f_{SK} parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both t_{SKH} and t_{SKl} limits must be observed. Therefore, it is not allowable to set $1/f_{SK} = t_{SKHminimum} + t_{SKLminimum}$ for shorter SK cycle time operation.

Note 5: CS (Chip Select) must be brought low (to V_{IL}) for an interval of t_{CS} in order to reset all internal device registers (device reset) prior to beginning another opcode cycle. (This is shown in the opcode diagrams in the following pages.)

AC Test Conditions

V_{CC} Range	V_{IL}/V_{IH} Input Levels	V_{IL}/V_{IH} Timing Level	V_{OL}/V_{OH} Timing Level	I_{OL}/I_{OH}
2.7V ≤ V_{CC} ≤ 5.5V (Extended Voltage Levels)	.03V/1.8V	1.0V	0.8V/1.5V	±10µA
4.5V ≤ V_{CC} ≤ 5.5V (TTL Levels)	0.4V/2.4V	1.0V/2.0V	0.4V/2.4V	-2.1mA/0.4mA
Output Load: 1 TTL Gate (C_L = 100 pF)				

MICROWIRE I/O Pin Description

Chip Select (CS):

This pin enables and disables the MICROWIRE device and performs 3 general functions:

1. When in the low state, the MICROWIRE device is disabled and the output tri-stated (high impedance). If this pin is brought high (rising edge active), all internal registers are reset and the device is enabled, allowing MICROWIRE communication via DI/DO pins. To restate, the CS pin must be held high during all device communication and opcode functions. If the CS pin is brought low, all functions will be disabled and reset when CS is brought high again. The exception to this is when a programming cycle is initiated (see 2 and 3). Again, all activity on the CS, DI and DO pins is ignored until CS is brought high.
2. After entering all required opcode and address data, bringing CS low initiates the (asynchronous) programming cycle.
3. When programming is in progress, the Data-Out pin will display the programming status as either BUSY (DO low) or READY (DO high) when CS is brought high. (Again, the output will be tri-stated when CS is low.) To restate, during programming, the CS pin may be brought high and low any number of times to view the programming status without affect the programming operation. Once programming is completed (Output in READY state), the output is 'cleared' (returned to normal tri-state condition) by clocking in a Start Bit. After the Start Bit is clocked in, the output will return to a tri-stated condition. When clocked in, this Start Bit can be the first bit in a command string, or CS can be brought low again to reset all internal circuits.

Serial Clock (SK):

This pin is the clock input (rising edge active) for clocking in all opcodes and data on the DI pin and clocking out all data on the DO pin.However, this pin has no effect on the asynchronous programming cycle (see the CS pin section) as the BUSY/READY status is a function of the CS pin only.

Data-In (DI):

All serial communication into the device is performed using this input pin (rising edge active). In order to avoid false Start Bits, or related issues, it is advised to keep the DI pin in the low state unless actually clocking in data bits (Start Bit, Opcode, Address or incoming data bits to be programmed). Please note that the first '1' clocked into the device (after CS is brought high) is seen as a Start Bit and the beginning of a serial command string, so caution must be observed when bringing CS high.

Data-Out (DO):

All serial communication out of the device (READ opcode) is performed using this output pin (rising edge active) as well as indicating the READY/BUSY status duting the asynchronous programming cycle. Note that, during READ operations, the output data is clocked out after the last address bit (A0) is clocked in. If a 3-wire application is required (where DI and DO are tied together), sections in AN-758, or related application notes, must be followed for correct operation.

Organization (ORG):

This pin controls the device architecture (8-bit data word vs. 16-bit data word). If the ORG pin is brought to V_{CC}, the device is configured wiht a 16-bit data word and if the ORG pin is brought to V_{SS} (Ground), the device is configured with an 8-bit data word (refer to other sections for details of both configurations). If the ORG pin is left floating, the device will default to a 16-bit data word.

Instruction Set for the NM93C56A

ORG Pin Logic	Memory	
	Configuration	# of Address Bits
0	256 x 8	9 Bits
1	128 x 16	8 Bits

Note: The leading (MSB) bit is a "don't care," but must be included in the address string.

128 by 16-Bit Organization (NM93C56A when ORG = V_{CC} or NC)

Instruction	SB	OP-Code 2 Bits	Address 8 Bits	Data 16 Bits	Comments
READ	1	10	A7–A0		Read data stored in selected registers.
EWEN	1	00	11XXXXXX		Enables programming modes.
EWDS	1	00	00XXXXXX		Disables all programming modes.
ERASE	1	11	A7–A0		Erase selected register.
WRITE	1	01	A7–A0	D15–D0	Writes data pattern D15–D0 into selected register.
ERAL	1	00	10XXXXXX		Erases all registers.
WRAL	1	00	01XXXXXX	D15–D0	Writes data pattern D15–D0 into all registers.

Note: The A7 bit is a "don't care" bit, but must be entered in the Address string.

256 by 8-Bit Organization (NM93C56A when ORG = GND)

Instruction	SB	OP-Code 2 Bits	Address 9 Bits	Data 8 Bits	Comments
READ	1	10	A8–A0		Read data stored in selected registers.
EWEN	1	00	11XXXXXXX		Enables programming modes.
EWDS	1	00	00XXXXXXX		Disables all programming modes.
ERASE	1	11	A8–A0		Erase selected register.
WRITE	1	01	A8–A0	D7–D0	Writes data pattern D7–D0 into selected registers.
ERAL	1	00	10XXXXXXX		Erases all registers.
WRAL	1	00	01XXXXXXX	D7–D0	Writes data pattern D7–D0 into all registers.

Note: The A8 bit is a "don't care" bit, but must be entered in the Address string.

Functional Description

Programming:

1. Programming is initiated by clocking in the Start Bit, Opcode bits, Address bits and the 8/16 data bits (refer to the ORG pin section).
2. Programming is started by bringing the CS pin low. Once the programming cycle is started, it cannot be stopped. (Bringing V_{CC} low will stop any programming, but will also result in data corruption.)
3. The status of the programming cycle (BUSY or READY) is observed by bringing the CS pin high and observing the output state. If the output is LOW, the device is still programming (BUSY). If the output is HIGH, the programming cycle has been completed and the device is ready for the next operation. Note that the output will be tri-stated each time CS is brought low and the R/B status will be shown each time CS is brought high.
4. After programming, the READY state (output HIGH) can be reset and the output tri-stated by clocking in a single Start Bit. This Start Bit can be the first bit in a command string, or CS can be brought low again to reset all internal circuits. In any case, clocking in a '1' bit will tri-state the output.

Read (READ)

The READ instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a serial-out shift register. A dummy bit (logical 0) precedes the serial data output string. Output data changes are initiated by a low to high transition of SK after the last address bit (A0) is clocked in.

Erase/Write Enable (EWEN)

When V_{CC} is applied to the part, it “powers up” in the Erase/Write Disable (EWDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once an Erase/Write Enable instruction is executed, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} is removed from the part.

Functional Description (Continued)

Erase/Write Disable (EWDS):

To protect against accidental data overwrites, the Erase/Write Disable (EWDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

Erase (ERASE):

The ERASE instruction will program all bits in the specified register to the logical “1” state. Please refer to the Programming section for details.

Write (WRITE):

The WRITE instruction is followed by 16 bits of data (or 8 bits of data when using the NM93C56A in the x8 organization) to be written into the specified address. Please refer to the Programming section for details.

Erase All (ERAL):

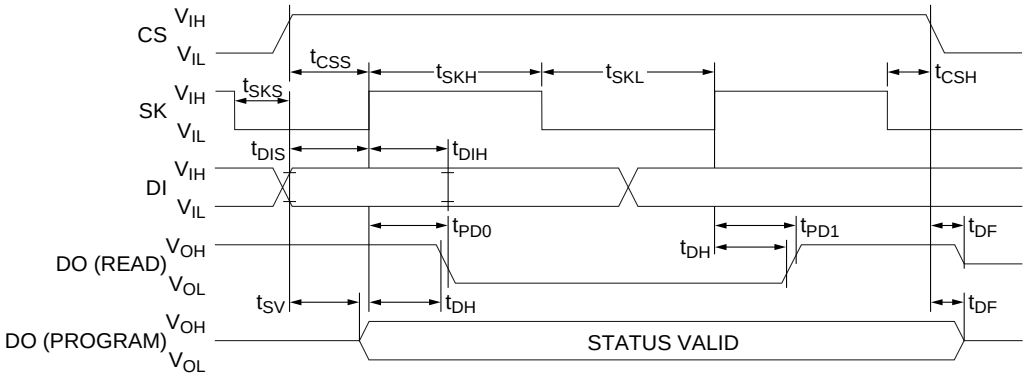
The ERAL instruction will simultaneously program all registers in the memory array to the logical “1” state.

Write All (WRAL):

The WRAL instruction will simultaneously program all registers with the data pattern specified in the instruction.

Timing Diagrams for the NM93C56A

Synchronous Data Timing



DS012509-4

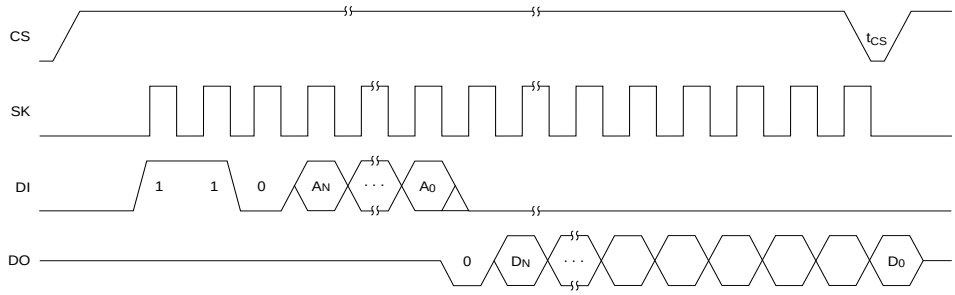
Timing Diagrams for the NM93C56A (Continued)

Key for Timing Diagrams
Organization of Address and Data Fields for NM93C56A

ORG Pin	Organization	A_N	D_N
V_{CC} or NC	128 x 16	A7	D15
V_{SS}	256 x 8	A8	D7

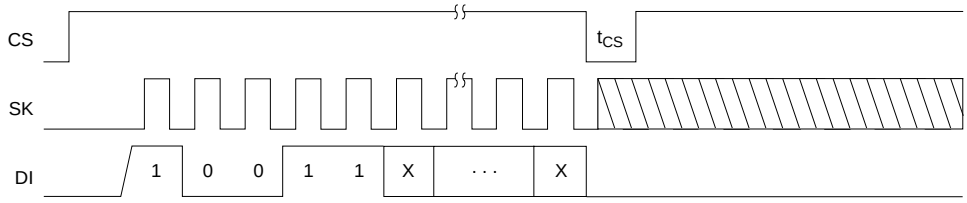
Note: The MSB is "don't care."

READ



DS012509-5

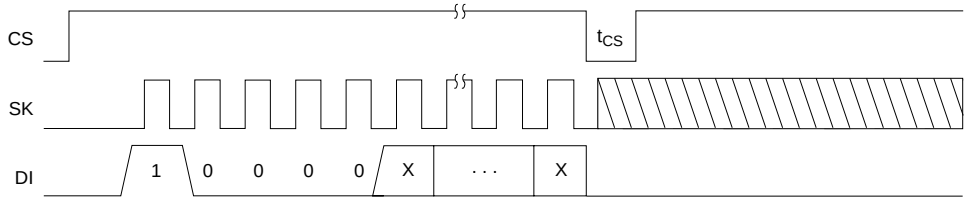
EWEN
DO = TRI-STATE



ORG = V_{CC}, 6 X'S
ORG = V_{SS}, 7 X'S

DS012509-6

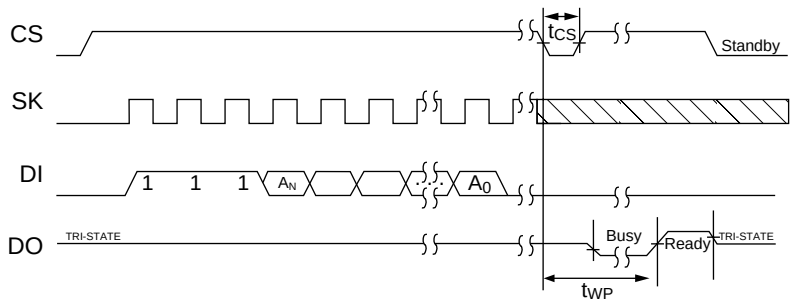
EWDS
DO = TRI-STATE



ORG = V_{CC}, 6 X'S
ORG = V_{SS}, 7 X'S

DS012509-7

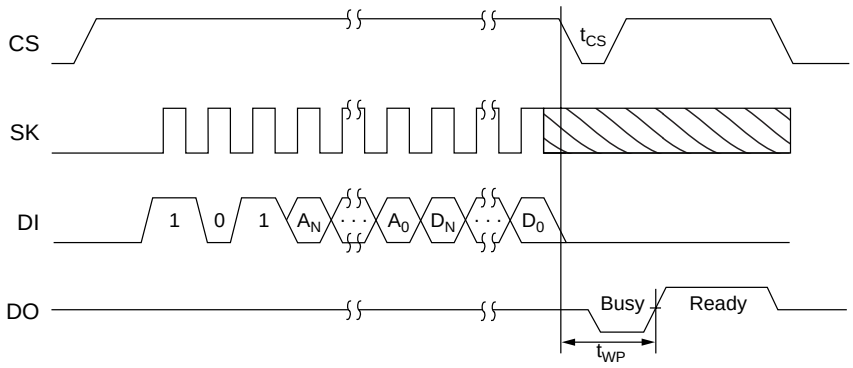
ERASE



DS012509-8

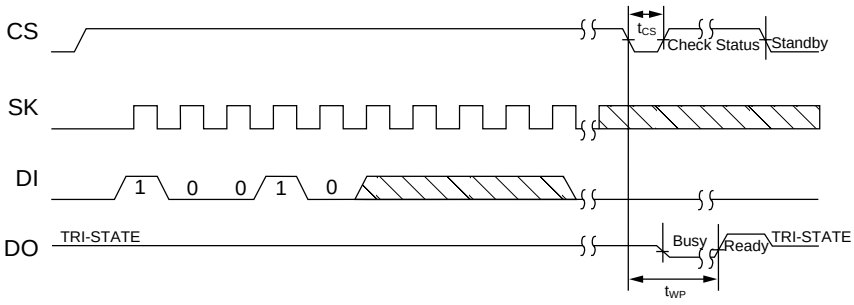
Timing Diagrams for the NM93C56A (Continued)

WRITE



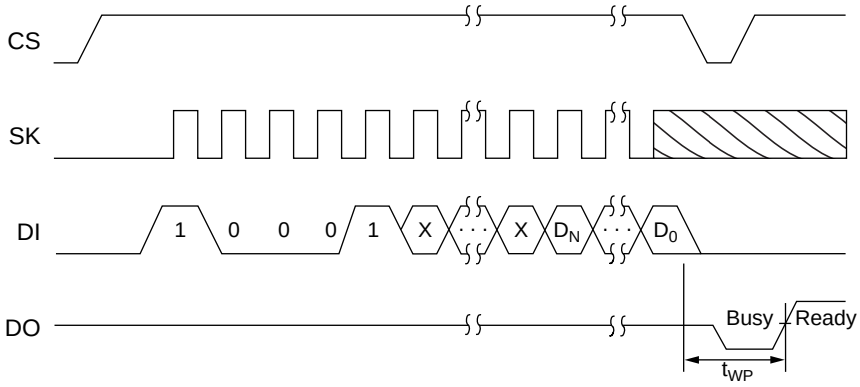
DS012509-9

ERAL



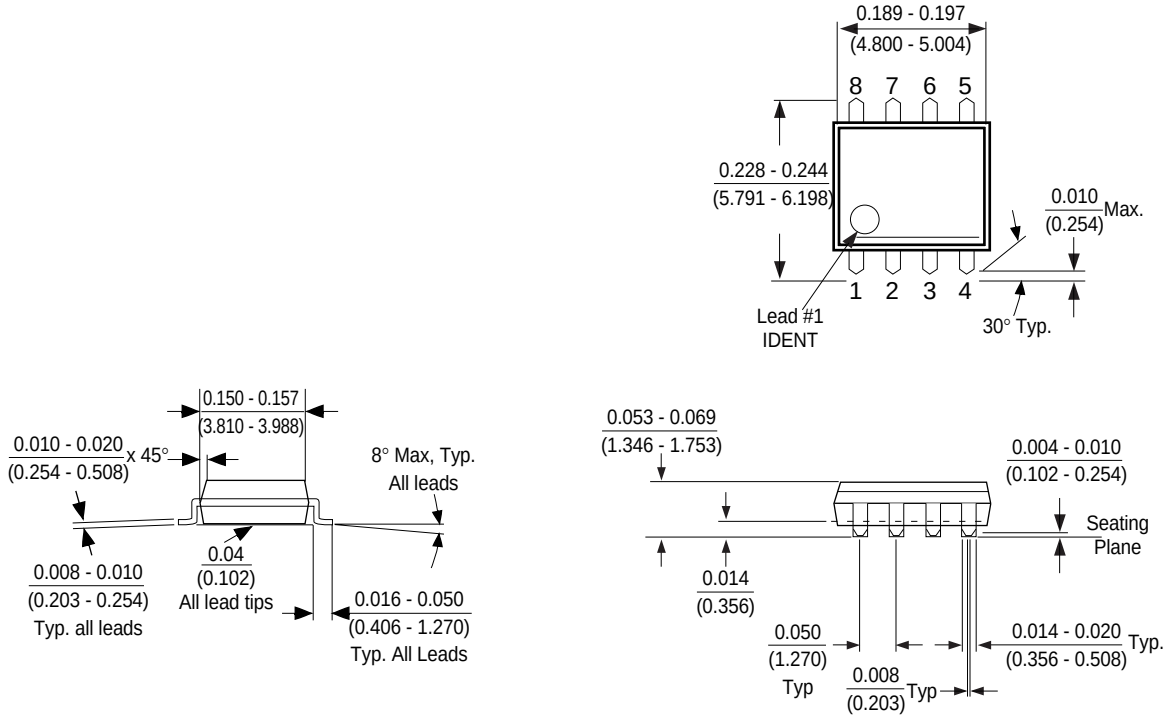
DS012509-10

WRAL



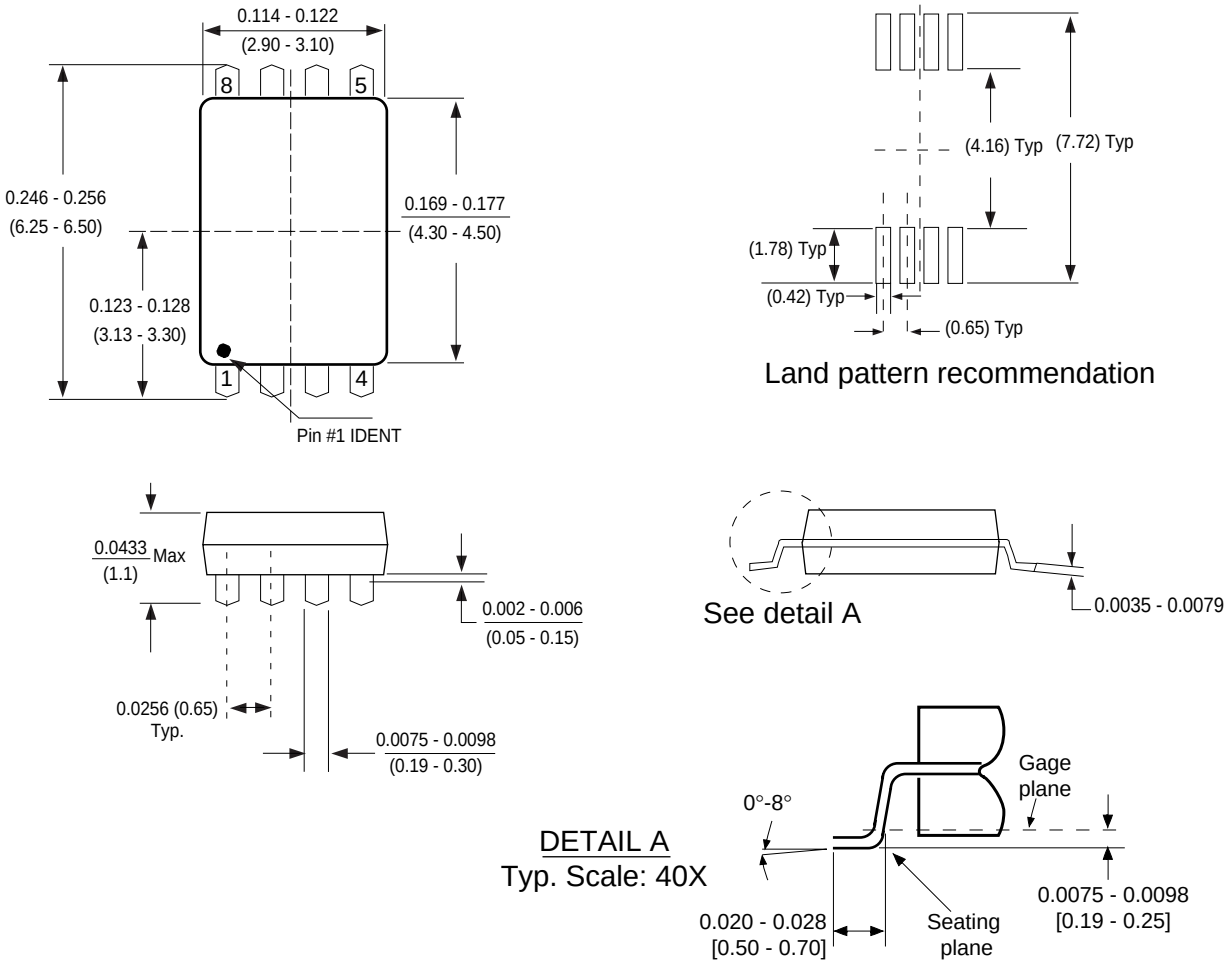
DS012509-11

Physical Dimensions inches (millimeters) unless otherwise noted



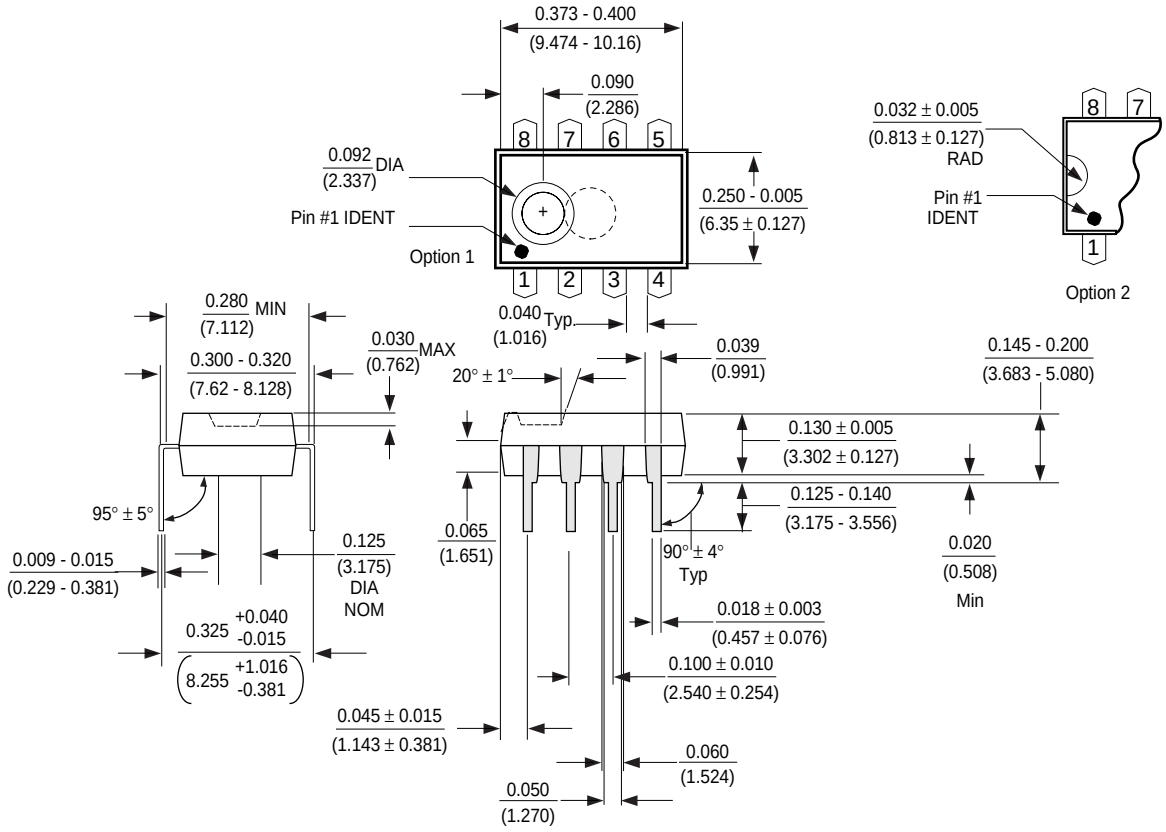
Molded Small Outline Package (M8)
Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin Molded TSSOP, JEDEC (MT8)
Package Number MTC08

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Package Number N08E

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

March 1999

NM93C66
4K-Bit Serial CMOS EEPROM (MICROWIRE™ Bus Interface)

General Description

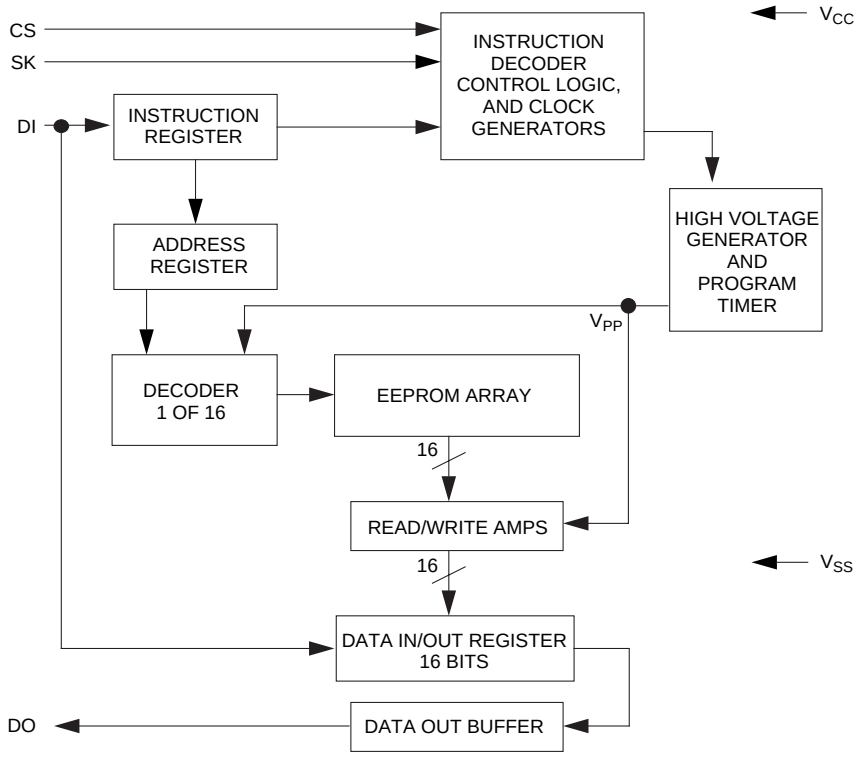
The NM93C66 devices are 4096 bits of CMOS non-volatile electrically erasable memory divided into 256 16-bit registers. They are fabricated using Fairchild Semiconductor's floating-gate CMOS process for high reliability, high endurance and low power consumption. These memory devices are available in an 8-pin SOIC or 8-pin TSSOP package for small space considerations.

The serial interface that operates this EEPROM is MICROWIRE compatible for simple interface to standard microcontrollers and microprocessors. There are 7 instructions which control this device: Read, Write Enable, Erase, Erase All, Write, Write All, and Write Disable. The ready/busy status is available on the DO pin to indicate the completion of a programming cycle.

Features

- Device status during programming mode
- Typical active current of 200µA
  10µA standby current typical
  1µA standby current typical (L)
  0.1µA standby current typical (LZ)
- No erase required before write
- Reliable CMOS floating gate technology
- 2.7V to 5.5V operation in all modes
- MICROWIRE compatible serial I/O
- Self-timed programming cycle
- 40 years data retention
- Endurance: 1,000,000 data changes
- Packages available: 8-pin SO, 8-pin DIP, 8-pin TSSOP

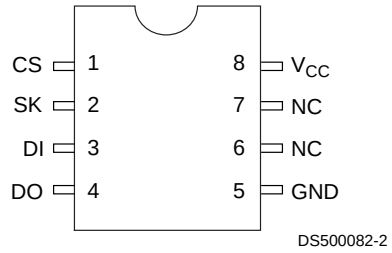
Block Diagram



DS500082-1

Connection Diagrams

Dual-In-Line Package (N),
8-Pin SO (M8) and 8-Pin TSSOP (MT8)



Top View
See Package Number
N08E, M08A and MTC08

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply

Ordering Information

NM 93 C XX LZ E XX

	Letter	Description
Package	N	8-Pin DIP
	M8	8-Pin SO8
	MT8	8-Pin TSSOP
Temp. Range	None	0 to 70°C
	V	-40 to +125°C
	E	-40 to +85°C
Voltage Operating Range	Blank	4.5V to 5.5V
	L	2.7V to 4.5V
	LZ	2.7V to 4.5V and <1µA Standby Current
Density	66	4K
	C	CMOS
Interface	93	MICROWIRE
NM		**Fairchild Non-Volatile Memory**

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Range

Ambient Operating Temperature	
NM93C66	0°C to +70°C
NM93C66E	-40°C to +85°C
NM93C66V	-40°C to +125°C
Power Supply (V_{CC})	4.5V to 5.5V

Standard V_{CC} (4.5V to 5.5V) DC and AC Electrical Characteristics

Symbol	Parameter	Part Number	Conditions	Min.	Max.	Units
I_{CCA}	Operating Current		CS = V_{IH}, SK = 1MHz		1	mA
I_{CCS}	Standby Current		CS = V_{IL}		50	µA
I_{IL} I_{OL}	Input Leakage Output Leakage		V_{IN} = 0V to V_{CC} (Note 2)		±1	µA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			-0.1 2	0.8 V_{CC} +1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage		I_{OL} = 2.1mA I_{OH} = -400 µA	 2.4	0.4	V V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage		I_{OL} = 10 µA I_{OH} = -10 µA	 V_{CC} -0.2	0.2	V V
f_{SK}	SK Clock Frequency		(Note 3)	0	1	MHz
t_{SKH}	SK High Time	NM93C66 NM93C66E/V		250 300		ns
t_{SKL}	SK Low Time			250		ns
t_{SKS}	SK Setup Time		SK must be at V_{IL} for t_{SKS} before CS goes high	50		ns
t_{CS}	Minimum CS Low Time		(Note 4)	250		ns
t_{CSS}	CS Setup Time			50		ns
t_{DH}	DO Hold Time			70		ns
t_{DIS}	DI Setup Time	NM93C66 NM93C66E/V		100 200		ns
t_{CSH}	CS Hold Time			0		ns
t_{DIH}	DI Hold Time			20		ns
t_{PD1}	Output Delay to "1"				500	ns
t_{PD0}	Output Delay to "0"				500	ns
t_{SV}	CS to Status Valid				500	ns
t_{DF}	CS to DO in TRI-STATE		CS = V_{IL}		100	ns
t_{WP}	Write Cycle Time				10	ms

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Range

Ambient Operating Temperature	
NM93C66L/LZ	0°C to +70°C
NM93C66LE/LZE	-40°C to +85°C
NM93C66LV/LZV	-40°C to +125°C
Power Supply (V_{CC})	2.7V to 4.5V

Low V_{CC} (2.7V to 4.5V) DC and AC Electrical Characteristics

Symbol	Parameter	Part Number	Conditions	Min.	Max.	Units
I_{CCA}	Operating Current		CS = V_{IH}, SK = 250KHz		1	mA
I_{CCS}	Standby Current L LZ		CS = V_{IL}		 10 1	 µA µA
I_{IL} I_{OL}	Input Leakage Output Leakage		V_{IN} = 0V to V_{CC}		±1	µA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			-0.1 0.8 V_{CC}	0.15 V_{CC} V_{CC} +1	V
V_{OL} V_{OH}	Output Low Voltage Output High Voltage		I_{OL} = 10 µA I_{OH} = -10 µA	 0.9 V_{CC}	0.1 V_{CC}	V V
f_{SK}	SK Clock Frequency		(Note 3)	0	250	KHz
t_{SKH}	SK High Time			1		µs
t_{SKL}	SK Low Time			1		µs
t_{SKS}	SK Setup Time		SK must be at V_{IL} for t_{SKS} before CS goes high	0.2		µs
t_{CS}	Minimum CS Low Time		(Note 4)	1		µs
t_{CSS}	CS Setup Time			0.2		µs
t_{DH}	DO Hold Time			70		ns
t_{DIS}	DI Setup Time			0.4		µs
t_{CSH}	CS Hold Time			0		ns
t_{DIH}	DI Hold Time			0.4		µs
t_{PD1}	Output Delay to "1"				2	µs
t_{PD0}	Output Delay to "0"				2	µs
t_{SV}	CS to Status Valid				1	µs
t_{DF}	CS to DO in TRI-STATE		CS = V_{IL}		0.4	µs
t_{WP}	Write Cycle Time				15	ms

Capacitance T_A = 25°C, f = 1 MHz (Note 5)

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical leakage values are in the 20nA range.

Note 3: The shortest allowable SK clock period = $1/f_{SK}$ (as shown under the f_{SK} parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both t_{SKH} and t_{SKL} limits must be observed. Therefore, it is not allowable to set $1/f_{SK} = t_{SKHminimum} + t_{SKLminimum}$ for shorter SK cycle time operation.

Note 4: CS (Chip Select) must be brought low (to V_{IL}) for an interval of t_{CS} in order to reset all internal device registers (device reset) prior to beginning another opcode cycle. (This is shown in the opcode diagram on the following page.)

Note 5: This parameter is periodically sampled and not 100% tested.

AC Test Conditions

V_{CC} Range	V_{IL}/V_{IH} Input Levels	V_{IL}/V_{IH} Timing Level	V_{OL}/V_{OH} Timing Level	I_{OL}/I_{OH}
2.7V ≤ V_{CC} ≤ 5.5V (Extended Voltage Levels)	.03V/1.8V	1.0V	0.8V/1.5V	±10µA
4.5V ≤ V_{CC} ≤ 5.5V (TTL Levels)	0.4V/2.4V	1.0V/2.0V	0.4V/2.4V	-2.1mA/0.4mA
Output Load: 1 TTL Gate (C_L = 100 pF)				

Functional Description

The NM93C66 device has 7 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. The next 10 bits carry the op code and the 8-bit address for register selection.

Read (READ):

The READ instruction outputs serial data on the D0 pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

Write Enable (WEN):

When V_{CC} is applied to the part, it 'powers-up' in the Write Disable (WDS) state. Therefore, all programming modes must be preceded by a Write Enable (WEN) instruction. Once a Write Enable instruction is executed, programming remains enabled until aWrite Disable (WDS) instruction is executed or V_{CC} is removed from the part.

Erase (ERASE):

The ERASE instruction will program all bits in the specified register to the logical "1" state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum time of t_{CS}. DO = logical "0" indicates that the register, at the address specified in the instruction, has been erased, and the part is ready for another instruction.

Write (WRITE):

The WRITE instruction is followed by the address and 16 bits of data to be written into the specified address. After the last bit of data is put in the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. The D0 pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of t_{CS}. D0 = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Erase All (ERAL):

The ERAL instruction will simultaneously program all registers in the memory array and set each bit to the logical "1" state. The Erase All cycle is identical to the ERASE cycle except for the different op-code. As in the ERASE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval.

Write All (WRALL):

The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval.

Write Disable (WDS):

To protect against accidental data disturb, the WDS instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

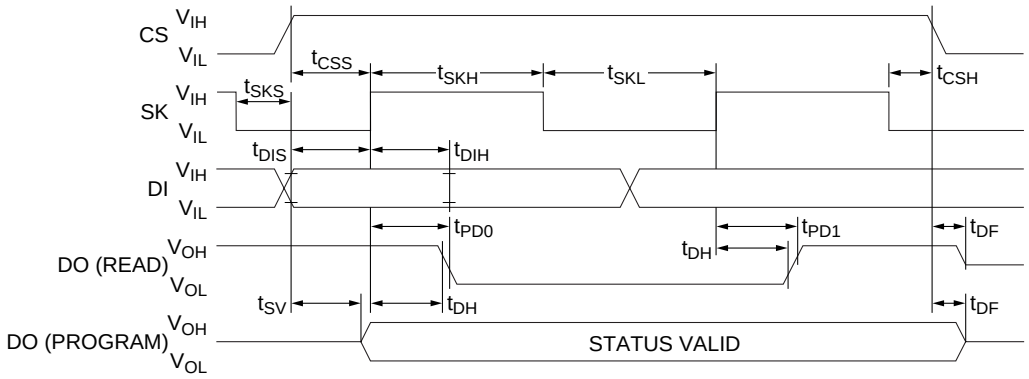
Note: The Fairchild CMOS EEPROMs do not require an "ERASE" or "ERASE ALL" operation prior to the "WRITE" and "WRITE ALL" instructions. The "ERASE" and "ERASE ALL" instructions are included to maintain compatibility with earlier technology EEPROMs.

Instruction Set for the NM93C66

Instruction	SB	Op. Code	Address	Data	Comments
READ	1	10	A7-A0		Reads data stored in memory, at specified address.
WEN	1	00	11xxxxxx		Write enable must precede all programming modes.
ERASE	1	11	A7-A0		Erase selected register.
WRITE	1	01	A7-A0	D15-D0	Writes selected register.
ERAL	1	00	10xxxxxx		Erases all registers.
WRALL	1	00	01xxxxxx	D15-D0	Writes all registers.
WDS	1	00	00xxxxxx		Disables all programming instructions.

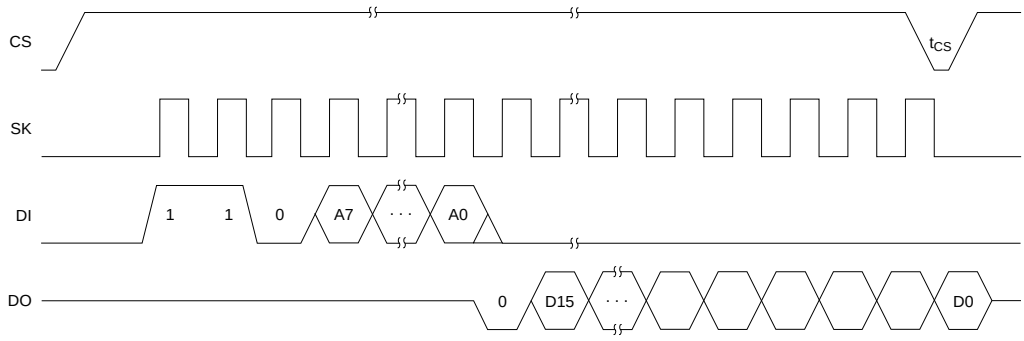
Timing Diagrams

Synchronous Data Timing



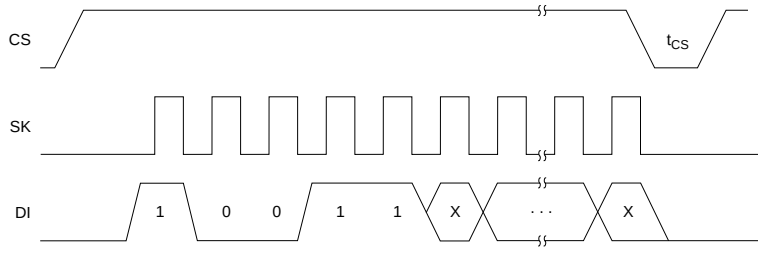
DS500082-4

READ



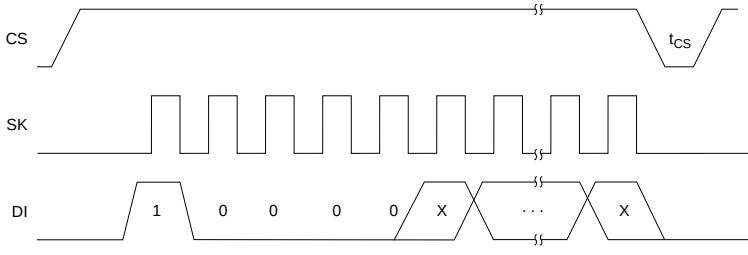
DS500082-5

WEN



DS500082-6

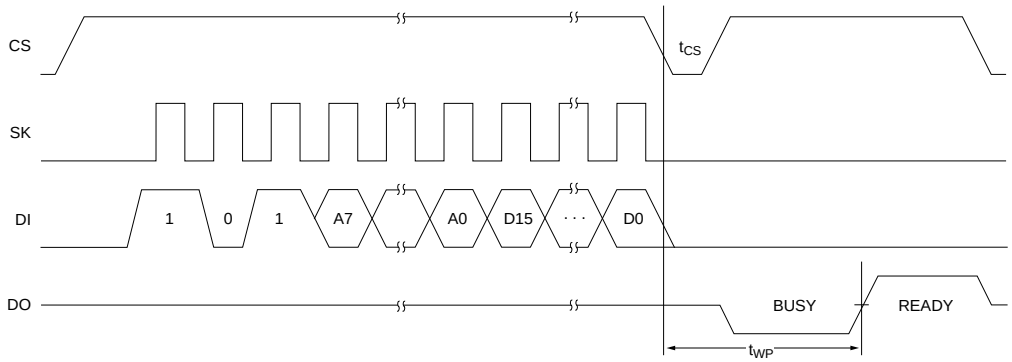
WDS



DS500082-7

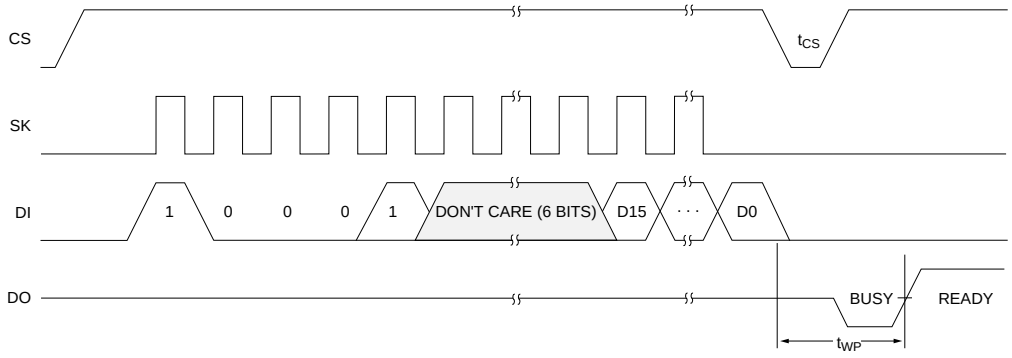
Timing Diagrams (Continued)

WRITE



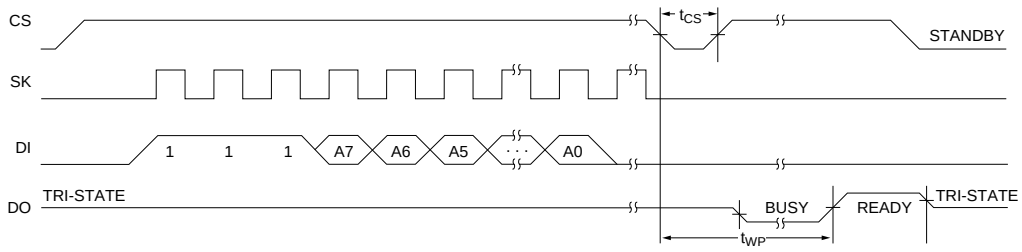
DS500082-8

WRALL



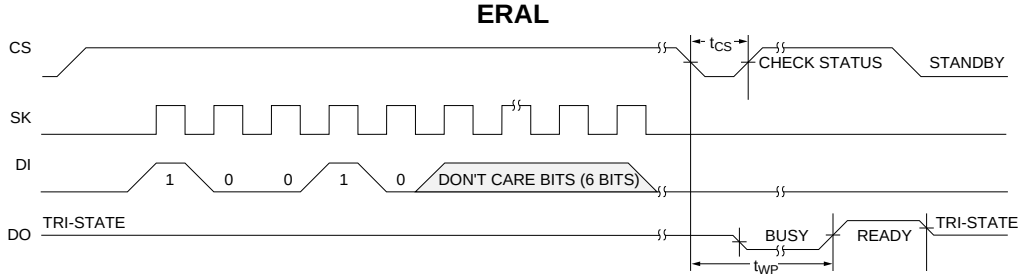
DS500082-9

ERASE



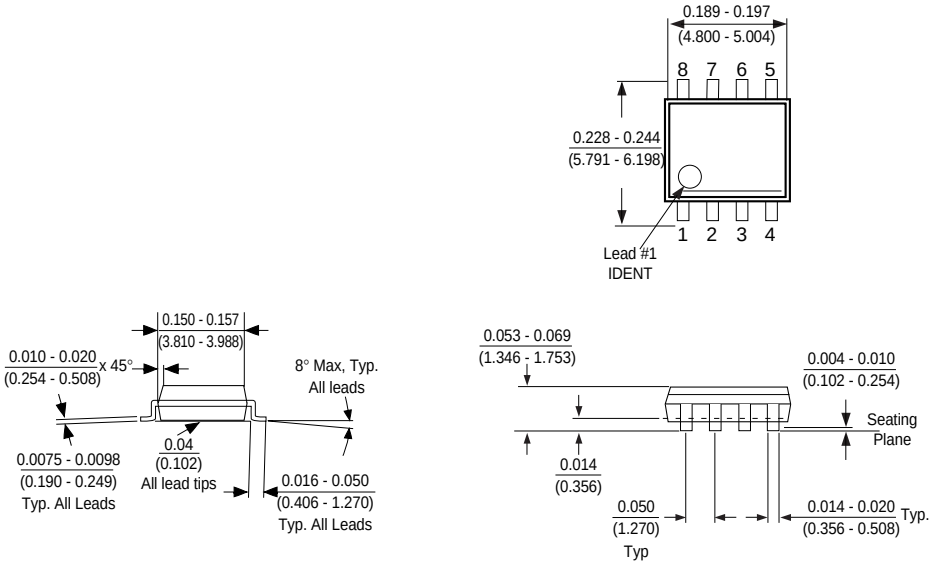
DS500082-10

ERAL

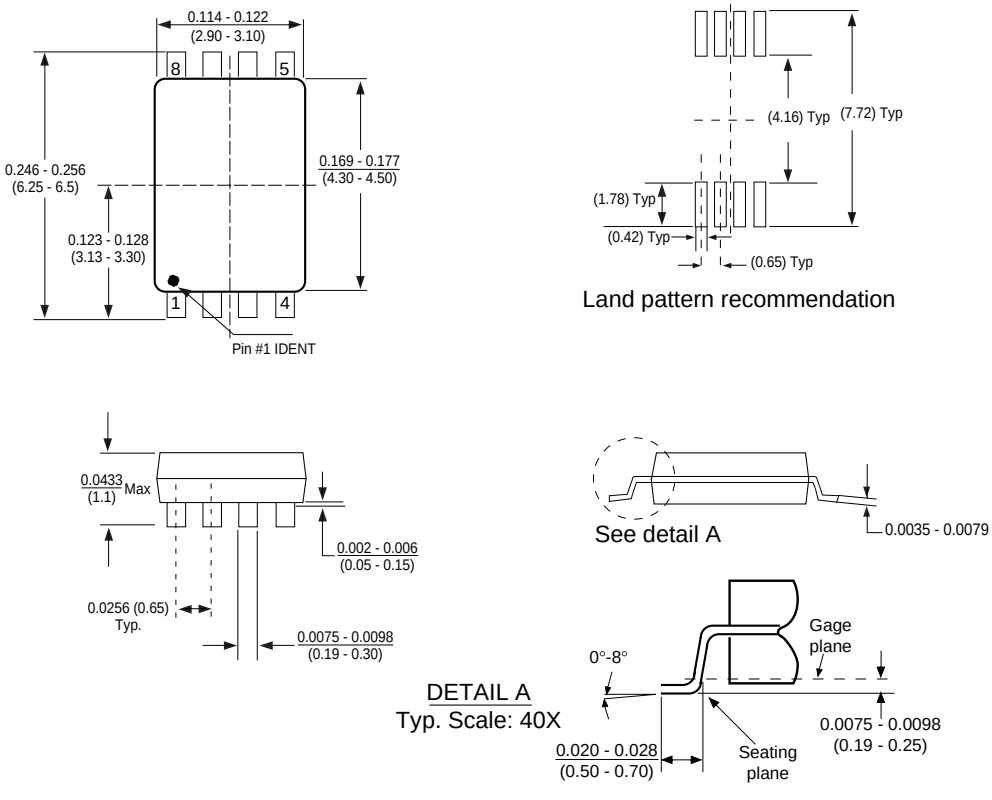


DS500082-11

Physical Dimensions inches (millimeters) unless otherwise noted



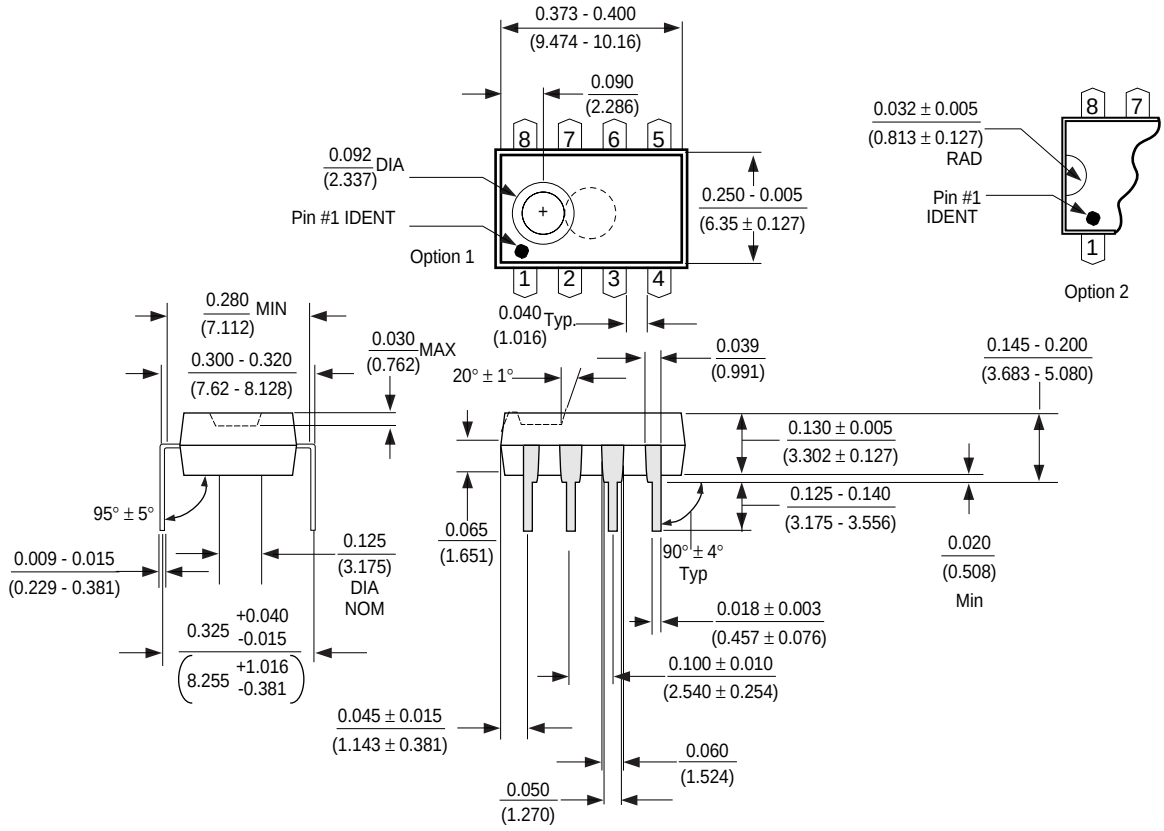
Molded Small Out-Line Package (M8)
Package Number M08A



Notes: Unless otherwise specified
1. Reference JEDEC registration MO153. Variation AA. Dated 7/93

8-Pin Molded TSSOP, JEDEC (MT8)
Package Number MTC08

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Package Number N08E

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

March 1999

NM93C66A
4K-Bit Serial CMOS EEPROM (MICROWIRE™ Bus Interface)

General Description

The NM93C66A is 4,096 bits of CMOS non-volatile, electrically erasable memory available user organized as either 256 16-bit registers or 512 8-bit registers. The user organization is determined by the status of the ORG input. The memory device is fabricated using Fairchild Semiconductor's floating gate CMOS process for high reliability, high endurance and low power consumption. The NM93C66A is available in both 8-pin SO and TSSOP packages for space considerations.

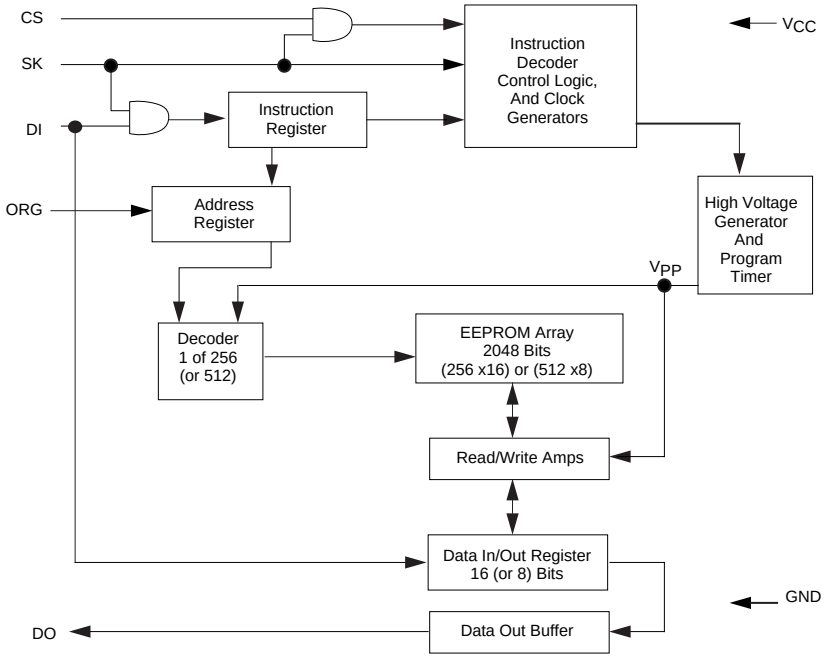
The EEPROM is MICROWIRE compatible for simple interfacing to a wide variety of microcontrollers and microprocessors. There are 7 instructions that operate the NM93C66A: Read, Erase/Write Enable, Erase, Write, Erase/Write Disable, Write All, and Erase All.

The NM93C66A defaults to the 256 x 16 configuration if the ORG pin (Pin 6) is left floating, as it is internally pulled up to V_{CC}.

Features

- 2.7V to 5.5V operation in all modes
- Typical active current of 200μA
  10μA standby current typical
  1μA standby current typical (L)
  0.1μA standby current typical (LZ)
- Self-timed programming cycle
- Device status indication during programming mode
- No erase required before write
- Reliable CMOS floating gate technology
- MICROWIRE compatible serial I/O
- 40 years data retention
- Endurance: 1,000,000 data changes
- Packages available: 8-pin TSSOP, 8-pin SO, 8-pin DIP

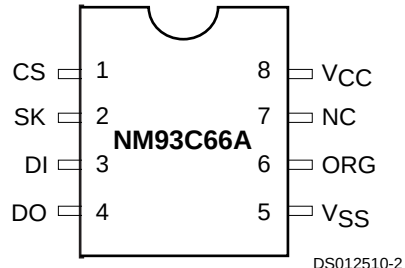
Block Diagram



DS012510-1

Connection Diagram

Dual-In-Line Package (N)
8-Pin SO Package (M8)
and 8-Pin TSSOP Package (MT8)



Top View
See Package Number
N08E, M08A and MTC08

Pin Names

Pin	Description
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V_{SS}	Ground
ORG	Memory Organization Select
NC	No Connect
V_{CC}	Positive Power Supply

Ordering Information

NM 93 C XX A LZ E XX

		Letter Description
Package	N	8-Pin DIP
	M8	8-Pin SO8
	MT8	8-Pin TSSOP
Temp. Range	None	0 to 70°C
	V	-40 to +125°C
	E	-40 to +85°C
Voltage Operating Range	Blank	4.5V to 5.5V
	L	2.7V to 4.5V
	LZ	2.7V to 4.5V and <1µA Standby Current
	A	x8 or x16 Configuration
Density	66	4K
	C	CMOS
Interface	93	MICROWIRE
	NM	**Fairchild Non-Volatile Memory**

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltages with Respect to Ground	V_{CC} +1 to -0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93C66A	0°C to +70°C
NM93C66AE	-40°C to +85°C
NM93C66AV	-40°C to +125°C
Power Supply (V_{CC}) Range	4.5V to 5.5V

DC and AC Electrical Characteristics $4.5V \le V_{CC} \le 5.5V$

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CCA}	Operating Current		CS = V_{IH},SK=1 MHz		1	mA
I_{CCS}	Standby Current		CS = 0V ORG = V_{CC} or NC		50	µA
I_{IL}	Input Leakage		V_{IN} = 0V to V_{CC} (Note 2)	-1	1	µA
I_{ILO}	Input Leakage ORG Pin		ORG Tied to V_{CC} ORG Tied to V_{SS} (Note 3)	-1 -2.5	1 2.5	µA
I_{OL}	Output Leakage		V_{IN} = 0V to V_{CC}	-1	1	µA
V_{IL}	Input Low Voltage			-0.1	0.8	V
V_{IH}	Input High Voltage			2	V_{CC} +1	V
V_{OL1}	Output Low Voltage		I_{OL} = 2.1 mA		0.4	V
V_{OH1}	Output High Voltage		I_{OH} = -400 µA	2.4		V
V_{OL2}	Output Low Voltage		I_{OL} = 10 µA		0.2	V
V_{OH2}	Output High Voltage		I_{OL} = -10 µA	V_{CC} - 0.2		V
f_{SK}	SK Clock Frequency		(Note 4)	0	1	MHz
t_{SKH}	SK High Time	NM93C66A NM93C66AE		250 300		ns
t_{SKL}	SK Low Time			250		ns
t_{SKS}	SK Setup Time		SK must be at V_{IL} for t_{SKS} before CS goes high	50		ns
t_{CS}	Minimum CS Low Time		(Note 5)	250		ns
t_{CSS}	CS Set-Up Time			50		ns
t_{DH}	DO Hold Time			70		ns
t_{DIS}	DI Set-Up Time	NM93C66A NM93C66AE/V		100 200		ns
t_{CSH}	CS Hold Time			0		ns
t_{DIH}	DI Hold Time			20		ns
t_{PD1}	Output Delay to “1”				500	ns
t_{PD0}	Output Delay to “0”				500	ns
t_{SV}	CS to Status Valid				500	ns
t_{DF}	CS to DO in TRI-STATE®				100	ns
t_{WP}	Write Cycle Time				10	ms

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Range

Ambient Operating Temperature	
NM93C66AL/LZ	0°C to +70°C
NM93C66ALE/LZE	-40°C to +85°C
NM93C66ALV/LZV	-40°C to +125°C
Power Supply (V_{CC})	2.7V to 4.5V

Low V_{CC} (2.7V to 4.5V) DC and AC Electrical Characteristics

Symbol	Parameter	Part Number	Conditions	Min.	Max.	Units
I_{CCA}	Operating Current		CS = V_{IH}, SK = 250KHz		1	mA
I_{CCS}	Standby Current L LZ		CS = V_{IL}		 10 1	 µA µA
I_{IL}	Input Leakage		V_{IN} = 0V to V_{CC} (Note 2)		±1	µA
I_{ILO}	Input Leakage ORG Pin		ORG tied to V_{CC} ORG tied to V_{SS} (Note 3)	-1 -2.5	1 2.5	µA
I_{OL}	Output Leakage		V_{IN} = 0V to V_{CC}		±1	µA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			-0.1 0.8 V_{CC}	0.15 V_{CC} V_{CC} +1	V
V_{OL} V_{OH}	Output Low Voltage Output High Voltage		I_{OL} = 10 µA I_{OH} = -10 µA	 0.9 V_{CC}	0.1 V_{CC}	V V
f_{SK}	SK Clock Frequency		(Note 4)	0	250	KHz
t_{SKH}	SK High Time			1		µs
t_{SKL}	SK Low Time			1		µs
t_{SKS}	SK Setup Time		SK must be at V_{IL} for t_{SKS} before CS goes high	0.2		µs
t_{CS}	Minimum CS Low Time		(Note 5)	1		µs
t_{CSS}	CS Setup Time			0.2		µs
t_{DH}	DO Hold Time			70		ns
t_{DIS}	DI Setup Time			0.4		µs
t_{CSH}	CS Hold Time			0		ns
t_{DIH}	DI Hold Time			0.4		µs
t_{PD1}	Output Delay to "1"				2	µs
t_{PD0}	Output Delay to "0"				2	µs
t_{SV}	CS to Status Valid				1	µs
t_{DF}	CS to DO in TRI-STATE		CS = V_{IL}		0.4	µs
t_{WP}	Write Cycle Time				15	ms

Capacitance T_A = 25°C, f = 1 MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical leakage values are in the 20 nA range.

Note 3: The ORG pin may draw > 1 µA when in the x8 mode ude to an internal pull-up transistor.

Note 4: The shortest allowable SK clock period = $1/f_{SK}$ (as shown under the f_{SK} f_{SK} parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both t_{SKH} and t_{SKl} limits must be observed. Therefore, it is not allowable to set $1/f_{SK} = t_{SKHminimum} + t_{SKLminimum}$ for shorter SK cycle time operation.

Note 5: CS (Chip Select) must be brought low (to V_{IL}) for an interval of t_{CS} in order to reset all internal device registers (device reset) prior to beginning another opcode cycle. (This is shown in the opcode diagrams in the following pages.)

AC Test Conditions

V_{CC} Range	V_{IL}/V_{IH} Input Levels	V_{IL}/V_{IH} Timing Level	V_{OL}/V_{OH} Timing Level	I_{OL}/I_{OH}
2.7V ≤ V_{CC} ≤ 5.5V (Extended Voltage Levels)	.03V/1.8V	1.0V	0.8V/1.5V	±10µA
4.5V ≤ V_{CC} ≤ 5.5V (TTL Levels)	0.4V/2.4V	1.0V/2.0V	0.4V/2.4V	-2.1mA/0.4mA
Output Load: 1 TTL Gate (C_L = 100 pF)				

MICROWIRE I/O Pin Description

Chip Select (CS):

This pin enables and disables the MICROWIRE device and performs 3 general functions:

1. When in the low state, the MICROWIRE device is disabled and the output tri-stated (high impedance). If this pin is brought high (rising edge active), all internal registers are reset and the device is enabled, allowing MICROWIRE communication via DI/DO pins. To restate, the CS pin must be held high during all device communication and opcode functions. If the CS pin is brought low, all functions will be disabled and reset when CS is brought high again. The exception to this is when a programming cycle is initiated (see 2 and 3). Again, all activity on the CS, DI and DO pins is ignored until CS is brought high.
2. After entering all required opcode and address data, bringing CS low initiates the (asynchronous) programming cycle.
3. When programming is in progress, the Data-Out pin will display the programming status as either BUSY (DO low) or READY (DO high) when CS is brought high. (Again, the output will be tri-stated when CS is low.) To restate, during programming, the CS pin may be brought high and low any number of times to view the programming status without affect the programming operation. Once programming is completed (Output in READY state), the output is 'cleared' (returned to normal tri-state condition) by clocking in a Start Bit. After the Start Bit is clocked in, the output will return to a tri-stated condition. When clocked in, this Start Bit can be the first bit in a command string, or CS can be brought low again to reset all internal circuits.

Serial Clock (SK):

This pin is the clock input (rising edge active) for clocking in all opcodes and data on the DI pin and clocking out all data on the DO pin.However, this pin has no effect on the asynchronous programming cycle (see the CS pin section) as the READY/BUSY status is a function of the CS pin only.

Data-In (DI):

All serial communication into the device is performed using this input pin (rising edge active). In order to avoid false Start Bits, or related issues, it is advised to keep the DI pin in the low state unless actually clocking in data bits (Start Bit, Opcode, Address or incoming data bits to be programmed). Please note that the first '1' clocked into the device (after CS is brought high) is seen as a Start Bit and the beginning of a serial command string, so caution must be observed when bringing CS high.

Data-Out (DO):

All serial communication out of the device (READ opcode) is performed using this output pin (rising edge active) as well as indicating the READY/BUSY status duting the asynchronous programming cycle. Note that, during READ operations, the output data is clocked out after the last address bit (A0) is clocked in. If a 3-wire application is required (where DI and DO are tied together), sections in AN-758, or related application notes, must be followed for correct operation.

Organization (ORG):

This pin controls the device architecture (8-bit data word vs. 16-bit data word). If the ORG pin is brought to V_{CC}, the device is configured with a 16-bit data word and if the ORG pin is brought to V_{SS} (Ground), the device is configured with an 8-bit data word (refer to other sections for details of both configurations). If the ORG pin is left floating, the device will default to a 16-bit data word.

Instruction Set for NM93C66A

ORG Pin Logic	Memory	
	Configuration	# of Address Bits
0	512 x 8	9 Bits
1	256 x 16	8 Bits

256 by 16-Bit Organization (NM93C66A when ORG = V_{CC} or NC)

Instruction	SB	OP-Code 2 Bits	Address 8 Bits	Data 16 Bits	Comments
READ	1	10	A7–A0		Read data stored in selected registers.
EWEN	1	00	11XXXXXX		Enables programming modes.
EWDS	1	00	00XXXXXX		Disables all programming modes.
ERASE	1	11	A7–A0		Erase selected register.
WRITE	1	01	A7–A0	D15–D0	Writes data pattern D15–D0 into selected register.
ERAL	1	00	10XXXXXX		Erases all registers.
WRAL	1	00	01XXXXXX	D15–D0	Writes data pattern D15–D0 into all registers.

512 by 8-Bit Organization (NM93C66A when ORG = GND)

Instruction	SB	OP-Code 2 Bits	Address 9 Bits	Data 8 Bits	Comments
READ	1	10	A8–A0		Read data stored in selected registers.
EWEN	1	00	11XXXXXXX		Enables programming modes.
EWDS	1	00	00XXXXXXX		Disables all programming modes.
ERASE	1	11	A8–A0		Erase selected register.
WRITE	1	01	A8–A0	D7–D0	Writes data pattern D7–D0 into selected register.
ERAL	1	00	10XXXXXXX		Erases all registers.
WRAL	1	00	01XXXXXXX	D7–D0	Writes data pattern D7–D0 into all registers.

Functional Description

Programming:

1. Programming is initiated by clocking in the Start Bit, Opcode bits, Address bits and the 8/16 data bits (refer to the ORG pin section).
2. Programming is started by bringing the CS pin low. Once the programming cycle is started, it cannot be stopped. (Bringing V_{CC} low will stop any programming, but will also result in data corruption.)
3. The status of the programming cycle (BUSY or READY) is observed by bringing the CS pin high and observing the output state. If the output is LOW, the device is still programming (BUSY). If the output is HIGH, the programming cycle has been completed and the device is ready for the next operation. Note that the output will be tri-stated each time CS is brought low and the R/B status will be shown each time CS is brought high.
4. After programming, the READY state (output HIGH) can be reset and the output tri-stated by clocking in a single Start Bit. This Start Bit can be the first bit in a command string, or CS can be brought low again to reset all internal circuits. In any case, clocking in a '1' bit will tri-state the output.

Read (READ):

The READ instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a serial-out shift register. A dummy bit (logical 0) precedes the serial data output string. Output data changes are initiated by a low to high transition of SK after the last address bit (A0) is clocked in.

Erase/Write Enable (EWEN):

When V_{CC} is applied to the part, it “powers up” in the Erase/Write Disable (EWDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once an Erase/Write Enable instruction is executed, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} is removed from the part.

Functional Description (Continued)

Erase/Write Disable (EWDS):

To protect against accidental data overwrites, the Erase/Write Disable (EWDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

Erase (ERASE):

The ERASE instruction will program all bits in the specified register to the logical “1” state. Please refer to the Programming section for details.

Write (WRITE):

The WRITE instruction is followed by 16 bits of data (or 8 bits of data when using the NM93C66A in the x8 organization) to be written into the specified address. Please refer to the Programming section for details.

Erase All (ERAL):

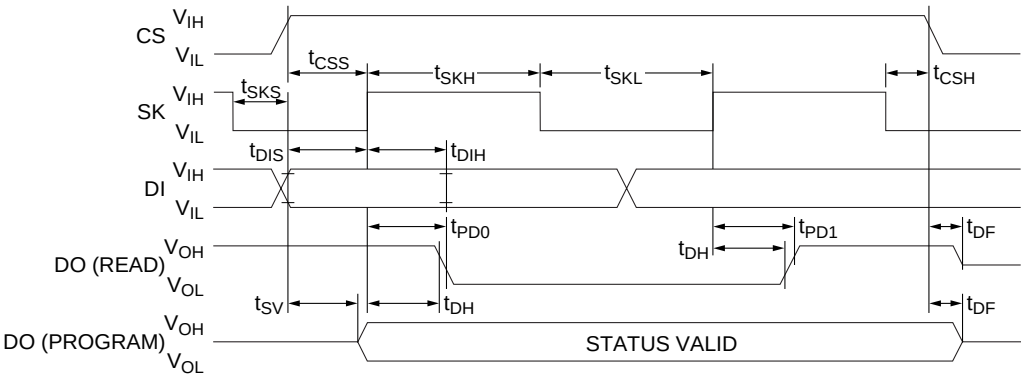
The ERAL instruction will simultaneously program all registers in the memory array to the logical “1” state.

Write All (WRAL):

The WRAL instruction will simultaneously program all registers with the data pattern specified in the instruction.

Timing Diagrams for the NM93C66A

Synchronous Data Timing



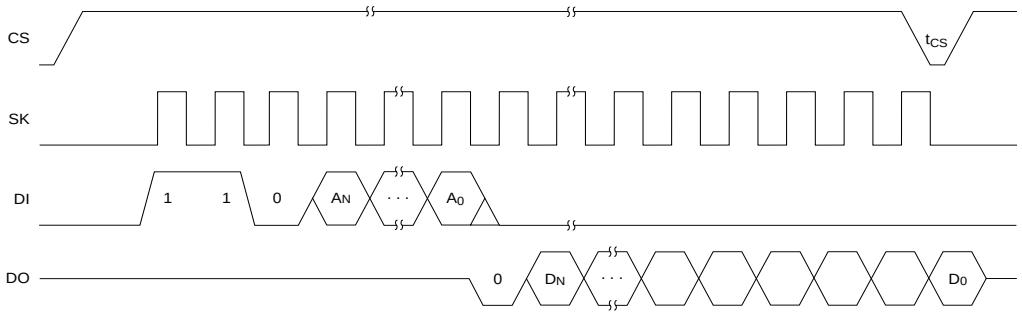
DS012510-4

Timing Diagrams for the NM93C66A (Continued)

Key for Timing Diagrams
Organization of Address and Data Fields for the NM93C66A

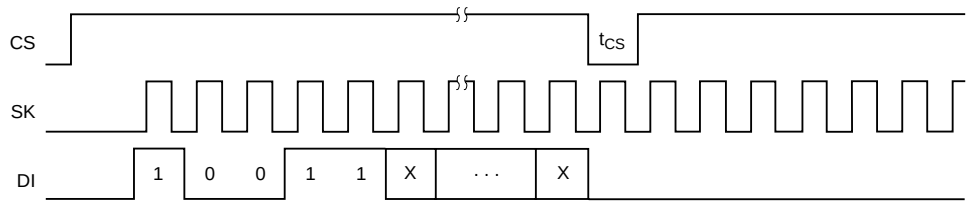
ORG Pin	Organization	A_N	D_N
V_{CC} or NC	256 x 16	A7	D15
V_{SS}	512 x 8	A8	D7

READ



DS012510-5

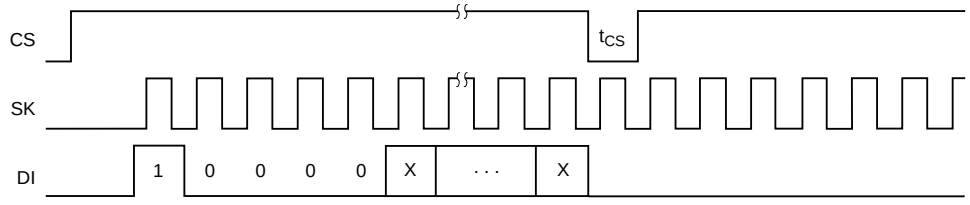
EWEN
DO = TRI-STATE



ORG = V_{CC}, 6 X'S
ORG = V_{SS}, 7 X'S

DS012510-6

EWDS
DO = TRI-STATE

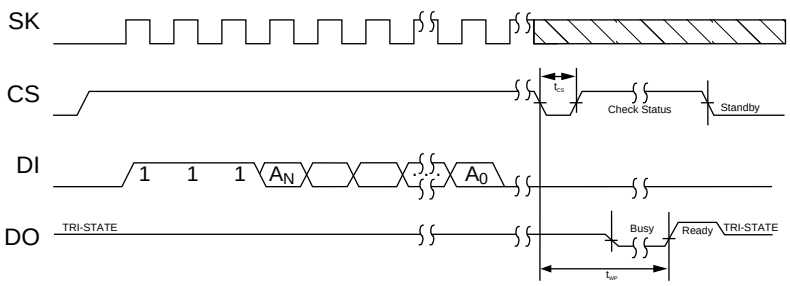


ORG = V_{CC}, 6 X'S
ORG = V_{SS}, 7 X'S

DS012510-7

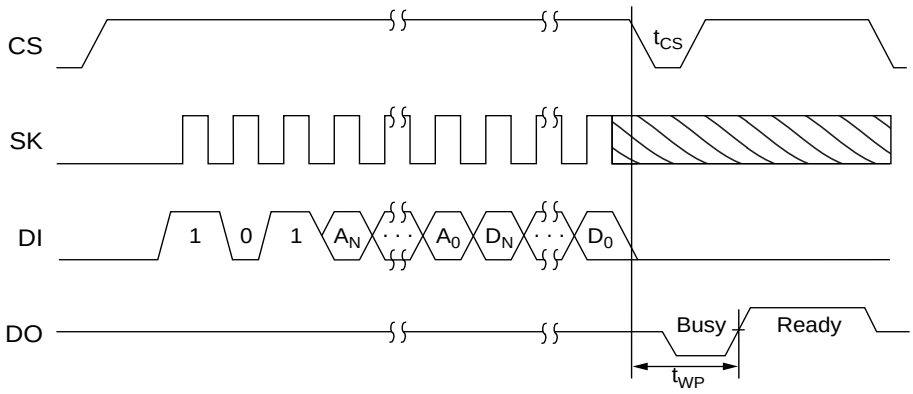
Timing Diagrams for the NM93C66A (Continued)

ERASE



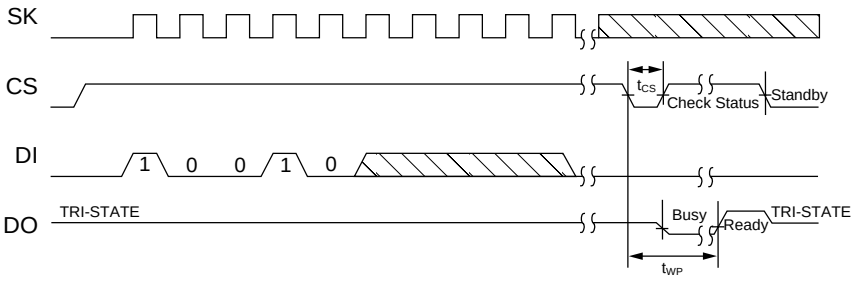
DS012510-8

WRITE



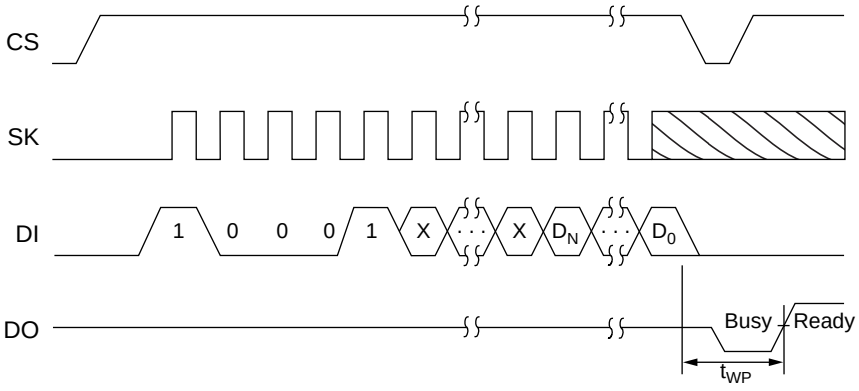
DS012510-9

ERAL



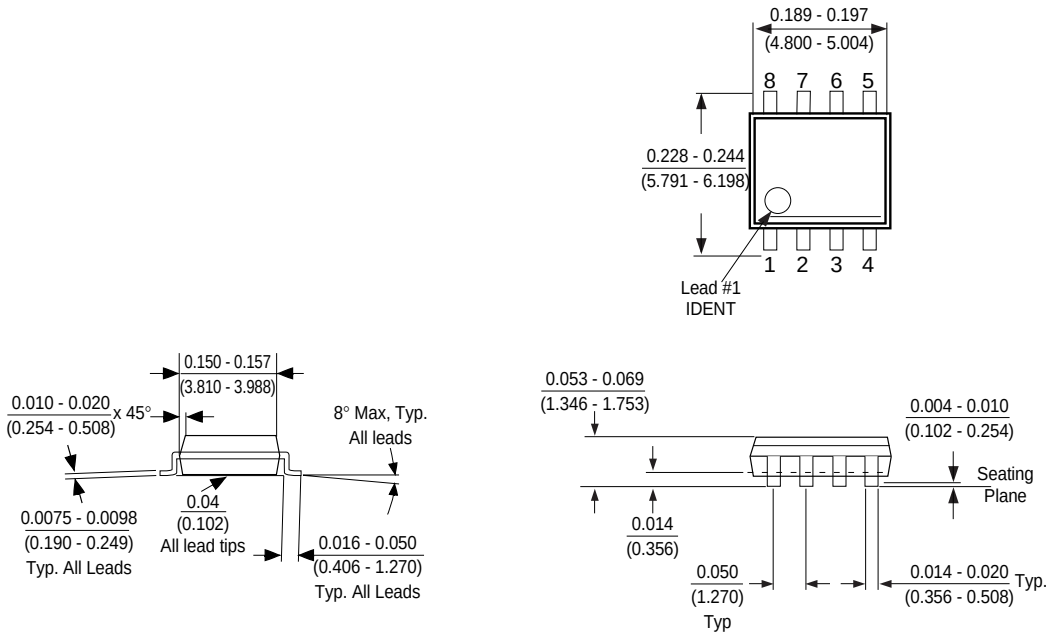
DS012510-10

WRAL



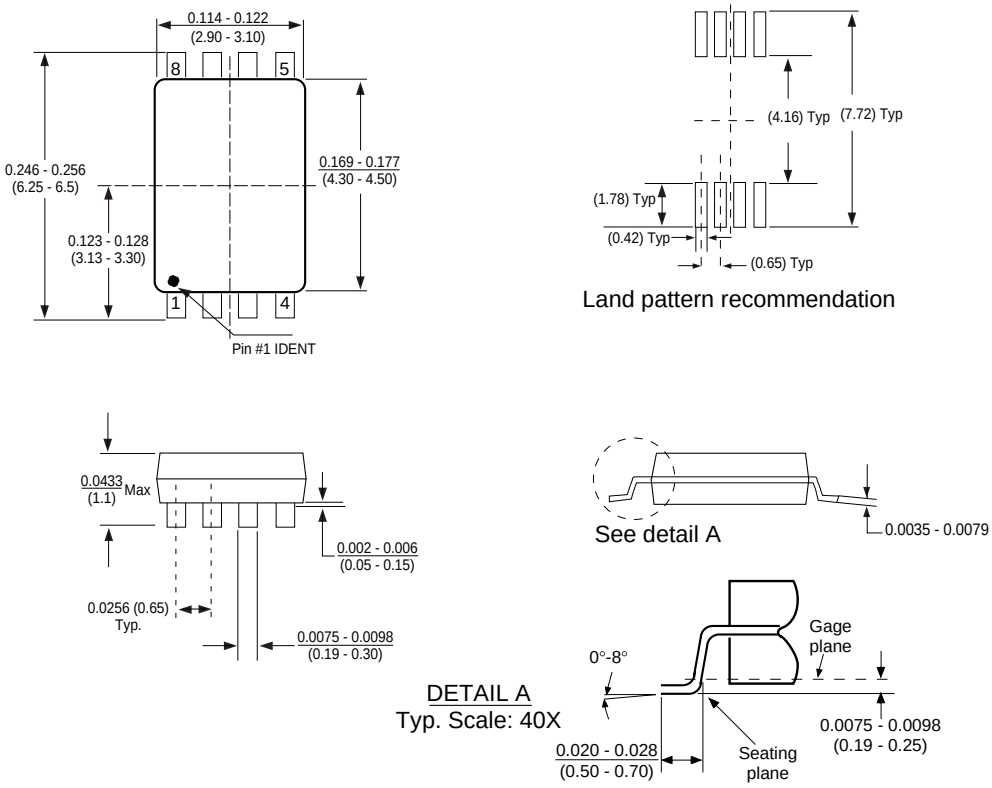
DS012510-11

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Small Outline Package (M8)
Package Number M08A

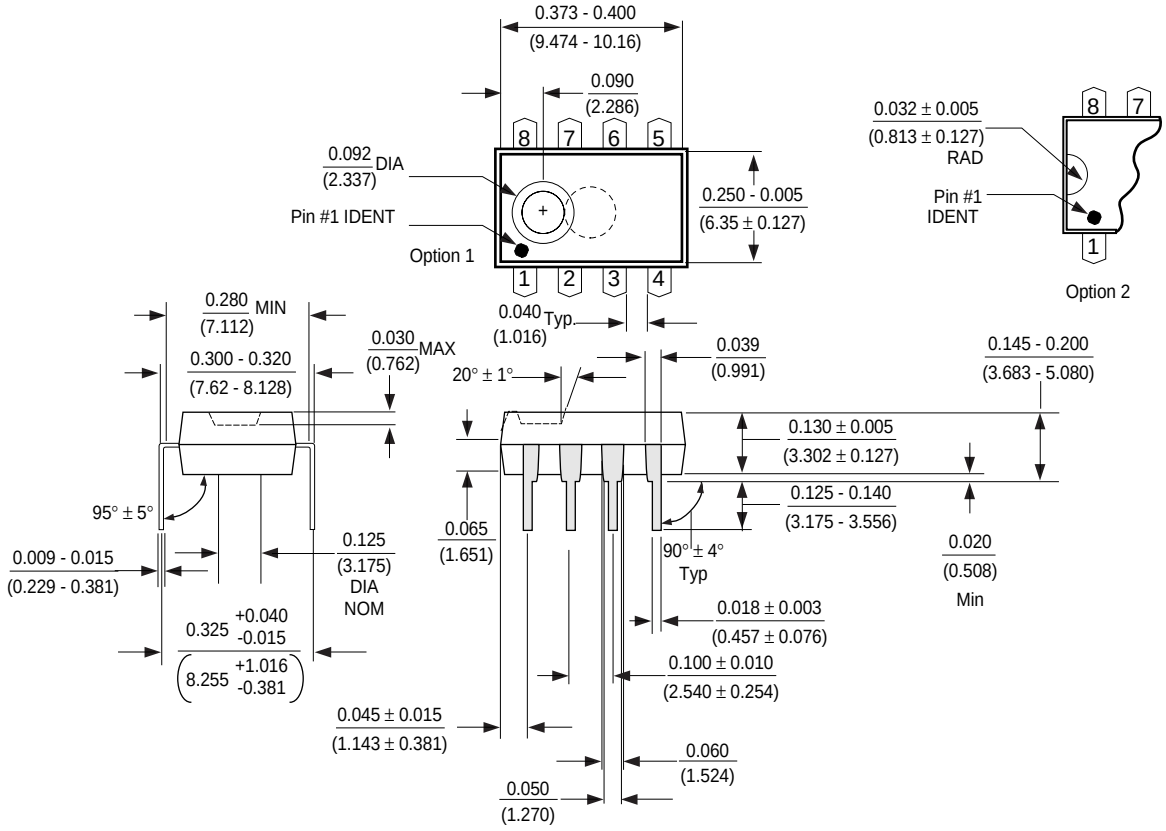
Physical Dimensions inches (millimeters) unless otherwise noted



Notes: Unless otherwise specified
1. Reference JEDEC registration MO153. Variation AA. Dated 7/93

8-Pin Molded TSSOP, JEDEC (MT8)
Package Number MTC08

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Package Number N08E

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

March 1999

NM93C86A
16K-Bit Serial EEPROM (MICROWIRE™ Bus Interface)

General Description

The NM93C86A is 16,384 bits of CMOS nonvolatile, electrically erasable memory available in user organized as either 1024 16-bit registers or 2048 8-bit registers. The user organization is determined by the status of the ORG input. The memory device is fabricated using Fairchild Semiconductor's floating gate CMOS process for high reliability, high endurance and low power consumption. The NM93C86A is available in 8-pin SO and TSSOP packages for space considerations.

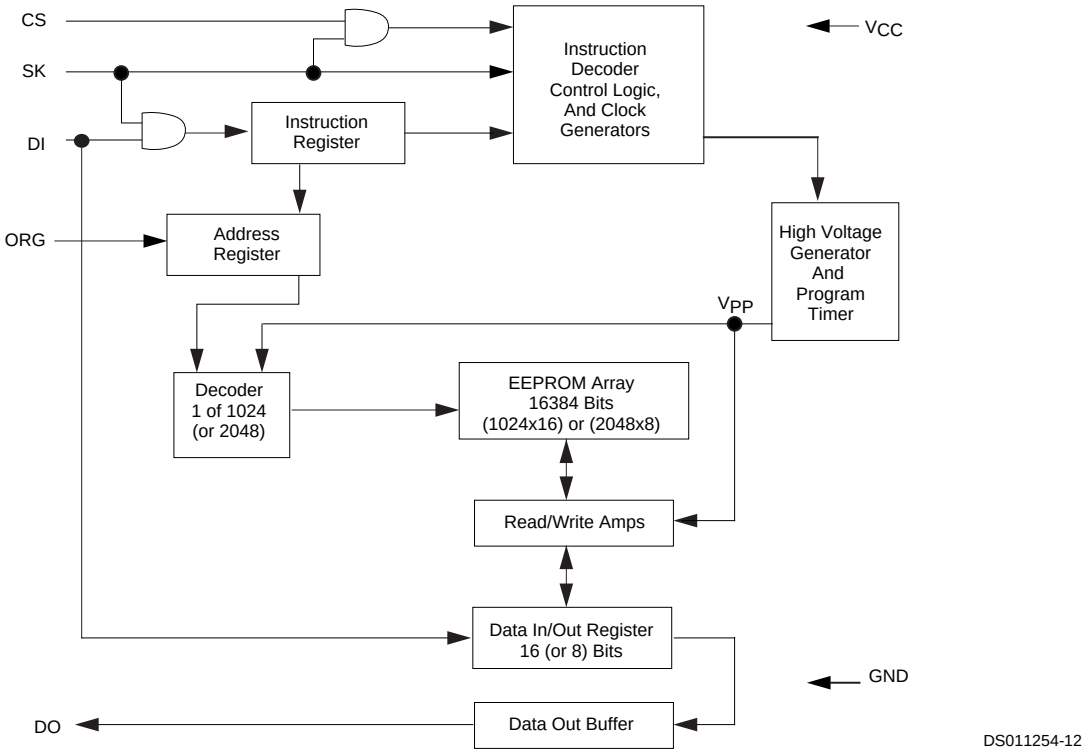
The EEPROM is MICROWIRE™ compatible for simple interfacing to a wide variety of microcontrollers and microprocessors. There are 7 instructions that operate the NM93C86A: Read, Erase/Write Enable, Erase, Write, Erase/Write Disable, Write All, and Erase All.

The NM93C86A defaults to the 1024 x 16 configuration if the ORG pin (Pin 6) is left floating, as it is internally pulled up to V_{CC}.

Features

- 2.7V to 5.5V operation in all modes
- Typical active current of 200μA
  10μA standby current typical
  1μA standby current typical (L)
  0.1μA standby current typical (LZ)
- Device status indication during programming mode
- No erase required before write
- Reliable CMOS floating gate technology
- MICROWIRE™ compatible serial I/O
- Self-timed programming cycle
- 40 years data retention
- Endurance: 1,000,000 data changes
- Packages available: 8-pin SO, 8-pin DIP

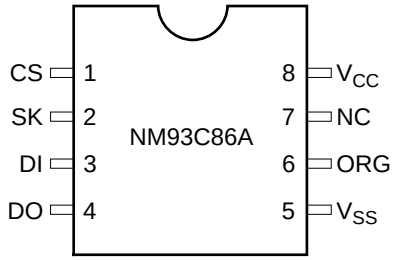
Block Diagram



DS011254-12

Connection Diagram

Dual-In-Line Package (N)
and 8-Pin SO Package (M8)



DS011254-14

Top View
See Package Number
N08E and M08A

Pin Names

Pin	Description
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V_{SS}	Ground
ORG	Memory Organization Select
NC	No Connect
V_{CC}	Positive Power Supply

Ordering Information

NM 93 C XX A LZ E XX

		Letter	Description
Package		N	8-Pin DIP
		M8	8-Pin SO8
Temp. Range		None	0 to 70°C
		V	-40 to +125°C
		E	-40 to +85°C
Voltage Operating Range		Blank	4.5V to 5.5V
		L	2.7V to 4.5V
		LZ	2.7V to 4.5V and <1µA Standby Current
		A	x8 or x16 Configuration
Density		86	16K
		C	CMOS
Interface		93	MICROWIRE
NM			**Fairchild Non-Volatile Memory**

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltage with Respect to Ground	V_{CC} + 1 to -0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V

Operating Range

Ambient Operating Temperature	
NM93C86A	0°C to +70°C
NM93C86AE	-40°C to +85°C
NM93C86AV	-40°C to +125°C
Power Supply (V_{CC}) Range	4.5V to 5.5V

DC and AC Electrical Characteristics $4.5V \le V_{CC} \le 5.5V$

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CCA}	Operating Current		CS = V_{IH}, SK=1 MHz		1	mA
I_{CCS}	Standby Current		CS = 0V ORG = V_{CC} or NC		50	µA
I_{IL}	Input Leakage		V_{IN} = 0V to V_{CC} (Note 2)	-1	1	µA
I_{ILO}	Input Leakage ORG Pin		ORG tied to V_{CC} ORG tied to V_{SS} (Note 3)	-1 -2.5	1 2.5	µA
I_{OL}	Output Leakage		V_{IN} = 0V to V_{CC}	-1	1	µA
V_{IL}	Input Low Voltage			-0.1	0.8	V
V_{IH}	Input High Voltage			2	V_{CC} +1	V
V_{OL1}	Output Low Voltage		I_{OL} = 2.1 mA		0.4	V
V_{OH1}	Output High Voltage		I_{OH} = -400 µA	2.4		V
V_{OL2}	Output Low Voltage		I_{OL} = 10 µA		0.2	V
V_{OH2}	Output High Voltage		I_{OL} = -10 µA	V_{CC} - 0.2		V
f_{SK}	SK Clock Frequency		(Note 4)	0	1	MHz
t_{SKH}	SK High Time	NM93C86A NM93C86AE/V		250 300		ns
t_{SKL}	SK Low Time			250		ns
t_{SKS}	SK Setup Time		SK must be at V_{IL} for t_{SKS} before CS goes high	50		ns
t_{CS}	Minimum CS Low Time		(Note 5)	250		ns
t_{CSS}	CS Set-up Time			50		ns
t_{DH}	DO Hold Time			70		ns
t_{DIS}	DI Set-up Time	NM93C86A NM93C86AE/V		100 200		ns
t_{CSH}	CS Hold Time			0		ns
t_{DIH}	DI Hold Time			20		ns
t_{PD1}	Output Delay to “1”				500	ns
t_{PD0}	Output Delay to “0”				500	ns
t_{SV}	CS to Status Valid				500	ns
t_{DF}	CS to DO in TRI-STATE®				100	ns
t_{WP}	Write Cycle Time				10	ms

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Range

Ambient Operating Temperature	
NM93C86AL/LZ	0°C to +70°C
NM93C86ALE/LZE	-40°C to +85°C
NM93C86ALV/LZV	-40°C to +125°C
Power Supply (V_{CC})	2.7V to 4.5V

Low V_{CC} (2.7V to 4.5V) DC and AC Electrical Characteristics

Symbol	Parameter	Part Number	Conditions	Min.	Max.	Units
I_{CCA}	Operating Current		CS = V_{IH}, SK = 250KHz		1	mA
I_{CCS}	Standby Current L LZ		CS = V_{IL}		 10 1	 µA µA
I_{IL}	Input Leakage		V_{IN} = 0V to V_{CC} (Note 2)		±1	µA
I_{ILO}	Input Leakage ORG Pin		ORG tied to V_{CC} ORG tied to V_{SS} (Note 3)	-1 -2.5	1 2.5	µA
I_{OL}	Output Leakage		V_{IN} = 0V to V_{CC}		±1	µA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			-0.1 0.8 V_{CC}	0.15 V_{CC} V_{CC} +1	V
V_{OL} V_{OH}	Output Low Voltage Output High Voltage		I_{OL} = 10 µA I_{OH} = -10 µA	 0.9 V_{CC}	0.1 V_{CC}	V V
f_{SK}	SK Clock Frequency		(Note 4)	0	250	KHz
t_{SKH}	SK High Time			1		µs
t_{SKL}	SK Low Time			1		µs
t_{SKS}	SK Setup Time		SK must be at V_{IL} for t_{SKS} before CS goes high	0.2		µs
t_{CS}	Minimum CS Low Time		(Note 5)	1		µs
t_{CSS}	CS Setup Time			0.2		µs
t_{DH}	DO Hold Time			70		ns
t_{DIS}	DI Setup Time			0.4		µs
t_{CSH}	CS Hold Time			0		ns
t_{DIH}	DI Hold Time			0.4		µs
t_{PD1}	Output Delay to "1"				2	µs
t_{PD0}	Output Delay to "0"				2	µs
t_{SV}	CS to Status Valid				1	µs
t_{DF}	CS to DO in TRI-STATE		CS = V_{IL}		0.4	µs
t_{WP}	Write Cycle Time				15	ms

Capacitance T_A = 25°C, f = 1 MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical leakage values are in the 20 nA range.

Note 3: The ORG pin may draw > 1 µA when in the x8 mode ude to an internal pull-up transistor.

Note 4: The shortest allowable SK clock period = $1/f_{SK}$ (as shown under the f_{SK} f_{SK} parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both t_{SKH} and t_{SKl} limits must be observed. Therefore, it is not allowable to set $1/f_{SK} = t_{SKHminimum} + t_{SKLminimum}$ for shorter SK cycle time operation.

Note 5: CS (Chip Select) must be brought low (to V_{IL}) for an interval of t_{CS} in order to reset all internal device registers (device reset) prior to beginning another opcode cycle. (This is shown in the opcode diagrams in the following pages.)

AC Test Conditions

V_{CC} Range	V_{IL}/V_{IH} Input Levels	V_{IL}/V_{IH} Timing Level	V_{OL}/V_{OH} Timing Level	I_{OL}/I_{OH}
2.7V ≤ V_{CC} ≤ 5.5V (Extended Voltage Levels)	.03V/1.8V	1.0V	0.8V/1.5V	±10µA
4.5V ≤ V_{CC} ≤ 5.5V (TTL Levels)	0.4V/2.4V	1.0V/2.0V	0.4V/2.4V	-2.1mA/0.4mA
Output Load: 1 TTL Gate (C_L = 100 pF)				

MICROWIRE I/O Pin Description

Chip Select (CS):

This pin enables and disables the MICROWIRE device and performs 2 general functions:

1. When in the low state, the MICROWIRE device is disabled and the output tri-stated (high impedance). If this pin is brought high (rising edge active), all internal registers are reset and the device is enabled, allowing MICROWIRE communication via DI/DO pins. To restate, the CS pin must be held high during all device communication and opcode functions. If the CS pin is brought low, all functions will be disabled and reset when CS is brought high again. The exception to this is when a programming cycle is initiated. Again, all activity on the CS, DI and DO pins is ignored until CS is brought high.
2. When programming is in progress, the Data-Out pin will display the programming status as either BUSY (DO low) or READY (DO high) when CS is brought high. (Again, the output will be tri-stated when CS is low.) To restate, during programming, the CS pin may be brought high and low any number of times to view the programming status without affect the programming operation. Once programming is completed (Output in READY state), the output is 'cleared' (returned to normal tri-state condition) by clocking in a Start Bit. After the Start Bit is clocked in, the output will return to a tri-stated condition. When clocked in, this Start Bit can be the first bit in a command string, or CS can be brought low again to reset all internal circuits.

   Unlike the lower density members of the Microwire product family (NM93C06, NM93C46, NM93C56, NM93C66) programming is not initiated by bringing CS low.

Instruction Set for the NM93C86A

ORG Pin Logic	Memory	
	Configuration	# of Address Bits
0	2048 x 8	11 Bits
1	1024 x 16	10 Bits

Serial Clock (SK):

This pin is the clock input (rising edge active) for clocking in all opcodes and data on the DI pin and clocking out all data on the DO pin. However, this pin has no effect on the asynchronous programming cycle (see the CD pin section) as the BUSY/READY status is a function of the CD pin only.

Data-In (DI):

All serial communication into the device is performed using this input pin (rising edge active). In order to avoid false Start Bits, or related issues, it is advised to keep the DI pin in the low state unless actually clocking in data bits (Start Bit, Opcode, Address or incoming data bits to be programmed). Please note that the first '1' clocked into the device (after CS is brought high) is seen as a Start Bit and the beginning of a serial command string, so caution must be observed when bringing CS high.

Data-Out (DO):

All serial communication out of the device (READ opcode) is performed using this output pin (rising edge active) as well as indicating the READY/BUSY status duting the asynchronous programming cycle. Note that, during READ operations, the output data is clocked out after the last address bit (A0) is clocked in. If a 3-wire application is required (where DI and DO are tied together), sections in AN-758, or related application notes, must be followed for correct operation.

Organization (ORG):

This pin controls the device architecture (8-bit data word vs. 16-bit data word). If the ORG pin is brought to V_{CC}, the device is configured with a 16-bit data word and if the ORG pin is brought to V_{SS} (Ground), the device is configured with an 8-bit data word (refer to other sections for details of both configurations). If the ORG pin is left floating, the device will default to a 16-bit data word.

1024 by 16-Bit Organization (NM93C86A when ORG = V_{CC} or NC)

Instruction	SB	Op Code 2 Bits	Address 10 Bits	Data 16 Bits	Function
READ	1	10	A9–A0		Read data stored in selected registers.
EWEN	1	00	11XXXXXXXX		Enables programming modes.
EWDS	1	00	00XXXXXXXX		Disables all programming modes.
ERASE	1	11	A9–A0		Erases selected register.
WRITE	1	01	A9–A0	D15–D0	Writes data pattern D15–D0 into selected register.
ERAL	1	00	10XXXXXXXX		Erases all registers.
WRAL	1	00	01XXXXXXXX	D15–D0	Writes data pattern D15–D0 into all registers.

2048 by 8-Bit Organization (NM93C86A when ORG = GND)

Instruction	SB	Op Code 2 Bits	Address 11 Bits	Data 8 Bits	Function
READ	1	10	A10–A0		Read data stored in selected registers.
EWEN	1	00	11XXXXXXXXX		Enables programming modes.
EWDS	1	00	00XXXXXXXXX		Disables all programming modes.
ERASE	1	11	A10–A0		Erases selected register.
WRITE	1	01	A10–A0	D7–D0	Writes data pattern D7–D0 into selected register.
ERAL	1	00	10XXXXXXXXX		Erases all registers.
WRAL	1	00	01XXXXXXXXX	D7–D0	Writes data pattern D7–D0 into all registers.

Functional Description

Programming

The programming cycle is automatically started after entering the LAST bit of the programming instruction string (unlike other Microwire family members which use CS to initiate programming). This feature, counting the number of instruction bits, decreases the likelihood of inadvertent programming and allows the programming to be cancelled before sending out the last bit in the string (be bringing CS low).

Programming Instruction	Last Bit in String
WRITE	D0
WRAL	D0
ERASE	A0
ERAL	A0

Note that, in the ERASE/ERAL instructions, the A0 bit is the last bit in the string and clocking in that bit will initiate programming. In order to maintain compatibility, **CS may be brought low after clocking in the last bit, but it is not necessary.**

In all programming modes the READY/BUSY status of the device can be determined by polling the DO pin. After clocking in the last bit of the instruction sequence and with the CS held "high", the DO pin will exit the high impedance state and indicate the READY/BUSY status of the device. DO = logical "0" indicates that programming is still in progress and no other instruction can be executed. DO = logical "1" indicates that the device is READY for another instruction. If CS is forced "low" the DO pin will return to the high impedance state. After the programming cycle has been completed and DO = logical "1", the DO pin can be reset back to the high impedance state by clocking a logical "1" into the DI pin. (This is also performed with the start bit on all op codes, thus clocking an instruction has the same effect.)

Read (READ)

The READ instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a serial-out shift register. A dummy bit (logical 0) precedes the serial data output string. Output data changes are initiated by a low to high transition of SK clock after the last address bit (A0) is clocked in.

Erase/Write Enable (EWEN)

When V_{CC} is applied to the part, it "powers up" in the Erase/Write Disable (EWDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once an Erase/Write Enable instruction is executed, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} is removed from the part.

Functional Description (Continued)

Erase/Write Disable (EWDS)

To protect against accidental data overwrites, the Erase/Write Disable (EWDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

Erase (ERASE)

The ERASE instruction will program all bits in the specified register to the logical "1" state. The self-timed programming cycle is initiated on the rising edge of the SK clock as the last address bit (A0) is clocked in. At this point CS, SK and DI become don't care states. After starting an Erase cycle the DO pin indicates the READY/BUSY status of the chip if CS is held "high". DO = logical "0" indicates that programming is still in progress. DO = logical "1" indicates that the register, at the address specified in the instruction, has been erased.

Write (WRITE)

The WRITE instruction is followed by 16 bits of data (or 8 bits of data when using the NM93C86A in the x8 organization) to be written into the specified address. Note that if the CS is brought "low" before clocking in all of the data bits, then the WRITE instruction will be aborted. The self-timed programming cycle is initiated on the rising edge of the SK clock as the last data bit (D0) is clocked in. At this point, CS, SK and DI become don't care states. No separate ERASE cycle is required before a WRITE instruction.

As in the ERASE instruction, after starting a WRITE cycle, the DO pin indicates the READY/BUSY status of the chip if CS is held "high". DO = logical "0" indicates that programming is still in progress. DO = logical "1" indicates that the register, at the address specified in the instruction, has been written and that the part is ready for another instruction.

Erase All (ERAL)

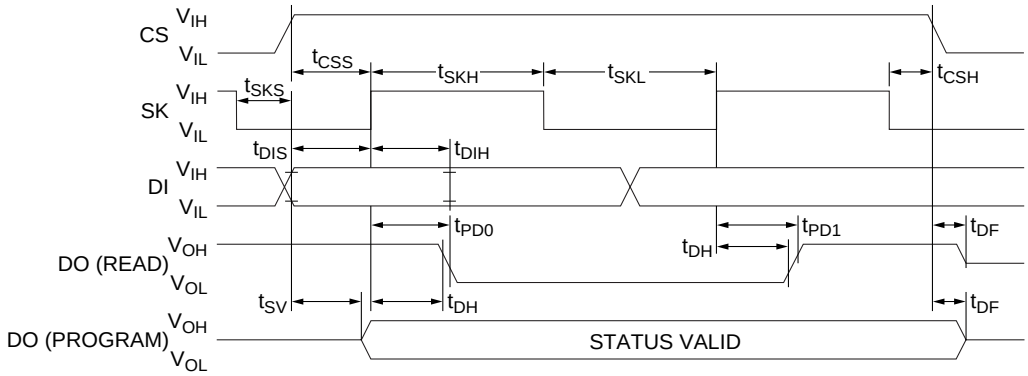
The ERAL instruction will simultaneously program all registers in the memory array to the logical "1" state.

Write All (WRAL)

The WRAL instruction will simultaneously program all registers with the data pattern specified in the instruction.

Timing Diagrams for the NM93C86A

Synchronous Data Timing



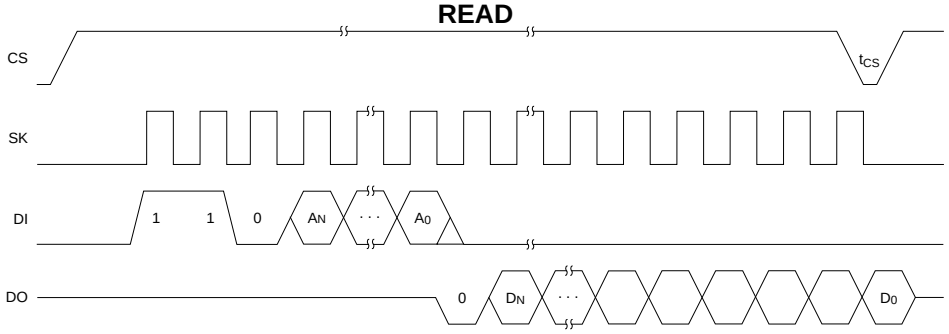
DS011254-3

Timing Diagrams for the NM93C86A (Continued)

Key for Timing Diagrams
Organization of Address and Data Fields for the NM93C86A

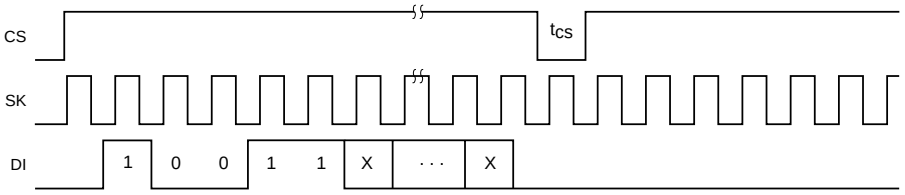
ORG	Organization	A_N	D_N
V_{CC} or NC	1024 x 16	A9	D15
V_{SS}	2048 x 8	A10	D7

READ



DS011254-4

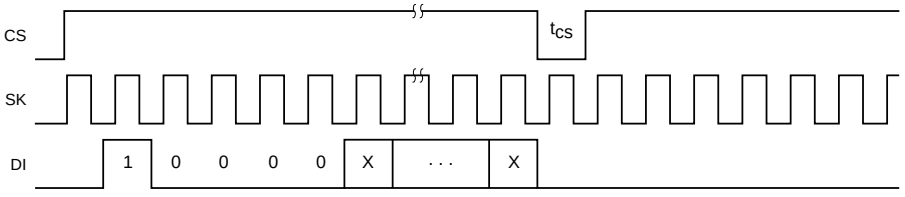
EWEN
DO = TRI-STATE



ORG = V_{CC}, 8 X's
ORG = V_{SS}, 9 X's

DS011254-5

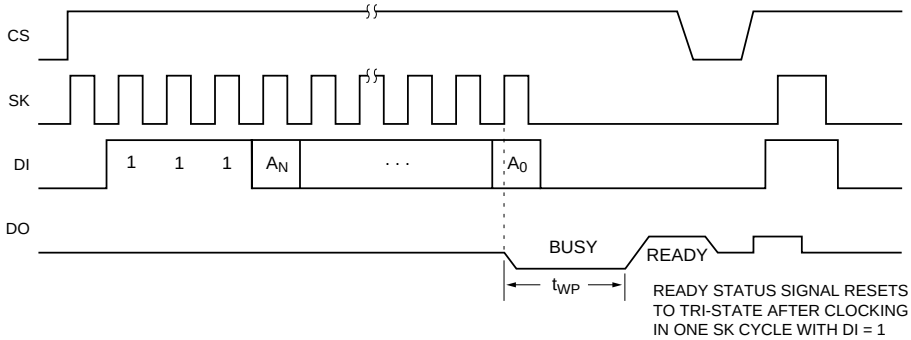
EWDS
DO = TRI-STATE



ORG = V_{CC}, 8 X's
ORG = V_{SS}, 9 X's

DS011254-6

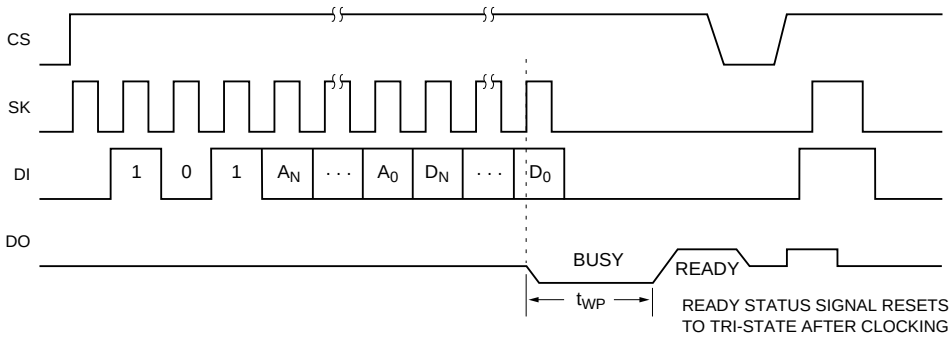
ERASE



DS011254-7

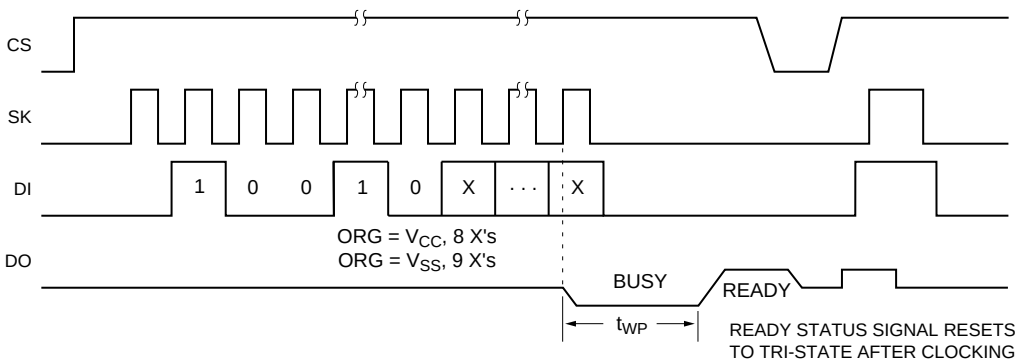
Timing Diagrams for the NM93C86A (Continued)

WRITE



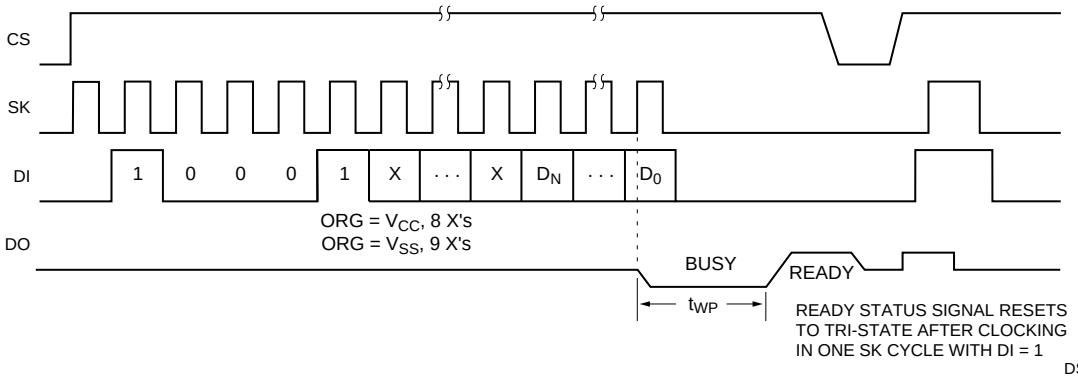
DS011254-8

ERAL



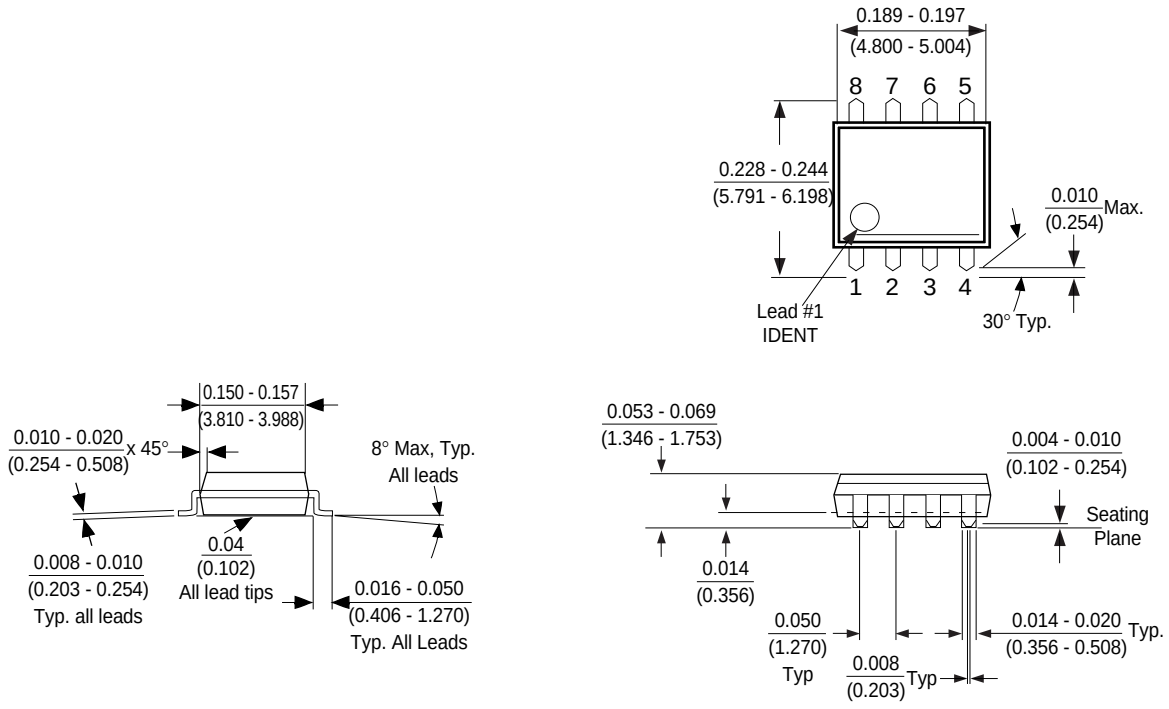
DS011254-9

WRAL

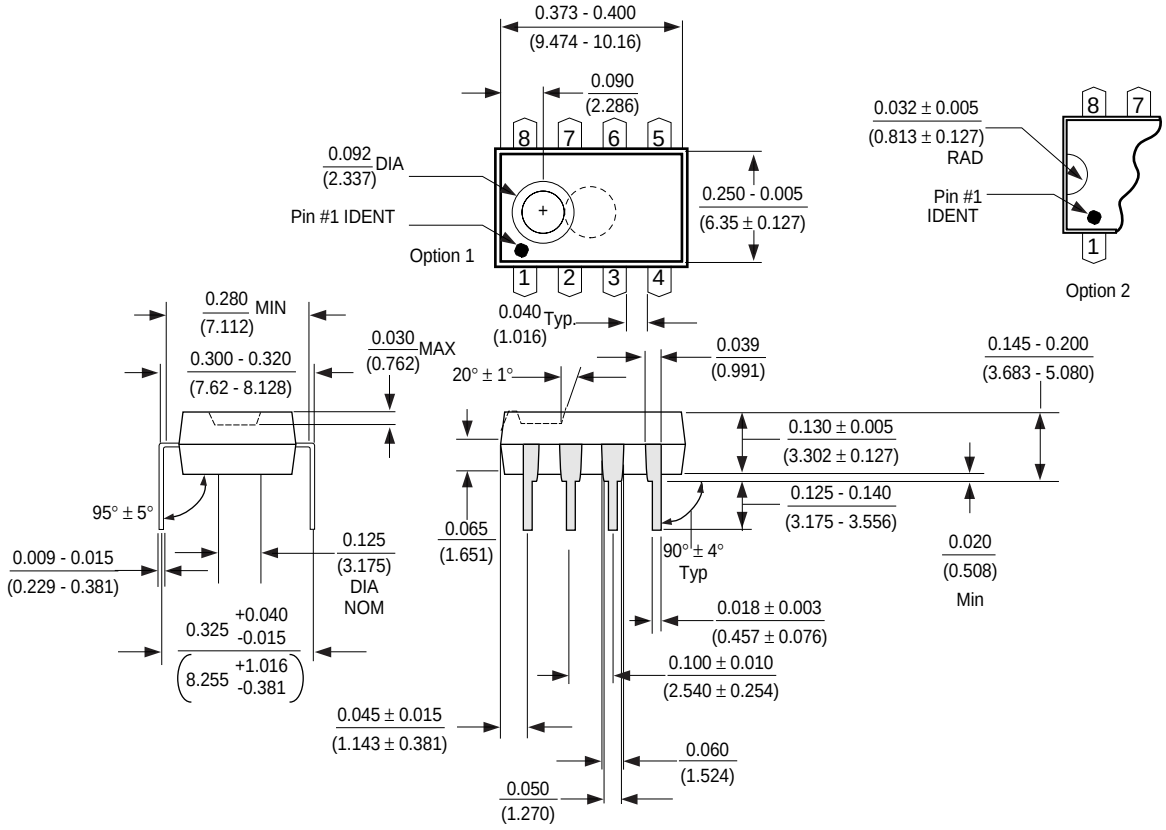


DS011254-10

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Small Outline Package (M8)
Package Number M08A



Molded Dual-in-Line Package (N)
Package Number N08E

Life Support Policy

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

May 1999

NM93C86AU
16K-Bit MICROWIRE™ Interface Serial EEPROM

General Description

The NM93C86AU is a 16K (16,384) bit serial interface CMOS EEPROM (Electrically Erasable Programmable Read-Only Memory). This device fully conforms to the MICROWIRE™ 4-wire protocol which uses Chip Select (CS), Clock (SK). Data-in (DI) and Data-out (DO) pins to synchronously control the EEPROM data transfer and the ORG pin, which allows configuring the part for an 8-bit or 16-bit data format. In addition, the serial interface allows a minimal pin count, packaging designed to simplify PC board layout requirements and offers the designer a variety of low voltage and low power options.

The NM93C86AU MICROWIRE EEPROM offers the user the ability to configure the EEPROM as a 16-bit dataword (ORG pin = V_{CC}; 16 bits x 1,024 addresses) or an 8-bit data byte (ORG pin = V_{SS}; 8 bits x 2,048 addresses).

Fairchild EEPROMs are designed and tested for applications requiring high endurance, high reliability, and low power consumption for a continuously reliable non-volatile solution for all markets.

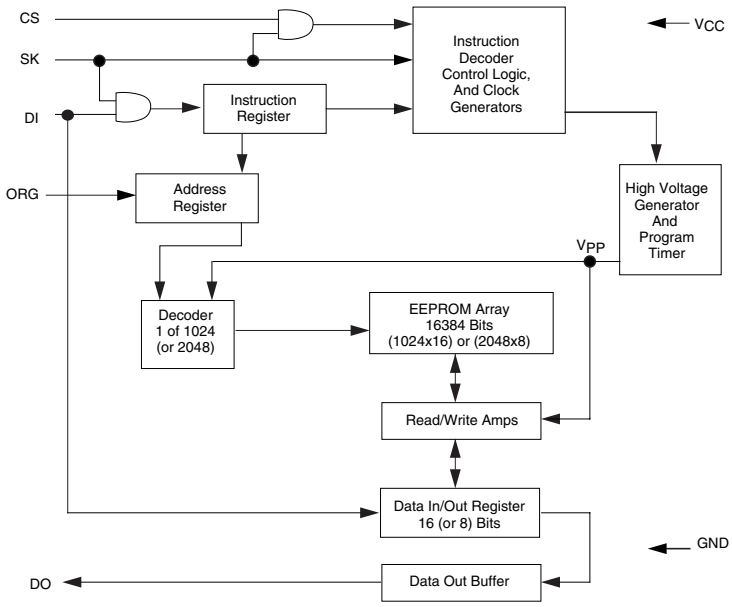
Functions

- MICROWIRE™ 4-wire interface
- 16K bits organized as 8 x 2,048 or 16 x 1,024 organization (ORG pin control)
- Extended 2.7V to 5.5V operating voltage
- 1MHz operation
- Self-timed programming cycle (6ms typical)
- "Programming complete" indicated by DO Ready/Busy polling

Features

- The MICROWIRE interface offers the greatest ease of use vs. clock rate of serial data transfer methods
- Bulk mode programming to allow simultaneous programming of all addresses
- Low V_{CC} Programming Lockout (3.8V)
  — "H" option (Standard V_{CC} range) parts only
- Schmitt trigger (hysteresis) on all inputs
- Typical 200µA active current (I_{CCA})
- Typical 1µA standby current (I_{SB}) for "L" devices and 0.1µA standby current for "LZ" devices
- Endurance: Up to 1,000,000 data changes
- Data retention greater than 40 years

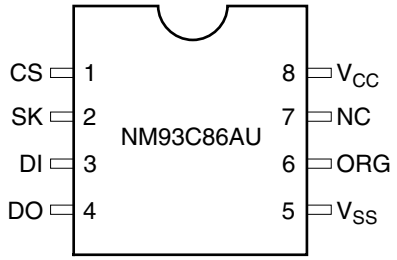
Block Diagram



DS800021-12

Connection Diagram

Dual-In-Line Package (N)
and 8-Pin SO Package (M8)



DS800021-14

Top View
See Package Number
N08E and M08A

Pin Names

Pin	Description
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V_{SS}	Ground
ORG	Memory Organization Select
NC	No Connect
V_{CC}	Positive Power Supply

Ordering Information

NM 93 C XX A U LZ E XX

		Letter	Description
Package		N	8-Pin DIP
		M8	8-Pin SO8
Temp. Range		None	0 to 70°C
		V	-40 to +125°C
		E	-40 to +85°C
Voltage Operating Range		Blank	4.5V to 5.5V
		L	2.7V to 4.5V
		LZ	2.7V to 4.5V and <1μA Standby Current
		H	4.5 to 5.5V and V_{CC} Lockout
		Ultralite	CS100UL Process
		A	x8 or x16 Configuration
Density		86	16K
		C	CMOS
Interface		93	MICROWIRE
		NM	**Fairchild Non-Volatile Memory**

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltage with Respect to Ground	V_{CC} + 1 to -0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V

Operating Range

Ambient Operating Temperature	
NM93C86AU	0°C to +70°C
NM93C86AUE	-40°C to +85°C
NM93C86AUV	-40°C to +125°C
Power Supply (V_{CC}) Range	
NM93C86AU/NM93C86AUH	4.5V to 5.5V

DC and AC Electrical Characteristics $4.5V \le V_{CC} \le 5.5V$

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CCA}	Operating Current		CS = V_{IH}, SK=1 MHz		1	mA
I_{CCS}	Standby Current		CS = 0V ORG = V_{CC} or NC		50	µA
I_{IL}	Input Leakage		V_{IN} = 0V to V_{CC} (Note 2)	-1	1	µA
I_{ILO}	Input Leakage ORG Pin		ORG tied to V_{CC} ORG tied to V_{SS} (Note 3)	-1 -2.5	1 2.5	µA
I_{OL}	Output Leakage		V_{IN} = 0V to V_{CC}	-1	1	µA
V_{IL}	Input Low Voltage			-0.1	0.8	V
V_{IH}	Input High Voltage			2	V_{CC} +1	V
V_{OL1}	Output Low Voltage		I_{OL} = 2.1 mA		0.4	V
V_{OH1}	Output High Voltage		I_{OH} = -400 µA	2.4		V
V_{OL2}	Output Low Voltage		I_{OL} = 10 µA		0.2	V
V_{OH2}	Output High Voltage		I_{OL} = -10 µA	V_{CC} - 0.2		V
f_{SK}	SK Clock Frequency		(Note 4)	0	1	MHz
t_{SKH}	SK High Time	NM93C86AU NM93C86AUE/V		250 300		ns
t_{SKL}	SK Low Time			250		ns
t_{SKS}	SK Setup Time		SK must be at V_{IL} for t_{SKS} before CS goes high	50		ns
t_{CS}	Minimum CS Low Time		(Note 5)	250		ns
t_{CSS}	CS Set-up Time			50		ns
t_{DH}	DO Hold Time			70		ns
t_{DIS}	DI Set-up Time	NM93C86AU NM93C86AUE/V		100 200		ns
t_{CSH}	CS Hold Time			0		ns
t_{DIH}	DI Hold Time			20		ns
t_{PD1}	Output Delay to “1”				500	ns
t_{PD0}	Output Delay to “0”				500	ns
t_{SV}	CS to Status Valid				500	ns
t_{DF}	CS to DO in TRI-STATE®				100	ns
t_{WP}	Write Cycle Time				10	ms

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Range

Ambient Operating Temperature	
NM93C86AUL/LZ	0°C to +70°C
NM93C86AULE/LZE	-40°C to +85°C
NM93C86AULV/LZV	-40°C to +125°C
Power Supply (V_{CC})	2.7V to 4.5V

Low V_{CC} (2.7V to 4.5V) DC and AC Electrical Characteristics

Symbol	Parameter	Part Number	Conditions	Min.	Max.	Units
I_{CCA}	Operating Current		CS = V_{IH}, SK = 250KHz		1	mA
I_{CCS}	Standby Current L LZ		CS = V_{IL}		 10 1	 µA µA
I_{IL}	Input Leakage		V_{IN} = 0V to V_{CC} (Note 2)		±1	µA
I_{ILO}	Input Leakage ORG Pin		ORG tied to V_{CC} ORG tied to V_{SS} (Note 3)	-1 -2.5	1 2.5	µA
I_{OL}	Output Leakage		V_{IN} = 0V to V_{CC}		±1	µA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			-0.1 0.8 V_{CC}	0.15 V_{CC} V_{CC} +1	V
V_{OL} V_{OH}	Output Low Voltage Output High Voltage		I_{OL} = 10 µA I_{OH} = -10 µA	 0.9 V_{CC}	0.1 V_{CC}	V V
f_{SK}	SK Clock Frequency		(Note 4)	0	250	KHz
t_{SKH}	SK High Time			1		µs
t_{SKL}	SK Low Time			1		µs
t_{SKS}	SK Setup Time		SK must be at V_{IL} for t_{SKS} before CS goes high	0.2		µs
t_{CS}	Minimum CS Low Time		(Note 5)	1		µs
t_{CSS}	CS Setup Time			0.2		µs
t_{DH}	DO Hold Time			70		ns
t_{DIS}	DI Setup Time			0.4		µs
t_{CSH}	CS Hold Time			0		ns
t_{DIH}	DI Hold Time			0.4		µs
t_{PD1}	Output Delay to "1"				2	µs
t_{PD0}	Output Delay to "0"				2	µs
t_{SV}	CS to Status Valid				1	µs
t_{DF}	CS to DO in TRI-STATE		CS = V_{IL}		0.4	µs
t_{WP}	Write Cycle Time				15	ms

Capacitance T_A = 25°C, f = 1 MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical leakage values are in the 20 nA range.

Note 3: The ORG pin may draw > 1 µA when in the x8 mode ude to an internal pull-up transistor.

Note 4: The shortest allowable SK clock period = $1/f_{SK}$ (as shown under the f_{SK} f_{SK} parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both t_{SKH} and t_{SKL} limits must be observed. Therefore, it is not allowable to set $1/f_{SK} = t_{SKHminimum} + t_{SKLminimum}$ for shorter SK cycle time operation.

Note 5: CS (Chip Select) must be brought low (to V_{IL}) for an interval of t_{CS} in order to reset all internal device registers (device reset) prior to beginning another opcode cycle. (This is shown in the opcode diagrams in the following pages.)

AC Test Conditions

V_{CC} Range	V_{IL}/V_{IH} Input Levels	V_{IL}/V_{IH} Timing Level	V_{OL}/V_{OH} Timing Level	I_{OL}/I_{OH}
2.7V ≤ V_{CC} ≤ 5.5V (Extended Voltage Levels)	.03V/1.8V	1.0V	0.8V/1.5V	±10µA
4.5V ≤ V_{CC} ≤ 5.5V (TTL Levels)	0.4V/2.4V	1.0V/2.0V	0.4V/2.4V	-2.1mA/0.4mA
Output Load: 1 TTL Gate (C_L = 100 pF)				

MICROWIRE I/O Pin Description

Chip Select (CS):

This pin enables and disables the MICROWIRE device and performs 2 general functions:

1. When in the low state, the MICROWIRE device is disabled and the output tri-stated (high impedance). If this pin is brought high (rising edge active), all internal registers are reset and the device is enabled, allowing MICROWIRE communication via DI/DO pins. To restate, the CS pin must be held high during all device communication and opcode functions. If the CS pin is brought low, all functions will be disabled and reset when CS is brought high again. The exception to this is when a programming cycle is initiated. Again, all activity on the CS, DI and DO pins is ignored until CS is brought high.
2. When programming is in progress, the Data-Out pin will display the programming status as either BUSY (DO low) or READY (DO high) when CS is brought high. (Again, the output will be tri-stated when CS is low.) To restate, during programming, the CS pin may be brought high and low any number of times to view the programming status without affect the programming operation. Once programming is completed (Output in READY state), the output is 'cleared' (returned to normal tri-state condition) by clocking in a Start Bit. After the Start Bit is clocked in, the output will return to a tri-stated condition. When clocked in, this Start Bit can be the first bit in a command string, or CS can be brought low again to reset all internal circuits.

   Unlike the lower density members of the Microwire product family (NM93C06, NM93C46, NM93C56, NM93C66) programming is not initiated by bringing CS low.

Serial Clock (SK):

This pin is the clock input (rising edge active) for clocking in all opcodes and data on the DI pin and clocking out all data on the DO pin. However, this pin has no effect on the asynchronous programming cycle (see the CD pin section) as the BUSY/READY status is a function of the CD pin only.

Data-In (DI):

All serial communication into the device is performed using this input pin (rising edge active). In order to avoid false Start Bits, or related issues, it is advised to keep the DI pin in the low state unless actually clocking in data bits (Start Bit, Opcode, Address or incoming data bits to be programmed). Please note that the first '1' clocked into the device (after CS is brought high) is seen as a Start Bit and the beginning of a serial command string, so caution must be observed when bringing CS high.

Data-Out (DO):

All serial communication out of the device (READ opcode) is performed using this output pin (rising edge active) as well as indicating the READY/BUSY status duting the asynchronous programming cycle. Note that, during READ operations, the output data is clocked out after the last address bit (A0) is clocked in. If a 3-wire application is required (where DI and DO are tied together), sections in AN-758, or related application notes, must be followed for correct operation.

Organization (ORG):

This pin controls the device architecture (8-bit data word vs. 16-bit data word). If the ORG pin is brought to V_{CC}, the device is configured with a 16-bit data word and if the ORG pin is brought to V_{SS} (Ground), the device is configured with an 8-bit data word (refer to other sections for details of both configurations). If the ORG pin is left floating, the device will default to a 16-bit data word.

Instruction Set for the NM93C86AU

ORG Pin Logic	Memory	
	Configuration	# of Address Bits
0	2048 x 8	11 Bits
1	1024 x 16	10 Bits

1024 by 16-Bit Organization (NM93C86AU when ORG = V_{CC} or NC)

Instruction	SB	Op Code 2 Bits	Address 10 Bits	Data 16 Bits	Function
READ	1	10	A9–A0		Read data stored in selected registers.
EWEN	1	00	11XXXXXXXX		Enables programming modes.
EWDS	1	00	00XXXXXXXX		Disables all programming modes.
ERASE	1	11	A9–A0		Erases selected register.
WRITE	1	01	A9–A0	D15–D0	Writes data pattern D15–D0 into selected register.
ERAL	1	00	10XXXXXXXX		Erases all registers.
WRAL	1	00	01XXXXXXXX	D15–D0	Writes data pattern D15–D0 into all registers.

2048 by 8-Bit Organization (NM93C86AU when ORG = GND)

Instruction	SB	Op Code 2 Bits	Address 11 Bits	Data 8 Bits	Function
READ	1	10	A10–A0		Read data stored in selected registers.
EWEN	1	00	11XXXXXXXXX		Enables programming modes.
EWDS	1	00	00XXXXXXXXX		Disables all programming modes.
ERASE	1	11	A10–A0		Erases selected register.
WRITE	1	01	A10–A0	D7–D0	Writes data pattern D7–D0 into selected register.
ERAL	1	00	10XXXXXXXXX		Erases all registers.
WRAL	1	00	01XXXXXXXXX	D7–D0	Writes data pattern D7–D0 into all registers.

Functional Description

Programming

The programming cycle is automatically started after entering the LAST bit of the programming instruction string (unlike other Microwire family members which use CS to initiate programming). This feature, counting the number of instruction bits, decreases the likelihood of inadvertent programming and allows the programming to be cancelled before sending out the last bit in the string (be bringing CS low).

Programming Instruction	Last Bit in String
WRITE	D0
WRAL	D0
ERASE	A0
ERAL	A0

Note that, in the ERASE/ERAL instructions, the A0 bit is the last bit in the string and clocking in that bit will initiate programming. In order to maintain compatibility, **CS may be brought low after clocking in the last bit, but it is not necessary.**

In all programming modes the READY/BUSY status of the device can be determined by polling the DO pin. After clocking in the last bit of the instruction sequence and with the CS held "high", the DO pin will exit the high impedance state and indicate the READY/BUSY status of the device. DO = logical "0" indicates that programming is still in progress and no other instruction can be executed. DO = logical "1" indicates that the device is READY for another instruction. If CS is forced "low" the DO pin will return to the high impedance state. After the programming cycle has been completed and DO = logical "1", the DO pin can be reset back to the high impedance state by clocking a logical "1" into the DI pin. (This is also performed with the start bit on all op codes, thus clocking an instruction has the same effect.)

Read (READ)

The READ instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a serial-out shift register. A dummy bit (logical 0) precedes the serial data output string. Output data changes are initiated by a low to high transition of SK clock after the last address bit (A0) is clocked in.

Erase/Write Enable (EWEN)

When V_{CC} is applied to the part, it "powers up" in the Erase/Write Disable (EWDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once an Erase/Write Enable instruction is executed, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} is removed from the part.

Functional Description (Continued)

Erase/Write Disable (EWDS)

To protect against accidental data overwrites, the Erase/Write Disable (EWDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

Erase (ERASE)

The ERASE instruction will program all bits in the specified register to the logical "1" state. The self-timed programming cycle is initiated on the rising edge of the SK clock as the last address bit (A0) is clocked in. At this point CS, SK and DI become don't care states. After starting an Erase cycle the DO pin indicates the READY/BUSY status of the chip if CS is held "high". DO = logical "0" indicates that programming is still in progress. DO = logical "1" indicates that the register, at the address specified in the instruction, has been erased.

Write (WRITE)

The WRITE instruction is followed by 16 bits of data (or 8 bits of data when using the NM93C86AU in the x8 organization) to be written into the specified address. Note that if the CS is brought "low" before clocking in all of the data bits, then the WRITE instruction will be aborted. The self-timed programming cycle is initiated on the rising edge of the SK clock as the last data bit (D0) is clocked in. At this point, CS, SK and DI become don't care states. No separate ERASE cycle is required before a WRITE instruction.

As in the ERASE instruction, after starting a WRITE cycle, the DO pin indicates the READY/BUSY status of the chip if CS is held "high". DO = logical "0" indicates that programming is still in progress. DO = logical "1" indicates that the register, at the address specified in the instruction, has been written and that the part is ready for another instruction.

Erase All (ERAL)

The ERAL instruction will simultaneously program all registers in the memory array to the logical "1" state.

Write All (WRAL)

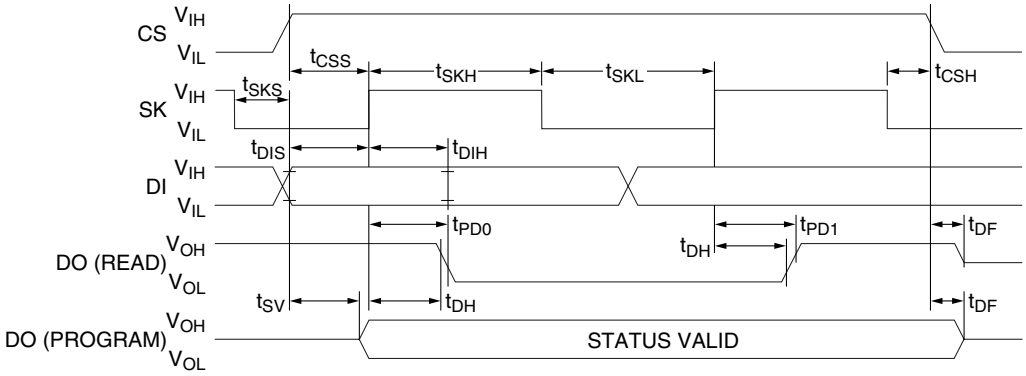
The WRAL instruction will simultaneously program all registers with the data pattern specified in the instruction.

Low V_{CC} Lockout

The NM93C86AxHx ("H" option) protects against data corruption during programming by preventing any programming operations if V_{CC} drops below approximately 3.8V (V_{CC} Lockout trip level). This is accomplished by continually monitoring the CS (Chip Select) pin and, when active (high), preventing programming if the V_{CC} drops below the Lockout trip level. After any programming opcode is fully clocked in and the V_{PP} internal high voltage has been turned on, the lockout is disabled. The lockout is inactive if any opcode is entered **except** a programming opcode. **Disabled programming is indicated by no BUSY signal appearing at the output (the output remains tri-stated).** To restate, the V_{CC} Lockout feature is active from the time CS goes high up to the time that the V_{PP} internal high voltage is turned on. (The Low V_{CC} Lockout feature is not enabled for any non-programming opcodes.) **Once programming has begun, the programming cycle cannot be interrupted except by removal of V_{CC} , which could result in data corruption.**

Timing Diagrams for the NM93C86AU

Synchronous Data Timing



DS800021-3

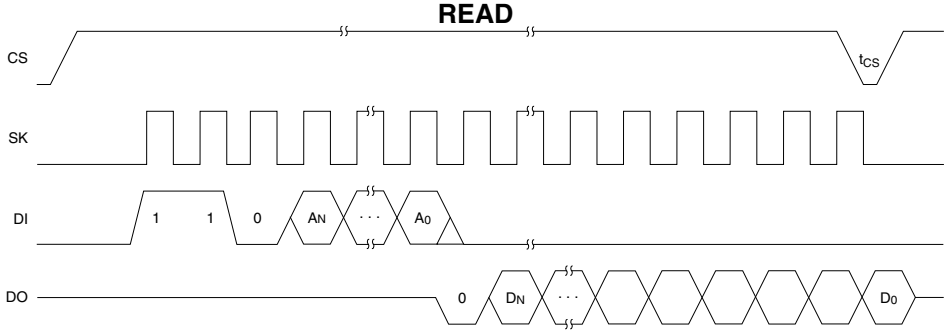
Timing Diagrams for the NM93C86AU (Continued)

Key for Timing Diagrams

Organization of Address and Data Fields for the NM93C86AU

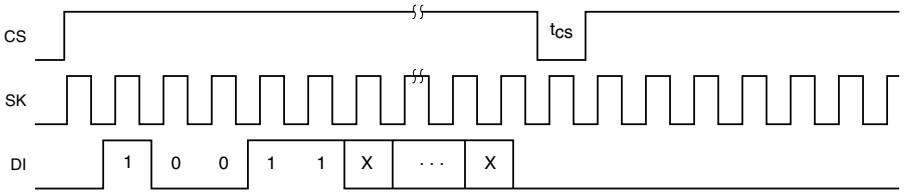
ORG	Organization	A_N	D_N
V_{CC} or NC	1024 x 16	A9	D15
V_{SS}	2048 x 8	A10	D7

READ



DS800021-4

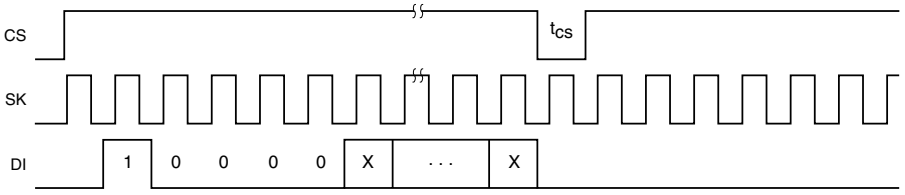
EWEN
DO = TRI-STATE



ORG = V_{CC}, 8 X's
ORG = V_{SS}, 9 X's

DS800021-5

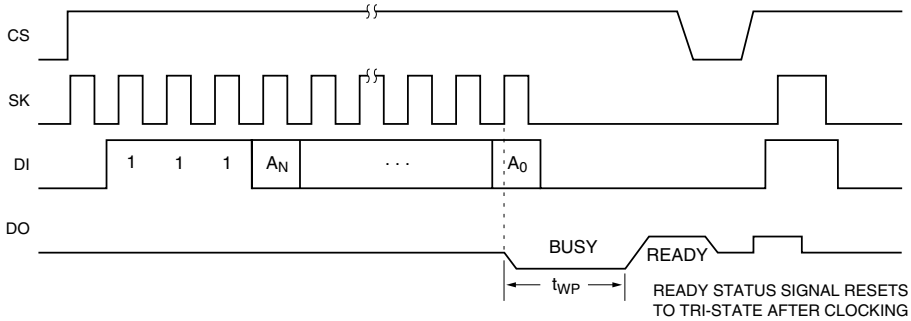
EWDS
DO = TRI-STATE



ORG = V_{CC}, 8 X's
ORG = V_{SS}, 9 X's

DS800021-6

ERASE

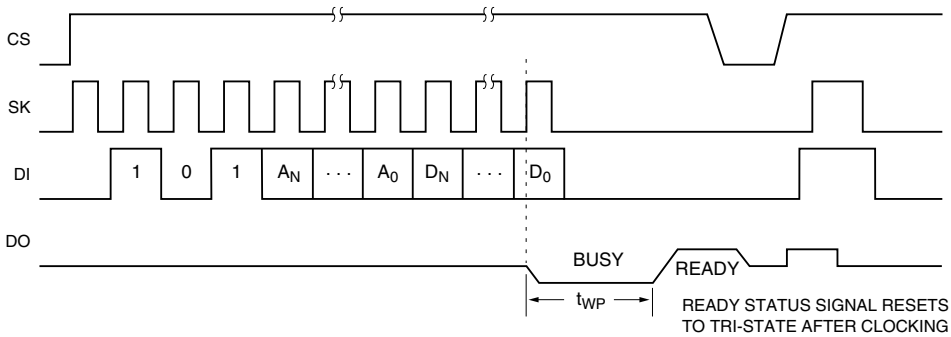


READY STATUS SIGNAL RESETS TO TRI-STATE AFTER CLOCKING IN ONE SK CYCLE WITH DI = 1

DS800021-7

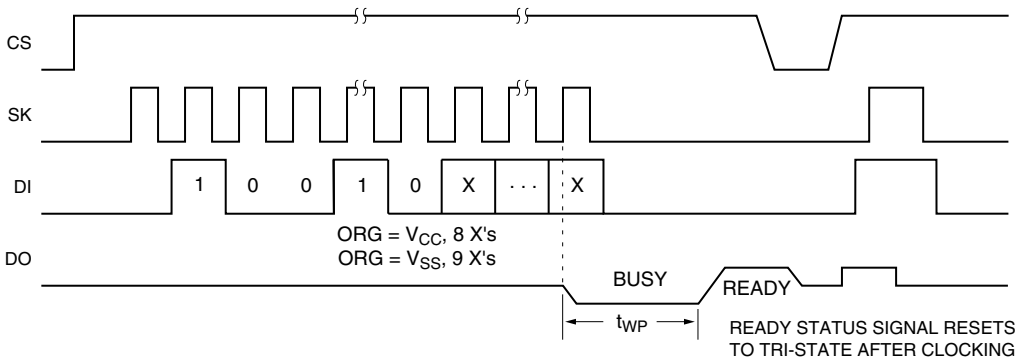
Timing Diagrams for the NM93C86AU (Continued)

WRITE



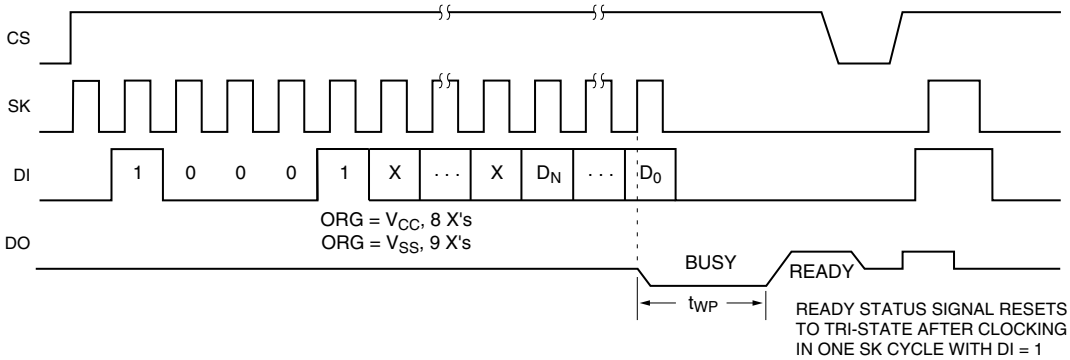
DS800021-8

ERAL



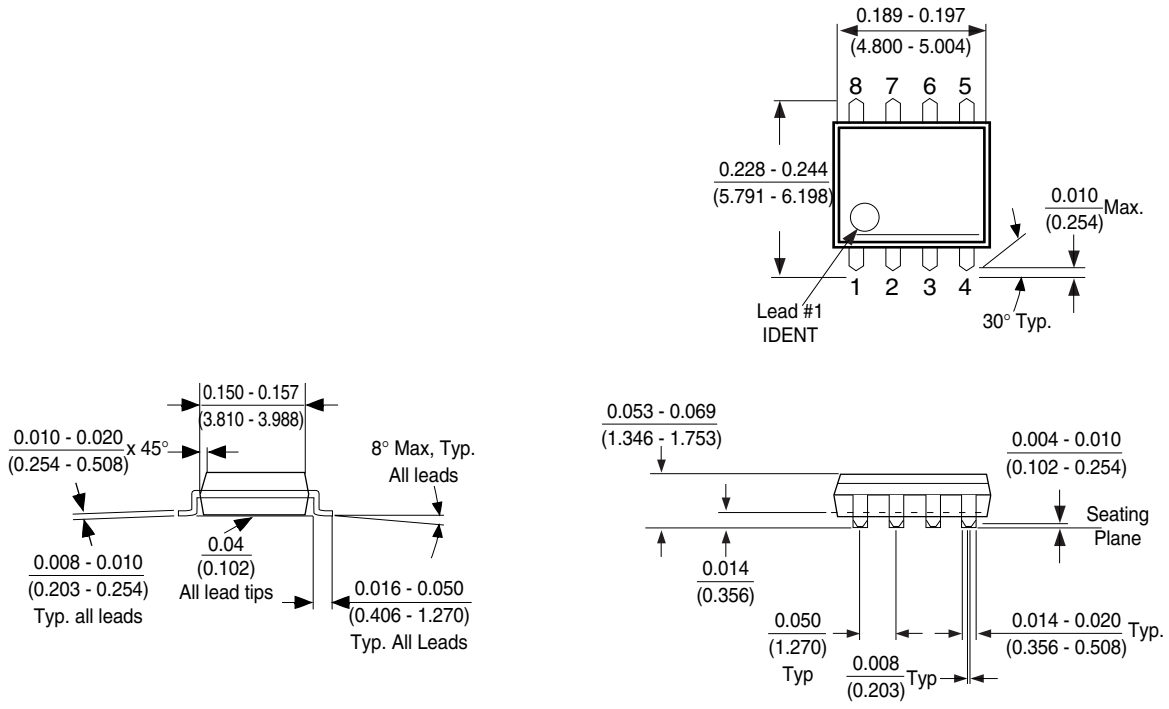
DS800021-9

WRAL



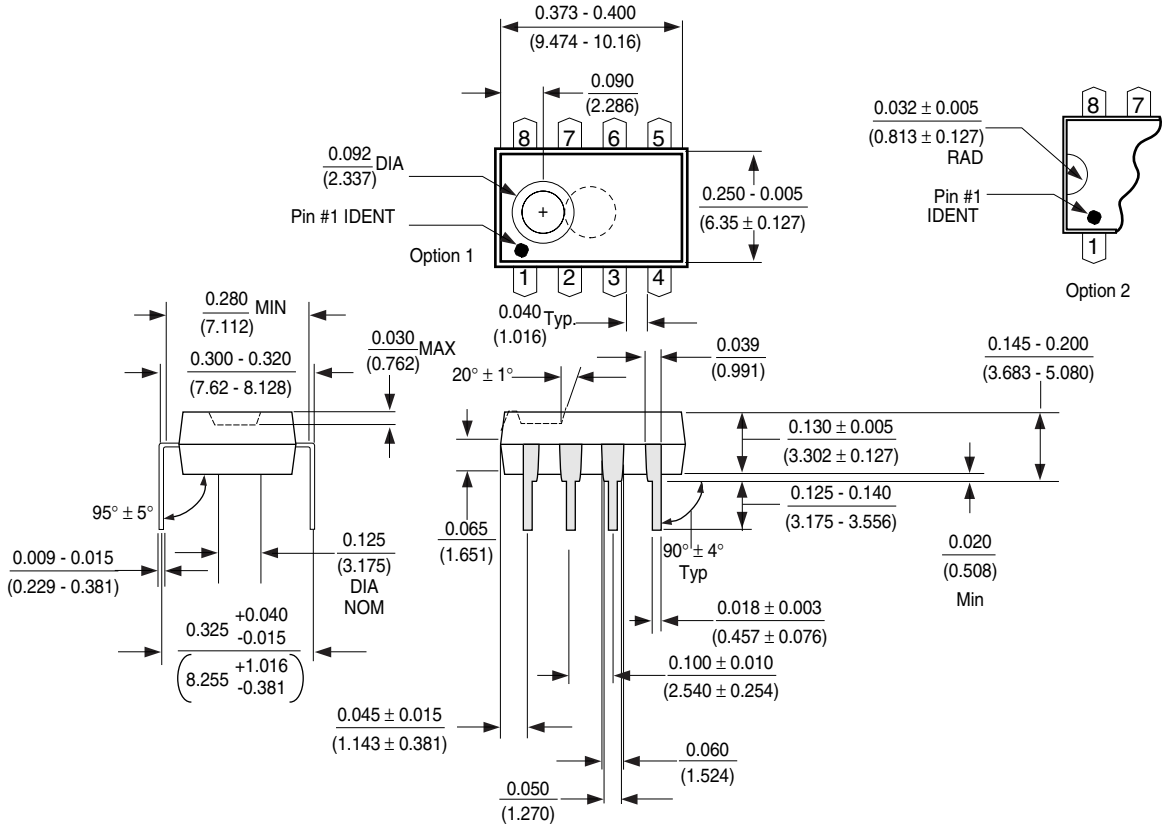
DS800021-10

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Small Outline Package (M8)
Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-in-Line Package (N)
Package Number N08E

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FAIRCHILD SEMICONDUCTOR™

February 2000

NM93CS06 (MICROWIRE™ Bus Interface) 256-Bit Serial EEPROM with Data Protect and Sequential Read

General Description

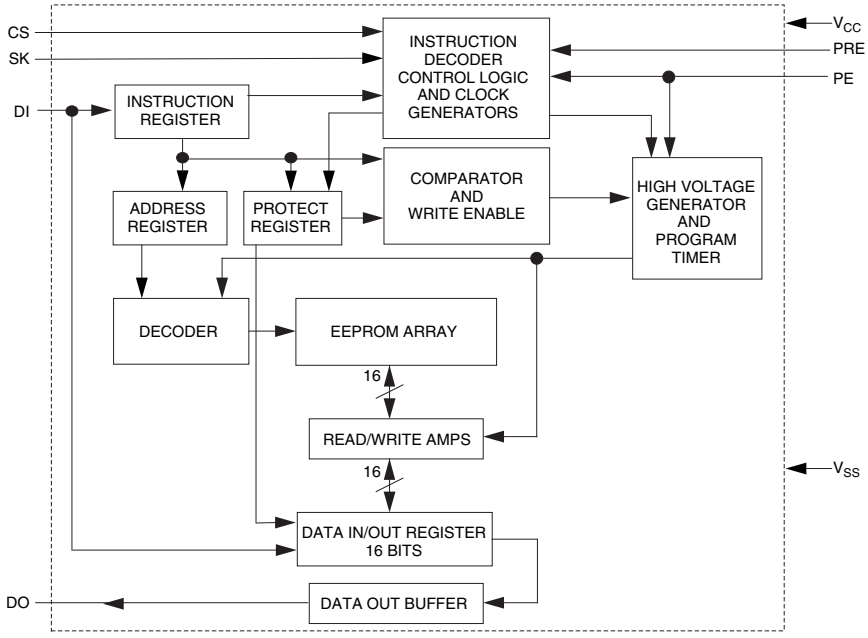
NM93CS06 is a 256-bit CMOS non-volatile EEPROM organized as 16 x 16-bit array. This device features MICROWIRE interface which is a 4-wire serial bus with chipselect (CS), clock (SK), data input (DI) and data output (DO) signals. This interface is compatible to many of standard Microcontrollers and Microprocessors. NM93CS06 offers programmable write protection to the memory array using a special register called Protect Register. Selected memory locations can be protected against write by programming this Protect Register with the address of the first memory location to be protected (all locations greater than or equal to this first address are then protected from further change). Additionally, this address can be "permanently locked" into the device, making all future attempts to change data impossible. In addition this device features "sequential read", by which, entire memory can be read in one cycle instead of multiple single byte read cycles. There are 10 instructions implemented on the NM93CS06, 5 of which are for memory operations and the remaining 5 are for Protect Register operations. This device is fabricated using Fairchild Semiconductor floating-gate CMOS process for high reliability, high endurance and low power consumption.

"LZ" and "L" versions of NM93CS06 offer very low standby current making them suitable for low power applications. This device is offered in both SO and TSSOP packages for small space considerations.

Features

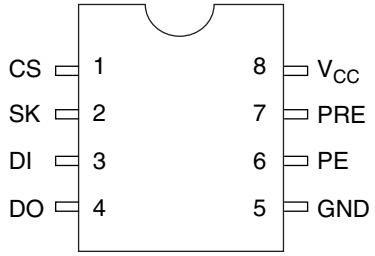
- Wide V_{CC} 2.7V - 5.5V
- Programmable write protection
- Sequential register read
- Typical active current of 200μA
  10μA standby current typical
  1μA standby current typical (L)
  0.1μA standby current typical (LZ)
- No Erase instruction required before Write instruction
- Self timed write cycle
- Device status during programming cycles
- 40 year data retention
- Endurance: 1,000,000 data changes
- Packages available: 8-pin SO, 8-pin DIP, 8-pin TSSOP

Functional Diagram



Connection Diagram

Dual-In-Line Package (N)
8–Pin SO (M8) and 8–Pin TSSOP (MT8)



Top View
Package Number
N08E, M08A and MTC08

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
V_{CC}	Power Supply

Ordering Information

NM 93 CS XX LZ E XXX

	Letter	Description
Package	N	8-pin DIP
	M8	8-pin SO
	MT8	8-pin TSSOP
Temp. Range	None	0 to 70°C
	V	-40 to +125°C
	E	-40 to +85°C
Voltage Operating Range	Blank	4.5V to 5.5V
	L	2.7V to 5.5V
	LZ	2.7V to 5.5V and <1µA Standby Current
Density	06	256 bits
	C	CMOS
	CS	Data protect and sequential read
Interface	93	MICROWIRE
Fairchild Memory Prefix		

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to -0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93CS06	0°C to +70°C
NM93CS06E	-40°C to +85°C
NM93CS06V	-40°C to +125°C
Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 4.5V to 5.5V unless otherwise specified

Symbol	Parameter	Conditions	Min	Max	Units
I_{CCA}	Operating Current	CS = V_{IH}, SK=1.0 MHz		1	mA
I_{CCS}	Standby Current	CS = V_{IL}		50	µA
I_{IL} I_{OL}	Input Leakage Output Leakage	V_{IN} = 0V to V_{CC} (Note 2)		±-1	µA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage		-0.1 2	0.8 V_{CC} +1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage	I_{OL} = 2.1 mA I_{OH} = -400 µA	 2.4	0.4	V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage	I_{OL} = 10 µA I_{OH} = -10 µA	 V_{CC} - 0.2	0.2	V
f_{SK}	SK Clock Frequency	(Note 3)		1	MHz
t_{SKH}	SK High Time	0°C to +70°C -40°C to +125°C	250 300		ns
t_{SKL}	SK Low Time		250		ns
t_{SKS}	SK Setup Time		50		ns
t_{CS}	Minimum CS Low Time	(Note 4)	250		ns
t_{CSS}	CS Setup Time		100		ns
t_{PRES}	PRE Setup Time		50		ns
t_{DH}	DO Hold Time		70		ns
t_{PES}	PE Setup Time		50		ns
t_{DIS}	DI Setup Time		100		ns
t_{CSH}	CS Hold Time		0		ns
t_{PEH}	PE Hold Time		250		ns
t_{PREH}	PRE Hold Time		50		ns
t_{DIH}	DI Hold Time		20		ns
t_{PD}	Output Delay			500	ns
t_{SV}	CS to Status Valid			500	ns
t_{DF}	CS to DO in Hi-Z	CS = V_{IL}		100	ns
t_{WP}	Write Cycle Time			10	ms

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to -0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93CS06L/LZ	0°C to +70°C
NM93CS06LE/LZE	-40°C to +85°C
NM93CS06LV/LZV	-40°C to +125°C
Power Supply (V_{CC})	2.7V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 2.7V to 5.5V unless otherwise specified

Symbol	Parameter	Conditions	Min	Max	Units
I_{CCA}	Operating Current	CS = V_{IH}, SK=1.0 MHz		1	mA
I_{CCS}	Standby Current L LZ (2.7V to 4.5V)	CS = V_{IL}		 10 1	 µA µA
I_{IL} I_{OL}	Input Leakage Output Leakage	V_{IN} = 0V to V_{CC} (Note 2)		±1	µA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage		-0.1 0.8V_{CC}	0.15V_{CC} V_{CC} +1	V
V_{OL} V_{OH}	Output Low Voltage Output High Voltage	I_{OL} = 10µA I_{OH} = -10µA	 0.9V_{CC}	0.1V_{CC}	V
f_{SK}	SK Clock Frequency	(Note 3)	0	250	KHz
t_{SKH}	SK High Time		1		µs
t_{SKL}	SK Low Time		1		µs
t_{SKS}	SK Setup Time		0.2		µs
t_{CS}	Minimum CS Low Time	(Note 4)	1		µs
t_{CSS}	CS Setup Time		0.2		µs
t_{PRES}	PRE Setup Time		50		ns
t_{DH}	DO Hold Time		70		ns
t_{PES}	PE Setup Time		50		ns
t_{DIS}	DI Setup Time		0.4		µs
t_{CSH}	CS Hold Time		0		ns
t_{PEH}	PE Hold Time		250		ns
t_{PREH}	PRE Hold Time		50		ns
t_{DIH}	DI Hold Time		0.4		µs
t_{PD}	Output Delay			2	µs
t_{SV}	CS to Status Valid			1	µs
t_{DF}	CS to DO in Hi-Z	CS = V_{IL}		0.4	µs
t_{WP}	Write Cycle Time			15	ms

Capacitance T_A = 25°C, f = 1 MHz (Note 5)

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical leakage values are in the 20nA range.

Note 3: The shortest allowable SK clock period = $1/f_{SK}$ (as shown under the f_{SK} parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both t_{SKH} and t_{SKL} limits must be observed. Therefore, it is not allowable to set $1/f_{SK} = t_{SKHminimum} + t_{SKLminimum}$ for shorter SK cycle time operation.

Note 4: CS (Chip Select) must be brought low (to V_{IL}) for an interval of t_{CS} in order to reset all internal device registers (device reset) prior to beginning another opcode cycle. (This is shown in the opcode diagram on the following page.)

Note 5: This parameter is periodically sampled and not 100% tested.

AC Test Conditions

V_{CC} Range	V_{IL}/V_{IH} Input Levels	V_{IL}/V_{IH} Timing Level	V_{OL}/V_{OH} Timing Level	I_{OL}/I_{OH}
2.7V ≤ V_{CC} ≤ 5.5V (Extended Voltage Levels)	0.3V/1.8V	1.0V	0.8V/1.5V	±10µA
4.5V ≤ V_{CC} ≤ 5.5V (TTL Levels)	0.4V/2.4V	1.0V/2.0V	0.4V/2.4V	2.1mA/-0.4mA
Output Load: 1 TTL Gate (C_L = 100 pF)				

Pin Description

Chip Select (CS)

This is an active high input pin to NM93CS06 EEPROM (the device) and is generated by a master that is controlling the device. A high level on this pin selects the device and a low level deselects the device. All serial communications with the device is enabled only when this pin is held high. However this pin cannot be permanently tied high, as a rising edge on this signal is required to reset the internal state-machine to accept a new cycle and a falling edge to initiate an internal programming after a write cycle. All activity on the SK, DI and DO pins are ignored while CS is held low.

Serial Clock (SK)

This is an input pin to the device and is generated by the master that is controlling the device. This is a clock signal that synchronizes the communication between a master and the device. All input information (DI) to the device is latched on the rising edge of this clock input, while output data (DO) from the device is driven from the rising edge of this clock input. This pin is gated by CS signal.

Serial Input (DI)

This is an input pin to the device and is generated by the master that is controlling the device. The master transfers Input information (Start bit, Opcode bits, Array addresses and Data) serially via this pin into the device. This Input information is latched on the rising edge of the SCK. This pin is gated by CS signal.

Serial Output (DO)

This is an output pin from the device and is used to transfer Output data via this pin to the controlling master. Output data is serially shifted out on this pin from the rising edge of the SCK. This pin is active only when the device is selected.

Protect Register Enable (PRE)

This is an active high input pin to the device and is used to distinguish operations to memory array and operations to Protect Register. When this pin is held low, operations to the memory array are enabled. When this pin is held high, operations to the Protect Register are enabled. This pin operates in conjunction with PE pin. Refer Table1 for functional matrix of this pin for various operations.

Program Enable (PE)

This is an active high input pin to the device and is used to enable operations, that are write in nature, to the memory array and to the Protect register. When this pin is held high, operations that are “write” in nature are enabled. When this pin is held low, operations that are “write” in nature are disabled. This pin operates in conjunction with PRE pin. Refer Table1 for functional matrix of this pin for various operations.

Microwire Interface

A typical communication on the Microwire bus is made through the CS, SK, DI and DO signals. To facilitate various operations on the Memory array and on the Protect Register, a set of 10 instructions are implemented on NM93CS06. The format of each instruction is listed in Table 1.

Instruction

Each of the above 10 instructions is explained under individual instruction descriptions.

Start Bit

This is a 1-bit field and is the first bit that is clocked into the device when a Microwire cycle starts. This bit has to be “1” for a valid cycle to begin. Any number of preceding “0” can be clocked into the device before clocking a “1”.

Opcode

This is a 2-bit field and should immediately follow the start bit. These two bits (along with PRE, PE signals and 2 MSB of address field) select a particular instruction to be executed.

Address Field

This is a 6-bit field and should immediately follow the Opcode bits. In NM93CS06, only the LSB 4 bits are used for address decoding during READ, WRITE and PRWRITE instructions. During these instructions (READ, WRITE and PRWRITE), the MSB 2 bits are "don't care" (can be 0 or 1). During all other instructions (with the exception of PRREAD), the MSB 2 bits are used to decode instruction (along with Opcode bits, PRE and PE signals).

Data Field

This is a 16-bit field and should immediately follow the Address bits. Only the WRITE and WRALL instructions require this field. D15 (MSB) is clocked first and D0 (LSB) is clocked last (both during writes as well as reads).

TABLE 1. Instruction set

Instruction	Start Bit	Opcode Field	Address Field						Data Field	PRE Pin	PE Pin
READ	1	10	X	X	A3	A2	A1	A0		0	X
WEN	1	00	1	1	X	X	X	X		0	1
WRITE	1	01	X	X	A3	A2	A1	A0	D15-D0	0	1
WRALL	1	00	0	1	X	X	X	X	D15-D0	0	1
WDS	1	00	0	0	X	X	X	X		0	X
PRREAD	1	10	X	X	X	X	X	X		1	X
PREN	1	00	1	1	X	X	X	X		1	1
PRCLEAR	1	11	1	1	1	1	1	1		1	1
PRWRITE	1	01	X	X	A3	A2	A1	A0		1	1
PRDS	1	00	0	0	0	0	0	0		1	1

Functional Description

A typical Microwire cycle starts by first selecting the device (bringing the CS signal high). Once the device is selected, a valid Start bit ("1") should be issued to properly recognize the cycle. Following this, the 2-bit opcode of appropriate instruction should be issued. After the opcode bits, the 6-bit address information should be issued. For certain instructions, some (or all) of these 6 bits are don't care values (can be "0" or "1"), but they should still be issued. Following the address information, depending on the instruction (WRITE and WRALL), 16-Bit data is issued. Otherwise, depending on the instruction (READ and PRREAD), the device starts to drive the output data on the DO line. Other instructions perform certain control functions and do not deal with data bits. The Microwire cycle ends when the CS signal is brought low. However during certain instructions, falling edge of the CS signal initiates an internal cycle (Programming), and the device remains busy till the completion of the internal cycle. Each of the 10 instructions is explained in detail in the following sections.

Memory Instructions

Following five instructions, READ, WEN, WRITE, WRALL and WDS are specific to operations intended for memory array. The PRE pin should be held low during these instructions.

1) Read and Sequential Read (READ)

READ instruction allows data to be read from a selected location in the memory array. Input information (Start bit, Opcode and Address) for this instruction should be issued as listed under Table1. Upon receiving a valid input information, decoding of the opcode and the address is made, followed by data transfer from the selected memory location into a 16-bit serial-out shift register. This 16-bit data is then shifted out on the DO pin. D15 bit (MSB) is shifted out first and D0 bit (LSB) is shifted out last. A dummy-bit (logical 0) precedes this 16-bit data output string. Output data changes are initiated on the rising edge of the SK clock. After reading the 16-bit data, the CS signal can be brought low to end the Read cycle. The PRE pin should be held low during this cycle. Refer *Read cycle diagram*.

This device also offers "sequential memory read" operation to allow reading of data from the additional memory locations instead of just one location. It is started in the same manner as normal read but the cycle is continued to read further data (instead of terminating after reading the first 16-bit data). After providing 16-bit data, the device automatically increments the address pointer to the next location and continues to provide the data from that location. Any number of locations can be read out in this manner, however, after reading out from the last location, the address pointer points back to the first location. If the cycle is continued further, data will be read from this first location onward. In this mode of read, the dummy-bit is present only when the very first data is read (like normal read cycle) and is not present on subsequent data reads. The PRE pin should be held low during this cycle. Refer *Sequential Read cycle diagram*.

2) Write Enable (WEN)

When V_{CC} is applied to the part, it "powers up" in the Write Disable (WDS) state. Therefore, all programming operations (for both memory array and Protect Register) must be preceded by a Write Enable (WEN) instruction. Once a Write Enable instruction is executed, programming remains enabled until a Write Disable (WDS) instruction is executed or V_{CC} is completely removed from the part. Input information (Start bit, Opcode and Address) for this WEN instruction should be issued as listed under Table1. The device becomes write-enabled at the end of this cycle when the CS signal is brought low. The PRE pin should be held low during this cycle. Execution of a READ instruction is independent of WEN instruction. Refer *Write Enable cycle diagram.*

3) Write (WRITE)

WRITE instruction allows write operation to a specified location in the memory with a specified data. This instruction is valid only when the following are true:

- Device is write-enabled (Refer WEN instruction)
- Address of the write location is not write-protected
- PE pin is held high during this cycle
- PRE pin should be held low during this cycle

Input information (Start bit, Opcode, Address and Data) for this WRITE instruction should be issued as listed under Table1. After inputting the last bit of data (D0 bit), CS signal must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. It takes t_{WP} time (Refer appropriate DC and AC Electrical Characteristics table) for the internal programming cycle to finish. During this time, the device remains busy and is not ready for another instruction.

The status of the internal programming cycle can be polled at any time by bringing the CS signal high again, after t_{CS} interval. When CS signal is high, the DO pin indicates the READY/BUSY status of the chip. DO = logical 0 indicates that the programming is still in progress. DO = logical 1 indicates that the programming is finished and the device is ready for another instruction. It is not required to provide the SK clock during this status polling. While the device is busy, it is recommended that no new instruction be issued. Refer *Write cycle diagram.*

It is also recommended to follow this instruction (after the device becomes READY) with a Write Disable (WDS) instruction to safeguard data against corruption due to spurious noise, inadvertent writes etc.

4) Write All (WRALL)

Write all (WRALL) instruction is similar to the Write instruction except that WRALL instruction will simultaneously program all memory locations with the data pattern specified in the instruction. This instruction is valid only when the following are true:

- Protect Register has been cleared (Refer PRCLEAR instruction)
- Device is write-enabled (Refer WEN instruction)
- PE pin is held high during this cycle
- PRE pin should be held low during this cycle

Input information (Start bit, Opcode, Address and Data) for this WRALL instruction should be issued as listed under Table1. After inputting the last bit of data (D0 bit), CS signal must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. It takes t_{WP} time (Refer appropriate DC and AC Electrical Characteristics table) for the internal programming cycle to finish. During this time, the device remains busy and is not ready for another instruction. Status of the internal programming can be polled as described under WRITE instruction description. While the device is busy, it is recommended that no new instruction be issued. Refer *Write All cycle diagram.*

5) Write Disable (WDS)

Write Disable (WDS) instruction disables all programming operations and is recommended to follow all programming operations. Executing this instruction after a valid write instruction would protect against accidental data disturb due to spurious noise, glitches, inadvertent writes etc. Input information (Start bit, Opcode and Address) for this WDS instruction should be issued as listed under Table1. The device becomes write-disabled at the end of this cycle when the CS signal is brought low. Execution of a READ instruction is independent of WDS instruction. Refer *Write Disable cycle diagram.*

Protect Register Instructions

Following five instructions, PRREAD, PREN, PRCLEAR, PRWRITE and PRDS are specific to operations intended for Protect Register. The PRE pin should be held high during these instructions.

1) Protect Register Read (PRREAD)

This instruction reads the content of the internal Protect Register. Content of this register is 6-bit wide and is the starting address of the "write-protected" section of the memory array. All memory locations greater than or equal to this address are write-protected. Input information (Start bit, Opcode and Address) for this PRREAD instruction should be issued as listed under Table1. Upon receiving a valid input information, decoding of the opcode and the address is made, followed by data transfer (address information) from the Protect Register. This 6-bit data is then shifted out on the DO pin with the MSB first and the LSB last. Like the READ instruction a dummy-bit (logical 0) precedes this 6-bit data output string. Output data changes are initiated on the rising edge of the SK clock. After reading the 6-bit data, the CS signal can be brought low to end the PRREAD cycle. The PRE pin should be held high during this cycle. Refer *Protect Register Read cycle diagram.*

Though the content of this register is 6-bit wide, only the last 4 bits (LSB) are valid for NM93CS06 device.

2) Protect Register Enable (PREN)

This instruction is required to enable PRCLEAR, PRWRITE and PRDS instructions and should be executed prior to executing PRCLEAR, PRWRITE and PRDS instructions. However, this PREN instruction is enabled (valid) only the following are true

- Device is write-enabled (Refer WEN instruction)
- PE pin is held high during this cycle
- PRE pin is held high during this cycle

Input information (Start bit, Opcode and Address) for this PREN instruction should be issued as listed under Table1. The Protect Register becomes enabled for PRCLEAR, PRWRITE and PRDS instructions at the end of this cycle when the CS signal is brought low. Note that this PREN instruction **must immediately precede** a PRCLEAR, PRWRITE or PRDS instruction. In other words, no other instruction should be executed between a PREN instruction and a PRCLEAR, PRWRITE or PRDS instruction. Refer *Protect Register Enable cycle diagram.*

3) Protect Register Clear (PRCLEAR)

This instruction clears the content of the Protect register and therefore enables write operations (WRITE or WRALL) to all memory locations. Executing this instruction will program the content of the Protect Register with a pattern of all 1s. However, in this case, WRITE operation to the last memory address (0x001111) is still enabled. PRCLEAR instruction is enabled (valid) only when the following are true:

- PREN instruction was executed **immediately prior** to PRCLEAR instruction
- PE pin is held high during this cycle
- PRE pin is held high during this cycle

Input information (Start bit, Opcode and Address) for this PRCLEAR instruction should be issued as listed under Table1. After inputting the last bit of address (A0 bit), CS signal must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed clear cycle. It takes t_{WP} time (Refer appropriate DC and AC Electrical Characteristics table) for the internal clear cycle to finish. During this time, the device remains busy and is not ready for another instruction. Status of the internal programming can be polled as described under WRITE instruction description. While the device is busy, it is recommended that no new instruction be issued. Refer *Protect Register Clear cycle diagram.*

4) Protect Register Write (PRWRITE)

This instruction is used to write the starting address of the memory section to be write-protected into the Protect register. After the execution of PRWRITE instruction, all memory locations greater than or equal to this address are write-protected. PRWRITE instruction is enabled (valid) only the following are true:

- PRCLEAR instruction was executed first (to clear the Protect Register)
- PREN instruction was executed **immediately prior** to PRWRITE instruction
- PE pin is held high during this cycle
- PRE pin is held high during this cycle

Input information (Start bit, Opcode and Address) for this PRWRITE instruction should be issued as listed under Table1. After inputting the last bit of address (A0 bit), CS signal must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. It takes t_{WP} time (Refer appropriate DC and AC Electrical Characteristics table) for the internal programming cycle to finish. During this time, the device remains busy and is not ready for another instruction. Status of the internal programming can be polled as described under WRITE instruction description. While the device is busy, it is recommended that no new instruction be issued. Refer *Protect Register Write cycle diagram.*

5) Protect Register Disable (PRDS)

Unlike all other instructions, this instruction is a **one-time-only** instruction which when executed **permanently write-protects the Protect Register** and renders it unalterable in the future. This instruction is useful to safeguard vital data (typically read only data) in the memory against any possible corruption. PRDS instruction is enabled (valid) only the following are true:

- PREN instruction was executed **immediately prior** to PRDS instruction
- PE pin is held high during this cycle
- PRE pin is held high during this cycle

Input information (Start bit, Opcode and Address) for this PRDS instruction should be issued as listed under Table1. After inputting the last bit of address (A0 bit), CS signal must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. It takes t_{WP} time (Refer appropriate DC and AC Electrical Characteristics table) for the internal programming cycle to finish. During this time, the device remains busy and is not ready for another instruction. Status of the internal programming can be polled as described under WRITE instruction description. While the device is busy, it is recommended that no new instruction be issued. The Protect Register is permanently write-protected at the end of this cycle. Refer *Protect Register Disable cycle diagram.*

Clearing of Ready/Busy status

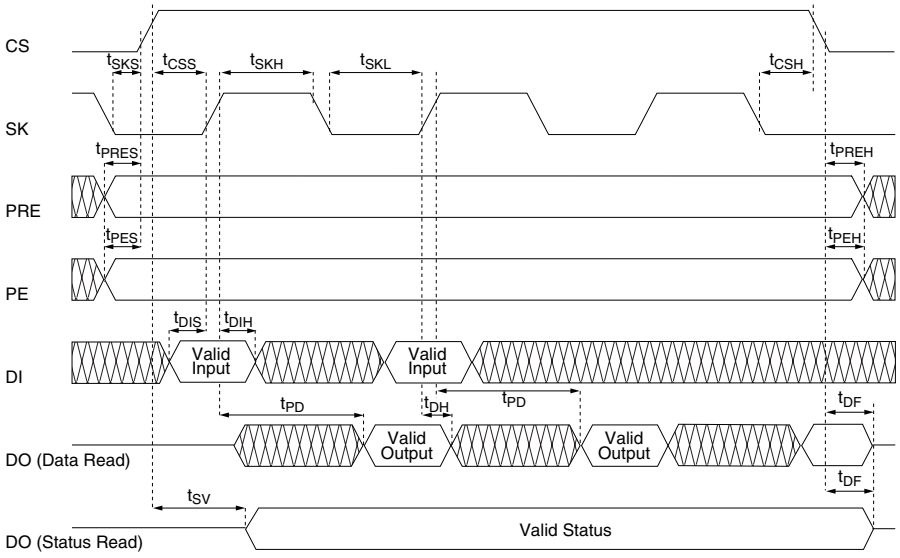
When programming is in progress, the Data-Out pin will display the programming status as either BUSY (low) or READY (high) when CS is brought high (DO output will be tri-stated when CS is low). To restate, during programming, the CS pin may be brought high and low any number of times to view the programming status without affecting the programming operation. Once programming is completed (Output in READY state), the output is 'cleared' (returned to normal tri-state condition) by clocking in a Start Bit. After the Start Bit is clocked in, the output will return to a tri-stated condition. When clocked in, this Start Bit can be the first bit in a command string, or CS can be brought low again to reset all internal circuits. Refer *Clearing Ready Status* diagram.

Related Document

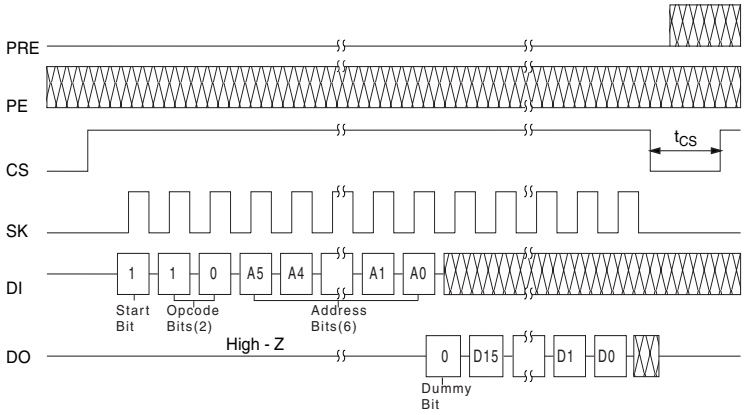
Application Note: AN758 - Using Fairchild's MICROWIRE™ EEPROM.

Timing Diagrams

SYNCHRONOUS DATA TIMING

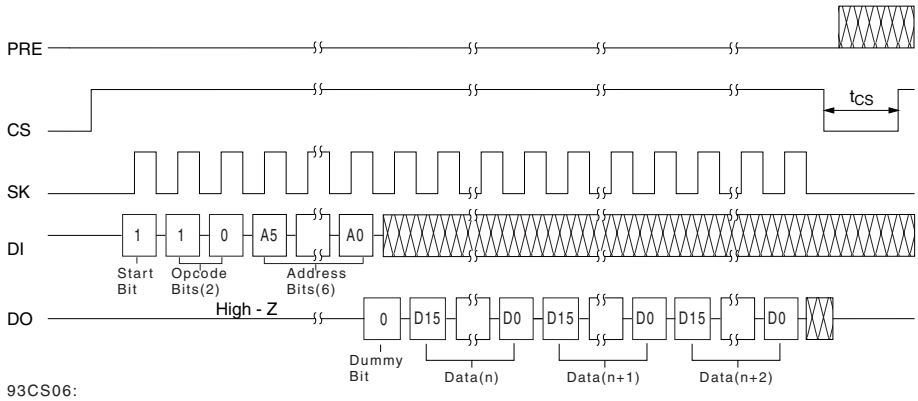


NORMAL READ CYCLE (READ)



93CS06:
Address bits pattern -> x-x-A3-A2-A1-A0; (x -> Don't Care, can be 0 or 1); (A3-A0 -> User defined)

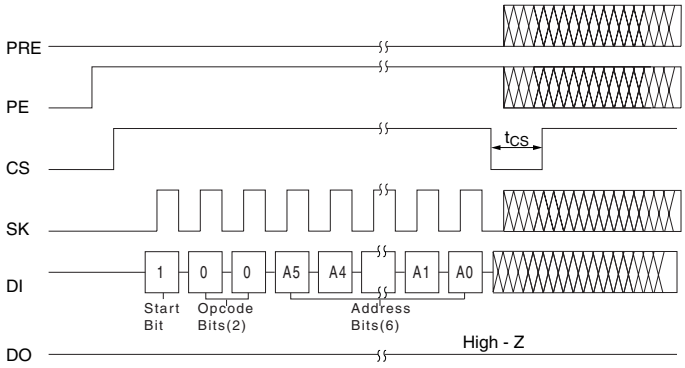
SEQUENTIAL READ CYCLE (PRE = 0; PE = X)



93CS06:
Address bits pattern -> x-x-A3-A2-A1-A0; (x -> Don't Care, can be 0 or 1); (A3-A0 -> User defined)

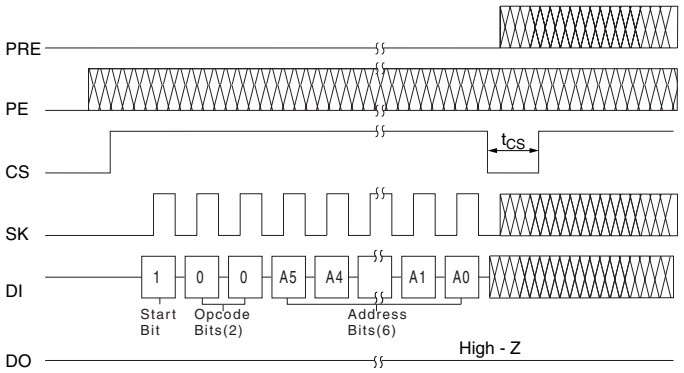
Timing Diagrams (Continued)

WRITE ENABLE CYCLE (WEN)



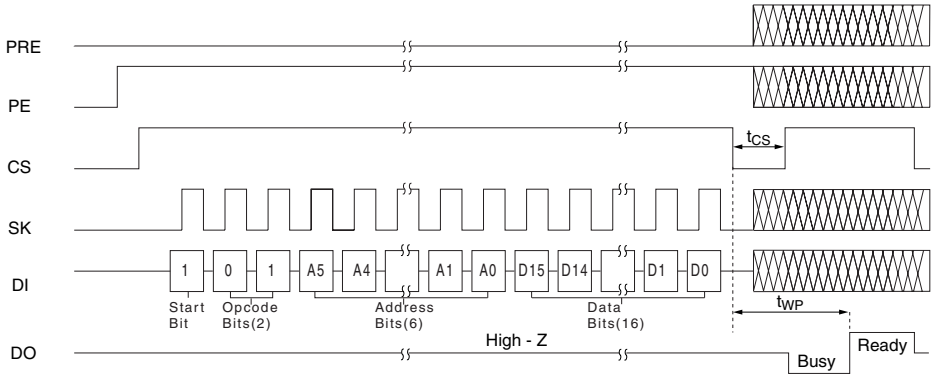
93CS06:
Address bits pattern -> 1-1-x-x-x-x; (x -> Don't Care, can be 0 or 1)

WRITE DISABLE CYCLE (WDS)



93CS06:
Address bits pattern -> 0-0-x-x-x-x; (x -> Don't Care, can be 0 or 1)

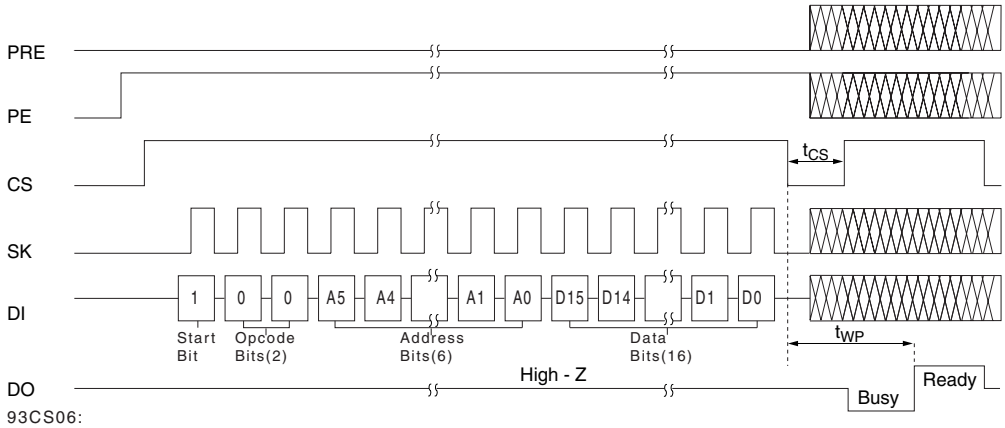
WRITE CYCLE (WRITE)



93CS06:
Address bits pattern -> x-x-A3-A2-A1-A0; (x -> Don't Care, can be 0 or 1); (A3-A0 -> User defined)
Data bits pattern -> User defined

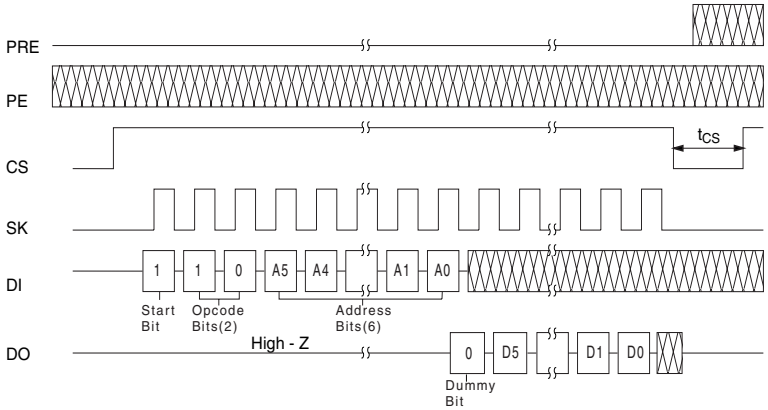
Timing Diagrams (Continued)

WRITE ALL CYCLE (WRALL)



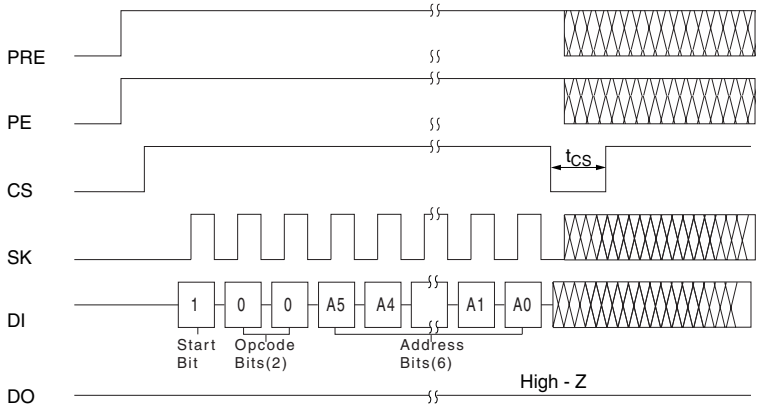
93CS06:
Address bits pattern -> 0-1-x-x-x-x; (x -> Don't Care, can be 0 or 1)
Data bits pattern -> User defined

PROTECT REGISTER READ CYCLE (PRREAD)



93CS06:
Address bits pattern -> x-x-x-x-x-x; (x -> Don't Care, can be 0 or 1)
Of the 6-bit output data(D5-D0), only D3 to D0 are valid and they correspond to A3 to A0 respectively.

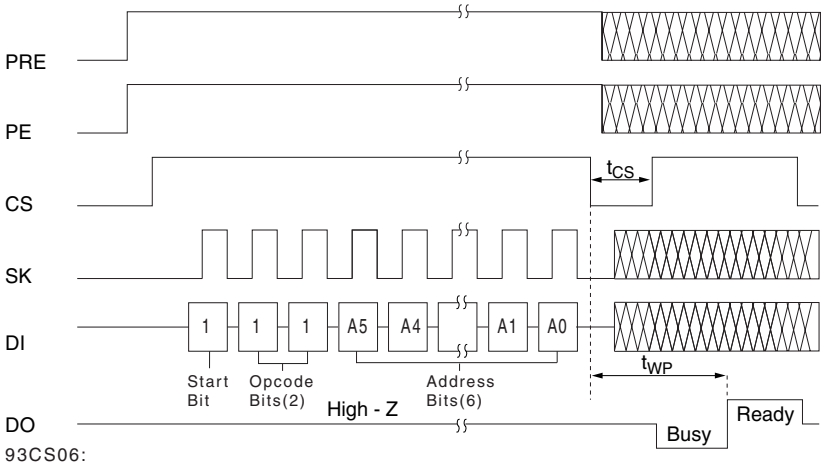
PROTECT REGISTER ENABLE CYCLE (PREN)



93CS06:
Address bits pattern -> 1-1-x-x-x-x; (x -> Don't Care, can be 0 or 1)

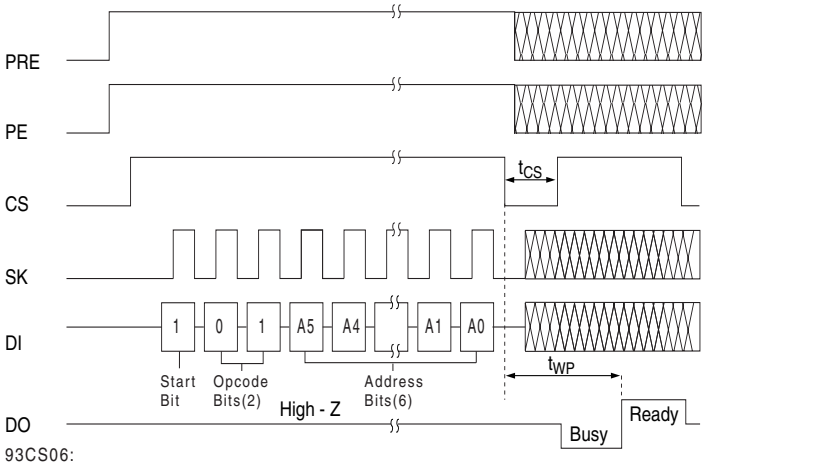
Timing Diagrams (Continued)

PROTECT REGISTER CLEAR CYCLE (PRCLEAR)



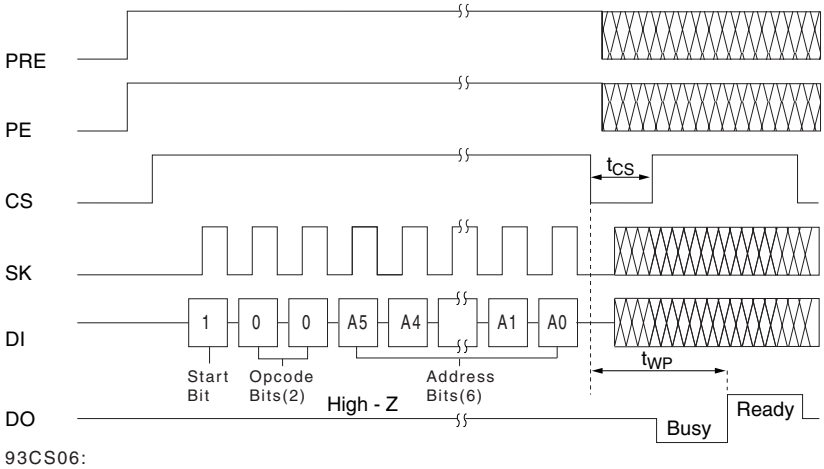
93CS06:
Address bits pattern -> 1-1-1-1-1-1

PROTECT REGISTER WRITE CYCLE (PRWRITE)



93CS06:
Address bits pattern -> x-x-A3-A2-A1-A0; (x -> Don't Care, can be 0 or 1); (A3-A0 -> User defined)

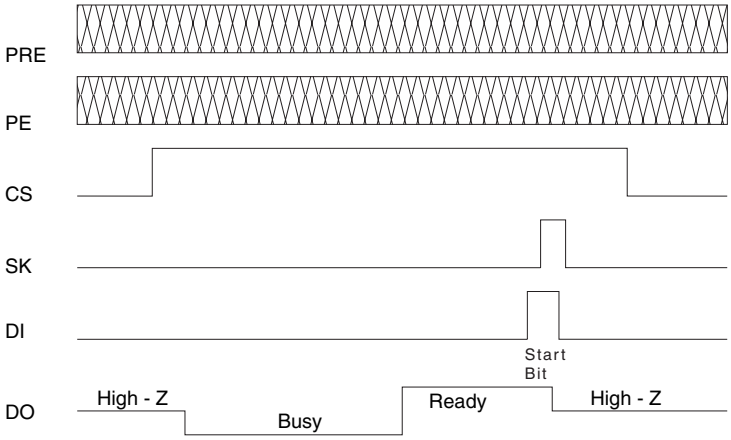
PROTECT REGISTER DISABLE CYCLE (PRDS)



93CS06:
Address bits pattern -> 0-0-0-0-0-0

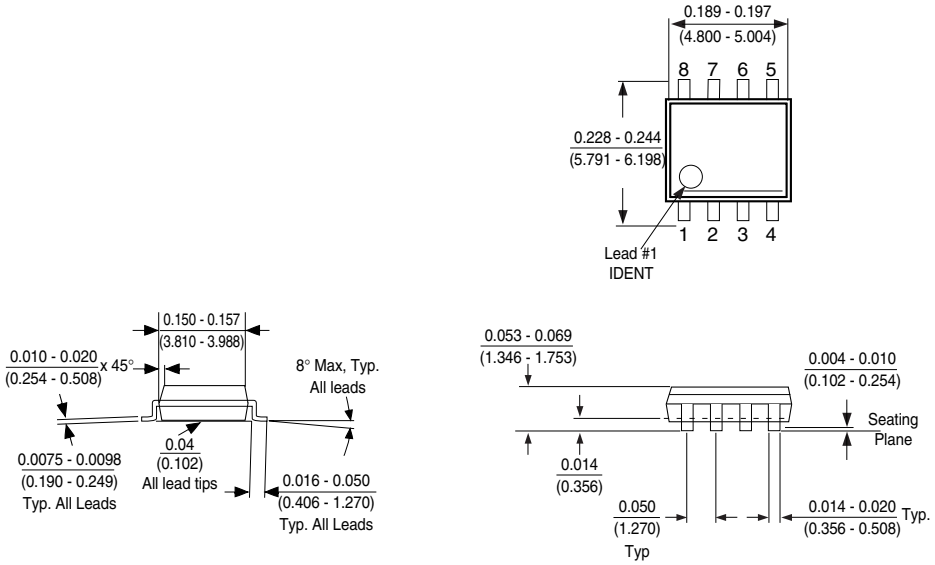
Timing Diagrams (Continued)

CLEARING READY STATUS



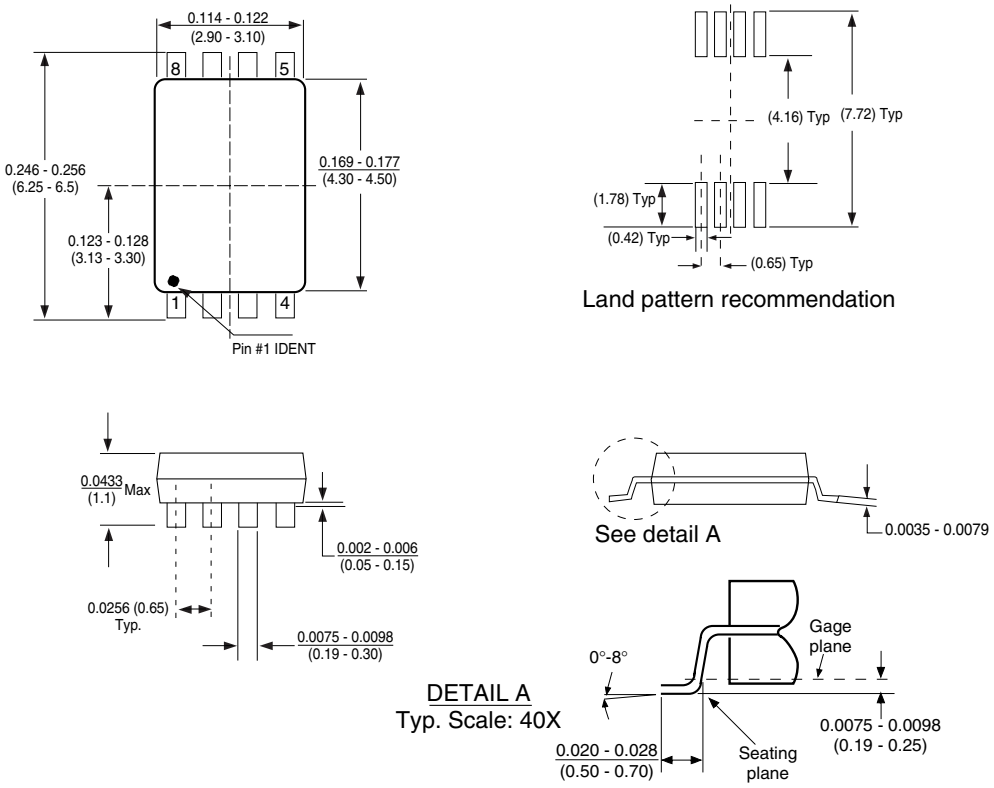
Note: This Start bit can also be part of a next instruction. Hence the cycle can be continued(instead of getting terminated, as shown) as if a new instruction is being issued.

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Package, Small Outline, 0.15 Wide, 8-Lead (M8)
Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted

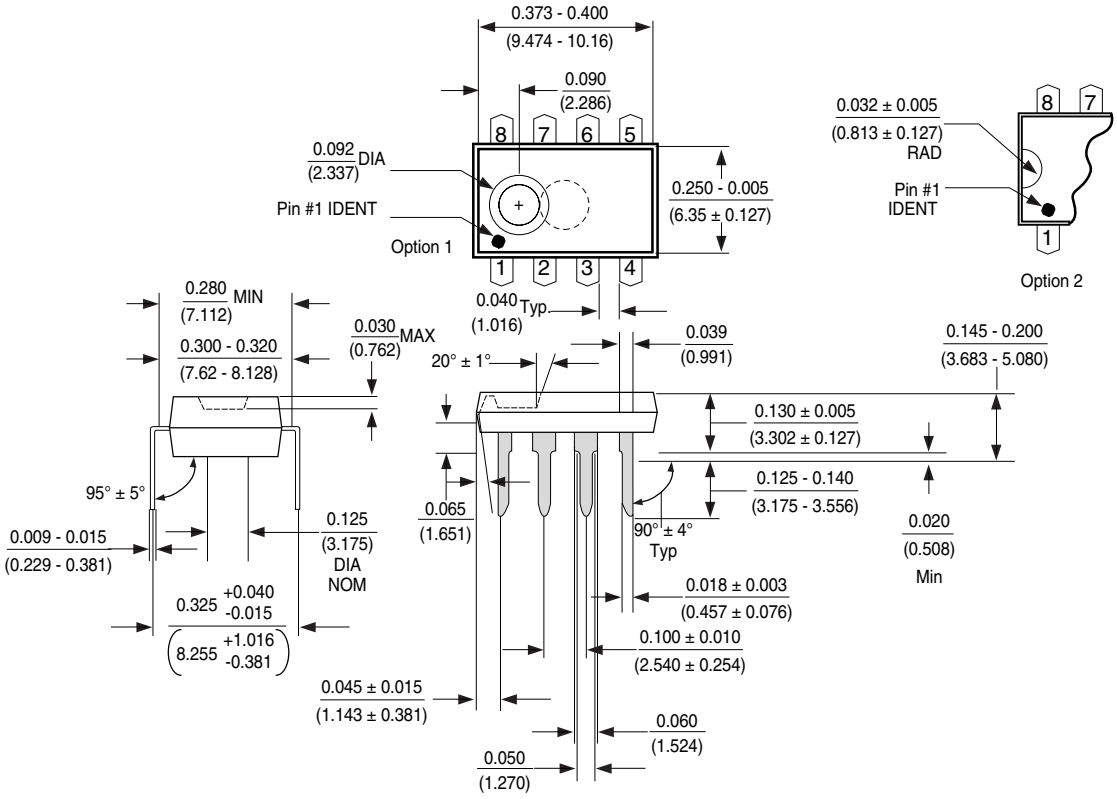


Notes: Unless otherwise specified

1. Reference JEDEC registration MO153. Variation AA. Dated 7/93

8-Pin Molded TSSOP, JEDEC (MT8)
Package Number MTC08

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Package Number N08E

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

February 2000

NM93CS46 (MICROWIRE™ Bus Interface) 1024-Bit Serial EEPROM with Data Protect and Sequential Read

General Description

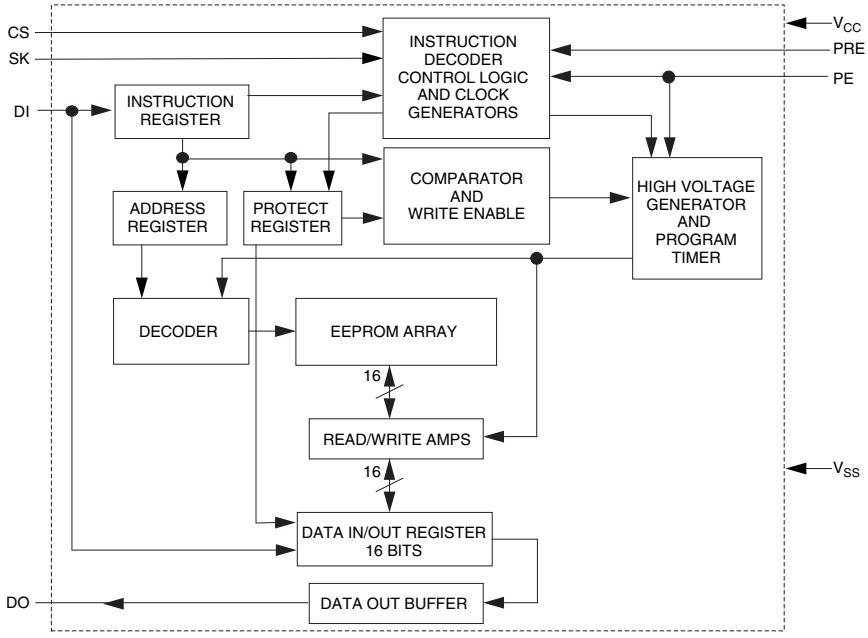
NM93CS46 is a 1024-bit CMOS non-volatile EEPROM organized as 64 x 16-bit array. This device features MICROWIRE interface which is a 4-wire serial bus with chipselect (CS), clock (SK), data input (DI) and data output (DO) signals. This interface is compatible to many of standard Microcontrollers and Microprocessors. NM93CS46 offers programmable write protection to the memory array using a special register called Protect Register. Selected memory locations can be protected against write by programming this Protect Register with the address of the first memory location to be protected (all locations greater than or equal to this first address are then protected from further change). Additionally, this address can be "permanently locked" into the device, making all future attempts to change data impossible. In addition this device features "sequential read", by which, entire memory can be read in one cycle instead of multiple single byte read cycles. There are 10 instructions implemented on the NM93CS46, 5 of which are for memory operations and the remaining 5 are for Protect Register operations. This device is fabricated using Fairchild Semiconductor floating-gate CMOS process for high reliability, high endurance and low power consumption.

"LZ" and "L" versions of NM93CS46 offer very low standby current making them suitable for low power applications. This device is offered in both SO and TSSOP packages for small space considerations.

Features

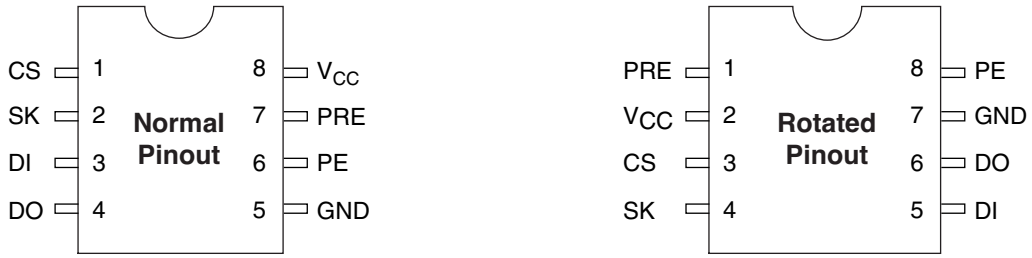
- Wide V_{CC} 2.7V - 5.5V
- Programmable write protection
- Sequential register read
- Typical active current of 200μA
  10μA standby current typical
  1μA standby current typical (L)
  0.1μA standby current typical (LZ)
- No Erase instruction required before Write instruction
- Self timed write cycle
- Device status during programming cycles
- 40 year data retention
- Endurance: 1,000,000 data changes
- Packages available: 8-pin SO, 8-pin DIP, 8-pin TSSOP

Functional Diagram



Connection Diagram

Dual-In-Line Package (N)
8–Pin SO (M8) and 8–Pin TSSOP (MT8)



Top View
Package Number
N08E, M08A and MTC08

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
V_{CC}	Power Supply

Ordering Information

		Letter	Description
NM	**Fairchild Memory Prefix**		
93	**Interface**	93	MICROWIRE
CS		C	CMOS
		CS	Data protect and sequential read
XX	**Density**	46	1024 bits
T		Blank	Normal Pin Out
		T	Rotated Pin Out
LZ	**Voltage Operating Range**	Blank	4.5V to 5.5V
		L	2.7V to 5.5V
		LZ	2.7V to 5.5V and <1µA Standby Current
E	**Temp. Range**	None	0 to 70°C
		V	-40 to +125°C
		E	-40 to +85°C
XXX	**Package**	N	8-pin DIP
		M8	8-pin SO
		MT8	8-pin TSSOP

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to -0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93CS46	0°C to +70°C
NM93CS46E	-40°C to +85°C
NM93CS46V	-40°C to +125°C
Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 4.5V to 5.5V unless otherwise specified

Symbol	Parameter	Conditions	Min	Max	Units
I_{CCA}	Operating Current	CS = V_{IH}, SK=1.0 MHz		1	mA
I_{CCS}	Standby Current	CS = V_{IL}		50	µA
I_{IL} I_{OL}	Input Leakage Output Leakage	V_{IN} = 0V to V_{CC} (Note 2)		±-1	µA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage		-0.1 2	0.8 V_{CC} +1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage	I_{OL} = 2.1 mA I_{OH} = -400 µA	 2.4	0.4	V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage	I_{OL} = 10 µA I_{OH} = -10 µA	 V_{CC} - 0.2	0.2	V
f_{SK}	SK Clock Frequency	(Note 3)		1	MHz
t_{SKH}	SK High Time	0°C to +70°C -40°C to +125°C	250 300		ns
t_{SKL}	SK Low Time		250		ns
t_{SKS}	SK Setup Time		50		ns
t_{CS}	Minimum CS Low Time	(Note 4)	250		ns
t_{CSS}	CS Setup Time		100		ns
t_{PRES}	PRE Setup Time		50		ns
t_{DH}	DO Hold Time		70		ns
t_{PES}	PE Setup Time		50		ns
t_{DIS}	DI Setup Time		100		ns
t_{CSH}	CS Hold Time		0		ns
t_{PEH}	PE Hold Time		250		ns
t_{PREH}	PRE Hold Time		50		ns
t_{DIH}	DI Hold Time		20		ns
t_{PD}	Output Delay			500	ns
t_{SV}	CS to Status Valid			500	ns
t_{DF}	CS to DO in Hi-Z	CS = V_{IL}		100	ns
t_{WP}	Write Cycle Time			10	ms

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to -0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93CS46L/LZ	0°C to +70°C
NM93CS46LE/LZE	-40°C to +85°C
NM93CS46LV/LZV	-40°C to +125°C
Power Supply (V_{CC})	2.7V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 2.7V to 5.5V unless otherwise specified

Symbol	Parameter	Conditions	Min	Max	Units
I_{CCA}	Operating Current	CS = V_{IH}, SK=1.0 MHz		1	mA
I_{CCS}	Standby Current L LZ (2.7V to 4.5V)	CS = V_{IL}		 10 1	 µA µA
I_{IL} I_{OL}	Input Leakage Output Leakage	V_{IN} = 0V to V_{CC} (Note 2)		±1	µA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage		-0.1 0.8V_{CC}	0.15V_{CC} V_{CC} +1	V
V_{OL} V_{OH}	Output Low Voltage Output High Voltage	I_{OL} = 10µA I_{OH} = -10µA	 0.9V_{CC}	0.1V_{CC}	V
f_{SK}	SK Clock Frequency	(Note 3)	0	250	KHz
t_{SKH}	SK High Time		1		µs
t_{SKL}	SK Low Time		1		µs
t_{SKS}	SK Setup Time		0.2		µs
t_{CS}	Minimum CS Low Time	(Note 4)	1		µs
t_{CSS}	CS Setup Time		0.2		µs
t_{PRES}	PRE Setup Time		50		ns
t_{DH}	DO Hold Time		70		ns
t_{PES}	PE Setup Time		50		ns
t_{DIS}	DI Setup Time		0.4		µs
t_{CSH}	CS Hold Time		0		ns
t_{PEH}	PE Hold Time		250		ns
t_{PREH}	PRE Hold Time		50		ns
t_{DIH}	DI Hold Time		0.4		µs
t_{PD}	Output Delay			2	µs
t_{SV}	CS to Status Valid			1	µs
t_{DF}	CS to DO in Hi-Z	CS = V_{IL}		0.4	µs
t_{WP}	Write Cycle Time			15	ms

Capacitance T_A = 25°C, f = 1 MHz (Note 5)

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical leakage values are in the 20nA range.

Note 3: The shortest allowable SK clock period = $1/f_{SK}$ (as shown under the f_{SK} parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both t_{SKH} and t_{SKL} limits must be observed. Therefore, it is not allowable to set $1/f_{SK} = t_{SKHminimum} + t_{SKLminimum}$ for shorter SK cycle time operation.

Note 4: CS (Chip Select) must be brought low (to V_{IL}) for an interval of t_{CS} in order to reset all internal device registers (device reset) prior to beginning another opcode cycle. (This is shown in the opcode diagram on the following page.)

Note 5: This parameter is periodically sampled and not 100% tested.

AC Test Conditions

V_{CC} Range	V_{IL}/V_{IH} Input Levels	V_{IL}/V_{IH} Timing Level	V_{OL}/V_{OH} Timing Level	I_{OL}/I_{OH}
2.7V ≤ V_{CC} ≤ 5.5V (Extended Voltage Levels)	0.3V/1.8V	1.0V	0.8V/1.5V	±10µA
4.5V ≤ V_{CC} ≤ 5.5V (TTL Levels)	0.4V/2.4V	1.0V/2.0V	0.4V/2.4V	2.1mA/-0.4mA
Output Load: 1 TTL Gate (C_L = 100 pF)				

Pin Description

Chip Select (CS)

This is an active high input pin to NM93CS46 EEPROM (the device) and is generated by a master that is controlling the device. A high level on this pin selects the device and a low level deselects the device. All serial communications with the device is enabled only when this pin is held high. However this pin cannot be permanently tied high, as a rising edge on this signal is required to reset the internal state-machine to accept a new cycle and a falling edge to initiate an internal programming after a write cycle. All activity on the SK, DI and DO pins are ignored while CS is held low.

Serial Clock (SK)

This is an input pin to the device and is generated by the master that is controlling the device. This is a clock signal that synchronizes the communication between a master and the device. All input information (DI) to the device is latched on the rising edge of this clock input, while output data (DO) from the device is driven from the rising edge of this clock input. This pin is gated by CS signal.

Serial Input (DI)

This is an input pin to the device and is generated by the master that is controlling the device. The master transfers Input information (Start bit, Opcode bits, Array addresses and Data) serially via this pin into the device. This Input information is latched on the rising edge of the SCK. This pin is gated by CS signal.

Serial Output (DO)

This is an output pin from the device and is used to transfer Output data via this pin to the controlling master. Output data is serially shifted out on this pin from the rising edge of the SCK. This pin is active only when the device is selected.

Protect Register Enable (PRE)

This is an active high input pin to the device and is used to distinguish operations to memory array and operations to Protect Register. When this pin is held low, operations to the memory array are enabled. When this pin is held high, operations to the Protect Register are enabled. This pin operates in conjunction with PE pin. Refer Table1 for functional matrix of this pin for various operations.

Program Enable (PE)

This is an active high input pin to the device and is used to enable operations, that are write in nature, to the memory array and to the Protect register. When this pin is held high, operations that are "write" in nature are enabled. When this pin is held low, operations that are "write" in nature are disabled. This pin operates in conjunction with PRE pin. Refer Table1 for functional matrix of this pin for various operations.

Microwire Interface

A typical communication on the Microwire bus is made through the CS, SK, DI and DO signals. To facilitate various operations on the Memory array and on the Protect Register, a set of 10 instructions are implemented on NM93CS46. The format of each instruction is listed in Table 1.

Instruction

Each of the above 10 instructions is explained under individual instruction descriptions.

Start Bit

This is a 1-bit field and is the first bit that is clocked into the device when a Microwire cycle starts. This bit has to be "1" for a valid cycle to begin. Any number of preceding "0" can be clocked into the device before clocking a "1".

Opcode

This is a 2-bit field and should immediately follow the start bit. These two bits (along with PRE, PE signals and 2 MSB of address field) select a particular instruction to be executed.

Address Field

This is a 6-bit field and should immediately follow the Opcode bits. In NM93CS46, all 6 bits are used for address decoding during READ, WRITE and PRWRITE instructions. During all other instructions (with the exception of PRREAD), the MSB 2 bits are used to decode instruction (along with Opcode bits, PRE and PE signals).

Data Field

This is a 16-bit field and should immediately follow the Address bits. Only the WRITE and WRALL instructions require this field. D15 (MSB) is clocked first and D0 (LSB) is clocked last (both during writes as well as reads).

TABLE 1. Instruction set

Instruction	Start Bit	Opcode Field	Address Field						Data Field	PRE Pin	PE Pin
READ	1	10	A5	A4	A3	A2	A1	A0		0	X
WEN	1	00	1	1	X	X	X	X		0	1
WRITE	1	01	A5	A4	A3	A2	A1	A0	D15-D0	0	1
WRALL	1	00	0	1	X	X	X	X	D15-D0	0	1
WDS	1	00	0	0	X	X	X	X		0	X
PRREAD	1	10	X	X	X	X	X	X		1	X
PREN	1	00	1	1	X	X	X	X		1	1
PRCLEAR	1	11	1	1	1	1	1	1		1	1
PRWRITE	1	01	A5	A4	A3	A2	A1	A0		1	1
PRDS	1	00	0	0	0	0	0	0		1	1

Functional Description

A typical Microwire cycle starts by first selecting the device (bringing the CS signal high). Once the device is selected, a valid Start bit ("1") should be issued to properly recognize the cycle. Following this, the 2-bit opcode of appropriate instruction should be issued. After the opcode bits, the 6-bit address information should be issued. For certain instructions, some (or all) of these 6 bits are don't care values (can be "0" or "1"), but they should still be issued. Following the address information, depending on the instruction (WRITE and WRALL), 16-Bit data is issued. Otherwise, depending on the instruction (READ and PRREAD), the device starts to drive the output data on the DO line. Other instructions perform certain control functions and do not deal with data bits. The Microwire cycle ends when the CS signal is brought low. However during certain instructions, falling edge of the CS signal initiates an internal cycle (Programming), and the device remains busy till the completion of the internal cycle. Each of the 10 instructions is explained in detail in the following sections.

Memory Instructions

Following five instructions, READ, WEN, WRITE, WRALL and WDS are specific to operations intended for memory array. The PRE pin should be held low during these instructions.

1) Read and Sequential Read (READ)

READ instruction allows data to be read from a selected location in the memory array. Input information (Start bit, Opcode and Address) for this instruction should be issued as listed under Table1. Upon receiving a valid input information, decoding of the opcode and the address is made, followed by data transfer from the selected memory location into a 16-bit serial-out shift register. This 16-bit data is then shifted out on the DO pin. D15 bit (MSB) is shifted out first and D0 bit (LSB) is shifted out last. A dummy-bit (logical 0) precedes this 16-bit data output string. Output data changes are initiated on the rising edge of the SK clock. After reading the 16-bit data, the CS signal can be brought low to end the Read cycle. The PRE pin should be held low during this cycle. Refer *Read cycle diagram*.

This device also offers "sequential memory read" operation to allow reading of data from the additional memory locations instead of just one location. It is started in the same manner as normal read but the cycle is continued to read further data (instead of terminating after reading the first 16-bit data). After providing 16-bit data, the device automatically increments the address pointer to the next location and continues to provide the data from that location. Any number of locations can be read out in this manner, however, after reading out from the last location, the address pointer points back to the first location. If the cycle is continued further, data will be read from this first location onward. In this mode of read, the dummy-bit is present only when the very first data is read (like normal read cycle) and is not present on subsequent data reads. The PRE pin should be held low during this cycle. Refer *Sequential Read cycle diagram*.

2) Write Enable (WEN)

When V_{CC} is applied to the part, it "powers up" in the Write Disable (WDS) state. Therefore, all programming operations (for both memory array and Protect Register) must be preceded by a Write Enable (WEN) instruction. Once a Write Enable instruction is executed, programming remains enabled until a Write Disable (WDS) instruction is executed or V_{CC} is completely removed from the part. Input information (Start bit, Opcode and Address) for this WEN instruction should be issued as listed under Table1. The device becomes write-enabled at the end of this cycle when the CS signal is brought low. The PRE pin should be held low during this cycle. Execution of a READ instruction is independent of WEN instruction. Refer *Write Enable cycle diagram.*

3) Write (WRITE)

WRITE instruction allows write operation to a specified location in the memory with a specified data. This instruction is valid only when the following are true:

- Device is write-enabled (Refer WEN instruction)
- Address of the write location is not write-protected
- PE pin is held high during this cycle
- PRE pin should be held low during this cycle

Input information (Start bit, Opcode, Address and Data) for this WRITE instruction should be issued as listed under Table1. After inputting the last bit of data (D0 bit), CS signal must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. It takes t_{WP} time (Refer appropriate DC and AC Electrical Characteristics table) for the internal programming cycle to finish. During this time, the device remains busy and is not ready for another instruction.

The status of the internal programming cycle can be polled at any time by bringing the CS signal high again, after t_{CS} interval. When CS signal is high, the DO pin indicates the READY/BUSY status of the chip. DO = logical 0 indicates that the programming is still in progress. DO = logical 1 indicates that the programming is finished and the device is ready for another instruction. It is not required to provide the SK clock during this status polling. While the device is busy, it is recommended that no new instruction be issued. Refer *Write cycle diagram.*

It is also recommended to follow this instruction (after the device becomes READY) with a Write Disable (WDS) instruction to safeguard data against corruption due to spurious noise, inadvertent writes etc.

4) Write All (WRALL)

Write all (WRALL) instruction is similar to the Write instruction except that WRALL instruction will simultaneously program all memory locations with the data pattern specified in the instruction. This instruction is valid only when the following are true:

- Protect Register has been cleared (Refer PRCLEAR instruction)
- Device is write-enabled (Refer WEN instruction)
- PE pin is held high during this cycle
- PRE pin should be held low during this cycle

Input information (Start bit, Opcode, Address and Data) for this WRALL instruction should be issued as listed under Table1. After inputting the last bit of data (D0 bit), CS signal must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. It takes t_{WP} time (Refer appropriate DC and AC Electrical Characteristics table) for the internal programming cycle to finish. During this time, the device remains busy and is not ready for another instruction. Status of the internal programming can be polled as described under WRITE instruction description. While the device is busy, it is recommended that no new instruction be issued. Refer *Write All cycle diagram.*

5) Write Disable (WDS)

Write Disable (WDS) instruction disables all programming operations and is recommended to follow all programming operations. Executing this instruction after a valid write instruction would protect against accidental data disturb due to spurious noise, glitches, inadvertent writes etc. Input information (Start bit, Opcode and Address) for this WDS instruction should be issued as listed under Table1. The device becomes write-disabled at the end of this cycle when the CS signal is brought low. Execution of a READ instruction is independent of WDS instruction. Refer *Write Disable cycle diagram.*

Protect Register Instructions

Following five instructions, PRREAD, PREN, PRCLEAR, PRWRITE and PRDS are specific to operations intended for Protect Register. The PRE pin should be held high during these instructions.

1) Protect Register Read (PRREAD)

This instruction reads the content of the internal Protect Register. Content of this register is 6-bit wide and is the starting address of the "write-protected" section of the memory array. All memory locations greater than or equal to this address are write-protected. Input information (Start bit, Opcode and Address) for this PRREAD instruction should be issued as listed under Table1. Upon receiving a valid input information, decoding of the opcode and the address is made, followed by data transfer (address information) from the Protect Register. This 6-bit data is then shifted out on the DO pin with the MSB first and the LSB last. Like the READ instruction a dummy-bit (logical 0) precedes this 6-bit data output string. Output data changes are initiated on the rising edge of the SK clock. After reading the 6-bit data, the CS signal can be brought low to end the PRREAD cycle. The PRE pin should be held high during this cycle. Refer *Protect Register Read cycle diagram.*

2) Protect Register Enable (PREN)

This instruction is required to enable PRCLEAR, PRWRITE and PRDS instructions and should be executed prior to executing PRCLEAR, PRWRITE and PRDS instructions. However, this PREN instruction is enabled (valid) only the following are true

- Device is write-enabled (Refer WEN instruction)
- PE pin is held high during this cycle
- PRE pin is held high during this cycle

Input information (Start bit, Opcode and Address) for this PREN instruction should be issued as listed under Table1. The Protect Register becomes enabled for PRCLEAR, PRWRITE and PRDS instructions at the end of this cycle when the CS signal is brought low. Note that this PREN instruction **must immediately precede** a PRCLEAR, PRWRITE or PRDS instruction. In other words, no other instruction should be executed between a PREN instruction and a PRCLEAR, PRWRITE or PRDS instruction. Refer *Protect Register Enable cycle diagram.*

3) Protect Register Clear (PRCLEAR)

This instruction clears the content of the Protect register and therefore enables write operations (WRITE or WRALL) to all memory locations. Executing this instruction will program the content of the Protect Register with a pattern of all 1s. However, in this case, WRITE operation to the last memory address (0x111111) is still enabled. PRCLEAR instruction is enabled (valid) only when the following are true:

- PREN instruction was executed **immediately prior** to PRCLEAR instruction
- PE pin is held high during this cycle
- PRE pin is held high during this cycle

Input information (Start bit, Opcode and Address) for this PRCLEAR instruction should be issued as listed under Table1. After inputting the last bit of address (A0 bit), CS signal must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed clear cycle. It takes t_{WP} time (Refer appropriate DC and AC Electrical Characteristics table) for the internal clear cycle to finish. During this time, the device remains busy and is not ready for another instruction. Status of the internal programming can be polled as described under WRITE instruction description. While the device is busy, it is recommended that no new instruction be issued. Refer *Protect Register Clear cycle diagram.*

4) Protect Register Write (PRWRITE)

This instruction is used to write the starting address of the memory section to be write-protected into the Protect register. After the execution of PRWRITE instruction, all memory locations greater than or equal to this address are write-protected. PRWRITE instruction is enabled (valid) only the following are true:

- PRCLEAR instruction was executed first (to clear the Protect Register)
- PREN instruction was executed **immediately prior** to PRWRITE instruction
- PE pin is held high during this cycle
- PRE pin is held high during this cycle

Input information (Start bit, Opcode and Address) for this PRWRITE instruction should be issued as listed under Table1. After inputting the last bit of address (A0 bit), CS signal must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. It takes t_{WP} time (Refer appropriate DC and AC Electrical Characteristics table) for the internal programming cycle to finish. During this time, the device remains busy and is not ready for another instruction. Status of the internal programming can be polled as described under WRITE instruction description. While the device is busy, it is recommended that no new instruction be issued. Refer *Protect Register Write cycle diagram.*

5) Protect Register Disable (PRDS)

Unlike all other instructions, this instruction is a **one-time-only** instruction which when executed **permanently write-protects the Protect Register** and renders it unalterable in the future. This instruction is useful to safeguard vital data (typically read only data) in the memory against any possible corruption. PRDS instruction is enabled (valid) only the following are true:

- PREN instruction was executed **immediately prior** to PRDS instruction
- PE pin is held high during this cycle
- PRE pin is held high during this cycle

Input information (Start bit, Opcode and Address) for this PRDS instruction should be issued as listed under Table1. After inputting the last bit of address (A0 bit), CS signal must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. It takes t_{WP} time (Refer appropriate DC and AC Electrical Characteristics table) for the internal programming cycle to finish. During this time, the device remains busy and is not ready for another instruction. Status of the internal programming can be polled as described under WRITE instruction description. While the device is busy, it is recommended that no new instruction be issued. The Protect Register is permanently write-protected at the end of this cycle. Refer *Protect Register Disable cycle diagram.*

Clearing of Ready/Busy status

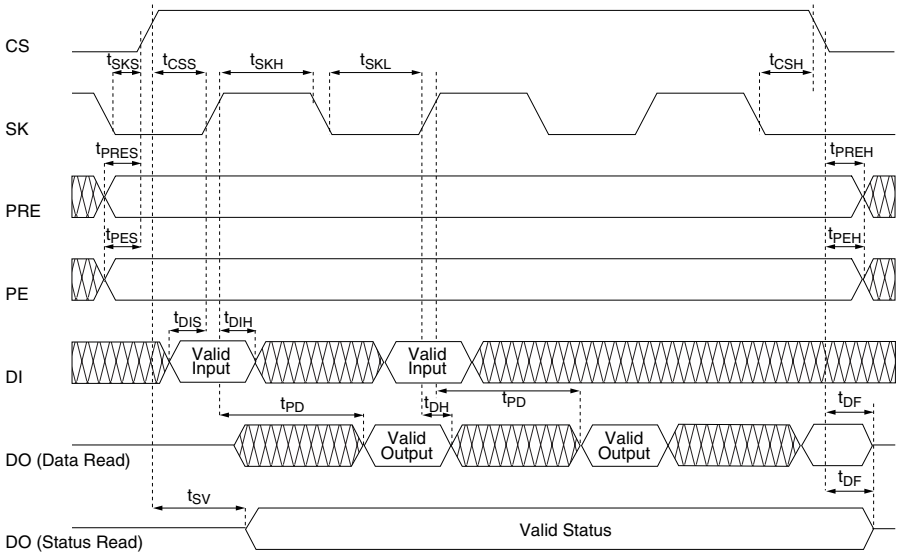
When programming is in progress, the Data-Out pin will display the programming status as either BUSY (low) or READY (high) when CS is brought high (DO output will be tri-stated when CS is low). To restate, during programming, the CS pin may be brought high and low any number of times to view the programming status without affecting the programming operation. Once programming is completed (Output in READY state), the output is 'cleared' (returned to normal tri-state condition) by clocking in a Start Bit. After the Start Bit is clocked in, the output will return to a tri-stated condition. When clocked in, this Start Bit can be the first bit in a command string, or CS can be brought low again to reset all internal circuits. Refer *Clearing Ready Status* diagram.

Related Document

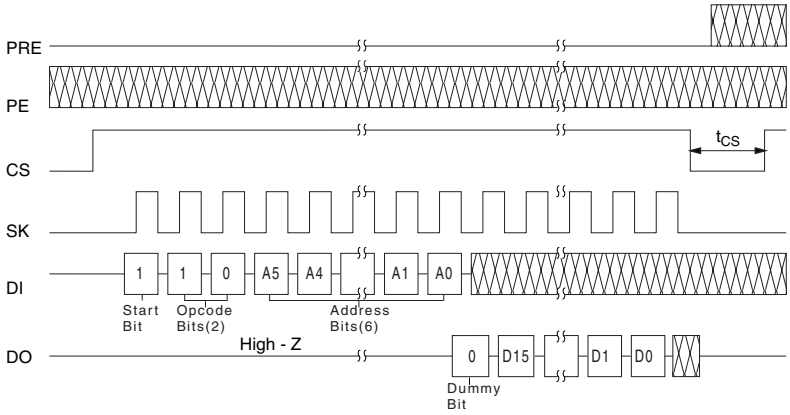
Application Note: AN758 - Using Fairchild's MICROWIRE™ EEPROM.

Timing Diagrams

SYNCHRONOUS DATA TIMING

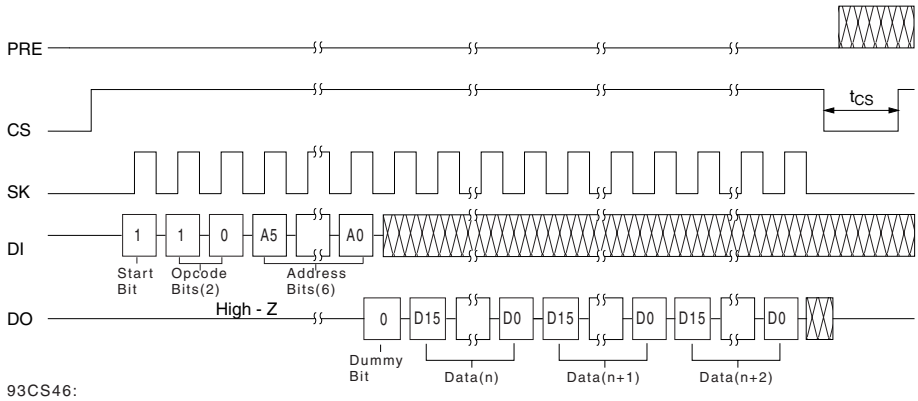


NORMAL READ CYCLE (READ)



93CS46:
Address bits pattern -> User defined

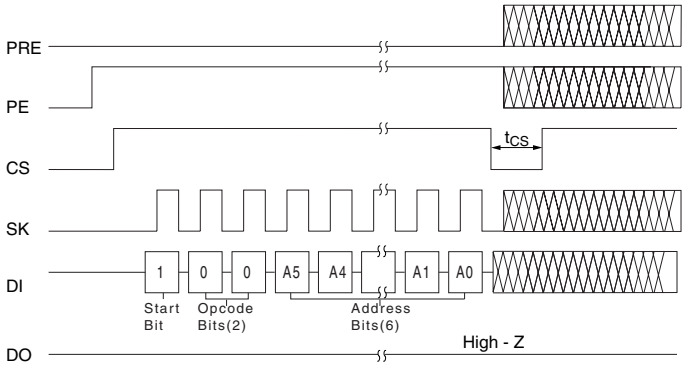
SEQUENTIAL READ CYCLE (PRE = 0; PE = X)



93CS46:
Address bits pattern -> User defined

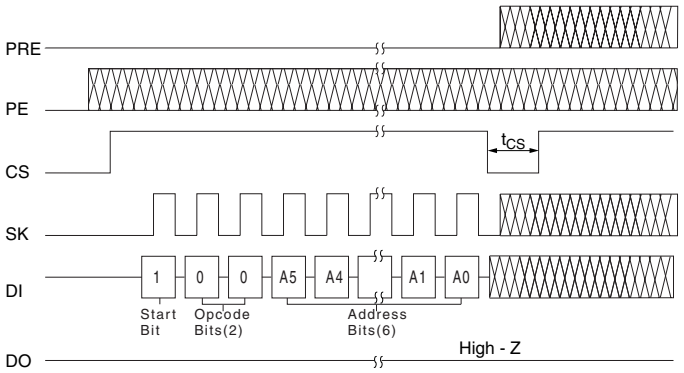
Timing Diagrams (Continued)

WRITE ENABLE CYCLE (WEN)



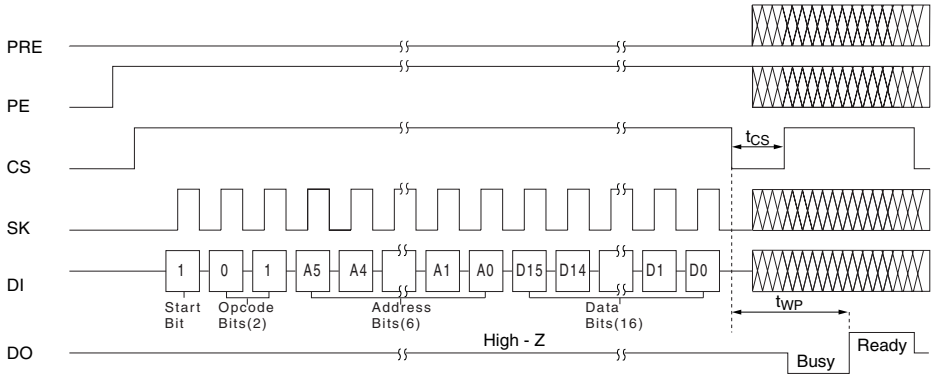
93CS46:
Address bits pattern -> 1-1-x-x-x-x; (x -> Don't Care, can be 0 or 1)

WRITE DISABLE CYCLE (WDS)



93CS46:
Address bits pattern -> 0-0-x-x-x-x; (x -> Don't Care, can be 0 or 1)

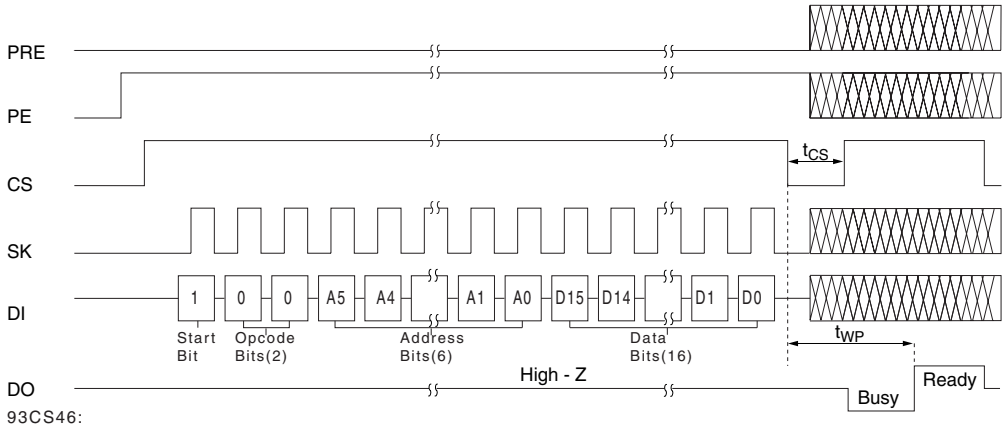
WRITE CYCLE (WRITE)



93CS46:
Address bits pattern -> User defined
Data bits pattern -> User defined

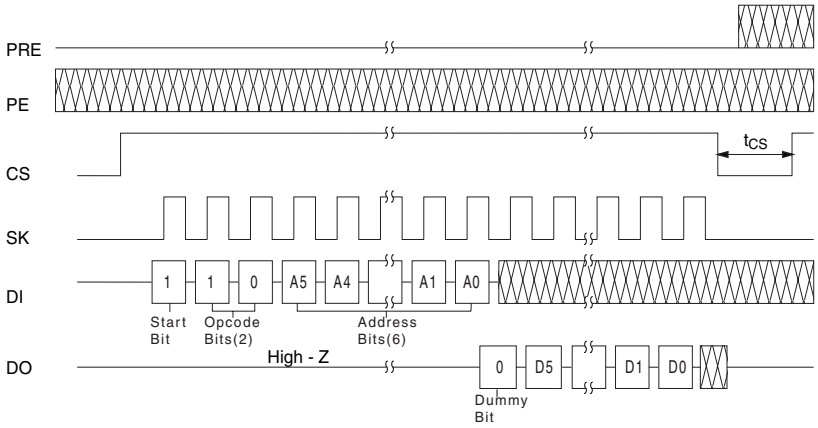
Timing Diagrams (Continued)

WRITE ALL CYCLE (WRALL)



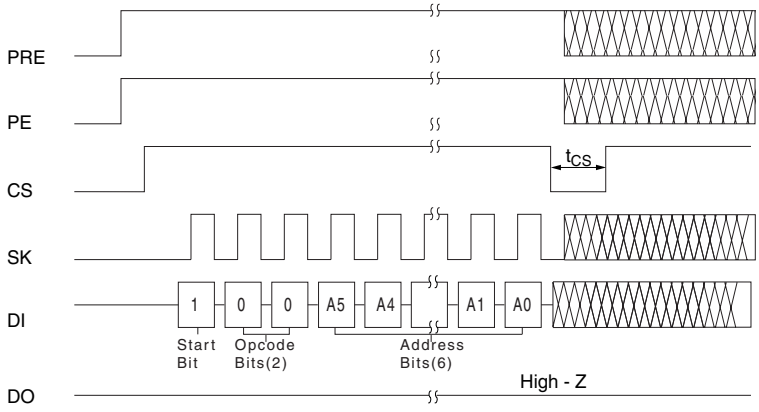
93CS46:
Address bits pattern -> 0-1-x-x-x-x; (x -> Don't Care, can be 0 or 1)
Data bits pattern -> User defined

PROTECT REGISTER READ CYCLE (PRREAD)



93CS46:
Address bits pattern -> x-x-x-x-x-x; (x -> Don't Care, can be 0 or 1)

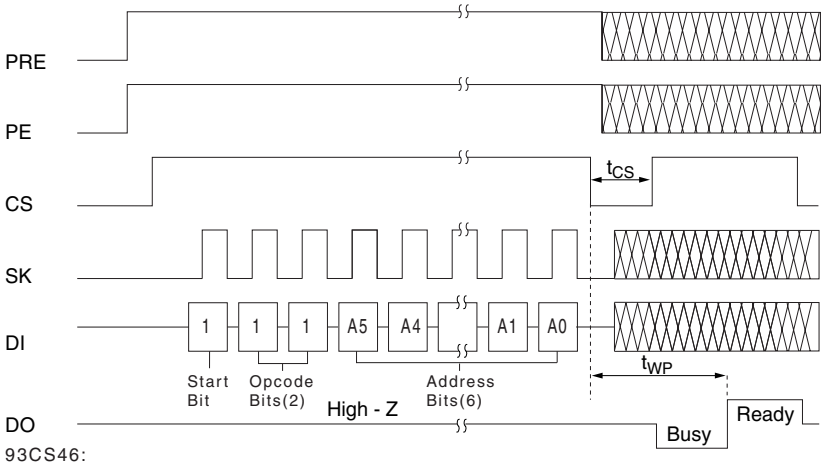
PROTECT REGISTER ENABLE CYCLE (PREN)



93CS46:
Address bits pattern -> 1-1-x-x-x-x; (x -> Don't Care, can be 0 or 1)

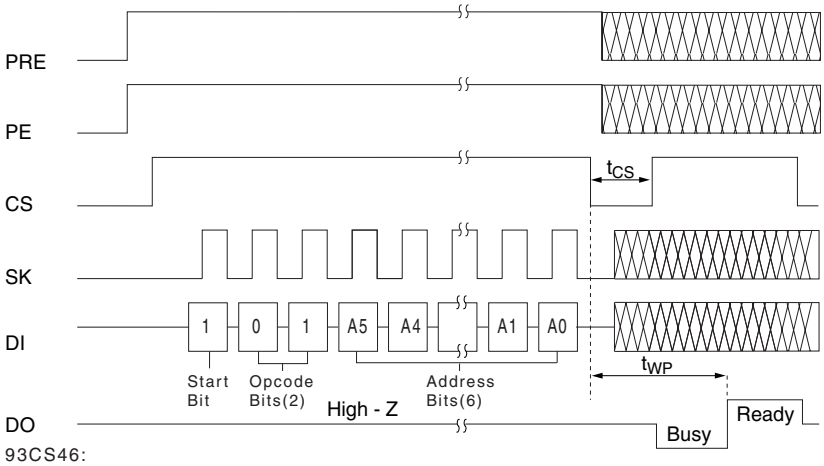
Timing Diagrams (Continued)

PROTECT REGISTER CLEAR CYCLE (PRCLEAR)



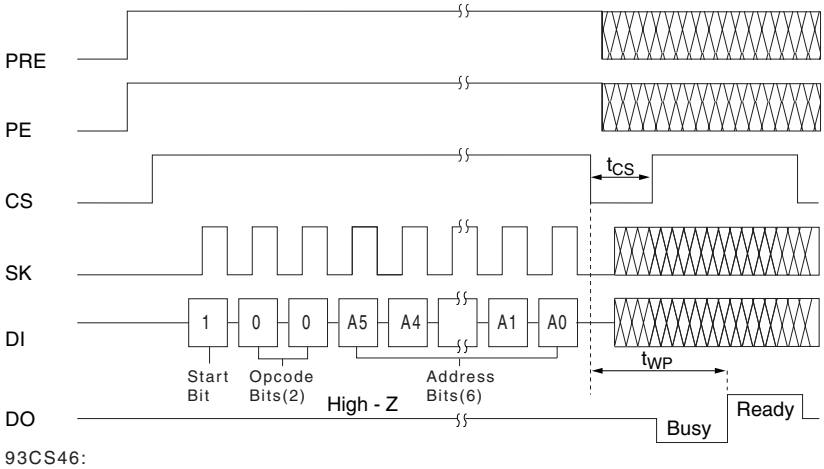
93CS46:
Address bits pattern -> 1-1-1-1-1-1

PROTECT REGISTER WRITE CYCLE (PRWRITE)



93CS46:
Address bits pattern -> User defined

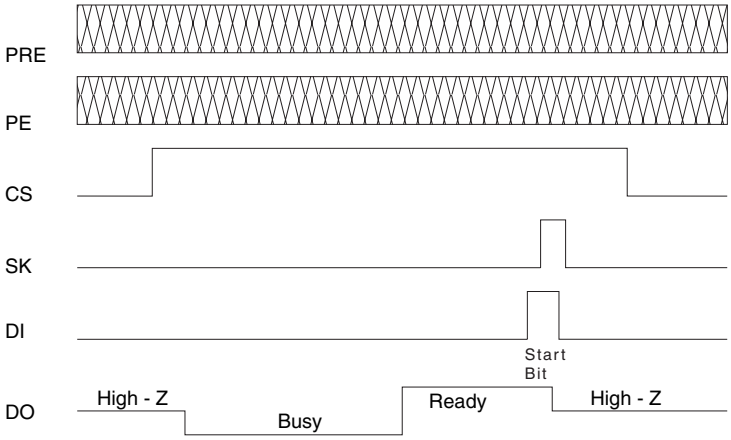
PROTECT REGISTER DISABLE CYCLE (PRDS)



93CS46:
Address bits pattern -> 0-0-0-0-0-0

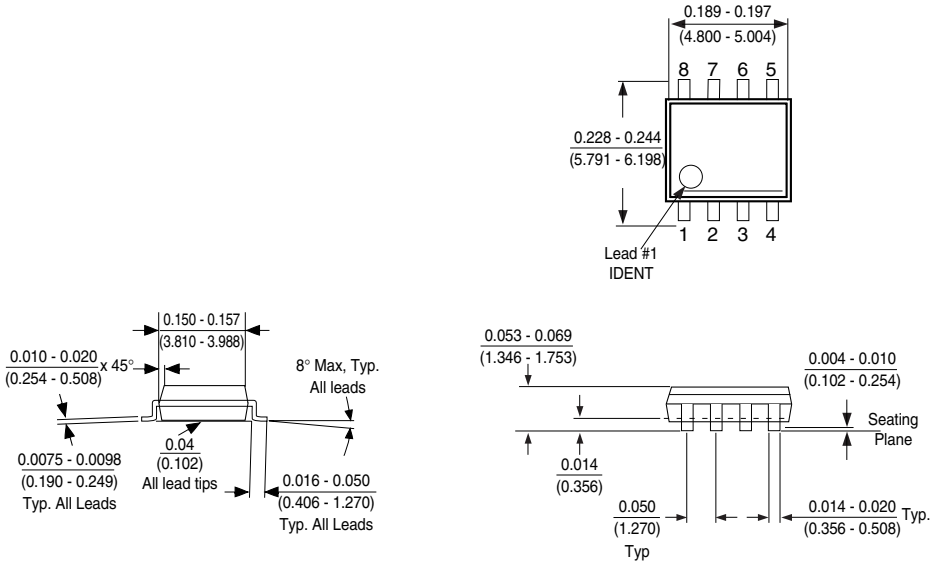
Timing Diagrams (Continued)

CLEARING READY STATUS



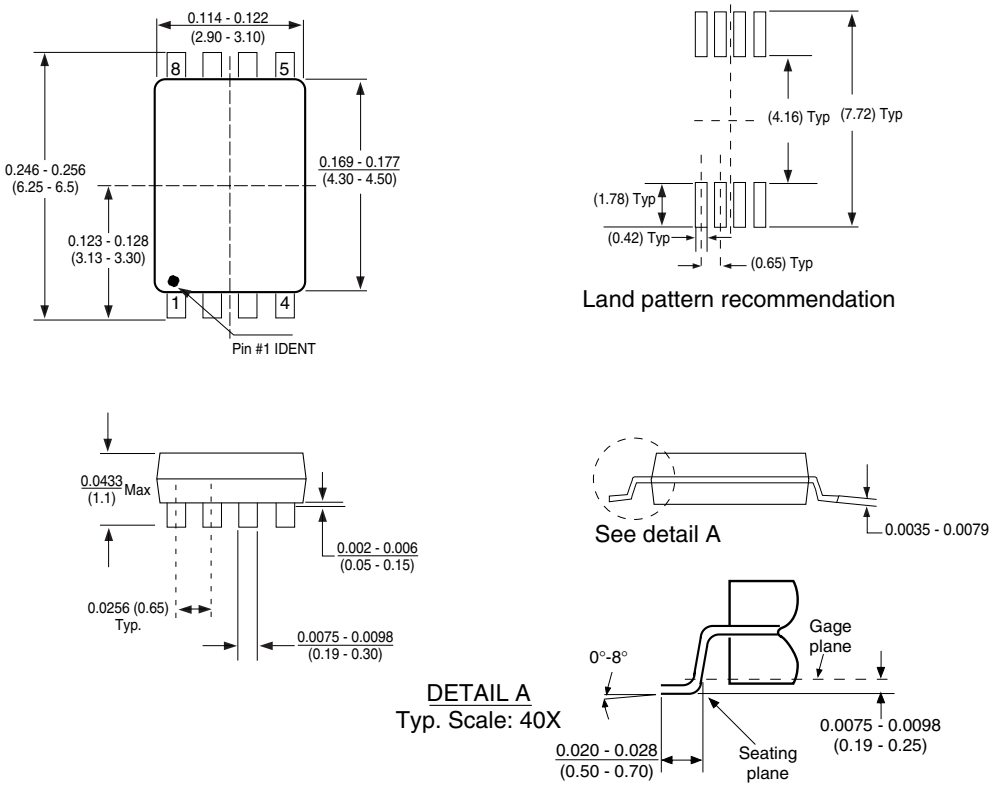
Note: This Start bit can also be part of a next instruction. Hence the cycle can be continued(instead of getting terminated, as shown) as if a new instruction is being issued.

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Package, Small Outline, 0.15 Wide, 8-Lead (M8)
Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted

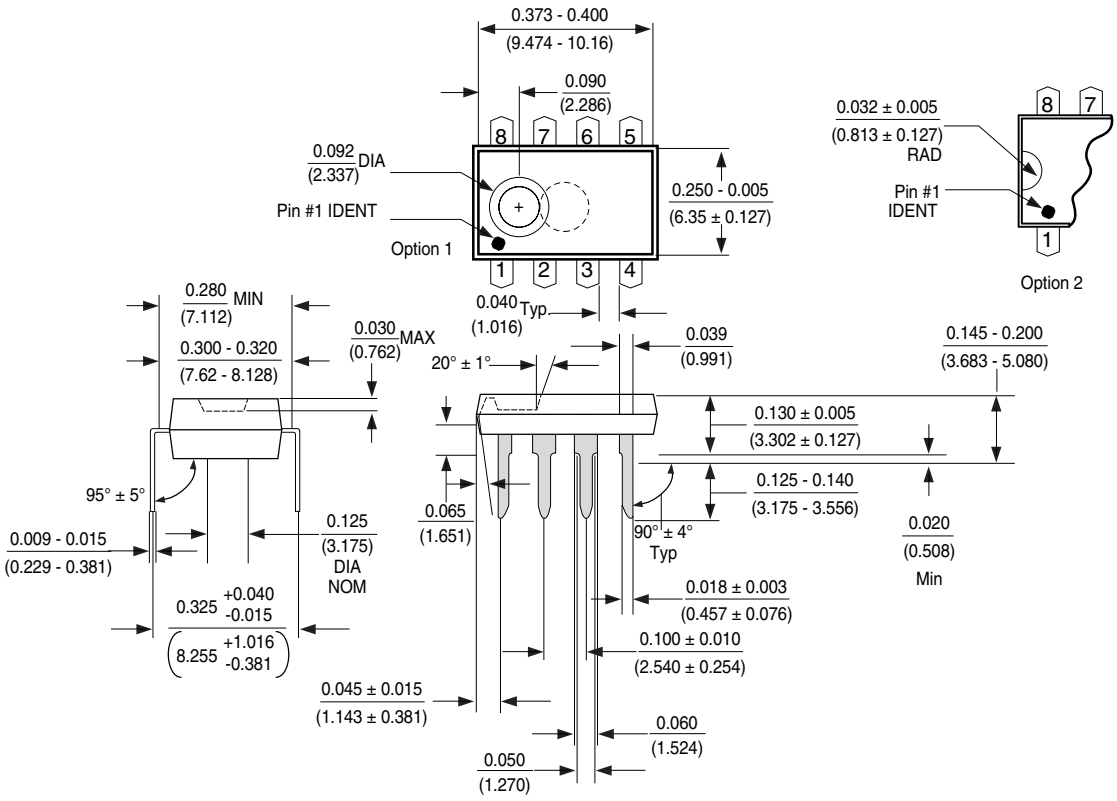


Notes: Unless otherwise specified

1. Reference JEDEC registration MO153. Variation AA. Dated 7/93

8-Pin Molded TSSOP, JEDEC (MT8)
Package Number MTC08

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Package Number N08E

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FAIRCHILD SEMICONDUCTOR™

February 2000

NM93CS56 (MICROWIRE™ Bus Interface) 2048-Bit Serial EEPROM with Data Protect and Sequential Read

General Description

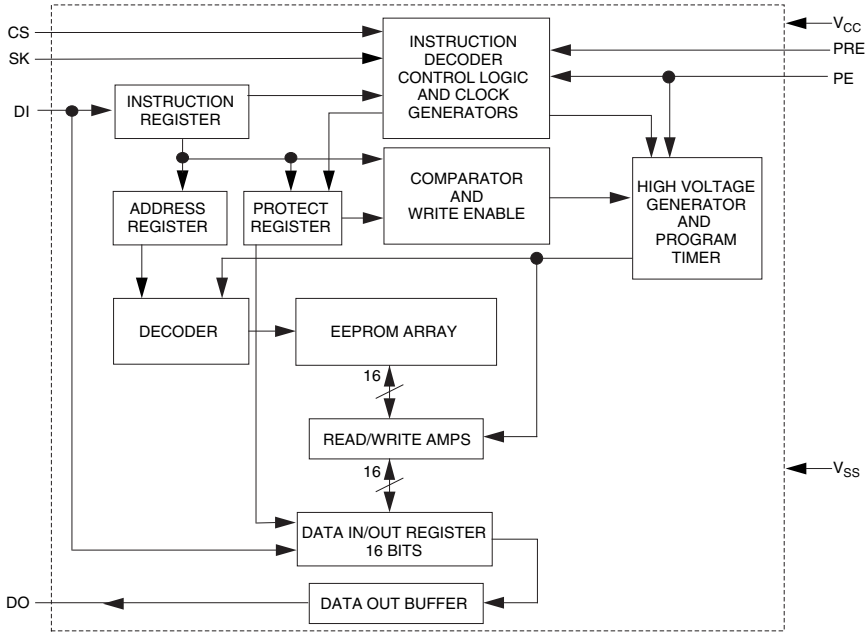
NM93CS56 is a 2048-bit CMOS non-volatile EEPROM organized as 128 x 16-bit array. This device features MICROWIRE interface which is a 4-wire serial bus with chipselect (CS), clock (SK), data input (DI) and data output (DO) signals. This interface is compatible to many of standard Microcontrollers and Microprocessors. NM93CS56 offers programmable write protection to the memory array using a special register called Protect Register. Selected memory locations can be protected against write by programming this Protect Register with the address of the first memory location to be protected (all locations greater than or equal to this first address are then protected from further change). Additionally, this address can be "permanently locked" into the device, making all future attempts to change data impossible. In addition this device features "sequential read", by which, entire memory can be read in one cycle instead of multiple single byte read cycles. There are 10 instructions implemented on the NM93CS56, 5 of which are for memory operations and the remaining 5 are for Protect Register operations. This device is fabricated using Fairchild Semiconductor floating-gate CMOS process for high reliability, high endurance and low power consumption.

"LZ" and "L" versions of NM93CS56 offer very low standby current making them suitable for low power applications. This device is offered in both SO and TSSOP packages for small space considerations.

Features

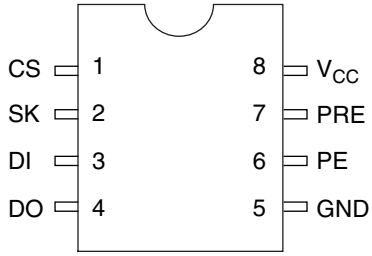
- Wide V_{CC} 2.7V - 5.5V
- Programmable write protection
- Sequential register read
- Typical active current of 200μA
  10μA standby current typical
  1μA standby current typical (L)
  0.1μA standby current typical (LZ)
- No Erase instruction required before Write instruction
- Self timed write cycle
- Device status during programming cycles
- 40 year data retention
- Endurance: 1,000,000 data changes
- Packages available: 8-pin SO, 8-pin DIP, 8-pin TSSOP

Functional Diagram



Connection Diagram

Dual-In-Line Package (N)
8–Pin SO (M8) and 8–Pin TSSOP (MT8)



Top View
Package Number
N08E, M08A and MTC08

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
V_{CC}	Power Supply

Ordering Information

NM 93 CS XX LZ E XXX

	Letter	Description
Package	N	8-pin DIP
	M8	8-pin SO
	MT8	8-pin TSSOP
Temp. Range	None	0 to 70°C
	V	-40 to +125°C
	E	-40 to +85°C
Voltage Operating Range	Blank	4.5V to 5.5V
	L	2.7V to 5.5V
	LZ	2.7V to 5.5V and <1µA Standby Current
Density	56	2048 bits
	C	CMOS
	CS	Data protect and sequential read
Interface	93	MICROWIRE
Fairchild Memory Prefix		

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to -0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93CS56	0°C to +70°C
NM93CS56E	-40°C to +85°C
NM93CS56V	-40°C to +125°C
Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 4.5V to 5.5V unless otherwise specified

Symbol	Parameter	Conditions	Min	Max	Units
I_{CCA}	Operating Current	CS = V_{IH}, SK=1.0 MHz		1	mA
I_{CCS}	Standby Current	CS = V_{IL}		50	µA
I_{IL} I_{OL}	Input Leakage Output Leakage	V_{IN} = 0V to V_{CC} (Note 2)		±-1	µA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage		-0.1 2	0.8 V_{CC} +1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage	I_{OL} = 2.1 mA I_{OH} = -400 µA	 2.4	0.4	V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage	I_{OL} = 10 µA I_{OH} = -10 µA	 V_{CC} - 0.2	0.2	V
f_{SK}	SK Clock Frequency	(Note 3)		1	MHz
t_{SKH}	SK High Time	0°C to +70°C -40°C to +125°C	250 300		ns
t_{SKL}	SK Low Time		250		ns
t_{SKS}	SK Setup Time		50		ns
t_{CS}	Minimum CS Low Time	(Note 4)	250		ns
t_{CSS}	CS Setup Time		100		ns
t_{PRES}	PRE Setup Time		50		ns
t_{DH}	DO Hold Time		70		ns
t_{PES}	PE Setup Time		50		ns
t_{DIS}	DI Setup Time		100		ns
t_{CSH}	CS Hold Time		0		ns
t_{PEH}	PE Hold Time		250		ns
t_{PREH}	PRE Hold Time		50		ns
t_{DIH}	DI Hold Time		20		ns
t_{PD}	Output Delay			500	ns
t_{SV}	CS to Status Valid			500	ns
t_{DF}	CS to DO in Hi-Z	CS = V_{IL}		100	ns
t_{WP}	Write Cycle Time			10	ms

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to -0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93CS56L/LZ	0°C to +70°C
NM93CS56LE/LZE	-40°C to +85°C
NM93CS56LV/LZV	-40°C to +125°C
Power Supply (V_{CC})	2.7V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 2.7V to 5.5V unless otherwise specified

Symbol	Parameter	Conditions	Min	Max	Units
I_{CCA}	Operating Current	CS = V_{IH}, SK=1.0 MHz		1	mA
I_{CCS}	Standby Current L LZ (2.7V to 4.5V)	CS = V_{IL}		 10 1	 µA µA
I_{IL} I_{OL}	Input Leakage Output Leakage	V_{IN} = 0V to V_{CC} (Note 2)		±1	µA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage		-0.1 0.8V_{CC}	0.15V_{CC} V_{CC} +1	V
V_{OL} V_{OH}	Output Low Voltage Output High Voltage	I_{OL} = 10µA I_{OH} = -10µA	 0.9V_{CC}	0.1V_{CC}	V
f_{SK}	SK Clock Frequency	(Note 3)	0	250	KHz
t_{SKH}	SK High Time		1		µs
t_{SKL}	SK Low Time		1		µs
t_{SKS}	SK Setup Time		0.2		µs
t_{CS}	Minimum CS Low Time	(Note 4)	1		µs
t_{CSS}	CS Setup Time		0.2		µs
t_{PRES}	PRE Setup Time		50		ns
t_{DH}	DO Hold Time		70		ns
t_{PES}	PE Setup Time		50		ns
t_{DIS}	DI Setup Time		0.4		µs
t_{CSH}	CS Hold Time		0		ns
t_{PEH}	PE Hold Time		250		ns
t_{PREH}	PRE Hold Time		50		ns
t_{DIH}	DI Hold Time		0.4		µs
t_{PD}	Output Delay			2	µs
t_{SV}	CS to Status Valid			1	µs
t_{DF}	CS to DO in Hi-Z	CS = V_{IL}		0.4	µs
t_{WP}	Write Cycle Time			15	ms

Capacitance T_A = 25°C, f = 1 MHz (Note 5)

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical leakage values are in the 20nA range.

Note 3: The shortest allowable SK clock period = $1/f_{SK}$ (as shown under the f_{SK} parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both t_{SKH} and t_{SKL} limits must be observed. Therefore, it is not allowable to set $1/f_{SK} = t_{SKHminimum} + t_{SKLminimum}$ for shorter SK cycle time operation.

Note 4: CS (Chip Select) must be brought low (to V_{IL}) for an interval of t_{CS} in order to reset all internal device registers (device reset) prior to beginning another opcode cycle. (This is shown in the opcode diagram on the following page.)

Note 5: This parameter is periodically sampled and not 100% tested.

AC Test Conditions

V_{CC} Range	V_{IL}/V_{IH} Input Levels	V_{IL}/V_{IH} Timing Level	V_{OL}/V_{OH} Timing Level	I_{OL}/I_{OH}
2.7V ≤ V_{CC} ≤ 5.5V (Extended Voltage Levels)	0.3V/1.8V	1.0V	0.8V/1.5V	±10µA
4.5V ≤ V_{CC} ≤ 5.5V (TTL Levels)	0.4V/2.4V	1.0V/2.0V	0.4V/2.4V	2.1mA/-0.4mA
Output Load: 1 TTL Gate (C_L = 100 pF)				

Pin Description

Chip Select (CS)

This is an active high input pin to NM93CS56 EEPROM (the device) and is generated by a master that is controlling the device. A high level on this pin selects the device and a low level deselects the device. All serial communications with the device is enabled only when this pin is held high. However this pin cannot be permanently tied high, as a rising edge on this signal is required to reset the internal state-machine to accept a new cycle and a falling edge to initiate an internal programming after a write cycle. All activity on the SK, DI and DO pins are ignored while CS is held low.

Serial Clock (SK)

This is an input pin to the device and is generated by the master that is controlling the device. This is a clock signal that synchronizes the communication between a master and the device. All input information (DI) to the device is latched on the rising edge of this clock input, while output data (DO) from the device is driven from the rising edge of this clock input. This pin is gated by CS signal.

Serial Input (DI)

This is an input pin to the device and is generated by the master that is controlling the device. The master transfers Input information (Start bit, Opcode bits, Array addresses and Data) serially via this pin into the device. This Input information is latched on the rising edge of the SCK. This pin is gated by CS signal.

Serial Output (DO)

This is an output pin from the device and is used to transfer Output data via this pin to the controlling master. Output data is serially shifted out on this pin from the rising edge of the SCK. This pin is active only when the device is selected.

Protect Register Enable (PRE)

This is an active high input pin to the device and is used to distinguish operations to memory array and operations to Protect Register. When this pin is held low, operations to the memory array are enabled. When this pin is held high, operations to the Protect Register are enabled. This pin operates in conjunction with PE pin. Refer Table1 for functional matrix of this pin for various operations.

Program Enable (PE)

This is an active high input pin to the device and is used to enable operations, that are write in nature, to the memory array and to the Protect register. When this pin is held high, operations that are "write" in nature are enabled. When this pin is held low, operations that are "write" in nature are disabled. This pin operates in conjunction with PRE pin. Refer Table1 for functional matrix of this pin for various operations.

Microwire Interface

A typical communication on the Microwire bus is made through the CS, SK, DI and DO signals. To facilitate various operations on the Memory array and on the Protect Register, a set of 10 instructions are implemented on NM93CS56. The format of each instruction is listed in Table 1.

Instruction

Each of the above 10 instructions is explained under individual instruction descriptions.

Start Bit

This is a 1-bit field and is the first bit that is clocked into the device when a Microwire cycle starts. This bit has to be "1" for a valid cycle to begin. Any number of preceding "0" can be clocked into the device before clocking a "1".

Opcode

This is a 2-bit field and should immediately follow the start bit. These two bits (along with PRE, PE signals and 2 MSB of address field) select a particular instruction to be executed.

Address Field

This is a 8-bit field and should immediately follow the Opcode bits. In NM93CS56, only the LSB 7 bits are used for address decoding during READ, WRITE and PRWRITE instructions. During these three instructions (READ, WRITE and PRWRITE), the MSB is "don't care" (can be 0 or 1). During all other instructions (with the exception of PRREAD), the MSB 2 bits are used to decode instruction (along with Opcode bits, PRE and PE signals).

Data Field

This is a 16-bit field and should immediately follow the Address bits. Only the WRITE and WRALL instructions require this field. D15 (MSB) is clocked first and D0 (LSB) is clocked last (both during writes as well as reads).

TABLE 1. Instruction set

Instruction	Start Bit	Opcode Field	Address Field								Data Field	PRE Pin	PE Pin
READ	1	10	X	A6	A5	A4	A3	A2	A1	A0		0	X
WEN	1	00	1	1	X	X	X	X	X	X		0	1
WRITE	1	01	X	A6	A5	A4	A3	A2	A1	A0	D15-D0	0	1
WRALL	1	00	0	1	X	X	X	X	X	X	D15-D0	0	1
WDS	1	00	0	0	X	X	X	X	X	X		0	X
PRREAD	1	10	X	X	X	X	X	X	X	X		1	X
PREN	1	00	1	1	X	X	X	X	X	X		1	1
PRCLEAR	1	11	1	1	1	1	1	1	1	1		1	1
PRWRITE	1	01	X	A6	A5	A4	A3	A2	A1	A0		1	1
PRDS	1	00	0	0	0	0	0	0	0	0		1	1

Functional Description

A typical Microwire cycle starts by first selecting the device (bringing the CS signal high). Once the device is selected, a valid Start bit ("1") should be issued to properly recognize the cycle. Following this, the 2-bit opcode of appropriate instruction should be issued. After the opcode bits, the 8-bit address information should be issued. For certain instructions, some (or all) of these 8 bits are don't care values (can be "0" or "1"), but they should still be issued. Following the address information, depending on the instruction (WRITE and WRALL), 16-Bit data is issued. Otherwise, depending on the instruction (READ and PRREAD), the device starts to drive the output data on the DO line. Other instructions perform certain control functions and do not deal with data bits. The Microwire cycle ends when the CS signal is brought low. However during certain instructions, falling edge of the CS signal initiates an internal cycle (Programming), and the device remains busy till the completion of the internal cycle. Each of the 10 instructions is explained in detail in the following sections.

Memory Instructions

Following five instructions, READ, WEN, WRITE, WRALL and WDS are specific to operations intended for memory array. The PRE pin should be held low during these instructions.

1) Read and Sequential Read (READ)

READ instruction allows data to be read from a selected location in the memory array. Input information (Start bit, Opcode and Address) for this instruction should be issued as listed under Table1. Upon receiving a valid input information, decoding of the opcode and the address is made, followed by data transfer from the selected memory location into a 16-bit serial-out shift register. This 16-bit data is then shifted out on the DO pin. D15 bit (MSB) is shifted out first and D0 bit (LSB) is shifted out last. A dummy-bit (logical 0) precedes this 16-bit data output string. Output data changes are initiated on the rising edge of the SK clock. After reading the 16-bit data, the CS signal can be brought low to end the Read cycle. The PRE pin should be held low during this cycle. Refer *Read cycle diagram*.

This device also offers "sequential memory read" operation to allow reading of data from the additional memory locations instead of just one location. It is started in the same manner as normal read but the cycle is continued to read further data (instead of terminating after reading the first 16-bit data). After providing 16-bit data, the device automatically increments the address pointer to the next location and continues to provide the data from that location. Any number of locations can be read out in this manner, however, after reading out from the last location, the address pointer points back to the first location. If the cycle is continued further, data will be read from this first location onward. In this mode of read, the dummy-bit is present only when the very first data is read (like normal read cycle) and is not present on subsequent data reads. The PRE pin should be held low during this cycle. Refer *Sequential Read cycle diagram*.

2) Write Enable (WEN)

When V_{CC} is applied to the part, it "powers up" in the Write Disable (WDS) state. Therefore, all programming operations (for both memory array and Protect Register) must be preceded by a Write Enable (WEN) instruction. Once a Write Enable instruction is executed, programming remains enabled until a Write Disable (WDS) instruction is executed or V_{CC} is completely removed from the part. Input information (Start bit, Opcode and Address) for this WEN instruction should be issued as listed under Table1. The device becomes write-enabled at the end of this cycle when the CS signal is brought low. The PRE pin should be held low during this cycle. Execution of a READ instruction is independent of WEN instruction. Refer *Write Enable cycle diagram.*

3) Write (WRITE)

WRITE instruction allows write operation to a specified location in the memory with a specified data. This instruction is valid only when the following are true:

- Device is write-enabled (Refer WEN instruction)
- Address of the write location is not write-protected
- PE pin is held high during this cycle
- PRE pin should be held low during this cycle

Input information (Start bit, Opcode, Address and Data) for this WRITE instruction should be issued as listed under Table1. After inputting the last bit of data (D0 bit), CS signal must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. It takes t_{WP} time (Refer appropriate DC and AC Electrical Characteristics table) for the internal programming cycle to finish. During this time, the device remains busy and is not ready for another instruction.

The status of the internal programming cycle can be polled at any time by bringing the CS signal high again, after t_{CS} interval. When CS signal is high, the DO pin indicates the READY/BUSY status of the chip. DO = logical 0 indicates that the programming is still in progress. DO = logical 1 indicates that the programming is finished and the device is ready for another instruction. It is not required to provide the SK clock during this status polling. While the device is busy, it is recommended that no new instruction be issued. Refer *Write cycle diagram.*

It is also recommended to follow this instruction (after the device becomes READY) with a Write Disable (WDS) instruction to safeguard data against corruption due to spurious noise, inadvertent writes etc.

4) Write All (WRALL)

Write all (WRALL) instruction is similar to the Write instruction except that WRALL instruction will simultaneously program all memory locations with the data pattern specified in the instruction. This instruction is valid only when the following are true:

- Protect Register has been cleared (Refer PRCLEAR instruction)
- Device is write-enabled (Refer WEN instruction)
- PE pin is held high during this cycle
- PRE pin should be held low during this cycle

Input information (Start bit, Opcode, Address and Data) for this WRALL instruction should be issued as listed under Table1. After inputting the last bit of data (D0 bit), CS signal must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. It takes t_{WP} time (Refer appropriate DC and AC Electrical Characteristics table) for the internal programming cycle to finish. During this time, the device remains busy and is not ready for another instruction. Status of the internal programming can be polled as described under WRITE instruction description. While the device is busy, it is recommended that no new instruction be issued. Refer *Write All cycle diagram.*

5) Write Disable (WDS)

Write Disable (WDS) instruction disables all programming operations and is recommended to follow all programming operations. Executing this instruction after a valid write instruction would protect against accidental data disturb due to spurious noise, glitches, inadvertent writes etc. Input information (Start bit, Opcode and Address) for this WDS instruction should be issued as listed under Table1. The device becomes write-disabled at the end of this cycle when the CS signal is brought low. Execution of a READ instruction is independent of WDS instruction. Refer *Write Disable cycle diagram.*

Protect Register Instructions

Following five instructions, PRREAD, PREN, PRCLEAR, PRWRITE and PRDS are specific to operations intended for Protect Register. The PRE pin should be held high during these instructions.

1) Protect Register Read (PRREAD)

This instruction reads the content of the internal Protect Register. Content of this register is 8-bit wide and is the starting address of the "write-protected" section of the memory array. All memory locations greater than or equal to this address are write-protected. Input information (Start bit, Opcode and Address) for this PRREAD instruction should be issued as listed under Table 1. Upon receiving a valid input information, decoding of the opcode and the address is made, followed by data transfer (address information) from the Protect Register. This 8-bit data is then shifted out on the DO pin with the MSB first and the LSB last. Like the READ instruction a dummy-bit (logical 0) precedes this 8-bit data output string. Output data changes are initiated on the rising edge of the SK clock. After reading the 8-bit data, the CS signal can be brought low to end the PRREAD cycle. The PRE pin should be held high during this cycle. Refer *Protect Register Read cycle diagram.*

Though the content of this register is 8-bit wide, only the last 7 bits (LSB) are valid for NM93CS56 device.

2) Protect Register Enable (PREN)

This instruction is required to enable PRCLEAR, PRWRITE and PRDS instructions and should be executed prior to executing PRCLEAR, PRWRITE and PRDS instructions. However, this PREN instruction is enabled (valid) only the following are true

- Device is write-enabled (Refer WEN instruction)
- PE pin is held high during this cycle
- PRE pin is held high during this cycle

Input information (Start bit, Opcode and Address) for this PREN instruction should be issued as listed under Table1. The Protect Register becomes enabled for PRCLEAR, PRWRITE and PRDS instructions at the end of this cycle when the CS signal is brought low. Note that this PREN instruction **must immediately precede** a PRCLEAR, PRWRITE or PRDS instruction. In other words, no other instruction should be executed between a PREN instruction and a PRCLEAR, PRWRITE or PRDS instruction. Refer *Protect Register Enable cycle diagram.*

3) Protect Register Clear (PRCLEAR)

This instruction clears the content of the Protect register and therefore enables write operations (WRITE or WRALL) to all memory locations. Executing this instruction will program the content of the Protect Register with a pattern of all 1s. However, in this case, WRITE operation to the last memory address (0x01111111) is still enabled. PRCLEAR instruction is enabled (valid) only when the following are true:

- PREN instruction was executed **immediately prior** to PRCLEAR instruction
- PE pin is held high during this cycle
- PRE pin is held high during this cycle

Input information (Start bit, Opcode and Address) for this PRCLEAR instruction should be issued as listed under Table1. After inputting the last bit of address (A0 bit), CS signal must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed clear cycle. It takes t_{WP} time (Refer appropriate DC and AC Electrical Characteristics table) for the internal clear cycle to finish. During this time, the device remains busy and is not ready for another instruction. Status of the internal programming can be polled as described under WRITE instruction description. While the device is busy, it is recommended that no new instruction be issued. Refer *Protect Register Clear cycle diagram.*

4) Protect Register Write (PRWRITE)

This instruction is used to write the starting address of the memory section to be write-protected into the Protect register. After the execution of PRWRITE instruction, all memory locations greater than or equal to this address are write-protected. PRWRITE instruction is enabled (valid) only the following are true:

- PRCLEAR instruction was executed first (to clear the Protect Register)
- PREN instruction was executed **immediately prior** to PRWRITE instruction
- PE pin is held high during this cycle
- PRE pin is held high during this cycle

Input information (Start bit, Opcode and Address) for this PRWRITE instruction should be issued as listed under Table1. After inputting the last bit of address (A0 bit), CS signal must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. It takes t_{WP} time (Refer appropriate DC and AC Electrical Characteristics table) for the internal programming cycle to finish. During this time, the device remains busy and is not ready for another instruction. Status of the internal programming can be polled as described under WRITE instruction description. While the device is busy, it is recommended that no new instruction be issued. Refer *Protect Register Write cycle diagram.*

5) Protect Register Disable (PRDS)

Unlike all other instructions, this instruction is a **one-time-only** instruction which when executed **permanently write-protects the Protect Register** and renders it unalterable in the future. This instruction is useful to safeguard vital data (typically read only data) in the memory against any possible corruption. PRDS instruction is enabled (valid) only the following are true:

- PREN instruction was executed **immediately prior** to PRDS instruction
- PE pin is held high during this cycle
- PRE pin is held high during this cycle

Input information (Start bit, Opcode and Address) for this PRDS

instruction should be issued as listed under Table1. After inputting the last bit of address (A0 bit), CS signal must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. It takes t_{WP} time (Refer appropriate DC and AC Electrical Characteristics table) for the internal programming cycle to finish. During this time, the device remains busy and is not ready for another instruction. Status of the internal programming can be polled as described under WRITE instruction description. While the device is busy, it is recommended that no new instruction be issued. The Protect Register is permanently write-protected at the end of this cycle. Refer *Protect Register Disable cycle diagram.*

Clearing of Ready/Busy status

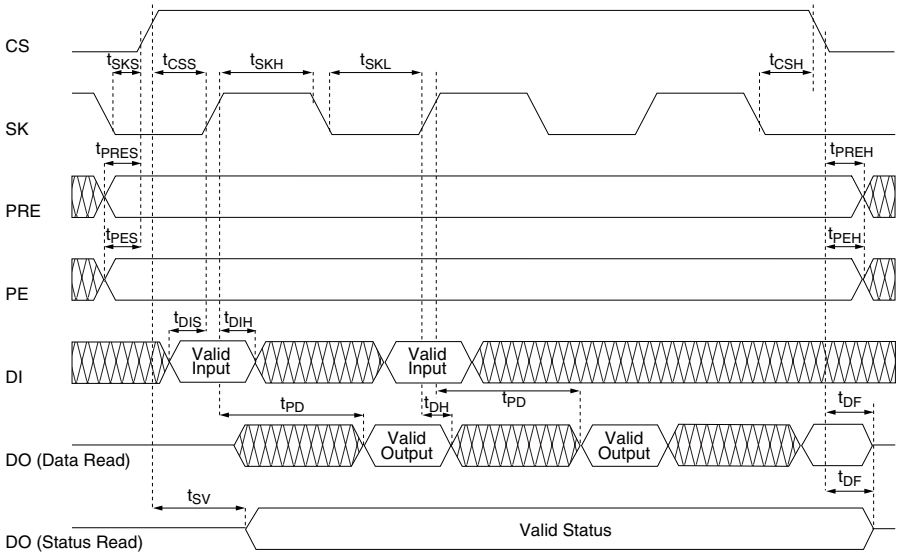
When programming is in progress, the Data-Out pin will display the programming status as either BUSY (low) or READY (high) when CS is brought high (DO output will be tri-stated when CS is low). To restate, during programming, the CS pin may be brought high and low any number of times to view the programming status without affecting the programming operation. Once programming is completed (Output in READY state), the output is 'cleared' (returned to normal tri-state condition) by clocking in a Start Bit. After the Start Bit is clocked in, the output will return to a tri-stated condition. When clocked in, this Start Bit can be the first bit in a command string, or CS can be brought low again to reset all internal circuits. Refer *Clearing Ready Status* diagram.

Related Document

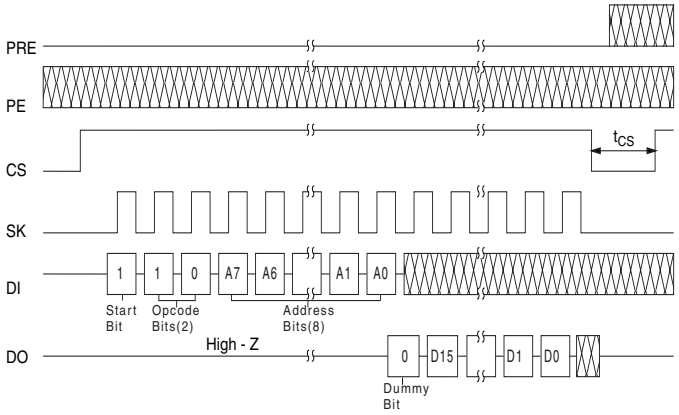
Application Note: AN758 - Using Fairchild's MICROWIRE™ EEPROM.

Timing Diagrams

SYNCHRONOUS DATA TIMING

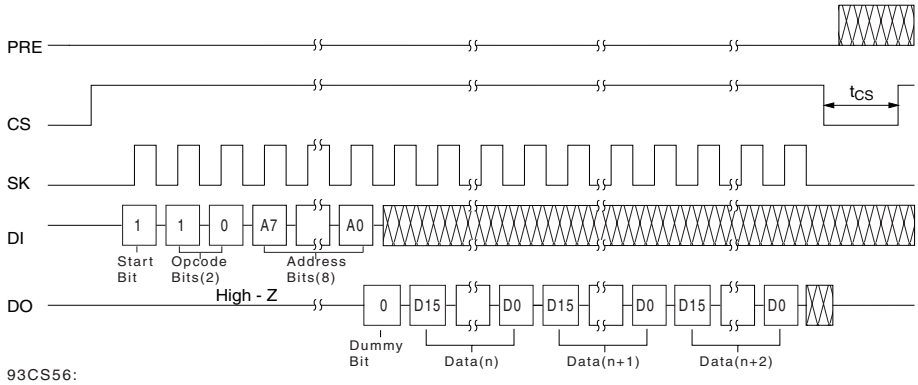


NORMAL READ CYCLE (READ)



93CS56:
Address bits pattern -> x-A6-A5-A4-A3-A2-A1-A0; (x -> Don't Care, can be 0 or 1); (A6-A0 -> User defined)

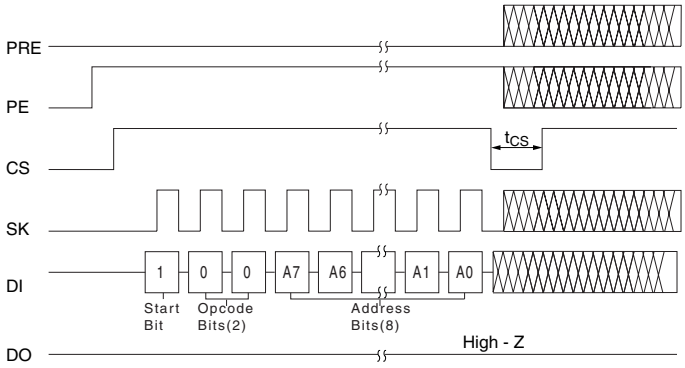
SEQUENTIAL READ CYCLE (PRE = 0; PE = X)



93CS56:
Address bits pattern ->x-A6-A5-A4-A3-A2-A1-A0; (x -> Don't Care, can be 0 or 1); (A6-A0 -> User defined)

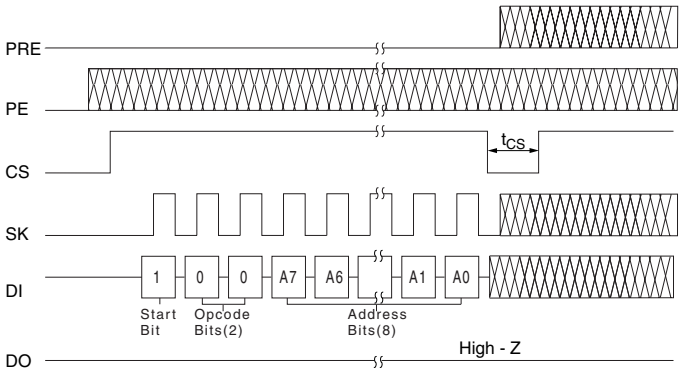
Timing Diagrams (Continued)

WRITE ENABLE CYCLE (WEN)



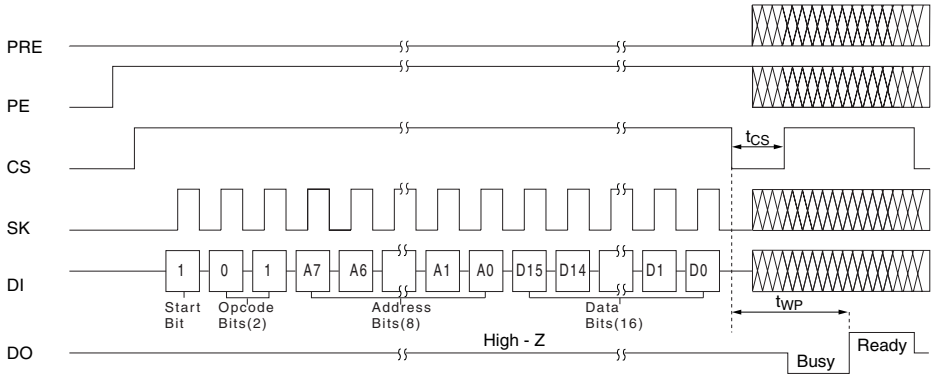
93CS56:
Address bits pattern -> 1-1-x-x-x-x-x-x; (x -> Don't Care, can be 0 or 1)

WRITE DISABLE CYCLE (WDS)



93CS56:
Address bits pattern -> 0-0-x-x-x-x-x-x; (x -> Don't Care, can be 0 or 1)

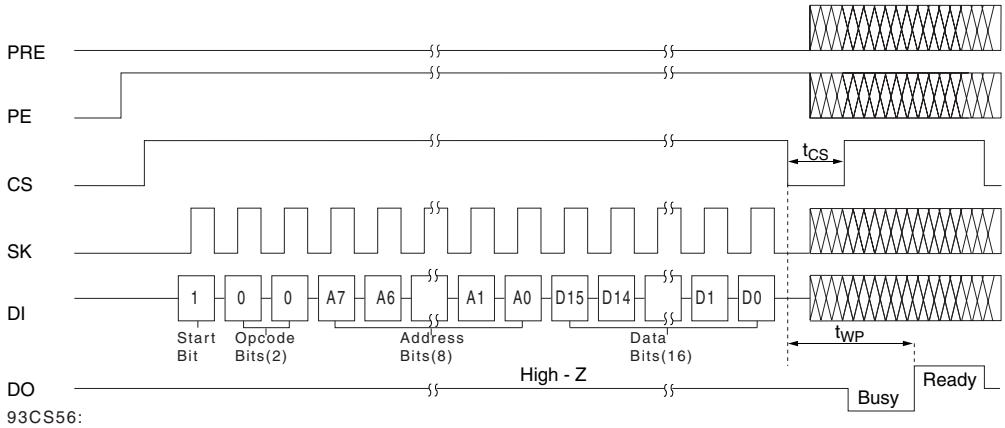
WRITE CYCLE (WRITE)



93CS56:
Address bits pattern -> x-A6-A5-A4-A3-A2-A1-A0; (x -> Don't Care, can be 0 or 1); (A6-A0 -> User defined)
Data bits pattern -> User defined

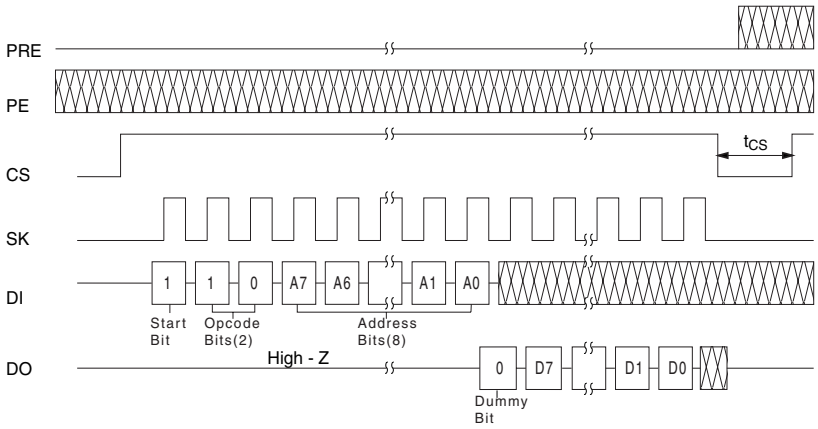
Timing Diagrams (Continued)

WRITE ALL CYCLE (WRALL)



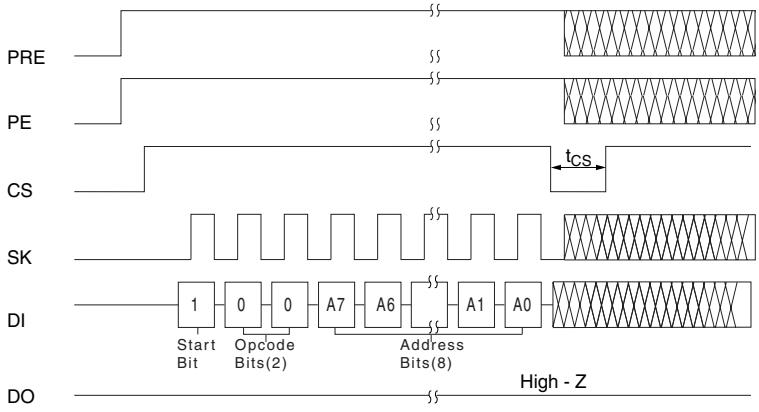
93CS56:
Address bits pattern -> 0-1-x-x-x-x-x-x; (x -> Don't Care, can be 0 or 1)
Data bits pattern -> User defined

PROTECT REGISTER READ CYCLE (PRREAD)



93CS56:
Address bits pattern -> x-x-x-x-x-x-x-x; (x -> Don't Care, can be 0 or 1)

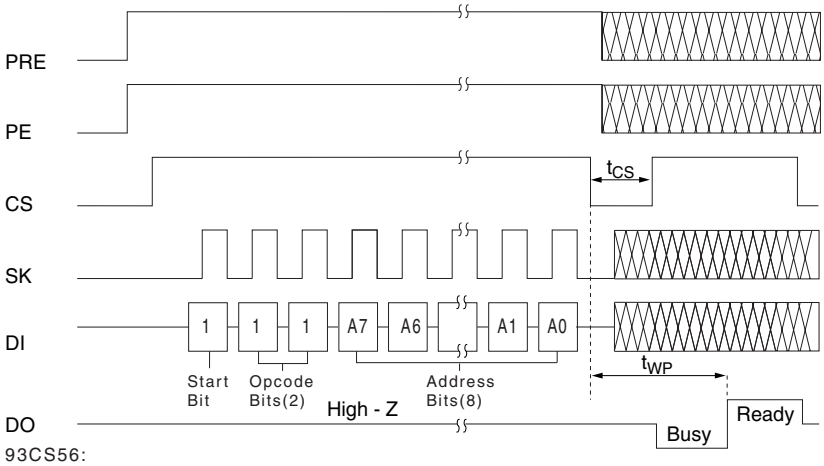
PROTECT REGISTER ENABLE CYCLE (PREN)



93CS56:
Address bits pattern -> 1-1-x-x-x-x-x-x; (x -> Don't Care, can be 0 or 1)

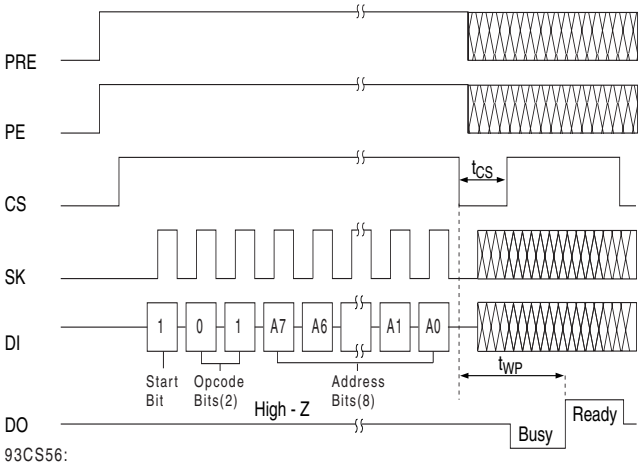
Timing Diagrams (Continued)

PROTECT REGISTER CLEAR CYCLE (PRCLEAR)



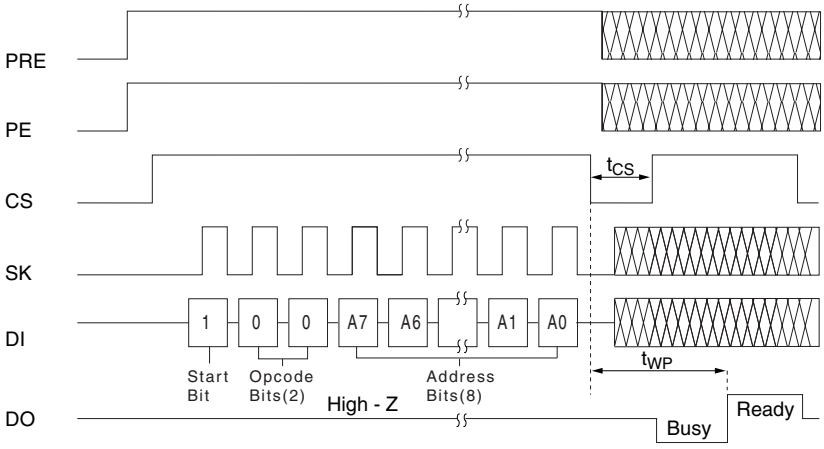
93CS56:
Address bits pattern -> 1-1-1-1-1-1-1-1

PROTECT REGISTER WRITE CYCLE (PRWRITE)



93CS56:
Address bits pattern -> x-A6-A5-A4-A3-A2-A1-A0; (x -> Don't Care, can be 0 or 1); (A6-A0 -> User defined)

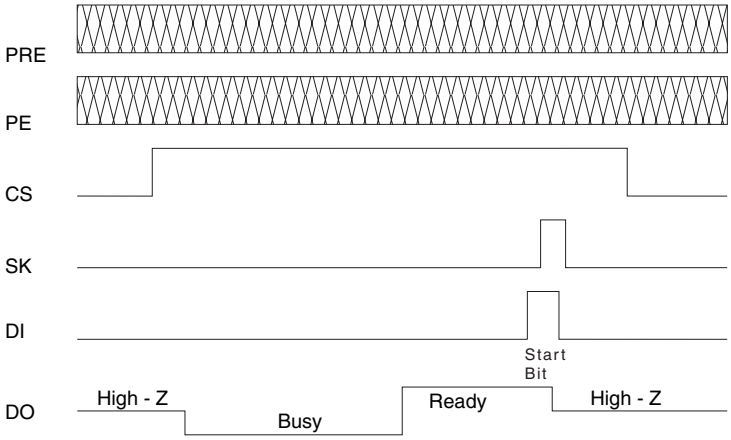
PROTECT REGISTER DISABLE CYCLE (PRDS)



93CS56:
Address bits pattern -> 0-0-0-0-0-0-0-0

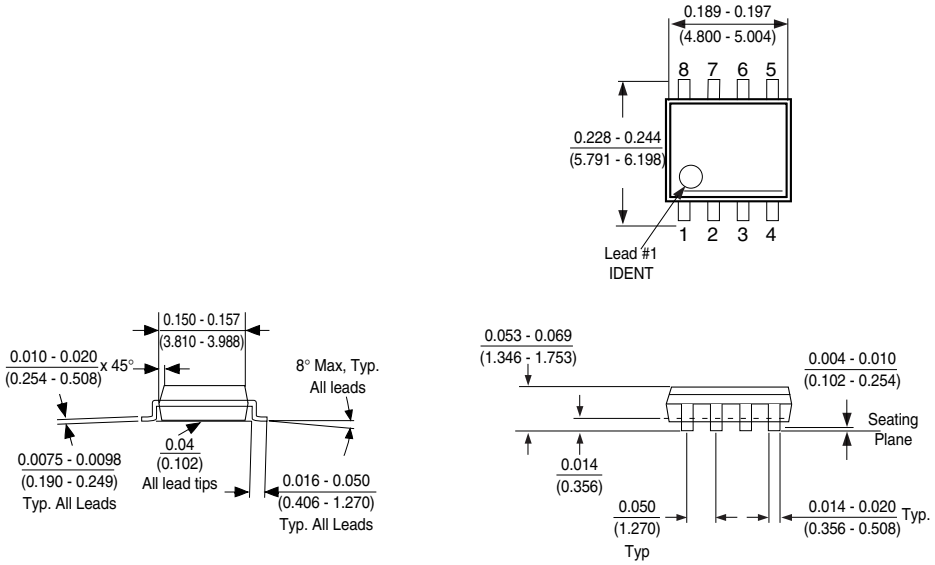
Timing Diagrams (Continued)

CLEARING READY STATUS



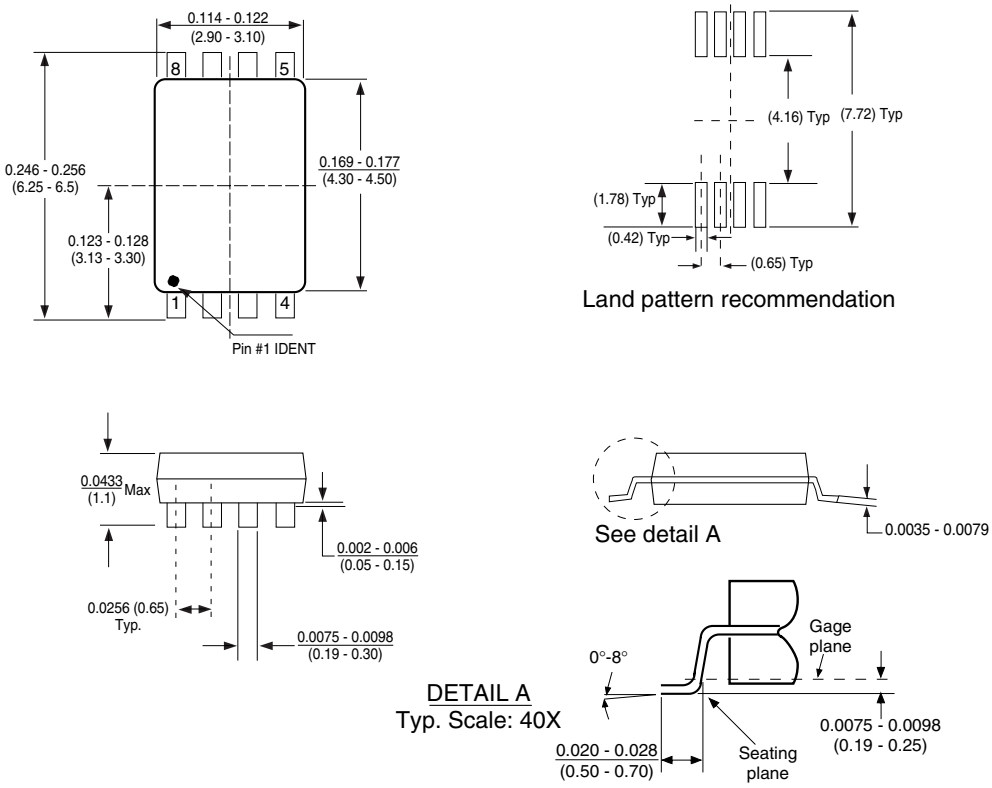
Note: This Start bit can also be part of a next instruction. Hence the cycle can be continued(instead of getting terminated, as shown) as if a new instruction is being issued.

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Package, Small Outline, 0.15 Wide, 8-Lead (M8)
Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted

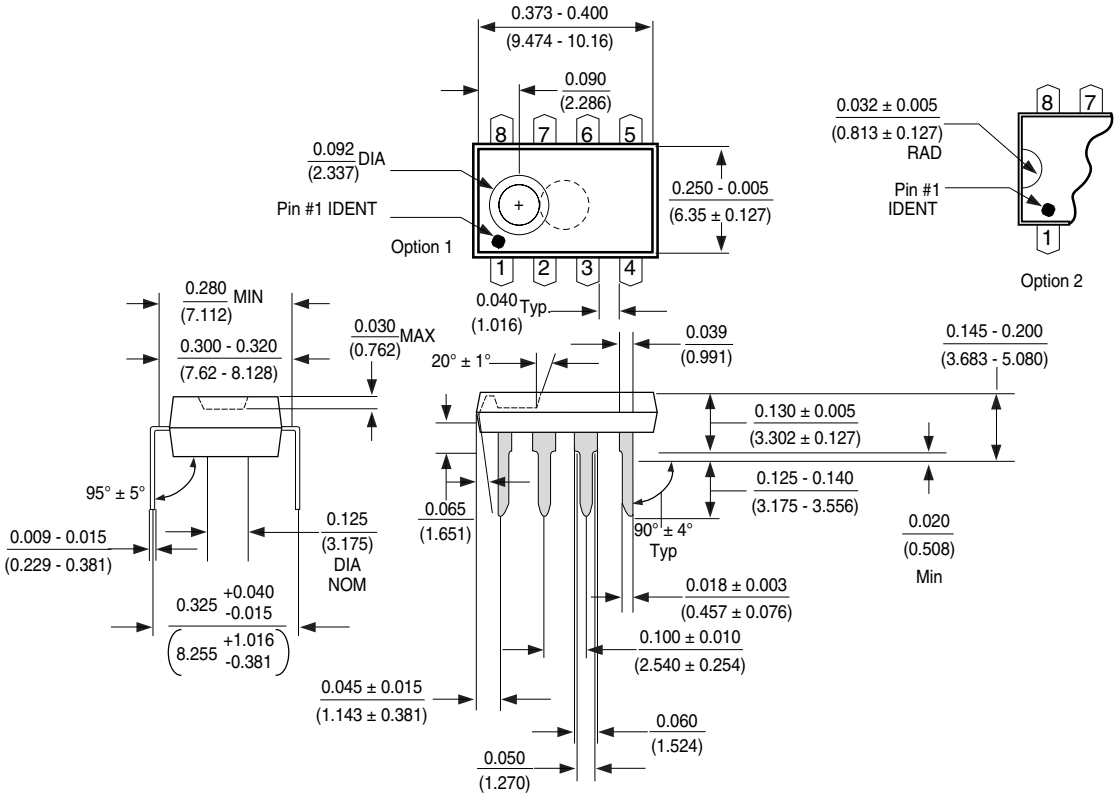


Notes: Unless otherwise specified

1. Reference JEDEC registration MO153. Variation AA. Dated 7/93

8-Pin Molded TSSOP, JEDEC (MT8)
Package Number MTC08

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Package Number N08E

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FAIRCHILD SEMICONDUCTOR™

February 2000

NM93CS66 (MICROWIRE™ Bus Interface) 4096-Bit Serial EEPROM with Data Protect and Sequential Read

General Description

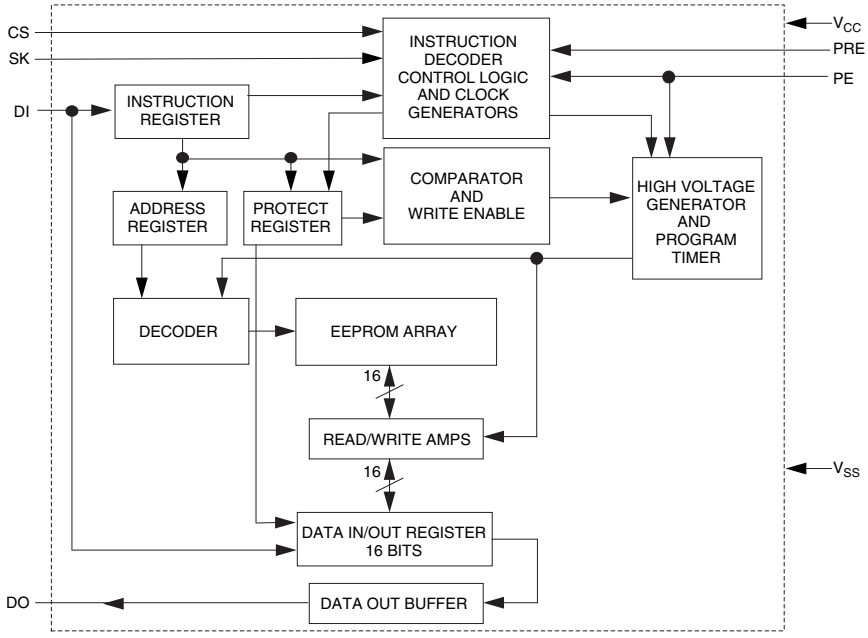
NM93CS66 is a 4096-bit CMOS non-volatile EEPROM organized as 256 x 16-bit array. This device features MICROWIRE interface which is a 4-wire serial bus with chipselect (CS), clock (SK), data input (DI) and data output (DO) signals. This interface is compatible to many of standard Microcontrollers and Microprocessors. NM93CS66 offers programmable write protection to the memory array using a special register called Protect Register. Selected memory locations can be protected against write by programming this Protect Register with the address of the first memory location to be protected (all locations greater than or equal to this first address are then protected from further change). Additionally, this address can be "permanently locked" into the device, making all future attempts to change data impossible. In addition this device features "sequential read", by which, entire memory can be read in one cycle instead of multiple single byte read cycles. There are 10 instructions implemented on the NM93CS66, 5 of which are for memory operations and the remaining 5 are for Protect Register operations. This device is fabricated using Fairchild Semiconductor floating-gate CMOS process for high reliability, high endurance and low power consumption.

"LZ" and "L" versions of NM93CS66 offer very low standby current making them suitable for low power applications. This device is offered in both SO and TSSOP packages for small space considerations.

Features

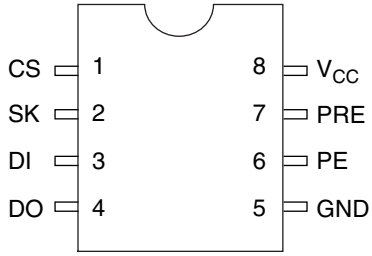
- Wide V_{CC} 2.7V - 5.5V
- Programmable write protection
- Sequential register read
- Typical active current of 200μA
  10μA standby current typical
  1μA standby current typical (L)
  0.1μA standby current typical (LZ)
- No Erase instruction required before Write instruction
- Self timed write cycle
- Device status during programming cycles
- 40 year data retention
- Endurance: 1,000,000 data changes
- Packages available: 8-pin SO, 8-pin DIP, 8-pin TSSOP

Functional Diagram



Connection Diagram

Dual-In-Line Package (N)
8–Pin SO (M8) and 8–Pin TSSOP (MT8)



Top View
Package Number
N08E, M08A and MTC08

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
V_{CC}	Power Supply

Ordering Information

NM 93 CS XX LZ E XXX

	Letter	Description
Package	N	8-pin DIP
	M8	8-pin SO
	MT8	8-pin TSSOP
Temp. Range	None	0 to 70°C
	V	-40 to +125°C
	E	-40 to +85°C
Voltage Operating Range	Blank	4.5V to 5.5V
	L	2.7V to 5.5V
	LZ	2.7V to 5.5V and <1µA Standby Current
Density	66	4096 bits
	C	CMOS
	CS	Data protect and sequential read
Interface	93	MICROWIRE
Fairchild Memory Prefix		

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to -0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93CS66	0°C to +70°C
NM93CS66E	-40°C to +85°C
NM93CS66V	-40°C to +125°C
Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 4.5V to 5.5V unless otherwise specified

Symbol	Parameter	Conditions	Min	Max	Units
I_{CCA}	Operating Current	CS = V_{IH}, SK=1.0 MHz		1	mA
I_{CCS}	Standby Current	CS = V_{IL}		50	µA
I_{IL} I_{OL}	Input Leakage Output Leakage	V_{IN} = 0V to V_{CC} (Note 2)		±-1	µA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage		-0.1 2	0.8 V_{CC} +1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage	I_{OL} = 2.1 mA I_{OH} = -400 µA	 2.4	0.4	V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage	I_{OL} = 10 µA I_{OH} = -10 µA	 V_{CC} - 0.2	0.2	V
f_{SK}	SK Clock Frequency	(Note 3)		1	MHz
t_{SKH}	SK High Time	0°C to +70°C -40°C to +125°C	250 300		ns
t_{SKL}	SK Low Time		250		ns
t_{SKS}	SK Setup Time		50		ns
t_{CS}	Minimum CS Low Time	(Note 4)	250		ns
t_{CSS}	CS Setup Time		100		ns
t_{PRES}	PRE Setup Time		50		ns
t_{DH}	DO Hold Time		70		ns
t_{PES}	PE Setup Time		50		ns
t_{DIS}	DI Setup Time		100		ns
t_{CSH}	CS Hold Time		0		ns
t_{PEH}	PE Hold Time		250		ns
t_{PREH}	PRE Hold Time		50		ns
t_{DIH}	DI Hold Time		20		ns
t_{PD}	Output Delay			500	ns
t_{SV}	CS to Status Valid			500	ns
t_{DF}	CS to DO in Hi-Z	CS = V_{IL}		100	ns
t_{WP}	Write Cycle Time			10	ms

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to -0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93CS66L/LZ	0°C to +70°C
NM93CS66LE/LZE	-40°C to +85°C
NM93CS66LV/LZV	-40°C to +125°C
Power Supply (V_{CC})	2.7V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 2.7V to 5.5V unless otherwise specified

Symbol	Parameter	Conditions	Min	Max	Units
I_{CCA}	Operating Current	CS = V_{IH}, SK=1.0 MHz		1	mA
I_{CCS}	Standby Current L LZ (2.7V to 4.5V)	CS = V_{IL}		 10 1	 µA µA
I_{IL} I_{OL}	Input Leakage Output Leakage	V_{IN} = 0V to V_{CC} (Note 2)		±1	µA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage		-0.1 0.8V_{CC}	0.15V_{CC} V_{CC} +1	V
V_{OL} V_{OH}	Output Low Voltage Output High Voltage	I_{OL} = 10µA I_{OH} = -10µA	 0.9V_{CC}	0.1V_{CC}	V
f_{SK}	SK Clock Frequency	(Note 3)	0	250	KHz
t_{SKH}	SK High Time		1		µs
t_{SKL}	SK Low Time		1		µs
t_{SKS}	SK Setup Time		0.2		µs
t_{CS}	Minimum CS Low Time	(Note 4)	1		µs
t_{CSS}	CS Setup Time		0.2		µs
t_{PRES}	PRE Setup Time		50		ns
t_{DH}	DO Hold Time		70		ns
t_{PES}	PE Setup Time		50		ns
t_{DIS}	DI Setup Time		0.4		µs
t_{CSH}	CS Hold Time		0		ns
t_{PEH}	PE Hold Time		250		ns
t_{PREH}	PRE Hold Time		50		ns
t_{DIH}	DI Hold Time		0.4		µs
t_{PD}	Output Delay			2	µs
t_{SV}	CS to Status Valid			1	µs
t_{DF}	CS to DO in Hi-Z	CS = V_{IL}		0.4	µs
t_{WP}	Write Cycle Time			15	ms

Capacitance T_A = 25°C, f = 1 MHz (Note 5)

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical leakage values are in the 20nA range.

Note 3: The shortest allowable SK clock period = $1/f_{SK}$ (as shown under the f_{SK} parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both t_{SKH} and t_{SKL} limits must be observed. Therefore, it is not allowable to set $1/f_{SK} = t_{SKHminimum} + t_{SKLminimum}$ for shorter SK cycle time operation.

Note 4: CS (Chip Select) must be brought low (to V_{IL}) for an interval of t_{CS} in order to reset all internal device registers (device reset) prior to beginning another opcode cycle. (This is shown in the opcode diagram on the following page.)

Note 5: This parameter is periodically sampled and not 100% tested.

AC Test Conditions

V_{CC} Range	V_{IL}/V_{IH} Input Levels	V_{IL}/V_{IH} Timing Level	V_{OL}/V_{OH} Timing Level	I_{OL}/I_{OH}
2.7V ≤ V_{CC} ≤ 5.5V (Extended Voltage Levels)	0.3V/1.8V	1.0V	0.8V/1.5V	±10µA
4.5V ≤ V_{CC} ≤ 5.5V (TTL Levels)	0.4V/2.4V	1.0V/2.0V	0.4V/2.4V	2.1mA/-0.4mA
Output Load: 1 TTL Gate (C_L = 100 pF)				

Pin Description

Chip Select (CS)

This is an active high input pin to NM93CS66 EEPROM (the device) and is generated by a master that is controlling the device. A high level on this pin selects the device and a low level deselects the device. All serial communications with the device is enabled only when this pin is held high. However this pin cannot be permanently tied high, as a rising edge on this signal is required to reset the internal state-machine to accept a new cycle and a falling edge to initiate an internal programming after a write cycle. All activity on the SK, DI and DO pins are ignored while CS is held low.

Serial Clock (SK)

This is an input pin to the device and is generated by the master that is controlling the device. This is a clock signal that synchronizes the communication between a master and the device. All input information (DI) to the device is latched on the rising edge of this clock input, while output data (DO) from the device is driven from the rising edge of this clock input. This pin is gated by CS signal.

Serial Input (DI)

This is an input pin to the device and is generated by the master that is controlling the device. The master transfers Input information (Start bit, Opcode bits, Array addresses and Data) serially via this pin into the device. This Input information is latched on the rising edge of the SCK. This pin is gated by CS signal.

Serial Output (DO)

This is an output pin from the device and is used to transfer Output data via this pin to the controlling master. Output data is serially shifted out on this pin from the rising edge of the SCK. This pin is active only when the device is selected.

Protect Register Enable (PRE)

This is an active high input pin to the device and is used to distinguish operations to memory array and operations to Protect Register. When this pin is held low, operations to the memory array are enabled. When this pin is held high, operations to the Protect Register are enabled. This pin operates in conjunction with PE pin. Refer Table1 for functional matrix of this pin for various operations.

Program Enable (PE)

This is an active high input pin to the device and is used to enable operations, that are write in nature, to the memory array and to the Protect register. When this pin is held high, operations that are "write" in nature are enabled. When this pin is held low, operations that are "write" in nature are disabled. This pin operates in conjunction with PRE pin. Refer Table1 for functional matrix of this pin for various operations.

Microwire Interface

A typical communication on the Microwire bus is made through the CS, SK, DI and DO signals. To facilitate various operations on the Memory array and on the Protect Register, a set of 10 instructions are implemented on NM93CS66. The format of each instruction is listed in Table 1.

Instruction

Each of the above 10 instructions is explained under individual instruction descriptions.

Start Bit

This is a 1-bit field and is the first bit that is clocked into the device when a Microwire cycle starts. This bit has to be "1" for a valid cycle to begin. Any number of preceding "0" can be clocked into the device before clocking a "1".

Opcode

This is a 2-bit field and should immediately follow the start bit. These two bits (along with PRE, PE signals and 2 MSB of address field) select a particular instruction to be executed.

Address Field

This is a 8-bit field and should immediately follow the Opcode bits. In NM93CS66, all 8 bits are used for address decoding during READ, WRITE and PRWRITE instructions.During all other instructions (with the exception of PRREAD), the MSB 2 bits are used to decode instruction (along with Opcode bits, PRE and PE signals).

Data Field

This is a 16-bit field and should immediately follow the Address bits. Only the WRITE and WRALL instructions require this field. D15 (MSB) is clocked first and D0 (LSB) is clocked last (both during writes as well as reads).

TABLE 1. Instruction set

Instruction	Start Bit	Opcode Field	Address Field								Data Field	PRE Pin	PE Pin
READ	1	10	A7	A6	A5	A4	A3	A2	A1	A0		0	X
WEN	1	00	1	1	X	X	X	X	X	X		0	1
WRITE	1	01	A7	A6	A5	A4	A3	A2	A1	A0	D15-D0	0	1
WRALL	1	00	0	1	X	X	X	X	X	X	D15-D0	0	1
WDS	1	00	0	0	X	X	X	X	X	X		0	X
PRREAD	1	10	X	X	X	X	X	X	X	X		1	X
PREN	1	00	1	1	X	X	X	X	X	X		1	1
PRCLEAR	1	11	1	1	1	1	1	1	1	1		1	1
PRWRITE	1	01	A7	A6	A5	A4	A3	A2	A1	A0		1	1
PRDS	1	00	0	0	0	0	0	0	0	0		1	1

Functional Description

A typical Microwire cycle starts by first selecting the device (bringing the CS signal high). Once the device is selected, a valid Start bit ("1") should be issued to properly recognize the cycle. Following this, the 2-bit opcode of appropriate instruction should be issued. After the opcode bits, the 8-bit address information should be issued. For certain instructions, some (or all) of these 8 bits are don't care values (can be "0" or "1"), but they should still be issued. Following the address information, depending on the instruction (WRITE and WRALL), 16-Bit data is issued. Otherwise, depending on the instruction (READ and PRREAD), the device starts to drive the output data on the DO line. Other instructions perform certain control functions and do not deal with data bits. The Microwire cycle ends when the CS signal is brought low. However during certain instructions, falling edge of the CS signal initiates an internal cycle (Programming), and the device remains busy till the completion of the internal cycle. Each of the 10 instructions is explained in detail in the following sections.

Memory Instructions

Following five instructions, READ, WEN, WRITE, WRALL and WDS are specific to operations intended for memory array. The PRE pin should be held low during these instructions.

1) Read and Sequential Read (READ)

READ instruction allows data to be read from a selected location in the memory array. Input information (Start bit, Opcode and Address) for this instruction should be issued as listed under Table1. Upon receiving a valid input information, decoding of the opcode and the address is made, followed by data transfer from the selected memory location into a 16-bit serial-out shift register. This 16-bit data is then shifted out on the DO pin. D15 bit (MSB) is shifted out first and D0 bit (LSB) is shifted out last. A dummy-bit (logical 0) precedes this 16-bit data output string. Output data changes are initiated on the rising edge of the SK clock. After reading the 16-bit data, the CS signal can be brought low to end the Read cycle. The PRE pin should be held low during this cycle. Refer *Read cycle diagram*.

This device also offers "sequential memory read" operation to allow reading of data from the additional memory locations instead of just one location. It is started in the same manner as normal read but the cycle is continued to read further data (instead of terminating after reading the first 16-bit data). After providing 16-bit data, the device automatically increments the address pointer to the next location and continues to provide the data from that location. Any number of locations can be read out in this manner, however, after reading out from the last location, the address pointer points back to the first location. If the cycle is continued further, data will be read from this first location onward. In this mode of read, the dummy-bit is present only when the very first data is read (like normal read cycle) and is not present on subsequent data reads. The PRE pin should be held low during this cycle. Refer *Sequential Read cycle diagram*.

2) Write Enable (WEN)

When V_{CC} is applied to the part, it "powers up" in the Write Disable (WDS) state. Therefore, all programming operations (for both memory array and Protect Register) must be preceded by a Write Enable (WEN) instruction. Once a Write Enable instruction is executed, programming remains enabled until a Write Disable (WDS) instruction is executed or V_{CC} is completely removed from the part. Input information (Start bit, Opcode and Address) for this WEN instruction should be issued as listed under Table1. The device becomes write-enabled at the end of this cycle when the CS signal is brought low. The PRE pin should be held low during this cycle. Execution of a READ instruction is independent of WEN instruction. Refer *Write Enable cycle diagram.*

3) Write (WRITE)

WRITE instruction allows write operation to a specified location in the memory with a specified data. This instruction is valid only when the following are true:

- Device is write-enabled (Refer WEN instruction)
- Address of the write location is not write-protected
- PE pin is held high during this cycle
- PRE pin should be held low during this cycle

Input information (Start bit, Opcode, Address and Data) for this WRITE instruction should be issued as listed under Table1. After inputting the last bit of data (D0 bit), CS signal must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. It takes t_{WP} time (Refer appropriate DC and AC Electrical Characteristics table) for the internal programming cycle to finish. During this time, the device remains busy and is not ready for another instruction.

The status of the internal programming cycle can be polled at any time by bringing the CS signal high again, after t_{CS} interval. When CS signal is high, the DO pin indicates the READY/BUSY status of the chip. DO = logical 0 indicates that the programming is still in progress. DO = logical 1 indicates that the programming is finished and the device is ready for another instruction. It is not required to provide the SK clock during this status polling. While the device is busy, it is recommended that no new instruction be issued. Refer *Write cycle diagram.*

It is also recommended to follow this instruction (after the device becomes READY) with a Write Disable (WDS) instruction to safeguard data against corruption due to spurious noise, inadvertent writes etc.

4) Write All (WRALL)

Write all (WRALL) instruction is similar to the Write instruction except that WRALL instruction will simultaneously program all memory locations with the data pattern specified in the instruction. This instruction is valid only when the following are true:

- Protect Register has been cleared (Refer PRCLEAR instruction)
- Device is write-enabled (Refer WEN instruction)
- PE pin is held high during this cycle
- PRE pin should be held low during this cycle

Input information (Start bit, Opcode, Address and Data) for this WRALL instruction should be issued as listed under Table1. After inputting the last bit of data (D0 bit), CS signal must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. It takes t_{WP} time (Refer appropriate DC and AC Electrical Characteristics table) for the internal programming cycle to finish. During this time, the device remains busy and is not ready for another instruction. Status of the internal programming can be polled as described under WRITE instruction description. While the device is busy, it is recommended that no new instruction be issued. Refer *Write All cycle diagram.*

5) Write Disable (WDS)

Write Disable (WDS) instruction disables all programming operations and is recommended to follow all programming operations. Executing this instruction after a valid write instruction would protect against accidental data disturb due to spurious noise, glitches, inadvertent writes etc. Input information (Start bit, Opcode and Address) for this WDS instruction should be issued as listed under Table1. The device becomes write-disabled at the end of this cycle when the CS signal is brought low. Execution of a READ instruction is independent of WDS instruction. Refer *Write Disable cycle diagram.*

Protect Register Instructions

Following five instructions, PRREAD, PREN, PRCLEAR, PRWRITE and PRDS are specific to operations intended for Protect Register. The PRE pin should be held high during these instructions.

1) Protect Register Read (PRREAD)

This instruction reads the content of the internal Protect Register. Content of this register is 8-bit wide and is the starting address of the "write-protected" section of the memory array. All memory locations greater than or equal to this address are write-protected. Input information (Start bit, Opcode and Address) for this PRREAD instruction should be issued as listed under Table 1. Upon receiving a valid input information, decoding of the opcode and the address is made, followed by data transfer (address information) from the Protect Register. This 8-bit data is then shifted out on the DO pin with the MSB first and the LSB last. Like the READ instruction a dummy-bit (logical 0) precedes this 8-bit data output string. Output data changes are initiated on the rising edge of the SK clock. After reading the 8-bit data, the CS signal can be brought low to end the PRREAD cycle. The PRE pin should be held high during this cycle. Refer *Protect Register Read cycle diagram.*

2) Protect Register Enable (PREN)

This instruction is required to enable PRCLEAR, PRWRITE and PRDS instructions and should be executed prior to executing PRCLEAR, PRWRITE and PRDS instructions. However, this PREN instruction is enabled (valid) only the following are true

- Device is write-enabled (Refer WEN instruction)
- PE pin is held high during this cycle
- PRE pin is held high during this cycle

Input information (Start bit, Opcode and Address) for this PREN instruction should be issued as listed under Table1. The Protect Register becomes enabled for PRCLEAR, PRWRITE and PRDS instructions at the end of this cycle when the CS signal is brought low. Note that this PREN instruction **must immediately precede** a PRCLEAR, PRWRITE or PRDS instruction. In other words, no other instruction should be executed between a PREN instruction and a PRCLEAR, PRWRITE or PRDS instruction. Refer *Protect Register Enable cycle diagram.*

3) Protect Register Clear (PRCLEAR)

This instruction clears the content of the Protect register and therefore enables write operations (WRITE or WRALL) to all memory locations. Executing this instruction will program the content of the Protect Register with a pattern of all 1s. However, in this case, WRITE operation to the last memory address (0x11111111) is still enabled. PRCLEAR instruction is enabled (valid) only when the following are true:

- PREN instruction was executed **immediately prior** to PRCLEAR instruction
- PE pin is held high during this cycle
- PRE pin is held high during this cycle

Input information (Start bit, Opcode and Address) for this PRCLEAR instruction should be issued as listed under Table1. After inputting the last bit of address (A0 bit), CS signal must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed clear cycle. It takes t_{WP} time (Refer appropriate DC and AC Electrical Characteristics table) for the internal clear cycle to finish. During this time, the device remains busy and is not ready for another instruction. Status of the internal programming can be polled as described under WRITE instruction description. While the device is busy, it is recommended that no new instruction be issued. Refer *Protect Register Clear cycle diagram.*

4) Protect Register Write (PRWRITE)

This instruction is used to write the starting address of the memory section to be write-protected into the Protect register. After the execution of PRWRITE instruction, all memory locations greater than or equal to this address are write-protected. PRWRITE instruction is enabled (valid) only the following are true:

- PRCLEAR instruction was executed first (to clear the Protect Register)
- PREN instruction was executed **immediately prior** to PRWRITE instruction
- PE pin is held high during this cycle
- PRE pin is held high during this cycle

Input information (Start bit, Opcode and Address) for this PRWRITE instruction should be issued as listed under Table1. After inputting the last bit of address (A0 bit), CS signal must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. It takes t_{WP} time (Refer appropriate DC and AC Electrical Characteristics table) for the internal programming cycle to finish. During this time, the device remains busy and is not ready for another instruction. Status of the internal programming can be polled as described under WRITE instruction description. While the device is busy, it is recommended that no new instruction be issued. Refer *Protect Register Write cycle diagram.*

5) Protect Register Disable (PRDS)

Unlike all other instructions, this instruction is a **one-time-only** instruction which when executed **permanently write-protects the Protect Register** and renders it unalterable in the future. This instruction is useful to safeguard vital data (typically read only data) in the memory against any possible corruption. PRDS instruction is enabled (valid) only the following are true:

- PREN instruction was executed **immediately prior** to PRDS instruction
- PE pin is held high during this cycle
- PRE pin is held high during this cycle

Input information (Start bit, Opcode and Address) for this PRDS instruction should be issued as listed under Table1. After inputting the last bit of address (A0 bit), CS signal must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. It takes t_{WP} time (Refer appropriate DC and AC Electrical Characteristics table) for the internal programming cycle to finish. During this time, the device remains busy and is not ready for another instruction. Status of the internal programming can be polled as described under WRITE instruction description. While the device is busy, it is recommended that no new instruction be issued. The Protect Register is permanently write-protected at the end of this cycle. Refer *Protect Register Disable cycle diagram.*

Clearing of Ready/Busy status

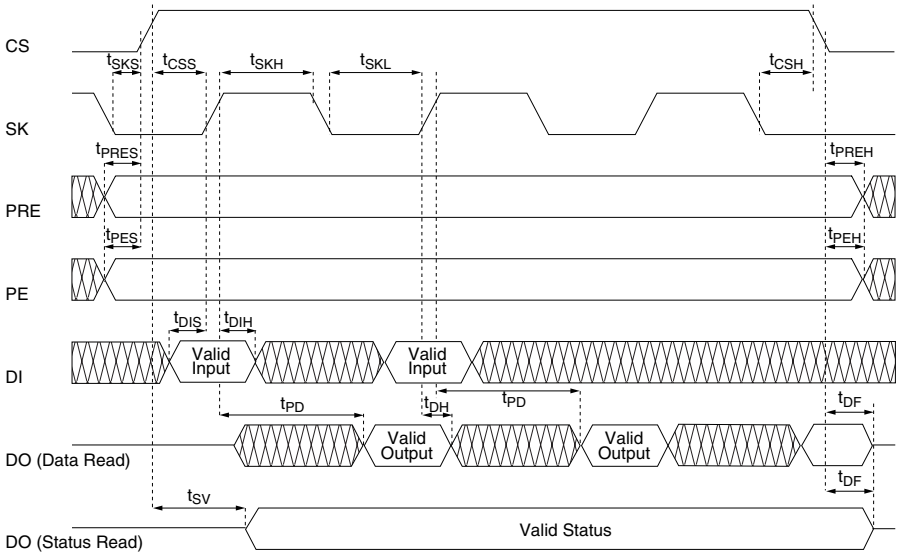
When programming is in progress, the Data-Out pin will display the programming status as either BUSY (low) or READY (high) when CS is brought high (DO output will be tri-stated when CS is low). To restate, during programming, the CS pin may be brought high and low any number of times to view the programming status without affecting the programming operation. Once programming is completed (Output in READY state), the output is 'cleared' (returned to normal tri-state condition) by clocking in a Start Bit. After the Start Bit is clocked in, the output will return to a tri-stated condition. When clocked in, this Start Bit can be the first bit in a command string, or CS can be brought low again to reset all internal circuits. Refer *Clearing Ready Status* diagram.

Related Document

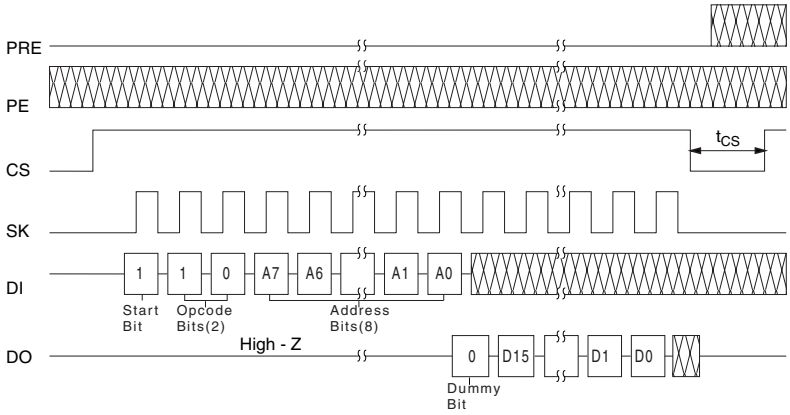
Application Note: AN758 - Using Fairchild's MICROWIRE™ EEPROM.

Timing Diagrams

SYNCHRONOUS DATA TIMING

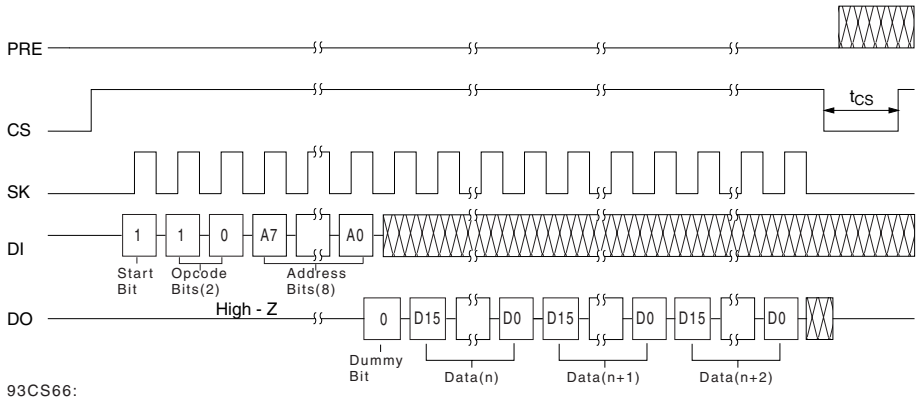


NORMAL READ CYCLE (READ)



93CS66:
Address bits pattern -> User defined

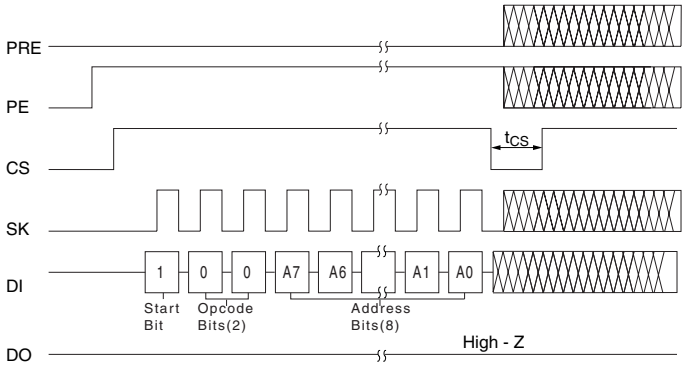
SEQUENTIAL READ CYCLE (PRE = 0; PE = X)



93CS66:
Address bits pattern -> User defined

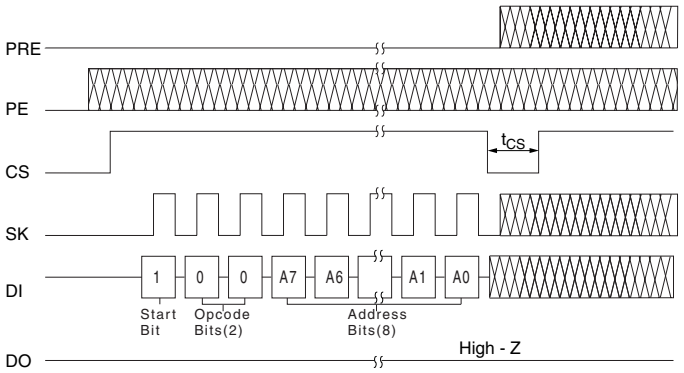
Timing Diagrams (Continued)

WRITE ENABLE CYCLE (WEN)



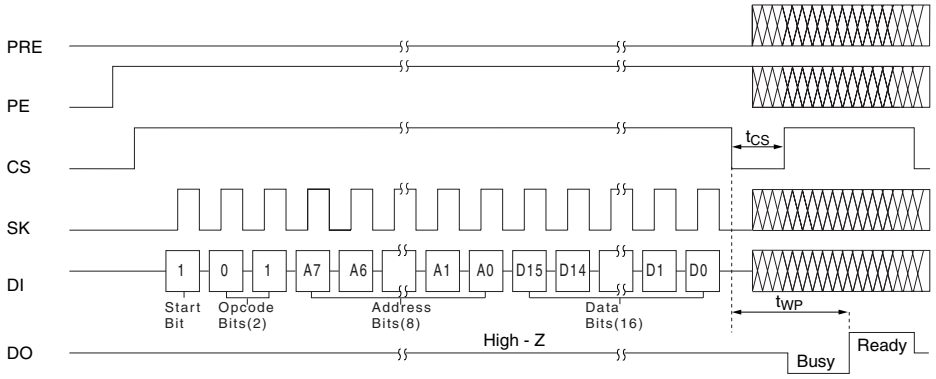
93CS66:
Address bits pattern -> 1-1-x-x-x-x-x-x; (x -> Don't Care, can be 0 or 1)

WRITE DISABLE CYCLE (WDS)



93CS66:
Address bits pattern -> 0-0-x-x-x-x-x-x; (x -> Don't Care, can be 0 or 1)

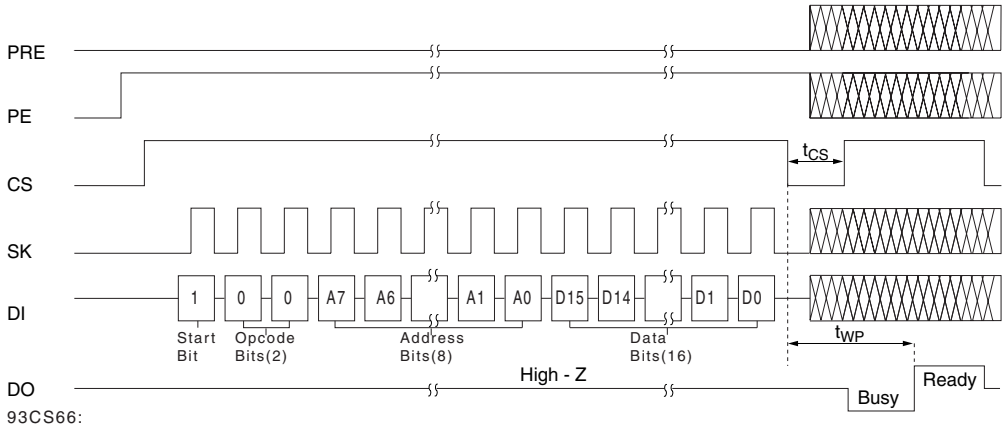
WRITE CYCLE (WRITE)



93CS66:
Address bits pattern -> User defined
Data bits pattern -> User defined

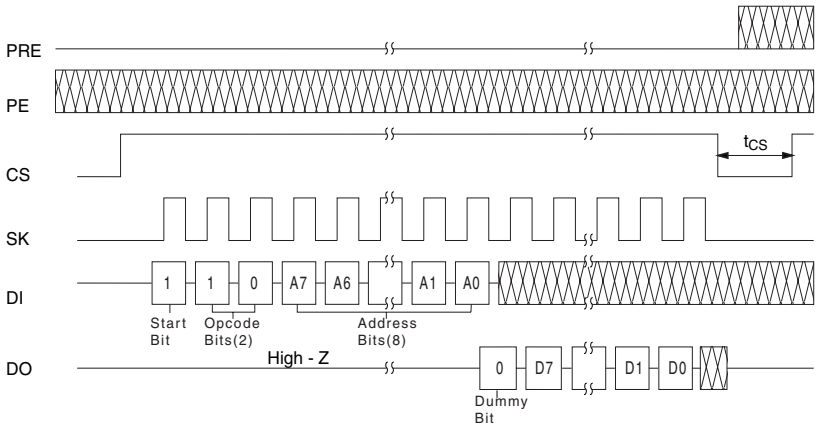
Timing Diagrams (Continued)

WRITE ALL CYCLE (WRALL)



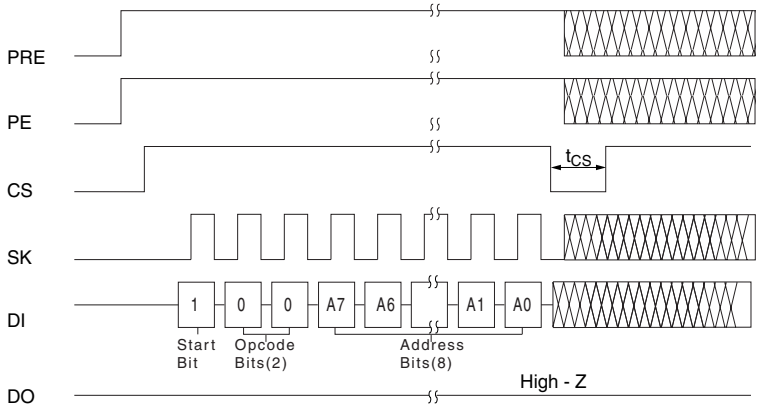
93CS66:
Address bits pattern -> 0-1-x-x-x-x-x-x; (x -> Don't Care, can be 0 or 1)
Data bits pattern -> User defined

PROTECT REGISTER READ CYCLE (PRREAD)



93CS66:
Address bits pattern -> x-x-x-x-x-x-x-x; (x -> Don't Care, can be 0 or 1)

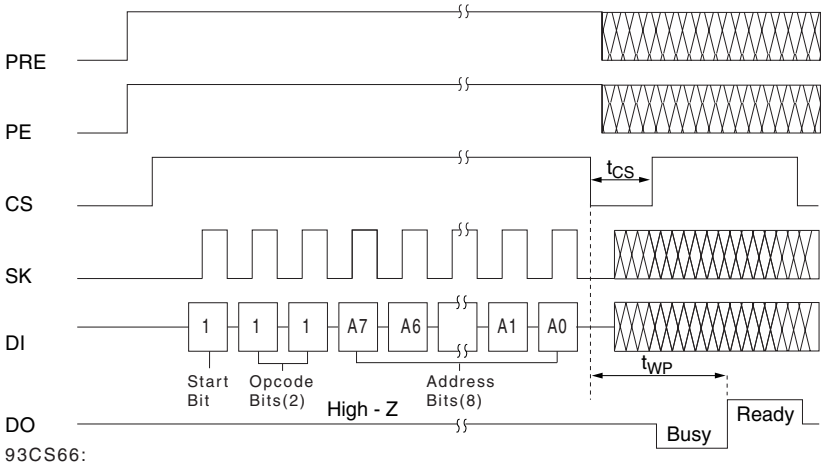
PROTECT REGISTER ENABLE CYCLE (PREN)



93CS66:
Address bits pattern -> 1-1-x-x-x-x-x-x; (x -> Don't Care, can be 0 or 1)

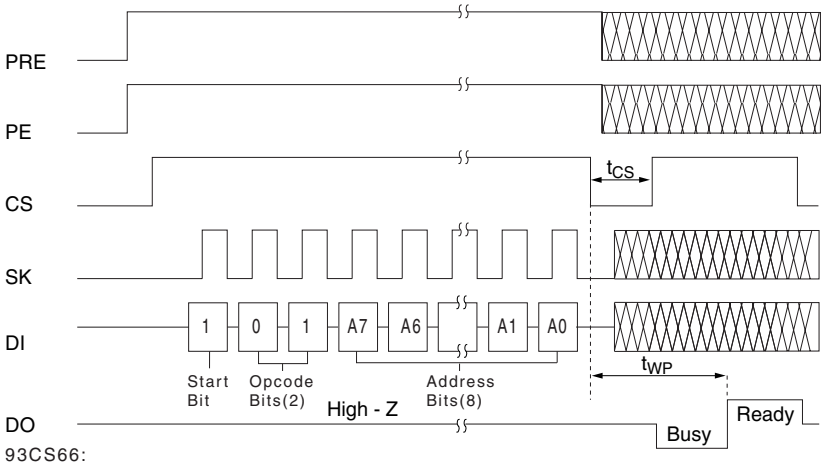
Timing Diagrams (Continued)

PROTECT REGISTER CLEAR CYCLE (PRCLEAR)



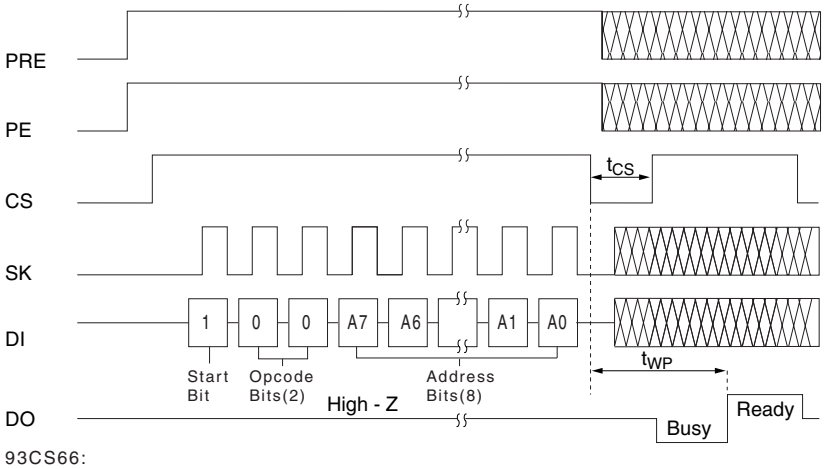
93CS66:
Address bits pattern -> 1-1-1-1-1-1-1-1

PROTECT REGISTER WRITE CYCLE (PRWRITE)



93CS66:
Address bits pattern -> User defined

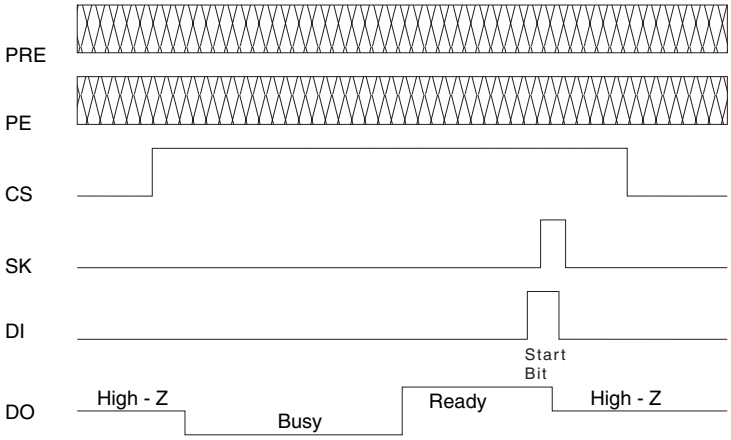
PROTECT REGISTER DISABLE CYCLE (PRDS)



93CS66:
Address bits pattern -> 0-0-0-0-0-0-0-0

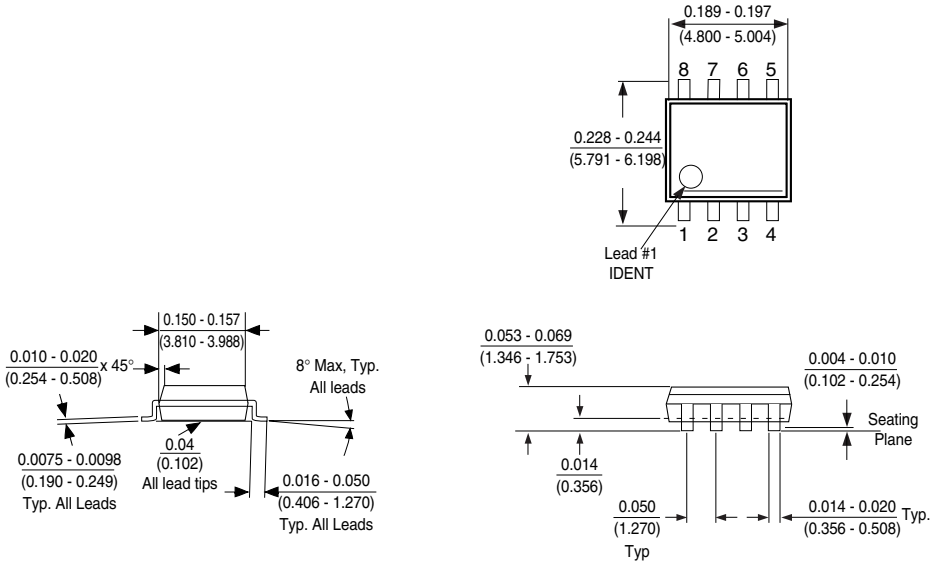
Timing Diagrams (Continued)

CLEARING READY STATUS



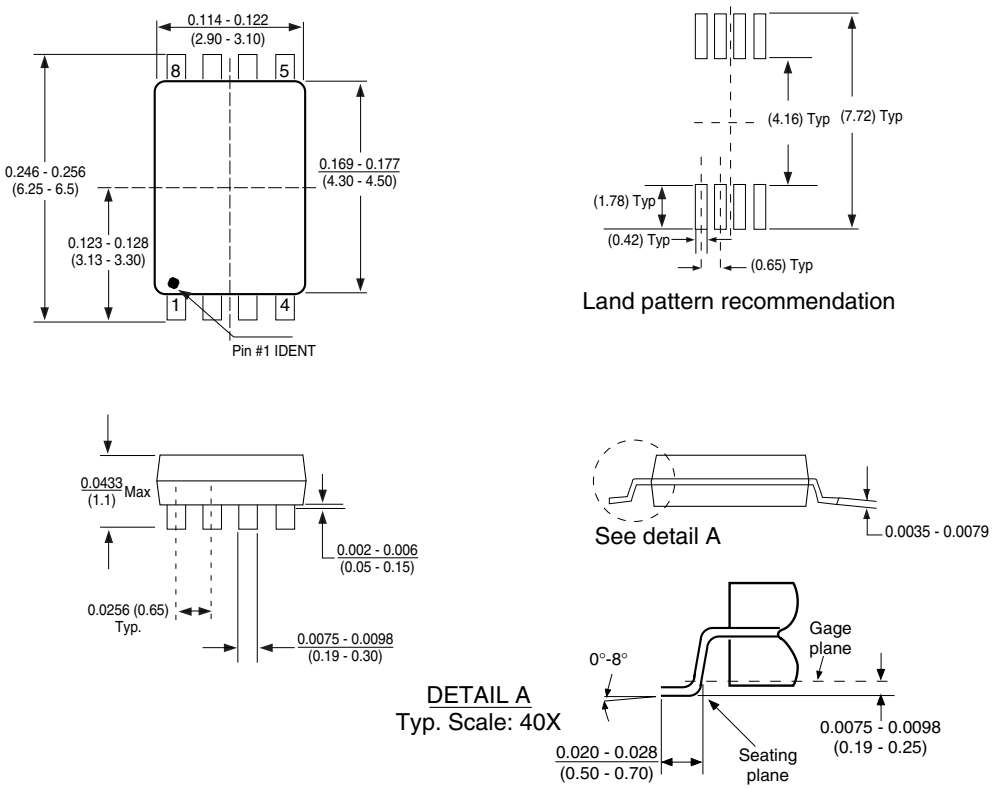
Note: This Start bit can also be part of a next instruction. Hence the cycle can be continued(instead of getting terminated, as shown) as if a new instruction is being issued.

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Package, Small Outline, 0.15 Wide, 8-Lead (M8)
Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted

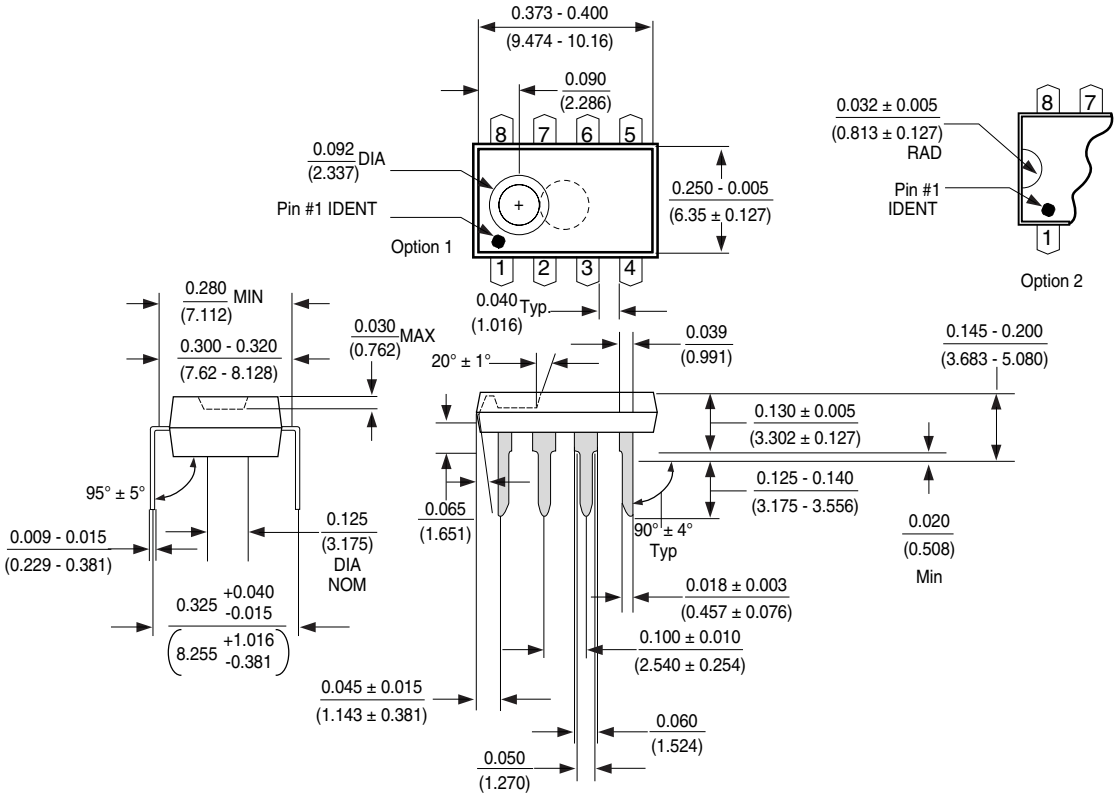


Notes: Unless otherwise specified

1. Reference JEDEC registration MO153. Variation AA. Dated 7/93

8-Pin Molded TSSOP, JEDEC (MT8)
Package Number MTC08

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Package Number N08E

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

July 1998

NM95HS01/NM95HS02
HiSeC™ High Security Rolling Code Generator

General Description

The NM95HS01/02 HiSeC Rolling Code Generator is a small footprint, monolithic CMOS device designed to provide a complete, low-cost, high security solution to the problem of generating encrypted signals for remote keyless entry (RKE) applications.

The NM95HS01/02 generates a fully encoded bit stream each time one of (up to) 4 switch inputs is activated. The patented* coding scheme utilizes 2 48 possible user-programmable coding combinations, and features high linear complexity and correlation immunity. High security is guaranteed by generating a unique (rolling) code for each transmission, and can be further enhanced by creating customized algorithms for individual customers. With this product, each key can be designed to be both unique and highly secure.

The NM95HS01/02 supports either an IR or RF signal transmitter, and can be clocked with either an RC clock (NM95HS01) or a crystal oscillator (NM95HS02). The device operates over a voltage range of 2.2V to 6.5V, and offers a low power standby mode (<1 μA) for battery applications. The product is available in both 8-pin and 14-pin SO packages with 2 or 4 key switch inputs that can be used for customer presets such as seat positions, and vehicle operating functions such as car door locking/unlocking.

Note: *Patents Pending

Features

- High security coding scheme with 2^{48} combinations
- High linear complexity and correlation immunity
- 2.2V to 6.5V operation
- Less than 1 μA standby current
- Full resynchronization capability
- Unique customized algorithm option
- 13 bytes on-chip non-volatile configuration memory
- RC or XTAL clock options for to 4.1 MHz operation
- Supports both IR and RF signal transmission
- Selection of bit coding and transmission frame formats
- Space saving narrow body SO8 or SO14 packages
- Up to 4 key switch inputs on SO14 package

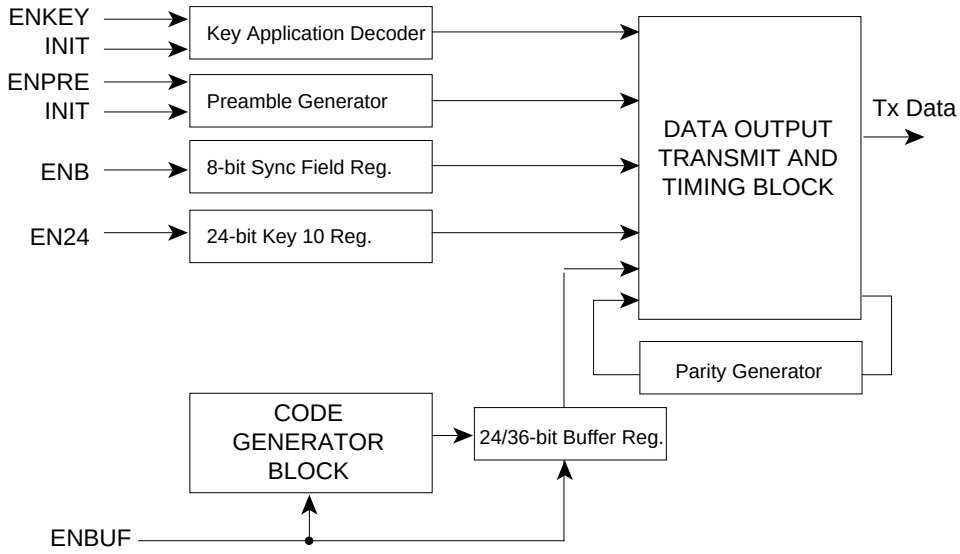
Applications

- Remote Keyless Entry (RKE) applications
- Burglar alarms/garage door openers
- Individualized recognition/transmission systems
- Personalized consumer automotive applications

Relevant Documents

- Designing and Programming a Complete HiSeC™ -based RKE System: AN-985

Functional Block Diagram



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Note: Signals shown are internal logic signals.

FIGURE 1.

General Characteristics

The NM95HS01/02HiSeC Generator was developed to meet existing standards for rolling code-based security systems.

Theft prevention systems typically involve user identification and transmission of information at various distances from the vehicle. These Remote Keyless Entry (RKE) systems are generally implemented with IR transmitters for short distances, or RF transmitters for longer distances. RF transmission has become state of the art; however the longer distances involved require a much higher degree of security, since the possibility of signal interception is greatly increased.

These applications are ideally served by the NM95HS01/02. This generator is a small footprint, low current solution that supports both IR and RF transmission. The device is available in an 8-pin SO package with 2 key switch inputs, or a 14-pin SO package with 4 key switch inputs.

The proprietary coding scheme used generates a rolling code based on 2 48 possible user combinations, and ensures a high level of coding security for any RKE application. The NM95HS01 can be clocked with an RC circuit, while the NM95HS02 can be clocked with a crystal oscillator.

General Device Operation

The Functional Block Diagram (Figure 1) shows the internal elements of the code generating logic and program registers.

The NM95HS01/02 HiSeC Generator achieves its high security level by combining the contents of several dynamic data registers in a non-linear manner to generate an encoded output. Data in the registers is comprised of a mixture of user programmable data, factory programmable data, and randomized data. This inherently random and separate data is encrypted by clocking it through a non-linear logic block, and feeding part of the output back to produce a final coded output with a high degree of linear complexity and correlation immunity.

The NM95HS01/02 incorporates 13 bytes of non-volatile EEPROM memory which can be used to configure the device registers. This memory is accessible to the user, and can be configured to the desired configuration, then write-disabled to prevent tampering.

User programmable data includes 24 bits of the code block, a 24-bit key ID register, and an 8-bit sync field register.

The 24-bit key ID register can be used to configure a large number of unique keys, each of which will produce a unique encoded output bit stream. The 24 bits in the code generator block are mixed with coded data.

The output of this block is then fed into the 24-/36-bit buffer register, where the 40 bits are recombined to produce a 24-or 36-bit output (a user option). The 8-bit sync field register can be configured by the user to provide a pattern to facilitate synchronization between the transmitter and receiver.

The details of the code block are available to customers, and exclusive algorithms are available and under contract with Fairchild. Call your local sales office for details.

The HiSeC Generator is shipped with a standard algorithm as a standard product, with the configuration shown.

Figure 2 shows a general operational block diagram of the NM95HS01/02 HiSeC Generator. The 4 key switch inputs shown use internal pull-up resistors, and are suitable for normally open, single pole input switches connected to ground. The inputs are buffered by debounce logic which repeatedly polls the inputs to determine if a key switch has been asserted. If any key switch input is seen as low for four continuous 10 ms samples, its associated output is set high, the HiSeC control logic is activated, and a security code is generated and transmitted.

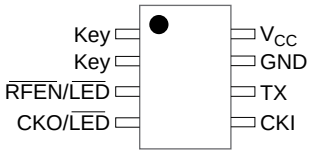
The timer block is used to set the key debounce time and the IR or RF clock times. These clock times are used as the time base for the chosen bit coding format. The timer block is also used to generate the interframe pause time, and the timeout delay, if these are enabled. These parameters are configured by the user in the 13-byte on-chip EEPROM array.

The NM95HS01 version of the device uses an RC network to clock the CKI input pin. The CKO/LED pin is not required for clocking, but may be used for a visual indicator LED. If the NM95HS02 crystal oscillator version is used, the device is clocked using both the CKI and CKO pins. If an LED is used with this device, it may be grounded through the RFEN /LED pin. Either the CKO/LED or the RFEN/LED output pins can provide the sink current needed to drive an indicator LED. The RFEN pin is active low during signal transmission, and is used to provide power to the RF circuit only during transmission to increase battery life.

The transmit output (TX) pin is a configurable logic level output, and is used to transmit the encoded bit stream. An on-chip power-on reset circuit is used to initialize the device during power-up.

Connection Diagrams

8–Pin SO Package (M8)



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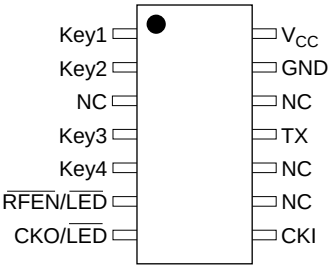
Top View
See Package Number
M08A (M8) or N08E (N)

14-Pin SO Package (M14) and
14-Pin Dual-In-Line Package (N14)
14-Pin TSSOP Package (MT14)



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Top View
See Package Number
M14A (M), MTC14 (MT14) N14A (N14)

Pin Names

Pin	Description
KEYn	Key Input
$\overline{\text{RFEN}}/\overline{\text{LED}}$	RF Enable/LED
CKO/$\overline{\text{LED}}$	XTAL Clock/LED
TX	Data Transmit
CKI	RC Clock Input
GND	Ground
V_{CC}	Supply Voltage

Ordering Information

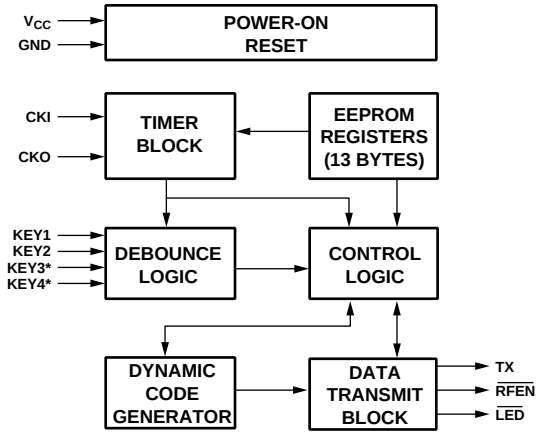
Commercial Temperature Range (0°C to +70°C)

Order Number
NM95HS01M8/NM95HS02M8
NM95HS01N/NM95HS02N
NM95HS01M/NM95HS02M
NM95HS01MT14/NM95HS02MT14
NM95HS01N14/NM95HS02N14

Extended Temperature Range (-40°C to +85°C)

Order Number
NM95HS01EM8/NM95HS02EM8
NM95HS01EN/NM95HS02EN
NM95HS01EM/NM95HS02EM
NM95HS01EN14/NM95HS02EN14

Ordering Information (Continued)



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***Note:** Keys 3 and 4 available in 14-pin packages.

FIGURE 2. Operational Block Diagram of the NM95HS01/02 HiSeC Generator

General Transmitter Circuit Configurations

Figure 3 shows several typical circuit configurations for a HiSeC based RKE system transmitter. Note that all circuits require few external components beyond a battery and transmitter stage. IR and RF bit timing may be optimized through the timer block settings in the EEPR0M array, which allows flexibility in selecting the smallest and least expensive clock components in the chosen design range.

The first two circuits are examples of RF transmitter applications, with both RC and crystal (XTAL) oscillator clocks; the third circuit is an example of an IR transmitter application. Two circuits are configured for an LED. Note that the LED pin refers to a visual indicator LED, and not the IR LED which might be used in an IR transmitter circuit.

The LEDSEL bit in the EEPROM array determines whether the RFEN/LED or CKO/LED pins are dedicated to the LED for a particular circuit configuration. LED pin select options are detailed in Table 1.

Design considerations for selecting and optimizing clock component values are detailed in the Generator Clock Design Parameters section.

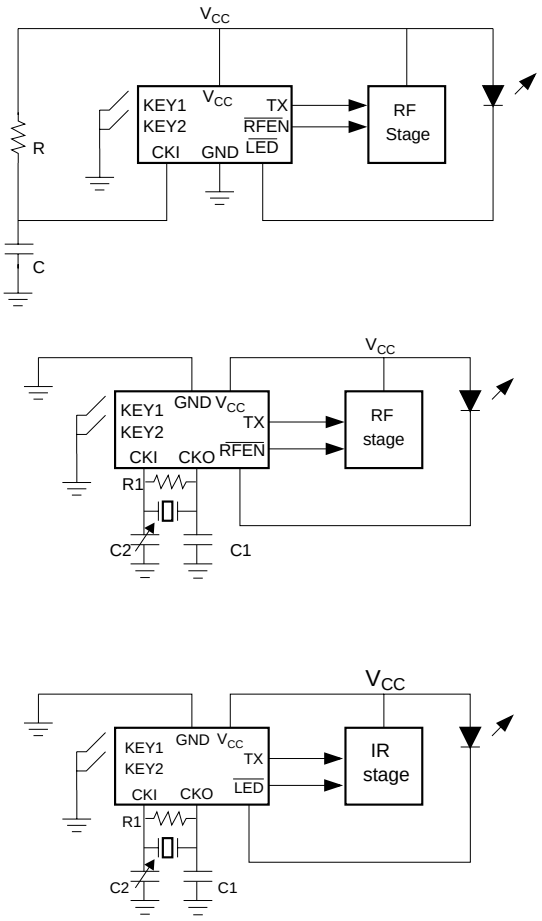

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FIGURE 3. Typical Transmitter Circuit Configurations

TABLE 1. $\overline{\text{LED}}$ Pin Select Options

Clock	LEDSEL	$\overline{\text{RFEN}}$/$\overline{\text{LED}}$	CKO/$\overline{\text{LED}}$	Function
RC	X	$\overline{\text{RFEN}}$	$\overline{\text{LED}}$	RF Mode with LED
XTAL	0	$\overline{\text{LED}}$	CKO	RF Mode w/o LED
XTAL	1	$\overline{\text{RFEN}}$	CKO	IR mode with LED

Either the LED or RFEN outputs of the NM95HS01/02 can be used to indicate device transmission.
The LED output is active during a pause, whereas the RFEN output is active during frame transmission.
The IR Drive Current is 10 mA so an amplifier stage may be needed.

Bit Coding Formats

The NM95HS01/02 HiSeC Generator supports eleven-bit coding formats which may be used for IR and RF transmission. Seven-bit formats are available for RF applications, and four are available for IR applications. One-bit format is reserved for future use.

Bit coding formats are selected by configuring four bits in the EEPROM array: IRSEL, PRSEL2, PRSEL1 and PRSEL0. Table II shows the possible bit coding options available.

Each bit coding format has a distinction which may be advantageous for a particular application. RF bit coding format 0 is the simplest bit coding scheme, and data may be easily recovered from a transmission by exclusive OR-ing the data and clock stream. Both RF bit coding formats 0 and 2 have a DC level that is independent of the data.

RF format 4, and the IR modes operate with a constant transmission energy per message, and RF coding formats 1, 3, 5 and 7 are pulse-width modulated (PWM) formats which are relatively easy to decode. RF coding format 7 has a low duty cycle.

Bit Coding Formats (Continued)

The IR bit coding formats are modulated versions of RF coding format 4, and are all suitable for IR applications. The duty cycle and number of pulses are variable among these four to allow the user to fine tune the IR circuit power curve.

IR bit coding formats all follow the same general pattern. In this mode, a logic "1" is always two periods long, and a "0" is always three periods long. This may be an important consideration when considering preamble and sync timing.

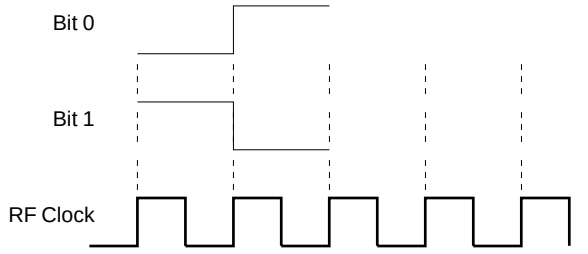
Waveform diagrams for all available RF and IR bit transmission coding formats are shown below.

TABLE 2. Transmission Bit Coding Options

IRSEL	PRSEL2	PRSEL1	PRSEL0	Function
0	0	0	0	RF Bit Coding Format 0
0	0	0	1	RF Bit Coding Format 1
0	0	1	0	RF Bit Coding Format 2
0	0	1	1	RF Bit Coding Format 3
0	1	0	0	RF Bit Coding Format 4
0	1	0	1	RF Bit Coding Format 5
0	1	1	0	Reserved
0	1	1	1	RF Bit Coding Format 7
1	0	0	0	IR Bit Coding Format 1
1	0	0	1	IR Bit Coding Format 2
1	0	1	0	IR Bit Coding Format 3
1	0	1	1	IR Bit Coding Format 4
1	1	X	X	Reserved

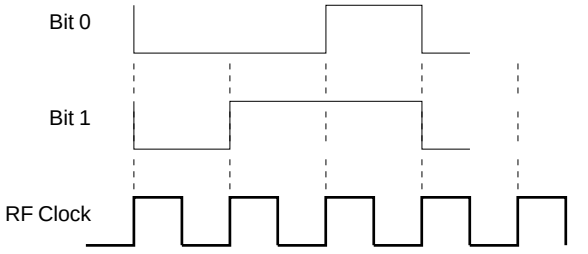
Bit Transmission Coding Formats

RF Bit Coding Format 0 (Manchester Code)



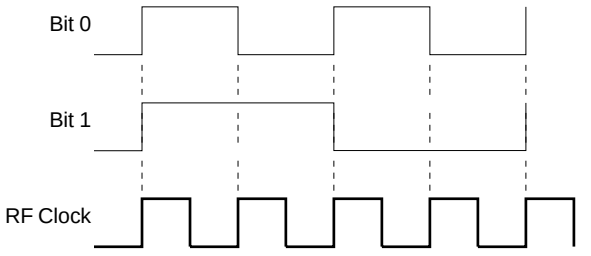
DS012302-6

RF Bit Coding Format 1 (33%/66% — End High)



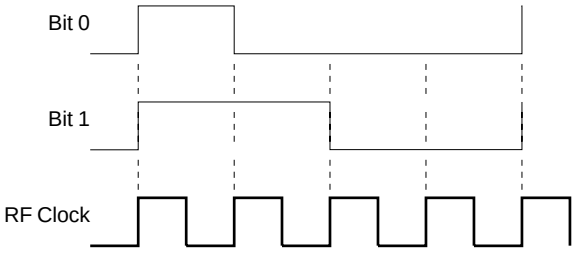
DS012302-7

RF Bit Coding Format 2 (50% Duty Cycle)



DS012302-8

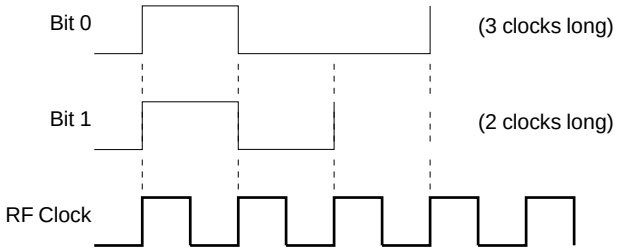
RF Bit Coding Format 3 (25%/50% — Start High)



DS012302-9

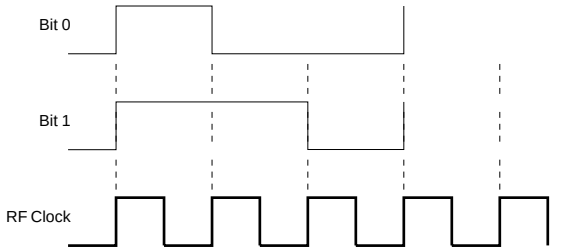
Bit Transmission Coding Formats (Continued)

RF Bit Coding Format 4 (IR Style)



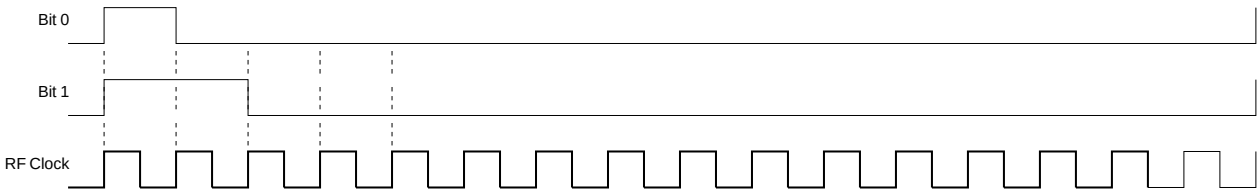
DS012302-10

RF Bit Coding Format 5 (33%/66% — Start High)



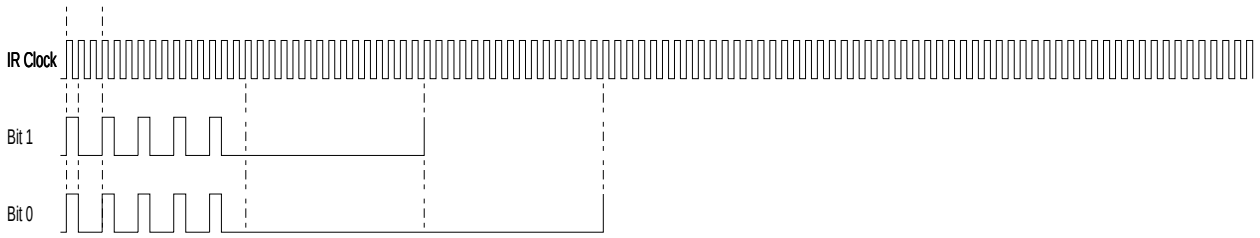
DS012302-11

RF Bit Coding Format 7 (Low Duty Cycle — 1:16/2:16)



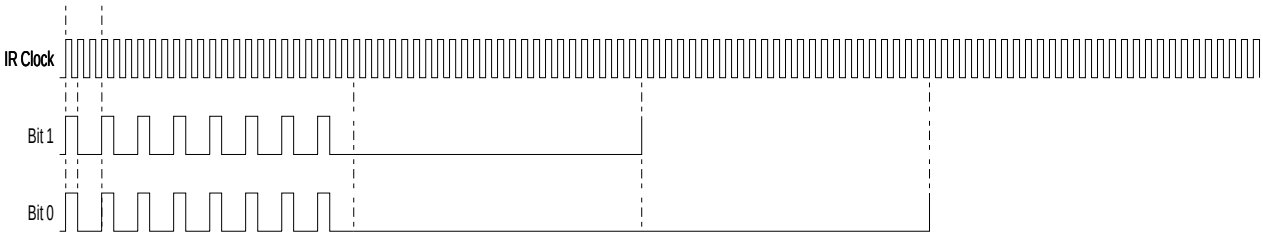
DS012302-12

IR Bit Coding Format 1 (5 Pulses — 33% Duty Cycle)



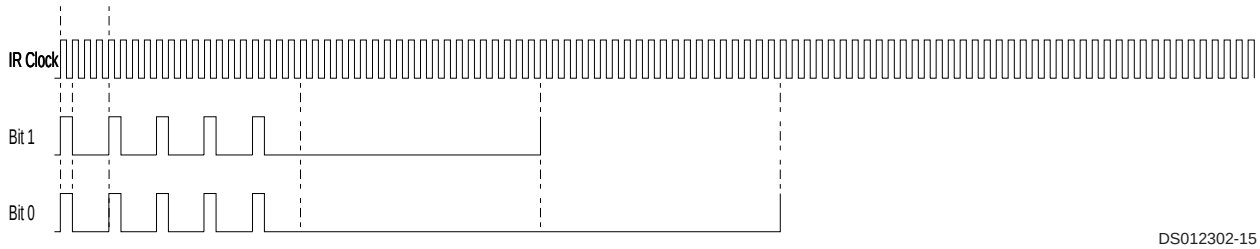
DS012302-13

IR Bit Coding Format 2 (8 Pulses — 33% Duty Cycle)



DS012302-14

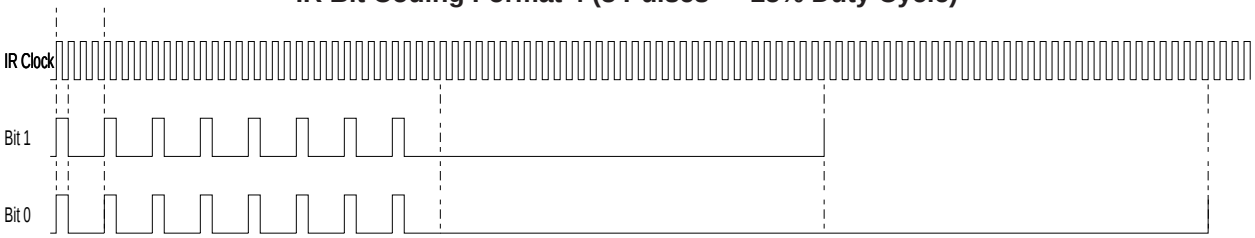
IR Bit Coding Format 3 (5 Pulses — 25% Duty Cycle)



DS012302-15

Bit Transmission Coding Formats (Continued)

IR Bit Coding Format 4 (8 Pulses — 25% Duty Cycle)



DS012302-16

Programmable Signal Output Polarity

The transmit (TX) output pin signal polarity and quiescent state output is controlled by the TxPol bit, which may be configured in EEPR0M. If TxPol = 0, the TX output pin will be at a logic low when no frame is transmitted, or when a “0” appears as data in a frame. Conversely, if TxPol = 1, the TX output pin will be at a logic high when no frame is transmitted, or when a “1” appears as data in a frame.

This option allows the designer to choose between a configuration where a logic “1” represents power transmission (for example, when an RF stage is activated by driving the base of an NPN transistor), and a configuration where a logic “0” represents power transmission (for example, when an IR LED is connected between VCC and the TX output).

Data Frames

The NM95HS01/02 HiSeC Generator transmits the encrypted data it generates as data frames. These frames are transmitted through an IR or RF transmitter stage using the bit coding format selected.

The NM95HS01/02 transmits two types of data frames: a normal data frame, and a synchronization (sync) frame. The format of each frame is similar, but there are slight differences to suit the purposes of each. Normal data frames are used to transmit encoded data in general operation. Sync frames are used to synchronize (or initialize) the HiSeC to its decoder.

Data frames are comprised of a number of different fields. Each field occupies a fixed position in the data frame, and serves a specific purpose. Most data fields are user-configurable to some extent. The user may enable/disable the presence of a field, control its length, or modify its format. The user also has several options available to tailor the data frame transmission format, such as pause time between frames, and time-out time. Options are configured by programming the on-chip EEPR0M array. The content and format of each of the fields is discussed below.

NORMAL DATA FRAME

The NM95HS01/02 HiSeC Generator transmits normal data frames in general operating mode. Frame transmission begins each time a key switch is asserted, and continues as long as the key is held down. The device has an option to terminate transmitting data frames, and go into halt mode, if a key is held down for more than 80 seconds (if the TIMEOUTEN feature has been enabled).

The normal data frame format contains both dynamic code and key application data (in the data field). Since the length of several fields is adjustable, there are several possibilities for the length of the data frame. The shortest possible normal data frame is 29 bits, and the longest possible normal data frame is 92 bits. 24 bits of dynamic code, 4 bits of key application data, and 1 stop bit are always present.

The composition of a normal data frame is shown in Figure 4.

SYNC FRAME

The NM95HS01/02 HiSeC Generator transmits sync frames only in sync mode so that it can synchronize itself with its decoder. This mode occurs only during initialization of the device, or after holding a key down for more than 10 seconds (if the AutoResync feature has been enabled).

The sync frame format contains both start code and a fixed 4-bit sync code of 0000. This sync code replaces the key application data in the data field, and is used to confirm HiSeC sync mode to the decoder.

Sync mode is built into the generator to allow resynchronization of the device under certain conditions as a convenience to the end user. If the designer wishes to preclude any possible resynchronization, the presence of the sync code allows the decoder to detect any synchronization attempt.

Since the length of several fields is adjustable, there are several possibilities for the length of a sync frame. The shortest possible sync frame is 45 bits, and the longest possible sync frame is 96 bits. 40 bits of start code, 4 bits of sync code, and 1 stop bit are always present.

The composition of a sync frame is shown in Figure 5.

Data Frames (Continued)

0/11 bits	0/8 bits	0/20/24 bits	4 bits	24/36 bits	0/8 bits	1 bit
Preamble	**Sync Field**	**Key ID Field**	**Data Field**	**Dynamic Code**	**Parity Field**	**Stop Bit**

FIGURE 4. Normal Data Frame Configuration

0/11 bits	0/8 bits	0/20/24 bits	4 bits	40 bits	0/8 bits	1 bit
Preamble	**Sync Field**	**Key ID Field**	**Sync Code**	**Start Code**	**Parity Field**	**Stop Bit**

FIGURE 5. Sync Frame Configuration

Data Frame Fields

Data frames are comprised of a number of data fields. Each field occupies a fixed position in the data frame, and serves a specific purpose. Most data fields are user-configurable by programming the on-chip EEPROM array. The content and format of each field is discussed below, as well as the EEPROM options available.

All data frame fields are transmitted Most Significant Bit first.

THE PREAMBLE

The user has the option of allowing a preamble to be tranmitted as the first frame of either a normal data frame or a sync frame. This option is enabled/disabled by setting the PreamblePresent bit in the EEPROM array. PreamblePresent = 0 means no preamble is transmitted. PreamblePresent = 1 means an 11-bit preamble is transmitted as described below.

The purpose of the preamble is to generate a relatively long, clearly recognizable bit pattern to give the decoder a chance to “wake up” and configure its logic circuits and registers. This allows the receiver to be placed in a standby mode to conserve power for battery applications.

The preamble is only transmitted once as the first frame of a data transmission, regardless of how long the key is held down, although the remaining frames of the data transmission (including any inter-frame pauses) will continue to repeat as long as the key remains depressed.

The preamble has a fixed format of two bit times at system logic high, then one-bit time at system logic low, then eight zeroes using the user-selected bit coding format. This arrangement is clearly shown in Figure 6for several bit coding formats.

If desired, a preamble may be isolated from the frame by eight-bit times at logic low during a frame transmission. This can be achieved by enabling the sync field in NRZ mode with the byte 0h.

SYNC FIELD

If enabled, the sync field is transmitted in every normal data frame or sync frame to provide a bit timing reference for the rest of the frame. This allows the decoder to determine the proper bit coding format the generator is using, and to synchronize to it.

The sync field option is set with the SyncPresent bit in the EEPROM array. If SyncPresent = 0, no sync field is sent. If SyncPresent = 1 an 8-bit sync field is included in the data transmission. This 8-bit field is transmitted Most Significant Bit first.

The sync field data is programmable, and can be encoded with any user-selected bit coding format, or with an NRZ (unencoded binary) bit format. The option to select between a user bit coding format and NRZ format is set by configuring the SyncType bit in the EEPROM array. If SyncType = 0, sync field data is sent according to the user-selected IR or RF bit coding format. If SyncType = 1, the information is sent in NRZ format with the bit length determined by the chosen IR or RF bit coding format.

For NRZ bit coding, both high and low bit times are the same as the IR or RF bit coding time. For bit coding modes where the “1”s and “0”s have different bit lengths — all IR modes for example — the length of the NRZ “1” and “0” bits have correspondingly different bit lengths.

RF bit coding format 7 is a special case. As in the other formats, if SyncType = 0, information is sent according to the user-set IR or RF bit coding format. However, if SyncType = 1, a “0” is sent using the bit coding determined by the IR or RF coding format, and a “1” is sent as an NRZ zero. This is to maintain the “spirit” of the low duty cycle arrangement for RF format 7.

Figure 7 shows sync field examples for several bit coding formats.

Data Frame Fields (Continued)

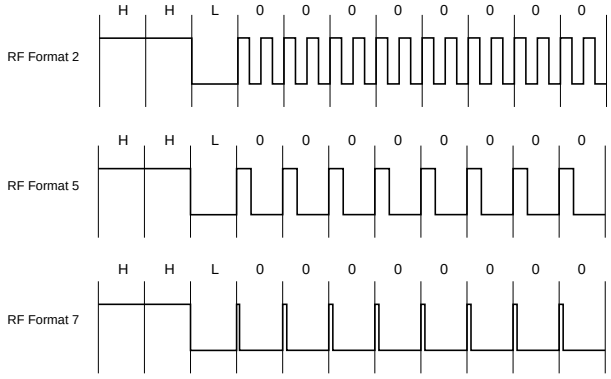


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FIGURE 6. Preamble Format Examples

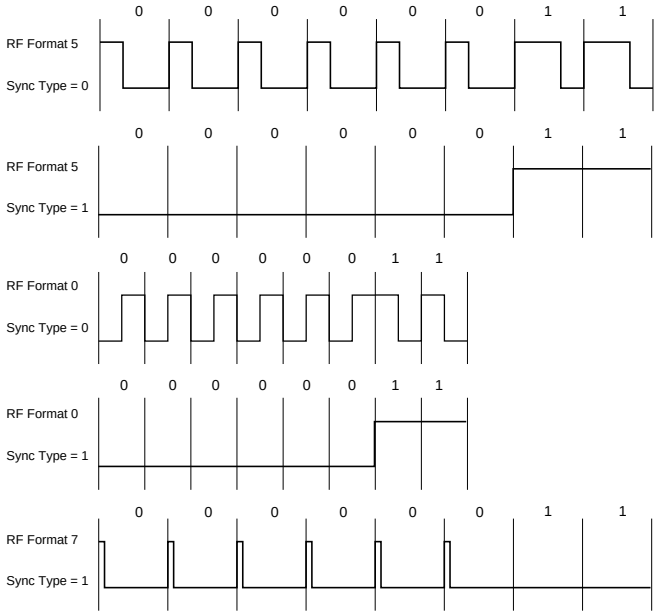

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FIGURE 7. Sync Field Examples for Data Byte 03h

KEY ID FIELD

The key ID field is another user option. Both its presence and the length of its field can be configured in EEPROM. If FixPresent = 0, no key ID field will be transmitted with the frame. If FixPresent = 1, a 24-bit field will be transmitted.

The contents of the key ID field are programmable by the user. Its purpose is to provide a unique identification code for each user key to allow a decoder to identify a particular key in applications where a decoder may be configured for multiple keys. Since the key ID register allows 24 bits, there are 2 24 possible key combinations. Each user key will be unique, and take full advantage of the HiSeC Generator's high security coding scheme.

The field size is selected with the FixSize bit. If FixSize = 1, the 24-bit field is selected. If FixSize = 0, the 20-bit field is selected. Since a full 24 bits are allowed in the Key ID register, the NM95HS01/02 will transmit the most significant 20 bits if FixSize = 0. The field is transmitted in the user-selected bit coding format.

DATA FIELD

The data field is transmitted with every frame. It has several uses, which are discussed here. The primary use of the data field is to indicate which key switch has been pressed. Since each key switch input can be associated with a particular application, the decoder can determine which function to initiate.

The data field is 4 bits long, and each key switch input is associated with a particular bit in the field. If any key switch is pressed, its corresponding bit in the data field will be seen as a "1". Any key switch not pressed is seen as a default "0". Key bits are transmitted in the order: K1, K2, K3, K4. The sync code field in the sync frame is a special case of the data field, and is found in the same position in the data frame. In any sync frame, the sync code is always 0000, so the decoder can always distinguish between a normal data frame and a sync frame. Since each bit represents a key, and a data frame is initiated as a result of pressing a key, it is not possible to have all zeroes in a normal data frame.

Data Frame Fields (Continued)

The data field can also serve as a low battery indicator. This is an option which can be enabled by setting the CompareEnable bit. If CompareEnable = 1, and the NM95HS01/02 detects a low battery level, the device will signal that fact by alternating between transmitting normal data frames with the correct key usage information, and transmitting normal data frames with a data field of 1111. In the first data frame, the data field will represent the true state of the four key inputs. In the next frame, this field will be all ones. This sequence will be repeated as long as frames are being transmitted. For sync frames, this field will not alternate, and the data will remain 0000 regardless of the battery level. Setting CompareEnable = 0 disables the low battery detect option.

DYNAMIC CODE FIELD

The dynamic code field is transmitted with every frame, and its length is programmable. If DynSize = 0, a 24-bit field is sent; if DynSize = 1, a 36-bit field is sent. Its function is to provide a secure dynamic code which changes with each new transmission. The field is the result of combining the 11-, 13-, and 16-bit CRC registers using non-linear logic and feedback. The result of this process is stored in the 24-/36-bit buffer register. If DynSize = 0, 24 of the possible 36 bits are transmitted in the field. Increasing the field length provides additional security.

The start code field in a sync frame is a special case of the dynamic code field. In sync mode, 40 bits of data are sent regardless of the setting of the DynSize bit.

PARITY FIELD

The parity field is an 8-bit field that is transmitted with every frame to ensure data integrity. It is a user option that is enabled by setting ParityPresent = 1.

The parity check is a bytewise exclusive OR-ing of all the bytes in the data frame from the sync field to the dynamic code field. The preamble, parity field and stop bit are not included. In practice, the parity process works as follows: bit m of the 8-bit parity field is a modulo 2 addition of the data frame bits m, m+8, m+16, … to the end of the frame. If the addition of the “1”s in these bits is odd, bit m of the parity field is set to “1”. If the addition is even, bit m is set to “0”. This process is continued for all 8 parity bits.

If the frame is not byte aligned, the parity field is calculated by zero extending the last four bits, calculating the bytewise exclusive OR-ing of all the bytes as described above, then swapping the higher and lower nibbles to give the correct parity.

STOP BIT

The stop bit is present in all frames. It is used to delimit the end of the frame for bit formats that require a definite end. It is necessary for formats that end with a long zero pulse. IR modes require a stop bit to distinguish between a “0” and a “1” in the next-to-last bit of a frame. The stop bit is read as a “1”, and is added for all modes.

DATA FRAME SEQUENCING AND TRANSMISSION

The NM95HS01/02 becomes operational any time a key is pressed. When this happens, the code generator logic is clocked to randomize the data and generate a new rolling code. Once the code is generated, data frames using this new code are repeatedly transmitted over the TX output pin as long as the key remains pressed. These data frames are separated by a pause whose length is programmable.

The transmission sequence is always begun by a preamble if this option is enabled. The preamble is only transmitted once, since its function is to wake the decoder from sleep mode if it is powered down for battery conservation. The preamble is then followed by a data frame, pause, data frame, pause, … etc.

TRANSMISSION INDICATION

Both the $\overline{\text{LED}}$ and $\overline{\text{RFEN}}$ signals can be used to indicate HiSeC rolling code transmission. The $\overline{\text{LED}}$ output is active low during the transmission of a pause, whereas the $\overline{\text{RFEN}}$ output is active low during transmission of either a frame or a pause. Either output may be used to provide a visual indication of transmission by connecting an LED between V_{CC} and $\overline{\text{LED}}$ or $\overline{\text{RFEN}}$.

If the low battery detect option is enabled, and the battery is low, the LED output is active only during the pause following the first frame of a new code transmission. It is not active on successive pauses, in order to conserve power.

Operational Timing Issues

DATA FRAME PAUSE LENGTH

After the complete transmission of a data frame, a pause is inserted before the next data frame is transmitted. The pause length can be modifed by configuring the 2-bit PauseLength parameter in EEPR0M. PauseLength is broken down into two single bit parameters, Pause1 and Pause0. Available configuration options are shown in Table 3.

TABLE 3. Pause Length Select Options

PAUSE1	PAUSE0	Function	Pause Time
0	0	0 x P3 Output	No Pause
0	1	8 x P3 Output	20 ms
1	0	20 x P3 Output	50 ms
1	1	50 x P3 Output	100 ms

HiSeC GENERATOR TIME-OUT

If the NM95HS01/02 time-out option is enabled (TIMEOUTEN = 1), the device will enter halt mode 80 seconds after a key is first activated, regardless of whether the key is still being pressed. This option guards against the condition that a key may be stuck low, which could drain the battery. If TIMEOUTEN = 0, the generator will continue to transmit data frames as long as a key is pressed.

HiSeC GENERATOR TIMER BLOCK

Bit timing and several function operating times are set in the generator through a user programmable timer block. This timer block is used to provide IR and RF bit timing signals, the interframe pause time, the AutoResync timing period, and the time-out delay.

The NM95HS01/02 timer block consists of three programmable 6-bit prescalers and a fixed 16-bit prescaler. The input to Prescaler1 is 1⁄4 of the frequency of CKI. The output is the IR clock. This signal becomes the input to Prescaler2. The output from Prescaler2 is the RF clock. This signal then becomes the input to Prescaler3. The output from Prescaler3 is a target value of 2.5 ms. Finally. this 2.5 ms timing signal becomes the input to the fixed 16-bit prescaler.

Operational Timing Issues (Continued)

There are several outputs from this prescaler. The 2.5 ms is divided by 4, 4096 and 32768, and these times are used to set the key debounce time (10 ms), the AutoResync time (>10 sec), and the generator time-out period (>80 sec), respectively.

The NM95HS01/02 timer block is shown in Figure 8.

The purpose of the prescalers is to provide various timing signals to the state machines in the generator. The IR clock is used as a time base for the various IR bit coding formats. The RF clock is used for RF bit coding formats. A programmable bit called SCLK determines whether the IR clock (SCLK = 0) or the RF clock (SCLK = 1) is used as the bit timing time base. In addition to SCLK, the system designer can program Prescaler1, Prescaler2 and Prescaler3 separately to set the necessary division factors. Since each of these prescalers is 6 bits, permissible values range from 2 to 64.

The system designer must set the programmable prescalers to meet the necessary timing requirements for all the functions discussed above. All of these timings are interdependent.

Figure 9 provides the basis for an example in calculating the necessary timing for these functions, and setting the timer block appropriately.

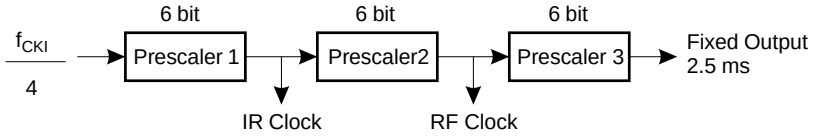


FIGURE 8. The NM95HS01/02 Timer Block

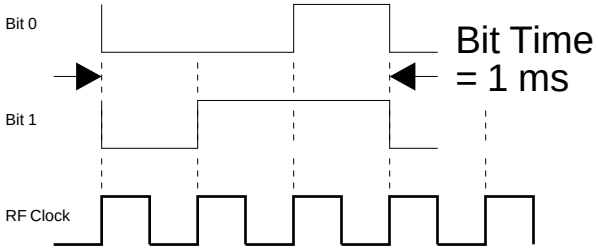


FIGURE 9. NM95HS01/02 Timer Block Example

As an example, consider the following situation. A designer wishes to design an RF data transmitter using RF bit coding format 5 with a bit time of 1 ms. The designer also wishes to use a 3 MHz crystal oscillator as the system clock.

The required bit time of 1 ms encompasses three RF clock periods for RF bit coding format 5. Therefore, the RF clock time needs to be 1/3 of 1 ms (=333 µs). The timer block has a target value of 2.5 ms (2500 µs) as the output of Prescaler3. Since the RF clock signal is divided by Prescaler3, Prescaler3 divides the signal by 2500/333 = 7.5. This figure is rounded off to become 8.

One point of possible confusion should be clarified here. Whenever a division value is calculated for any of the 3 prescalers, the prescaler should be configured with one unit less than that division value. For example, in this case, we calculated a division value of 8 (after rounding) for Prescaler3. Therefore, Prescaler3 should be programmed with 8 - 1=7.

Next we calculate values for Prescaler1 and Prescaler2.

Although the crystal oscillator uses both the CKI and CKO pins, only the CKI input is relevant here. The CKI input frequency is 3 MHz, and 1/4 of that is 0.75 MHz. This is the input frequency to the HiSeC timer block, and the corresponding timing signal is 1.33 µs.

Since the RF clock must be 333 µs, Prescalers1 and 2 together must divide by 333/1.33 = 250. A convenient choice would be to make Prescaler1 divide by 10 and Prescaler2 divide by 25.

Therefore, load Prescaler1 with 10 - 1 = 9, and Prescaler2 with 25 - 1 = 24.

DEBOUNCE LOGIC

The key switch input signals are connected to the debounce logic block, which continuously polls the inputs to determine if a key switch has been asserted. If a key switch has been asserted, its normally high input will be seen as a low. If the input is seen low for four continuous debounce strobe signals, it is considered to be a stable signal, and its associated output from the debounce logic block is set high. This enables the generator control logic, and a code is generated and transmitted.

This debounced output signal is deasserted as soon as the key is released and its signal goes high again. This assumes normal operation. However, if a key remained pressed for a long time, the generator might time-out before seeing the signal go high again (if TIMEOUTEN = 1). The generator would then enter halt mode even if the key remained pressed. The generator would come out of halt mode when it saw the falling edge of another key input, which would occur when another key is pressed.

LOW BATTERY DETECT OPTION

The NM95HS01/02 contains an internal comparator circuit that detects low battery voltage, and indicates this condition to the data frame generator. The CompareEnable parameter in EEPROM enables this function (CompareEnable = 1). During halt mode, the comparator is switched off completely to minimize power consumption. The BatteryType parameter in EEPROM selects the threshold voltage range for the comparator. If BatteryType = 1, the comparator assumes a 6V battery, and sets the low battery detect region to approxi-

Operational Timing Issues (Continued)

mately 4.4V to 4.8V. If BatteryType = 0, the comparator assumes a 3V battery, and sets the low battery detect region to approximately 2.2V to 2.4V.

Data output signals are sampled for low voltage at the start of the data field during frame transmission. If a low battery voltage level is detected, and the detect option is enabled, the LED will signal the condition by flashing at the first pause in the data frame transmission, and alternating normal data field data with a data field containing all ones. This procedure is explained more fully in the Data Field section.

Security Aspects

The basis of the HiSeC Generator is to provide a means of communicating information between the device and its decoder across some distance. Since data is transmitted at a distance, there is a possibility of signal interception and unauthorized use of the data by a third party. The NM95HS01/02 has been designed to provide such a high level of complexity and correlation immunity that intercepting the signal is immaterial.

INITIALIZATION/SYNCHRONIZATION

Initialization is the process of synchronizing the generator with its decoder for the first time. The NM95HS01/02 uses the following procedure to initialize the device.

The user inserts a new battery into the HiSeC-based device, which causes the LED to light. The LED also has a secondary function for synchronization and initialization procedures. It will light to prompt the end user that it expects some action, and therefore serves as a guide.

When the LED lights, the user presses a key. The LED will go off as the generator begins randomizing its registers, and configuring its internal logic. When the user releases the key, the LED will light a second time. This is a signal for the user to press a key again. This second action shifts the generator into sync mode. This causes the NM95HS01/02 to transmit at least four sync frames, allowing the decoder to synchronize to the generator. The generator then exits sync mode, and is ready tor normal operation.

RESYNCHRONIZATION

If synchronization is lost between the generator and its decoder, resynchronization is accomplished using a sync frame. A sync frame is generated in two cases: when the battery is removed and replaced, or the user initiates an initialization procedure by holding Key Switch 1 and Key Switch 2 simultaneously for 5 seconds.

A sync frame provides the decoder with enough information to "learn" the key and synchronize to it.

For the highest possible security protection, resynchronization can be completely excluded by configuring the decoder to recognize, and refuse to act upon, the transmission of a sync frame. The sync frame format is discussed more fully elsewhere, but briefly, it can be recognized by the presence of all zeroes in the data field. In this case, if synchronization is lost between the generator and decoder, they could not be made to function together.

Security Aspects

NORMAL OPERATION

Once the NM95HS01/02 has been initialized, the device will generate and transmit a new code each time a key is pressed. If a key is held down, the same frame (plus any pauses between frames) is transmitted repeatedly. If the key is held down for longer than 80 seconds, the generator will go into halt mode to conserve battery power, and will stop transmitting data frames (if the TIMEOUTEN option is enabled).

Another option available during normal generator operation is the ability to generate a resync after a key has been pressed for more than 10 seconds (if the AutoResync option is enabled). This option allows the end user to resynchronize the generator if necessary, without having to remove and replace the battery.

FORWARD CALCULATION AND CODE WINDOWS

Aside from using a sync frame, there is another way to ensure the NM95HS01/02 remains in sync with its decoder during normal operation. The decoder can perform a forward calculation to predict what the next generator codes will be. This is an important point, and should be considered carefully in designing the decoding system.

In a well-designed system, the decoder should be able to calculate forward for some reasonable number of codes, and store the results for future reference. This allows the decoder to remain in sync even if it misses one or more codes from the generator. This could occur if the receiver did not receive a transmission clearly, or if someone activated the keys outside the range of the receiver.

Increasing the depth of this code window would allow the decoder to miss a greater number of codes from the generator, and still remain in sync. One method for implementing a code window is to include a MICROWIRE™ EEPROM (such as the NM93Cx6) in the decoder design, and store the codes in memory. This becomes even more important if the decoder is designed to accomodate several HiSeC generator devices. In this case, the decoder should have a code window available for each device.

Generator Clock Design Parameters

Table 4, Table 5, and Table 6 provide a basis for selecting component values for both the RC clocked generator (NM95HS01) and the crystal (XTAL) oscillator clocked generator (NM95HS02).

The component values shown in the tables have been chosen for low cost, general availability, and reliable operation. Components are referenced to the circuit schematics shown in Figure 3. Though there is some flexibility in selecting alternate values, there are constraints on permissible component values.

All resistors and capacitors should be kept within the following ranges; 3 kΩ ≤ R_x ≤ 200 kΩ and 50 pF ≤ C_x ≤ 200 pF.

TABLE 4. RC Clock Components, TA = 25°C, V_{CC} = 5V–6.5V

R (kΩ)	C (pF)	CKI (MHz)	CKI (ns)
3.3	82	2.12–2.32	470–430
5.6	100	1.1–1.17	870–850

Generator Clock Design Parameters

(Continued)

TABLE 4. RC Clock Components, TA = 25°C, V_{CC} = 5V–6.5V (Continued)

R (kΩ)	C (pF)	CKI (MHz)	CKI (ns)
6.8	100	0.9–0.95	1100–1050

TABLE 5. RC Clock Components, TA = 25°C, V_{CC} = 2.5V

R (kΩ)	C (pF)	CKI (MHz)	CKI (ns)
3.3	82	1.53–1.6	650–600
5.6	100	0.9–1	1100–1000
6.8	100	0.8–0.83	1250–1200

TABLE 6. XTAL Clock Components, TA = 25°C, V_{CC} = 2.5V–6.5V

R1 (MΩ)	C1 (pF)	C2 (pF)	CKI (MHz)	CKI (ns)
1	30	30–36	4	250

TABLE 7. NM95HS01/02 EEPROM Array Configuration and Definitions

Parameter	Bits	Address	Function
AutoResync	1	Byte 0, bit 7	Allows user to send a sync frame by holding a key down for >10 seconds
LEDSEL	1	Byte 0, bit 6	Determines whether $\overline{RFEN}$/$\overline{LED}$ or CKO/$\overline{LED}$ is the LED connect pin for the NM95HS02
BatteryType	1	Byte 0, bit 5	Selects between 3V and 6V battery voltage
TIMEOUTEN	1	Byte 0, bit 4	Disables data transmission if key is depressed >80 seconds
Pause Length (Pause0/Pause1)	2	Byte 0, bits 3–2	Sets the pause time between data frames during data transmission (0/20/50/100) ms
FactoryDisableBit	1	Byte 0, bit 1	Disables ability to write to Byte 12
WriteDisableBit	1	Byte 0, bit 0	Enables/disables ability to write into EEPROM array
PreamblePresent	1	Byte 1, bit 7	Enables/disables presence of preamble field
SyncType	1	Byte 1, bit 6	Determines if sync field is sent in user-selected IR/RF format or default NRZ format
SyncPresent	1	Byte 1, bit 5	Enables/disables presence of sync field
FixSize	1	Byte 1, bit 4	Determines length of Key ID field (0/20/24 bits)
FixPresent	1	Byte 1, bit 3	Enables/disables presence of Key ID field
DynSize	1	Byte 1, bit 2	Determines length of Dynamic Code field (24/36 bits)
ParityPresent	1	Byte 1, bit 1	Enables/disables presence of parity field
CompareEnable	1	Byte 1, bit 0	Enables/disables low battery detect option
BitTransmitFormat IRSel PRSeI2,1,0	 1 3	 Byte 2, bit 7 Byte 2, bits 6–4	Selects among the 12 possible IR/RF bit coding formats Selects between IR and RF bit coding formats Used with IRSeI to select particular bit coding format
TxPol	1	Byte 2, bit 3	Sets the quiescent output state and data logic level on the TX output pin
SCLK	1	Byte 2, bit 2	Determines whether the IR clock or RF clock is used as the bit timing time base
Prescaler3	6	Byte 2, bits 1–0 Byte 3, bits 7–4	Sets interframe delay time and key debounce time (Also generates timeout delay time)
Prescaler2	6	Byte 3, bits 3–0 Byte 4, bits 7–6	Sets RF Clock timing
Prescaler1	6	Byte 4, bits 5–0	Sets IR Clock timing
DynamicCode	24	Bytes 5–7	Sets initial configuration of the Rolling Code registers
KeyIDCode	24	Bytes 8–10	Sets user-configurable key identification register
SyncFieldCode	8	Byte 11	Sets configuration of sync field register
Reserved	8	Byte 12	Reserved for factory use — unique customized algorithm option

Note: The first bit clocked into the device is Byte 0, bit 7. The seventh and eight bits are the chip disable bits. Once they are set, and V_{CC} is removed, the chip will be disabled.

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature -65°C to +150°C

Input or Output Voltages with Respect to Ground
- All except K1 or K2 -0.5V to +7V
- K1 or K2 -0.5V to +13V

Lead Temperature
- (Soldering, 10 sec.) +300°C

ESD Rating 2000V

Ambient Operating Temperature
- NM95HS01/NM95HS02 0°C to +70°C
- NM95HS01E/NM95HS02E -40°C to +85°C

Power Supply (V_{CC}) Range 2.2V to 6.5V

NM95HS01/02 DC and AC Electrical Characteristics $2.2V \le V_{CC} \le 6.5V$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC}	Supply Voltage		2.5	5.0	6.5	V
V_{RW}	Read/Write Voltage		4.5	5.0	5.5	V
V_{SV}	Supervoltage	(Note 2)	11.5	12.0	12.5	V
I_{CC}	Supply Current					
	Halt Mode (3.0V) (Note 2)	CKI = 0 MHz, V_{CC} = 3.0V		0.1	1	µA
	Halt Mode (6.0V)	CKI = 0 MHz, V_{CC} = 6.0V		0.5	2	µA
	Normal Mode	CKI = 4.1 MHz, V_{CC} = 6V		1	3	mA
V_{IH}	Input Voltage (High)	CKI: Logic High	0.8 V_{CC}			V
		All Others; Logic High	0.7 V_{CC}			V
V_{IL}	Input Voltage (Low)	CKI: Logic Low			0.2 V_{CC}	V
		All Others: Logic Low			0.2 V_{CC}	V
I_P	Pullup Current	V_{CC} = 6V, V_{IN} = 0V	35	120	250	µA
I_{RF}	Leakage Current (RFEN)	V_{CC} = 6V, RFEN = 6V			1	µA
I_{OUT}	Output Current					
	Source (Push-Pull)	V_{CC} = 4.5V, V_{OH} = 3.3V	10			mA
	Sink (Push-Pull)	V_{CC} = 4.5V, V_{OL} = 0.4V	15			mA
t_{PS}	Power Supply Rise Time		1 µs	10 µs	10 ms	
I_{MP}	Max. Sink-Source Current per Pin				20	mA
V_{TH}	Comparator Threshold Voltage	BattType = 0 (3V)	2.2		2.4	V
		BattType = 1 (6V)	4.4		4.8	V
t_{WW}	K1 Initiate Write Time	$t_{WW} = t_{WHW} + t_{WLW}$	40			µs
t_{WHW}	Write Time High		20			µs
t_{WLW}	Write Time Low		20			µs
t_{SW}	K2 Setup Time		20			µs
t_{HW}	K2 Hold Time		20			µs
t_{PW}	Program Write Time		10			ms
t_{CKIHSW}	Supervoltage Low to Clock High Time		10			µs
t_{SVLW}	Clock Low to Supervolt High Time		10			µs
t_{XW}	Exit Write Time			10		µs
t_{DSW}	Data Setup Time		100			ns
t_{DHW}	Data Hold Time		100			ns
t_{WR}	Initiate K1 Read Time	$t_{WR} = t_{WHR} + t_{WLR}$		40		µs
t_{WHR}	Read Time High			20		µs
t_{WLR}	Read Time Low			20		µs
t_{CKIHSR}	Start Read Time		10			µs
t_{CKI}	Clock Period Time	XTAL Clock	2000		DC	ns
	(Note 4)	RC Clock	2000		DC	ns
t_{CKIH}	Clock High Time	XTAL Clock	1000		DC	ns
	(Note 4)	RC Clock	1000		DC	ns
t_{CKIL}	Clock Low Time	XTAL Clock	1000		DC	ns
	(Note 4)	RC Clock	1000		DC	ns

NM95HS01/02 DC and AC Electrical Characteristics (Continued)

$2.2V \le V_{CC} \le 6.5V$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DAR}	Data Access Time	$t_{DAR} = t_{CKIH} + t_{DALR}$	1.1			µs
t_{DALR}	Data Access Time Low		100			ns
t_{ENDR}	End Read Time			10		µs
t_{SVLR}	K1 Supervoltage Low Time (Read)			10		µs
t_{XR}	Exit Read Time			10		µs

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The standby current of <1 µA is tested at 3V. During HALT Mode only a very small current is required to maintain the code in the shift registers. HALT mode is exited by depressing one of the input keys.

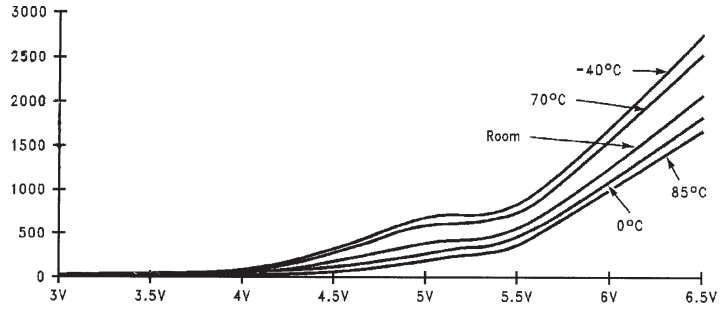
Note 3: The clock rate used to program the NM95HS01/02 is generally less than the normal operating mode clock rate, and should be temporarily reduced as necessary to meet the programming specifications shown here. For example, a generator might normally operate at 4 MHz, but should be programmed at ≤0.5 MHz (2000 ns).

Note 4: Parameter characterized but not 100% tested.

Capacitance (Note 2) T_A = +25°C, f = 1 MHz

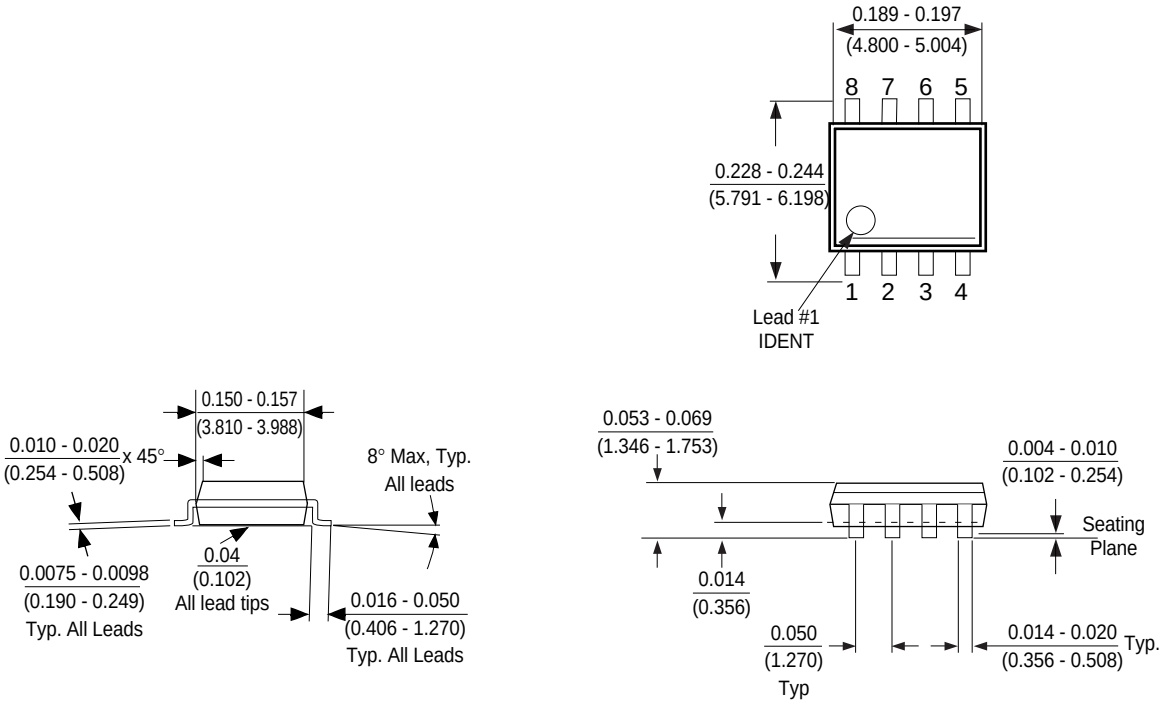
Symbol	Test	Max	Units
C_{IN}	Input Capacitance	7	pF
C_{OUT}	0utput Capacitance	12	pF

Typical Halt Mode Current (nA) vs Voltage over Termperature

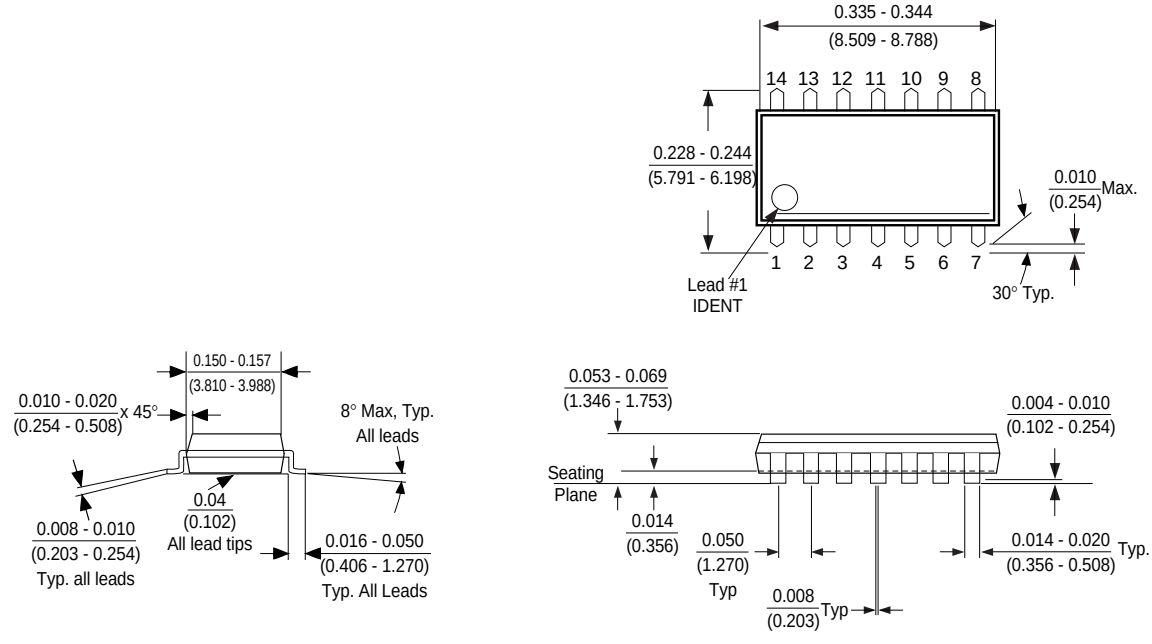


DS012302-23

Physical Dimensions inches (millimeters) unless otherwise noted

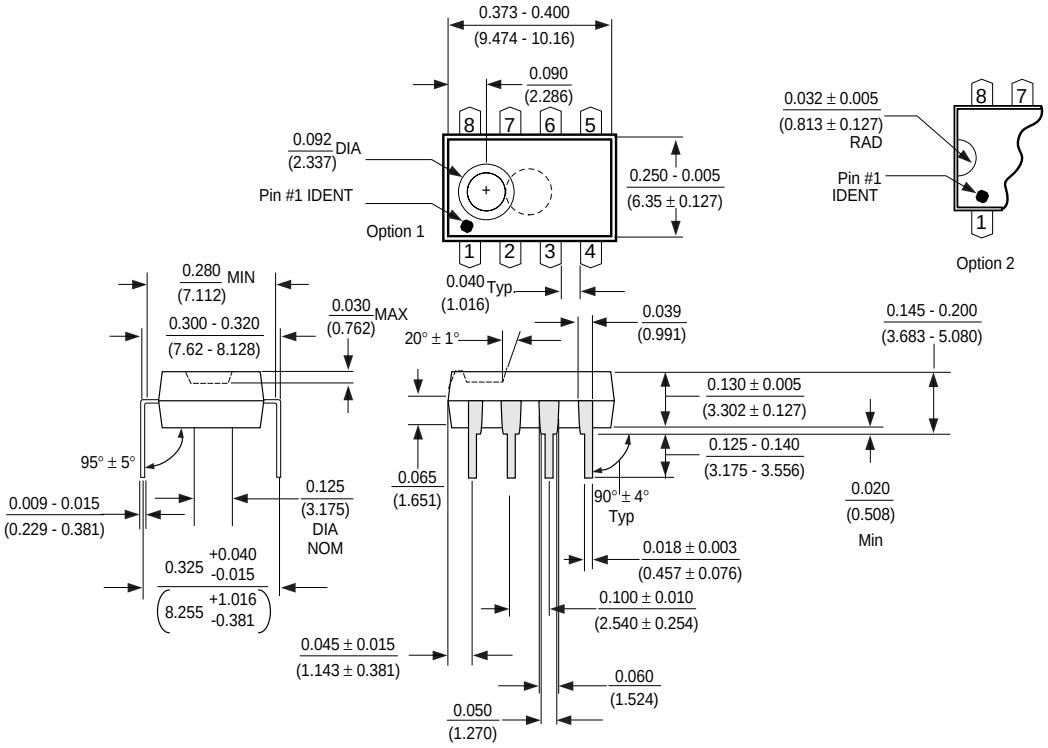


8-Lead (0.150" Wide) Molded Small Outline Package, JEDEC
Order Number NM95HS01M8 or NM95HS02M8
Package Number M08A

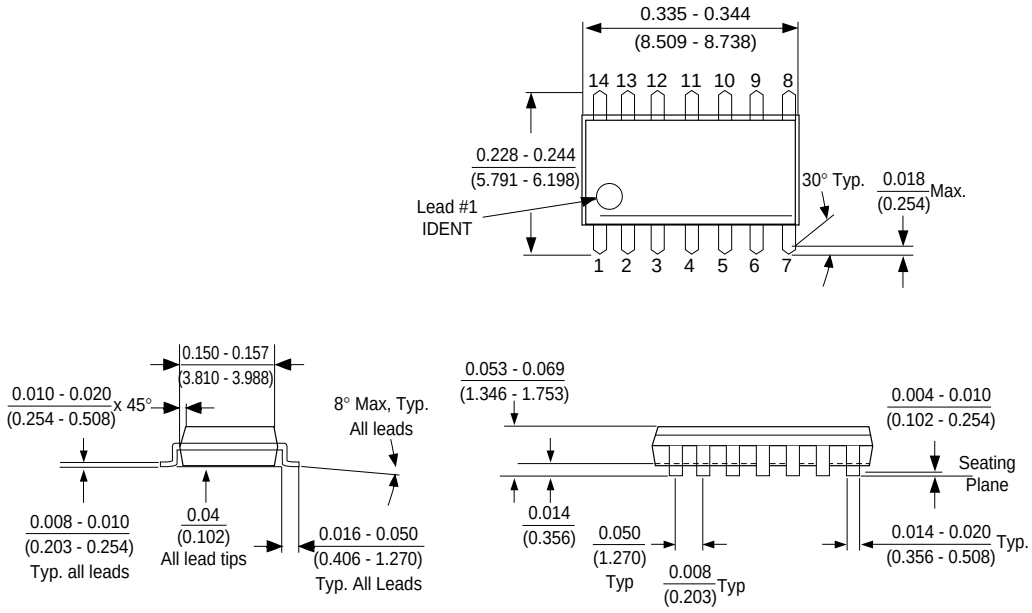


14-Lead (0.150" Wide) Molded Small Outline Package, JEDEC
Order Number NM95HS01M14 or NM95HS02M14
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted

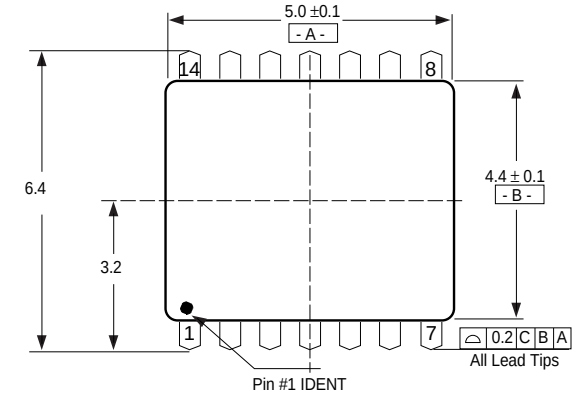


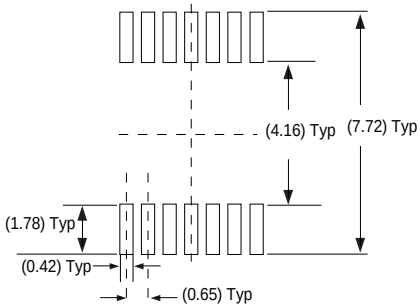
8-Lead Dual-In-Line Package
Order Number NM95HS01N, NM95HS01EN, NM95HS02N or NM95HS02EN
Package Number N08E



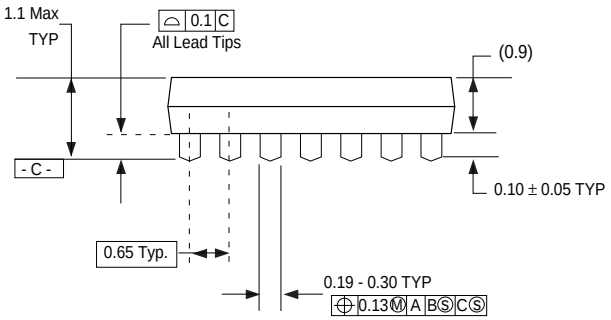
14-Lead (0.300" Wide) Molded Dual-In-Line Package
Order Number NM95HS01N14 or NM95HS02N14
Package Number N14A

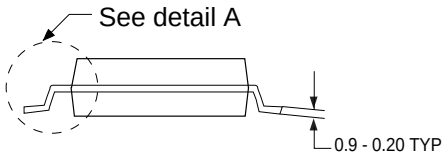
Physical Dimensions inches (millimeters) unless otherwise noted

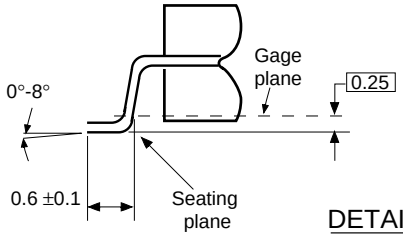




Land pattern recommendation







DETAIL A
Typ. Scale: 40X

Dimensions are in millimeters

14-Lead Molded Thin Shrink Small Outline Package, JEDEC
Order Number NM95HS01MT14/NM95HS02MT14
Package Number MTC14

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FAIRCHILD SEMICONDUCTOR™

July 1998

NM95MS14
Plug 'n Play Front-End Devices for ISA-Bus Systems

General Description

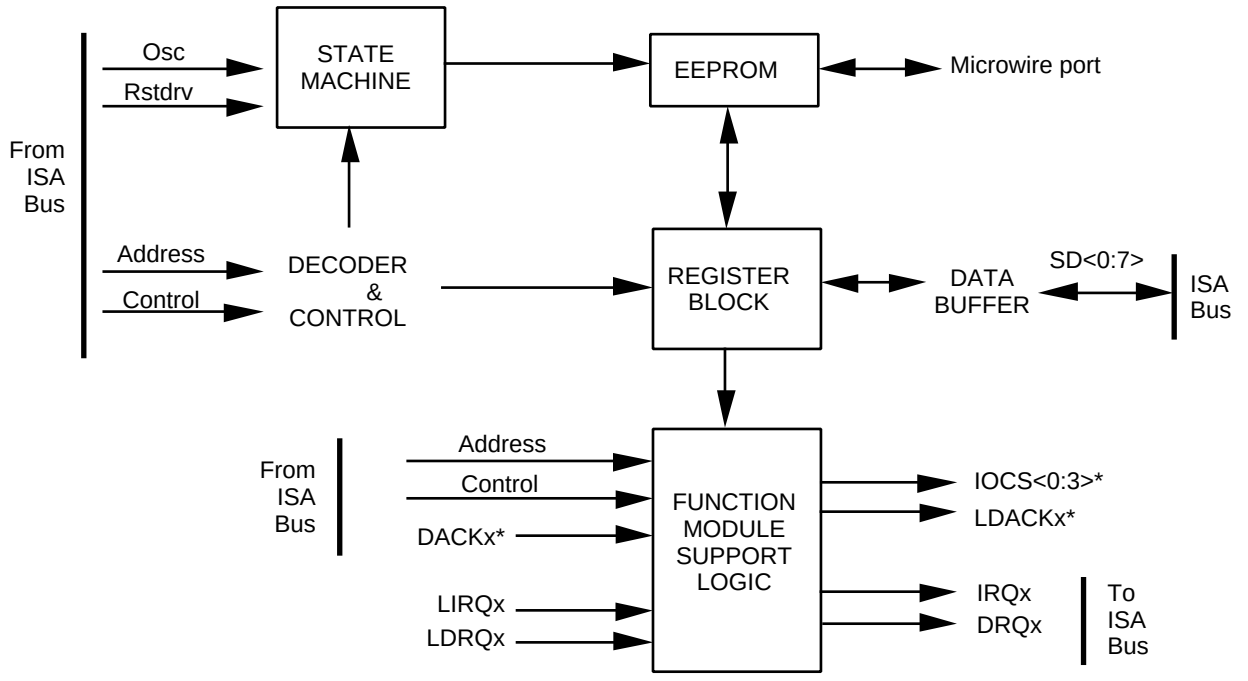
The NM95MS14 is the smaller of a family of devices designed to provide complete Plug 'n Play Capability for ISA bus systems. The NM95MS14 includes the necessary state machine logic to manage the Plug 'n Play protocol in addition to switches for steering Interrupt and DMA requests. It also features a built-in 2k bits of serial EEPROM for storing the resource data specified in the Plug 'n Play Standard. In addition, 4k bits of EEPROM is available for use by other on-board logic. This device provides a "truly complete" single-chip solution for implementing Plug 'n Play on ISA-Bus Adapter cards. The NM95MS14 supports one logical device with a flexible choice of DMA/IRQ selection and I/O Chipselect generation.

NM95MS14 is implemented using Fairchild's Advanced CMOS process and operates single power supply. The NM95MS14 is available in a 48-pin TQFP package.

Features

- Complete implementation of Plug 'n Play standard
  — Direct interface to ISA bus
- Two modes of operation
  — DMA mode
  — Extended Interrupt mode
- 6 or 8 ISA bus interrupt lines and 2 DRQ/DACK lines supported
- On-chip EEPROM for resource request table
- Additional 4 Kbits of on-chip EEPROM available for external access
- 24 mA drivers for data outputs
- 48-pin TQFP

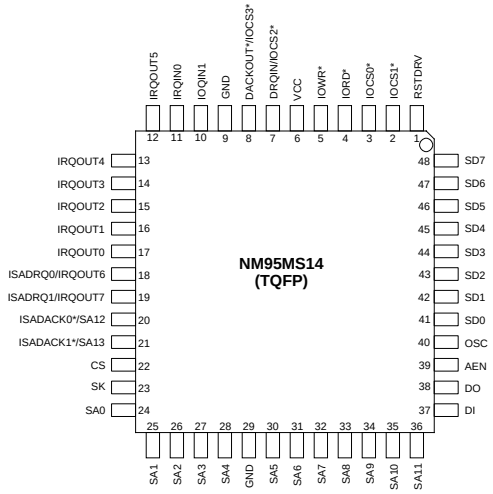
Block Diagram



DS012315-1

Connection Diagram

Commercial Temperature Range (0°C to +70°C)



DS012315-2

Order Number NM95MS14VBH

Signals	Type	Description
SA<11:0>	I	Address inputs from the ISA bus.
IORD*	I	I/O read strobe from the ISA bus.
IOWR*	I	I/O write strobe from the ISA bus.
AEN	I	Address Enable from ISA Bus —used in conjunction with DMA.
SD<7:0>	I/O	Data bus —lower byte —from/to the ISA bus.
OSC (Note 2)	I	"OSC" Clock from the ISA bus —used for internal state machines.
RSTDRV	I	Reset input from the ISA bus.
CS	I	Chip select for Microwire port. **There should be a pulldown resistor of 4.7k on CS pin if** unused externally or directly connected to GND.
SK, DI	I	Clock and Data input lines for Microwire bus connection to access a portion (4k) on chip EEPROM.
DO	O	Data output line for the Microwire interface detailed above.
IRQOUT<5:0>	O	Connection to ISA bus interrupt request pins. On-chip interrupt request(s) may be connected to any 6 of the ISA IRQ lines.
IRQIN<1:0>	I	Interrupt request from on-board logic
DRQin/IOCS2*	I	DMA request from on-board logic, or Programmable chipselect (2) depending on mode selected.
DACKOUT*/IOCS3*	O	DMA Acknowledge for on-board logic or Programmable chipselect (3) depending on mode selected.
ISADRQ<1:0>/ IRQOUT<7:6>	O	Connection for two ISA bus DMA Request lines, or additional interrupt request lines depending on the mode selected.
ISADACK<1:0>*/ SA<13:12>	I	DMA Acknowledge from the ISA bus or additional address lines depending on the mode selected.
IOCS<1:0>*	O	Programmable chip selects to address on-board peripheral.

Note 1: Signal name with a "*" means its an active low signal.

Note 2: "OSC" clock from ISA Bus is fixed at a standard frequency of 14.318 MHz. NM95MS14 is designed and tested for 14.318 MHz. However the NM95MS14 can handle frequencies up to 24 MHz though it is not 100% tested.

Pinout Details for the NM95MS14

Mode 00 = DMA Mode; Mode 01 = Extended Interrupt Mode

Pin #	Pin Name	
TQFP	DMA Ext.	Intr.
1	RSTDRV	RSTDRV
2	IOCS1*	IOCS1*
3	IOCS0*	IOCS0*
4	IORD*	IORD*
5	IOWR*	IOWR*
6	V_{CC}	V_{CC}
7	DRQIN	IOCS2*
8	DACKOUT*	IOCS3*
9	GND	GND
10	IRQIN1	IRQIN1
11	IRQIN0	IRQIN0
12	IRQOUT5	IRQOUT5
13	IRQOUT4	IRQOUT4
14	IRQOUT3	IRQOUT3
15	IRQOUT2	IRQOUT2
16	IRQOUT1	IRQOUT1
17	IRQOUT0	IRQOUT0
18	ISADRQ0	IRQOUT6
19	ISADRQ1	IRQOUT7
20	ISADACK*	SA12
21	ISADACK1*	SA13
22	CS	CS
23	SK	SK
24	SA0	SA0

Pin #	Pin Name	
25	SA1	SA1
26	SA2	SA2
27	SA3	SA3
28	SA4	SA4
29	GND	GND
30	SA5	SA5
31	SA6	SA6
32	SA7	SA7
33	SA8	SA8
34	SA9	SA9
35	SA10	SA10
36	SA11	SA11
37	DI	DI
38	DO	DO
39	AEN	AEN
40	OSC	OSC
41	SD0	SD0
42	SD1	SD1
43	SD2	SD2
44	SD3	SD3
45	SD4	SD4
46	SD5	SD5
47	SD6	SD6
48	SD7	SD7

Note 3: Mode selection (00 or 01) is done by setting MS bits in the EEPROM configuration register. Detailed information about this is described in User's Guide.

Absolute Maximum Ratings (Note 4)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltages with Respect to Ground	V_{CC} + 1V to -0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V Min

Operating Conditions

Ambient Operating Temperature NM95MS14	0°C to +70°C
Positive Power Supply (V_{CC})	4.5V to 5.5V

DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 5)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		—	10.0	mA
I_{LI}	Input Leakage Current	V_{IN} = GND or V_{CC}		0.2	1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}			1.0	µA
V_{IL}	Input Low Voltage			-0.1	0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1.0	V
V_{OL}	Output Low Voltage	I_{OL} = 24 mA (Note 7) I_{OL} = 2.1 mA (Note 8)			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -3 mA (Note 7) I_{OH} = -400 µA (Note 8)	2.4 2.4			V V

Capacitance T_A = +25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Conditions	Max	Units
CI/O (Note 6)	Input/Output Capacitance	VI/O = 0V	8	pF
C_{IN} (Note 6)	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT} (Note 6)	Output Capacitance	V_{OUT} = 0V	6	pF

Note 4: This footnote is intentionally blank.

Note 5: Typical values are for T_A = 25°C and nominal supply voltage (5V).

Note 6: This parameter is periodically sampled and not 100% tested.

Note 7: These values are for ISA signals like SD[0:7], IRQx, DRQx.

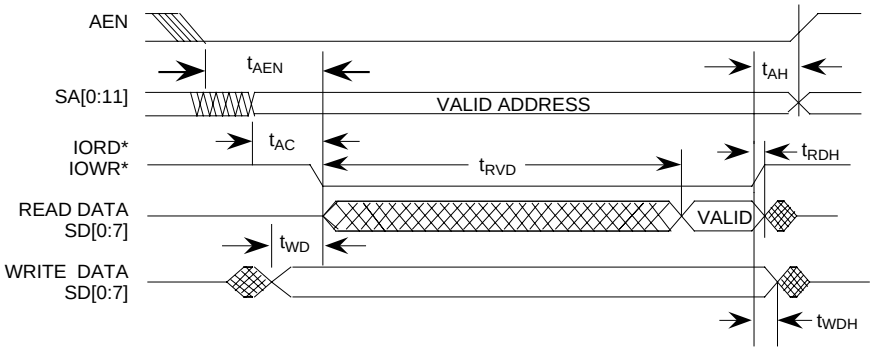
Note 8: These values are for card signal like IOCS[0:3]*, DO(EEPROM).

AC Electrical Characteristics

Symbol	Parameter	Min	Max	Unit
t_{AEN}	AEN Valid to Command Active	100		ns
t_{AC}	Address Valid to Command Active	88		ns
t_{RVD}	Active Read to Valid Data		200	ns
t_{AH}	Address, AEN Hold from Inactive Command	30		ns
t_{RDH}	Read Data Hold from Inactive Read		5	ns
t_{WD}	Write Data Valid before Write Active	22		ns
t_{WDH}	Write Data Hold after Write Inactive	25		ns
t_{CSA}	Chip Selects Valid from Address Valid	5	25	ns
t_{CSC}	Chip Selects Valid from Command Active	5	25	ns
t_{IDD}	Propagation Delay for IRQ/DRQ/DACK	5	25	ns

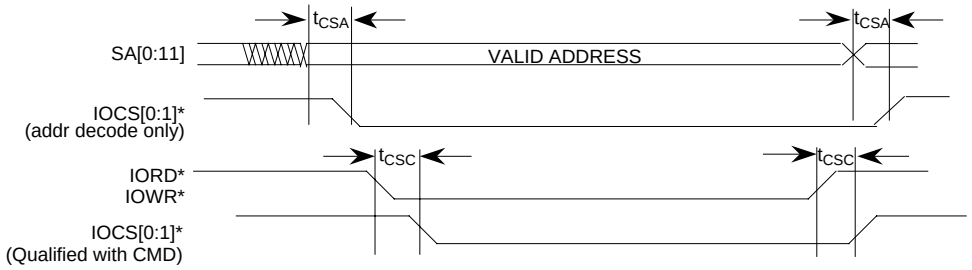
Timing Diagrams

(1) Timings for ISA Read/Write Cycle



DS012315-3

(2) Decode Delay for Chipselect Generation



DS012315-4

(3) Propagation Delay for IRQ/DRQ/DACK

DS012315-5

Introduction

The NM95MS14 is a single-chip solution for the ISA Plug 'n Play (PnP) specification. It implements the complete state machine and the necessary logic for supporting configurable Interrrupts and DMA channels on the ISA bus for one logical device. Apart from providing "Plug 'n Play" capability, it has built-in EEPROM that eliminates external EEPROM. This device is available in a space saving 48-pin Thin Quad Flat Pack (TQFP) package.

Functional Description

NM95MS14 has two modes of operation, viz, "DMA mode" and "Extended Interrupt mode". These modes are programmed using the mode select (MS) bits in one of the configuration registers (Refer to the User's guide for detailed information). Each of these modes are discussed below.

DMA Mode

In the DMA mode, support is provided for

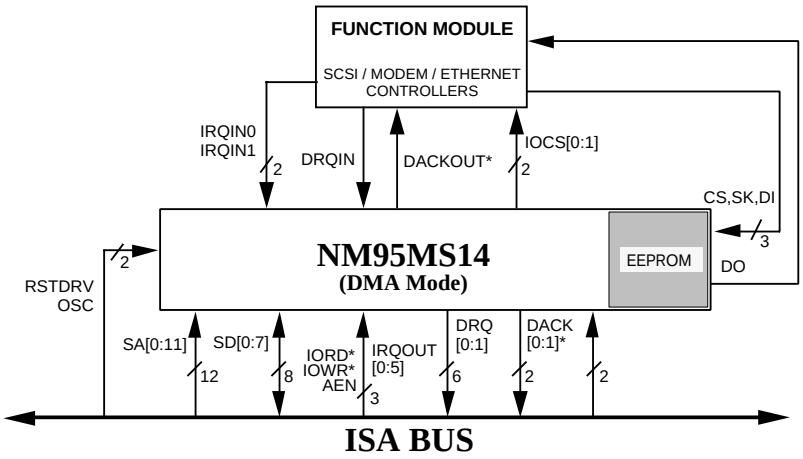
1. One on-board DMA request that is switchable to any two DMA channels on the ISA bus.

2. Two on-board interrupt request lines switchable to any six IRQ lines on the ISA bus.

3. Two programmable I/O chip selects for on-board logic.

Figure 1 shows a Block Diagram of NM95MS14 configured for DMA Mode.

Block Diagrams



DS012315-6

FIGURE 1.

Extended Interrupt Mode

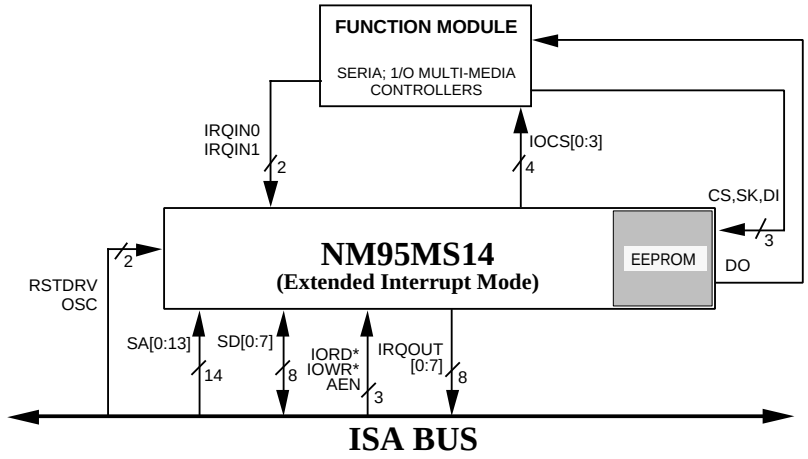
In the Ext. Int mode, support is provided for:

1. Two on-board interrupt request lines switchable to any eight IRQ lines on the ISA bus.

2. Four programmable I/O chip selects for on-board logic.

3. ISA address SA12 and SA13 are also included for extended decode.

Figure 2 shows a Block Diagram of NM95MS14 configured for Extended Interrupt Mode.



DS012315-7

FIGURE 2.

Chipselect Generation

Individual I/O chipselect can be generated in the following two ways:

A) Address Decode only

B) Address Decode qualified by Command (IORD*, IOWR*).

On-Chip EEPROM

NM95MS14 has 6k of EEPROM on chip. All the PnP resource data structure for the logical device is stored in this EEPROM. Of the 6k bits, 4k bits are available for the logical device's external usage. The logical device can access the EEPROM through a microwire port, which is essentially a 4-wire serial bus. The pins CS, SK, DI & DO follow the exact timing as the standard microwire bus and are compatible to the NM93Cxx family of EEPROMs.

EEPROM Programming

The entire 6k bits of EEPROM can be programmed through the ISA bus. The EEPROM can be programmed by putting the device (NM95MS14) in the Config. state (as defined in the PnP standard). Under this state 4 registers at address 0xF0–0xF3 are accessible to program the EEPROM. The data to be programmed is loaded in register at address 0xF3 and 0xF2 (LSB and MSB respectively). The address to be programmed is loaded in register at address 0xF1. The Ninth bit of address for 6k bits of memory is provided through the register at address 0xF0. Both read write are possible. The

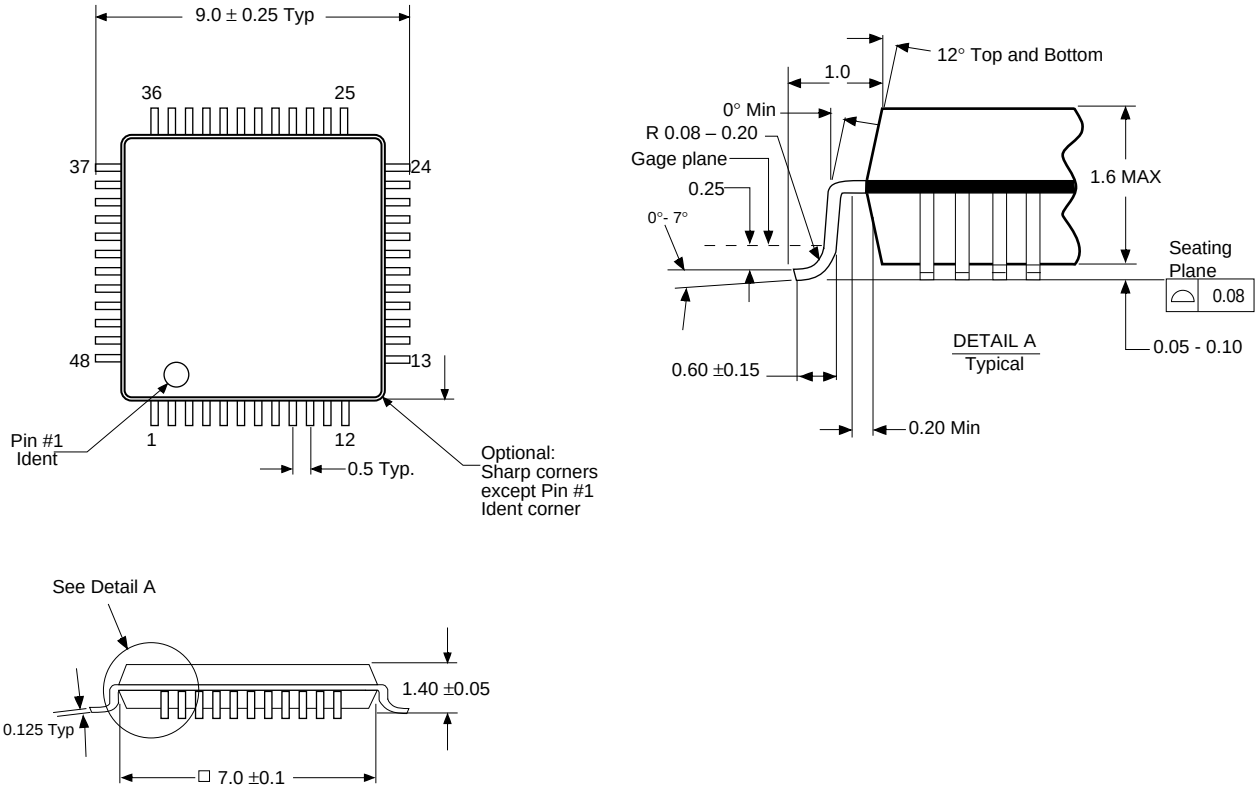
EEPROM Programming (Continued)

actual operation does not begin until Go Ahead (GA) bit is set. Programming a word takes approximately 10 ms. The status of the operation can be polled by the Status bit. This bit is set when the operation is in progress and will be reset when complete. The register at address 0xF0 is COMMAND register. This is the handshake register in programming the EEPROM and is explained below in a tabular format.

COMMAND register	0xF0	Bit[1:0] - OP Code bits 10 - Read operation 01 - Write operation Bit[2] GA(Go ahead bits) If set to 1 the programming will continue. Bit[6:3] - Reserved, should be 0. Bit[7] - It provides A8 of the address. A[0:7] is provided by 0xF1 reg. (Note 9)
Address Register	0xF1	AddressRegister [A0–A7]
Data Register	0xF2	Data Byte [MSB]
Data Register	0xF3	Data Byte [LSB]
STATUS Register	0x05	Bit[0] - Status/Busy bit "0" is busy, "1" is done.

Note 9: The PNP resource data portion of the internal memory is at high address. Hence to program that portion, Bit [7] of register 0XF0 (Address A8) should be set to "1".

Physical Dimensions inches (millimeters) unless otherwise noted



TQFP Package (VBH)
Package Number VBH48A
Order Number NM95MS14VBH

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FAIRCHILD SEMICONDUCTOR™

July 1998

NM95MS15
Plug and Play Front-End Device for ISA-Bus Systems

General Description

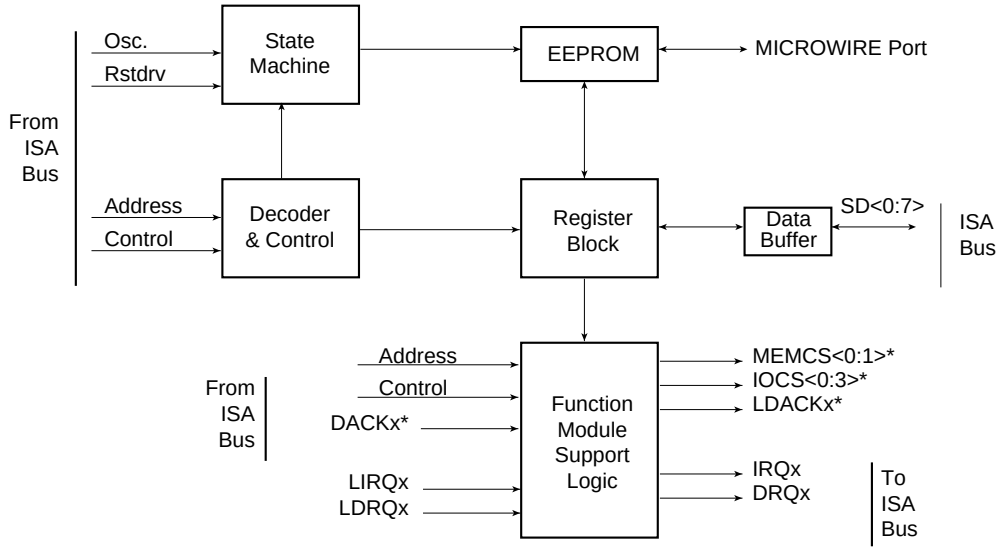
The NM95MS15 is one of the family of single chip solutions designed to provide complete Plug and Play capability for ISA bus systems. The NM95MS15 includes the necessary state machine logic to manage the Plug and Play protocol in addition to switches for steering Interrupt and DMA requests. It also features a built-in 4k bits of serial EEPROM for storing the resource data specified in the Plug and Play Standard. In addition, 4k bits of the EEPROM is available for use by other on-board logic. This device provides a truly complete single-chip solution for implementing Plug and Play on ISA-Bus adapter cards. The NM95MS15 supports two logical devices with a flexible choice of DMA/IRQ selection, I/O, and MEMORY Chip Select generation.

NM95MS15 is implemented using Fairchild's advanced CMOS process and operates from a single power supply. The NM95MS15 is available in a 64-pin TQFP package.

Features

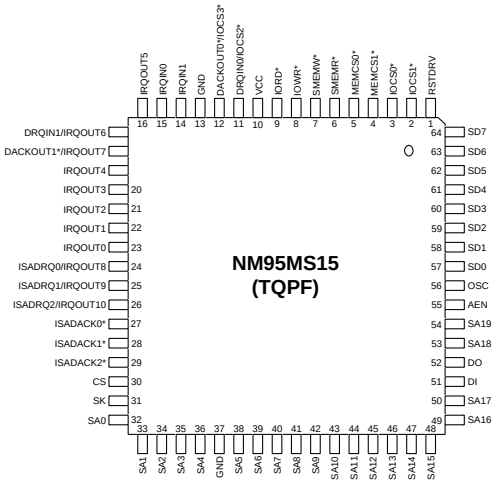
- Single chip implementation of complete Plug and Play Standard
  - Direct interface to ISA-bus
- Three modes of operation
  - Normal DMA mode
  - Extended Interrupt mode
  - Extended DMA mode
- 6, 8, or 11 ISA-bus interrupt lines and 3 DRQ/DACK lines supported (IRQ's and DRQ's are mode dependent)
- On-chip EEPROM for resource request table
- Additional 4k bits of on-chip EEPROM available for external access
- 24 mA drivers for data outputs
- 64-pin TQFP package

Functional Diagram



DS012394-1

Connection Diagram



DS012394-2

Commercial Temperature Range (0°C to +70°C)

Order Number NM95MS15VEH

Signals	Type	Description
SA<19:0>	I	Address inputs from the ISA bus.
IORD* (Note 1) , SMEMR* (Note 1)	I	I/O and memory read strobes from the ISA bus.
IOWR* (Note 1) , SMEMW* (Note 1)	I	I/O write and memory write strobes from the ISA bus.
AEN	I	Address Enable from ISA bus—used in conjunction with DMA.
SD<7:0>	I/O	Data bus—lower byte—from/to the ISA bus.
OSC (Note 2)	I	"OSC" Clock from ISA bus—used for internal state machine.
RSTDRV	I	Reset input from the ISA bus.
SK,DI	I	Clock and Data input lines for microwire bus connection to access a portion (4k) on chip EEPROM.
CS	I	Chip select for microwire bus connection to access 4k on chip EEPROM. This pin should be pulled down to GND, if the 4k user portion is not used.
DO	O	Data output line for the Microwire interface detailed above.
IRQOUT<5:0>	O	Connection to ISA bus interrupt request pins. On-chip interrupt requests may be connected to any of the 6 lines.
IRQOUT6/DRQIN1	I/O	Interrupt request line to the ISA bus or DMA request line from on-board logic.
IRQOUT7/DACKOUT1* (Note 1)	O	Interrupt request line to the ISA bus or DMA ackowledge for on-board logic.
IRQIN<1:0>	I	Interrupt request from on-board logic.
DRQIN0/IOCS2* (Note 1)	I/O	DMA request from on-board logic or IOCS2 depending on mode selected.
DACKOUT0*/IOCS3*	O	DMA Acknowledge for on-board logic or IOCS3 depending on mode selected.
ISADRQ<2:0>/IRQOUT<10:8>	O	Connection for three ISA bus DMA Request lines, or additional interrupt request lines depending on the mode selected.
ISADACK<2:0>* (Note 1)	I	DMA acknowledge from the ISA bus.
IOCS<1:0>* (Note 1)	O	Programmable chip selects to address on-board peripherals
MEMCS<1:0>* (Note 1)	O	Programmable chip selects to address on-board ROM/Memory.

Note 1: * Means active low signal

Connection Diagram (Continued)

Note 2: "OSC" clock from ISA Bus is fixed at a standard frequency of 14.318 MHz. NM95MS15 is designed and tested for this frequency. However NM95MS15 can handle frequencies up to 24 MHz though it is not 100% tested.

Pinout Details for the NM95MS15

Mode 00 = DMA Mode; Mode 01 = Extended Interrupt Mode; Mode 10 = Extended DMA Mode

Pin #		Pin Name	
TQFP	Mode "00"	Mode "01"	Mode "10"
1	RSTDRV	RSTDRV	RSTDRV
2	IOCS1*	IOCS1*	IOCS1*
3	IOCS0*	IOCS0*	IOCS0*
4	MEMCS1*	MEMCS1*	MEMCS1*
5	MEMCS0*	MEMCS0*	MEMCS0*
6	SMEMR*	SMEMR*	SMEMR*
7	SMEMW*	SMEMW*	SMEMW*
8	IOWR*	IOWR*	IOWR*
9	IORD*	IORD*	IORD*
10	V_{CC}	V_{CC}	V_{CC}
11	DRQIN0	IOCS2*	DRQIN0
12	DACKOUT0*	IOCS3*	DACKOUT0*
13	GND	GND	GND
14	IRQIN1	IRQIN1	IRQIN1
15	IRQIN0	IRQIN0	IRQIN0
16	IRQOUT5	IRQOUT5	IRQOUT5
17	IRQOUT6	IRQOUT6	DRQIN1
18	IRQOUT7	IRQOUT7	DACKOUT1*
19	IRQOUT4	IRQOUT4	IRQOUT4
20	IRQOUT3	IRQOUT3	IRQOUT3
21	IRQOUT2	IRQOUT2	IRQOUT2
22	IRQOUT1	IRQOUT1	IRQOUT1
23	IRQOUT0	IRQOUT0	IRQOUT0
24	ISADRQ0	IRQOUT8 (Note 4)	ISADRQ0
25	ISADRQ1	IRQOUT9 (Note 4)	ISADRQ1
26	ISADRQ2	IRQOUT10 (Note 4)	ISADRQ2
27	ISADACK0*	NC	ISADACK0*
28	ISADACK1*	NC	ISADACK1*
29	ISADACK2*	NC	ISADACK2*
30	CS	CS	CS
31	SK	SK	SK
32	SA0	SA0	SA0

Pin #		Pin Name	
TQFP	Mode "00"	Mode "01"	Mode "10"
33	SA1	SA1	SA1
34	SA2	SA2	SA2
35	SA3	SA3	SA3
36	SA4	SA4	SA4
37	GND	GND	GND
38	SA5	SA5	SA5
39	SA6	SA6	SA6
40	SA7	SA7	SA7
41	SA8	SA8	SA8
42	SA9	SA9	SA9
43	SA10	SA10	SA10
44	SA11	SA11	SA11
45	SA12	SA12	SA12
46	SA13	SA13	SA13
47	SA14	SA14	SA14
48	SA15	SA15	SA15
49	SA16	SA16	SA16
50	SA17	SA17	SA17
51	DI	DI	DI
52	DO	DO	DO
53	SA18	SA18	SA18
54	SA19	SA19	SA19
55	AEN	AEN	AEN
56	OSC	OSC	OSC
57	SD0	SD0	SD0
58	SD1	SD1	SD1
59	SD2	SD2	SD2
60	SD3	SD3	SD3
61	SD4	SD4	SD4
62	SD5	SD5	SD5
63	SD6	SD6	SD6
64	SD7	SD7	SD7

Note 3: Mode selection (00, 01 or 10) is done by setting MS bits in the EEPROM configuration register. Detailed information about this is described in User's Guide.

Note 4: In Mode "01", IRQOUT8, 9, 10 are hardwired to ISA Bus interrupts IRQ10, IRQ11, IRQ12 respectively. This information supercedes the description in the "NM95MS15 User's Guide".

Absolute Maximum Ratings (Note 5)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltages with Respect to Ground	V_{CC} + 1V to -0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V Min

Operating Conditions

Ambient Operating Temperature NM95MS15	0°C to +70°C
Positive Power Supply (V_{CC})	4.5V to 5.5V

DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min (Note 6)	Typ	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		6	20	mA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.2	15	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}			15	µA
V_{IL}	Input Low Voltage			-0.1	0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1.0	V
V_{OL}	Output Low Voltage	I_{OL} = 24 mA (Note 8) I_{OL} = 2.1 mA (Note 9)		0.4	V	
V_{OH}	Output High Voltage	I_{OH} = -3 mA (Note 8) I_{OH} = -400 µA (Note 9)	2.4 2.4		V V	

Capacitance T_A = +25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Conditions	Max	Units
$C_{I/O}$ (Note 7)	Input/Output Capacitance	$V_{I/O}$ = 0V	8	pF
C_{IN} (Note 7)	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT} (Note 7)	Output Capacitance	V_{OUT} = 0V	6	pF

Note 5: Stresses above those listed under ≤Absolute Maximum Ratings≤ may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 6: Typical values are for T_A = 25°C and nominal supply voltage (5V).

Note 7: This parameter is periodically sampled and not 100% tested.

Note 8: These values are for ISA signals SD[0:7], IRQx, DRQx.

Note 9: These values are for card signal IOCS[0:3]*, MEMCS[0:1]*, DO(EEPROM).

AC Electrical Characteristics

Symbol	Parameter	Min	Max	Unit
t_{AEN}	AEN Valid to Command Active	100		ns
t_{AC}	Address Valid to Command Active	88		ns
t_{RVD}	Active Read to Valid Data		200	ns
t_{AH}	Address, AEN Hold from Inactive Command	30		ns
t_{RDH}	Read Data Hold from Inactive Read		5	ns
t_{WD}	Write Data Valid before Write Active	22		ns
t_{WDH}	Write Data Hold after Write Inactive	25		ns
t_{CSA}	Chip Selects Valid from Address Valid	5	25	ns
t_{CSC}	Chip Selects Valid from Command Active	5	25	ns
t_{IDD}	Propagation Delay for IRQ/DRQ/DACK	5	25	ns

Resource Allocation Amongst the Two Logical Devices

NM95MS15 supports two Plug n Play logical devices: Logical Device #0, and Logical Device #1. The total resource structure supported by the NM95MS15 is allocated to each of these logical devices as follows:

Mode "00"

	Logical Device #0	*Logical Device #1*
1) I/O chipselects	IOCS0*	IOCS1*
2) Memory chipselects	MEMCS0*	MEMCS1*
3) Local IRQ input	IRQIN0	IRQIN1
4) Local DQR input	DRQIN0	——

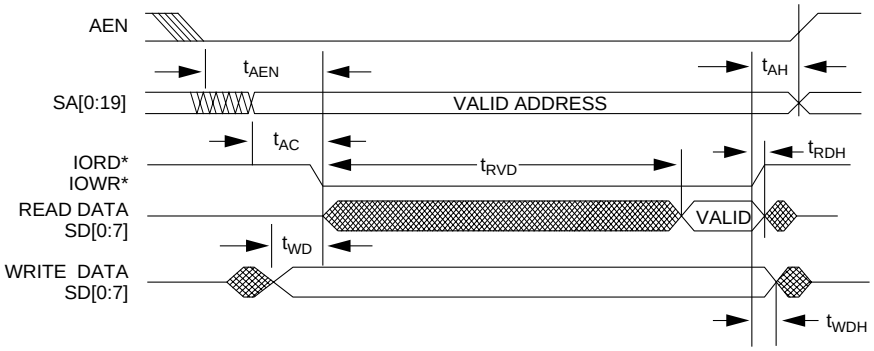
Mode "01"

	Logical Device #0	*Logical Device #1*
1) I/O chipselects	IOCS0* and IOCS2*	IOCS1* and IOCS3*
2) Memory chipselects	MEMCS0*	MEMCS1*
3) Local IRQ input	IRQIN0	IRQIN1

Mode "10"

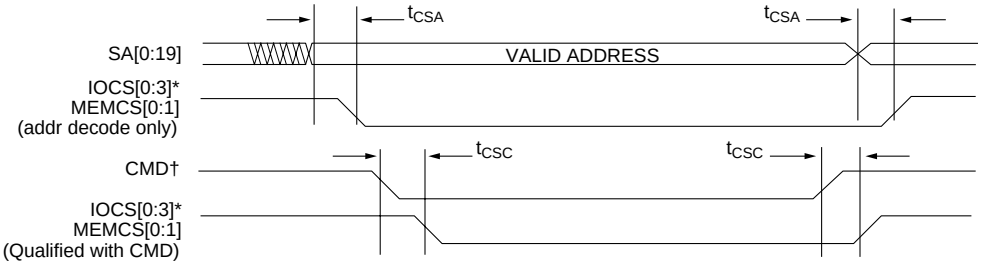
	Logical Device #0	*Logical Device #1*
1) I/O chipselects	IOCS0*	IOCS1*
2) Memory chipselects	MEMCS0*	MEMCS1*
3) Local IRQ input	IRQIN0	IRQIN1
4) Local DQR input	DRQIN0	DRQIN1

(1) Timings for ISA Read/Write Cycle



DS012394-3

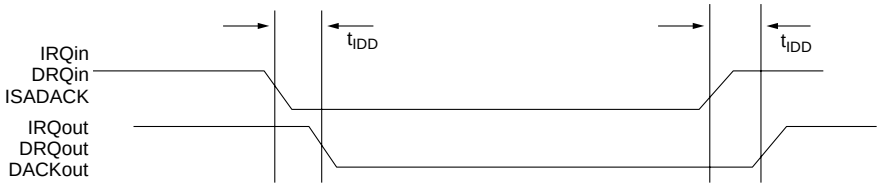
(2) Decode Delay for Chip select Generation



DS012394-4

Note: CMD† means IORD*, IOWR*, SMEMR* and SMEMW*

(3) Propagation Delay for IRQ/DRQ/DACK



DS012394-5

INTRODUCTION

The NM95MS15 is a single-chip solution for the ISA Plug and Play (PnP) specification. It implements the complete state machine and the necessary logic for supporting configurable Interrupts and DMA channels on the ISA bus for one logical device. Apart from providing "PnP" capability, it has built-in EEPROM that eliminates external EEPROM. This device is available in a space saving 64-pin Thin Quad Flat Pack (TQFP) package.

Functional Description

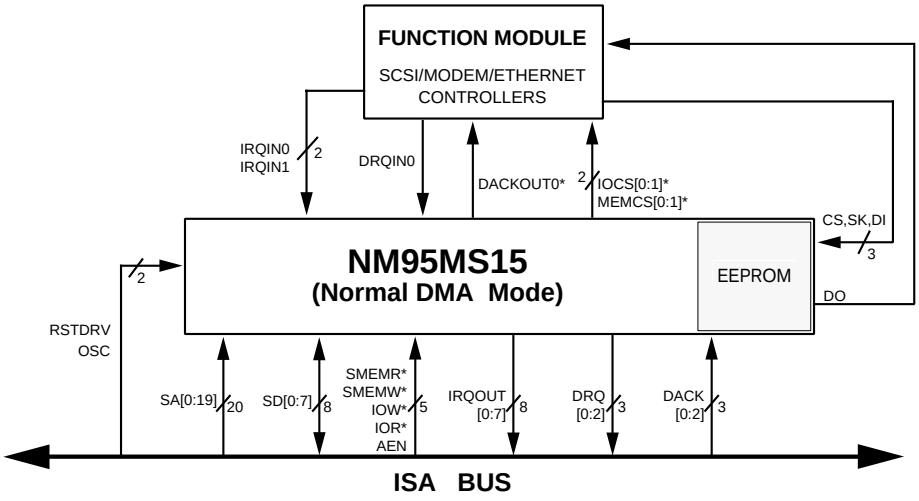
NM95MS15 has three modes of operation, viz, "Normal DMA mode", "Extended Interrupt Mode" and "Extended DMA mode". These modes are programmed using the mode select (MS) bits in one of the configuration registers (Refer to the User's guide for detailed information). Each of these modes are discussed below.

Normal DMA Mode

In the Normal DMA mode, support is provided for

1. One on-board DMA request that is switchable to any three DMA channels on the ISA bus.
2. Two on-board interrupt request lines switchable to any eight IRQ lines on the ISA bus.
3. Two programmable I/O chip selects for on-board logic.
4. Two programmable Memory chip selects for on-board logic.

Figure 1 shows a Block Diagram of NM95MS15 configured for Normal DMA Mode.



DS012394-6

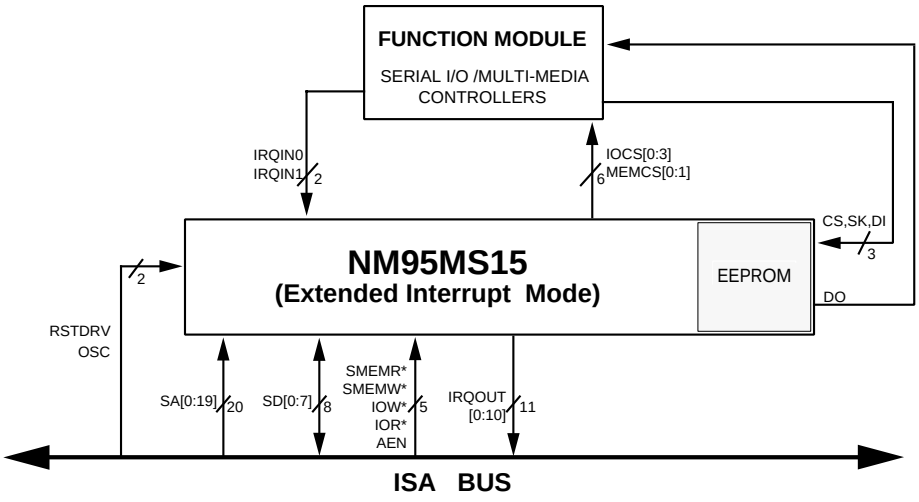
FIGURE 1.

Extended Interrupt Mode

In the Ext. Int mode, support is provided for:

1. Two on-board interrupt request lines switchable to any eleven IRQ lines on the ISA bus.
2. Four programmable I/O chip selects for on-board logic.
3. Two programmable Memory chip selects for on-board logic.

Figure 2 shows a Block Diagram of NM95MS15 configured for Extended Interrupt Mode.



DS012394-7

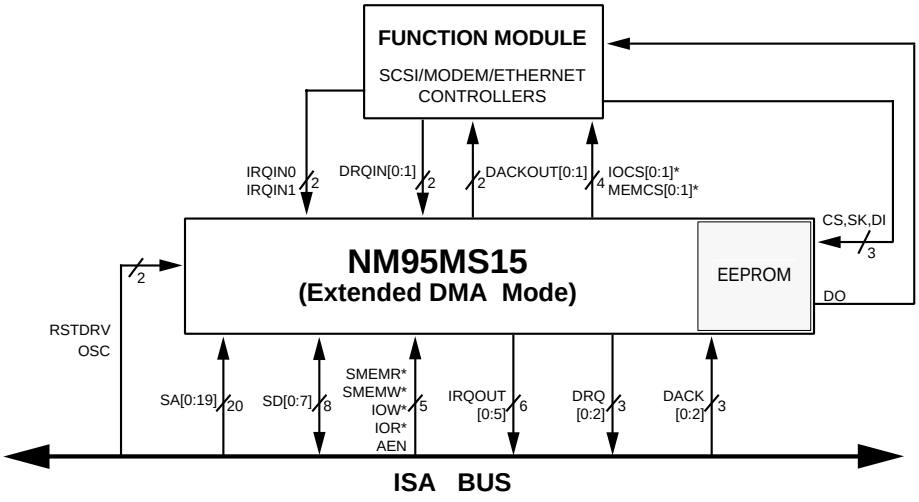
FIGURE 2.

Extended DMA Mode

In the Extended DMA mode, support is provided for:

1. Two on-board DMA request that is switchable to any three DMA channels on the ISA bus.
2. Two on-board interrupt request lines switchable to any six IRQ lines on the ISA bus.
3. Two programmable I/O chip selects for on-board logic.
4. Two programmable Memory chip selects for on-board logic.

Figure 3 shows a Block Diagram of NM95MS15 configured for Extended DMA Mode.



DS012394-8

FIGURE 3.

Chip Select Generation

Individual I/O or Memory chip select can be generated in the following two ways:

A) Address Decode only

B) Address Decode qualified by Command (IORD*, IOWR* or SMEMR*, SMEMW*).

On-Chip EEPROM

NM95MS15 has 8k bits of EEPROM on chip. All the PnP resource data structure for the logical device is stored in this EEPROM. Of the 8k bits, 4k bits are available for the logical device's external usage. The logical device can access the EEPROM through a microwire port, which is essentially a 4-wire serial bus. The pins CS, SK, DI & DO follow the exact timing as the standard microwire bus and are compatible to the NM93Cxx family of EEPROMs.

EEPROM Programming

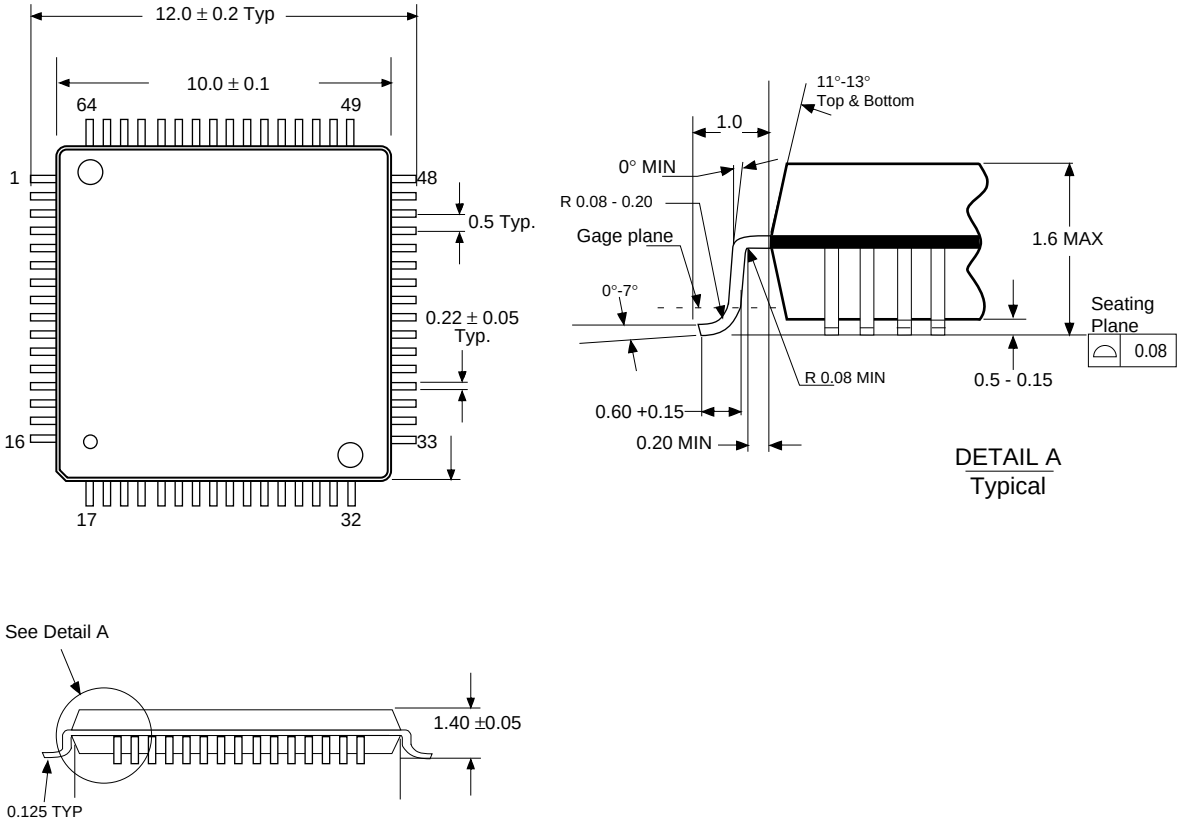
The entire 8k bits of EEPROM can be programmed throughthe ISA bus. The EEPROM can be programmed by puttingthe device (NM95MS15) in the Configuration state (as definedin the PnP standard). Under this state 4 registers at address 0xF0–0xF3 are accessible to program the EEPROM. The data to be programmed is loaded in register at address 0xF3 and 0xF2 (LSB and MSB

Ninth bit of address for 8k bits of memory is provided through the register at address 0xF0. Both read write are possible. The actual operation does not begin until Go Ahead (GA) bit is set. Programming a word takes approximately 10 ms. The status of the operation can be polled by the Status bit. This bit is set when the operation is in progress and will be reset when complete. The register at address 0xF0 is the COMMAND register. This is the handshake register in programming the EEPROM and is explained below in a tabular format.

COMMAND register	0xF0	Bit[1:0]	- OP Code bits 10 - Read operation 01 - Write operation
		Bit[2]	GA(Go ahead bits) If set to 1 the programming will continue.
		Bit[6:3]	- Reserved, should be 0.
		Bit[7]	- It provides A8 of the address. A[0:7] is provided by 0xF1 reg. (Note 10)
STATUS register	0x05	Bit[0]	- Status/Busy bit during programming "0" is busy, "1" is done.
Address Register	0xF1	Address Register [A0–A7]	
Data Register	0xF2	Data Byte [MSB]	
Data Register	0xF3	Data Byte [LSB]	

Note 10: The PNP resource data portion of the internal memory is at high address. Hence to program that portion, bit [7] of register 0xF0 (A8) should be set to 1.

Physical Dimensions inches (millimeters) unless otherwise noted



TQFP Packages (VEH)
Order Number NM95MS15VEH
Package Number VEH64A

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FAIRCHILD SEMICONDUCTOR™

July 1998

NM95MS16
Plug and Play Front-End Devices for ISA-BUS Systems

General Description

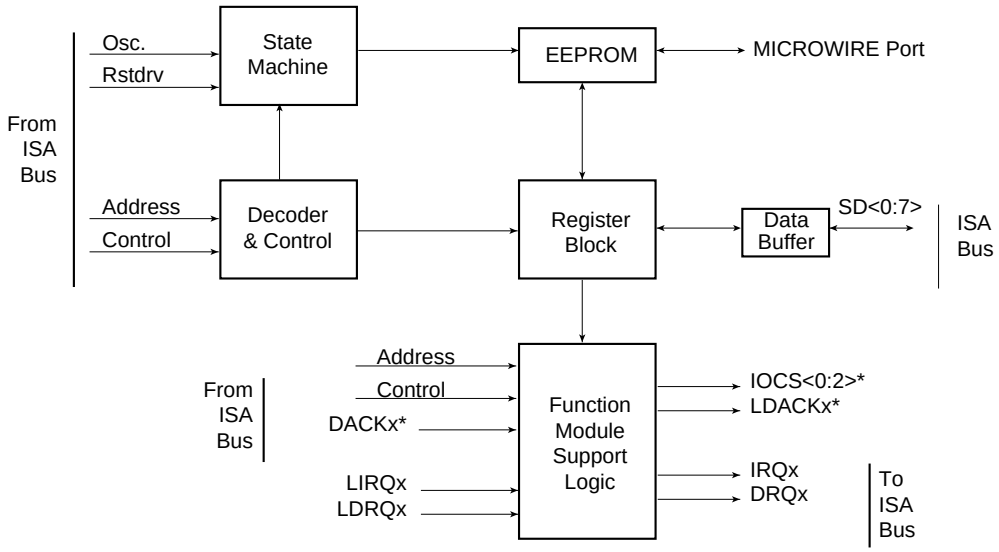
The NM95MS16 is the smaller of a family of devices designed to provide complete Plug and Play Capability for ISA bus systems. The NM95MS16 includes the necessary state machine logic to manage the Plug and Play protocol in addition to switches for steering Interrupt and DMA requests. It also features a built-in 2 kbits of serial EEPROM for storing the resource data specified in the Plug and Play Standard. In addition, 4 kbits of EEPROM is available for use by other on-board logic. This device provides a "truly complete" single-chip solution for implementing Plug and Play on ISA-Bus Adapter cards. The NM95MS16 supports one logical device with a flexible choice of DMA/IRQ selection and I/O Chipselect generation as well as offering 16-bit addressing in Mode 1.

NM95MS16 is implemented using Fairchild's Advanced CMOS process and operates single power supply. The NM95MS16 is available in a 48-pin TQFP package and 52-pin PLCC package.

Features

- Complete Implementation of Plug and Play Standard
  - Direct interface to ISA bus
- Two modes of operation
  - DMA mode
  - Extended Interrupt mode (**Windows® 95 logo** compatible)
- 6 or 8 ISA bus interrupt lines and 2 DRQ/DACK lines supported
- On-chip EEPROM for resource request table
- Additional 4 kbits of on-chip EEPROM available for external access
- 24 mA Drivers for Data outputs
- Complete compliance to ISA PnP specification (Ver. 1.0A)
- 48-Pin TQFP, and 52-Pin PLCC Packages

Block Diagram

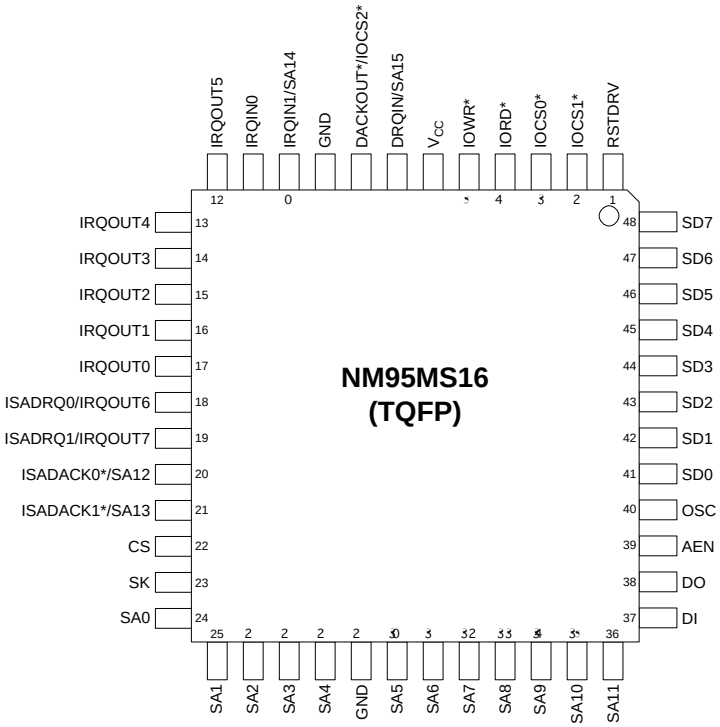


DS012601-1

Windows® 95 is a registered trademark of Microsoft Corporation.

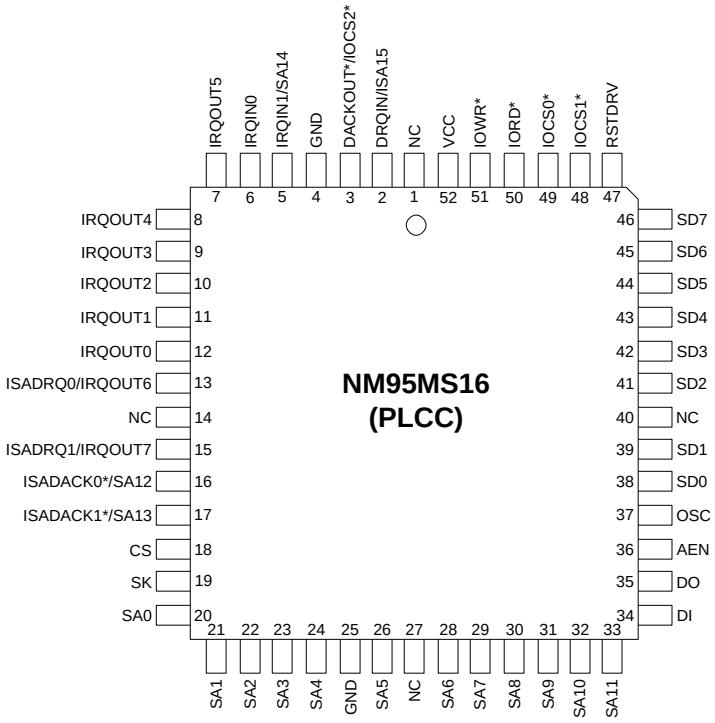
Connection Diagrams

Commercial Temperature Range (0°C to +70°C)



DS012601-2

Order Number NM95MS16VBH



DS012601-3

Order Number NM95MS16V

Connection Diagrams (Continued)

Signals	Type	Description
SA<11:0>	I	Address inputs from the ISA bus.
IORD*	I	I/O read strobe from the ISA bus.
IOWR*	I	I/O write strobe from the ISA bus.
AEN	I	Address Enable from ISA Bus —used in conjunction with DMA.
SD<7:0>	I/O	Data bus —lower byte —from/to the ISA bus.
OSC (Note 1)	I	"OSC" clock from the ISA bus —used for internal state machines.
RSTDRV	I	Reset input from the ISA bus.
CS	I	Chip select for Microwire port. **There should be a pull down resistor of 4.7k** on CS pin if unused externally, or directly connected to GND.
SK, DI	I	Clock and Data input lines for Microwire bus connection to access a portion (4k) on chip EEPROM.
DO	O	Data output line for the Microwire interface detailed above.
IRQOUT<5:0>	O	Connection to ISA bus interrupt request pins. On-chip interrupt request(s) may be connected to any 6 of the ISA IRQ lines.
IRQIN<1:0>	I	Interrupt request from on-board logic
DRQin/SA<15>	I	DMA request from on-board logic, or Address input from ISA bus depending on mode selected.
DACKOUT* /IOCS2*	O	DMA Acknowledge for on-board logic or Programmable chipselect (2) depending on mode selected.
ISADRQ<1:0>/IRQOUT<7:6>	O	Connection for two ISA bus DMA Request lines, or additional interrupt request lines depending on the mode selected.
ISADACK<1:0>*/SA<13:12>	I	DMA Acknowledge from the ISA bus or additional address lines depending on the mode selected.
IOCS<1:0>*	O	Programmable chip selects to address on-board peripheral.
IRQIN<1>/SA<14>	I	Interrupt request from on board logic or Address input from ISA bus depending on mode selected.

Signal name with a "" means its an active low signal.

Note 1: "OSC" clock from ISA Bus is fixed at a standard frequency of 14.318 MHz. NM95MS16 is designed and tested for 14.318 MHz. However NM95MS16 can handle frequencies up to 24 MHz though it is not 100% tested.

Pinout Details for the NM95MS16

Mode 00 = DMA Mode; Mode 01 = Extended Interrupt Mode

TQFP Pin	DMA Mode	Ext.Intr.Mode
1	RSTDRV	RSTDRV
2	IOCS1*	IOCS1*
3	IOCS0*	IOCS0*
4	IORD*	IORD*
5	IOWR*	IOWR*
6	V_{CC}	V_{CC}
7	DRQIN	SA15
8	DACKOUT*	IOCS2*
9	GND	GND
10	IRQIN1	SA14
11	IRQIN0	IRQIN0
12	IRQOUT5	IRQOUT5
13	IRQOUT4	IRQOUT4
14	IRQOUT3	IRQOUT3
15	IRQOUT2	IRQOUT2
16	IRQOUT1	IRQOUT1
17	IRQOUT0	IRQOUT0
18	ISADRQ0	IRQOUT6
19	ISADRQ1	IRQOUT7
20	ISADACK0*	SA12
21	ISADACK1*	SA13
22	CS	CS
23	SK	SK
24	SA0	SA0

TQFP Pin	DMA Mode	Ext.Intr.Mode
25	SA1	SA1
26	SA2	SA2
27	SA3	SA3
28	SA4	SA4
29	GND	GND
30	SA5	SA5
31	SA6	SA6
32	SA7	SA7
33	SA8	SA8
34	SA9	SA9
35	SA10	SA10
36	SA11	SA11
37	DI	DI
38	DO	DO
39	AEN	AEN
40	OSC	OSC
41	SD0	SD0
42	SD1	SD1
43	SD2	SD2
44	SD3	SD3
45	SD4	SD4
46	SD5	SD5
47	SD6	SD6
48	SD7	SD7

Note: Mode selection (00 or 01) is done by setting MS bits in the EEPROM configuration register. Detailed information about this is described in User's Guide.

Absolute Maximum Ratings (Note 2)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltages with Respect to Ground	V_{CC} + 1V to -0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V Min

Operating Conditions

Ambient Operating Temperature NM95MS16	0°C to +70°C
Positive Power Supply (V_{CC})	4.5V to 5.5V

DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 3)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz			15	mA
I_{LI}	Input Leakage Current	V_{IN} = GND or V_{CC}		0.2	15	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}			15	µA
V_{IL}	Input Low Voltage		-0.1	0.8	V	
V_{IH}	Input High Voltage		2.0		V_{CC} + 1.0	V
V_{OL}	Output Low Voltage	I_{OL} = 24 mA (Note 5) I_{OL} = 2.1 mA (Note 6)			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -3 mA (Note 5) I_{OH} = -400 µA (Note 6)	2.4 2.4			V V

Capacitance T_A = +25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Conditions	Max	Units
CI/O (Note 4)	Input/Output Capacitance	VI/O = 0V	8	pF
CIN (Note 4)	Input Capacitance	VIN = 0V	6	pF
COUT (Note 4)	Output Capacitance	VOUT = 0V	6	pF

Note 2: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 3: Typical values are for T_A = 25°C and nominal supply voltage (5V).

Note 4: This parameter is periodically sampled and not 100% tested.

Note 5: These values are for ISA signals like SD[0:7], IRQx, DRQx.

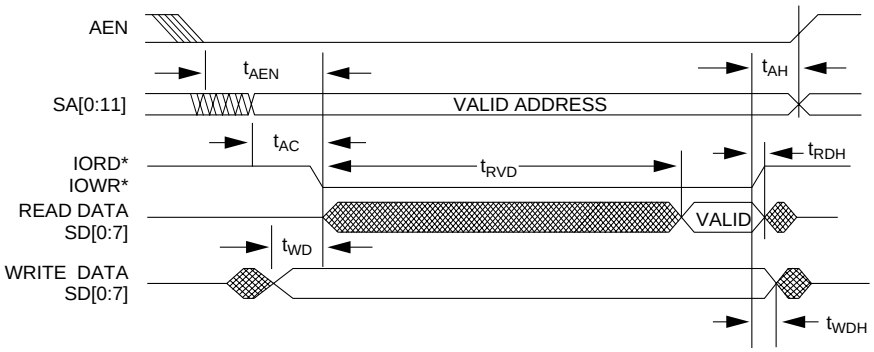
Note 6: These values are for card signal like IOCS[0:3]*, DO(EEPROM).

AC Electrical Characteristics

Symbol	Parameter	Min	Max	Unit
t_{AEN}	AEN Valid to Command Active	100		ns
t_{AC}	Address Valid to Command Active	88		ns
t_{RVD}	Active Read to Valid Data		200	ns
t_{AH}	Address, AEN Hold from Inactive Command	30		ns
t_{RDH}	Read Data Hold from Inactive Read		5	ns
t_{WD}	Write Data Valid before Write Active	22		ns
t_{WDH}	Write Data Hold after Write Inactive	25		ns
t_{CSA}	Chip Selects Valid from Address Valid	5	25	ns
t_{CSC}	Chip Selects Valid from Command Active	5	25	ns
t_{IDD}	Propagation Delay for IRQ/DRQ/DACK	5	25	ns

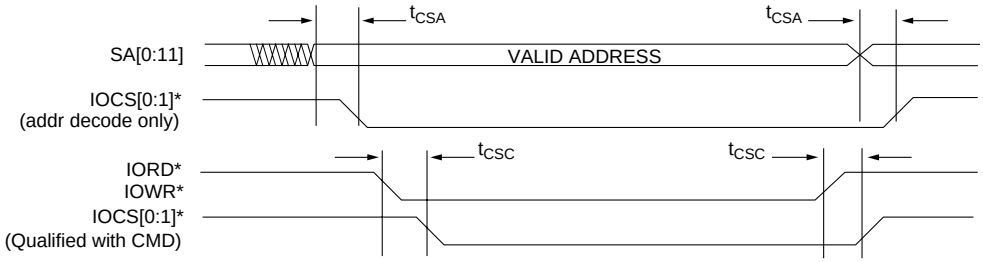
Timing Diagrams

Timings for ISA Read/Write Cycle



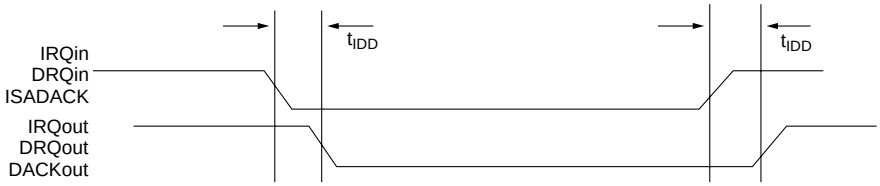
DS012601-4

Decode Delay for Chipselect Generation



DS012601-5

Propagation Delay for IRQ/DRQ/DACK



DS012601-6

INTRODUCTION

The NM95MS16 is a single-chip solution for the ISA Plug and Play (PnP) specification. It implements the complete state machine and the necessary logic for supporting configurable Interrrupts and DMA channels on the ISA bus for one logical device. Apart from providing "PnP" capability, it has built-in EEPROM that eliminates external EEPROM. This device is available in a space saving 48-pin Thin Quad Flat Pack (TQFP) package.

Functional Description

NM95MS16 has two modes of operation, viz, "DMA mode" and "Extended Interrupt mode". These modes are programmed using the mode select (MS) bits in one of the configuration registers (Refer to the NM95MS16 User's guide for detailed information). Each of these modes are discussed below.

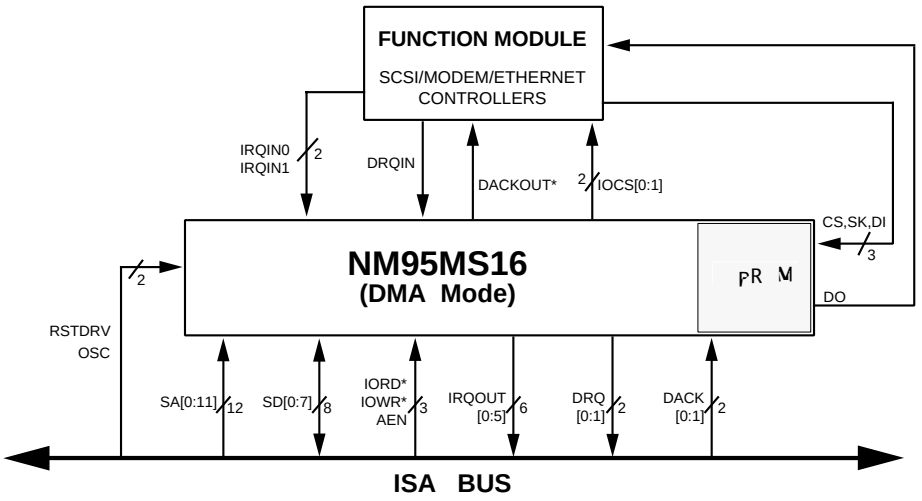
DMA Mode

In the DMA mode, support is provided for

1. One on-board DMA request that is switchable to any two DMA channels on the ISA bus.
2. Two on-board interrupt request lines switchable to any six IRQ lines on the ISA bus.
3. Two programmable I/O chip selects for on-board logic.

Figure 1 shows a Block Diagram of NM95MS16 configured for DMA Mode.

INTRODUCTION (Continued)



DS012601-7

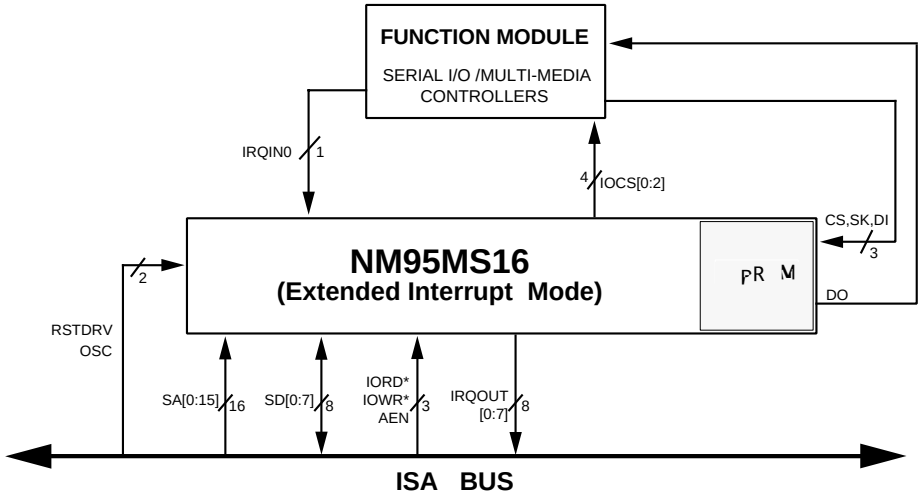
FIGURE 1.

Extended Interrupt Mode

In the Ext.Int. mode, support is provided for:

1. Two on-board interrupt request lines switchable to any eight IRQ lines on the ISA bus.
2. Three programmable I/O chip selects for on-board logic.
3. ISA address SA12–SA15 are also included for extended decode.

Figure 2 shows a Block Diagram of NM95MS16 configured for Extended Interrupt Mode.



DS012601-8

FIGURE 2.

Chipselect Generation

Individual I/O chipselect can be generated in the following two ways:

A) Address Decode only

B) Address Decode qualified by Command (IORD*, IOWR*).

On-Chip EEPROM

NM95MS16 has 6 kbits of EEPROM on chip. All the PnP resource data structure for the logical device is stored in this EEPROM. Of the 6 kbits, 4 kbits are available for the logical device's external usage. The logical device can access the EEPROM through a microwire port, which is essentially a 4-wire serial bus. The pins CS, SK, DI and DO follow the exact timing as the standard microwire bus and are compatible to the NM93Cxx family of EEPROMs.

INTRODUCTION (Continued)

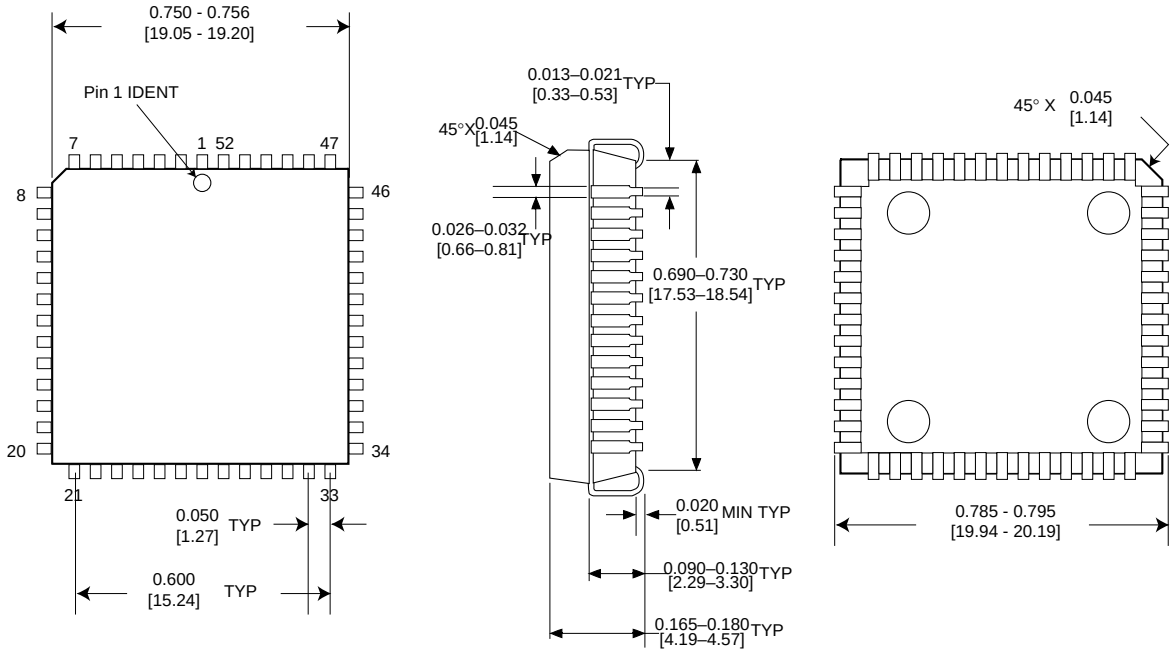
EEPROM Programming

The entire 6 kbits of EEPROM can be programmed through the ISA bus. The EEPROM can be programmed by putting the device (NM95MS16) in the Config. state (as defined in the PnP standard). Under this state 4 registers at address 0xF0–0xF3 are accessible to program the EEPROM. The data to be programmed is loaded in register at address 0xF3 and 0xF2 (LSB and MSB respectively). The address to be programmed is loaded in register at address 0xF1. The Ninth bit of address for 6 kbits of memory is provided through the register at address 0xF0. Both read write are possible. The actual operation does not begin until Go Ahead (GA) bit is set. Programming a word takes approximately 10 ms. The status of the operation can be polled by the Status bit. This bit is set when the operation is in progress and will be reset when complete. The register at address 0xF0 is COMMAND register. This is the handshake register in programming the EEPROM and is explained below in a tabular format.

COMMAND Register	0xF0	Bit[1:0] —OP Code bits 10 - Read operation 01 - Write operation 11 - Erase operation Bit[2] —GA(Go ahead bits) If set to 1 the programming will continue. Bit[6:3] —Reserved, should be 0. Bit[7] —It provides A8 of the address. A[0:7] is provided by 0xF1 reg. (Note 7)
Address Register	0xF1	AddressRegister [A0–A7]
Data Register	0xF2	Data Byte [MSB]
Data Register	0xF3	Data Byte [LSB]
STATUS Register	0x05	Bit[0] —Status/Busy bit. “0” if busy, “1” is done.

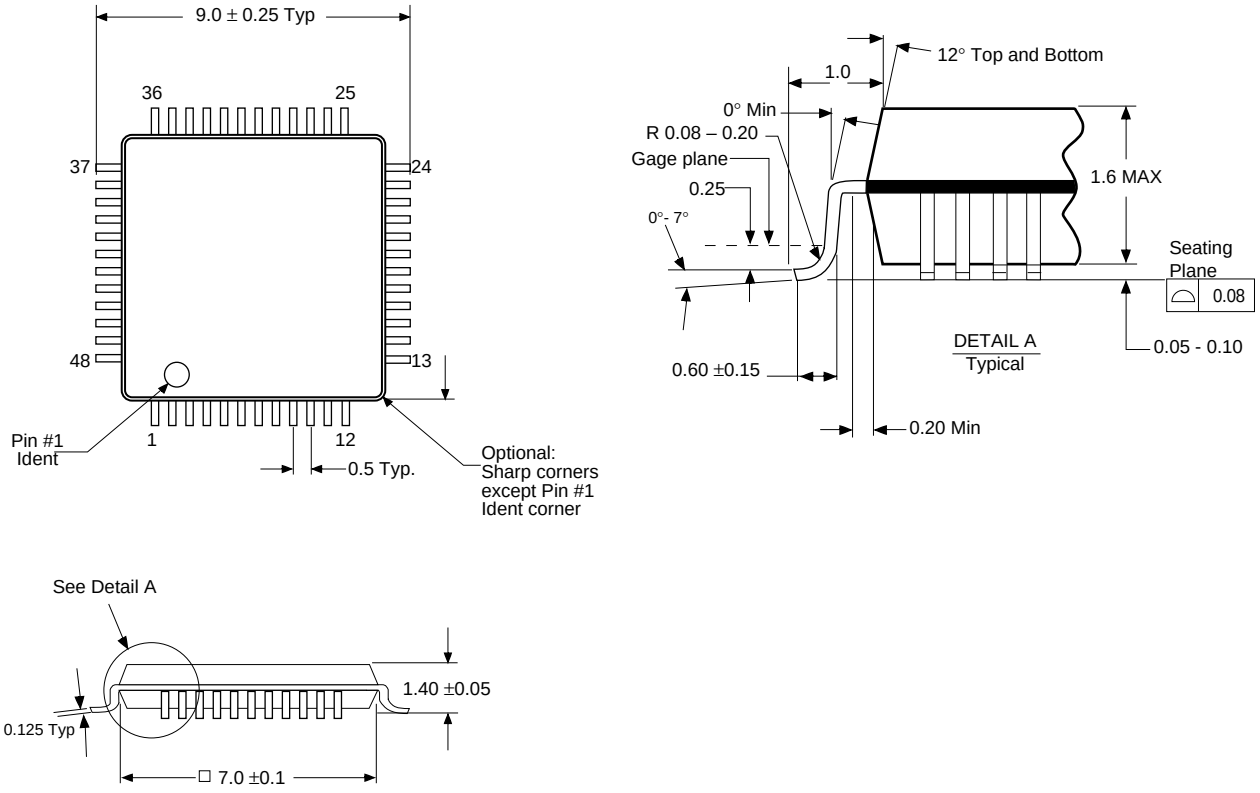
Note 7: The PNP resource data portion of the internal memory is at high address. Hence to program that portion, bit [7] of register 0xF0 (Address A8) should be set to “1”.

Physical Dimensions inches (millimeters) unless otherwise noted



52-Lead Molded Plastic Leaded Chip Carrier
Package Number V52A
Order Number NM95MS16V

Physical Dimensions inches (millimeters) unless otherwise noted



TQFP Package (VBH)
Package Number VBH48A
Order Number NM95MS16VBH

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FAIRCHILD SEMICONDUCTOR™

July 1998

NM95MS18
Plug & Play Front-end device for ISA-Bus Systems (Supports Windows®-NT, UNIX® and legacy systems)

General Description

The NM95MS18 is an industry standard ISA Plug-n-Play controller that also supports Non-Plug-n-Play platforms like DOS, WIN3.1x, Windows-NT and Unix.

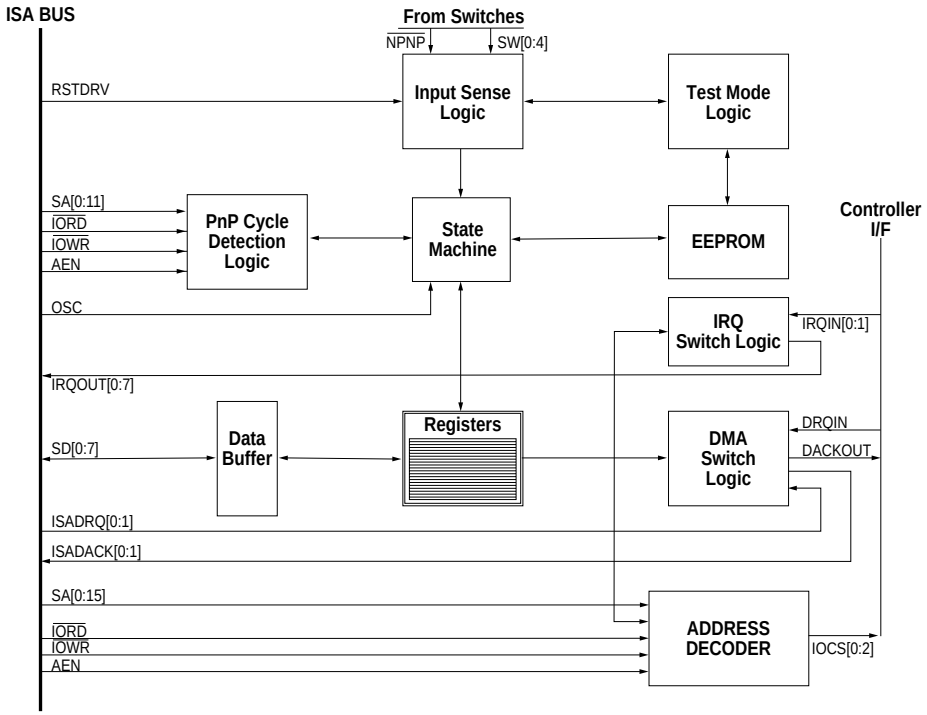
In additon to being completely compliant to ISA PnP Specification (Ver 1.0a), NM95MS18 integrates a total of 4Kbit of onchip EEPROM for both PnP Resource data as well as non-PnP configuration data to provide a true single chip solution.

NM95MS18 supports one logical device offering a flexible choice of DMA, Interrupt and I/O address decoding features within a single chip. NM95MS18 is implemented using Fairchild's Advanced CMOS process and operates on a single power supply.

Features

- Fully compliant with industry standard ISA PnP specification (Ver. 1.0a)
- Supports Non-PnP platforms like WINDOWS-NT, UNIX, DOS/WIN3.1x
  - — No configuration utilities needed
- Supports Non-PnP "legacy" mode
  - — Can be programmed to power-up in 31 settings
- On-chip "Write-Protected" EEPROM for:
  - — PnP Resource data (2Kbits)
  - — 31 Power-on "legacy" configurations (2Kbits)
- Two modes of operation:
  - — DMA Mode
  - — Extended Interrupt Mode (supports PC-97 requirements)
- Configurable Interrupt types:
  - — TTL O/P
  - — Open Drain O/P
- Supports Wire-AND I/O chipselects
- Fully compatible with NM95MS16
- Available in 52-Pin PLCC Package

Block Diagram



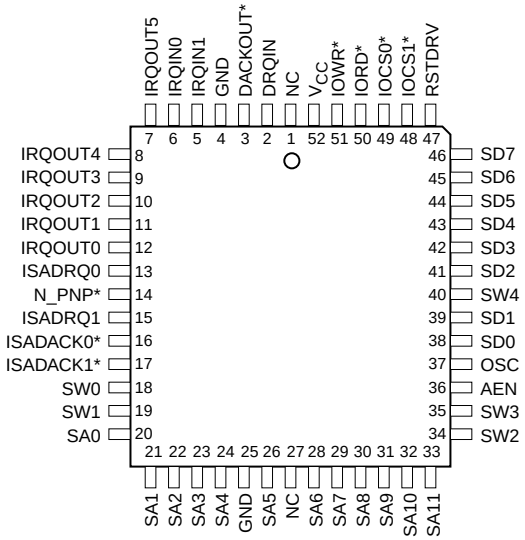
DS500033-1

Block Signal Description

Signal	Type	Description
SA[0:11]	I	Address inputs from the ISA bus.
SA[12:15]†	I	Address inputs from the ISA bus.
IORD*	I	I/O Read strobe from the ISA bus.
IOWR*	I	I/O Write strobe from the ISA bus.
AEN	I	Address Enable Strobe from ISA bus.
OSC	I	14.31818 MHz clock source from ISA bus.
RSTDRV	I	Reset signal from ISA bus.
SD[0:7]	I/O	ISA Data bus.
IRQIN0	I	Source Interrupt signal from onboard controller.
IRQIN1†	I	Source Interrupt signal from onboard controller.
IRQOUT[0:5]	O	Interrupt output signals from NM95MS18. Can be connected to any of ISA IRQ channels.
IRQOUT[6:7] †	O	Interrupt output signals from NM95MS18. Can be connected to any of ISA IRQ channels.
DRQIN†	I	Source DMA request signal from onboard controller to NM95MS18.
ISADRQ[0:1] †	O	DMA request output signals from NM95MS18. Can be connected to any of ISA DMA channels.
ISADACK[0:1]* †	I	DMA Acknowledge output signals from respective ISA DMA channels to which ISADRQ[0:1] are connected.
DACKOUT* †	I	DMA acknowledge signal from NM95MS18 to onboard controller.
IOCS[0:1]*	O	Programmable chipselects from NM95MS18 to onboard controller.
IOCS[2]* †	O	Programmable chipselects from NM95MS18 to onboard controller.
N_P 'N' P*	I	Input signal selecting either PNP mode or N_PNP mode of NM95MS18. This signal has a weak internal pull-up resistor defaulting to PnP mode and can be directly connected to ground . This signal is used in conjunction with SW[0:4] inputs. “1” - PNP mode. “0” - N_PNP mode.
SW[0:4]	I	Input signals to NM95MS18 selecting 1-out-of-31 Non-Plug-n-Play configurations. All these signals have a weak internal pull-up resistor and can be directly connected to ground. These signals are used in conjunction with N_PNP signal.

* Signal name with a “*” indicates active low signal.

† Multiplexed signals. Please refer Pinout Details.



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PLCC Pins

Pinout Details for NM95MS18 (PLCC Package)

Pin #	Pin Name	
Mode	DMA	Ext. Intr
1	NC	NC
2** (Note 3)	DRQIN	SA15
3**	DACKOUT*	IOCS2*
4	GND	GND
5**	IRQIN1	SA14
6	IRQIN0	IRQIN0
7	IRQOUT5	IRQOUT5
8	IRQOUT4	IRQOUT4
9	IRQOUT3	IRQOUT3
10	IRQOUT2	IRQOUT2
11	IRQOUT1	IRQOUT1
12	IRQOUT0	IRQOUT0
13**	ISADRQ0	IRQOUT6
14	N_PnP	N_PnP
15**	ISADRQ1	IRQOUT7
16**	ISADACK0*	SA12
17**	ISADACK1*	SA13
18	SW0	SW0
19	SW1	SW1
20	SA0	SA0
21	SA1	SA1
22	SA2	SA2
23	SA3	SA3
24	SA4	SA4
25	GND	GND
26	SA5	SA5

Pin #	Pin Name	
Mode	DMA	Ext. Intr
27	NC	NC
28	SA6	SA6
29	SA7	SA7
30	SA8	SA8
31	SA9	SA9
32	SA10	SA10
33	SA11	SA11
34	SW2	SW2
35	SW3	SW3
36	AEN	AEN
37	OSC	OSC
38	SD0	SD0
39	SD1	SD1
40	SW4	SW4
41	SD2	SD2
42	SD3	SD3
43	SD4	SD4
44	SD5	SD5
45	SD6	SD6
46	SD7	SD7
47	RSTDRV	RSTDRV
48	IOCS1*	IOCS1*
49	IOCS0*	IOCS0*
50	IORD*	IORD*
51	IOWR*	IOWR*
52	V_{CC}	V_{CC}

** Pins with multiplexed signals

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltages with Respect to Ground	V_{CC} + 1V to –0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min.

Operating Conditions

Ambient Operating Temperature NM95MS18	0°C to +70°C
Positive Power Supply (V_{CC})	4.5V to 5.5V

Note 1: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook sepcifications.

DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 2)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		TBD	10.0	mA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.2	1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}			1.0	µA
V_{IL}	Input Low Voltage			-0.1	0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1.0	V
V_{OL}	Output Low Voltage	I_{OL} = 24 mA (Note 4) I_{OL} = 2.1 mA (Note 5)			0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = -3 mA (Note 4) I_{OH} = -400 µA (Note 5)	2.4 2.4			V V

Capacitance T_A = +25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test Conditions	Min	Max	Units
$C_{I/O}$ (Note 3)	Input/Output Capacitance	$V_{I/O}$ = 0V	8	pF
C_{IN} (Note 3)	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT} (Note 3)	Output Capacitance	V_{OUT} = 0V	6	pF

Note 2: Typical values are for T_A = 25°C and nominal supply voltage (5V).

Note 3: This parameter is periodically sampled and not 100% tested.

Note 4: These values are for ISA signals like SD[0:7], IRQx, DRQx.

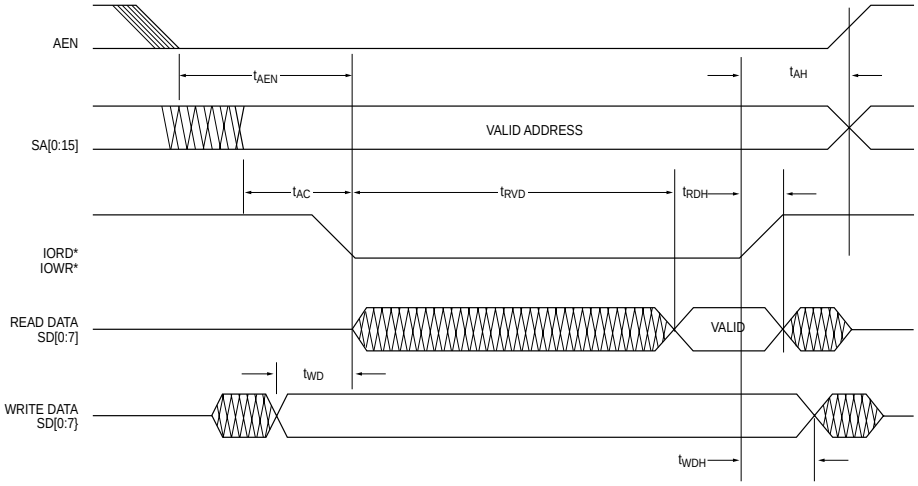
Note 5: These values are for card signal like IOCS[0:2]*, DO(EEPROM)

AC Electrical characteristics

Symbol	Parameter	Min	Max	Unit
t_{AEN}	AEN valid to command active	100		ns
t_{AC}	Address valid to command active	88		ns
t_{RVD}	Active read to valid data		150	ns
t_{AH}	Address, AEN hold from inactive command	30		ns
t_{RDH}	Read data hold from inactive read		5	ns
t_{WD}	Write data valid before write active	22		ns
t_{WDH}	Write data hold after write inactive	25		ns
t_{CSA}	Chip selects valid from address valid	5	20	ns
t_{CSC}	Chip selects valid from command active	5	20	ns
t_{IDD}	Propagation delay for IRQ/DRQ/DACK	5	20	ns

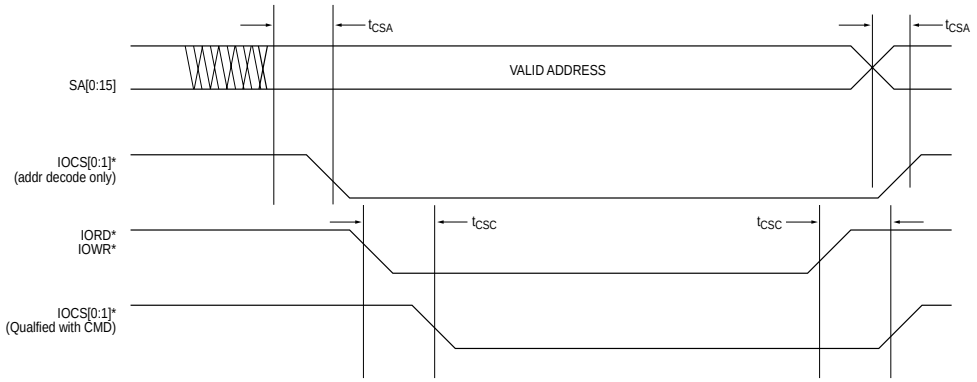
Timing Diagrams

Timings for ISA Read/Write Cycle



DS500033-3

Decode Delay for Chipselect Generation



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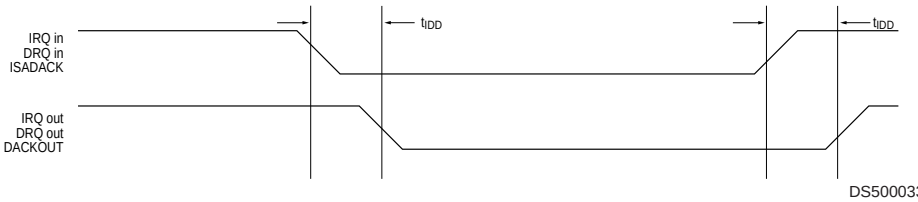
Propagation Delay for IRQ/DRQ/DACK



DS500033-5

INTRODUCTION

NM95MS18 supports both Plug-n-Play platforms (PC with WINDOWS-95 and/or PnP BIOS) as well as Non-Plug-n-Play platforms (PC with WINDOWS-NT, Win3.x/DOS and Non-PnP BIOS). The choice of interface (PnP or Non-PnP) is selected by using a single pin (N_PnP*). Under PnP interface, NM95MS18 is fully compliant with ISA Plug-n-Play specification (Ver 1.0a) and is functionally compatible to its predecessor NM95MS16. Under Non-P 'n' P interface, NM95MS18 powers-up active with a predetermined configuration eliminating any need for an external PnP configuration support. Five external inputs to NM95MS18 allows to choose the default power-up configuration from 31 different predetermined configurations. NM95MS18 integrates 2 kbits of on-board EEPROM to store all the 31 configuration information as well as an additional 2 kbits EEPROM area to store standard PnP resource information. Entire memory can be write protected. NM95MS18 also allows ISA interrupts to be shared.

Functional Description

As mentioned above, NM95MS18 can be configured for either Plug-n-Play environment or Non-Plug-n-Play environment. Under either interface, NM95MS18 provides a choice from 2 operating modes, viz, **DMA Mode** or **Extended Interrupt Mode** offering additional flexibility in selecting a suitable set of features for a particular application. Mode selection is made by setting appropriate bits in the "*I/O DECODE QUALIFICATION*" register in onboard EEPROM. Refer to "*NM95MS18 User's Guide*" for more detail. Each of these modes is explained below.

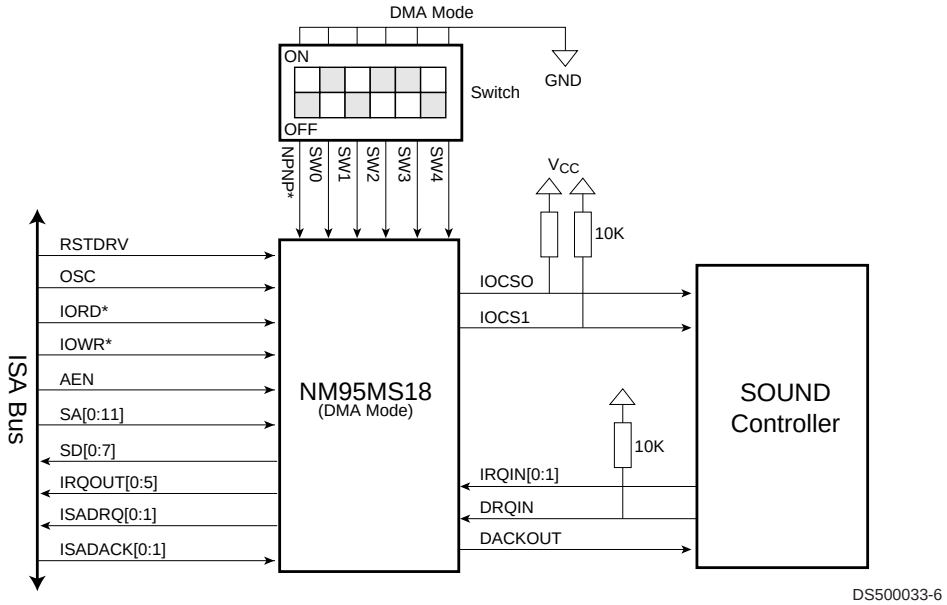
DMA Mode

In the DMA Mode, NM95MS18 provides the following features:

1. Two programmable I/O chipselects (IOCS0*and IOCS1*) each of which can be set to be decoded off of ISA address **SA[0:11]** and **IORD*/IOWR*** or just by **SA[0:11]**. In addition IOCS1* signal can be internally **Wire-ANDed** with IOCS0* signal, to provide "Output Enable" signal for ISA bus data buffers.
2. Two local Interrupt request signals switchable to any six IRQ channels on the ISA Bus. Choice of actual ISA IRQ channels selected is user dependent. Also the type of the six IRQ outputs can be independently set to be either **standard TTL type** or **Open-Drain type**. Selecting Open-Drain type allows interrupts to be shared on the ISA bus.
3. One local DMA request signal switchable to any two DMA channels on the ISA Bus. Choice of actual ISA DMA channels selected is user dependent.

Following figure shows a typical system block diagram of NM95MS18 used in DMA Mode.

DMA Mode



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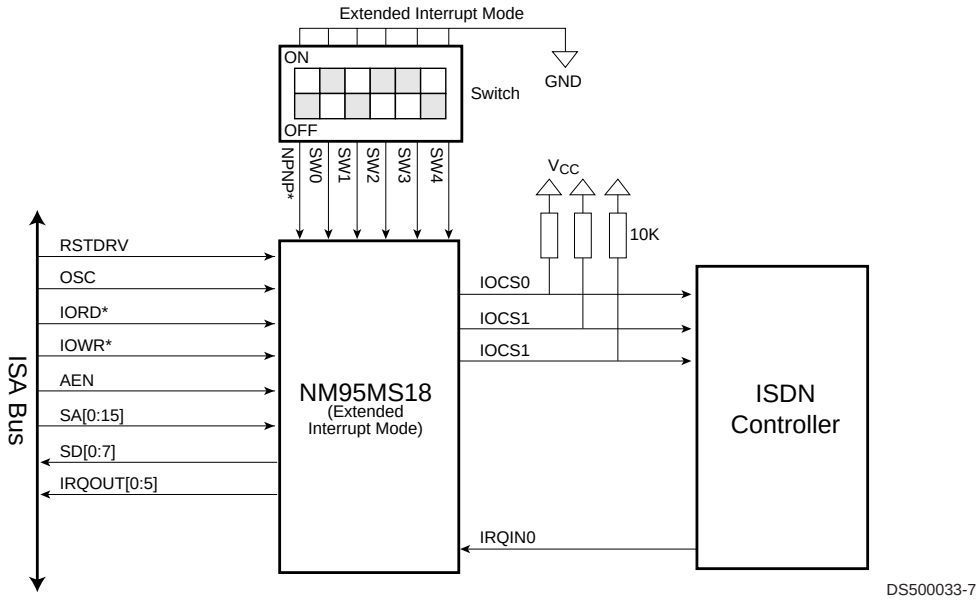
Extended Interrupt Mode (Supports PC-95/PC-97 Requirements)

In Extended Interrupt Mode, NM95MS18 provides these features:

1. Three programmable I/O chipselects (IOCS0*, IOCS1* and IOCS2*) each of which can be set to be decoded off of ISA address **SA[0:11]** and and **IORD*/IOWR*** or by just ISA address bus only. In addition IOCS1* and IOCS2* signals can be internally **Wire-ANDed** with IOCS0* signal, to provide "Output Enable" signal for ISA bus data buffers.
2. One on-board Interrupt request signals switchable to any eight IRQ channels on the ISA Bus. Choice of actual ISA IRQ channels selected is user dependent. Also the type of the eight IRQ outputs can be independently set to be either **standard TTL type** or **Open-Drain type**. Selecting Open-Drain type allows interrupts to be shared on the ISA bus.

Following figure shows a typical system block diagram of NM95MS18 used in Extended Interrupt Mode.

Extended Interrupt Mode (Supports PC-95/PC-97 Requirements)



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Interface Options of NM95MS18 Plug-n-Play/Non-Plug-n-Play)

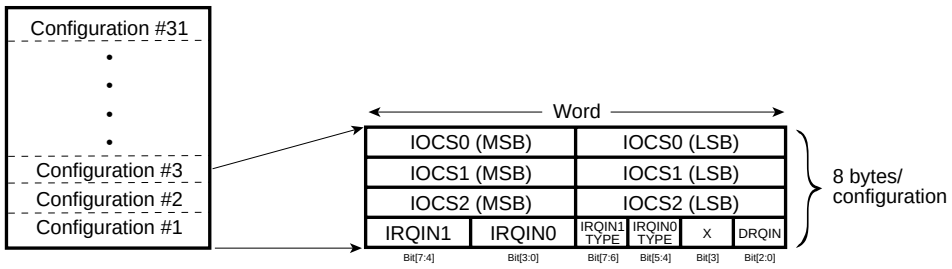
1) Plug-n-Play (PnP) Interface ("/N_PNP" = 1)

In a Plug-n-Play environment, a PnP configuration manager (typically PnP-BIOS, Windows'95 OS or PnP utility) that resides on the PC would read the *Plug-n-Play Resource data* fileand allocate the requested resource (I/O Address space, IRQ etc). PnP configuration is actually a defined process of updating defined PnP Registers on a PnP controller in a defined manner. The entire protocol and Register summary is provided in the ISA PnP Specification (Ver 1.0a). NM95MS18 is designed to be completely compliant with the existing ISA PnP standard and hence provides seamless PnP support for an ISA adapter. All that is required is to prepare the *Plug-n-Play Resource data* for an applicatDuring power-up, NM95MS18 defaults to Plug-n-Play interface if it senses logic "high" at the "N_PNP*" pin. This pin has an internal weak pullup logic and hence can be left unconnected for PnP interface.

2) Non-Plug-n-Play (legacy) Interface ("/N_PNP" = 0)

In a *legacy* interface NM95MS18 is designed to ignore the standard PnP configuration protocol and instead self-configure to a specific configuration. A specific configuration is selected by a set of switch inputs SW[0:4]. All possible combinations of these 5 inputs provide 31 configurations to choose from (the 32nd configuration is reserved for field programming. Refer section on "Software Write Configuration" for more detail). It is also possible to use fewer than five switch inputs (SW[0:3], SW[0:2], SW[0:1] or SW[0] to have fewer legacy configurations (15, 7, 3 or 1 respectively). All these five switch inputs have weak internal pull-up resistor allowing unused switch pins to be left unconnected when necessary.

During power-up, NM95MS18 defaults to Legacy interface if it senses logic "low" at the "N_P 'n' P*" pin. Along with "N_P 'n' P*" pin, the state of "SW[0:4]" inputs are also sensed to determine the particular legacy configuration that needs to be selected. Each legacy configuration occupies 8 bytes (4 Words) of internal memory as shown in the following figure.



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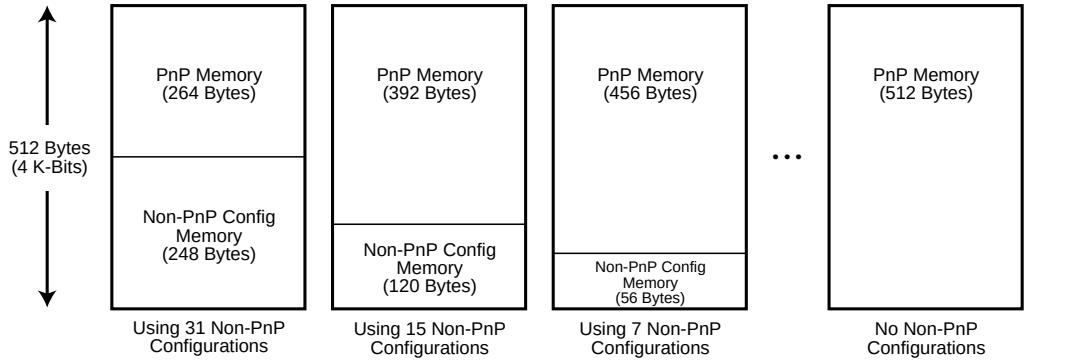
Interface Options of NM95MS18 (Plug-n-Play/Non-Plug-n-Play) (Continued)

Configuration #1 (first configuration) is stored at the bottom 8 bytes (higher address) of the memory and is selected when the SW[0:4] input reflects a "01111" combination. Following table describes all the configuration information with respect to SW[0:4] values and internal memory address.

Configuration Number	/N_PnP Signal	SW[0:4] Combination	Memory Location (Word Address)	Memory Location (Byte Address)
Configuration #1	0	0-1-1-1-1	0xFC - 0xFF	0x1F8 - 0x1FF
Configuration #2	0	1-0-1-1-1	0xF8 - 0xFB	0x1F0 - 0x1F7
Configuration #3	0	0-0-1-1-1	0xF4 - 0xF7	0x1E8 - 0x1EF
Configuration #4	0	1-1-0-1-1	0xF0 - 0xF3	0x1E0 - 0x1E7
Configuration #5	0	0-1-0-1-1	0xEC - 0xEF	0x1D8 - 0x1DF
Configuration #6	0	1-0-0-1-1	0xE8 - 0xEB	0x1D0 - 0x1D7
Configuration #7	0	0-0-0-1-1	0xE4 - 0xE7	0x1C8 - 0x1CF
Configuration #8	0	1-1-1-0-1	0xE0 - 0xE3	0x1C0 - 0x1C7
Configuration #9	0	0-1-1-0-1	0xDC - 0xDF	0x1B8 - 0x1BF
Configuration #10	0	1-0-1-0-1	0xD8 - 0xDB	0x1B0 - 0x1B7
Configuration #11	0	0-0-1-0-1	0xD4 - 0xD7	0x1A8 - 0x1AF
Configuration #12	0	1-1-0-0-1	0xD0 - 0xD3	0x1A0 - 0x1A7
Configuration #13	0	0-1-0-0-1	0xCC - 0xCF	0x198 - 0x19F
Configuration #14	0	1-0-0-0-1	0xC8 - 0xCB	0x190 - 0x197
Configuration #15	0	0-0-0-0-1	0xC4 - 0xC7	0x188 - 0x18F
Configuration #16	0	1-1-1-1-0	0xC0 - 0xC3	0x180 - 0x187
Configuration #17	0	0-1-1-1-0	0xBC - 0xBF	0x178 - 0x17F
Configuration #18	0	1-0-1-1-0	0xB8 - 0xBB	0x170 - 0x177
Configuration #19	0	0-0-1-1-0	0xB4 - 0xB7	0x168 - 0x16F
Configuration #20	0	1-1-0-1-0	0xB0 - 0xB3	0x160 - 0x167
Configuration #21	0	0-1-0-1-0	0xAC - 0xAF	0x158 - 0x15F
Configuration #22	0	1-0-0-1-0	0xA8 - 0xAB	0x150 - 0x157
Configuration #23	0	0-0-0-1-0	0xA4 - 0xA7	0x148 - 0x14F
Configuration #24	0	1-1-1-0-0	0xA0 - 0xA3	0x140 - 0x147
Configuration #25	0	0-1-1-0-0	0x9C - 0x9F	0x138 - 0x13F
Configuration #26	0	1-0-1-0-0	0x98 - 0x9B	0x130 - 0x137
Configuration #27	0	0-0-1-0-0	0x94 - 0x97	0x128 - 0x12F
Configuration #28	0	1-1-0-0-0	0x90 - 0x93	0x120 - 0x127
Configuration #29	0	0-1-0-0-0	0x8C - 0x8F	0x118 - 0x11F
Configuration #30	0	1-0-0-0-0	0x88 - 0x8B	0x110 - 0x117
Configuration #31	0	0-0-0-0-0	0x84 - 0x87	0x108 - 0x10F
Software Write	0	1-1-1-1-1	-	-

Internal EEPROM Memory of NM95MS18



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NM95MS18 has a total of 4Kbits (512 Bytes) onboard EEPROM. Of the 512 Bytes, a mimimum of 264 Bytes are allocated for storing *Plug-n-Play Resource data* and the remaining 248 Bytes can be used for storing up to 31 different default power-on Non-PnP configurations (a.k.a. *legacy configurations*). As shown in the above figure, depending on the number of *legacy configurations* supported (can be 31 or 15 or 7 or 3 or 1 or 0), the space for storing *Plug-n-Play Resource data* can be extended to 512 bytes.

SOFTWARE WRITE CONFIGURATION

Under Non-PnP mode when SW[0:4] inputs reflect a 1-1-1-1-1 pattern, NM95MS18 selects a configuration called “Software Write”. Primary use of this configuration is to allow field programming of the internal memory. Need for a field programming might arise if the predetermined 31 legacy configurations are exhausted and needs to be updated with a new set of 31 (or less) legacy configurations. Software-Write configuration overrides the general Write-Protection (refer Write-Protection section) offered by NM95MS18, temporarily.

Under this “Software Write” configuration the NM95MS18 expects an “Extended LFSR” key which is nothing but the regular 32 byte writes of LFSR sequence (as defined in the PnP Specification) followed by a 33rd byte write where the value is “0x9C”. Once the 33rd write is detected, NM95MS18 will automatically transtition to the “CONFIG” state of PnP mode where programming of internal memory is enabled. In this configuration NM95MS18 selects ISA address “0x203” as the default Read_Data_Port, by default.

WRITE PROTECTION

NM95MS18 offers “Write-Protection” for the entire 4Kbits of internal memory. Protection is enabled by setting bit[15] of the “I/O DECODE QUALIFICATION” register to “0”. Setting this bit to “1” disables write-protection. Under “Software Write configuration” this bit is overridden and write-protection is disabled.

PROGRAMMING OF ONCHIP EEPROM

The entire 4Kbit internal EEPROM can be programmed through the ISA bus or through MICROWIRE interface (TEST Mode). Each method is explained below.

PROGRAMMING THROUGH ISA BUS

This method is suited for in-circuit programmin where NM95MS18 is assembled on the ISA board before programming. NM95MS18 is shipped with a “1” pattern at all its bit locations from factory. This means it is shipped with “Write-Protection” disabled. Depending whether the “Write-Protection” is enabled or not there are two procedures to program the onchip memory. Each of these two procedures are explained below.

PROGRAMMING WHEN "WRITE-PROTECTION" IS DISABLED

Follow the procedure defined in ISA Plug-n-Play Specification (Ver. 1.0 a) to place NM95MS18 in "Config" mode of Plug-n-Play protocol. Once the device is is config state, programming of internal EEPROM is enabled. Programming is done by first setting the Address of the location, Data(16bit) to be programmed and then the "Go Ahead" bit to start the programming. A bit in the Status register provides the status of the operation. A programming utility is also available from Fairchild.

Following table summarizes all the registers involved during programming.

Internal EEPROM Memory of NM95MS18 (Continued)

PROGRAMMING INTERFACE

Programming EEPROM Register

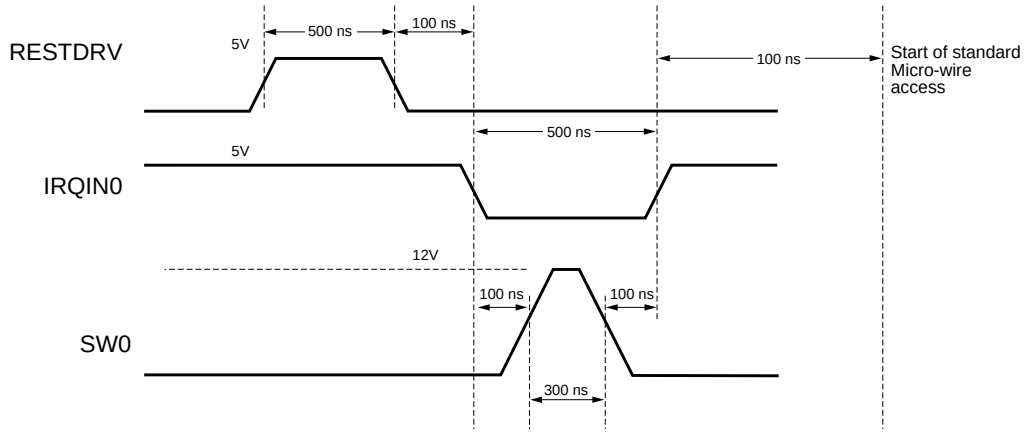
Name	Register	Definition
Status and Command Register	0xF0	Bit[1:0} OP Code bits 10 - Read operation 01 - Write operation 11 - Erase operation Bit [2] - GA (Go Ahead bits) If set to 1, the programming will continue Bit [7:3] - Reserved, should be 0
Address Register	0xF1	Address register [A0 - A7]
Data Register	0xF2	Data Byte [MSB]
Data Register	0xF3	Data Byte [LSB]
STATUS Register	0x05	Bit [0]: STATUS/BUSY bit during programming, '0' is BUSY, '1' is done

PROGRAMMING WHEN "WRITE-PROTECTION" IS ENABLED

In this case, programming is enabled when N_PNP* pin is "0" and the SW[0:4] inputs are "11111". Programming procedure is same as programming when Write-Protection is disabled with the exception of LFSR sequence. In this case 33-Byte Extended-LSFR should be used instead of 32-Byte LFSR.

PROGRAMMING THROUGH MICROWIRE INTERFACE (TEST MODE)

This method is suited when NM95MS18 is pre-programmed before board assembly. This method involves using special TEST mode of NM95MS18. Once the device is in TEST mode, the entire internal memory can be programmed like a standard Micro-wire EEPROM. The protocol to place the device in "test-mode" makes use of the following three signals, viz. RESETDRV, IRQIN0 and SW0. The timing diagram is shown below.



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Note: All timings shown here are minimum values.

Internal EEPROM Memory of NM95MS18 (Continued)

Details of timing information for Microwire protocol can be obtained from Fairchild's Microwire EEPROM Datasheets. Please refer NM93C66 datasheet. This datasheet can be downloaded from Fairchild's home page on World-Wide-Web. (http://www.fairchildsemi.com)

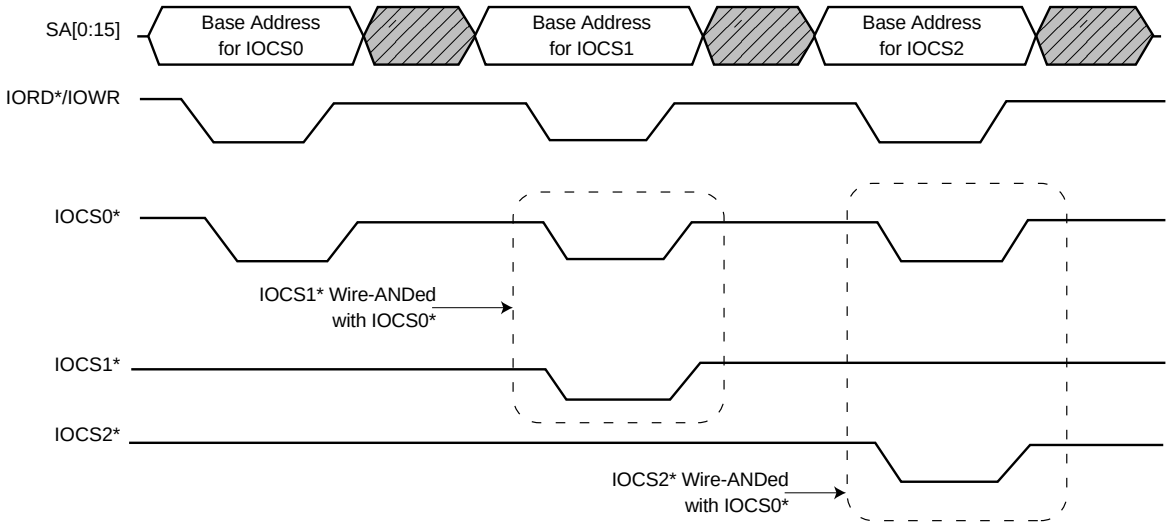
SHARING OF INTERRUPTS

Interrupt output (IRQOUTx) signals from NM95MS18 can be configured as either standard TTL type or Open-Drain type. Interrupt outputs configured as Open-Drain type can share an interrupt on the ISA bus. Sharing of interrupt increases ISA bus resource allocation probabilities and also allows presence of multiple cards of the same type. Each IRQOUTx signal can be individually set for either Interrupt type and this is done by setting appropriate bits in EEPROM register. Refer the USER'S GUIDE for more detail.

Wire-ANDing of I/O Chipselects

The IOCS1* and IOCS2* signals can be internally Wire-ANDed with IOCS0* signal on NM95MS18. When this feature is enabled, IOCS0* signal can also act as "Output Enable" signal for ISA bus data buffers eliminating extra glue logic on the board. Setting appropriate bits in EEPROM register enables this feature. Refer the USER'S GUIDE for more detail. Following diagram illustrates this feature.

WIRE-ANDing of I/O Chipselects



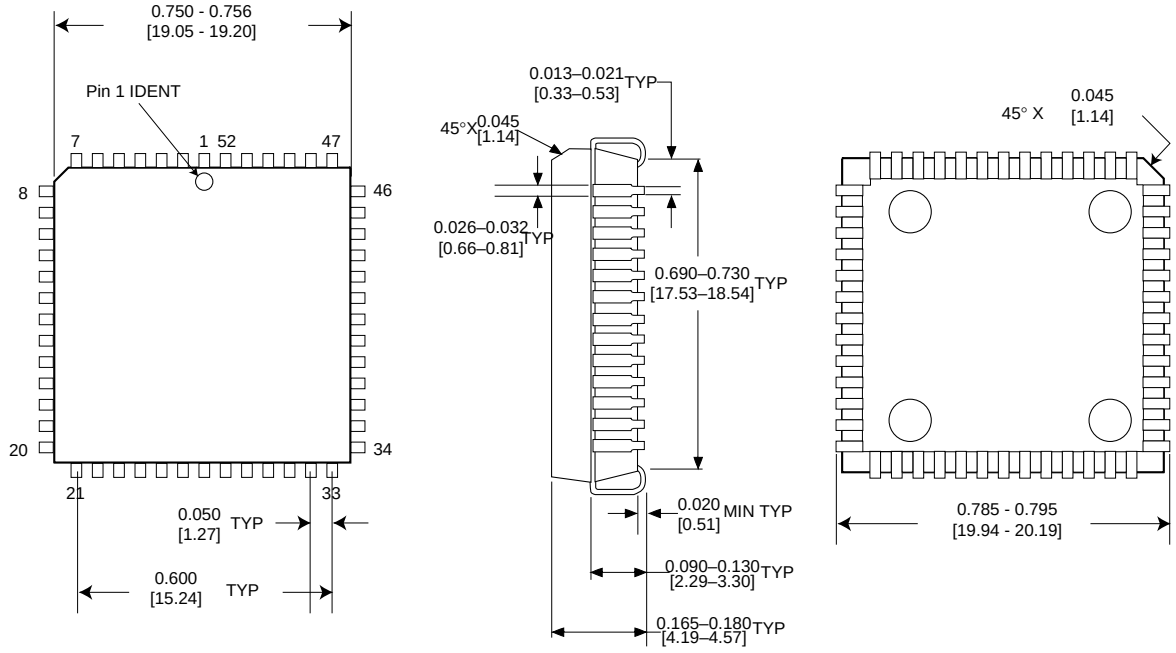
DS500033-11

Note 1: This illustratory waveform assumes that both IOCS1* and IOCS2* are set to be Wire-ANDed with IOCS0*. They can also be set individually.

Note 2: In this waveform, IOCSx* are set to be decoded off of address and IORD*/IOWR.

Note 3: Refer "I/O DECODE QUALIFICATION REGISTER" description for more information.

Physical Dimensions inches (millimeters) unless otherwise noted



52 Lead Molded Plastic Leaded Chip Carrier
Package Number V52A

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Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

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FAIRCHILD SEMICONDUCTOR™

January 1999

NMC27C16B
16,384-Bit (2048 x 8) CMOS EPROM

General Description

The NMC27C16B is a high performance 16K UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

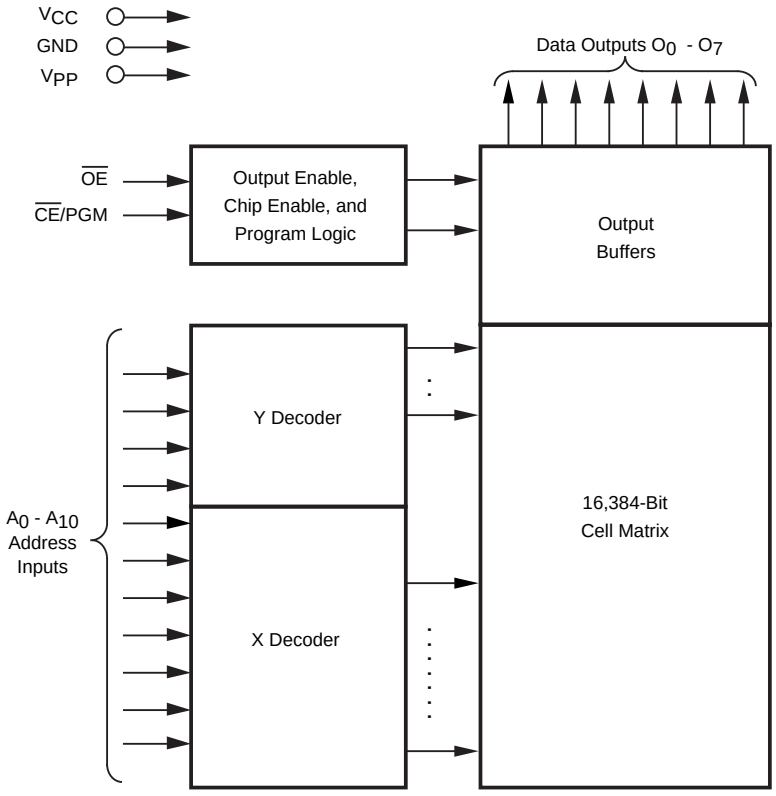
The NMC27C16B is packaged in a 24-pin dual-in-line package with a quartz window. The quartz window allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

This EPROM is fabricated with Fairchild's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Low CMOS power consumption
  Active power: 55 mW max
  Standby power: 0.55 mW max
- Extended temperature range available, -40°C to +85°C
- Fast and reliable programming (100 µs for most bytes)
- TTL compatible inputs/outputs
- TRI-STATE® output
- Manufacturer's identification code for automatic programming equipment
- High current CMOS level output drivers
- Upgrade for NMOS 2716

Block Diagram

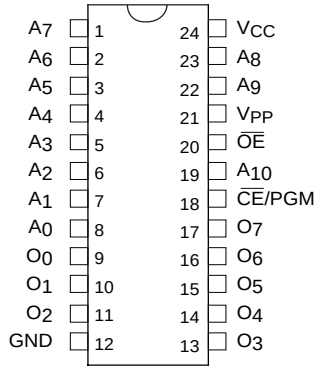


DS009180-1

Connection Diagram

27C256 27256	27C128 27128	27C64 2764	27C32 2732
V_{PP}	V_{PP}	V_{PP}	
A_{12}	A_{12}	A_{12}	
A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2
GND	GND	GND	GND

NMC27C16B
Dual-in-line-package



27C32 2732	27C64 2764	27C128 27128	27C256 27256
	V_{CC} / $\overline{PGM}$	V_{CC} / $\overline{PGM}$	V_{CC}
			A_{14}
V_{CC}	NC	A_{13}	A_{13}
A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9
A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C16B pins.

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Top View
Order Number NMC27C16BQ
See Package Number J24AQ

Pin Names

A0–A10	Addresses
$\overline{CE}/\overline{PGM}$	Chip Enable/Program
$\overline{OE}$	Output Enable
O0 –O7	Outputs
NC	No Connect

Commercial Temp. Range (0°C to 70°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C16BQ150	150
NMC27C16BQ200	200

Extended Temp. Range (-40°C to +85°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C16BQE200	200

Absolute Maximum Ratings (Note 1)

Temperature Under Bias
- Commercial Parts: -10°C to +80°C
- Extended Temp. Parts: -40°C to +85°C

Storage Temperature: -65°C to +150°C

V_{CC} Supply with Respect to Ground: +7.0V to -0.6V

All Input Voltages except A9 with Respect to Ground (Note 10): +6.5V to -0.6V

All Output Voltages with Respect to Ground (Note 10): V_{CC} +1.0V to GND - 0.6V

V_{PP} Supply and A9 Voltage with Respect to Ground: +14.0V to -0.6V

Power Dissipation: 1.0W

Lead Temp. (Soldering, 10 sec.): 300°C

Operating Conditions (Note 8)

Temperature Range
- NMC27C16BQ150, 200: 0°C to +70°C
- NMC27C16BQE 200: -40°C to +85°C

V_{CC} Power Supply: +5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ (Note 11)	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND		0.1	1	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$	0.1	1	µA	
I_{CC1} (Note 3)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f=5 MHz Inputs = V_{IH} or V_{IL} I/O = 0 mA		5	20	mA
I_{CC2} (Note 3)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		3	10	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	µA
I_{PP}	V_{PP} Load Current	V_{PP} = 5.5V			10	µA
V_{IL}	Input Low Voltage		-0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} +1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 mA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 µA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = -10 µA	V_{CC} - 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C16B				Units
			Q150		Q200, QE200		
			Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		60		60	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	50	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$	0	50	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{OE} = \overline{OE} = V_{IL}$	0		0		ns

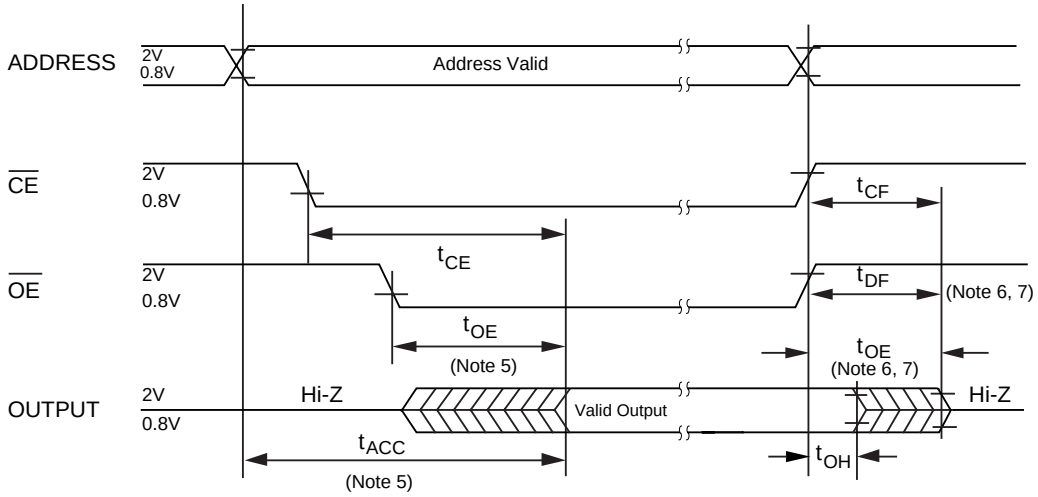
Capacitance T_A =+25°C, f = 1 MHz (Note 4)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	6	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	9	12	pF

AC Test Conditions

Output Load (Note 12)	1 TTL Gate and C_L = 100 pF
Input Rise and Fall Times	≤ 5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Note 2) (Note 9)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

Note 3: V_{PP} may be connected to V_{CC} except during programming. I_{CC1} ≤ the sum of the I_{CC} active and I_{PP} read currents.

Note 4: This parameter is only sampled and is not 100% tested.

Note 5: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.

Note 6: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) - 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 7: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 8: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND.

Note 9: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 10: Inputs and outputs can undershoot to -2.0V for 20 ns maximum.

Note 11: Typical values are for T_A = 25°C and nominal supply voltages.

Note 12: 1 TTL Gate: I_{DL} = 1.6 mA, I_{OH} = 400 µA.
C_L: 100 pF includes fixture capacitance

Programming Characteristics (Note 13) (Note 14) (Note 15) (Note 16)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			µs
t_{OES}	$\overline{OE}$ Setup Time		1			µs
t_{DS}	Data Setup Time		1			µs
t_{VCS}	V_{CC} Setup Time		1			µs
t_{VPS}	V_{PP} Setup Time		1			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		1			µs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE}/\overline{PGM} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	µs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE}/\overline{PGM} = V_{IL}$			150	ns
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IH}$ $\overline{OE} = V_{IH}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		3.0	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

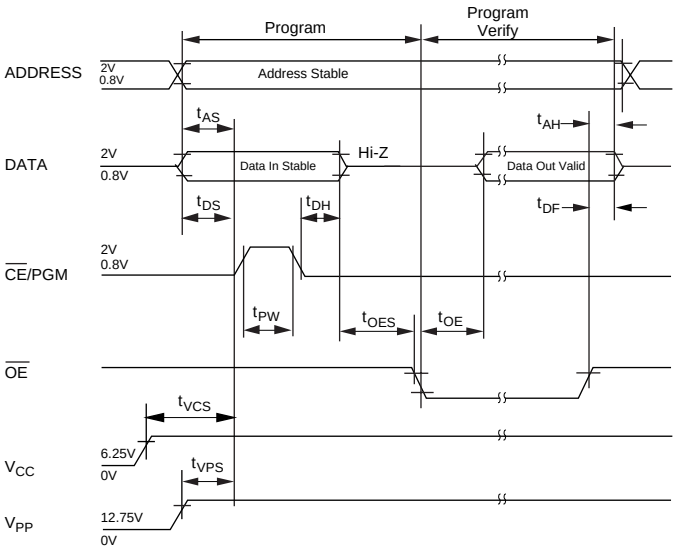
Note 13: Fairchild's standard product warranty applies only to devices programmed to specifications described herein.

Note 14: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 15: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 µF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 16: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings. The Min and Max Limit Parameters are Design parameters, not Tested or guaranteed.

Programming Waveforms



DS009180-4

Fast Programming Algorithm Flow Chart

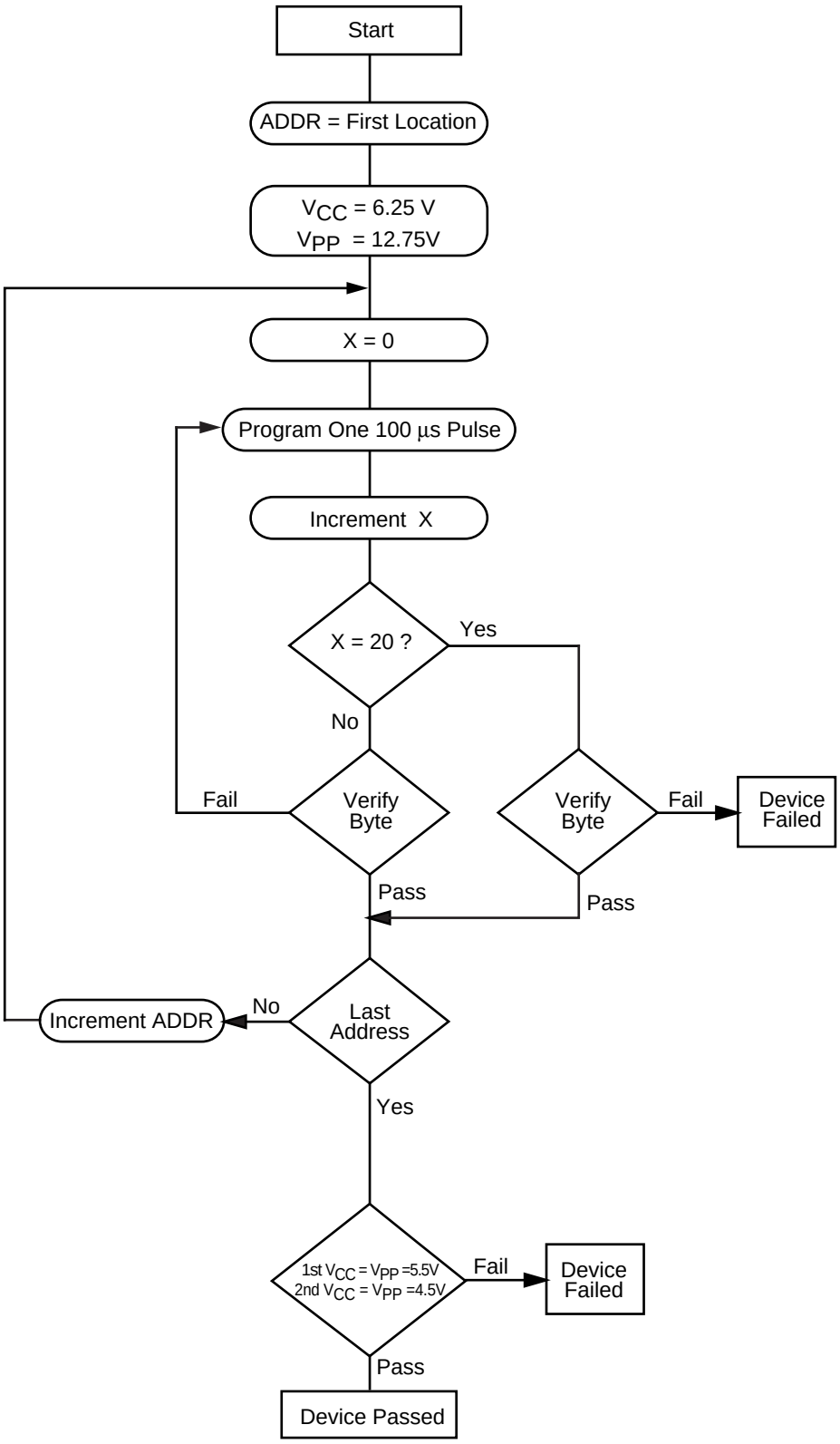


FIGURE 1.

DS009180-5

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C16B are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at V_{CC} in the other modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other modes.

Read Mode

The NMC27C16B has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27C16B has a standby mode which reduces the active power dissipation by 99%, from 100 mW to 0.50 mW. The NMC27C16B is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27C16Bs are usually used in larger memory arrays, Fairchild has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

1. the lowest possible memory power dissipation, and
2. complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 21 (V_{PP}) will damage the NMC27C16B.

Initially, and after each erasure, all bits of the NMC27C16B are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C16B is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 µF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins.

When the address and data are stable, an active high, TTL program pulse is applied to the $\overline{CE}/\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The NMC27C16B is programmed with the Fast Programming Algorithm shown in Figure 1. Each Address is programmed with a series of 100 µs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 µs pulse.

The NMC27C16B must not be programmed with a DC signal applied to the $\overline{CE}/\overline{PGM}$ input.

Programming multiple NMC27C16Bs in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C16Bs may be connected together when they are programmed with the same data. A high level TTL pulse applied to the CE/PGM input programs the paralleled NMC27C16Bs.

TABLE 1. Mode Selection

Pins / Mode	$\overline{CE}/\overline{PGM}$ (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	Outputs (9-11), (13-17)
Read	V_{IL}	V_{IL}	V_{CC}	5	D_{OUT}
Standby	V_{IH}	Don't Care	V_{CC}	5	Hi-Z
Output Disable	Don't Care	V_{IH}	V_{CC}	5	Hi-Z
Program	V_{IH}	V_{IH}	12.75V	6.25	D_{IN}
Program Verify	V_{IL}	V_{IL}	12.75V	6.25	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	12.75V	6.25	Hi-Z

Program Inhibit

Programming multiple NMC27C16Bs in parallel with different data is also easily accomplished. Except for $\overline{CE}/\overline{PGM}$ all like inputs (including $\overline{OE}$) of the parallel NMC27C16Bs may be common. A TTL high level program pulse applied to an NMC27C16B's $\overline{CE}/\overline{PGM}$ input with V_{PP} at 12.75V will program that NMC27C16B. A TTL low level $\overline{CE}/\overline{PGM}$ input inhibits the other NMC27C16Bs from being programmed.

Functional Description (Continued)

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. Except during programming and program verify, V_{PP} must be at V_{CC}.

MANUFACTURER'S IDENTIFICATION CODE

The NMC27C16B has a manufacturer's identification code to aid in programming. The code, shown in Table 3, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NMC27C16B is, "8F80", where "8F" designates that it is made by Fairchild Semiconductor, and "80" designates a 16k part.

The code is accessed by applying 12.0V ±0.5V to address pin A9. Addresses A1–A8, A10, CE , and OE are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at 25°C ± 5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C16B are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å – 4000Å range. After programming, opaque labels should be placed over the NMC27C16B window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C16B is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity x exposure time) for erasure should be a mimimum of 15 W-sec/cm^2.

The NMC27C16B should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table 2 shows the minimum NMC27C16B erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

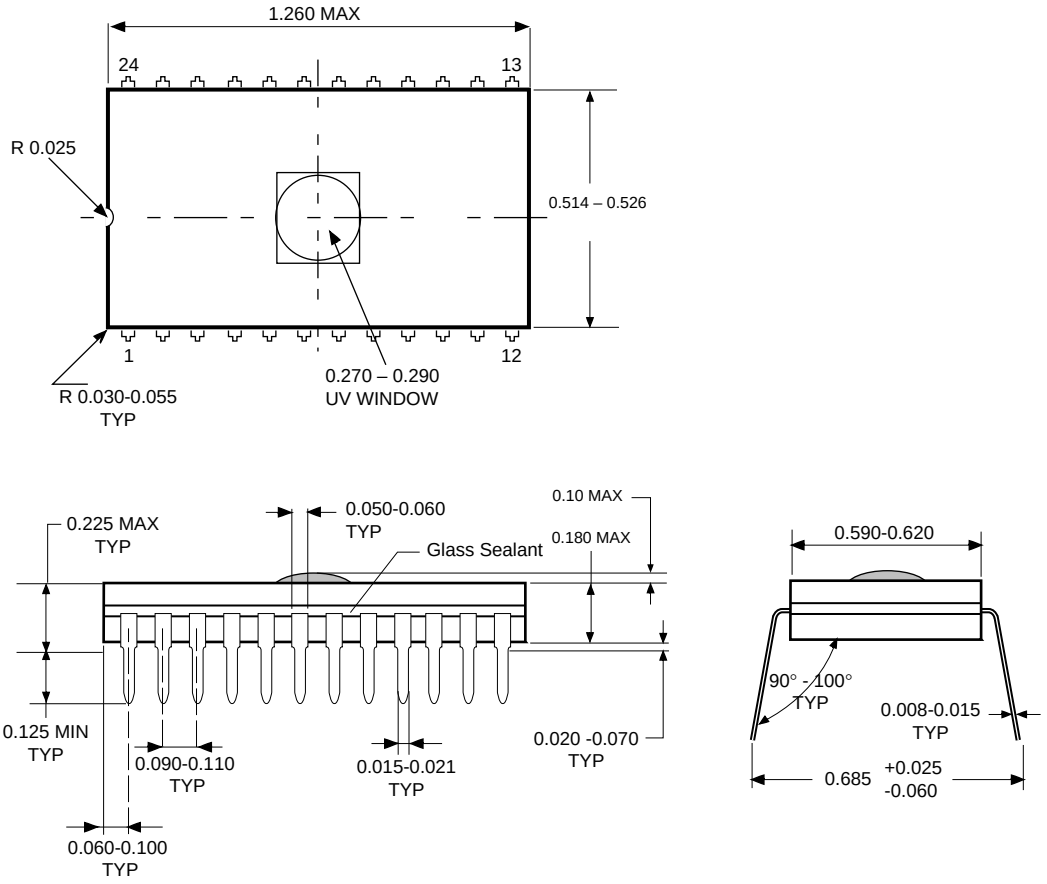
TABLE 2. Minimum NMC27C16B Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

TABLE 3. Manufacturer's Identification Code

Pins	A0 (8)	O7 (17)	O6 (16)	O5 (15)	O4 (14)	O3 (13)	O2 (11)	O1 (10)	O0 (9)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	1	0	0	0	0	0	0	0	80

Physical Dimensions inches (millimeters) unless otherwise noted



UV Window Cavity Dual-In-Line Package (Q)
Order Number NMC27C16BQ
Package Number J24AQ

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

January 1999

NMC27C32B
32,768-Bit (4096 x 8) CMOS EPROM

General Description

The NMC27C32B is a 32k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C32B is designed to operate with a single +5V power supply with ±10% tolerance.

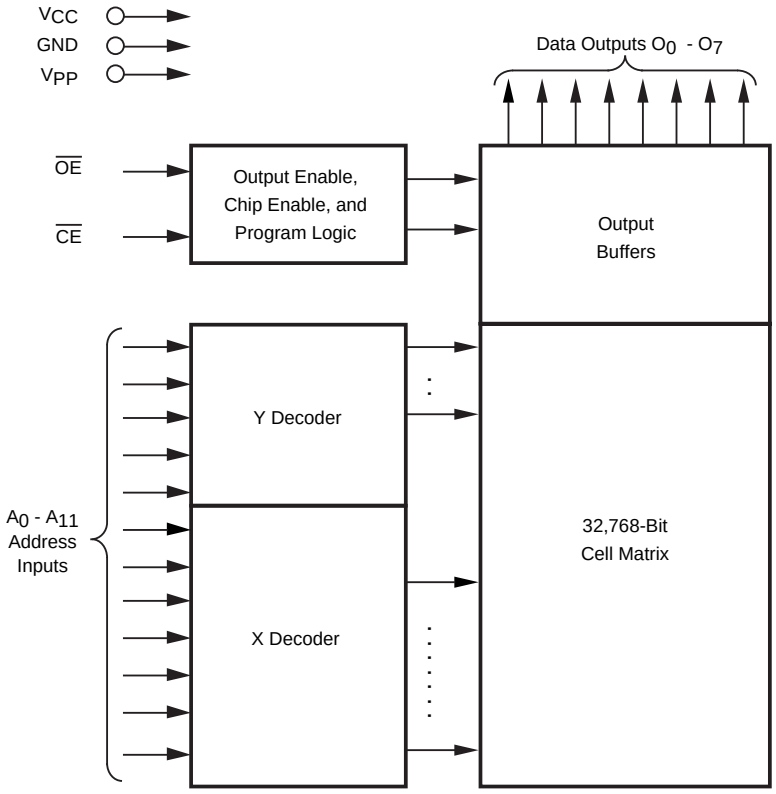
The NMC27C32B is packaged in a 24-pin dual-in-line package with a quartz window. The quartz window allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with Fairchild's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Low CMOS power consumption
  - — Active Power: 55 mW Max
  - — Standby Power: 0.55 mW Max
- Industrial temperature range, -40°C to +85°C
- Fast and reliable programming
- TTL, CMOS compatible inputs/outputs
- TRI-STATE ® output
- Manufacturer's identification code for automatic programming
- High current CMOS level output drivers
- Compatible with NMOS 2732

Block Diagram



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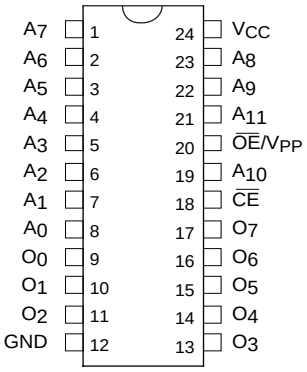
Connection Diagram

27C256 27256	27C128 27128	27C64 2764	27C16 2716
V_{PP}	V_{PP}	V_{PP}	
A_{12}	A_{12}	A_{12}	
A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2
GND	GND	GND	GND

NMC27C32B
Dual-in-line-package



27C16 2716	27C64 2764	27C128 27128	27C256 27256
	V_{CC}	V_{CC}	V_{CC}
	$\overline{PGM}$	$\overline{PGM}$	A_{14}
V_{CC}	NC	A_{13}	A_{13}
A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9
V_{PP}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C32B pin.

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Order Number NMC27C32BQ See Package Number J24AQ

Pin Names

A0–A11	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{PP}	Programming Voltage
O0 –O7	Outputs
V_{CC}	Power Supply
GND	Ground

Commercial Temp Range (0°C to +70°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C32BQ150	150
NMC27C32BQ200	200

Industrial Temp Range (-40°C to +85°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C32BQE200	200

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +150°C
V_{CC} Supply Voltage with Respect to Ground	+7.0V to -0.6V
All Input Voltages except A9 and $\overline{OE}/V_{PP}$ with Respect to Ground (Note 9)	+6.5V to -0.6V
All Output Voltages with Respect to Ground (Note 9)	V_{CC} +1.0V to GND-0.6V
$\overline{OE}/V_{PP}$ Supply and A9 Voltage with Respect to Ground	+14.0V to -0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C

Operating Conditions (Note 6)

Temperature Range	
NMC27C32BQ150, 200	0°C to +70°C
NMC27C32BQE 200	-40°C to +85°C
V_{CC} Power Supply	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND		0.01	1	µA
I_{PP}	$\overline{OE}/V_{PP}$ Load Current	$\overline{OE}/V_{PP} = V_{CC}$ or GND			10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$		0.01	1	µA
I_{CC1}	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f=5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		5	20	mA
I_{CC2}	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		3	10	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	µA
V_{IL}	Input Low Voltage		-0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} +1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 µA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = -10 µA	V_{CC} - 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C32B				Units
			Q150		Q200, QE200		
			Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		60		60	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	50	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$	0	50	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE}$ = V	0		0		ns

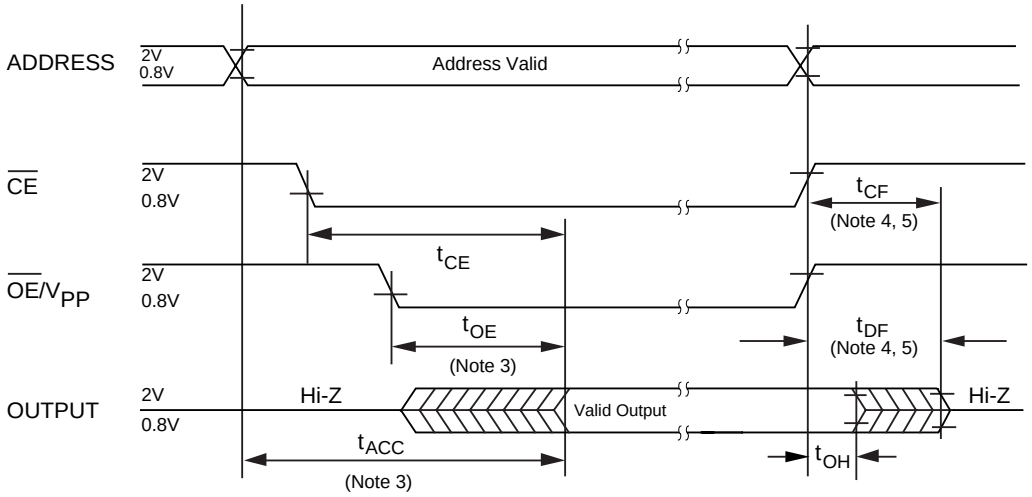
Capacitance (Note 2) T_A = +25°C, f = 1 MHz

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN1}	Input Capacitance except $\overline{OE}/V_{PP}$	V_{IN} = 0V	6	12	pF
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance	V_{IN} = 0V	16	20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	9	12	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Note 7)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) - 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: I_{OL} = 1.6 mA, I_{OH} = -400 µA
C_L: 100 pF includes fixture capacitance.

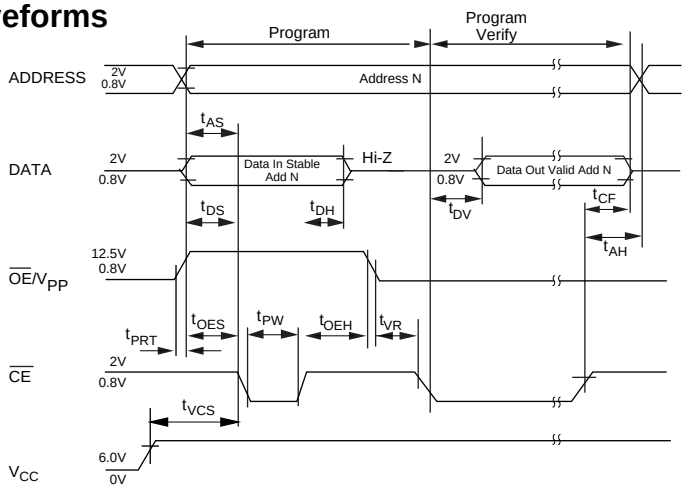
Note 9: Inputs and outputs can undershoot to -2.0V for 20 ns Max, except for $\overline{OE}/V_{PP}$ which cannot exceed -0.2V.

Note 10: Typical values are for T_A = 25°C and nominal supply voltages.

Programming Characteristics (Note 11) (Note 12) (Note 13) (Note 14)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			µs
t_{OES}	$\overline{OE}$ Setup Time		1			µs
t_{DS}	Data Setup Time		1			µs
t_{VCS}	V_{CC} Setup Time		1			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		1			µs
t_{CF}	Chip Enable to Output Float Delay	$\overline{OE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	µs
t_{OEH}	$\overline{OE}$ Hold Time		1			µs
t_{DV}	Data Valid from $\overline{CE}$	$\overline{OE} = V_{IL}$			250	ns
t_{PRT}	$\overline{OE}$ Pulse Rise Time During Programming		50			ns
t_{VR}	V_{PP} Recovery Time		1			µs
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{PP}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

Programming Waveforms



DS008827-4

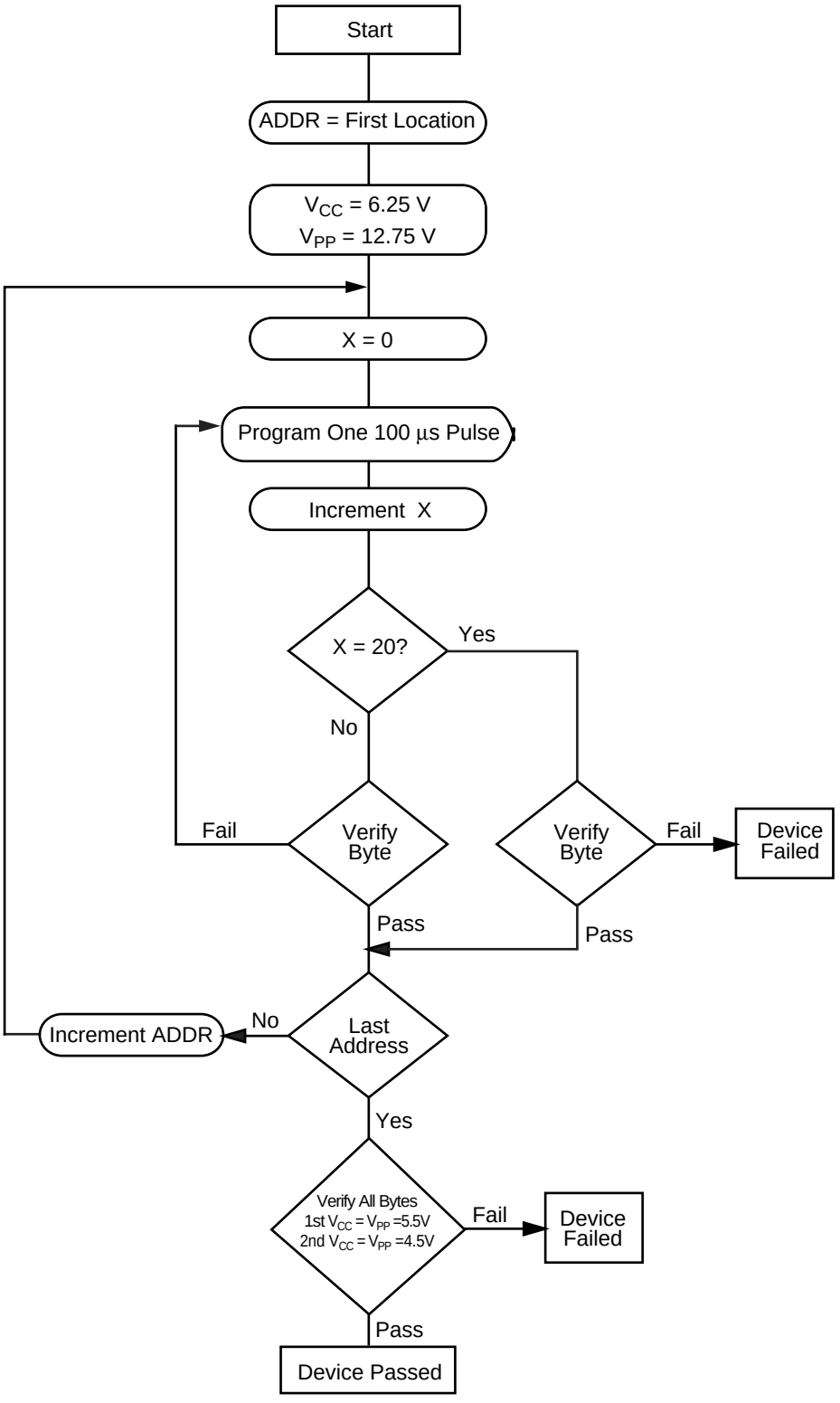
Note 11: Fairchild's standard product warranty applies only to devices programmed to specifications described herein.

Note 12: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 13: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 µF capacitor is required across V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 14: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings.

Fast Programming Algorithm Flow Chart (Note 14)



DS008827-5

FIGURE 1.

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C32B are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ during programming. In the program mode the $\overline{OE}/V_{PP}$ input is pulsed from a TTL low level to 12.75V.

Read Mode

The NMC27C32B has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from CE to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to ensure proper output data.

Standby Mode

The NMC27C32B has a standby mode which reduces the active power dissipation by 99%, from 55 mW to 0.55 mW. The NMC27C32B is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because EPROMs are usually used in larger memory arrays, Fairchild has provided a 2-line control function that accommodates this use of multiple memory connection. The 2-line control function allows for:

1. The lowest possible memory power dissipation, and
2. complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 20 $\overline{OE}/V_{PP}$ will damage the NMC27C32B.

Initially, and after each erasure, all bits of the NMC27C32B are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C32B is in the programming mode when $\overline{OE}/V_{PP}$ is at 12.75V. It is required that at least a 0.1 µF capacitor be placed across V_{CC} and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. The NMC27C32B is programmed with the Fast Programming Algorithm shown in Figure 1. Each Address is programmed with a series of 100 µs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will Program with a single 100 µs pulse.

The NMC27C32B must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming multiple NMC27C32Bs in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C32B may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled NMC27C32B.

TABLE 1. Mode Selection

Pins / Mode	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	Outputs (9–11, 13–17)
Read	V_{IL}	V_{IL}	5V	D_{OUT}
Standby	V_{IH}	Don't Care	5V	Hi-Z
Program	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	6.25V	D_{OUT}
Program Inhibit	V_{IH}	12.75V	6.25V	Hi-Z
Output Disable	Don't Care	V_{IH}	5V	Hi-Z

Program Inhibit

Programming multiple NMC27C32B in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$) of the parallel NMC27C32B may be common. A TTL low level program pulse applied to an NMC27C32B's $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 12.75V will program that NMC27C32B. A TTL high level $\overline{CE}$ input inhibits the other NMC27C32B from being programmed.

Functional Description (Continued)

Program Verify

A verify should be performed on the programmed bit to determine whether they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

MANUFACTURER'S IDENTIFICATION CODE

The NMC27C32B has a manufacturer's identification code to aid in programming. The code, shown in Table 2, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NMC27C32B is, "8F01", where "8F" designates that it is made by Fairchild Semiconductor, and "01" designates a 32k part.

The code is accessed by applying 12.0V ±0.5V to address pin A9. Addresses A1–A8, A10–A11, $\overline{CE}$, and $\overline{OE}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at 25°C ± 5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C32B are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å - 4000Å range. After programming, opaque labels should be placed over the NMC27C32B's window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C32B is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2.

The NMC27C32B should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

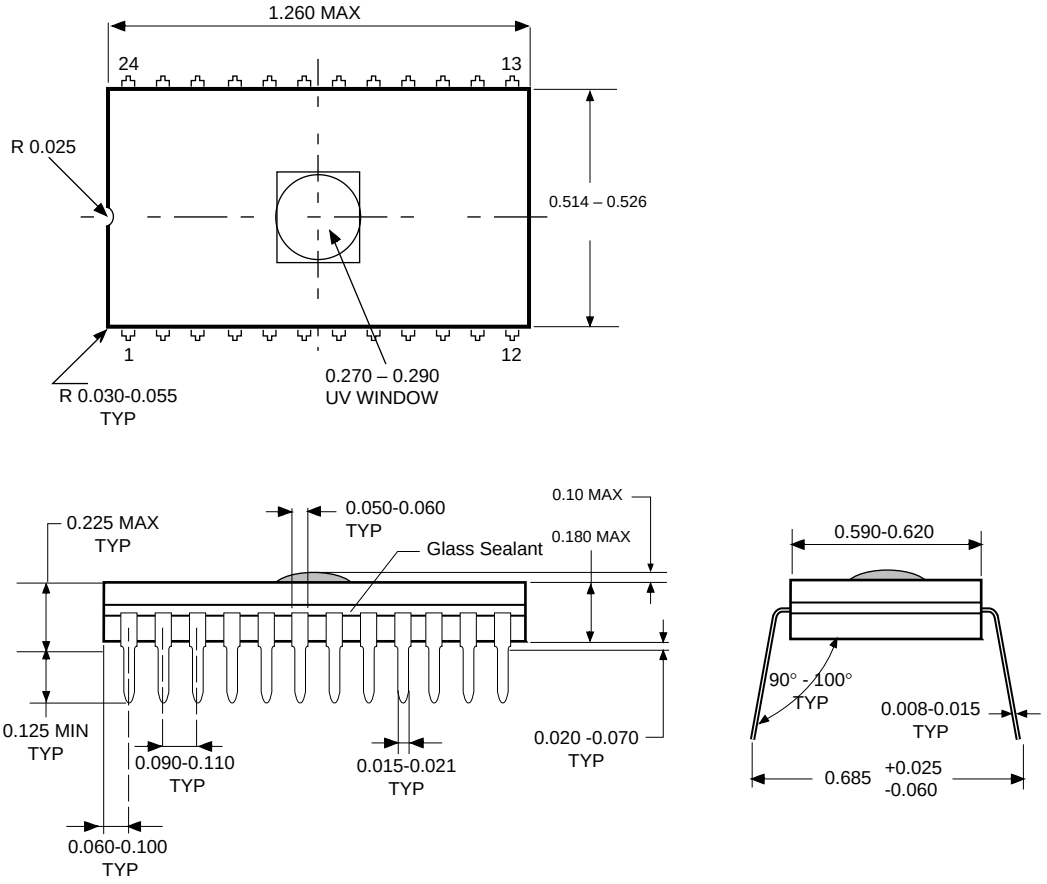
SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE 2. Manufacturer's Identification Code

Pins	A0 (8)	O7 (17)	O6 (16)	O5 (15)	O4 (14)	O3 (13)	O2 (11)	O1 (10)	O0 (9)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	0	0	0	0	0	0	0	1	01

Physical Dimensions inches (millimeters) unless otherwise noted



UV Window Cavity Dual-In-Line Cerdip Package (JQ)
Order Number NMC27C32BQ
Package Number J24AQ

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Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

January 1999

NMC27C64
65,536-Bit (8192 x 8) CMOS EPROM

General Description

The NMC27C64 is a 64K UV erasable, electrically reprogrammable and one-time programmable (OTP) CMOS EPROM ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C64 is designed to operate with a single +5V power supply with ±10% tolerance. The CMOS design allows the part to operate over extended and military temperature ranges.

The NMC27C64Q is packaged in a 28-pin dual-in-line package with a quartz window. The quartz window allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

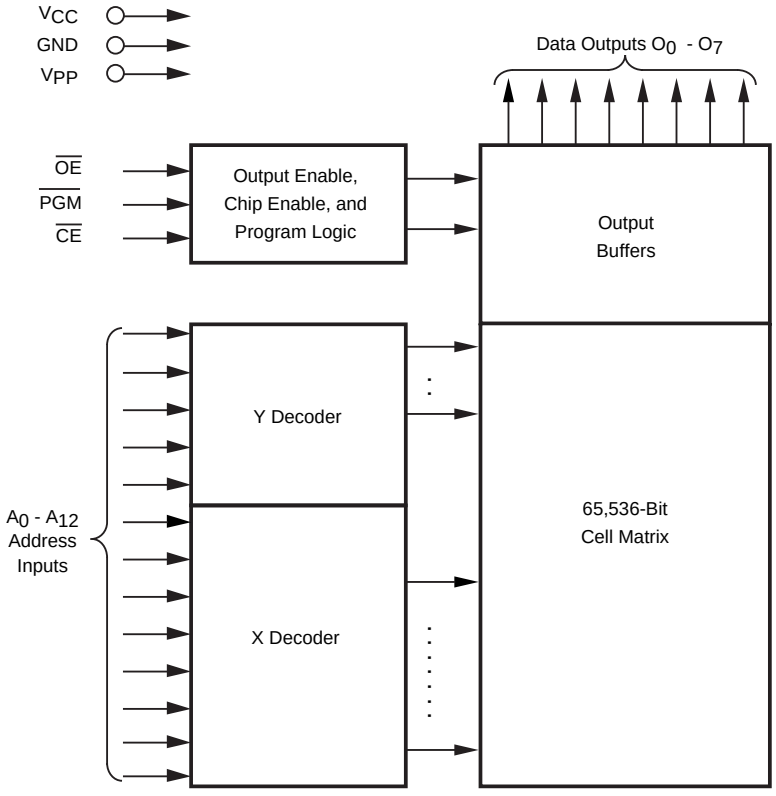
The NMC27C64N is packaged in a 28-pin dual-in-line plastic molded package without a transparent lid. This part is ideally suited for high volume production applications where cost is an important factor and programming only needs to be done once.

This family of EPROMs are fabricated with Fairchild's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- High performance CMOS
  - —150 ns access time
- JEDEC standard pin configuration
  - —28-pin Plastic DIP package
  - —28-pin CERDIP package
- Drop-in replacement for 27C64 or 2764
- Manufacturers identification code

Block Diagram



DS008634-1

Connection Diagram

27C512 27512	27C256 27256	27C128 27128	27C32 2732	27C16 2716					27C16 2716	27C32 2732	27C128 27128	27C256 27256	27C512 27512
A_{15}	V_{PP}	V_{PP}			V_{PP}	1	28	V_{CC}			V_{CC}	V_{CC}	V_{CC}
A_{12}	A_{12}	A_{12}			A_{12}	2	27	$\overline{PGM}$			$\overline{PGM}$	A_{14}	A_{14}
A_7	A_7	A_7	A_7	A_7	A_7	3	26	NC	V_{CC}	V_{CC}	A_{13}	A_{13}	A_{13}
A_6	A_6	A_6	A_6	A_6	A_6	4	25	A_8	A_8	A_8	A_8	A_8	A_8
A_5	A_5	A_5	A_5	A_5	A_5	5	24	A_9	A_9	A_9	A_9	A_9	A_9
A_4	A_4	A_4	A_4	A_4	A_4	6	23	A_{11}	V_{PP}	A_{11}	A_{11}	A_{11}	A_{11}
A_3	A_3	A_3	A_3	A_3	A_3	7	22	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_2	A_2	A_2	A_2	A_2	A_2	8	21	A_{10}	A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
A_1	A_1	A_1	A_1	A_1	A_1	9	20	$\overline{CE}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}$
A_0	A_0	A_0	A_0	A_0	A_0	10	19	O_7	O_7	O_7	O_7	O_7	O_7
O_0	O_0	O_0	O_0	O_0	O_0	11	18	O_6	O_6	O_6	O_6	O_6	O_6
O_1	O_1	O_1	O_1	O_1	O_1	12	17	O_5	O_5	O_5	O_5	O_5	O_5
O_2	O_2	O_2	O_2	O_2	O_2	13	16	O_4	O_4	O_4	O_4	O_4	O_4
GND	GND	GND	GND	GND	GND	14	15	O_3	O_3	O_3	O_3	O_3	O_3

NMC27C64

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C64 pins.

DS008634-2

Pin Names

A0–A12	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$O_0 - O_7$	Outputs
$\overline{PGM}$	Program
NC	No Connect
V_{PP}	Programming Voltage
V_{CC}	Power Supply
GND	Ground

Commercial Temperature Range V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C64Q, N 150	150
NMC27C64Q, N 200	200

Extended Temp Range (-40°C to +85°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C64QE, NE200	200

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to -0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} +1.0V to GND -0.6V
V_{PP} Supply Voltage and A_9 with Respect to Ground During Programming	+14.0V to -0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to -0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 7)

Temperature Range	
NMC27C64Q 150, 200 NMC27C64N 150, 200	0°C to +70°C
NMC27C64QE 200 NMC27C64NE 200	-40°C to +85°C
V_{CC} Power Supply	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	µA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$,f=5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		5	20	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		3	10	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	µA
I_{PP}	VPP Load Current	$V_{PP} = V_{CC}$		10	µA	
V_{IL}	Input Low Voltage		-0.1		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} +1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 0 µA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 0 µA	V_{CC} - 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C64				Units
			150		200, E200		
			Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$		60		60	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	60	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	60	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0		0		ns

Capacitance TA = +25˚C, f = 1 MHz (Note 2) NMC27C64Q

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	6	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	9	12	pF

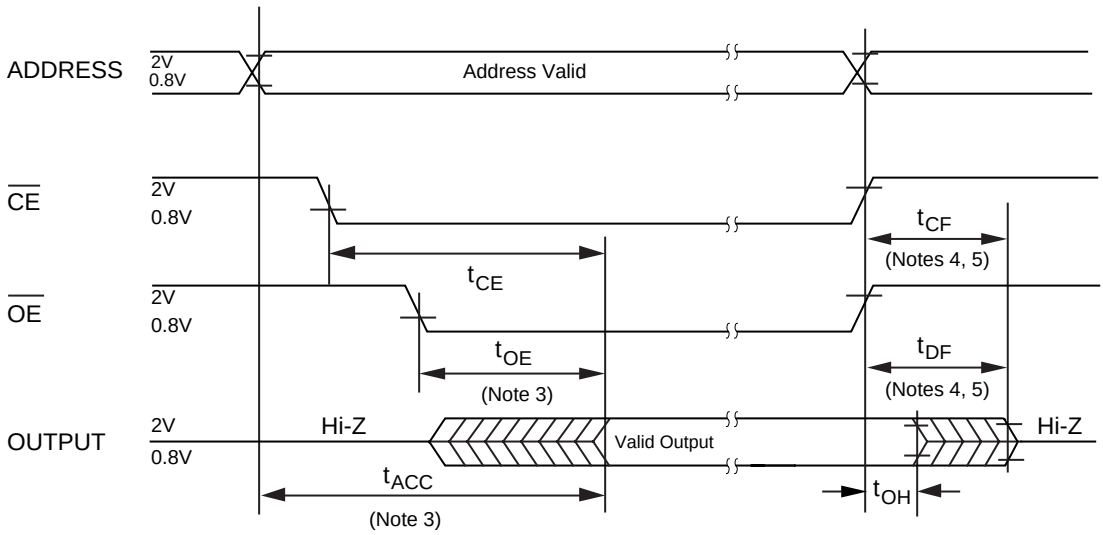
Capacitance TA = +25˚C, f = 1 MHz (Note 2) NMC27C64N

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	5	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	10	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Note 6) (Note 9)



Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE ® , the measured V_{OH1} (DC) ، 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: I_{OL} = 1.6 mA, I_{OH} = -400 µA.
C_L: 100 pF includes fixture capacitance.

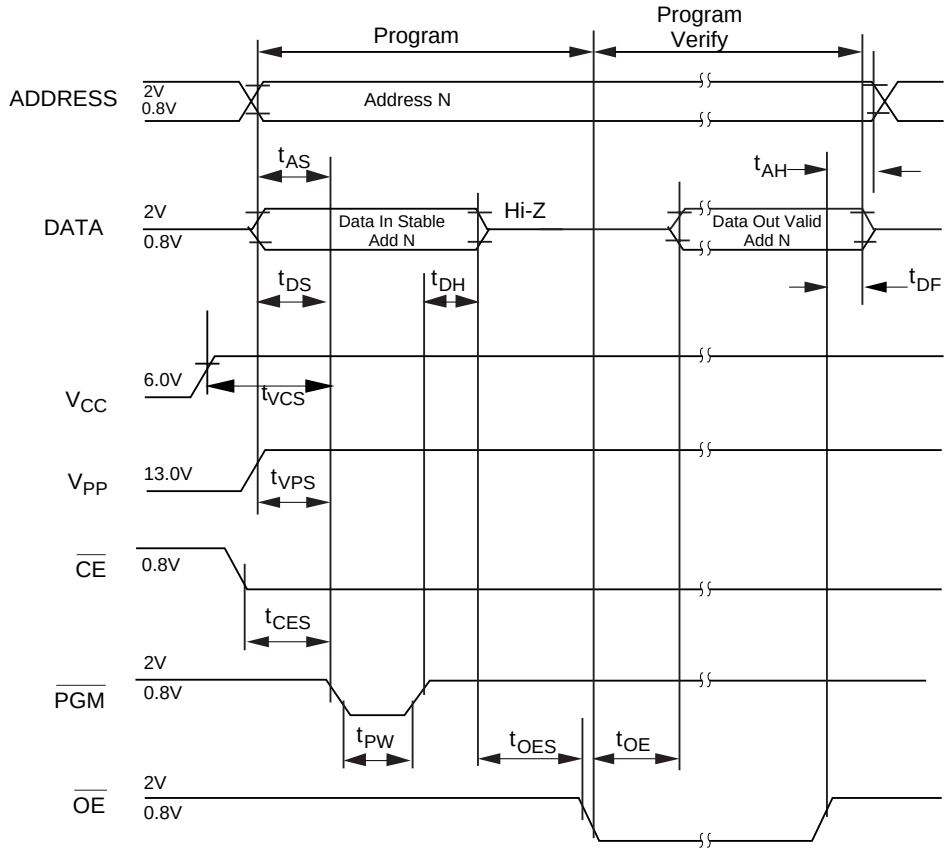
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to -2.0V for 20 ns Max.

Programming Characteristics (Note 11) (Note 12) (Note 13) (Note 14)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		2			µs
t_{OES}	$\overline{OE}$ Setup Time		2			µs
t_{CES}	$\overline{CE}$ Setup Time		2			µs
t_{DS}	Data Setup Time		2			µs
t_{VPS}	V_{PP} Setup Time		2			µs
t_{VCS}	V_{CC} Setup Time		2			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		2			µs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		130	ns
t_{PW}	Program Pulse Width		0.45	0.5	0.55	ms
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			150	ns
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	˚C
V_{CC}	Power Supply Voltage		5.75	6.0	6.25	V
V_{PP}	Programming Supply Voltage		12.2	13.0	13.3	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V

Programming Waveforms (Note 13)



Note 11: Fairchild's standard product warranty applies to devices programmed to specifications described herein.

Note 12: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 13: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 µF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 14: Programming and program verify are tested with the interactive Program Algorithm, at typical power supply voltages and timings.

Fast Programming Algorithm Flow Chart

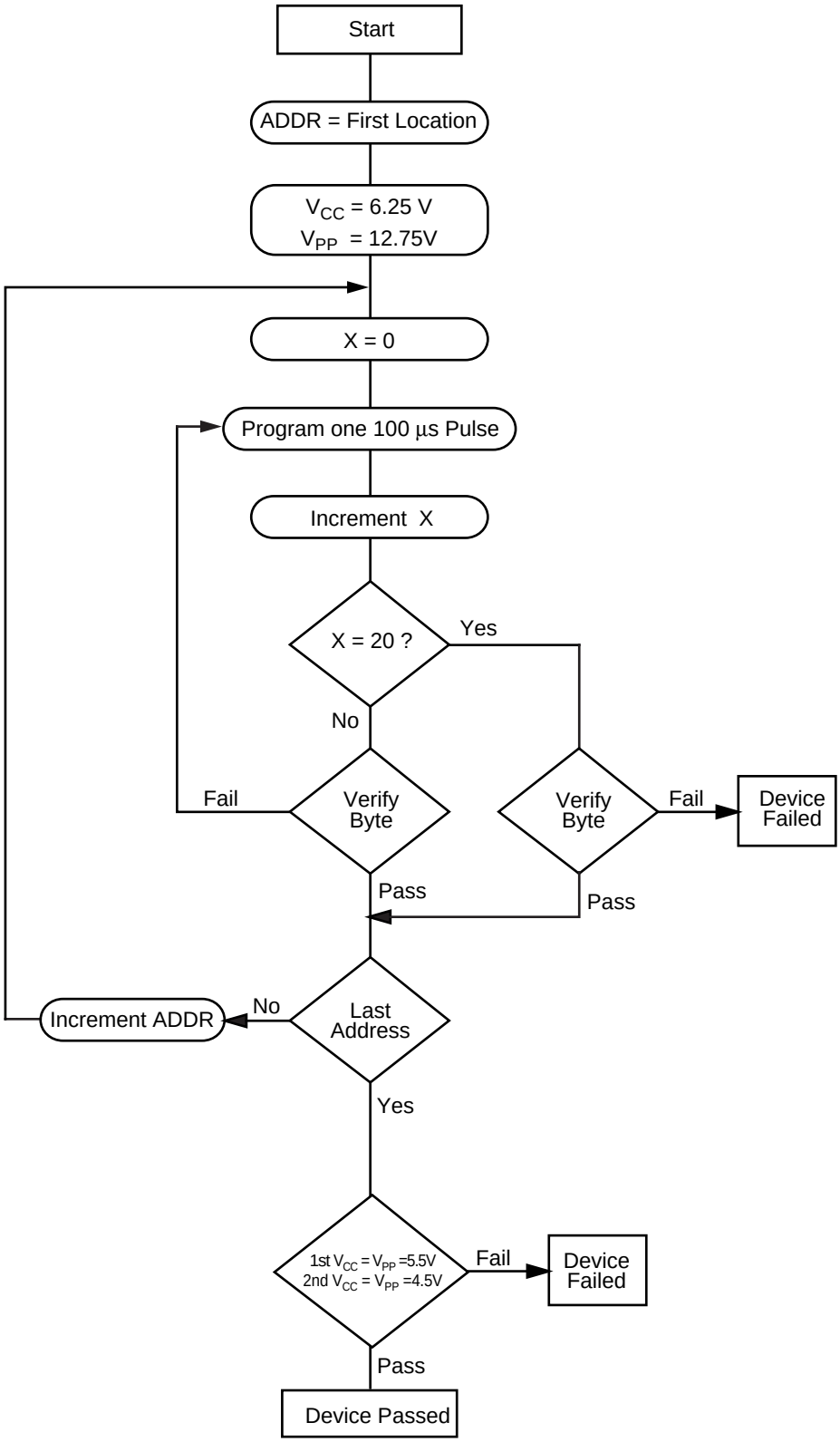


FIGURE 1.

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C64 are listed in Table 1. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6V during the three programming modes, and at 5V in the other three modes.

Read Mode

The NMC27C64 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. The programming pin ($\overline{PGM}$) should be at V_{IH} except during programming. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of OE , assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27C64 has a standby mode which reduces the active power dissipation by 99%, from 55 mW to 0.55 mW. The NMC27C64 is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27C64s are usually used in larger memory arrays, Fairchild has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

1. the lowest possible memory power dissipation, and
2. complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recomended that $\overline{CE}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the NMC27C64.

Initially, all bits of the NMC27C64 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. A "0" cannot be changed to a "1" once the bit has been programmed.

The NMC27C64 is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 µF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

For programming, $\overline{CE}$ should be kept TTL low at all times while V_{PP} is kept at 12.75V.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The NMC27C64 is programmed with the Fast Programming Algorithm shown in Figure 1. Each address is programmed with a series of 100 µs pulses until it verfies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 µs pulse. The NMC27C64 must not be programmed with a DC signal applied to the PGM input.

Programming multiple NMC27C64s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C64s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled NMC27C64s. If an application requires erasing and reprogramming, the NMC27C64Q UV erasable PROM in a windowed package should be used.

TABLE 1. Mode Selection

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	V_{IH}	5V	5V	D_{OUT}
Standby	V_{IH}	Don't Care	Don't Care	5V	5V	Hi-Z
Output Disable	Don't Care	V_{IH}	V_{IH}	5V	5V	Hi-Z
Program	V_{IL}	V_{IH}		13V	6V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	13V	6V	D_{OUT}
Program Inhibit	V_{IH}	Don't Care	Don't Care	13V	6V	Hi-Z

Functional Description (Continued)

Program Inhibit

Programming multiple NMC27C64s in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel NMC27C64 may be common. A TTL low level program pulse applied to an NMC27C64's $\overline{PGM}$ input with $\overline{CE}$ at V_{IL} and V_{PP} at 13.0V will program that NMC27C64. A TTL high level $\overline{CE}$ input inhibits the other NMC27C64s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 13.0V. V_{PP} must be at V_{CC}, except during programming and program verify.

MANUFACTURER'S IDENTIFICATION CODE

The NMC27C64 has a manufacturer's identification code to aid in programming. The code, shown in Table 2, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NMC27C64 is "8FC2", where "8F" designates that it is made by Fairchild Semiconductor, and "C2" designates a 64k part.

The code is accessed by applying 12V ± 0.5V to address pin A9. Addresses A1–A8, A10–A12, $\overline{CE}$, and $\overline{OE}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at 25°C ± 5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in a EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C64 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å – 4000Å range.

After programming, opaque labels should be placed over the NMC27C64's window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C64 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The NMC27C64 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

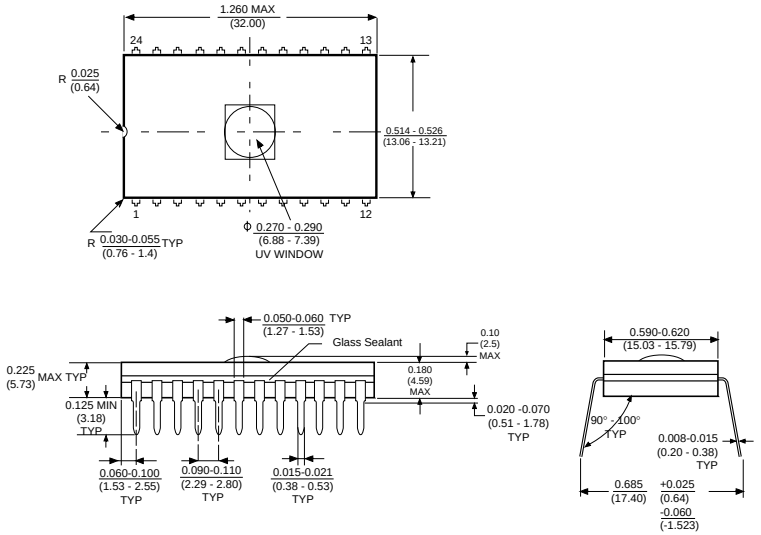
SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

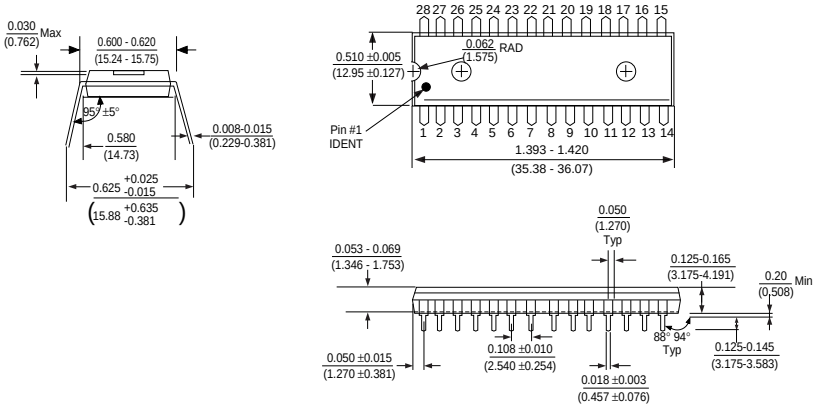
TABLE 2. Manufacturer's Identification Code

Pins	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	1	1	0	0	0	0	1	0	C2

Physical Dimensions inches (millimeters) unless otherwise noted



Dual-In-Line Package (Q)
Order Number NMC27C64Q
Package Number J28AQ



Dual-In-Line Package (N)
Order Number NMC27C64N
Package Number N28B

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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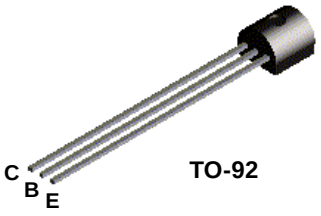
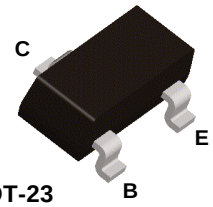
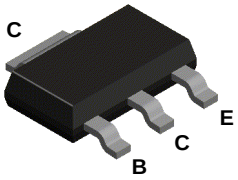


TO-92

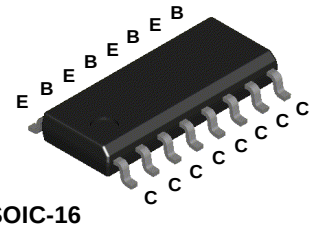


SOT-23
Mark: 1P

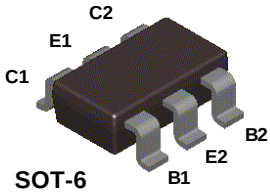


SOT-223

MMPQ2222 NMT2222



SOIC-16



SOT-6
Mark: .1B

NPN General Purpose Amplifier

This device is for use as a medium power amplifier and switch requiring collector currents up to 500 mA. Sourced from Process 19.

Absolute Maximum Ratings*

TA = 25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{CEO}	Collector-Emitter Voltage	40	V
V_{CBO}	Collector-Base Voltage	75	V
V_{EBO}	Emitter-Base Voltage	6.0	V
I_C	Collector Current - Continuous	1.0	A
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

NOTES:
1) These ratings are based on a maximum junction temperature of 150 degrees C.
2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

NPN General Purpose Amplifier
(continued)

Electrical Characteristics
TA = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Max	Units
OFF CHARACTERISTICS					
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage*	I_C = 10 mA, I_B = 0	40		V
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 10 µA, I_E = 0	75		V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 10 µA, I_C = 0	6.0		V
I_{CEX}	Collector Cutoff Current	V_{CE} = 60 V, $V_{EB(OFF)}$ = 3.0 V		10	nA
I_{CBO}	Collector Cutoff Current	V_{CB} = 60 V, I_E = 0 V_{CB} = 60 V, I_E = 0, T_A = 150°C		0.01 10	µA µA
I_{EBO}	Emitter Cutoff Current	V_{EB} = 3.0 V, I_C = 0		10	nA
I_{BL}	Base Cutoff Current	V_{CE} = 60 V, $V_{EB(OFF)}$ = 3.0 V		20	nA
ON CHARACTERISTICS					
h_{FE}	DC Current Gain	I_C = 0.1 mA, V_{CE} = 10 V I_C = 1.0 mA, V_{CE} = 10 V I_C = 10 mA, V_{CE} = 10 V I_C = 10 mA, V_{CE} = 10 V, T_A = -55°C I_C = 150 mA, V_{CE} = 10 V* I_C = 150 mA, V_{CE} = 1.0 V* I_C = 500 mA, V_{CE} = 10 V*	35 50 75 35 100 50 40	 300 	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage*	I_C = 150 mA, I_B = 15 mA I_C = 500 mA, I_B = 50 mA		0.3 1.0	V V
$V_{BE(sat)}$	Base-Emitter Saturation Voltage*	I_C = 150 mA, I_B = 1.0 mA I_C = 500 mA, I_B = 5.0 mA	0.6	1.2 2.0	V V
SMALL SIGNAL CHARACTERISTICS (except MMPQ2222 and NMT2222)					
f_T	Current Gain - Bandwidth Product	I_C = 20 mA, V_{CE} = 20 V, f = 100 MHz	300		MHz
C_{obo}	Output Capacitance	V_{CB} = 10 V, I_E = 0, f = 100 kHz		8.0	pF
C_{ibo}	Input Capacitance	V_{EB} = 0.5 V, I_C = 0, f = 100 kHz		25	pF
rb'C_C	Collector Base Time Constant	I_C = 20 mA, V_{CB} = 20 V, f = 31.8 MHz		150	pS
NF	Noise Figure	I_C = 100 µA, V_{CE} = 10 V, R_S = 1.0 kΩ, f = 1.0 kHz		4.0	dB
Re(h_{ie})	Real Part of Common-Emitter High Frequency Input Impedance	I_C = 20 mA, V_{CE} = 20 V, f = 300 MHz		60	Ω
SWITCHING CHARACTERISTICS (except MMPQ2222 and NMT2222)					
t_d	Delay Time	V_{CC} = 30 V, $V_{BE(OFF)}$ = 0.5 V,		10	ns
t_r	Rise Time	I_C = 150 mA, I_{B1} = 15 mA		25	ns
t_s	Storage Time	V_{CC} = 30 V, I_C = 150 mA,		225	ns
t_f	Fall Time	I_{B1} = I_{B2} = 15 mA		60	ns

*Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%

Spice Model

NPN (Is=14.34f Xti=3 Eg=1.11 Vaf=74.03 Bf=255.9 Ne=1.307 Ise=14.34f Ikf=.2847 Xtb=1.5 Br=6.092 Nc=2 Isc=0 Ikr=0 Rc=1 Cjc=7.306p Mjc=.3416 Vjc=.75 Fc=.5 Cje=22.01p Mje=.377 Vje=.75 Tr=46.91n Tf=411.1p Itf=.6 Vtf=1.7 Xtf=3 Rb=10)

NPN General Purpose Amplifier
(continued)

Thermal Characteristics
TA = 25°C unless otherwise noted

Symbol	Characteristic	Max		Units
		PN2222A	*PZT2222A	
P_D	Total Device Dissipation Derate above 25°C	625 5.0	1,000 8.0	mW mW/°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	83.3		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	200	125	°C/W

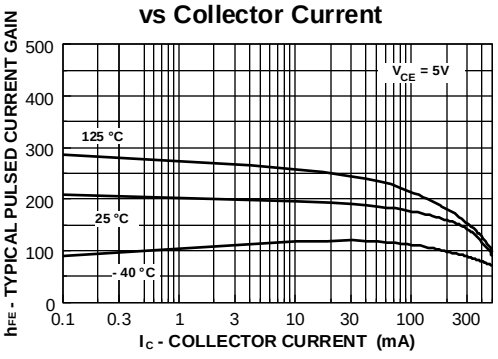
Symbol	Characteristic	Max		Units
		**MMBT2222A	MMPQ2222	
P_D	Total Device Dissipation Derate above 25°C	350 2.8	1,000 8.0	mW mW/°C
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient Effective 4 Die Each Die	357	 125 240	°C/W °C/W °C/W

*Device mounted on FR-4 PCB 36 mm X 18 mm X 1.5 mm; mounting pad for the collector lead min. 6 cm^2.

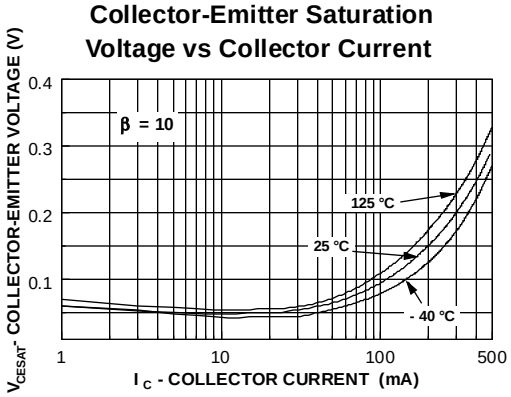
**Device mounted on FR-4 PCB 1.6" X 1.6" X 0.06."

Typical Characteristics

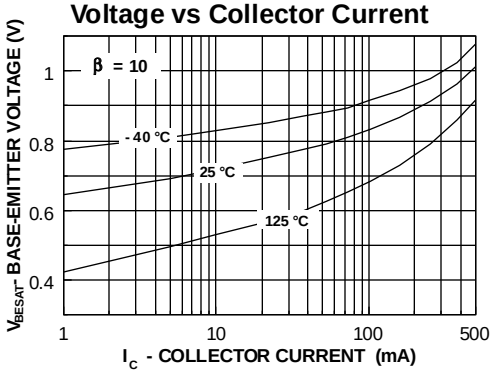
Typical Pulsed Current Gain vs Collector Current



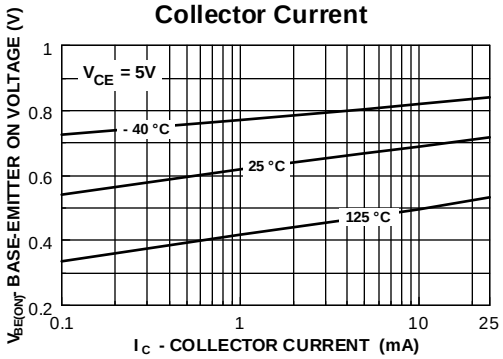
Collector-Emitter Saturation Voltage vs Collector Current



Base-Emitter Saturation Voltage vs Collector Current

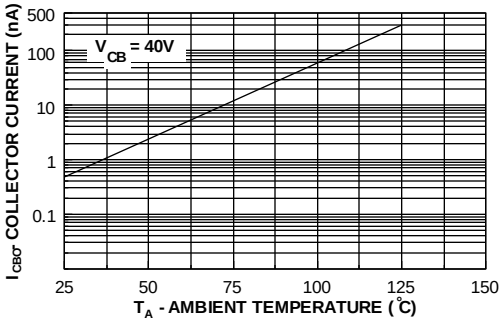


Base-Emitter ON Voltage vs Collector Current

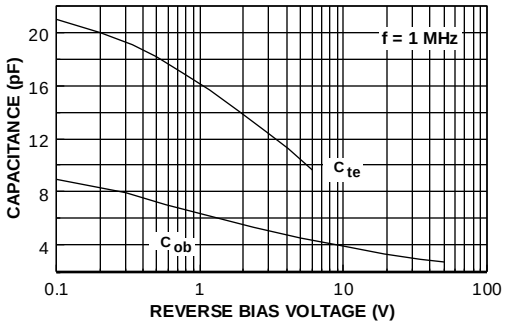


Typical Characteristics (continued)

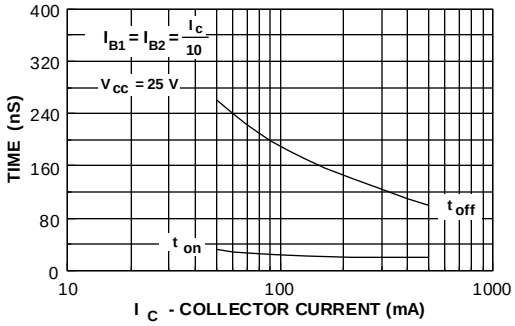
Collector-Cutoff Current vs Ambient Temperature



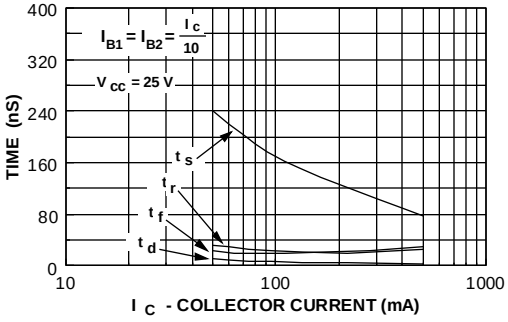
Emitter Transition and Output Capacitance vs Reverse Bias Voltage



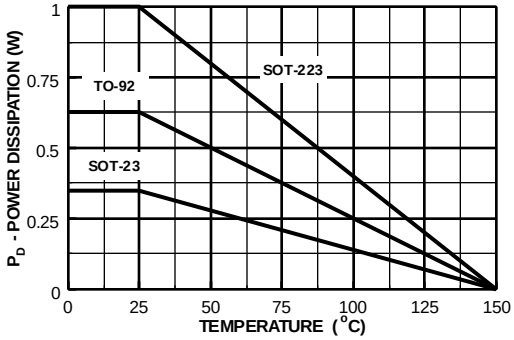
Turn On and Turn Off Times vs Collector Current



Switching Times vs Collector Current



Power Dissipation vs Ambient Temperature



Test Circuits

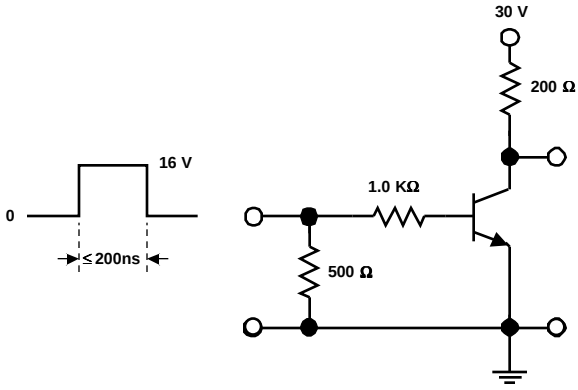


FIGURE 1: Saturated Turn-On Switching Time

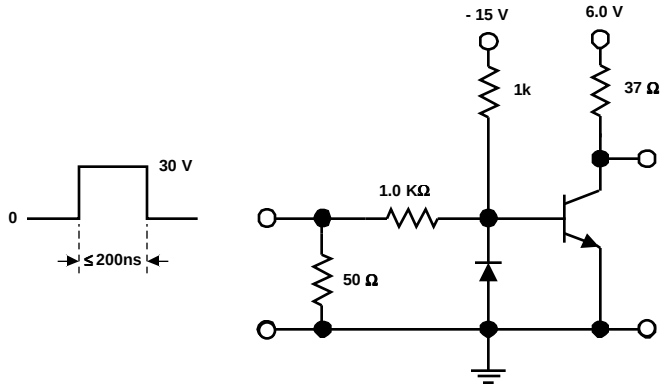
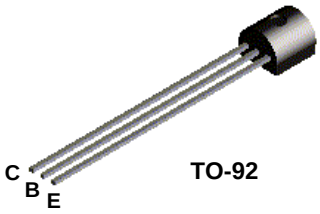


FIGURE 2: Saturated Turn-Off Switching Time

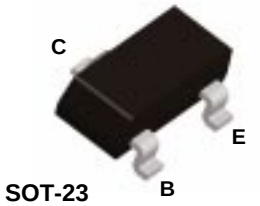
FAIRCHILD SEMICONDUCTOR TM

Discrete POWER & Signal Technologies

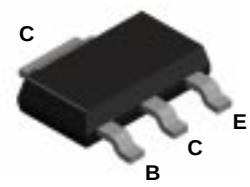
PN2907A MMBT2907A PZT2907A



TO-92

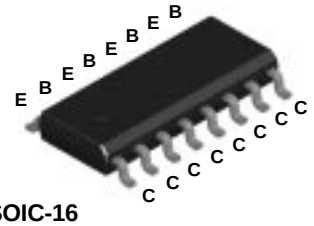


SOT-23
Mark: 2F

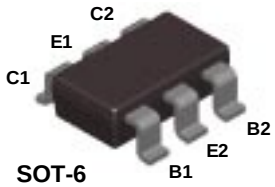


SOT-223

MMPQ2907 NMT2907



SOIC-16



SOT-6
Mark: .2B

PNP General Purpose Amplifier

This device is designed for use as a general purpose amplifier and switch requiring collector currents to 500 mA. Sourced from Process 63.

Absolute Maximum Ratings*

TA = 25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{CEO}	Collector-Emitter Voltage	60	V
V_{CBO}	Collector-Base Voltage	60	V
V_{EBO}	Emitter-Base Voltage	5.0	V
I_C	Collector Current - Continuous	800	mA
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

NOTES:
1) These ratings are based on a maximum junction temperature of 150 degrees C.
2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

PNP General Purpose Amplifier
(continued)

Electrical Characteristics
TA = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Max	Units
OFF CHARACTERISTICS					
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage*	I_C = 10 mA, I_B = 0	60		V
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 10 µA, I_E = 0	60		V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 10 µA, I_C = 0	5.0		V
I_B	Base Cutoff Current	V_{CB} = 30 V, V_{EB} = 0.5 V		50	nA
I_{CEX}	Collector Cutoff Current	V_{CE} = 30 V, V_{BE} = 0.5 V		50	nA
I_{CBO}	Collector Cutoff Current	V_{CB} = 50 V, I_E = 0 V_{CB} = 50 V, I_E = 0, T_A = 150°C		0.02 20	µA µA
ON CHARACTERISTICS					
h_{FE}	DC Current Gain	I_C = 0.1 mA, V_{CE} = 10 V I_C = 1.0 mA, V_{CE} = 10 V I_C = 10 mA, V_{CE} = 10 V I_C = 150 mA, V_{CE} = 10 V* I_C = 500 mA, V_{CE} = 10 V*	75 100 100 100 50	 300 	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage*	I_C = 150 mA, I_B = 15 mA I_C = 500 mA, I_B = 50 mA		0.4 1.6	V V
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	I_C = 150 mA, I_B = 15 mA* I_C = 500 mA, I_B = 50 mA		1.3 2.6	V V
SMALL SIGNAL CHARACTERISTICS (except MMPQ2907 and NMT2907)					
f_T	Current Gain - Bandwidth Product	I_C = 50 mA, V_{CE} = 20 V, f = 100 MHz	200		MHz
C_{obo}	Output Capacitance	V_{CB} = 10 V, I_E = 0, f = 100 kHz		8.0	pF
C_{ibo}	Input Capacitance	V_{EB} = 2.0 V, I_C = 0, f = 100 kHz		30	pF
SWITCHING CHARACTERISTICS (except MMPQ2907 and NMT2907)					
t_{on}	Turn-on Time	V_{CC} = 30 V, I_C = 150 mA, I_{B1} = 15 mA		45	ns
t_d	Delay Time			10	ns
t_r	Rise Time			40	ns
t_{off}	Turn-off Time	V_{CC} = 6.0 V, I_C = 150 mA, I_{B1} = I_{B2} = 15 mA		100	ns
t_s	Storage Time			80	ns
t_f	Fall Time			30	ns

*Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%

Spice Model

PNP (Is=650.6E-18 Xti=3 Eg=1.11 Vaf=115.7 Bf=231.7 Ne=1.829 Ise=54.81f Ikf=1.079 Xtb=1.5 Br=3.563 Nc=2 Isc=0 Ikr=0 Rc=.715 Cjc=14.76p Mjc=.5383 Vjc=.75 Fc=.5 Cje=19.82p Mje=.3357 Vje=.75 Tr=111.3n Tf=603.7p Itf=.65 Vtf=5 Xtf=1.7 Rb=10)

PNP General Purpose Amplifier
(continued)

Thermal Characteristics
TA = 25°C unless otherwise noted

Symbol	Characteristic	Max		Units
		PN2907A	*PZT2907A	
P_D	Total Device Dissipation Derate above 25°C	625 5.0	1,000 8.0	mW mW/°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	83.3		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	200	125	°C/W

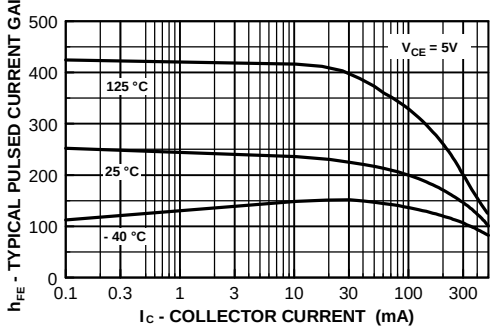
Symbol	Characteristic	Max		Units
		**MMBT2907A	MMPQ2907	
P_D	Total Device Dissipation Derate above 25°C	350 2.8	1,000 8.0	mW mW/°C
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient Effective 4 Die Each Die	357	 125 240	°C/W °C/W °C/W

*Device mounted on FR-4 PCB 36 mm X 18 mm X 1.5 mm; mounting pad for the collector lead min. 6 cm^2.

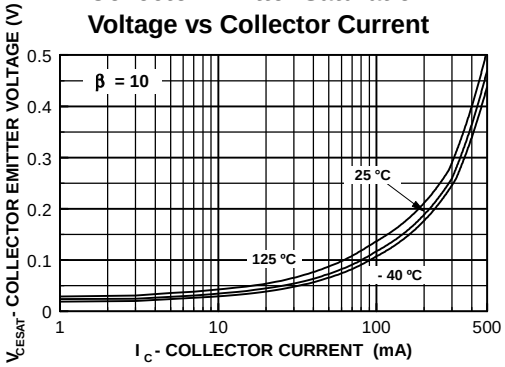
**Device mounted on FR-4 PCB 1.6" X 1.6" X 0.06."

Typical Characteristics

Typical Pulsed Current Gain vs Collector Current

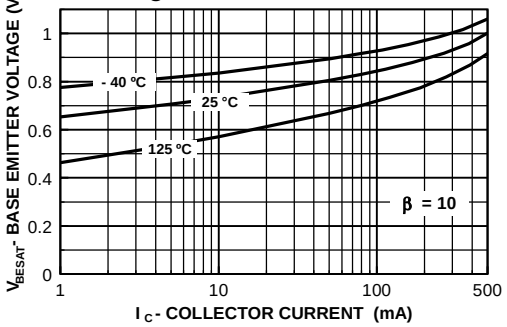


Collector-Emitter Saturation Voltage vs Collector Current

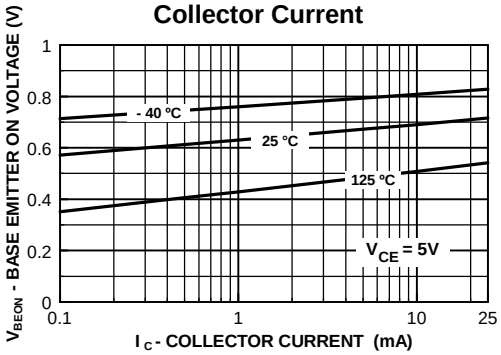


Typical Characteristics (continued)

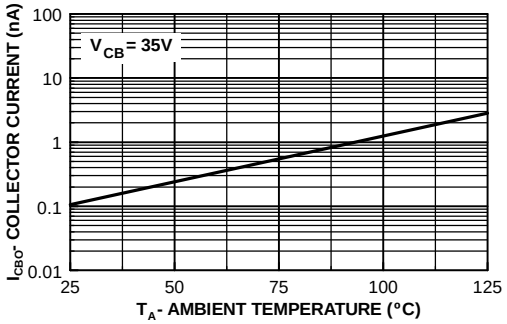
Base-Emitter Saturation Voltage vs Collector Current



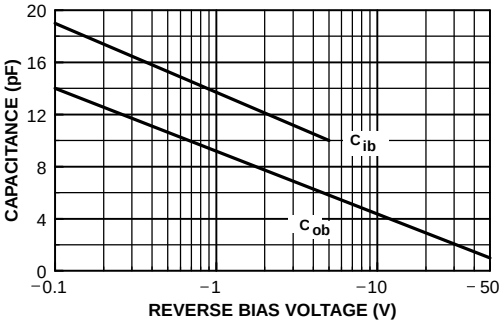
Base Emitter ON Voltage vs Collector Current



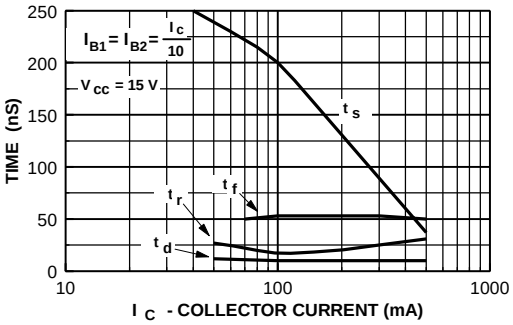
Collector-Cutoff Current vs. Ambient Temperature



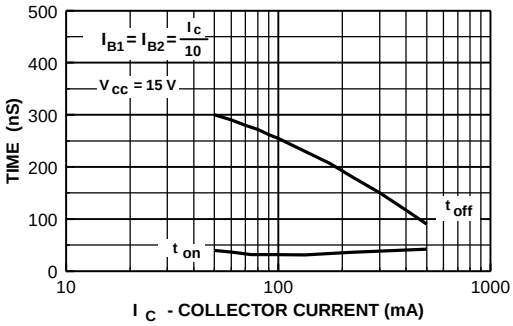
Input and Output Capacitance vs Reverse Bias Voltage



Switching Times vs Collector Current

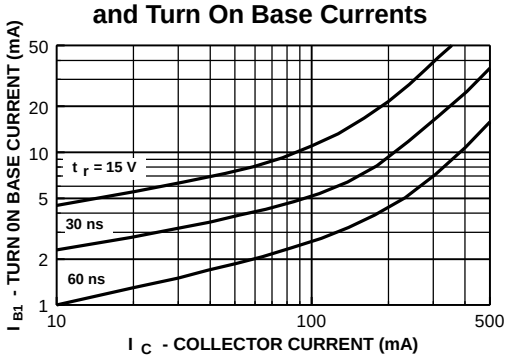


Turn On and Turn Off Times vs Collector Current

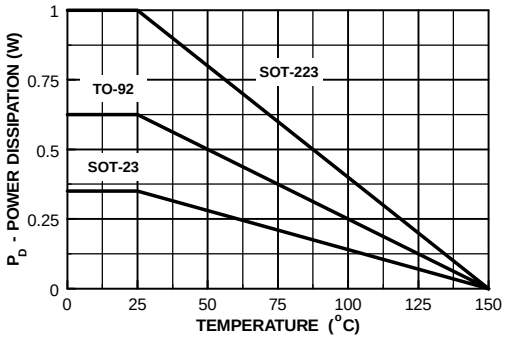


Typical Characteristics (continued)

Rise Time vs Collector and Turn On Base Currents



Power Dissipation vs Ambient Temperature



Test Circuits

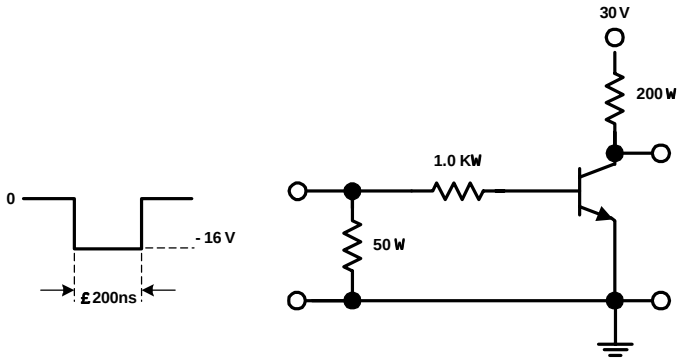


FIGURE 1: Saturated Turn-On Switching Time Test Circuit

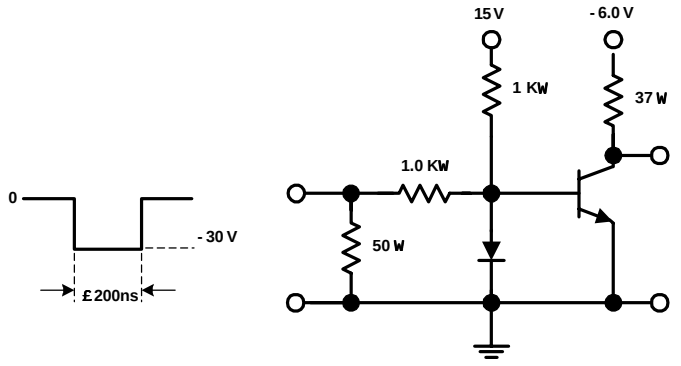


FIGURE 2: Saturated Turn-Off Switching Time Test Circuit

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MICROWIRE™
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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.