THIRD DOMAIN INCORPORATED

DIGITAL VIDEO SYNCHRONIZER
XTAL OSCILLATOR PHASE SELECTOR
RCS **-401** F

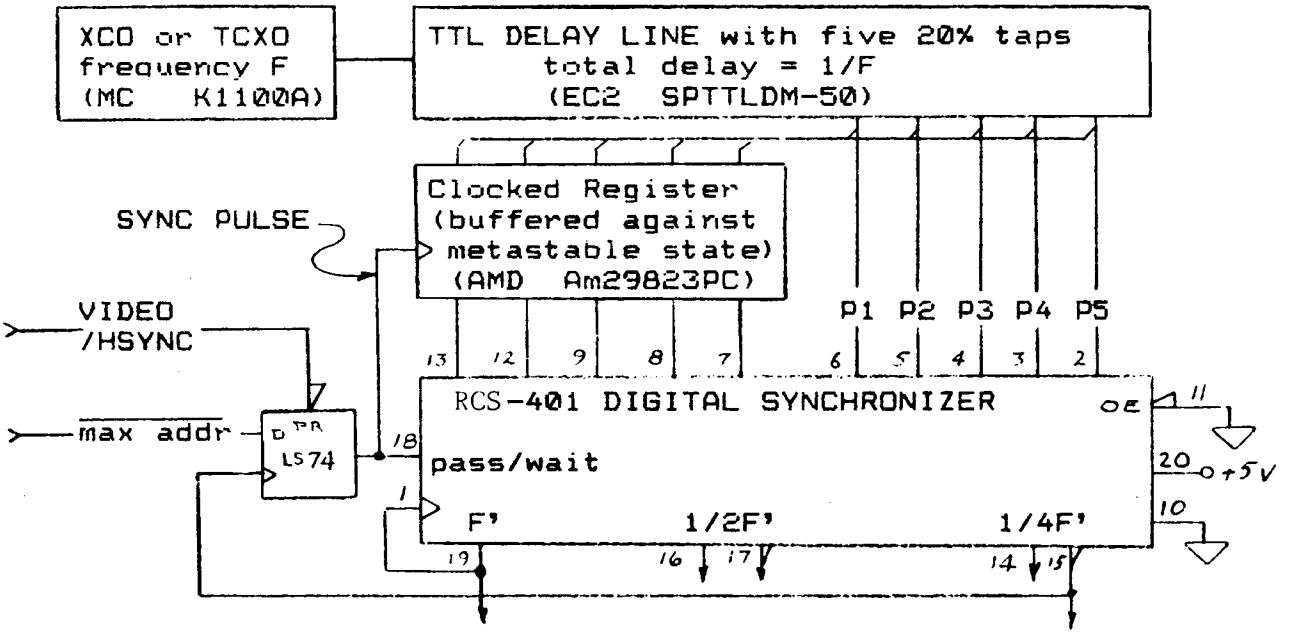
ENGINEERING DATA

DESCRIPTION

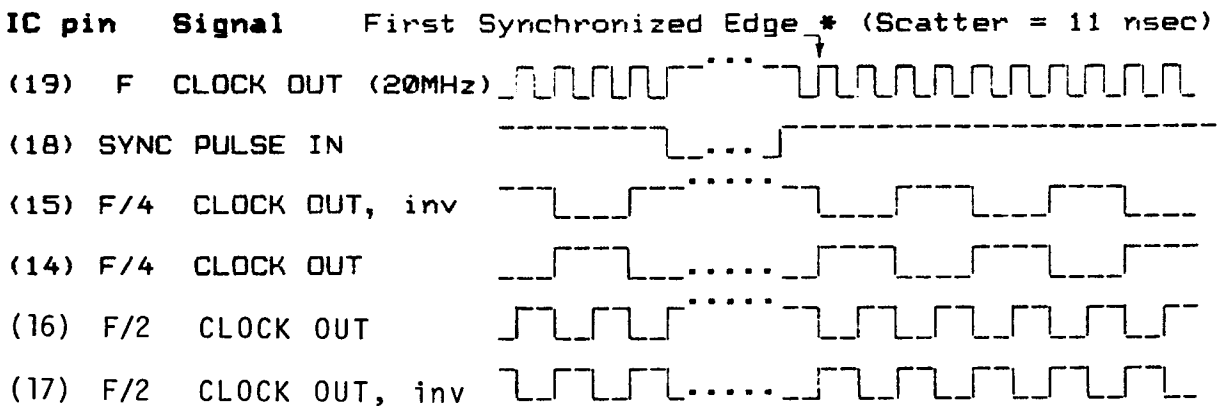
The RCS-401 synchronizes a fixed-frequency Crystal Controlled Clock Oscillator (XCO) to any relatively long-period asynchronous TTL pulse. Its operating range is designed to synchronize 2x multiples of all the sample clock frequencies that are commonly used in Video Digitizers.

MODE OF OPERATION

Three external components are necessary in addition to the RCS-401 in a synchronizer circuit. An oscillator of the XCO or TCXO type, a five-tap TTL delay module one clock period in length, and a clocked register that is buffered against metastable states. These four components are connected in the manner shown below:



The RCS-401 generates three frequencies separated by binary factors. The highest of the three is equal to the input frequency (F) from the XCO. The lower two are 1/2F and 1/4F subharmonics. Each of the three output signals is phase-locked to the sync pulse, and all cycles are whole and well-defined with respect to the active edge of the sync pulse as shown by the timing diagram on the next page.



There are many important differences that favor the digital RCS-401 over analog Phase-locked Loops (PLL). Primarily, the digital RCS-401 synchronizes a very stable XCO or an extremely stable temperature-controlled TCXO. The PLL circuit requires a Variable-Control Oscillator (VCO) which is much less stable than the XCO types. The RCS-401 locks onto its selected phase exactly 75 nsec after each synchronizing signal. The PLL is inherently unable to lock, it is always "searching", and its acquisition time can sometimes require several cycles of sync pulses. The RCS-401 creates no short pulses (ambiguous spikes), since its outputs hold at predefined levels during its "wait-for-next-sync" period. The PLL will generate long or short pulses at each sync moment and some circuits will glitch. Restartable oscillators will not glitch but they have the lack of stablity inherent in their RC multivibrators. The RCS-401 will not lose control when sync pulse period irregularities exceed one clock period. Under these conditions an ordinary PLL loses its capacity to distinguish "lead/lag".

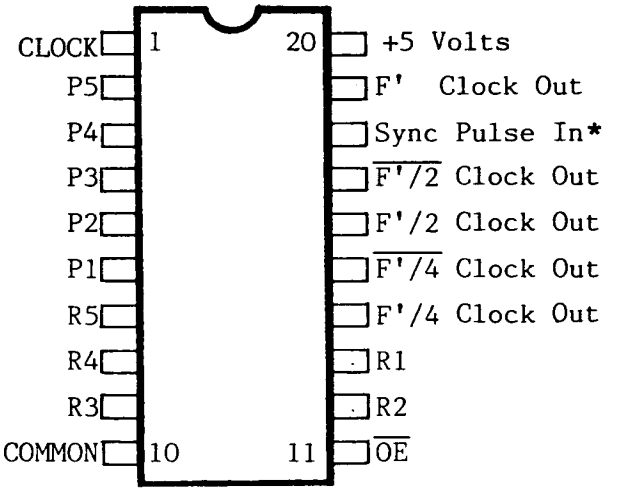
All synchronizers, whether digital or analog, provide precise measures of elapsed time between a "synchronizing" event and a sequential stream of "data" events. The uncertainty of this measure is an important factor in design decisions. In digital video, clock-to-sync uncertainty has the effect of blurring pixel boundaries; so the designer of high resolution video must try to hold worst case uncertainty below 15% of pixel width.

Worst Case Uncertainty (U), at time (T) for clock frequency (F) and oscillator stablity (P) percent, where sync lock phase error is given by 1/nF, and where the stablity window is given by PT:

For the RSS-401: U = 1/5F + PT Example: F = 20MHz T = 50 usec
For the PLL: U = 1/2F + PT P = .002% U = 11 nsec

In cases where the Sync is a stable and undistorted subharmonic of the Clock, the lock error terms drop to zero and the worst case uncertainty narrows to PT alone, where the XCO in the RCS-401 circuit has a clear stability advantage over the VCO in the PLL circuit. However where higher levels of uncertainty are acceptable, PLL circuits have the advantage of lower cost.

CONNECTIONS:



NOTE: Refer to the "Mode of Operation" section for exact use of the pin connections and their functions.

* The Sync-Pulse Input functions as a: pass/wait

ABSOLUTE MAXIMUM RATINGS:

Digital Supply Voltage (Pin 20 to 10)	+ 7.0 Volts
Input Voltage (Pins 1 -9, 11, 12, 13 & 18)	+ 5.5 Volts
Output Short Circuit Current (Pins 14 - 17, 19)	+ 130 mA
Output Low-State Voltage	+ 5.5 Volts
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Note: Absolute maximum ratings are those voltage, current and temperature levels beyond which permanent damage may result. Consult the Specifications and Mode of OPeration sections for conditions of normal operation.

PERIPHERAL COMPONENTS:

Proper operation is only attained if the components shown in the "Mode of Operation" section are used. The Clocked Register is a Am29823PC [AMD - Advanced Micro Devices] and the Delay LIne is SPTTLDM-XX (where XX is the period of the clock, 1/F, in nanoseconds), manufactured by Engineered Components Company.

SPECIFICATIONS:

+VL = +5 Volts, T_A = +25°C, unless otherwise specified

Parameter	Minimum	Typical	Maximum	Units
INPUT:				
Low level voltage			0.8	Volts
High level Voltage	2.0			Volts
Clamp Voltage		-0.8	-1.5	Volts
Low level Current		-0.02	-0.25	milliamps
High level Current			25	microamps
Maximum Current			1	milliamp
OUTPUT:				
Low level Voltage		0.3	0.5	Volts
High level Voltage	2.4	2.8		Volts
Low level Current		24		milliamps
High level Current		-3.2		milliamps
DYNAMICS:				
Clock Frequency [F]			40	MHz
Output Enable		8	15	nSec
Output Disable		8	15	nSec
Clock-to-Output		8	12	nSec
POWER SUPPLY:				
+VL Voltage Range	4.75	5	5.25	Volts
Supply Current		120	180	milliamps
Dissipation		600		milliwatts