μPD4311
16,384 x 1-BIT STATIC CMOS RAM

Description

The μPD4311 is a 16,384-word by 1-bit static random access memory fabricated with advanced silicon-gate technology. Its unique circuitry, using CMOS peripheral circuits and N-channel memory cells with polysilicon resistors, makes the μPD4311 a high-speed device that requires very low power and no clock or refreshing to operate.

The μPD4311 is packaged in a 20-pin plastic DIP.

Features

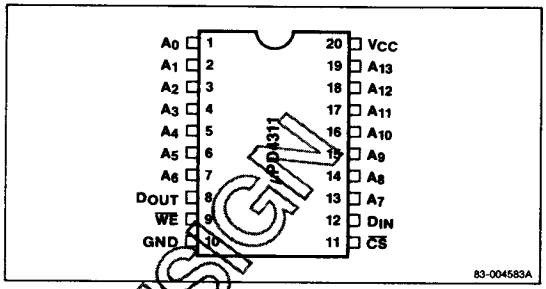
- ☐ Single +5-volt supply
- ☐ Fully static operation — no clock or refreshing required
- ☐ TTL-compatible inputs and outputs
- ☐ Separated data input and output
- ☐ Three-state output
- ☐ Low power dissipation
  - — 80 mA max (active)
  - — 2 mA max (standby)
- ☐ Standard 300-mil, 20-pin plastic DIP

Ordering Information

Part Number	Access Time (max)	Package
μPD4311C-35	35 ns	20-pin plastic DIP
C-45	45 ns	
C-55	55 ns	

Pin Configuration

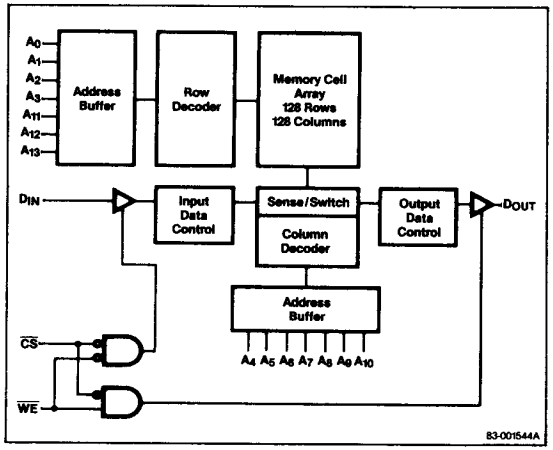
20-Pin Plastic DIP



Pin Identification

Symbol	Function
A_0-A_{13}	Address inputs
D_{IN}	Data input
D_{OUT}	Data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply

Block Diagram



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Absolute Maximum Ratings

Power supply voltage, V_{CC}	−0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	−0.5 to +7.0 V
Output voltage, V_{OUT}	−0.5 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Power dissipation, P_D	1.0 W

Notes:

(1) V_{IN} = −3.0 V min for 20 ns maximum pulse.

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC characteristics.

Capacitance

T_A = 25°C; f = 1 MHz (Note 1)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}			5	pF	V_{IN} = 0 V
Data output capacitance	C_{DOUT}			6	pF	V_{DOUT} = 0 V

Notes:

(1) This parameter is sampled and not 100% tested.

Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	I/O	I_{CC}
H	X	Not selected	Hi-Z	Standby
L	H	Read	D_{OUT}	Active
L	L	Write	Hi-Z	Active

Recommended DC Operating Conditions

T_A = 0 to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low (Note 1)	V_{IL}	−0.5		0.8	V
Input voltage, high	V_{IH}	2.2		6.0	V

Notes:

(1) V_{IL} = −3.0 V min for 20 ns maximum pulse.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}; V_{CC} = max
Output leakage current	I_{LO}	−2		2	μA	V_{OUT} = 0 V to V_{CC}; $\overline{CS}$ = V_{IH}; V_{CC} = max
Operating supply current	I_{CC}			80	mA	$\overline{CS}$ = V_{IL}; I_{DOUT} = 0 mA
Standby supply current	I_{SB}			15	mA	$\overline{CS}$ = V_{IH}
Standby supply current	I_{SB1}			2	mA	$\overline{CS}$ = V_{CC} − 0.2 V; V_{IN} ≤ 0.2 V or ≥ V_{CC} − 0.2 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

AC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0\ V \pm 10\%$

Parameter	Symbol	Limits μPD4311-35 Min	Limits μPD4311-35 Max	Limits μPD4311-45 Min	Limits μPD4311-45 Max	Limits μPD4311-55 Min	Limits μPD4311-55 Max	Unit	Test Conditions (Note 1)
Read Cycle									
Read cycle time	t_{RC}	35		45		55		ns	(Note 2)
Address access time	t_{AA}		35		45		55	ns	
Chip select access time	t_{ACS}		35		45		55	ns	
Output hold from address change	t_{OH}	5		5		5		ns	
Chip select to output in Lo-Z	t_{LZ}	5		5		5		ns	(Note 3)
Chip deselect to output in Hi-Z	t_{HZ}	0	20	0	25	0	30	ns	(Note 4)
Chip select to power-up time	t_{PU}	0		0		0		ns	
Chip deselect to power-down time	t_{PD}	0	35	0	40	0	45	ns	
Write Cycle									
Write cycle time	t_{WC}	35		45		55		ns	(Note 2)
Chip select to end of write	t_{CW}	35		40		45		ns	
Address valid to end of write	t_{AW}	35		40		45		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	25		30		35		ns	
Write recovery time	t_{WR}	0		0		0		ns	
Data valid to end of write	t_{DW}	20		25		25		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write enable to output in Hi-Z	t_{WZ}	0	20	0	25	0	30	ns	(Note 4)
Output active from end of write	t_{OW}	0		0		0		ns	(Note 3)

Notes:

(1) Input pulse levels = GND to 3.0 V
Input pulse rise and fall times = 5 ns
Timing reference levels = 1.5 V; see figures 1 and 2 for the output load.

(2) All read and write cycle timings are referenced from the last valid address to the first transitioning address.

(3) The transition is measured ±200 mV from steady state voltage with the loading shown in figure 2.

(4) The transition is measured at V_{OL} +200 mV and V_{OH} −200 mV with the loading shown in figure 2.

Figure 1. Output Load

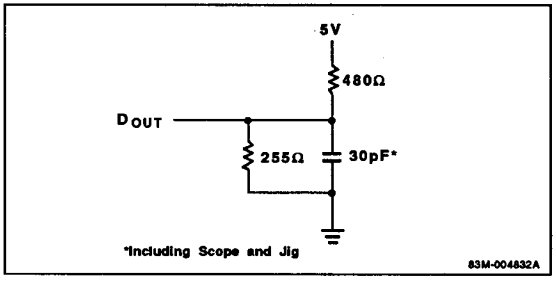
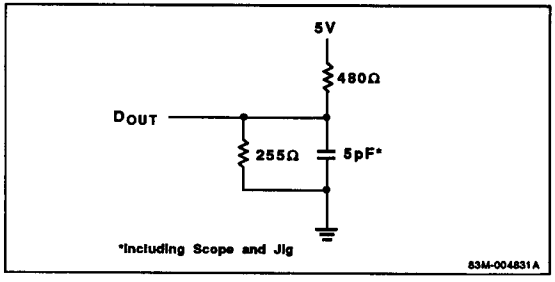
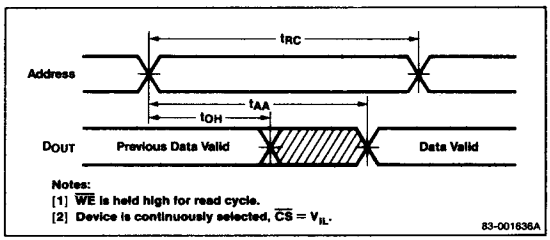


Figure 2. Output Load for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}



Timing Waveforms

Read Cycle No. 1 (Address Access)



Notes:
[1] $\overline{WE}$ is held high for read cycle.
[2] Device is continuously selected, $\overline{CS} = V_{IL}$.

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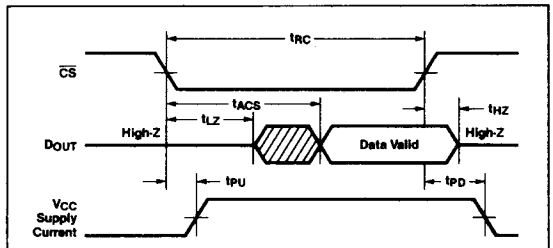
Read Cycle No.2 (Chip Select Access)



Notes: [1] $\overline{WE}$ is held high for read cycle.
[2] Address valid prior to or coincident with $\overline{CS}$ transition low.

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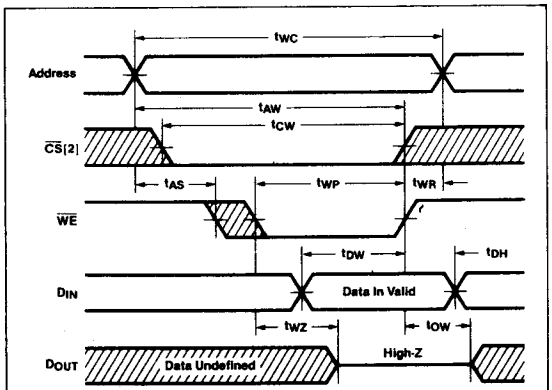
Write Cycle No. 1 ($\overline{WE}$ Controlled)



Note:
[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.
[2] If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the outputs remain in a high-impedance state.

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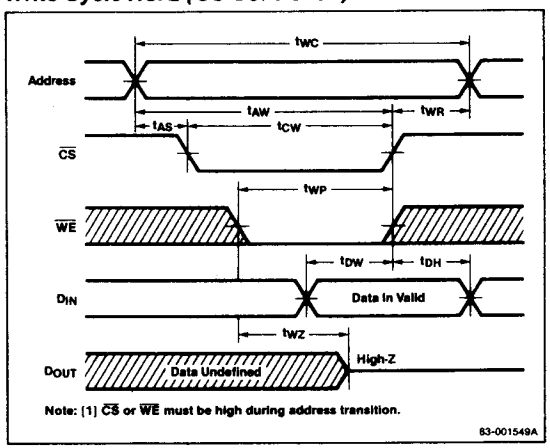
Write Cycle No. 2 ($\overline{CS}$ Controlled)



Note: [1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

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