SPANSION™ Flash Memory

Data Sheet

September 2003

This document specifies SPANSION™ memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this datasheet as a result of offering the device as a SPANSION™ product. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about SPANSION™ memory solutions.

DS05-20888-6E

FLASH MEMORY

CMOS

8 M (1 M × 8/512 K × 16) BIT

MBM29LV800TE60/70/90/MBM29LV800BE60/70/90

■ DESCRIPTION

The MBM29LV800TE/BE are a 8 M-bit, 3.0 V-only Flash memory organized as 1 M bytes of 8 bits each or 512 Kwords of 16 bits each. The MBM29LV800TE/BE are offered in a 48-pin TSOP (1) , 48-pin CSOP and 48-ball FBGA package. These devices are designed to be programmed in a system with the standard system 3.0 V V_{CC} supply. 12.0 V V_{PP} and 5.0 V V_{CC} are not required for write or erase operations. The devices can also be reprogrammed in standard EPROM programmers.

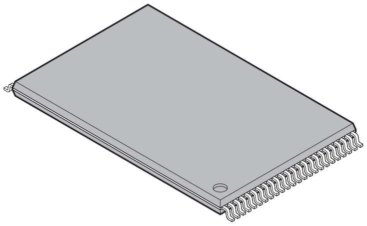
(Continued)

■ PRODUCT LINE UP

Part No.		MBM29LV800TE/BE		
Ordering Part No.	$V_{CC} = 3.3\ V^{+0.3\ V}_{-0.3\ V}$	60	—	—
	$V_{CC} = 3.0\ V^{+0.6\ V}_{-0.3\ V}$	—	70	90
Max Address Access Time (ns)		60	70	90
Max $\overline{CE}$ Access Time (ns)		60	70	90
Max $\overline{OE}$ Access Time (ns)		30	30	35

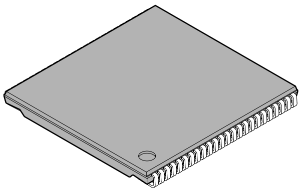
■ PACKAGES

48-pin Plastic TSOP (1)



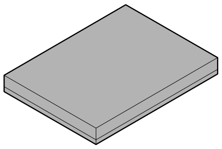
(FPT-48P-M19)

48-pin Plastic CSOP



(LCC-48P-M03)

48-ball Plastic FBGA



(BGA-48P-M20)

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The standard MBM29LV800TE/BE offer access times 60 ns, 70 ns and 90 ns, allowing operation of high-speed microprocessors without wait state. To eliminate bus contention, the devices have separate chip enable ($\overline{CE}$) , write enable ($\overline{WE}$) , and output enable ($\overline{OE}$) controls.

The MBM29LV800TE/BE are pin and command set compatible with JEDEC standard E^2PROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the devices is similar to reading from 5.0 V and 12.0 V Flash or EPROM devices.

The MBM29LV800TE/BE are programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Typically, each sector can be programmed and verified in about 0.5 seconds. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the devices automatically time the erase pulse widths and verify proper cell margin.

A sector is typically erased and verified in 1.0 second. (If already completely preprogrammed.)

The devices also feature a sector erase architecture. The sector mode allows each sector to be erased and reprogrammed without affecting other sectors. The MBM29LV800TE/BE are erased when shipped from the factory.

The devices feature single 3.0 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by $\overline{\text{Data}}$ Polling of DQ_7, by the Toggle Bit feature on DQ_6, or the RY/$\overline{BY}$ output pin. Once the end of a program or erase cycle has been completed, the devices internally resets to the read mode.

The MBM29LV800TE/BE also have hardware $\overline{RESET}$ pins. When this pin is driven low, execution of any Embedded Program Algorithm or Embedded Erase Algorithm is terminated. The internal state machine is then reset to the read mode. The $\overline{RESET}$ pin may be tied to the system reset circuitry. Therefore, if a system reset occurs during the Embedded Program Algorithm or Embedded Erase Algorithm, the device is automatically reset to the read mode and will have erroneous data stored in the address locations being programmed or erased. These locations need re-writing after the Reset. Resetting the device enables the system's microprocessor to read the boot-up firmware from the Flash memory.

Fujitsu's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability, and cost effectiveness. The MBM29LV800TE/BE memory electrically erase all bits within a sector simultaneously via Fowler-Nordhiem tunneling. The bytes/words are programmed one byte/word at a time using the EPROM programming mechanism of hot electron injection.

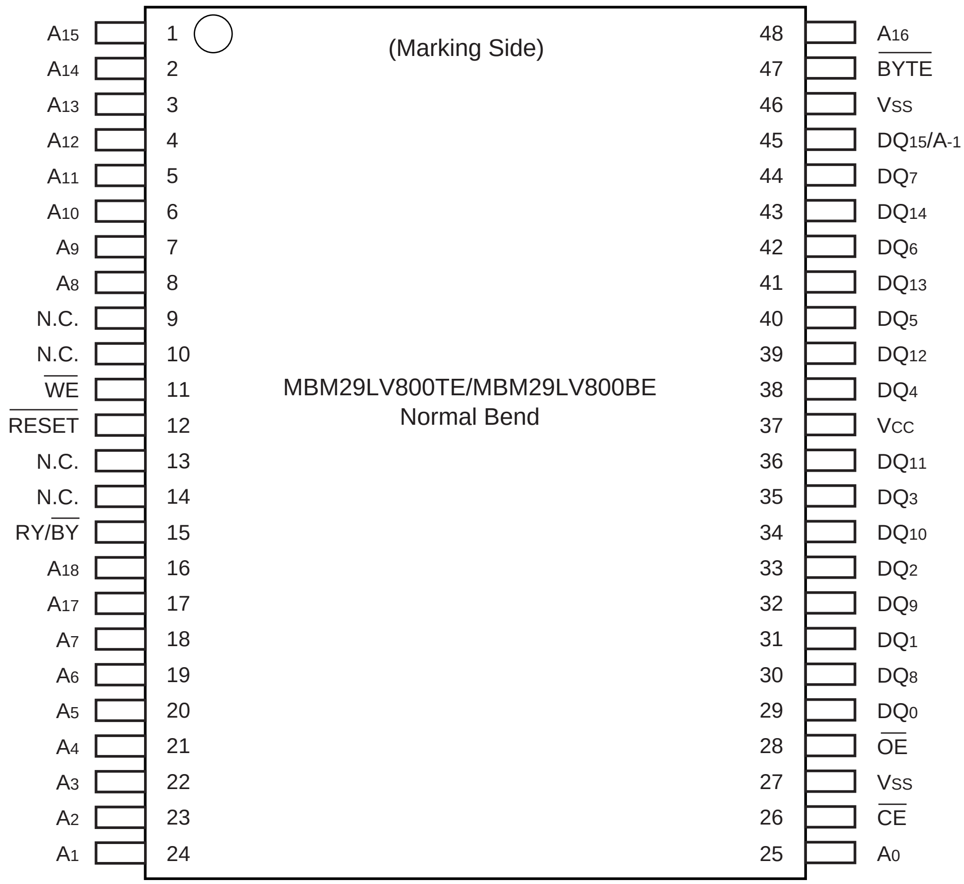
■ FEATURES

- **0.23 µm Process Technology**
- **Single 3.0 V Read, Program, and Erase**
  Minimized system level power requirements
- **Compatible with JEDEC-standard Commands**
  Use the same software commands as E^2PROMs
- **Compatible with JEDEC-standard World-wide Pinouts**
  48-pin TSOP (1) (Package suffix : TN Normal Bend Type)
  48-pin CSOP (Package suffix : PCV)
  48-ball FBGA (Package suffix : PBT)
- **Minimum 100,000 Program/Erase Cycles**
- **High Performance**
  70 ns maximum access time
- **Sector Erase Architecture**
  One 8 Kwords, two 4 Kwords, one 16 Kwords, and fifteen 32 Kwords sectors in word mode
  One 16 Kbytes, two 8 Kbytes, one 32 Kbytes, and fifteen 64 Kbytes sectors in byte mode
  Any combination of sectors can be concurrently erased, and also supports full chip erase.
- **Boot Code Sector Architecture**
  T = Top sector
  B = Bottom sector
- **Embedded Erase™* Algorithm**
  Automatically pre-programs and erases the chip or any sector.
- **Embedded Program™* Algorithm**
  Automatically writes and verifies data at specified address.
- **$\overline{\text{Data}}$ Polling and Toggle Bit Feature for Detection of Program or Erase Cycle Completion**
- **Ready/Busy Output (RY/$\overline{\text{BY}}$)**
  Hardware method for detection of program or erase cycle completion
- **Automatic Sleep Mode**
  When addresses remain stable, MBM29LV800TE/BE automatically switch themselves to low power mode.
- **Low V_{CC} Write Inhibit ≤ 2.5 V**
- **Erase Suspend/Resume**
  Suspends the erase operation to allow a read data and/or program in another sector within the same device.
- **Sector Protection**
  Hardware method disables any combination of sectors from program or erase operations.
- **Sector Protection Set Function by Extended Sector Protection Command**
- **Fast Programming Function by Extended Command**
- **Temporary Sector Unprotection**
  Temporary sector unprotection via the $\overline{\text{RESET}}$ pin

* : Embedde Erase™ and Embedded Program™ are trademarks of Advanced Micro Devices, Inc.

■ PIN ASSIGNMENTS

TSOP (1)



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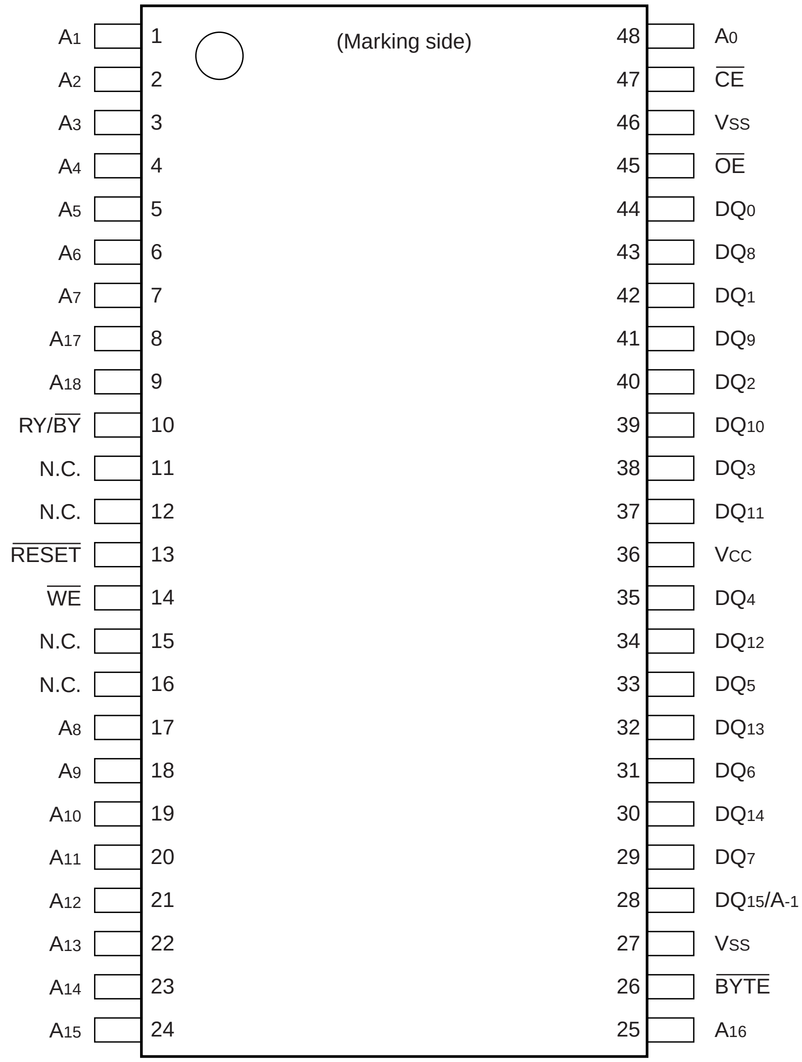
CSOP
(TOP VIEW)



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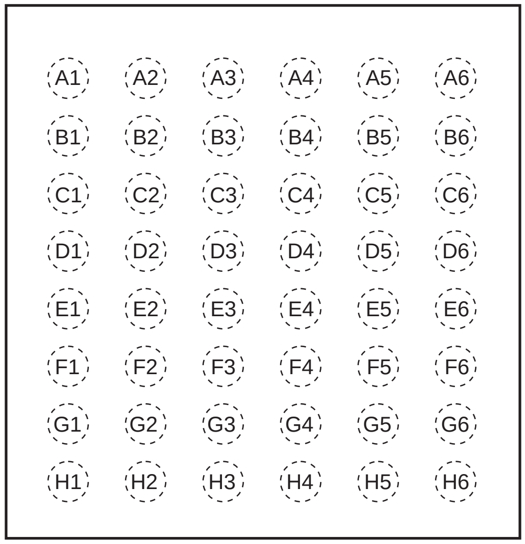
FBGA
(TOP VIEW)
Marking side



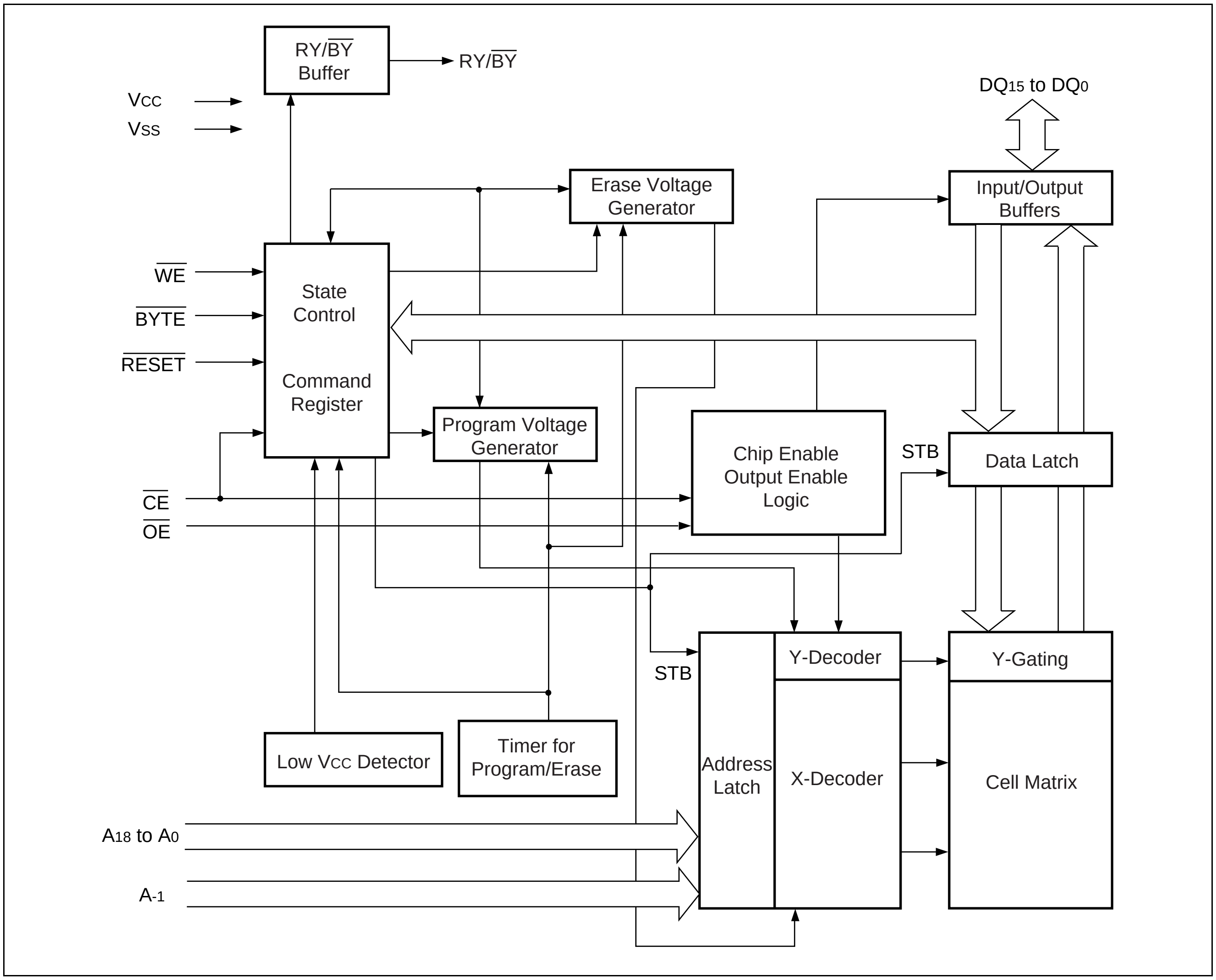
(BGA-48P-M20)

A1	A_3	A2	A_7	A3	RY/$\overline{BY}$	A4	$\overline{WE}$	A5	A_9	A6	A_{13}
B1	A_4	B2	A_{17}	B3	N.C.	B4	$\overline{RESET}$	B5	A_8	B6	A_{12}
C1	A_2	C2	A_6	C3	A_{18}	C4	N.C.	C5	A_{10}	C6	A_{14}
D1	A_1	D2	A_5	D3	N.C.	D4	N.C.	D5	A_{11}	D6	A_{15}
E1	A_0	E2	DQ_0	E3	DQ_2	E4	DQ_5	E5	DQ_7	E6	A_{16}
F1	$\overline{CE}$	F2	DQ_8	F3	DQ_{10}	F4	DQ_{12}	F5	DQ_{14}	F6	$\overline{BYTE}$
G1	$\overline{OE}$	G2	DQ_9	G3	DQ_{11}	G4	V_{CC}	G5	DQ_{13}	G6	DQ_{15}/A_{-1}
H1	V_{SS}	H2	DQ_1	H3	DQ_3	H4	DQ_4	H5	DQ_6	H6	V_{SS}

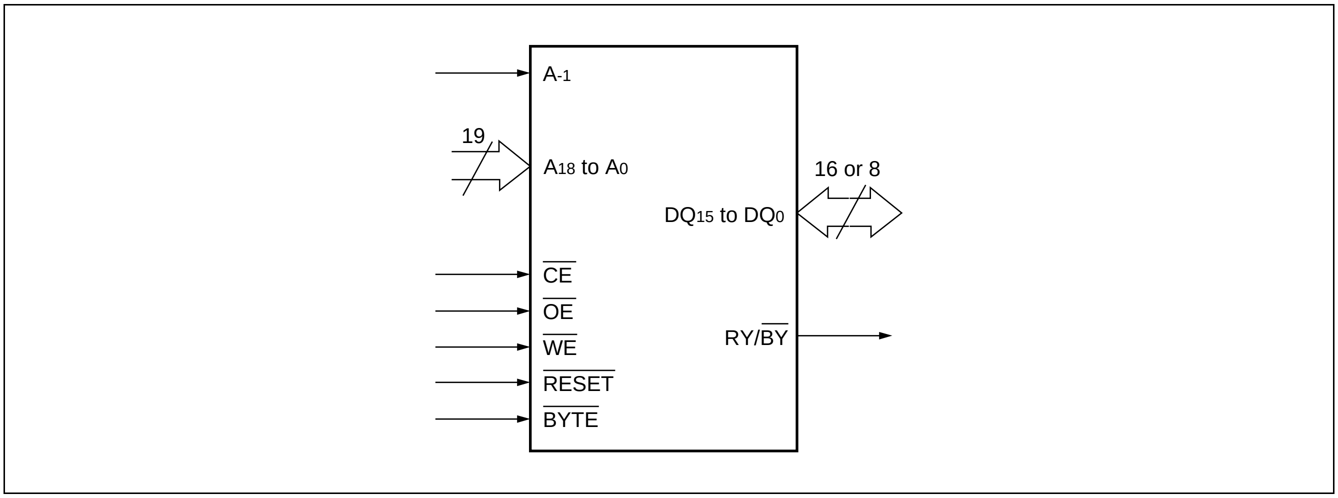
■ PIN DESCRIPTION

Pin name	Function
A_{18} to A_0, A_{-1}	Address Inputs
DQ_{15} to DQ_0	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
RY/$\overline{BY}$	Ready/Busy Output
$\overline{RESET}$	Hardware Reset Pin/Temporary Sector Unprotection
$\overline{BYTE}$	Selects 8-bit or 16-bit mode
N.C.	No Internal Connection
V_{SS}	Device Ground
V_{CC}	Device Power Supply

■ BLOCK DIAGRAM



■ LOGIC SYMBOL



■ DEVICE BUS OPERATION

MBM29LV800TE/BE User Bus Operations ($\overline{BYTE}$ = V_{IH})

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A_0	A_1	A_6	A_9	DQ_{15} to DQ_0	$\overline{RESET}$
Auto-Select Manufacturer Code *1	L	L	H	L	L	L	V_{ID}	Code	H
Auto-Select Device Code *1	L	L	H	H	L	L	V_{ID}	Code	H
Read *3	L	L	H	A_0	A_1	A_6	A_9	D_{OUT}	H
Standby	H	X	X	X	X	X	X	High-Z	H
Output Disable	L	H	H	X	X	X	X	High-Z	H
Write (Program/Erase)	L	H	L	A_0	A_1	A_6	A_9	D_{IN}	H
Enable Sector Protection *2, *4	L	V_{ID}		L	H	L	V_{ID}	X	H
Verify Sector Protection *2, *4	L	L	H	L	H	L	V_{ID}	Code	H
Temporary Sector Unprotection*5	X	X	X	X	X	X	X	X	V_{ID}
Reset (Hardware) /Standby	X	X	X	X	X	X	X	High-Z	L

Legend : L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}, = Pulse input. See "■ DC CHARACTERISTICS" for voltage levels.

*1: Manufacturer and device codes may also be accessed via a command register write sequence.
See "Sector Address Tables (MBM29LV800BE) " in "■ FLEXIBLE SECTOR-ERASE ARCHITECTURE".

*2: Refer to Sector Protection.

*3: $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.

*4: V_{CC} = 3.0 V to 3.6 V (MBM29LV800TE/BE 60)
= 2.7 V to 3.6 V (MBM29LV800TE/BE 70/90)

*5: Also used for the extended sector protection.

MBM29LV800TE/BE User Bus Operations ($\overline{BYTE} = V_{IL}$)

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	DQ_{15}/ A_{-1}	A_0	A_1	A_6	A_9	DQ_7 to DQ_0	$\overline{RESET}$
Auto-Select Manufacturer Code *1	L	L	H	L	L	L	L	V_{ID}	Code	H
Auto-Select Device Code *1	L	L	H	L	H	L	L	V_{ID}	Code	H
Read *3	L	L	H	A_{-1}	A_0	A_1	A_6	A_9	D_{OUT}	H
Standby	H	X	X	X	X	X	X	X	High-Z	H
Output Disable	L	H	H	X	X	X	X	X	High-Z	H
Write (Program/Erase)	L	H	L	A_{-1}	A_0	A_1	A_6	A_9	D_{IN}	H
Enable Sector Protection *2, *4	L	V_{ID}		L	L	H	L	V_{ID}	X	H
Verify Sector Protection *2, *4	L	L	H	L	L	H	L	V_{ID}	Code	H
Temporary Sector Unprotection *5	X	X	X	X	X	X	X	X	X	V_{ID}
Reset (Hardware) /Standby	X	X	X	X	X	X	X	X	High-Z	L

Legend : L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}, = Pulse input. See "■ DC CHARACTERISTICS" for voltage levels.

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= 2.7 V to 3.6 V (MBM29LV800TE/BE 70/90)

*5: Also used for the extended sector protection.

MBM29LV800TE/BE Command Definitions

Command Sequence		Bus Write Cycles Req'd	First Bus Write Cycle Addr.	First Bus Write Cycle Data	Second Bus Write Cycle Addr.	Second Bus Write Cycle Data	Third Bus Write Cycle Addr.	Third Bus Write Cycle Data	Fourth Bus Read/Write Cycle Addr.	Fourth Bus Read/Write Cycle Data	Fifth Bus Write Cycle Addr.	Fifth Bus Write Cycle Data	Sixth Bus Write Cycle Addr.	Sixth Bus Write Cycle Data
Read/Reset*1	Word	1	XXXh	F0h	—	—	—	—	—	—	—	—	—	—
	Byte													
Read/Reset*1	Word	3	555h	AAh	2AAh	55h	555h	F0h	RA*5	RD*5	—	—	—	—
	Byte		AAAh		555h		AAAh							
Autoselect	Word	3	555h	AAh	2AAh	55h	555h	90h	IA*5	ID*5	—	—	—	—
	Byte		AAAh		555h		AAAh							
Program	Word	4	555h	AAh	2AAh	55h	555h	A0h	PA	PD	—	—	—	—
	Byte		AAAh		555h		AAAh							
Chip Erase	Word	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h
	Byte		AAAh		555h		AAAh		AAAh		555h		AAAh	
Sector Erase	Word	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	SA	30h
	Byte		AAAh		555h		AAAh		AAAh		555h			
Erase Suspend		1	XXXh	B0h	—	—	—	—	—	—	—	—	—	—
Erase Resume		1	XXXh	30h	—	—	—	—	—	—	—	—	—	—
Set to Fast Mode	Word	3	555h	AAh	2AAh	55h	555h	20h	—	—	—	—	—	—
	Byte		AAAh		555h		AAAh							
Fast Program*2	Word	2	XXXh	A0h	PA	PD	—	—	—	—	—	—	—	—
	Byte		XXXh											
Reset from Fast Mode*2	Word	2	XXXh	90h	XXXh	*4 F0h	—	—	—	—	—	—	—	—
	Byte		XXXh		XXXh									
Extended Sector Protection*3	Word	3	XXXh	60h	SPA	60h	SPA	40h	SPA*5	SD*5	—	—	—	—
	Byte													

*1 : Both of these reset commands are equivalent.

*2 : This command is valid during Fast Mode.

*3 : This command is valid while $\overline{RESET}$ = V_{ID} (except during HiddenROM MODE) .

*4 : The data "00h" is also acceptable.

*5 : The fourth bus cycle is only for read.

Notes :
- Address bits A_{18} to A_{11} = X = "H" or "L" for all address commands except or Program Address (PA) and Sector Address (SA) .
- Bus operations are defined in "MBM29LV800TE/BE User Bus Operations ($\overline{BYTE}$ = V_{IH})" and "MBM29LV800TE/BE User Bus Operations ($\overline{BYTE}$ = V_{IL})".
- RA = Address of the memory location to be read.
  IA = Autoselect read address that sets A_6, A_1, A_0.
  PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
  SA = Address of the sector to be erased. The combination of A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12} will uniquely select any sector.

- RD = Data read from location RA during read operation.
  ID = Device code/manufacture code for the address located by IA.
  PD = Data to be programmed at location PA. Data is latched on the rising edge of $\overline{WE}$.
- SPA = Sector address to be protected. Set sector address (SA) and (A_6, A_1, A_0) = (0, 1, 0) .
  SD = Sector protection verify data. Output 01h at protected sector addressed and output 00h at unprotected sector addresses.
- The system should generate the following address patterns :
  Word Mode : 555h or 2AAh to addresses A_{10} to A_0
  Byte Mode : AAAh or 555h to addresses A_{10} to A_{-1}
- Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.
- The command combinations not described in Command Definitions are illegal.

MBM29LV800TE/BE Sector Protection Verify Autoselect Codes

Type			A_{18} to A_{12}	A_6	A_1	A_0	A_{-1}*1	Code (HEX)
Manufacture's Code			X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	04h
Device Code	MBM29LV800TE	Byte	X	V_{IL}	V_{IL}	V_{IH}	V_{IL}	DAh
		Word					X	22DAh
	MBM29LV800BE	Byte	X	V_{IL}	V_{IL}	V_{IH}	V_{IL}	5Bh
		Word					X	225Bh
Sector Protection			Sector Addresses	V_{IL}	V_{IH}	V_{IL}	V_{IL}	01h*2

*1 : A_{-1} is for Byte mode. At Byte mode, DQ_{14} to DQ_8 are High-Z and DQ_{15} is A_{-1}, the lowest address.

*2 : Outputs 01h at protected sector addresses and outputs 00h at unprotected sector addresses.

Expanded Autoselect Code Table

Type			Code	DQ_{15}	DQ_{14}	DQ_{13}	DQ_{12}	DQ_{11}	DQ_{10}	DQ_9	DQ_8	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacturer's Code			04h	A_{-1}/0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Device Code	MBM29 LV800TE	(B)	DAh	A_{-1}	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	1	1	0	1	1	0	1	0
		(W)	22DAh	0	0	1	0	0	0	1	0	1	1	0	1	1	0	1	0
	MBM29 LV800BE	(B)	5Bh	A_{-1}	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	0	1	0	1	1	0	1	1
		(W)	225Bh	0	0	1	0	0	0	1	0	0	1	0	1	1	0	1	1
Sector Protection*			01h	A_{-1}/0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

* : At Byte mode, DQ_{14} to DQ_8 are High-Z and DQ_{15} is A_{-1}, the lowest address.
(B) : Byte mode
(W) : Word mode
HI-Z : High-Z

■ FLEXIBLE SECTOR-ERASE ARCHITECTURE

Sector Address Tables (MBM29LV800TE)

Sector Address	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	Address Range (×8)	Address Range (×16)
SA0	0	0	0	0	X	X	X	00000h to 0FFFFh	00000h to 07FFFh
SA1	0	0	0	1	X	X	X	10000h to 1FFFFh	08000h to 0FFFFh
SA2	0	0	1	0	X	X	X	20000h to 2FFFFh	10000h to 17FFFh
SA3	0	0	1	1	X	X	X	30000h to 3FFFFh	18000h to 1FFFFh
SA4	0	1	0	0	X	X	X	40000h to 4FFFFh	20000h to 27FFFh
SA5	0	1	0	1	X	X	X	50000h to 5FFFFh	28000h to 2FFFFh
SA6	0	1	1	0	X	X	X	60000h to 6FFFFh	30000h to 37FFFh
SA7	0	1	1	1	X	X	X	70000h to 7FFFFh	38000h to 3FFFFh
SA8	1	0	0	0	X	X	X	80000h to 8FFFFh	40000h to 47FFFh
SA9	1	0	0	1	X	X	X	90000h to 9FFFFh	48000h to 4FFFFh
SA10	1	0	1	0	X	X	X	A0000h to AFFFFh	50000h to 57FFFh
SA11	1	0	1	1	X	X	X	B0000h to BFFFFh	58000h to 5FFFFh
SA12	1	1	0	0	X	X	X	C0000h to CFFFFh	60000h to 67FFFh
SA13	1	1	0	1	X	X	X	D0000h to DFFFFh	68000h to 6FFFFh
SA14	1	1	1	0	X	X	X	E0000h to EFFFFh	70000h to 77FFFh
SA15	1	1	1	1	0	X	X	F0000h to F7FFFh	78000h to 7BFFFh
SA16	1	1	1	1	1	0	0	F8000h to F9FFFh	7C000h to 7CFFFh
SA17	1	1	1	1	1	0	1	FA000h to FBFFFh	7D000h to 7DFFFh
SA18	1	1	1	1	1	1	X	FC000h to FFFFFh	7E000h to 7FFFFh

Sector Address Tables (MBM29LV800BE)

Sector Address	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	Address Range (×8)	Address Range (×16)
SA0	0	0	0	0	0	0	X	00000h to 03FFFh	00000h to 01FFFh
SA1	0	0	0	0	0	1	0	04000h to 05FFFh	02000h to 02FFFh
SA2	0	0	0	0	0	1	1	06000h to 07FFFh	03000h to 03FFFh
SA3	0	0	0	0	1	X	X	08000h to 0FFFFh	04000h to 07FFFh
SA4	0	0	0	1	X	X	X	10000h to 1FFFFh	08000h to 0FFFFh
SA5	0	0	1	0	X	X	X	20000h to 2FFFFh	10000h to 17FFFh
SA6	0	0	1	1	X	X	X	30000h to 3FFFFh	18000h to 1FFFFh
SA7	0	1	0	0	X	X	X	40000h to 4FFFFh	20000h to 27FFFh
SA8	0	1	0	1	X	X	X	50000h to 5FFFFh	28000h to 2FFFFh
SA9	0	1	1	0	X	X	X	60000h to 6FFFFh	30000h to 37FFFh
SA10	0	1	1	1	X	X	X	70000h to 7FFFFh	38000h to 3FFFFh
SA11	1	0	0	0	X	X	X	80000h to 8FFFFh	40000h to 47FFFh
SA12	1	0	0	1	X	X	X	90000h to 9FFFFh	48000h to 4FFFFh
SA13	1	0	1	0	X	X	X	A0000h to AFFFFh	50000h to 57FFFh
SA14	1	0	1	1	X	X	X	B0000h to BFFFFh	58000h to 5FFFFh
SA15	1	1	0	0	X	X	X	C0000h to CFFFFh	60000h to 67FFFh
SA16	1	1	0	1	X	X	X	D0000h to DFFFFh	68000h to 6FFFFh
SA17	1	1	1	0	X	X	X	E0000h to EFFFFh	70000h to 77FFFh
SA18	1	1	1	1	X	X	X	F0000h to FFFFFh	78000h to 7FFFFh

- One 16 Kbytes, two 8 Kbytes, one 32 Kbytes, and fifteen 64 Kbytes
- Individual-sector, multiple-sector, or bulk-erase capability
- Individual or multiple-sector protection is user definable.

	(×8)	(×16)
	FFFFFh	7FFFFh
16 Kbyte		
	FBFFFh	7DFFFh
8 Kbyte		
	F9FFFh	7CFFFh
8 Kbyte		
	F7FFFh	7BFFFh
32 Kbyte		
	EFFFFh	77FFFh
64 Kbyte		
	DFFFFh	6FFFFh
64 Kbyte		
	CFFFFh	67FFFh
64 Kbyte		
	BFFFFh	5FFFFh
64 Kbyte		
	AFFFFh	57FFFh
64 Kbyte		
	9FFFFh	4FFFFh
64 Kbyte		
	8FFFFh	47FFFh
64 Kbyte		
	7FFFFh	3FFFFh
64 Kbyte		
	6FFFFh	37FFFh
64 Kbyte		
	5FFFFh	2FFFFh
64 Kbyte		
	4FFFFh	27FFFh
64 Kbyte		
	3FFFFh	1FFFFh
64 Kbyte		
	2FFFFh	17FFFh
64 Kbyte		
	1FFFFh	0FFFFh
64 Kbyte		
	0FFFFh	07FFFh
64 Kbyte		
	00000h	00000h

MBM29LV800TE Sector Architecture

	(×8)	(×16)
	FFFFFh	7FFFFh
64 Kbyte		
	EFFFFh	77FFFh
64 Kbyte		
	DFFFFh	6FFFFh
64 Kbyte		
	CFFFFh	67FFFh
64 Kbyte		
	BFFFFh	5FFFFh
64 Kbyte		
	AFFFFh	57FFFh
64 Kbyte		
	9FFFFh	4FFFFh
64 Kbyte		
	8FFFFh	47FFFh
64 Kbyte		
	7FFFFh	3FFFFh
64 Kbyte		
	6FFFFh	37FFFh
64 Kbyte		
	5FFFFh	2FFFFh
64 Kbyte		
	4FFFFh	27FFFh
64 Kbyte		
	3FFFFh	1FFFFh
64 Kbyte		
	2FFFFh	17FFFh
64 Kbyte		
	1FFFFh	0FFFFh
64 Kbyte		
	0FFFFh	07FFFh
32 Kbyte		
	07FFFh	03FFFh
8 Kbyte		
	05FFFh	02FFFh
8 Kbyte		
	03FFFh	01FFFh
16 Kbyte		
	00000h	00000h

MBM29LV800BE Sector Architecture

■ FUNCTIONAL DESCRIPTION

Read Mode

The MBM29LV800TE/BE have two control functions which must be satisfied in order to obtain data at the outputs. $\overline{\text{CE}}$ is the power control and should be used for a device selection. $\overline{\text{OE}}$ is the output control and should be used to gate data to the output pins if a device is selected.

Address access time (t_{ACC}) is equal to delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable addresses and stable $\overline{\text{CE}}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{\text{OE}}$ to valid data at the output pins (Assuming the addresses have been stable for at least t_{ACC}-t_{OE} time) . When reading out data without changing addresses after power-up, it is necessary to input hardware reset or change $\overline{\text{CE}}$ pin from “H” or “L”

Standby Mode

There are two ways to implement the standby mode on the MBM29LV800TE/BE devices, one using both the $\overline{\text{CE}}$ and $\overline{\text{RESET}}$ pins; the other via the $\overline{\text{RESET}}$ pin only.

When using both pins, a CMOS standby mode is achieved with $\overline{\text{CE}}$ and $\overline{\text{RESET}}$ inputs both held at $V_{CC} \pm 0.3$ V. Under this condition, the current consumed is less than 5 µA. The device can be read with standard access time (t_{CE}) from either of these standby modes. During Embedded Algorithm operation, V_{CC} active current (I_{CC2}) is required even $\overline{\text{CE}}$ = “H”.

When using the $\overline{\text{RESET}}$ pin only, a CMOS standby mode is achieved with $\overline{\text{RESET}}$ input held at $V_{SS} \pm 0.3$ V ($\overline{\text{CE}}$ = “H” or “L”) . Under this condition the current consumed is less than 5 µA. Once the $\overline{\text{RESET}}$ pin is taken high, the device requires t_{RH} as wake up time for outputs to be valid for read access.

In the standby mode, the outputs are in the high impedance state, independently of the $\overline{\text{OE}}$ input.

Automatic Sleep Mode

There is a function called automatic sleep mode to restrain power consumption during read-out of MBM29LV800TE/BE data. This mode can be useful in the application such as handy terminal which requires low power consumption.

To activate this mode, MBM29LV800TE/BE automatically switches themselves to low power mode when MBM29LV800TE/BE addresses remain stable during access time of 150 ns. It is not necessary to control $\overline{\text{CE}}$, $\overline{\text{WE}}$, and $\overline{\text{OE}}$ on the mode. Under the mode, the current consumed is typically 1 µA (CMOS Level) .

Since the data are latched during this mode, the data are read-out continuously. If the addresses are changed, the mode is canceled automatically, and MBM29LV800TE/BE read-out the data for changed addresses.

Output Disable

With the $\overline{\text{OE}}$ input at a logic high level (V_{IH}) , the output from the devices is disabled. This will cause the output pins to be in a high impedance state.

Autoselect

The autoselect mode allows the reading out of a binary code from the devices and will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the devices to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the devices.

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 12.5 V) on address pin A_9. Two identifier bytes may then be sequenced from the devices outputs by toggling address A_0 from V_{IL} to V_{IH}. All addresses are DON’T CARES except A_0, A_1, A_6, and A_{-1}. (See “MBM29LV800TE/BE Sector Protection Verify Autoselect Codes” in “ ■ DEVICE BUS OPERATION”.)

The manufacturer and device codes may also be read via the command register, for instances when the MBM29LV800TE/BE are erased or programmed in a system without access to high voltage on the A_9 pin. The command sequence is illustrated in “MBM29LV800TE/BE Command Definitions” in “ ■ DEVICE BUS OPERATION”. (Refer to Autoselect Command section.)

Word 0 ($A_0 = V_{IL}$) represents the manufacturer's code (Fujitsu = 04h) and ($A_0 = V_{IH}$) represents the device identifier code (MBM29LV800TE = DAh and MBM29LV800BE = 5Bh for × 8 mode; MBM29LV800TE = 22DAh and MBM29LV800BE = 225Bh for × 16 mode) . These two bytes/words are given in "MBM29LV800TE/BE Sector Protection Verify Autoselect Codes" and "Expanded Autoselect Code Table" in "■ DEVICE BUS OPERATION". All identifiers for manufactures and device will exhibit odd parity with DQ_7 defined as the parity bit. In order to read the proper device codes when executing the autoselect, A_1 must be V_{IL}. (See "MBM29LV800TE/BE Sector Protection Verify Autoselect Codes" and "Expanded Autoselect Code Table" in "■ DEVICE BUS OPERATION".)

Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written by bringing $\overline{WE}$ to V_{IL}, while $\overline{CE}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later; while data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Sector Protection

The MBM29LV800TE/BE feature hardware sector protection. This feature will disable both program and erase operations in any number of sectors (0 through 18) . The sector protection feature is enabled using programming equipment at the user's site. The devices are shipped with all sectors unprotected. Alternatively, Fujitsu may program and protect sectors in the factory prior to shiping the device.

To activate this mode, the programming equipment must force V_{ID} on address pin A_9 and control pin $\overline{OE}$, (suggest V_{ID} = 11.5 V) , $\overline{CE} = V_{IL}$, and $A_6 = V_{IL}$. The sector addresses (A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12}) should be set to the sector to be protected. "Sector Address Tables (MBM29LV800TE)" and "Sector Address Tables (MBM29LV800BE) " in "■ FLEXIBLE SECTOR-ERASE ARCHITECTURE" define the sector address for each of the nineteen (19) individual sectors. Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same. Sector addresses must be held constant during the $\overline{WE}$ pulse. See "Sector Protection Timing Diagram" in "■ TIMING DIAGRAM" and "Sector Protection Algorithm" in "■ FLOW CHART" for sector protection waveforms and algorithm.

To verify programming of the protection circuitry, the programming equipment must force V_{ID} on address pin A_9 with $\overline{CE}$ and $\overline{OE}$ at V_{IL} and $\overline{WE}$ at V_{IH}. Scanning the sector addresses (A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12}) while (A_6, A_1, A_0) = (0, 1, 0) will produce a logical "1" code at device output DQ_0 for a protected sector. Otherwise the devices will read 00h for unprotected sector. In this mode, the lower order addresses, except for A_0, A_1, and A_6 are DON'T CARES. Address locations with $A_1 = V_{IL}$ are reserved for Autoselect manufacturer and device codes. A_{-1} requires to apply to V_{IL} on byte mode.

It is also possible to determine if a sector is protected in the system by writing an Autoselect command. Performing a read operation at the address location XX02h, where the higher order addresses (A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12}) are the desired sector address will produce a logical "1" at DQ_0 for a protected sector. See "MBM29LV800TE/BE Sector Protection Verify Autoselect Codes" and "Expanded Autoselect Code Table" in "■ DEVICE BUS OPERATION" for Autoselect codes.

Temporary Sector Unprotection

This feature allows temporary unprotection of previously protected sectors of the MBM29LV800TE/BE devices in order to change data. The Sector Unprotection mode is activated by setting the $\overline{RESET}$ pin to high voltage (V_{ID}) . During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once the V_{ID} is taken away from the $\overline{RESET}$ pin, all the previously protected sectors will be protected again. See "Temporary Sector Unprotection Timing Diagram" in "■ TIMING DIAGRAM" and "Temporary Sector Unprotection Algorithm" in "■ FLOW CHART".

Extended Sector Protection

In addition to normal sector protection, the MBM29LV800TE/BE have Extended Sector Protection as extended function. This function enables to protect sector by forcing V_{ID} on $\overline{RESET}$ pin and write a commnad sequence. Unlike conventional procedure, it is not necessary to force V_{ID} and control timing for control pins. The only $\overline{RESET}$ pin requires V_{ID} for sector protection in this mode. The extended sector protect requires V_{ID} on $\overline{RESET}$ pin. With this condition the operation is initiated by writing the set-up command (60h) into the command register. Then the sector addresses pins (A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13} and A_{12}) and (A_6, A_1, A_0) = (0, 1, 0) should be set to be protected (recommend to set V_{IL} for the other addresses pins) , and write extended sector protect command (60h) . A sector is generally protected in 250 µs. To verify programming of the protection circuitry, the sector addresses pins (A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13} and A_{12}) and (A_6, A_1, A_0) = (0, 1, 0) should be set and write a command (40h) . Following the command write, a logical "1" at device output DQ_0 produces for protected sector in the read operation. If the output is logical "0", repeat to write extended sector protect command (60h) again. To terminate the operation, it is necessary to set $\overline{RESET}$ pin to V_{IH} (refer to "Extended Sector Protection Algorithm" in "■ FLOW CHART") .

$\overline{\text{RESET}}$

Hardware Reset

The MBM29LV800TE/BE devices may be reset by driving the $\overline{RESET}$ pin to V_{IL}. The $\overline{RESET}$ pin has pulse requirement and has to be kept low (V_{IL}) for at least "t_{RP}" in order to properly reset the internal state machine. Any operation in the process of being executed is terminated and the internal state machine is reset to the read mode "t_{READY}" after the $\overline{RESET}$ pin goes low. Furthermore once the $\overline{RESET}$ pin goes high, the devices require an additional t_{RH} before it will allow read access. When the $\overline{RESET}$ pin is low, the devices will be in the standby mode for the duration of the pulse and all the data output pins will be tri-stated. If hardware reset occurs during program or erase operation, the data at that particular location is corrupted. Note that the RY/$\overline{BY}$ output signal should be ignored during the $\overline{RESET}$ pulse. See "$\overline{RESET}$, RY/$\overline{BY}$ Timing Diagram" in "■ TIMING DIAGRAM" for the timing diagram. Refer to Temporary Sector Unprotection for additional functionality.

If hardware reset occurs during Embedded Erase Algorithm, the erasing sector (s) cannot be used.

■ COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. "MBM29LV800TE/BE Command Definitions" in "■ DEVICE BUS OPERATION" defines the valid register command sequences. Note that the Erase Suspend (B0h) and Erase Resume (30h) commands are valid only while the Sector Erase operation is in progress. Furthermore both Read/Reset commands are functionally equivalent, resetting the device to the read mode. Note that commands are always written at DQ_7 to DQ_0 and DQ_{15} to DQ_8 bits are ignored.

Read/Reset Command

In order to return from Autoselect mode or Exceeded Timing Limits ($DQ_5 = 1$) to read/reset mode, the read/reset operation is initiated by writing the Read/Reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The devices remain enabled for reads until the command register contents are altered.

The devices will automatically power-up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. As such manufacture and device codes must be accessible while the devices reside in the target system. PROM programmers typically access the signature codes by raising A_9 to a high voltage. However multiplexing high voltage onto the address lines is not generally desired system design practice.

The device contains an Autoselect command operation to supplement traditional PROM programming methodology. The operation is initiated by writing the Autoselect command sequence into the command register.
Following the command write, a read cycle from address XX00h retrieves the manufacture code of 04h. A read cycle from address XX01h for ×16 (XX02h for ×8) returns the device code (MBM29LV800TE = DAh and MBM29LV 800BE = 5Bh for ×8 mode; MBM29LV800TE = 22DAh and MBM29LV800BE = 225Bh for ×16 mode) .
(See "MBM29LV800TE/BE Sector Protection Verify Autoselect Codes" and "Expanded Autoselect Code Table" in "■ DEVICE BUS OPERATION".) All manufacturer and device codes will exhibit odd parity with DQ_7 defined as the parity bit. Sector state (protection or unprotection) will be informed by address XX02h for ×16 (XX04h for ×8).
Scanning the sector addresses (A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12}) while (A_6, A_1, A_0) = (0, 1, 0) will produce a logical "1" at device output DQ_0 for a protected sector. The programming verification should be performed margin mode on the protected sector. (See "MBM29LV800TE/BE User Bus Operations ($\overline{BYTE} = V_{IH}$)" and "MBM29LV 800TE/BE User Bus Operations ($\overline{BYTE} = V_{IL}$)" in "■ DEVICE BUS OPERATION".)

To terminate the operation, it is necessary to write the Read/Reset command sequence into the register. To execute the Autoselect command during the operation, writing Read/Reset command sequence must precede the Autoselect command.

Byte/Word Programming

The devices are programmed on a byte-by-byte (or word-by-word) basis. Programming is a four bus cycle operation. There are two "unlock" write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens later and the data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first. The rising edge of $\overline{CE}$ or $\overline{WE}$ (whichever happens first) begins programming. Upon executing the Embedded Program Algorithm command sequence, the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

The automatic programming operation is completed when the data on DQ_7 is equivalent to data written to this bit at which time the devices return to the read mode and addresses are no longer latched. (See "Hardware Sequence Flags".) Therefore, the devices require that a valid address to the devices be supplied by the system at this particular instance of time. Hence, $\overline{\text{Data}}$ Polling must be performed at the memory location which is being programmed.

If hardware reset occurs during the programming operation, it is impossible to guarantee the data are being written.

Programming is allowed in any sequence and across sector boundaries. Beware that a data “0” cannot be programmed back to a “1”. Attempting to do so may either hang up the device or result in an apparent success according to the data polling algorithm but a read from read/reset mode will show that the data is still “0”. Only erase operations can convert “0”s to “1”s.

“Embedded Program™ Algorithm” in “■ FLOW CHART” illustrates the Embedded Program™ Algorithm using typical command strings and bus operations.

Chip Erase

Chip erase is a six bus cycle operation. There are two “unlock” write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the chip erase command.

Chip erase does not require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm command sequence the devices will automatically program and verify the entire memory for an all zero data pattern prior to electrical erase (Preprogram function) . The system is not required to provide any controls or timings during these operations.

The automatic erase begins on the rising edge of the last $\overline{WE}$ pulse in the command sequence and terminates when the data on DQ_7 is “1” (See Write Operation Status section.) at which time the device returns to read the mode.

Chip Erase Time; Sector Erase Time × All sectors + Chip Program Time (Preprogramming)

“Embedded Erase™ Algorithm” in “■ FLOW CHART” illustrates the Embedded Erase™ Algorithm using typical command strings and bus operations.

Sector Erase

Sector erase is a six bus cycle operation. There are two “unlock” write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the Sector Erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{WE}$, while the command (Data = 30h) is latched on the rising edge of $\overline{WE}$. After time-out of “t_{TOW}” from the rising edge of the last sector erase command, the sector erase operation will begin.

Multiple sectors may be erased concurrently by writing the six bus cycle operations on “MBM29LV800TE/BE Command Definitions” in “■ DEVICE BUS OPERATION”. This sequence is followed with writes of the Sector Erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than “t_{TOW}” otherwise that command will not be accepted and erasure will not start. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of “t_{TOW}” from the rising edge of the last $\overline{WE}$ will initiate the execution of the Sector Erase command (s) . If another falling edge of the $\overline{WE}$ occurs within the “t_{TOW}” time-out window the timer is reset. (Monitor DQ_3 to determine if the sector erase timer window is still open, see section DQ_3, Sector Erase Timer.) Once execution has begun resetting the devices will corrupt the data in the sector. In that case, restart the erase on those sectors and allow them to complete. (Refer to the Write Operation Status section for Sector Erase Timer operation.) Loading the sector erase buffer may be done in any sequence and with any number of sectors (0 to 18) .

Sector erase does not require the user to program the devices prior to erase. The devices automatically program all memory locations in the sector (s) to be erased prior to electrical erase (Preprogram function) . When erasing a sector or sectors the remaining unselected sectors are not affected. The system is not required to provide any controls or timings during these operations.

The automatic sector erase begins after the “t_{TOW}” time out from the rising edge of the $\overline{WE}$ pulse for the last sector erase command pulse and terminates when the data on DQ_7 is “1” (See Write Operation Status section.) at which time the devices return to the read mode. $\overline{\text{Data}}$ polling must be performed at an address within any of the sectors being erased. Multiple Sector Erase Time; [Sector Erase Time + Sector Program Time (Preprogramming)] × Number of Sector Erase

"Embedded Erase™ Algorithm" in "■ FLOW CHART" illustrates the Embedded Erase™ Algorithm using typical command strings and bus operations.

Erase Suspend/Resume

The Erase Suspend command allows the user to interrupt a Sector Erase operation and then perform data reads from or programs to a sector not being erased. This command is applicable ONLY during the Sector Erase operation which includes the time-out period for sector erase. Writting the Erase Suspend command during the Sector Erase time-out results in immediate termination of the time-out period and suspension of the erase operation.

Writing the Erase Resume command resumes the erase operation. The addresses are DON'T CARES when writing the Erase Suspend or Erase Resume command.

When the Erase Suspend command is written during the Sector Erase operation, the device will take a maximum of "t_{SPD}" to suspend the erase operation. When the devices have entered the erase-suspended mode, the RY/$\overline{BY}$ output pin and the DQ_7 bit will be at logic "1", and DQ_6 will stop toggling. The user must use the address of the erasing sector for reading DQ_6 and DQ_7 to determine if the erase operation has been suspended. Further writes of the Erase Suspend command are ignored.

When the erase operation has been suspended, the devices default to the erase-suspend-read mode. Reading data in this mode is the same as reading from the standard read mode except that the data must be read from sectors that have not been erase-suspended. Successively reading from the erase-suspended sector will cause DQ_2 to toggle while the device is in the erase-suspend-read mode (See the section on DQ_2) .

After entering the erase-suspend-read mode, the user can program the device by writing the appropriate command sequence for Program. This program mode is known as the erase-suspend-program mode. Again, programming in this mode is the same as programming in the regular Program mode except that the data must be programmed to sectors that are not erase-suspended. Successively reading from the erase-suspended sector while the devices are in the erase-suspend-program mode will cause DQ_2 to toggle. The end of the erase-suspended Program operation is detected by the RY/$\overline{BY}$ output pin, $\overline{\text{Data}}$ polling of DQ_7, or by the Toggle Bit I (DQ_6) which is the same as the regular Program operation. Note that DQ_7 must be read from the Program address while DQ_6 can be read from any address.

To resume the operation of Sector Erase, the Resume command (30h) should be written. Any further writes of the Resume command at this point will be ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Extended Command

(1) Fast Mode

MBM29LV800TE/BE have Fast Mode function. This mode dispenses with the initial two unclock cycles required in the standard program command sequence by writing Fast Mode command into the command register. In this mode, the required bus cycle for programming is two cycles instead of four bus cycles in standard program command. In Fast Mode, do not write any command other than the fast program/fast mode reset command. The read operation is also executed after exiting this mode. To exit this mode, it is necessary to write Fast Mode Reset command into the command register (Refer to "Embedded Programming Algorithm for Fast Mode" in "■ FLOW CHART") . The V_{CC} active current is required even $\overline{CE} = V_{IH}$ during Fast Mode.

(2) Fast Programming

During Fast Mode, the programming can be executed with two bus cycles operation. The Embedded Program Algorithm is executed by writing program set-up command (A0h) and data write cycles (PA/PD) (Refer to "Embedded Programming Algorithm for Fast Mode" in "■ FLOW CHART") .

Write Operation Status

Hardware Sequence Flags

Status			DQ_7	DQ_6	DQ_5	DQ_3	DQ_2
In Progress	Embedded Program Algorithm		$\overline{DQ_7}$	Toggle	0	0	1
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle
	Erase Suspended Mode	Erase Suspend Read (Erase Suspended Sector)	1	1	0	0	Toggle
		Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data
		Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{DQ_7}$	Toggle*1	0	0	1*2
Exceeded Time Limits	Embedded Program Algorithm		$\overline{DQ_7}$	Toggle	1	0	1
	Embedded Erase Algorithm		0	Toggle	1	1	N/A
	Erase Suspended Mode	Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{DQ_7}$	Toggle	1	0	N/A

*1 : Performing successive read operations from any address will cause DQ_6 to toggle.

*2 : Reading the byte address being programmed while in the erase-suspend program mode will indicate logic "1" at the DQ_2 bit. However, successive reads from the erase-suspended sector will cause DQ_2 to toggle.

Notes : • DQ_1 and DQ_0 are reserved pins for future use.
• DQ_4 is Fujitsu internal use only.

DQ_7

$\overline{\text{Data}}$ Polling

The MBM29LV800TE/BE devices feature $\overline{\text{Data}}$ Polling as a method to indicate to the host that the Embedded Algorithms are in progress or completed. During the Embedded Program Algorithm, an attempt to read devices will produce a complement of data last written to DQ_7. Upon completion of the Embedded Program Algorithm, an attempt to read device will produce true data last written to DQ_7. During the Embedded Erase Algorithm, an attempt to read device will produce a "0" at the DQ_7 output. Upon completion of the Embedded Erase Algorithm an attempt to read device will produce a "1" on DQ_7. The flowchart for $\overline{\text{Data}}$ Polling (DQ_7) is shown in "$\overline{\text{Data}}$ Polling Algorithm" in "■ FLOW CHART".

For chip erase and sector erase, the $\overline{\text{Data}}$ Polling is valid after the rising edge of the sixth $\overline{\text{WE}}$ pulse in the six write pulse sequence. $\overline{\text{Data}}$ Polling must be performed at sector address of sectors being erased, not protected sectors. Otherwise, the status may be invalid. Once the Embedded Algorithm operation is close to completion, MBM29LV800TE/BE data pins (DQ_7) may change asynchronously while the output enable ($\overline{\text{OE}}$) is asserted low. This means that devices are driving status information on DQ_7 at one instant of time and then that byte's valid data at the next instant of time. Depending on when the system samples the DQ_7 output, it may read the status or valid data. Even if device has completed the Embedded Algorithm operation and DQ_7 has a valid data, data outputs on DQ_6 to DQ_0 may be still invalid. The valid data on DQ_7 to DQ_0 will be read on the successive read attempts.

The $\overline{\text{Data}}$ Polling feature is active only during the Embedded Programming Algorithm, Embedded Erase Algorithm or sector erase time-out.

See "$\overline{\text{Data}}$ Polling during Embedded Algorithm Operation Timing Diagram" in "■ TIMING DIAGRAM" for the $\overline{\text{Data}}$ Polling timing specifications and diagrams.

DQ_6

Toggle Bit I

The MBM29LV800TE/BE also feature the “Toggle Bit I” as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During Embedded Program or Erase Algorithm cycle, successive attempts to read ($\overline{OE}$ toggling) data from the devices will result in DQ_6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ_6 will stop toggling and valid data will be read on the next successive attempts. During programming, the Toggle Bit I is valid after the rising edge of the fourth $\overline{WE}$ pulses in the four write pulse sequence. For chip erase and sector erase, the Toggle Bit I is valid after the rising edge of the sixth $\overline{WE}$ pulse in the six write pulses sequence. The Toggle Bit I is active during the sector time out.

In programming, if the sector being written is protected, the toggle bit will toggle for about 2 µs and then stop toggling with data unchanged. In erase, devices will erase all selected sectors except for ones that are protected. If all selected sectors are protected, the chip will toggle the toggle bit for about 200 µs and then drop back into read mode, having data unchanged.

Either $\overline{CE}$ or $\overline{OE}$ toggling will cause DQ_6 to toggle. In addition, an Erase Suspend/Resume command will cause DQ_6 to toggle.

See “Taggle Bit I during Embedded Algorithm Operation Timing Diagram” in “■ TIMING DIAGRAM” for the Toggle Bit I timing specifications and diagrams.

DQ_5

Exceeded Timing Limits

DQ_5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count) . Under these conditions, DQ_5 will produce a “1”. This is a failure condition which indicates that the program or erase cycle was not successfully completed. $\overline{Data}$ Polling is the only operating function of devices under this condition. The $\overline{CE}$ circuit will partially power down device under these conditions (to approximately 2 mA) . The $\overline{OE}$ and $\overline{WE}$ pins will control the output disable functions as described in “MBM29LV800TE/BE User Bus Operations ($\overline{BYTE}$ = V_{IH})” and “MBM29LV800TE/BE User Bus Operations ($\overline{BYTE}$ = V_{IL})” in “■ DEVICE BUS OPERATION”.

The DQ_5 failure condition may also appear if a user tries to program a non blank location without pre-erase. In this case, the devices lock out and never complete the Embedded Algorithm operation. Hence, the system never read valid data on DQ_7 bit and DQ_6 never stop toggling. Once devices have exceeded timing limits, the DQ_5 bit will indicate a “1.” Please note that this is not a device failure condition since devices were incorrectly used. If this occurs, reset device with command sequence.

DQ_3

Sector Erase Timer

After completion of the initial sector erase command sequence, sector erase time-out will begin. DQ_3 will remain low until the time-out is completed. $\overline{Data}$ Polling and Toggle Bit are valid after the initial sector erase command sequence.

If $\overline{Data}$ Polling or the Toggle Bit I indicates device has been written with a valid erase command, DQ_3 may be used to determine if the sector erase timer window is still open. If DQ_3 is high (“1”) the internally controlled erase cycle has begun : If DQ_3 is low (“0”) , the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of DQ_3 prior to and following each subsequent Sector Erase command. If DQ_3 were high on the second status check, the command may not have been accepted.

See “Hardware Sequence Flags”.

DQ_2

Toggle Bit II

This toggle bit II, along with DQ_6, can be used to determine whether the devices are in the Embedded Erase Algorithm or in Erase Suspend.

Successive reads from the erasing sector will cause DQ_2 to toggle during the Embedded Erase Algorithm. If the devices are in the erase-suspended-read mode, successive reads from the erase-suspended sector will cause DQ_2 to toggle. When the devices are in the erase-suspended-program mode, successive reads from the byte address of the non-erase suspended sector will indicate a logic “1” at the DQ_2 bit.

DQ_6 is different from DQ_2 in that DQ_6 toggles only when the standard program or Erase, or Erase Suspend Program operation is in progress. The behavior of these two status bits, along with that of DQ_7, is summarized as follows :

For example, DQ_2 and DQ_6 can be used together to determine if the erase-suspend-read mode is in progress. (DQ_2 toggles while DQ_6 does not.) See also “Hardware Sequence Flags” and “DQ_2 vs. DQ_6” in “■ TIMING DIAGRAM”.

Furthermore, DQ_2 can also be used to determine which sector is being erased. When device is in the erase mode, DQ_2 toggles if this bit is read from an erasing sector.

Toggle Bit Status

Mode	DQ_7	DQ_6	DQ_2
Program	$\overline{DQ_7}$	Toggle	1
Erase	0	Toggle	Toggle
Erase-Suspend Read (Erase-Suspended Sector) *1	1	1	Toggle
Erase-Suspend Program	$\overline{DQ_7}$	Toggle *1	1 *2

*1 : Performing successive read operations from any address will cause DQ_6 to toggle.

*2 : Reading the byte address being programmed while in the erase-suspend program mode will indicate logic “1” at the DQ_2 bit. However, successive reads from the erase-suspended sector will cause DQ_2 to toggle.

RY/$\overline{\text{BY}}$

Ready/Busy

MBM29LV800TE/BE provide a RY/$\overline{\text{BY}}$ open-drain output pin as a way to indicate to the host system that Embedded Algorithms are either in progress or has been completed. If output is low, devices are busy with either a program or erase operation. If output is high, devices are ready to accept any read/write or erase operation. If MBM29LV800TE/BE are placed in an Erase Suspend mode, RY/$\overline{\text{BY}}$ output will be high.

During programming, RY/$\overline{\text{BY}}$ pin is driven low after the rising edge of the fourth $\overline{\text{WE}}$ pulse. During an erase operation, RY/$\overline{\text{BY}}$ pin is driven low after the rising edge of the sixth $\overline{\text{WE}}$ pulse. RY/$\overline{\text{BY}}$ pin will indicate a busy condition during $\overline{\text{RESET}}$ pulse. Refer to “RY/$\overline{\text{BY}}$ Timing Diagram during Program/Erase Operation Timing Diagram” and “$\overline{\text{RESET}}$, RY/$\overline{\text{BY}}$ Timing Diagram” in “■ TIMING DIAGRAM” for a detailed timing diagram. RY/$\overline{\text{BY}}$ pin is pulled high in standby mode.

Since this is an open-drain output, RY/$\overline{\text{BY}}$ pins can be tied together in parallel with a pull-up resistor to V_{CC}.

Byte/Word Configuration

$\overline{\text{BYTE}}$ pin selects byte (8-bit) mode or word (16-bit) mode for MBM29LV800TE/BE devices. When this pin is driven high, devices operate in word (16-bit) mode. Data is read and programmed at DQ_{15} to DQ_0. When this pin is driven low, devices operates in byte (8-bit) mode. Under this mode, the DQ_{15}/A_{-1} pin becomes the lowest address bit, and DQ_{14} to DQ_8 bits are tri-stated. However, the command bus cycle is always an 8-bit operation and hence commands are written at DQ_7 to DQ_0 and DQ_{15} to DQ_8 bits are ignored. Refer to "Timing Diagram for Word Mode Configuration", "Timing Diagram for Byte Mode Configuration" and "$\overline{\text{BYTE}}$ Timing Diagram for Write Operations" in "■ TIMING DIAGRAM" for the timing diagram.

Data Protection

MBM29LV800TE/BE are designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up, devices automatically reset internal state machine in Read mode. Also, with its control register architecture, alteration of memory contents only occurs after successful completion of specific multi-bus cycle command sequences.

Devices also incorporate several features to prevent inadvertent write cycles resulting form V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than V_{LKO} (Min) . If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. Under this condition, the device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}. It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when V_{CC} is above V_{LKO} (Min) .

If Embedded Erase Algorithm is interrupted, there is possibility that the erasing sector (s) cannot be used.

Write Pulse "Glitch" Protection

Noise pulses of less than 3 ns (typical) on $\overline{\text{OE}}$, $\overline{\text{CE}}$, or $\overline{\text{WE}}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{\text{OE}} = V_{IL}$, $\overline{\text{CE}} = V_{IH}$, or $\overline{\text{WE}} = V_{IH}$. To initiate a write cycle, $\overline{\text{CE}}$ and $\overline{\text{WE}}$ must be a logical zero while $\overline{\text{OE}}$ is a logical one.

Power-Up Write Inhibit

Power-up of the devices with $\overline{\text{WE}} = \overline{\text{CE}} = V_{IL}$ and $\overline{\text{OE}} = V_{IH}$ will not accept commands on the rising edge of $\overline{\text{WE}}$. The internal state machine is automatically reset to the read mode on power-up.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Storage Temperature	Tstg	–55	+125	°C
Ambient Temperature with Power Applied	T_A	–40	+85	°C
Voltage with Respect to Ground All pins except A_9, $\overline{OE}$, $\overline{RESET}$ *1, *2	V_{IN}, V_{OUT}	–0.5	V_{CC} + 0.5	V
Power Supply Voltage *1	V_{CC}	–0.5	+5.5	V
A_9, $\overline{OE}$, and $\overline{RESET}$ *1, *3	V_{IN}	–0.5	+13.0	V

*1 : Voltage is defined on the basis of V_{SS} = GND = 0 V.

*2 : Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs or I/O pins may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CC} + 0.5 V. During voltage transitions, inputs or I/O pins may overshoot to V_{CC} + 2.0 V for periods of up to 20 ns.

*3 : Minimum DC input voltage on A_9, $\overline{OE}$, and $\overline{RESET}$ pins is –0.5 V. During voltage transitions, A_9, $\overline{OE}$, and $\overline{RESET}$ pins may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. Voltage difference between input and supply voltage (V_{IN} – V_{CC}) does not exceed + 9.0 V. Maximum DC input voltage on A_9, $\overline{OE}$, and $\overline{RESET}$ pins is +13.0 V which may overshoot to +14.0 V for periods of up to 20 ns.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Part No.	Value			Unit
			Min	Typ	Max	
Ambient Temperature	T_A	MBM29LV800TE/BE 60	–20	—	+70	°C
		MBM29LV800TE/BE 70/90	–40	—	+85	°C
Power Supply Voltage*	V_{CC}	MBM29LV800TE/BE 60	+3.0	—	+3.6	V
		MBM29LV800TE/BE 70/90	+2.7	—	+3.6	V

* : Voltage is defined on the basis of V_{SS} = GND = 0 V.

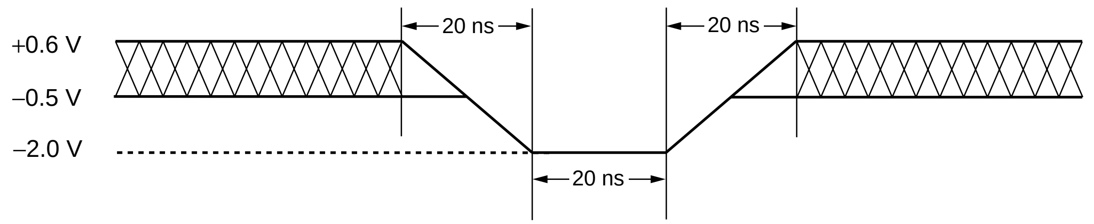
Note : Operating ranges define those limits between which the functionality of the device is guaranteed.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

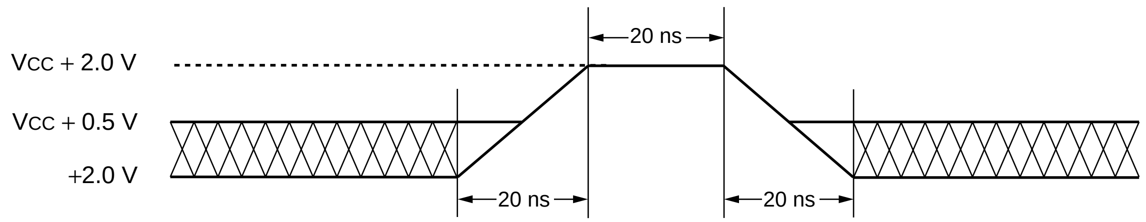
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

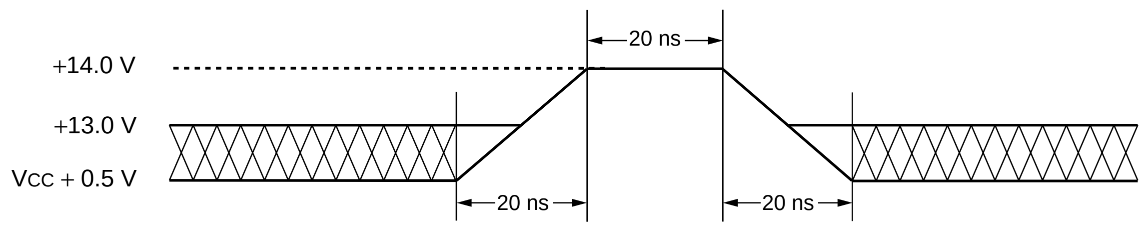
■ MAXIMUM OVERSHOOT/MAXIMUM UNDERSHOOT



Maximum Undershoot Waveform



Maximum Overshoot Waveform 1



Note : This wave form is applied for A_9, $\overline{\text{OE}}$, and $\overline{\text{RESET}}$.

Maximum Overshoot Waveform 2

■ DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Value		Unit
				Min	Max	
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max		–1.0	+1.0	µA
Output Leakage Current	I_{LO}	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max		–1.0	+1.0	µA
A_9, $\overline{OE}$, $\overline{RESET}$ Inputs Leakage Current	I_{LIT}	$V_{CC} = V_{CC}$ Max, A_9, $\overline{OE}$, $\overline{RESET}$ = 12.5 V		—	35	µA
V_{CC} Active Current *1	I_{CC1}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$, f = 10 MHz	Byte	—	22	mA
			Word		25	
		$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$, f = 5 MHz	Byte	—	12	mA
			Word		15	
V_{CC} Active Current *2	I_{CC2}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		—	35	mA
V_{CC} Current (Standby)	I_{CC3}	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{CC} \pm 0.3$ V, $\overline{RESET} = V_{CC} \pm 0.3$ V		—	5	µA
V_{CC} Current (Standby, Reset)	I_{CC4}	$V_{CC} = V_{CC}$ Max, $\overline{RESET} = V_{SS} \pm 0.3$ V		—	5	µA
V_{CC} Current (Automatic Sleep Mode) *3	I_{CC5}	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{SS} \pm 0.3$ V, $\overline{RESET} = V_{CC} \pm 0.3$ V, $V_{IN} = V_{CC} \pm 0.3$ V or $V_{SS} \pm 0.3$ V		—	5	µA
Input Low Level	V_{IL}	—		–0.5	0.6	V
Input High Level	V_{IH}	—		2.0	V_{CC} + 0.3	V
Voltage for Autoselect and Sector Protection (A_9, $\overline{OE}$, $\overline{RESET}$) *4	V_{ID}	—		11.5	12.5	V
Output Low Voltage Level	V_{OL}	I_{OL} = 4.0 mA, $V_{CC} = V_{CC}$ Min		—	0.45	V
Output High Voltage Level	V_{OH1}	I_{OH} = –2.0 mA, $V_{CC} = V_{CC}$ Min		2.4	—	V
	V_{OH2}	I_{OH} = –100 µA		V_{CC} – 0.4	—	V
Low V_{CC} Lock-Out Voltage	V_{LKO}	—		2.3	2.5	V

*1: I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 10 MHz) .

*2: I_{CC} is active while Embedded Algorithm (program or erase) is in progress.

*3: Automatic sleep mode enables the low power mode when address remains stable for 150 ns.

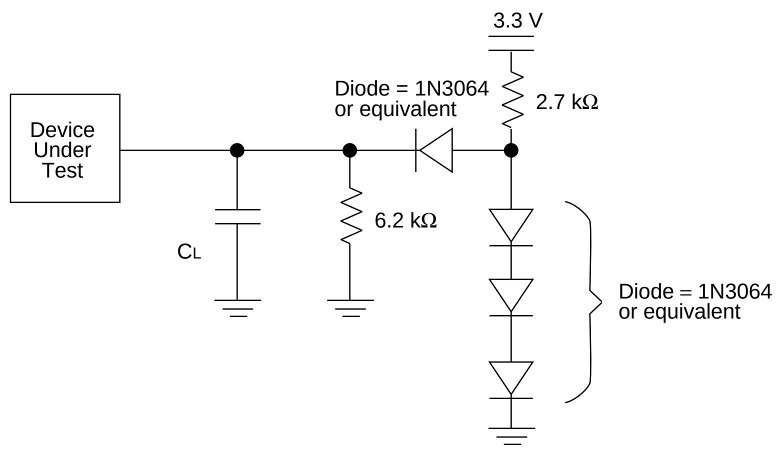
*4: (V_{ID} – V_{CC}) do not exceed 9 V.

■ AC CHARACTERISTICS

• **Read Only Operations Characteristics**

Parameter	Symbols		Test Setup	Value*						Unit
				60		70		90		
	JEDEC	Standard		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	—	60	—	70	—	90	—	ns
Address to Output Delay	t_{AVQV}	t_{ACC}	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	—	60	—	70	—	90	ns
Chip Enable to Output Delay	t_{ELQV}	t_{CE}	$\overline{OE} = V_{IL}$	—	60	—	70	—	90	ns
Output Enable to Output Delay	t_{GLQV}	t_{OE}	—	—	30	—	30	—	35	ns
Chip Enable to Output High-Z	t_{EHQZ}	t_{DF}	—	—	25	—	25	—	30	ns
Output Enable to Output High-Z	t_{GHQZ}	t_{DF}	—	—	25	—	25	—	30	ns
Output Hold Time From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First	t_{AXQX}	t_{OH}	—	0	—	0	—	0	—	ns
$\overline{RESET}$ Pin Low to Read Mode	—	t_{READY}	—	—	20	—	20	—	20	µs
$\overline{CE}$ to $\overline{BYTE}$ Switching Low or High	—	t_{ELFL} t_{ELFH}	—	—	5	—	5	—	5	ns

* : Test Conditions :
Output Load : 1 TTL gate and 30 pF (MBM29LV800TE60/BE60, MBM29LV800TE70/BE70)
1 TTL gate and 100 pF (MBM29LV800TE90/BE90)
Input rise and fall times : 5 ns
Input pulse levels : 0.0 V or 3.0 V
Timing measurement reference level
Input : 1.5 V
Output : 1.5 V



Note : C_L = 30 pF including jig capacitance (MBM29LV800TE60/BE60, MBM29LV800TE70/BE70)
C_L = 100 pF including jig capacitance (MBM29LV800TE90/BE90)

Test Conditions

• **Write/Erase/Program Operations**

Parameter		Symbol JEDEC	Symbol Standard	60 Min	60 Typ	60 Max	70 Min	70 Typ	70 Max	90 Min	90 Typ	90 Max	Unit
Write Cycle Time		t_{AVAV}	t_{WC}	60	—	—	70	—	—	90	—	—	ns
Address Setup Time		t_{AVWL}	t_{AS}	0	—	—	0	—	—	0	—	—	ns
Address Hold Time		t_{WLAX}	t_{AH}	45	—	—	45	—	—	45	—	—	ns
Data Setup Time		t_{DVWH}	t_{DS}	30	—	—	35	—	—	45	—	—	ns
Data Hold Time		t_{WHDX}	t_{DH}	0	—	—	0	—	—	0	—	—	ns
Output Enable Setup Time		—	t_{OES}	0	—	—	0	—	—	0	—	—	ns
Output Enable Hold Time	Read	—	t_{OEH}	0	—	—	0	—	—	0	—	—	ns
	Toggle and $\overline{\text{Data}}$ Polling			10	—	—	10	—	—	10	—	—	ns
Read Recover Time Before Write		t_{GHWL}	t_{GHWL}	0	—	—	0	—	—	0	—	—	ns
Read Recover Time Before Write		t_{GHEL}	t_{GHEL}	0	—	—	0	—	—	0	—	—	ns
$\overline{\text{CE}}$ Setup Time		t_{ELWL}	t_{CS}	0	—	—	0	—	—	0	—	—	ns
$\overline{\text{WE}}$ Setup Time		t_{WLEL}	t_{WS}	0	—	—	0	—	—	0	—	—	ns
$\overline{\text{CE}}$ Hold Time		t_{WHEH}	t_{CH}	0	—	—	0	—	—	0	—	—	ns
$\overline{\text{WE}}$ Hold Time		t_{EHWH}	t_{WH}	0	—	—	0	—	—	0	—	—	ns
Write Pulse Width		t_{WLWH}	t_{WP}	30	—	—	35	—	—	45	—	—	ns
$\overline{\text{CE}}$ Pulse Width		t_{ELEH}	t_{CP}	30	—	—	35	—	—	45	—	—	ns
Write Pulse Width High		t_{WHWL}	t_{WPH}	25	—	—	25	—	—	25	—	—	ns
$\overline{\text{CE}}$ Pulse Width High		t_{EHEL}	t_{CPH}	25	—	—	25	—	—	25	—	—	ns
Programming Operation	Byte	t_{WHWH1}	t_{WHWH1}	—	8	—	—	8	—	—	8	—	µs
	Word				16		—	16	—	—	16	—	
Sector Erase Operation *1		t_{WHWH2}	t_{WHWH2}	—	1	—	—	1	—	—	1	—	s
V_{CC} Setup Time		—	t_{VCS}	50	—	—	50	—	—	50	—	—	µs
Rise Time to V_{ID} *2		—	t_{VIDR}	500	—	—	500	—	—	500	—	—	ns
Voltage Transition Time *2		—	t_{VLHT}	4	—	—	4	—	—	4	—	—	µs
Write Pulse Width *2		—	t_{WPP}	100	—	—	100	—	—	100	—	—	µs
$\overline{\text{OE}}$ Setup Time to $\overline{\text{WE}}$ Active *2		—	t_{OESP}	4	—	—	4	—	—	4	—	—	µs
$\overline{\text{CE}}$ Setup Time to $\overline{\text{WE}}$ Active *2		—	t_{CSP}	4	—	—	4	—	—	4	—	—	µs
Recover Time From RY/$\overline{\text{BY}}$		—	t_{RB}	0	—	—	0	—	—	0	—	—	ns
$\overline{\text{RESET}}$ Pulse Width		—	t_{RP}	500	—	—	500	—	—	500	—	—	ns
$\overline{\text{RESET}}$ High Level Period Before Read		—	t_{RH}	200	—	—	200	—	—	200	—	—	ns
$\overline{\text{BYTE}}$ Switching Low to Output High-Z		—	t_{FLQZ}	—	—	25	—	—	25	—	—	30	ns

(Continued)

(Continued)

Parameter	Symbol		MBM29LV800TE/BE									Unit
			60			70			90			
	JEDEC	Standard	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$\overline{\text{BYTE}}$ Switching High to Output Active	—	t_{FHQV}	—	—	60	—	—	70	—	—	90	ns
Program/Erase Valid to RY/$\overline{\text{BY}}$ Delay	—	t_{BUSY}	—	—	90	—	—	90	—	—	90	ns
Delay Time from Embedded Output Enable	—	t_{EOE}	—	—	60	—	—	70	—	—	90	ns
Erase Time-out Time	—	t_{TOW}	50			50	—	—	50	—	—	µs
Erase Suspend Transition Time	—	t_{SPD}			20	—	—	20	—	—	20	µs

*1: Does not include the preprogramming time.

*2: For Sector Protection operation.

■ ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min	Typ	Max		
Sector Erase Time	—	1	10	s	Excludes programming time prior to erasure
Byte Programming Time	—	8	300	µs	Excludes system-level overhead
Word Programming Time	—	16	360		
Chip Programming Time	—	8.4	25	s	Excludes system-level overhead
Erase/Program Cycle	100,000	—	—	cycle	—

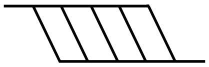
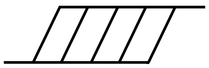
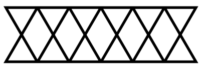
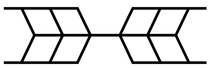
■ TSOP (1) , FBGA, CSOP PIN CAPACITANCE

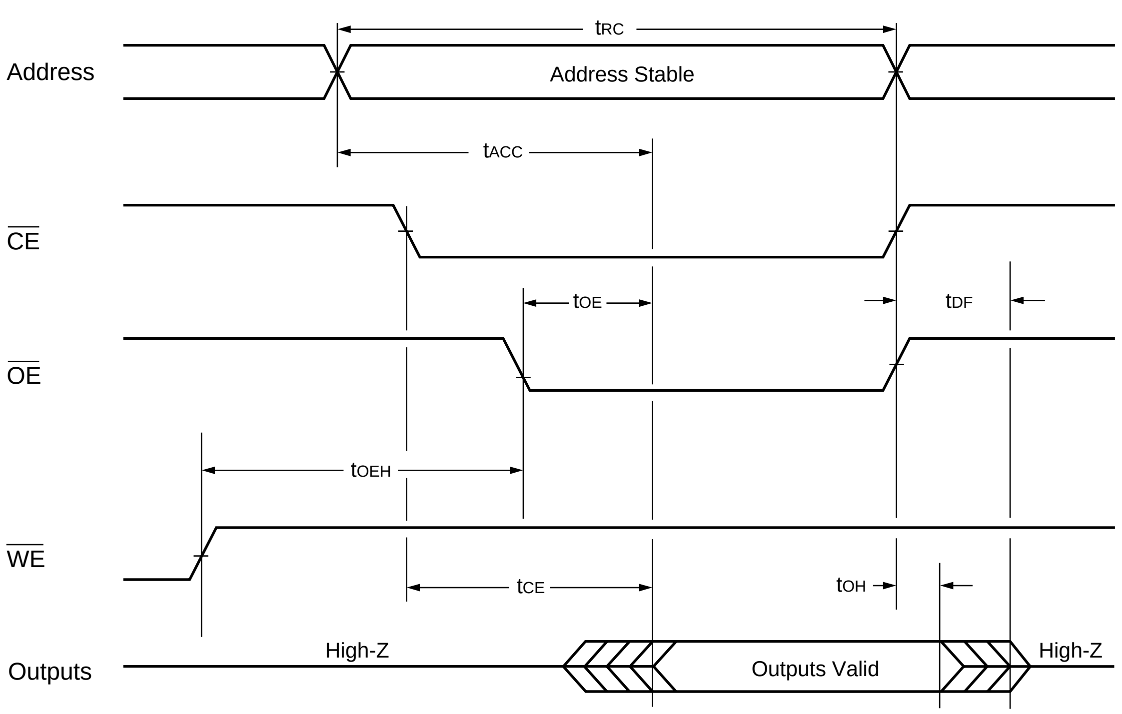
Parameter	Symbol	Test Setup	Typ	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0$	7.5	9.5	pF
Output Capacitance	C_{OUT}	$V_{OUT} = 0$	8.0	10.0	pF
Control Pin Capacitance	C_{IN2}	$V_{IN} = 0$	10.0	13.0	pF

Notes : • Test conditions $T_A = +25$ °C, f = 1.0 MHz
• DQ_{15}/A_{-1} pin capacitance is stipulated by output capacitance.

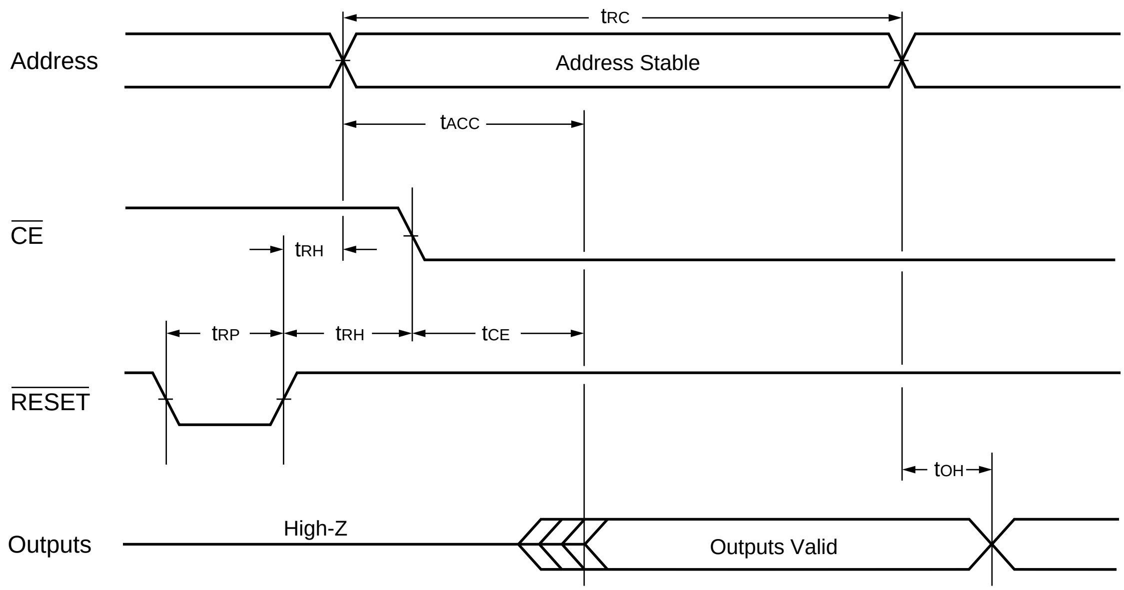
■ TIMING DIAGRAM

• **Key to Switching Waveforms**

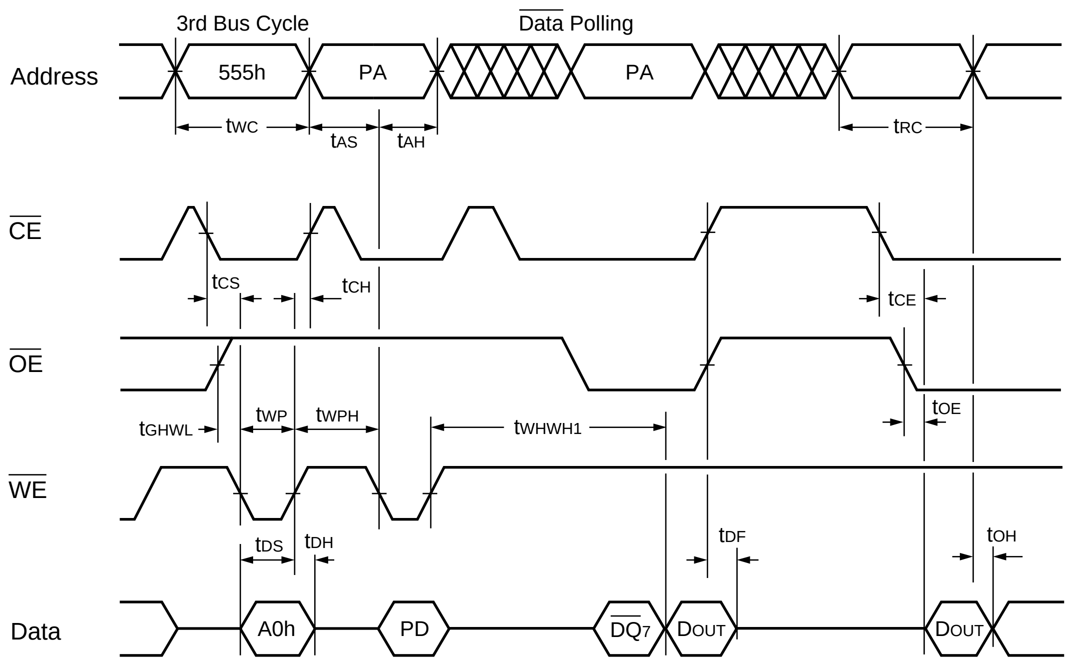
WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Change from H to L
	May Change from L to H	Will Change from L to H
	"H" or "L": Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State



Read Operation Timing Diagram

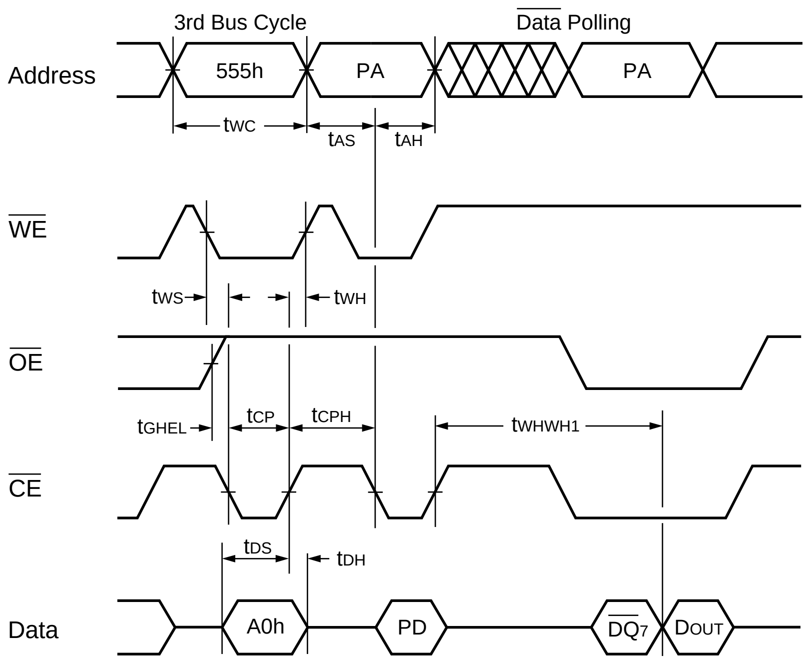


Hardware Reset/Read Operation Timing Diagram



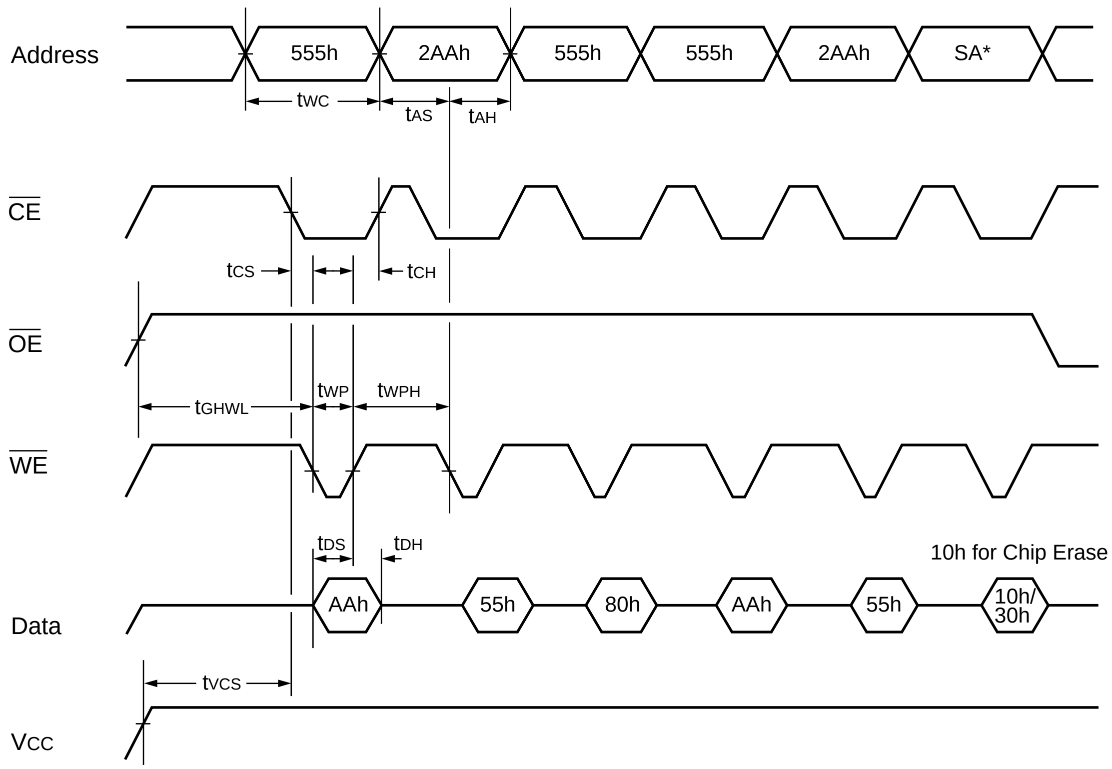
Notes :
- PA is the address of the memory location to be programmed.
- PD is the data to be programmed at word address.
- $\overline{DQ_7}$ is the output of the complement of the data written to the device.
- D_{OUT} is the output of the data written to the device.
- Figure indicates the last two bus cycles out of four bus cycles sequence.
- These waveforms are for the × 16 mode (the addresses differ from × 8 mode).

Alternate $\overline{\text{WE}}$ Controlled Program Operation Timing Diagram



Notes : • PA is the address of the memory location to be programmed.
- PD is the data to be programmed at word address.
- $\overline{DQ_7}$ is the output of the complement of the data written to the device.
- D_{OUT} is the output of the data written to the device.
- Figure indicates the last two bus cycles out of four bus cycles sequence.
- These waveforms are for the $\times$ 16 mode (the addresses differ from $\times$ 8 mode) .

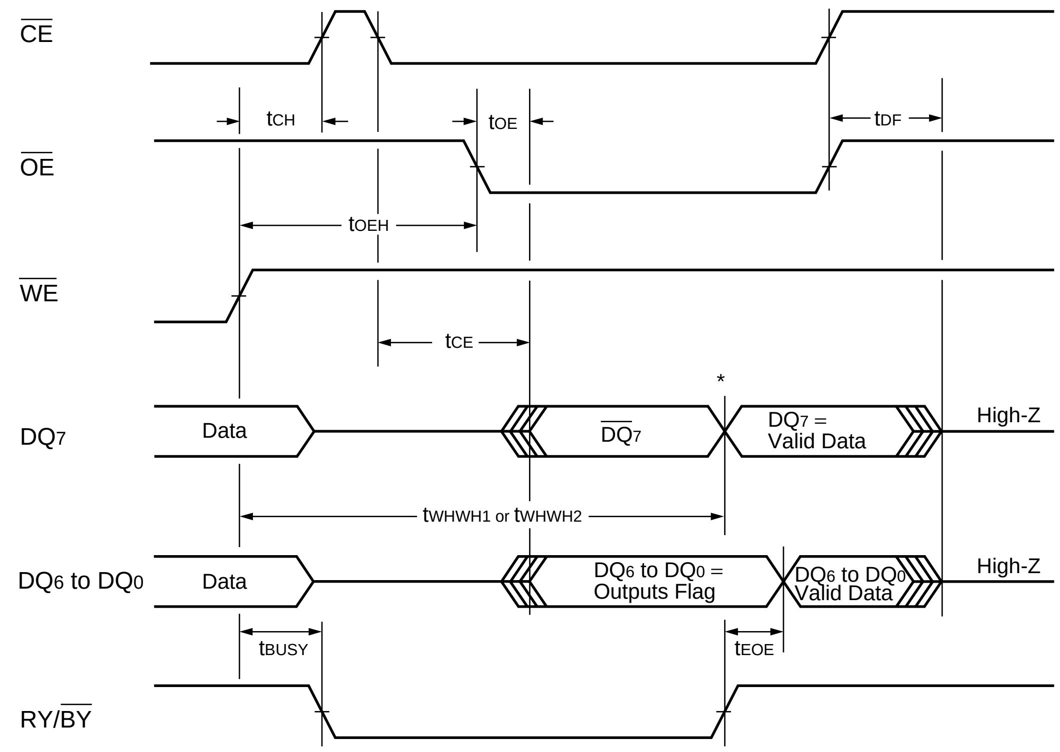
Alternate $\overline{\text{CE}}$ Controlled Program Operation Timing Diagram



* : SA is the sector address for Sector Erase. Addresses = 555h (Word) for Chip Erase.

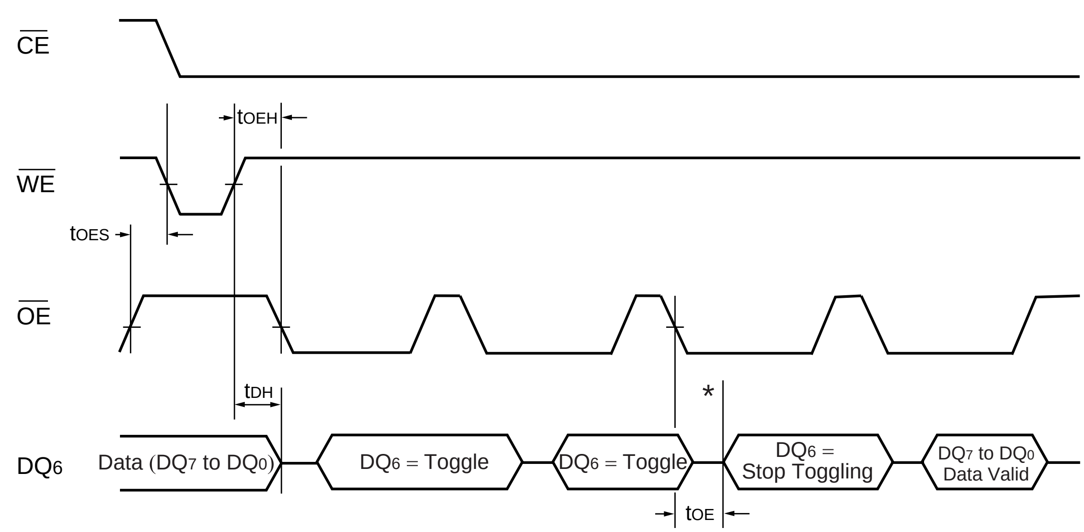
Note : These waveforms are for the × 16 mode (the addresses differ from × 8 mode) .

Chip/Sector Erase Operation Timing Diagram



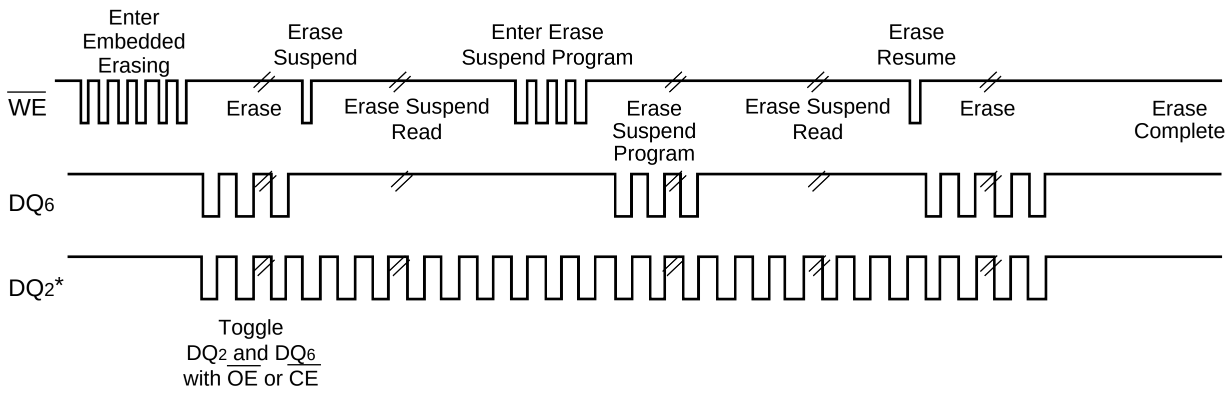
* : DQ_7 = Valid Data (The device has completed the Embedded operation) .

Data Polling during Embedded Algorithm Operation Timing Diagram



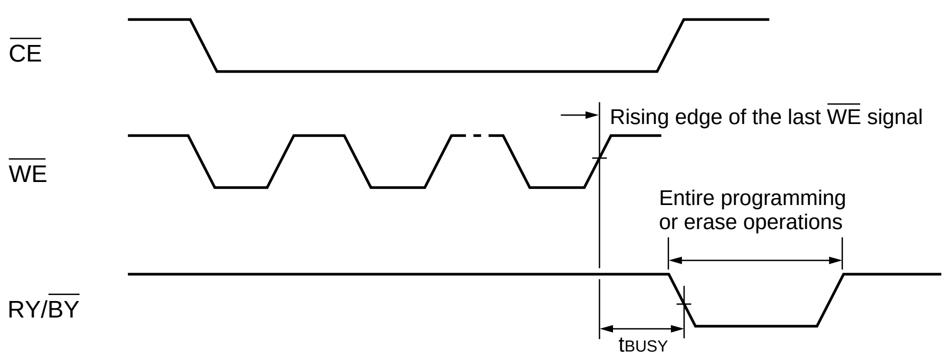
* : DQ_6 = Stops toggling. (The device has completed the Embedded operation.)

Toggle Bit I during Embedded Algorithm Operation Timing Diagram

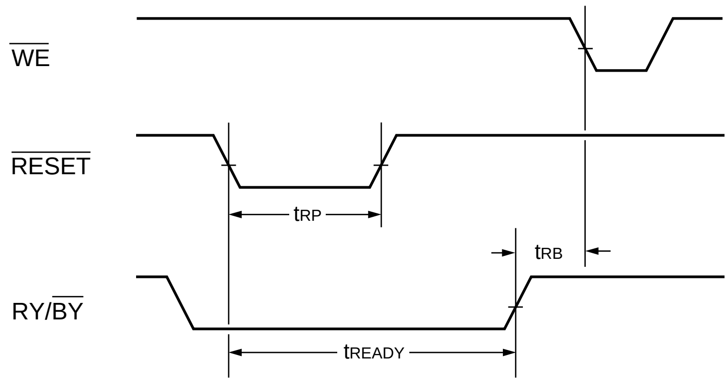


* : DQ_2 is read from the erase-suspended sector.

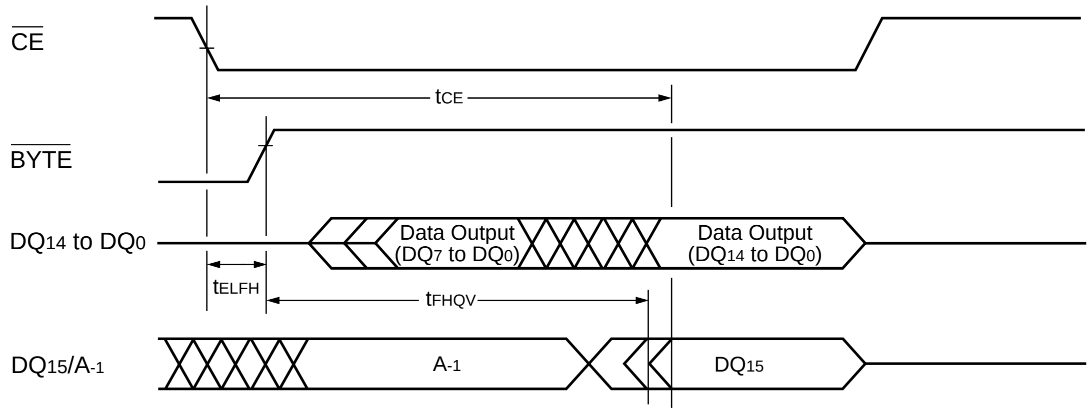
DQ_2 vs. DQ_6



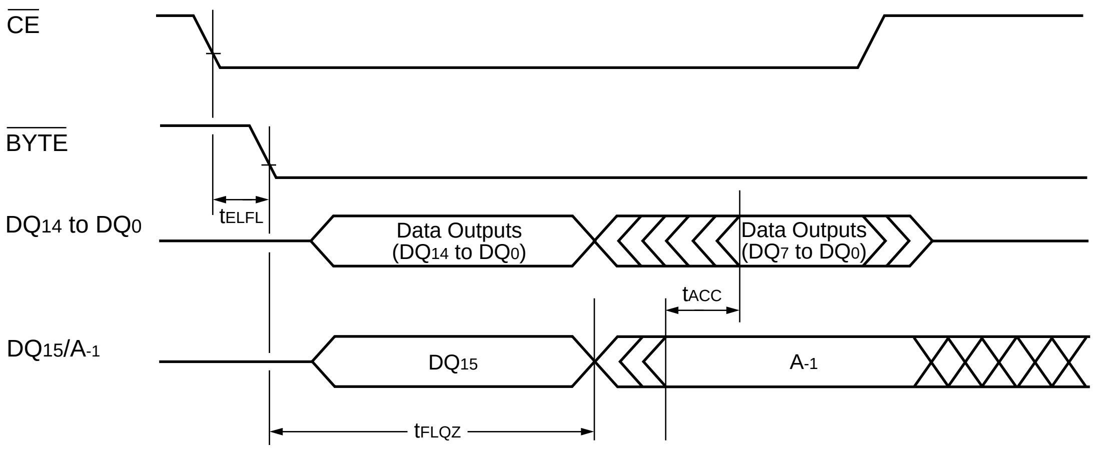
RY/BY Timing Diagram during Program/Erase Operation Timing Diagram



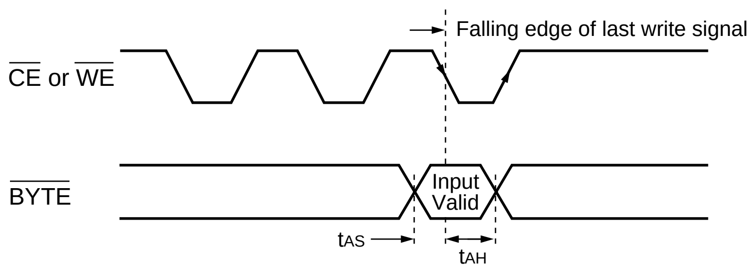
RESET, RY/BY Timing Diagram



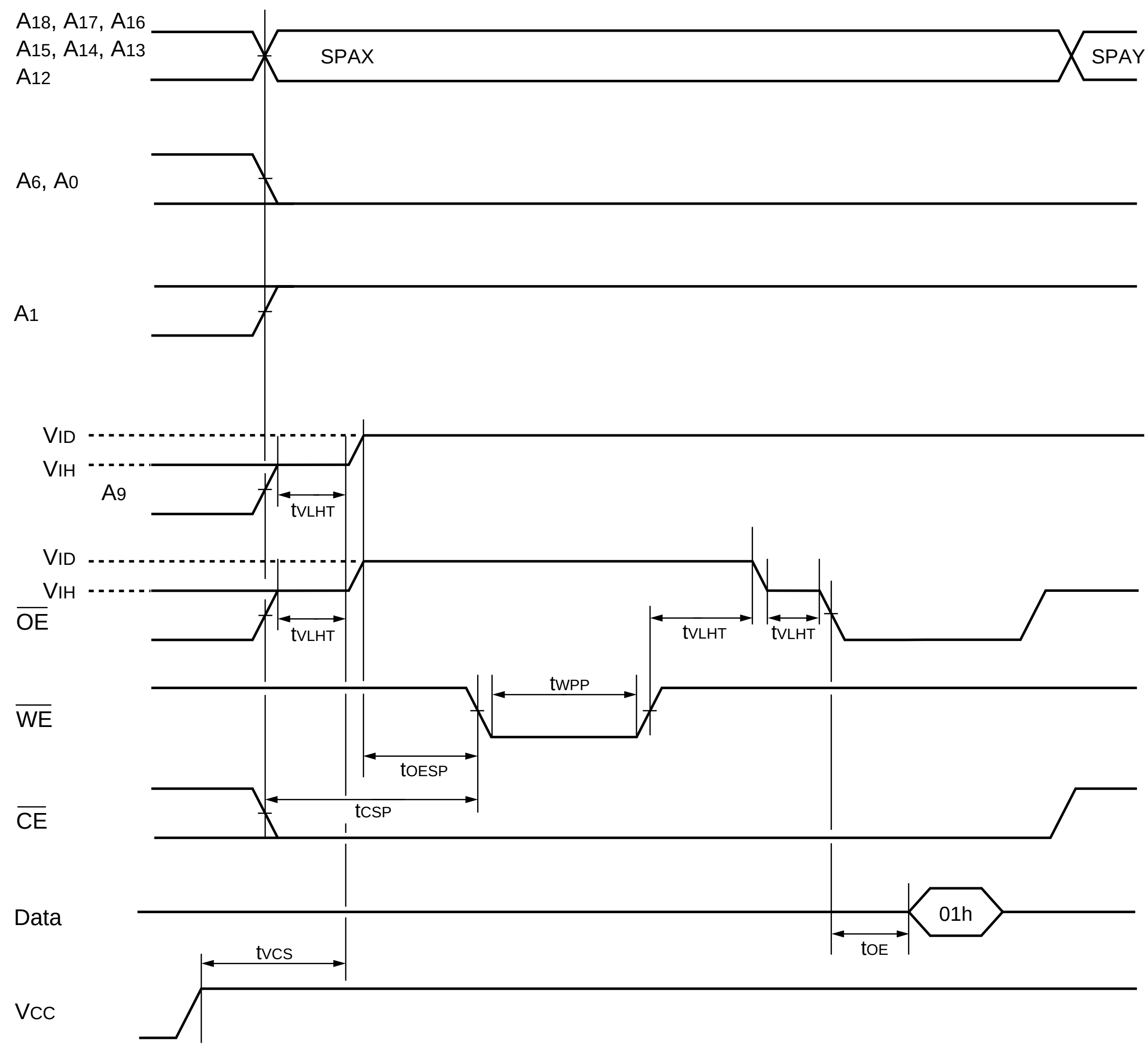
Timing Diagram for Word Mode Configuration



Timing Diagram for Byte Mode Configuration



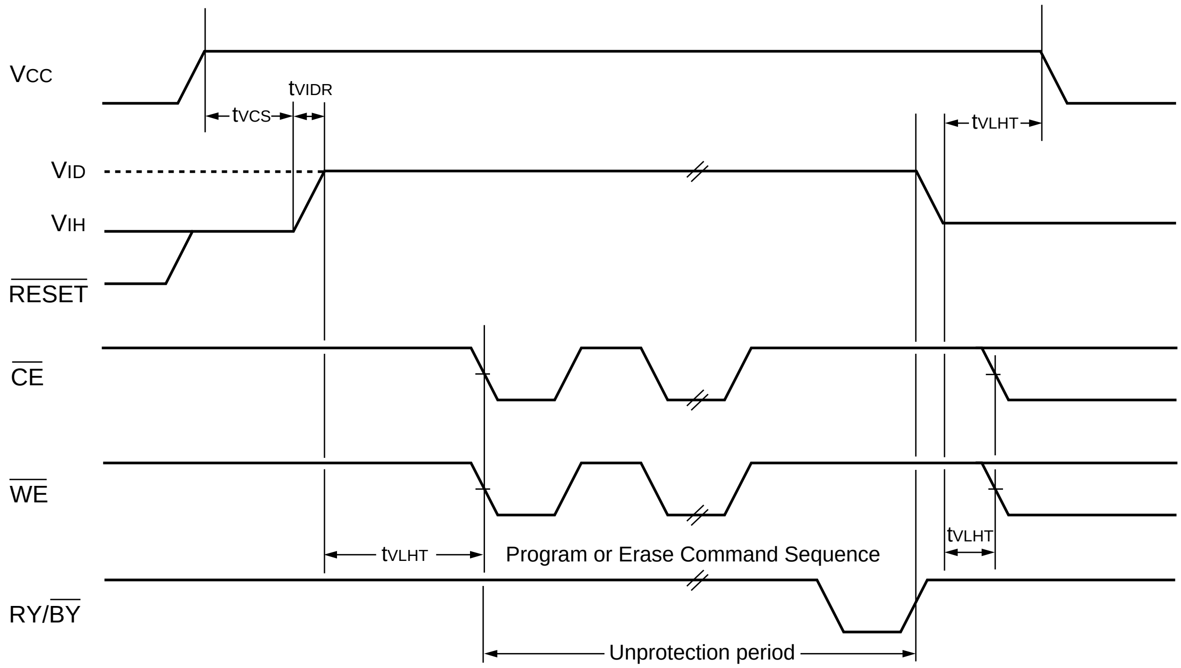
BYTE Timing Diagram for Write Operations



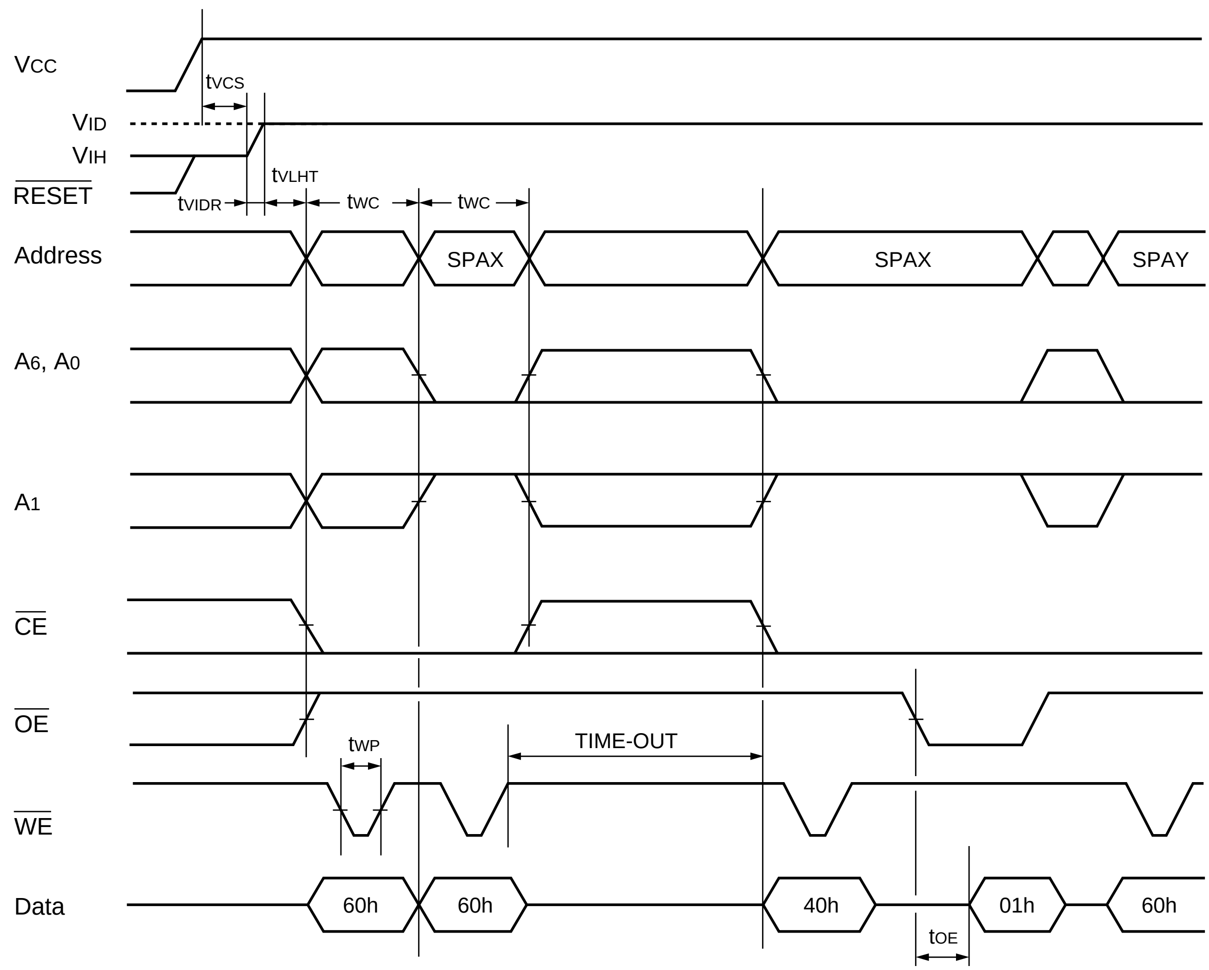
SPAX : Sector Address to be protected.
SPAY : Next Sector Address to be protected.

Note : A_{-1} is V_{IL} on byte mode.

Sector Protection Timing Diagram



Temporary Sector Unprotection Timing Diagram

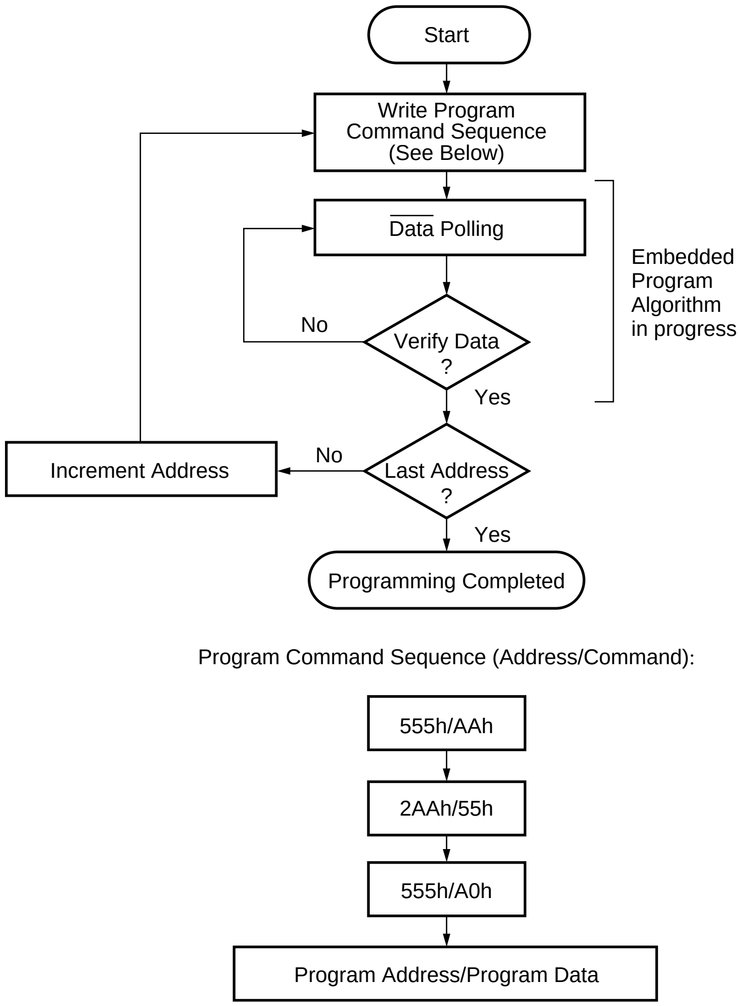


SPAX : Sector Address to be protected
SPAY : Next Sector Address to be protected
TIME-OUT : Time-Out window = 150 µs (Min)

Extended Sector Protection Timing Diagram

■ FLOW CHART

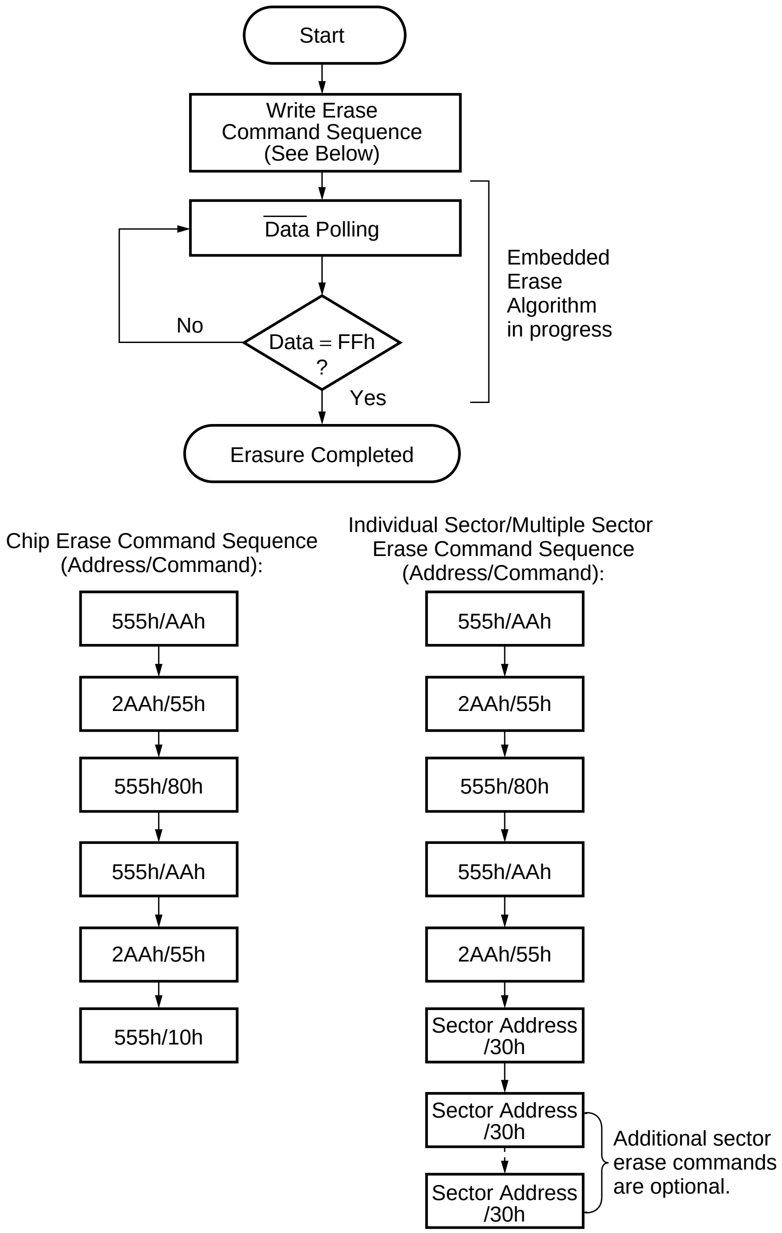
EMBEDDED ALGORITHM



Notes : • The sequence is applied for × 16 mode.
• The addresses differ from × 8 mode.

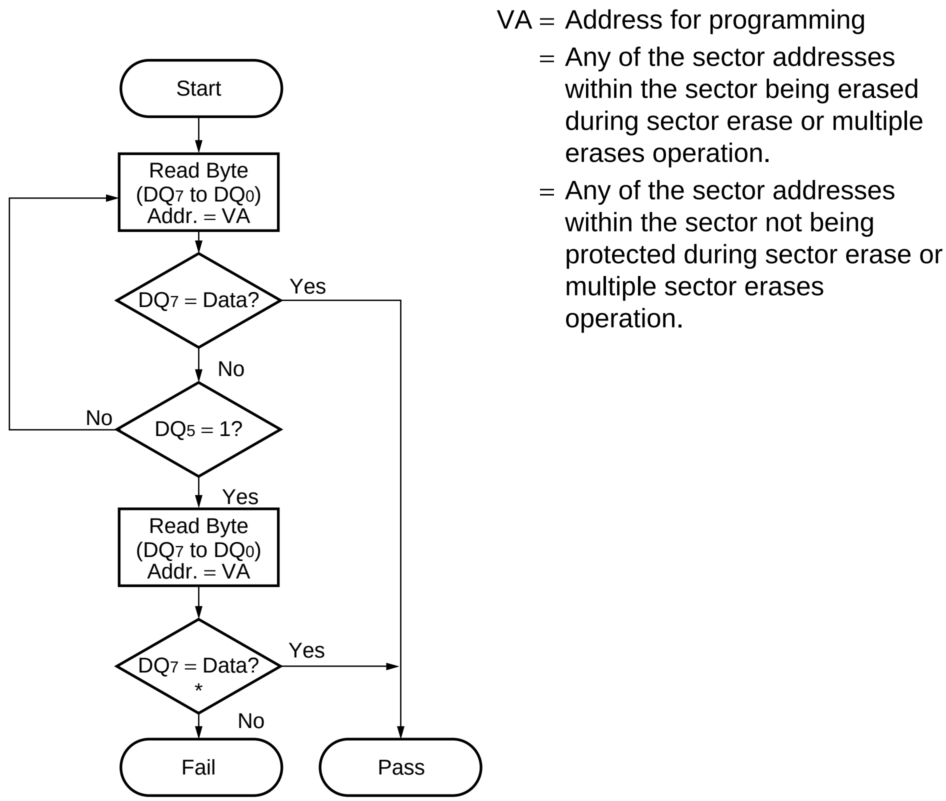
Embedded Program™ Algorithm

EMBEDDED ALGORITHM



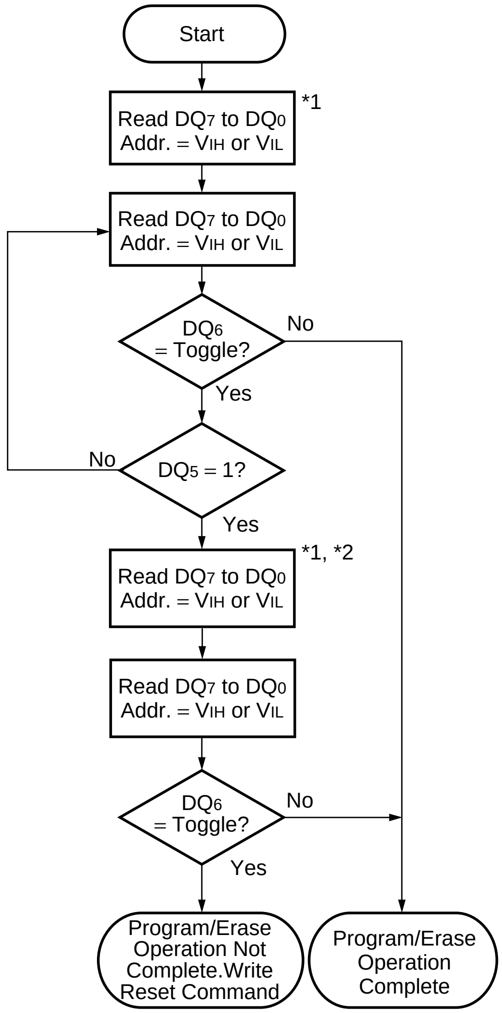
Notes :
- The sequence is applied for × 16 mode.
- The addresses differ from × 8 mode.

Embedded Erase™ Algorithm



* : DQ_7 is rechecked even if DQ_5 = “1” because DQ_7 may change simultaneously with DQ_5.

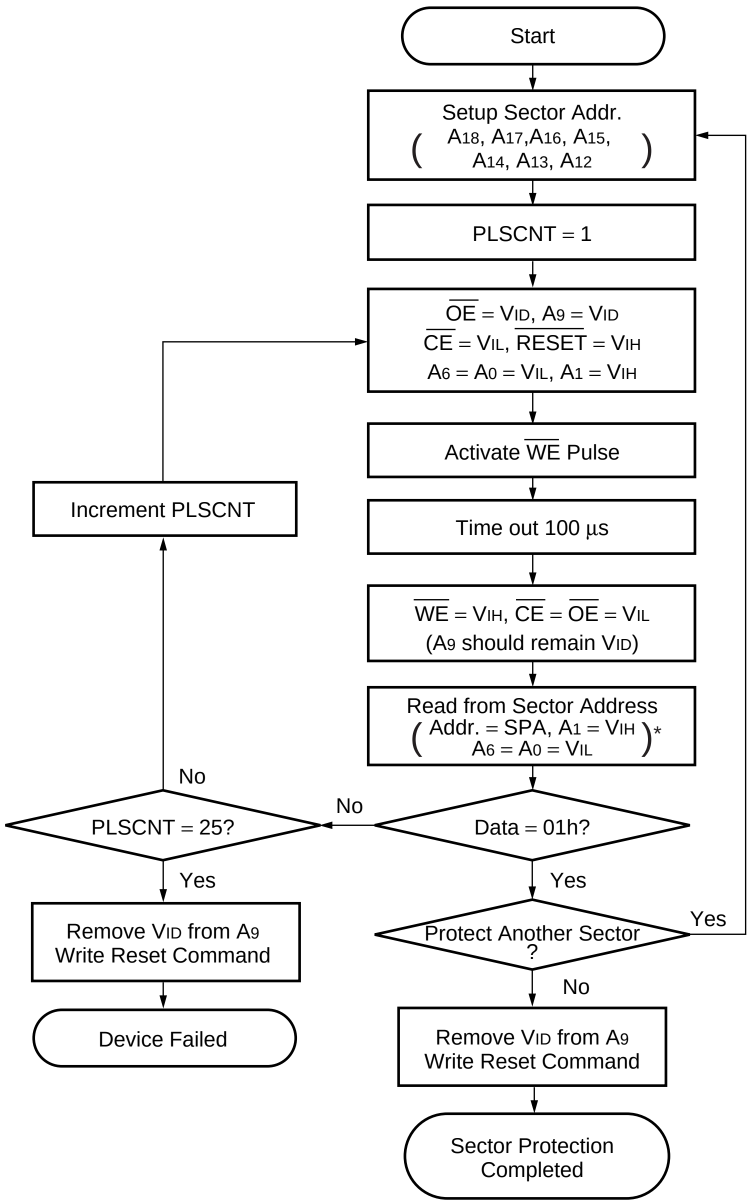
$\overline{\text{Data}}$ Polling Algorithm



*1 : Read toggle bit twice to determine whether it is toggling.

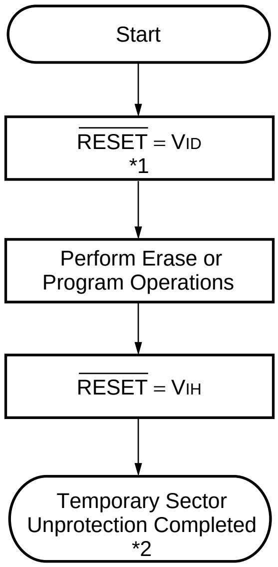
*2 : Recheck toggle bit because it may stop toggling as DQ_5 changes to “1”.

Toggle Bit Algorithm



* : A_{-1} is V_{IL} on byte mode.

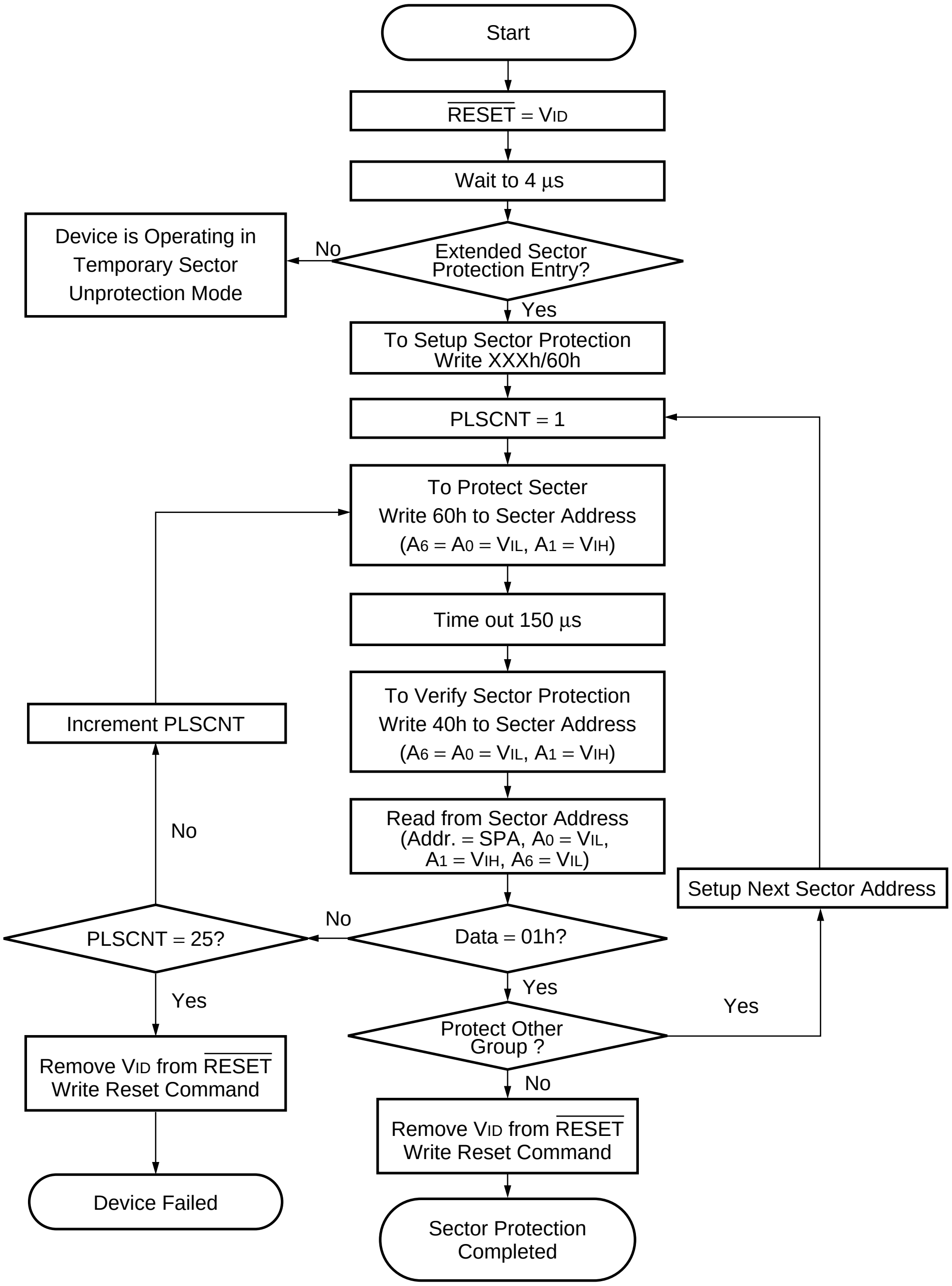
Sector Protection Algorithm



*1 : All protected sectors are unprotected.

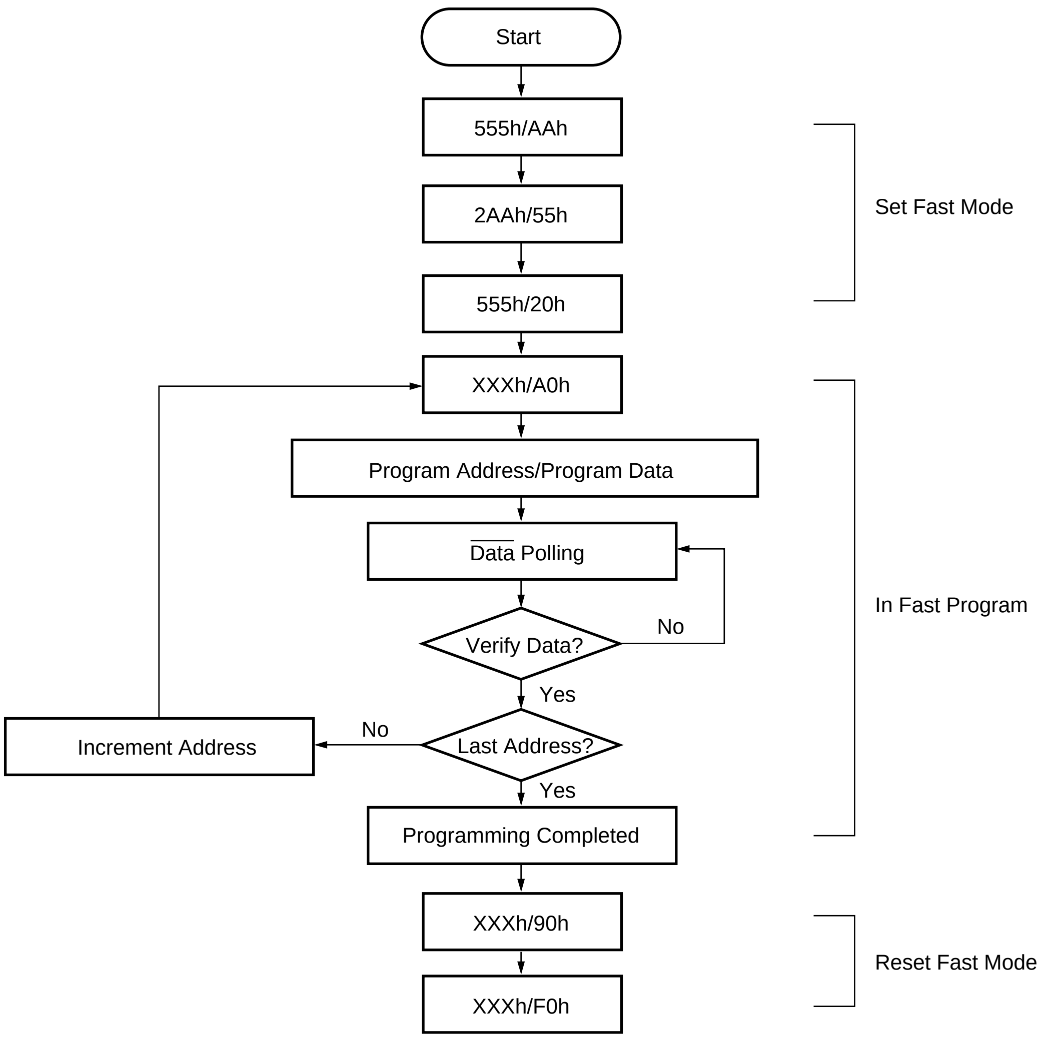
*2 : All previously protected sectors are protected once again.

Temporary Sector Unprotection Algorithm



Extended Sector Protection Algorithm

FAST MODE ALGORITHM



Notes : • The sequence is applied for × 16 mode.
• The addresses differ from × 8 mode.

Embedded Programming Algorithm for Fast Mode

■ ORDERING INFORMATION

Part No.	Package	Access Time (ns)	Remarks
MBM29LV800TE60TN MBM29LV800TE70TN MBM29LV800TE90TN	48-pin plastic TSOP (1) (FPT-48P-M19) (Normal Bend)	60 70 90	Top Sector
MBM29LV800TE60PCV MBM29LV800TE70PCV MBM29LV800TE90PCV	48-pin plastic CSOP (LCC-48P-M03)	60 70 90	
MBM29LV800TE60PBT MBM29LV800TE70PBT MBM29LV800TE90PBT	48-ball plastic FBGA (BGA-48P-M20)	60 70 90	
MBM29LV800BE60TN MBM29LV800BE70TN MBM29LV800BE90TN	48-pin plastic TSOP (1) (FPT-48P-M19) (Normal Bend)	60 70 90	Bottom Sector
MBM29LV800BE60PCV MBM29LV800BE70PCV MBM29LV800BE90PCV	48-pin plastic CSOP (LCC-48P-M03)	60 70 90	
MBM29LV800BE60PBT MBM29LV800BE70PBT MBM29LV800BE90PBT	48-ball plastic FBGA (BGA-48P-M20)	60 70 90	

MBM29LV800 T E 60 PCV

PACKAGE TYPE
TN = 48-Pin Thin Small Outline Package (TSOP) Standard Pinout
PCV = 48-Pin C-lead Small Outline Package (CSOP)
PBT = 48-Ball Fine Pitch Ball Grid Array Package (FBGA)

SPEED OPTION
See Product Selector Guide

Device Revision

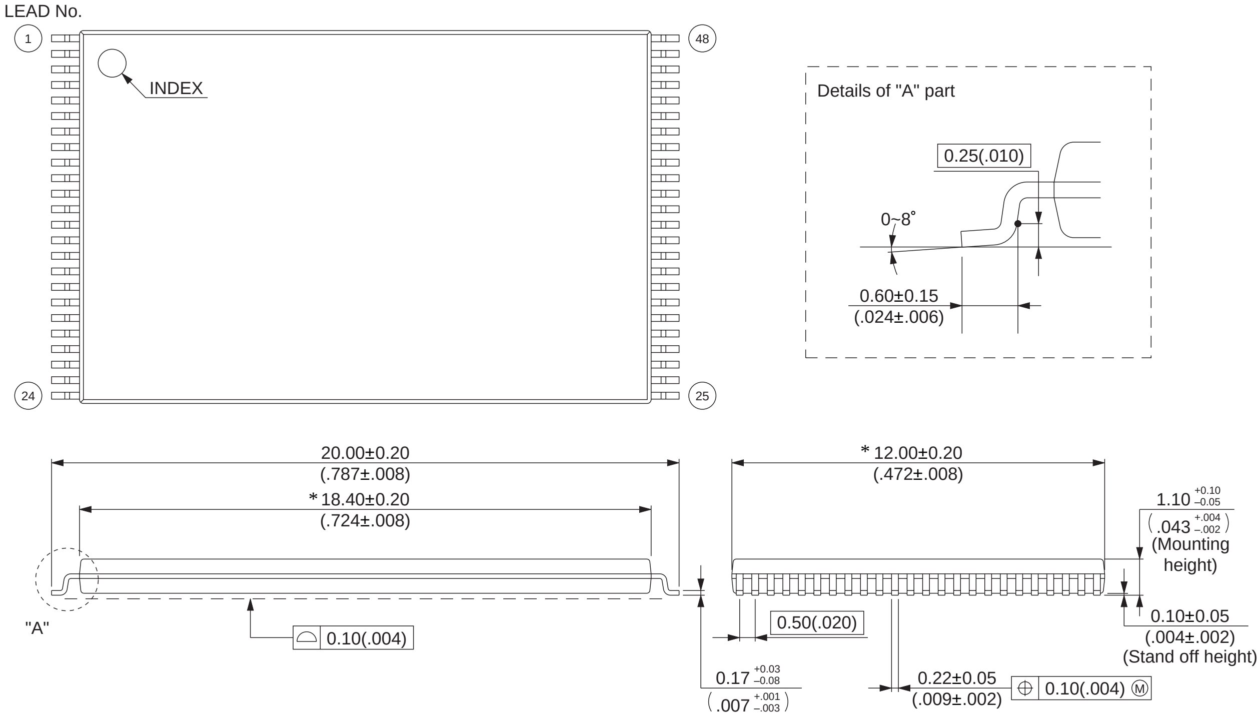
BOOT CODE SECTOR ARCHITECTURE
T = Top sector
B = Bottom sector

DEVICE NUMBER/DESCRIPTION
MBM29LV800
8 Mega-bit (1 M × 8-Bit or 512 K × 16-Bit) CMOS Flash Memory
3.0 V-only Read, Program, and Erase

■ PACKAGE DIMENSIONS

48-pin plastic TSOP (1)
(FPT-48P-M19)

Note 1) * : Values do not include resin protrusion.
Resin protrusion and gate protrusion are +0.15 (.006) Max (each side) .
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

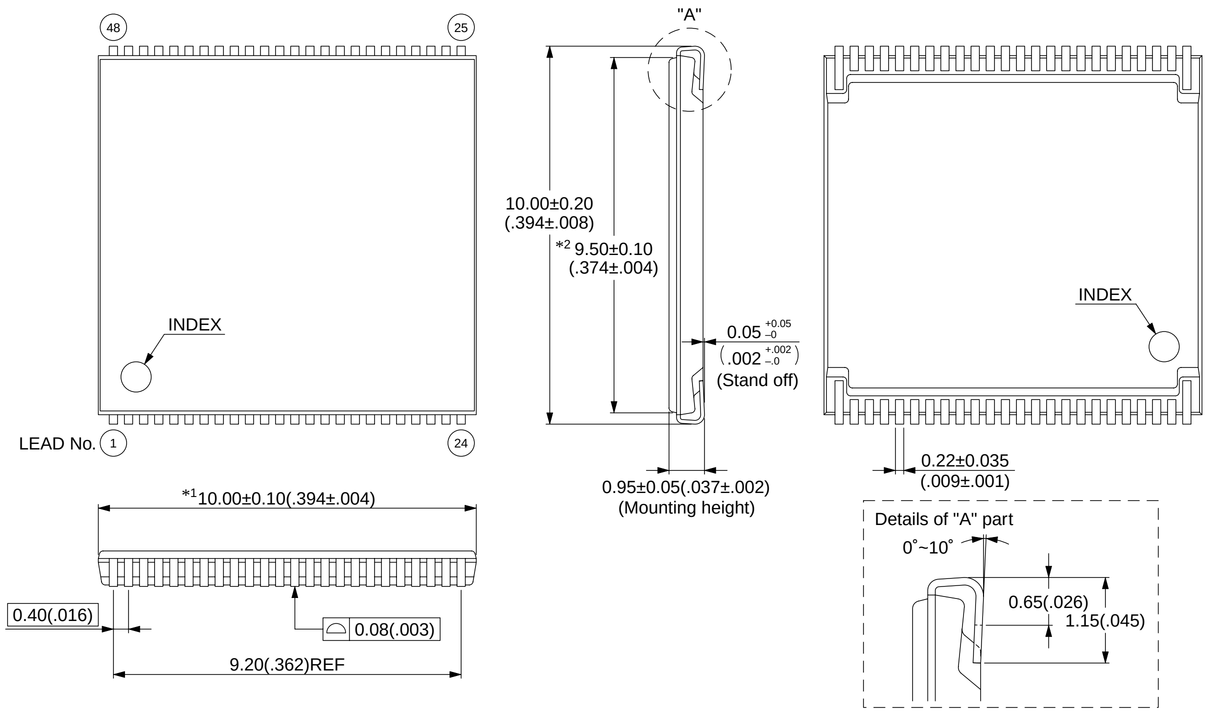


Dimensions in mm (inches) .
Note : The values in parentheses are reference values.

(Continued)

48-pin plastic CSOP
(LCC-48P-M03)

Note 1) *1 : Resin protrusion. (Each side : +0.15 (.006) Max) .
Note 2) *2 : These dimensions do not include resin protrusion.
Note 3) Pins width includes plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.

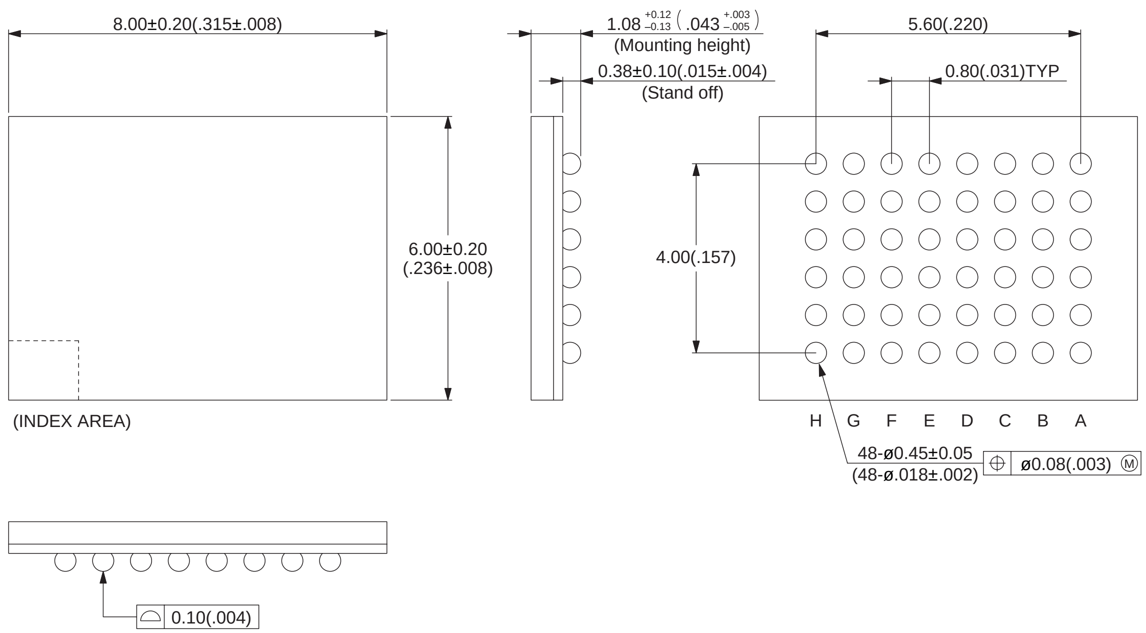


Dimensions in mm (inches) .
Note : The values in parentheses are reference values.

(Continued)

(Continued)

48-ball plastic FBGA
(BGA-48P-M20)



Dimensions in mm (inches) .
Note : The values in parentheses are reference values.

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