Specification

1. FEATURES

* Operating voltage : 2.5V - 5.5V.
* Maximum CPU operating frequency : 4,194,304Hz at 2.7V.
* Provide X' tal or RC oscillator. Both can run at high speed or slow speed(low power).
  RC oscillator can detect internal or external resister automatically.
* I/O port.
- 24 I/O pins.
  - 8 of 24 pins with wake up function.
* Five 12-bit timers.
* Four channels for voice or melody processing.
* Two DACs for voice or melody playing. Also, internal programming for single DAC playing.
* One pair of PWM for voice or melody playing.
* Eight interrupt sources :

NMI - Can be Watchdog Timer interrupt
IRQ0 - Timer 0 interrupt
IRQ1 - Timer 1 interrupt
IRQ2 - Timer 2 interrupt
IRQ3 - Timer 3 interrupt
IRQ4 - Timer 4 interrupt
IRQ5 - External interrupt
IRQ6 - Base Timer interrupt

2. PIN NAME ASSIGNMENT (Total: 97 pads)

	Pin Name	I/O	Function description
1)	P10~P17	I/O	8-bit I/O pins for port 1 with wake-up interrupt
2)	P20~P27	I/O	8-bit I/O pins for port 2
3)	P30~P37	I/O	8-bit I/O pins for port 3
4)	DAC1	O	Current output port
5)	DAC2	O	Current output port
6)	PWM1	O	Voltage output port
7)	PWM2	O	Voltage output port
8)	VCOCAP	I/O	PLL used.
9)	RXOSC	I	X' TAL or Ring osc pad
10)	XOSC2	O	X' TAL pad
11)	RESB	I	System reset pin; internal pull_high.
12)	TESTB	I	Test pin; internal pull_high.
13)	VDD	I	Power
14)	VDD(PWM)	I	Power for PWM module
15)	GND1	I	Ground
16)	GND2	I	Ground
17)	GND(PWM)	I	Ground for PWM module
18)	ROMSEL[1:0]	I	Rom size selection.
19)	ROMCSB	O	For external rom chip enable
20)	ROMEB[3:0]	O	For external rom chip output enable
21)	RADDR[19:14]	O	For external rom address
22)	XADDR[4:1]	O	For external rom address
23)	ADDR[15:0]	I/O	External rom and CPU address
24)	DATA[7:0]	I	Data from external rom
25)	IRQA	I	Low can derive to 7 IRQ vectors.
26)	ICE_MOD	I	High can be ICE mode used.
27)	R/W	I/O	Internal or external CPU r/w
28)	CPUDATA[7:0]	I/O	Internal or external CPU data
29)	RDY6502	O	Internal CPU RDY
30)	IRQL	O	Internal CPU IRQ
31)	NMIL	O	Internal CPU NMI
32)	CRESB	O	Internal CPU RESETB

33)	CPUCLK	O	Internal CPU clock input.
34)	PGMB	I	For programming EPROM or FLASH_ROM.
32)	XR	I	X' tal or Ring osc selection.

3. ADDRESS ARRANGEMENT

1) RAM (max. 192 bytes)

0000-00BF for data storage.

0100-01BF for stack and data area.. This area is overlapped with 0000-00BF.

2) ROM

ROMSEL[1:0] to select rom size type:

ROMSEL[1:0]=11 -> Max. can implement 32Meg bits by 8Meg x 4

ROMSEL[1:0]=10 -> Max. can implement 16Meg bits by 4Meg x 4

ROMSEL[1:0]=01 -> Max. can implement 8Meg bits by 2Meg x 4

ROMSEL[1:0]=00 -> Max. can implement 4Meg bits by 1Meg x 4

Max. 32Meg bits for program and speech data area.

This area splits into 256 banks(000~255). There are 16k bytes for every bank.

Related address shows below:

	BANK address	CPU address	ROM address
bank 0	00000000	8000-BFFF	000000-003FFF
bank 1	00000001	8000-BFFF	004000-007FFF
bank 2	00000010	8000-BFFF	008000-00BFFF
.....			
bank 254	11111110	8000-BFFF	3F8000-3FBFFF
bank 255	11111111	8000-BFFF	3FC000-3FFFFF
(bank 255	11111111	C000-FFFF	3FC000-3FFFFF)

If RESET or IRQ or NMI or Bank address=FF

ROM address will indicate to 3FC000-3FFFFF.

FFFF, FFFE - IRQ vector.

FFFD, FFFC - RES vector.

FFFB, FFFA - NMI vector for watchdog interrupt.

3) IRQ vector, if IRQ vector is optioned to 7 levels.

IRQA=0 -> IRQ vector =FFFF,FFFE

IRQA=1 -> IRQ0 vector =FFE1,FFE0 (timer_0)

IRQ1 vector =FFE3,FFE2 (timer_1)
IRQ2 vector =FFE5,FFE4 (timer_2)
IRQ3 vector =FFE7,FFE6 (timer_3)
IRQ4 vector =FFE9,FFE8 (timer_4)
IRQ5 vector =FFEB,FFEA (external)
IRQ6 vector =FFED,FFEC (base timer)

4. Register description

(1) Read and Write

00C0 IRQ flag register. Read & write.

Read function :

Bit 0 : = 1 Timer 0 flag, IRQ 0.
1 : = 1 Timer 1 flag, IRQ 1
2 : = 1 Timer 2 flag, IRQ 2.
3 : = 1 Timer 3 flag, IRQ 3.
4 : = 1 Timer 4 flag, IRQ 4.
5 : = 1 External flag, IRQ5.
6 : = 1 Base Timer flag, IRQ6
7 : = 1 Reserved.

Write function :

Bit 0 : = 0 Clear timer 0 flag.
1 : = 0 Clear timer 1 flag.
2 : = 0 Clear timer 2 flag.
3 : = 0 Cclear timer 3 flag.
4 : = 0 Clear timer 4 flag.
5 : = 0 Clear External flag.
6 : = 0 Clear Base Timer flag.
7 : = 0 Reserved.

00C1 Port 1 data. Read & write.

00C2 Port 1 external interrupt high to low transient indicating flag. Read & write.
(Falling edge)

Read function:

Bit 0 : 1 Indicate port_10 transient from high to low FLAG.
Bit 1 : 1 Indicate port_11 transient from high to low FLAG.
Bit 2 : 1 Indicate port_12 transient from high to low FLAG.
Bit 3 : 1 Indicate port_13 transient from high to low FLAG.
Bit 4 : 1 Indicate port_14 transient from high to low FLAG.
Bit 5 : 1 Indicate port_15 transient from high to low FLAG.
Bit 6 : 1 Indicate port_16 transient from high to low FLAG.
Bit 7 : 1 Indicate port_17 transient from high to low FLAG.
* These flags will be cleared by clear external interrupt flag.

Write function:

Bit 0 : 0 Disable and clear port_10 transient high to low flag
Bit 1 : 0 Disable and clear port_11 transient high to low flag
Bit 2 : 0 Disable and clear port_12 transient high to low flag
Bit 3 : 0 Disable and clear port_13 transient high to low flag
Bit 4 : 0 Disable and clear port_14 transient high to low flag
Bit 5 : 0 Disable and clear port_15 transient high to low flag
Bit 6 : 0 Disable and clear port_16 transient high to low flag
Bit 7 : 0 Disable and clear port_17 transient high to low flag

* The default value for each bit is 0.

00C3 Port 1 external interrupt low to high transient indicating flag. Read & write
(Rising edge)

Read function:

Bit 0 : 1 Indicate port_10 transient from low to high flag.
Bit 1 : 1 Indicate port_11 transient from low to high flag.
Bit 2 : 1 Indicate port_12 transient from low to high flag.
Bit 3 : 1 Indicate port_13 transient from low to high flag.
Bit 4 : 1 Indicate port_14 transient from low to high flag.
Bit 5 : 1 Indicate port_15 transient from low to high flag.
Bit 6 : 1 Indicate port_16 transient from low to high flag.
Bit 7 : 1 Indicate port_17 transient from low to high flag.
* These flags will be cleared by clear external interrupt flag.

Write function:

Bit 0 : 0 Disable and clear port_10 transient low to high flag
Bit 1 : 0 Disable and clear port_11 transient low to high flag
Bit 2 : 0 Disable and clear port_12 transient low to high flag
Bit 3 : 0 Disable and clear port_13 transient low to high flag
Bit 4 : 0 Disable and clear port_14 transient low to high flag
Bit 5 : 0 Disable and clear port_15 transient low to high flag
Bit 6 : 0 Disable and clear port_16 transient low to high flag
Bit 7 : 0 Disable and clear port_17 transient low to high flag
* The default value for each bit is 0.

00C4 Port 2 data. Read & write.

00C5 Port 3 data. Read & write.

(2) Port definition

00D0 Set port 1 bit function. Write only.

* An '1' in this register will set the corresponding pin of port 1 as an output pin.

* The default value for each bit is 0.

00D1 Set port 1 pull-up resistor. Write only.

* An '1' in this register will enable the pull-up resistor of the corresponding pin of port 1. But the pull-up resistor will be disabled if the pin is output low.
* The default value for each bit is 0.

00D2 Set port 1 pull-low resistor. Write only.

* An '1' in this register will enable the pull-low resistor of the corresponding pin of port 1. But the pull-low resistor will be disabled if the pin is output low.
* The default value for each bit is 0.

00D3 Set port 1 bitwise input type function. Write only.

Bit 0 : = 0 set this pin as an inverter type input.
= 1 set this pin as a schmitt type input.
1 : = 0 set this pin as an inverter type input.
= 1 set this pin as a schmitt type input.
2 : = 0 set this pin as an inverter type input.
= 1 set this pin as a schmitt type input.
3 : = 0 set this pin as an inverter type input.
= 1 set this pin as a dimmer type input.
4 : = 0 set this pin as an inverter type input.
= 1 set this pin as a dimmer type input.
5 : = 0 set this pin as an inverter type input.
= 1 set this pin as a schmitt type input.
6 : = 0 set this pin as a schmitt type input.
= 1 set this pin as an inverter type input.
7 : = 0 set this pin as a schmitt type input.
= 1 set this pin as an inverter type input.

* The default value for each bit is 0.

00D4 Port1 bitwise output type function selection. Write only.

Bit [7:0]= 0 set this pin as a buffer type output buffer.

0 : = 1 carrying 37.4kHz while data=1

1 : = 1 carrying 37.4kHz while data=0

2 : = 1 carrying 37.4kHz while data=1

3 : = 1 carrying 37.4kHz while data=0

4 : = 1 carrying 37.4kHz while data=1

5 : = 1 carrying 37.4kHz while data=0

6 : = 1 carrying 37.4kHz while data=1

7 : = 1 carrying 37.4kHz while data=0

* The default value for each bit is 0.

00D5 Set port 2 bit function. Write only.

* An '1' in this register will set the corresponding pin of port 2 as an output pin.
* The default value for each bit is 0.

00D6 Set port 2 pull-up resistor. Write only.

* An '1' in this register will enable the pull-up resistor of the corresponding pin of port 2. But the pull-up resistor will be disabled if the pin is output low.
* The default value for each bit is 0.

00D7 Set port 2 pull-low resistor. Write only.

* An '1' in this register will enable the pull-low resistor of the corresponding pin of port 2. But the pull-low resistor will be disabled if the pin is output low.
* The default value for each bit is 0.

00D8 Set port 2 bitwise input type function. Write only.

Bit 0 : = 0 set this pin as an inverter type input.

= 1 set this pin as a schmitt type input.

1 : = 0 set this pin as an inverter type input.

= 1 set this pin as a schmitt type input.

2 : = 0 set this pin as an inverter type input.

= 1 set this pin as a schmitt type input.

3 : = 0 set this pin as an inverter type input.

= 1 set this pin as a dimmer type input.

4 : = 0 set this pin as an inverter type input.
= 1 set this pin as a dimmer type input.
5 : = 0 set this pin as an inverter type input.
= 1 set this pin as a schmitt type input.
6 : = 0 set this pin as a schmitt type input.
= 1 set this pin as an inverter type input.
7 : = 0 set this pin as a schmitt type input.
= 1 set this pin as an inverter type input.

* The default value for each bit is 0.

00D9 Port2 bitwise output type function selection. Write only.

Bit [7:0]= 0 set this pin as a buffer type output buffer.
0 : = 1 carrying 37.4kHz while data=1
1 : = 1 carrying 37.4kHz while data=0
2 : = 1 carrying 37.4kHz while data=1
3 : = 1 carrying 37.4kHz while data=0
4 : = 1 carrying 37.4kHz while data=1
5 : = 1 carrying 37.4kHz while data=0
6 : = 1 carrying 37.4kHz while data=1
7 : = 1 carrying 37.4kHz while data=0

* The default value for each bit is 0.

00DA Set port 3 bit function. Write only.

* An '1' in this register will set the corresponding pin of port 3 as an output pin.
* The default value for each bit is 0.

00DB Set port 3 pull-up resistor. Write only.

* An '1' in this register will enable the pull-up resistor of the corresponding pin of port 3. But the pull-up resistor will be disabled if the pin is output low.
* The default value for each bit is 0.

00DC Set port 3 pull-low resistor. Write only.

* An '1' in this register will enable the pull-low resistor of the corresponding pin of port 3. But the pull-low resistor will be disabled if the pin is output low.
* The default value for each bit is 0.

00DD Clear watchdog timer. Write only.
Watchdog timer is about (System_clk/4)/128/256.

00DE IRQ selection. Write only.

Bit 5: =0 : Normal IRQ vector
=1 : 7 level IRQ vectors.
6: =0 : Timer0 INT=IRQ
=1 : Timer0 INT=NMI
7: =0 : Base Timer INT=IRQ
=1 : Base Timer INT=NMI

Note : Please note that do not assign two NMI sources at the same time, otherwise the NMI source can not be identified in software.

00DF Time base control. Write only.

Bit 0: =0 : Disable and reset base timer IRQ.
=1 : Enable base timer IRQ
2-1: If Bit[3]=0
=00 : system_clock/1024(resetable)
=01 : system_clock/4096(resetable)
=10 : system_clock/16384(resetable)
=11 : system_clock/65536(resetable)
If Bit[3]=1
=00 : 128Hz(resetable)
=01 : 32Hz(resetable)
=10 : 8Hz(resetable)
=11 : 2Hz(resetable)
3: =0 : base timer clock = system_clock
=1 : base timer clock=32768Hz

(3) Control register

00E0 To enter standby mode. Write only.

00E1 To enter sleep mode. Write only.
In sleep mode, the main system oscillator will be stopped. So, all function are stopped and only external interrupt can wake up this chip.

00E2

00E3 Bank select register. Write only.

* The default bank value is FF.

00E4 Audio Control register. Write only.

Bit 0 : = 0 Disable DAC1 and DAC2.
= 1 Enable DAC1 and DAC2.
1 : = 0 DAC1 and DAC2 is merged.
= 1 DAC1 and DAC2 is separated.
2 : = 0 Disable PWM.
= 1 Enable PWM
4-3 : If bit[5]=0
= 00 1.70mA(full) at 3v for each DAC
= 01 3.10mA(full) at 3v for each DAC
= 10 2.31mA(full) at 4.5v for each DAC
= 11 4.32mA(full) at 4.5v for each DAC
If bit[5]=1
= 00 1.42mA(full) at 3v for each DAC
= 01 2.66mA(full) at 3v for each DAC
= 10 1.93mA(full) at 4.5v for each DAC
= 11 3.67mA(full) at 4.5v for each DAC
5 : = 0 Current option 0
= 1 Current option 1(less than option_0 15%)
6 : = 0 Normal play function mode
= 1 Green voice mode play
7 : = 0 Normal play function mode
= 1 Output data interpolation

* The default value for each bit is 0.

00E5 Play mode control. Write only.

Bit 0 : = 0 Channel_1 in voice mode.
= 1 Channel_1 in melody mode. Timer 0 output to channel 1 and IRQ0 is disabled.

1 : = 0 Channel_2 in voice mode.
= 1 Channel_2 in melody mode. Timer 1 output to channel 1 and IRQ0 is disabled.
2 : = 0 Channel_3 in voice mode.
= 1 Channel_3 in melody mode. Timer 2 output to channel 1 and IRQ0 is disabled.
3 : = 0 Channel_4 be voice mode.
= 1 Channel_4 be melody mode. Timer 3 output to channel 1 and IRQ0 is disabled.
4 : = 0 Channel_(1,2) and (3,4) is not the same.
= 1 Channel_(1=2) latched by 1 and (3=4) latched by 3
5 : = 0 Channel_(1,2,3) is not the same.
= 1 Channel_(1=2=3) latched by 1
6 : = 0 Channel_(1,3) is not the same.
= 1 Channel_1=3) latched by 1
7 : = 0 Channel_(1,2,3,4) is not the same.
= 1 Channel_(1=2=3=4) latched by 1

* The melody output frequency is the timer IRQ freuency divided by 2.
* The default value for each bit is 0.

00E6 Data for Channel_1. Write only.

00E7 Data for Channel_2. Write only.

00E8 Data for Channel_3. Write only.

00E9 Data for Channel_4. Write only.

00EA Volume control for DAC1. Write only.
Bit 2-0 : Volume of DAC1.
* The default value for each bit is 0.

00EB Volume control for DAC2. Write only.
Bit 2-0 : Volume of DAC2.
* The default value for each bit is 0.

00EC Volume control for PWM channel. Write only.
Bit 2-0 : Volume of PWM channel.
* The default value for each bit is 0.

00ED System clock generator. Write only.

Bit 0: System clock

	RC option	X' tal option
=0	4meg:	Defined by bit 7 & 6
=1	32k	32k

2: =0 No speed up

=1 Speed up by PLL by shorter timer constant in low pass filter.

3: =0 low gain for X' tal.

=1 high gain for X' tal

4: =0 No speed up

=1 Speed up by [5] option

5: =0 For speed up PLL for 5v mode(about 3.9v release).

=1 For speed up PLL for 3v mode(about 1.5v release)

[7:6] : For X' tal option only.

=00 System clock=32768Hz x 128(by PLL)

=01 System clock=32768Hz x 192(by PLL)

=1x System clock=32768Hz x 256(by PLL)

00EE Reset base timer. Write only.

00EF Reserved. Do not use.

(4) Timer definition

00F0 Timer Control register. Write only.

Bit 0 : = 0 Disable timer 0.

= 1 Enable timer 0.

1 : = 0 Disable timer 1.

= 1 Enable timer 1.

2 : = 0 Disable timer 2.

= 1 Enable timer 2.

3 : = 0 Disable timer 3.

= 1 Enable timer 3.

4 : = 0 Disable timer 4.

= 1 Enable timer 4.

5 : = 0

= 1

6 : = 0 Enable WatchDog timer.

= 1 Disable WatchDog timer.

7 : = 0 WatchDog to reset whole chip.

= 1 WatchDog to generate NMI.

* The default value for each bit is 0.

00F1 Timer 0 source clock Control register. Write only.

Bit 0000 : = 0000 Clock source use (system_clock).

= 0001 Clock source use (system_clock/2).

= 0010 Clock source use (system_clock/4).

= 0011 Clock source use (system_clock/8).

= 0100 Clock source use (system_clock/16).

= 0101 Clock source use (system_clock/32).

= 0110 Clock source use (system_clock64).

= 0111 Clock source use (system_clock/128).

= 1000 Clock source use (system_clock/256).

= 1001 Clock source use (system_clock/512).

= 1010 Clock source use (system_clock/1024)(resetable).

= 1011 Clock source use (system_clock/8192)(resetable).

= 1100 Clock source use (system_clock/65536)(resetable).

= 1101 Clock source use (P15).

= 1110 Clock source use (P16).

= 1111 Clock source use (P17).

* The default value is 0010.

00F2 Timer 1 source clock Control register. Write only.

Bit 0000 : = 0000 Clock source use (system_clock).

= 0001 Clock source use (system_clock/2).

= 0010 Clock source use (system_clock/4).

= 0011 Clock source use (system_clock/8).

= 0100 Clock source use (system_clock/16).

= 0101 Clock source use (system_clock/32).

= 0110 Clock source use (system_clock64).

= 0111 Clock source use (system_clock/128).

= 1000 Clock source use (system_clock/256).

= 1001 Clock source use (system_clock/512).
= 1010 Clock source use (system_clock/1024)(resetable).
= 1011 Clock source use (system_clock/8192)(resetable).
= 1100 Clock source use (system_clock/65536)(resetable).
= 1101 Clock source use (P15).
= 1110 Clock source use (P16).
= 1111 Clock source use (P17).

* The default value is 0010.

00F3 Timer 2 source clock Control register. Write only.

Bit 0000 : = 0000 Clock source use (system_clock).
= 0001 Clock source use (system_clock/2).
= 0010 Clock source use (system_clock/4).
= 0011 Clock source use (system_clock/8).
= 0100 Clock source use (system_clock/16).
= 0101 Clock source use (system_clock/32).
= 0110 Clock source use (system_clock64).
= 0111 Clock source use (system_clock/128).
= 1000 Clock source use (system_clock/256).
= 1001 Clock source use (system_clock/512).
= 1010 Clock source use (system_clock/1024)(resetable).
= 1011 Clock source use (system_clock/8192)(resetable).
= 1100 Clock source use (system_clock/65536)(resetable).
= 1101 Clock source use (P15).
= 1110 Clock source use (P16).
= 1111 Clock source use (P17).

* The default value is 0010.

00F4 Timer 3 source clock Control register. Write only.

Bit 0000 : = 0000 Clock source use (system_clock).
= 0001 Clock source use (system_clock/2).
= 0010 Clock source use (system_clock/4).
= 0011 Clock source use (system_clock/8).
= 0100 Clock source use (system_clock/16).
= 0101 Clock source use (system_clock/32).
= 0110 Clock source use (system_clock64).

= 0111 Clock source use (system_clock/128).
= 1000 Clock source use (system_clock/256).
= 1001 Clock source use (system_clock/512).
= 1010 Clock source use (system_clock/1024)(resetable).
= 1011 Clock source use (system_clock/8192)(resetable).
= 1100 Clock source use (system_clock/65536)(resetable).
= 1101 Clock source use (P15).
= 1110 Clock source use (P16).
= 1111 Clock source use (P17).

* The default value is 0010.

00F5 Timer 4 source clock Control register. Write only.

Bit 0000 : = 0000 Clock source use (system_clock).
= 0001 Clock source use (system_clock/2).
= 0010 Clock source use (system_clock/4).
= 0011 Clock source use (system_clock/8).
= 0100 Clock source use (system_clock/16).
= 0101 Clock source use (system_clock/32).
= 0110 Clock source use (system_clock64).
= 0111 Clock source use (system_clock/128).
= 1000 Clock source use (system_clock/256).
= 1001 Clock source use (system_clock/512).
= 1010 Clock source use (system_clock/1024)(resetable).
= 1011 Clock source use (system_clock/8192)(resetable).
= 1100 Clock source use (system_clock/65536)(resetable).
= 1101 Clock source use (P15).
= 1110 Clock source use (P16).
= 1111 Clock source use (P17).

* The default value is 1001.

00F6 Timer 0 data. Write only.

* After timer 0 been enabled, the timer will start to count down. When timer counts to 0, the timer will count from the initial value and IRQ0

will happen.

* This timer data is used with $00F7. Total is 12 bits
* Valid values($00F7,$00F6)/ are from 1 to 4095. 0 is prohibited.

* Timer 1 input clock is ($00F1).
* The time elapse = ($00F7,$00F6) / ($00F1)

00F7 Timer 0 higher nibble data. Write only.

00F8 Timer 1 data. Write only.

* After timer 1 been enabled, the timer will start to count down. When timer counts to 1, the timer will count from the initial value and IRQ1 will happen.
* This timer data is used with $00F9. Total is 12 bits
* Valid values($00F9,$00F8)/ are from 1 to 4095. 0 is prohibited.
* Timer 1 input clock is ($00F2).
* The time elapse = ($00F9,$00F8) / ($00F2)

00F9 Timer 1 higher nibble data. Write only.

00FA Timer 2 data. Write only.

* After timer 2 been enabled, the timer will start to count down. When timer counts to 0, the timer will count from the initial value and IRQ2 will happen.
* This timer data is used with $00FB. Total is 12 bits
* Valid values($00FB,$00FA)/ are from 1 to 4095. 0 is prohibited.
* Timer 1 input clock is ($00F3).
* The time elapse = ($00FB,$00FA) / ($00F3)

00FB Timer 2 higher nibble data. Write only.

00FC Timer 3 data. Write only.

* After timer 3 been enabled, the timer will start to count down. When timer counts to 0, the timer will count from the initial value and IRQ3 will happen.
* This timer data is used with $00FD. Total is 12 bits
* Valid values($00FD,$00FC)/ are from 1 to 4095. 0 is prohibited.

* Timer 1 input clock is ($00F4).
* The time elapse = ($00FD,$00FC) / ($00F4)

00FD Timer 3 higher nibble data. Write only.

00FE Timer 4 data. Read and Write.

Read:

If timer_4 is disabled, read low 8 bit counter data.

Write:

* After timer 4 been enabled, the timer will start to count down. When timer counts to 0, the timer will count from the initial value and IRQ4 will happen.
* This timer data is used with $00FF. Total is 12 bits
* Valid values($00FF,$00FE)/ are from 1 to 4095. 0 is prohibited.
* Timer 1 input clock is ($00F5).
* The time elapse = ($00FF,$00FE) / ($00F5)

00FF Timer 4 higher nibble data. Read and Write.

Read:

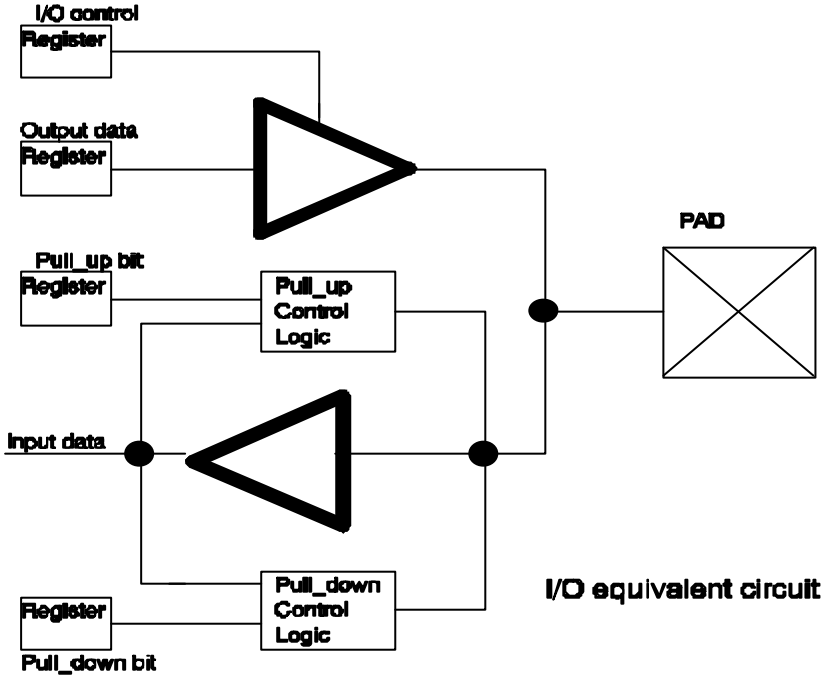
If timer_4 is disabled, read high 4 bit counter data.

5. DETALIS

(1) Base timer clock source(sys_clk/1024, sys_clk/4096, sys_clk/16384, sys_clk/65536) and Timer clock source(sys_clk/1024, sys_clk/8192) is resetable by ($00EE).

(2) Once External INT flag is cleared. Both Falling and Rising edge INT flag are Cleared.

(3)



(4) If INT_0 or INT_5 is optioned to NMI, we also can see these flags from ($00C0).

(5) For system clock changing: 4MHz to 32kHz or 32kHz to 4Mhz. After changed, needing 3 more clocks be pseudo clock.

(6) If channel(1,2,3,4) be melody mode, INT(0,1,2,3) will be tone generator.

(7) Timer data must write high nibble then low byte. If low byte first, the high nibble will be included after counting down to 0 then reload high nibble and low byte.

(8) DAC1 and DAC2 volume control is separated, even in merged(DAC1+DAC2) mode.

(9) Play mode control:

This can implement voice or melody mode for each channel. More than this, for weighting concerned, this chip can defined to (1+1+1+1) ,(1+1+2),(2+2),(1+3) channels. Channel_(1,2) derive to DAC1; channel_(3,4) derive to DAC2.

Channel_(1,2,3,4) derives to PWM port.

a. (1+1+1+1)

channel_1 can be melody or voice mode.
channel_2 can be melody or voice mode.
channel_3 can be melody or voice mode.
channel_4 can be melody or voice mode.

b. (1+1+2)

channel_1=channel_3 can be melody or voice mode.
(channel data and tone generator is assigned by channel_1,both channels' data and tone will be the same.)
channel_2 can be melody or voice mode.
channel_4 can be melody or voice mode.

c. (1+3)

channel_1=channel_2=channel_3 can be melody or voice mode.
(channel data and tone generator is assigned by channel_1,both channels' data and tone will be the same.)
channel_4 can be melody or voice mode.

d. (2+2)

channel_1=channel_2 can be melody or voice mode.
channel_3=channel_4 can be melody or voice mode.
(channel data and tone generator is assigned by channel_1,both channels' data and tone will be the same.)

(10) Ramp function implement

a. DAC note:

For DAC' s DC offset is 00H(for 8 bit). If the voice or melody data play is start from 80H. We need make a ram_up data to inhibit noise "pop".

And melody function is ramped up by 00H ~ 7FH. The others (80H~ FFH)
for envelope generation.(FFH is maximum amplitude. 80H is minimum amplitude).

b. PWM note:

For PWM' s DC offset is 80H(for 8 bit). If the voice or melody data play is start from 80H. We needn' t make a ram_up data to inhibit noise "pop".

If melody function is ramped up by 00H ~ 7FH, a noise will be existed. The others (80H~ FFH) for envelope generation.(FFH is maximum amplitude. 80H is minimum amplitude).

(11) 7 level IRQ:

This chip we have 7 IRQs. If we set to 7 level IRQ not only one IRQ, the hardware will take care the priority of these 7 interrupts.

The priority is:

INT6 > INT5 > INT4 > INT3 > INT2 > INT1 > INT0

Base_timer > External_int > Timer_4 > Timer_3 > Timer_2 > Timer_1 > Timer_0

6. ABSOLUTE MAXIMUM RATINGS

Operating temperature ..... 0 to 70 ℃
Storage temperature ..... -65 to 150 ℃
Supply voltage ..... 7 V
Input voltage ..... -0.6 to Vdd+0.6 V

7. ELECTRICAL CHARACTERISTIC :

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Supply Voltage	Vdd		2.5	3.0	3.5	V
RC oscillation frequency	∅sys	Vdd=2.7V	400		800	Khz
Operating current	Idd	Vdd=3V,∅sys=4Mhz		1.5		mA
Standby current	Istdby	Vdd=3V,∅sys=4Mhz		1		mA
Sleep mode current	Islp	Vdd=3V			1	μA
Input high voltage	Vih	Vdd=3.0V	2.0			V
Input low voltage	Vil	Vdd=3.0V	-0.6		0.8	V
Input high leakage current	Iih	Vih=Vdd			1	μA
Input low leakage current	Iil	Vil=0			-5	μA
Output high voltage	Voh	Ioh=-2mA	Vdd-0.4		Vdd	V
Output low voltage	Vol	Iol=4mA	0		0.4	V
Output high voltage (PWM1, PWM2)	Voh	Vdd=3V, Ioh=-60mA	Vdd-1		Vdd	V
Output low voltage (PWM1, PWM2)	Vol	Vdd=3V, Iol=75mA	0		1	V
AUD (D/A full scale)	Io	Vdd=3V, Rl=100 OHM		-4.0		mA

Customer Information Sheet

1. Customer's Name : _____

2. Project title : _____

3. Syntek part number : _____ (will be filled by Syntek)

4. Package --------- ( ) Chip ( ) PQFP

5. Others :

Customer : _____ Date : __/__/__

Salesman : _____ Date : __/__/__