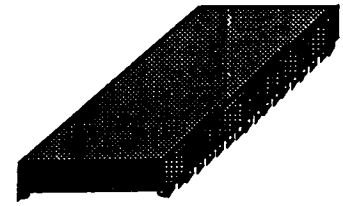
262,144-WORD by 4-BIT HIGH SPEED CMOS SYNCHRONOUS STATIC RAM **PRELIMINARY**

Description

The CXK77410J is a high speed CMOS synchronous static RAM with separate I/O pins, organized as 262,144-words by 4-bits. This synchronous SRAM integrates input registers, high speed SRAM and output registers onto a single monolithic IC. All input signals are latched at the positive edge of an external clock (CLK). The RAM data from the previous cycle is presented at the positive edge of the subsequent clock cycle. Write operation is initiated by the positive edge of CLK and is internally self-timed. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals. Pass-thru capability is also provided. 100MHz operation is obtained from a single 5V power supply.

CXK77410J
36 PIN SOJ (Plastic)

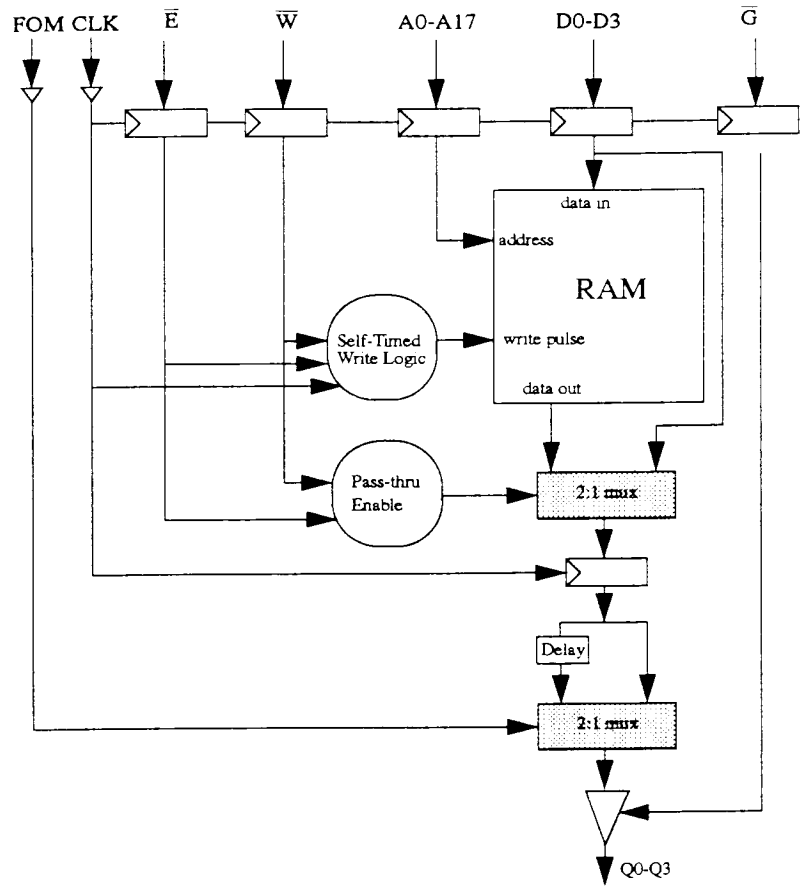


Structure
Silicon gate CMOS IC

Features

- High speed, low power consumption.
- Single +5V power supply : 5V ± 5%
- Inputs and outputs are TTL compatible.
- Write-through capability.
- Separate data input and output.
- 10 ns cycle time (100 MHz).
- All inputs and outputs are registered on a single clock edge.
- Self-timed write cycle.
- Arbitrary consecutive read/write cycles with no write recovery cycles.
- Available in a 36 pin 50 mil lead pitch 400 mil SOJ package.

FUNCTIONAL BLOCK DIAGRAM



FUNTIONAL DESCRIPTION

There are three possible user capabilities with this chip : Read operation, Write operation, and Pass-through operation.

The read operation requires $\overline{W}$ = "HIGH" at the rising edge of CLK. The memory location specified by the address inputs is latched and read internally. At the subsequent rising edge of CLK, if $\overline{G}$ = "LOW", the contents of the previous cycle are captured by the Data-out registers. The state of the output terminals reflect the contents of the Data-out registers.

The write and pass-through operations require $\overline{W}$ and $\overline{E}$ to be "LOW" at the rising edge of CLK. The contents of the Data-in registers are written into the memory locations specified by the address inputs. The write operation is entirely self-timed. The contents of the Data-in registers are also captured by the Data-out registers when $\overline{G}$ goes "LOW" at the subsequent rising edge of CLK and are also passed to the output terminals for write through operation.

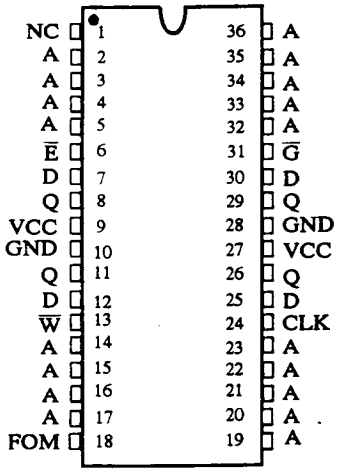
The pass through operation requires $\overline{W}$ = "LOW" and $\overline{E}$ = "HIGH" at the rising edge of CLK. The data is not written to memory, however the contents of Data-in registers are captured by the Data-out registers when $\overline{G}$ = "LOW" at the subsequent rising edge of CLK. It is also presented to the output terminals.

Wait states are not required between read and write cycles.

The FOM pin is used to control output timing, allowing the user to skew CLK to output and hold times.

Pin Configuration

(Top View)



Pin Description

Symbol	Description
A0 to A17	Address input
D0 to D3	Data input
Q0 to Q3	Data output
CLK	Clock
$\overline{E}$	Internal write enable input
$\overline{W}$	Write enable input
$\overline{G}$	Output enable input
FOM	Fast Output Mode option pin
Vcc	+5V power supply
GND	Ground

Pin Description

CLK (Clock, positive edge triggered)

All timing is controlled by the rising or positive edge of CLK. All synchronous input and output signals are registered on the rising edge of CLK with set-up and hold times referenced to that edge. Since only one edge of CLK is referenced, the duty cycle of CLK is not critical.

A0 to A17 (Address)

The Address inputs are decoded on-chip to select one of 262,144 words. The state of the Address inputs is registered into the Address register on the positive edge of CLK. The Address inputs must be valid during every positive edge with all set-up and hold times referenced to that edge.

D0 to D3 (Data input)

The state of the Data inputs is registered into the Data-in registers on the positive edge of CLK for the write operation. The data inputs must be valid during every positive edge with all set-up and hold times referenced to that edge.

Q0 to Q3 (Data input)

Output terminals are three-state. The state is defined by the Control block(refer the truth table). The Data outputs are triggered by the edge of CLK and the contents of the Output-Registers are presented.

$\overline{W}$ (Synchronous Write Enable, active low)

$\overline{W}$ is used to indicate whether a read or write operation is to be performed. $\overline{W}$ is "LOW" to perform a write operation. $\overline{W}$ is registered on every positive edge of CLK with set-up and hold times referenced to that edge. The internal timing required to store data into the memory array is self-timed.

$\overline{E}$ (Synchronous Internal Write Enable, active low)

$\overline{E}$ is used to control the write operation along with $\overline{W}$(refer the truth table). The state of $\overline{E}$ is registered on every positive edge of CLK with set-up and hold times referenced to that edge.

$\overline{G}$ (Synchronous Output Enable, active low)

$\overline{G}$ is used to control output registers and enable the output terminals. When $\overline{G}$ is "LOW", the data from the previous cycle will be captured into the output registers and also presented to the output terminals. When $\overline{G}$ is "HIGH", output registers will contain tri-stated information and the output terminals are tri-stated.The state of G is registered on every positive edge of CLK with set-up and hold times referenced to that edge.

FOM (Fast Output Mode, active high)

FOM is an option pin, which controls clock to output timing. When FOM is tied high, a built-in delay circuit is bypassed, allowing a faster output access time. Conversely, when FOM is tied low, the output data is routed through the delay circuit, giving better output hold time. FOM, if left unconnected (floating), defaults to an active high. This is accomplished by an internal pull-up device strobed by CLK and a unidirectional latch.

Absolute Maximum Ratings (T_a = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	-0.5 to +7.0	V
Input voltage	V_{IN}	-0.5* to V_{CC} + 0.5	V
Output voltage	V_O	-0.5 to V_{CC} + 0.5	V
Allowable power dissipation	P_D	1.0	W
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	-55 to 150	°C
Soldering temperature • time	T_{solder}	260 • 10	°C • sec

Truth Table

$\overline{E}(t_n)$	$\overline{W}(t_n)$	$\overline{G}(t_{n+1})$	Mode	$D_{0\text{-}3}(t_n)$	$Q_{0\text{-}3}(t_{n+1})$	V_{CC} Current
L	L	L	Write and Pass-thru	Valid	$D_{0\text{-}3}(t_n)$	I_{CC}
		H	Write	Valid	Hi - Z	I_{CC}
L	H	L	Read	Don't care	$D_{OUT}(t_n)$	I_{CC}
		H	Aborted read	Don't care	Hi - Z	I_{CC}
H	L	L	Pass-thru	Valid	$D_{0\text{-}3}(t_n)$	I_{CC}
		H	Aborted pass-thru	Valid	Hi - Z	I_{CC}
H	H	L	Read	Don't care	$D_{OUT}(t_n)$	I_{CC}
		H	Aborted read	Don't care	Hi - Z	I_{CC}

DC Recommended Operating Conditions (T_a = 25°C, GND =0V)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Input high voltage	V_{IH}	2.2	---	V_{CC} + 0.3	V
Input low voltage	V_{IL}	-0.3*	---	0.8	V

*V_{IL} = -3.0 V Min. for pulse width less than 20 ns.

Electrical Characteristics

•DC and operating characteristics

(Vcc = 5V± 5%, GND = 0V, T_a = 0 to 70°C)

Item	Symbol	Test conditions	Min	Typ*	Max	Unit
Input leakage current except pin 18	I_{LI}	Vin = GND to Vcc	-1	---	1	uA
Input leakage current Pin 18	$I_{LI,18}$	Vin = GND to Vcc, $V_{CLK}=V_{IH}$	-2000	---	1	uA
		Vin = GND to Vcc, $V_{CLK}=V_{IL}$	-1	---	1	uA
Output leakage current	I_{LO}	V_O = GND to Vcc $\overline{G} = V_{IH}$	-1	---	1	uA
Operating power supply current	I_{CC}	Cycle = 66.7 MHz Vin = V_{IH} or V_{IL}	---	---	170	mA
		Cycle = 80 MHz	---	---	190	mA
		Cycle = 100 MHz	---	---	200	mA
Output high voltage	V_{OH}	I_{OH} = -4.0 mA	2.4	---	---	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	---	---	0.4	V

* Vcc = 5V, T_a = 25°C

•I/O capacitance

(T_a = 25°C, f = 1 MHz)

Item	Symbol	Test conditions	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	---	5	pF
Output capacitance	C_{OUT}	V_{OUT} = 0V	---	8	pF
Clock input capacitance	C_{CLK}	V_{CLK} = 0V	---	8	pF

Note: These parameters are sampled and are not 100% tested.

•AC ELECTRICAL CHARACTERISTICS

	Item	Symbol	-10 (100 MHZ)		-12 (80 MHZ)		-15 (66.7 MHz)		Unit
			Min	Max	Min	Max	Min	Max	
	Clock period	t_{CP}	10	∞	12.5	∞	15	∞	ns
	Clock pulse high	t_{CH}	3	---	4	---	5	---	ns
	Clock pulse low	t_{CL}	3	---	4	---	5	---	ns
	Setup time	t_S	2	---	2	---	2.5	---	ns
	Hold time	t_H	1	---	1	---	1.5	---	ns
FOM = V_{IL}	Clock to output	t_{CQ}	2	6.5	2	7	2	8.5	ns
	Clock to output high impedance	t_{HZ}*2	2	5	2	6	2	7.5	ns
	Clock to output low impedance	t_{LZ}*2	2	---	2	---	2	---	ns
FOM = V_{IH}	Clock to output	t_{CQ}	1	5.5	1	6	1	7.5	ns
	Clock to output high impedance	t_{HZ}*2	1	4.5	1	5	1	6.5	ns
	Clock to output low impedance	t_{LZ}*2	1	---	1	---	1	---	ns

1. All parameters are specified over the range 0-70°C.
2. These parameters are sampled and are not 100% tested.

AC characteristics

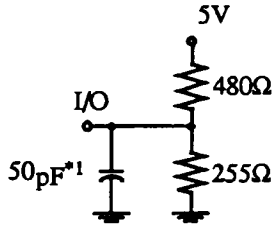
• AC test conditions

(Vcc = 5V ±5%, Ta = 0 to 70°C)

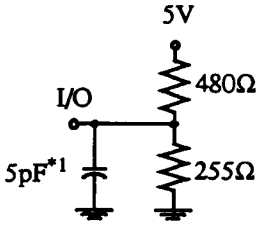
Item	Conditions
Input pulse high level	V_{IH} = 3.0V
Input pulse low level	V_{OL} = 0V
Input rise time	t_r = 3 ns
Input fall time	t_f = 3 ns
Input reference level	1.5V
Output reference level	0.8 V/2.0 V
Output load conditions	Fig.1

FIG.1

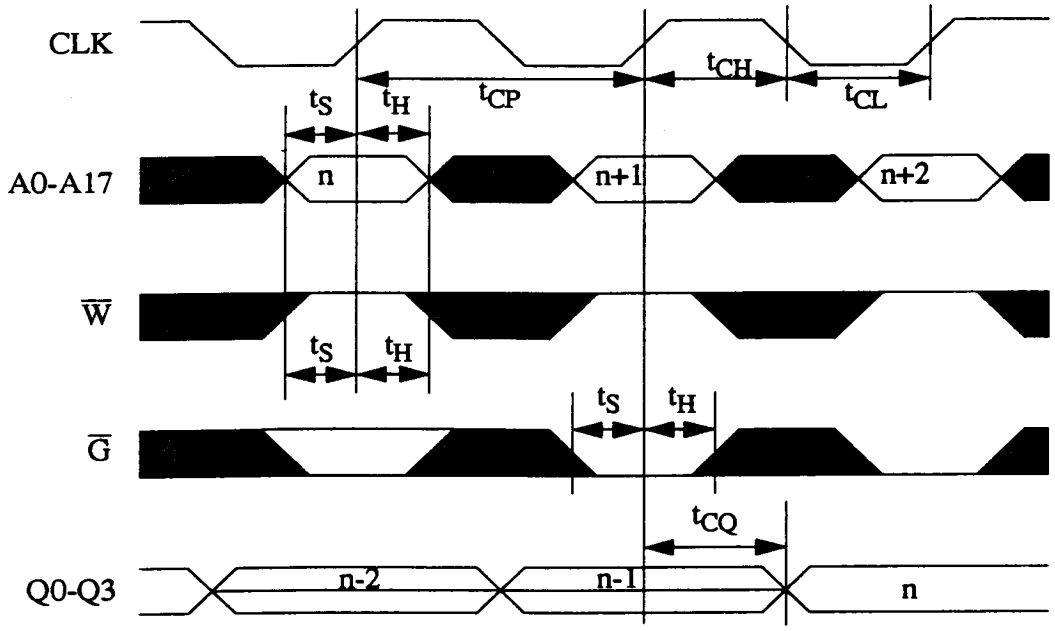
Output Load (1)



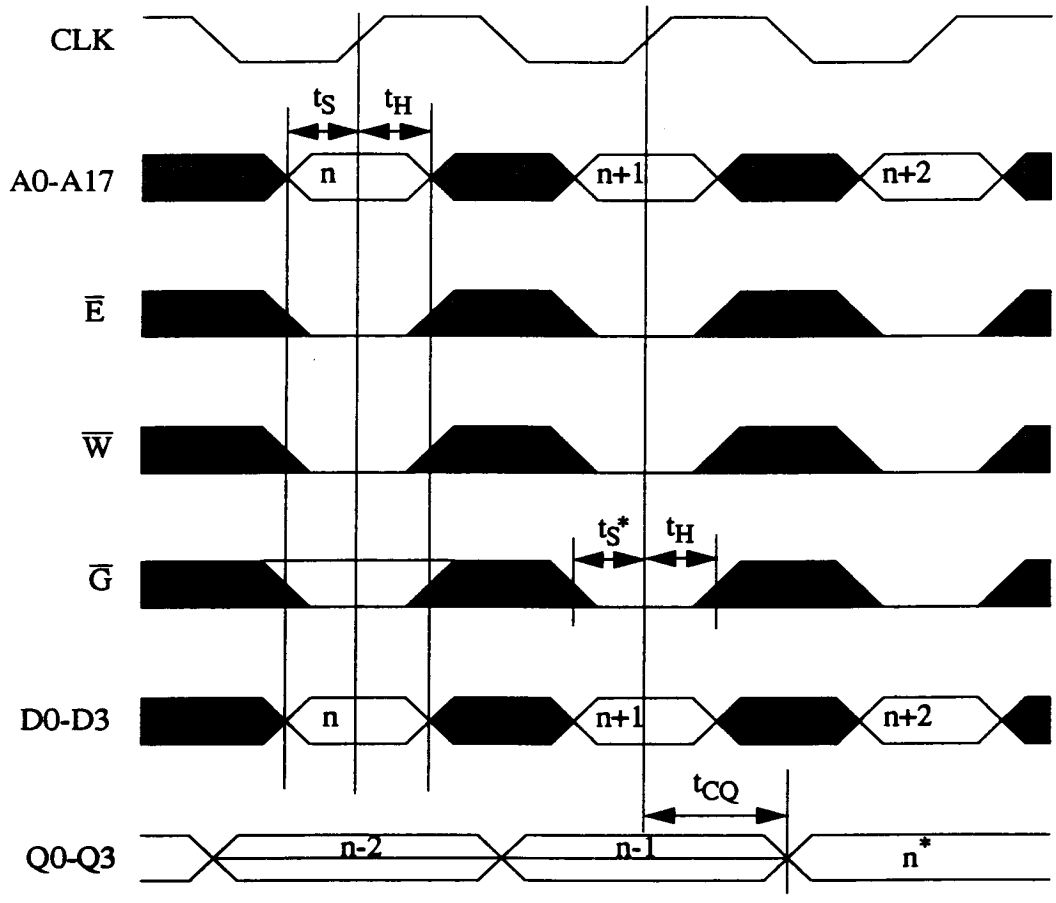
Output Load*2 (2)



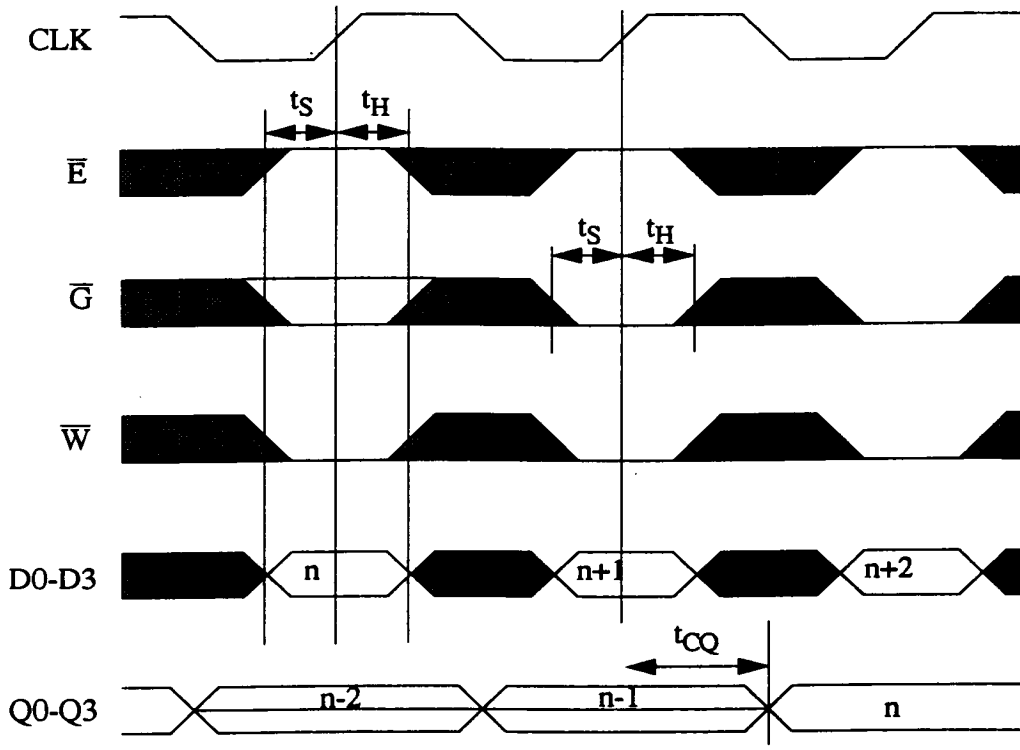
1. Including scope and jig capacitance.
2. For t_{LZ}, t_{HZ}.



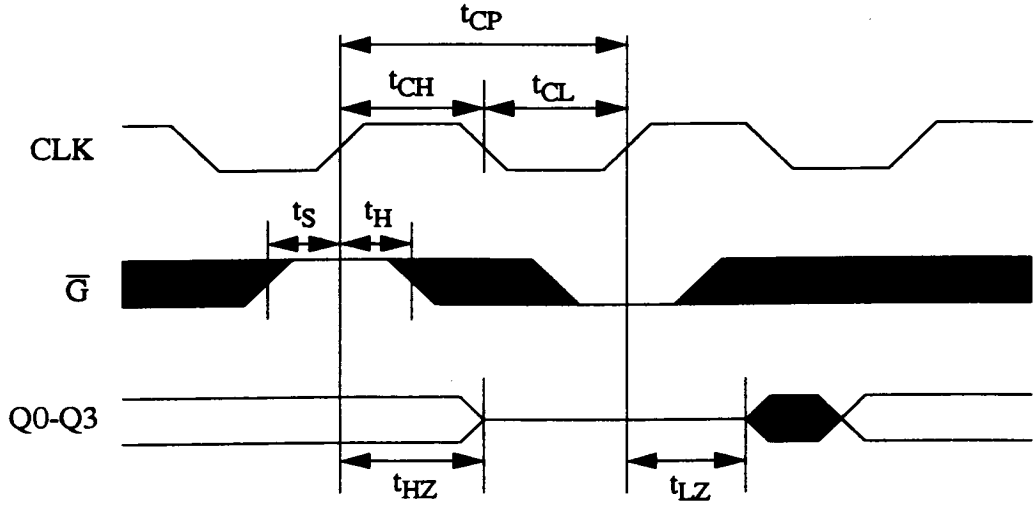
TIMING WAVEFORM OF READ CYCLE ($\overline{E}$ Don't care)



TIMING WAVEFORM OF WRITE CYCLE (* pass-thru option)



TIMING WAVEFORM OF PASS THROUGH CYCLE



TIMING WAVEFORM OF TRI-STATE OUTPUTS