

CYPRESS
SEMICONDUCTOR

T-46-23-08 CY7C170A

4096 x 4 Static R/W RAM

Features

- CMOS for optimum speed/power
- High speed
 - $t_{AA} = 15 \text{ ns}$
 - $t_{ACS} = 10 \text{ ns}$
- Low active power
 - 495 mW (commercial)
 - 660 mW (military)
- TTL-compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge
- Output enable
- V_{IH} of 2.2V

Functional Description

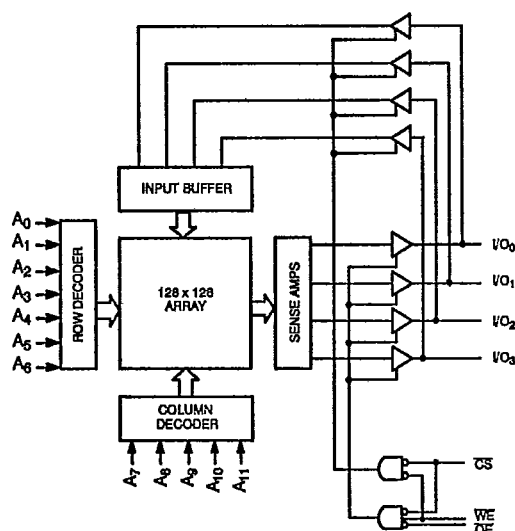
The CY7C170A is a high-performance CMOS static RAM organized as 4096 words by 4 bits. Easy memory expansion is provided by an active LOW chip select (CS), an active LOW output enable (OE) and three-state drivers.

Writing to the device is accomplished when the chip select (CS) and write enable (WE) inputs are both LOW. Data on the four input/output pins (I/O₀ through I/O₃) is written into the memory location specified on the address pins (A₀ through A₁₁).

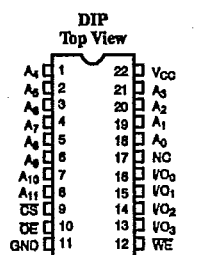
Reading the device is accomplished by taking chip select (CS) and output enable (OE) LOW, while write enable (WE) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the four data I/O pins.

The I/O pins stay in high-impedance state when chip select (CS) or output enable (OE) is HIGH, or write enable (WE) is LOW.

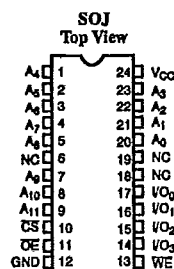
A die coat is used to insure alpha immunity.

Logic Block Diagram

C170A-1

Pin Configurations

C170A-2



C170A-3

Selection Guide

		7C170A-15	7C170A-20	7C170A-25	7C170A-35	7C170A-45
Maximum Access Time (ns)		15	20	25	35	45
Maximum Operating Current (mA)	Commercial	115	90	90	90	90
	Military		120	120	120	120

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	- 65°C to +150°C
Ambient Temperature with Power Applied	- 55°C to +125°C
Supply Voltage to Ground Potential (Pin 22 to Pin 21)	- 0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	- 0.5V to +7.0V
DC Input Voltage	- 3.0V to +7.0V
Output Current into Outputs (Low)	20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-up Current >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Military ^[1]	- 55°C to +125°C	5V ± 10%



SRAMs

Electrical Characteristics Over the Operating Range^[2]

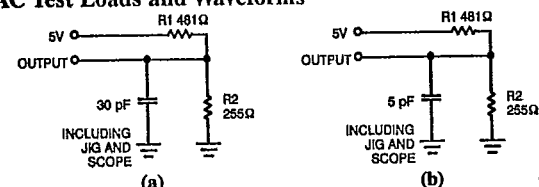
Parameters	Description	Test Conditions	7C170A-15		7C170A-20, 25, 35, 45		Units
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage		-3.0	0.8	-3.0	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	+10	-10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-10	+10	-10	+10	μA
I _{OS}	Output Short Circuit Current ^[3]	V _{CC} = Max., V _{OUT} = GND		-350		-350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA	Com'l	115		90	mA
			Mil			120	mA

Capacitance^[4]

Parameters	Description	Test Conditions	Max.	Units
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

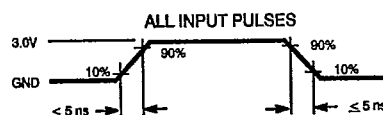
Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

Equivalent to:
THEVENIN EQUIVALENT
OUTPUT — 167Ω — 1.73V

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C170A-5



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CY7C170A

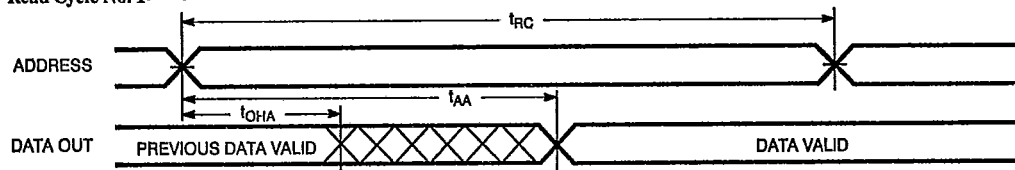
Switching Characteristics Over the Operating Range^[1, 5]

Parameters	Description	7C170A-15		7C170A-20		7C170A-25		7C170A-35		7C170A-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t _{RC}	Read Cycle Time	15		20		25		35		45		ns
t _{AA}	Address to Data Valid		15		20		25		35		45	ns
t _{OHA}	Data Hold from AddressChange	5		5		5		5		5		ns
t _{ACS}	$\overline{CS}$ LOW to Data Valid		10		15		15		25		30	ns
t _{DOE}	$\overline{OE}$ LOW to Data Valid		10		10		12		15		20	ns
t _{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		3		3		ns
t _{HZOE}	$\overline{OE}$ HIGH to High Z ^[6]		8		8		10		12		15	ns
t _{LZCS}	$\overline{CS}$ LOW to Low Z ^[7]	5		5		5		5		5		ns
t _{HZCS}	$\overline{CS}$ HIGH to High Z ^[6, 7]		8		8		10		15		15	ns
WRITE CYCLE ^[8]												
t _{WC}	Write Cycle Time	15		20		20		25		40		ns
t _{SCS}	$\overline{CS}$ LOW to Write End	12		15		20		25		30		ns
t _{AW}	Address Set-Up to Write End	12		15		20		25		30		ns
t _{HA}	Address Hold from Write End	0		0		0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t _{PWE}	$\overline{WE}$ Pulse Width	12		15		15		20		20		ns
t _{SD}	Data Set-Up to Write End	10		10		10		15		15		ns
t _{HD}	Data Hold from Write End	0		0		0		0		0		ns
t _{HZWE}	$\overline{WE}$ HIGH to High Z		7		7		7		10		15	ns
t _{LZWE}	$\overline{WE}$ HIGH to Low Z	5		5		5		5		5		ns

Notes:

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OH}/I_{OL} and 30-pF load capacitance.
- t_{HZCE} and t_{HZWE} are tested with $C_L = 5\text{pF}$ as in part (b) of AC Test Loads. Transition is measured $\pm 500\text{mV}$ from steady state voltage.
- At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are sampled and not 100% tested.
- The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- $\overline{WE}$ is HIGH for read cycle.
- Device is continuously selected, $\overline{CS} = V_{IL}$ and $\overline{OE} = V_{IL}$.
- Data I/O will be high-impedance if $\overline{OE} = V_{IH}$.
- Address valid prior to or coincident with $\overline{CS}$ transition LOW.
- If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms

Read Cycle No. 1^[9, 10]

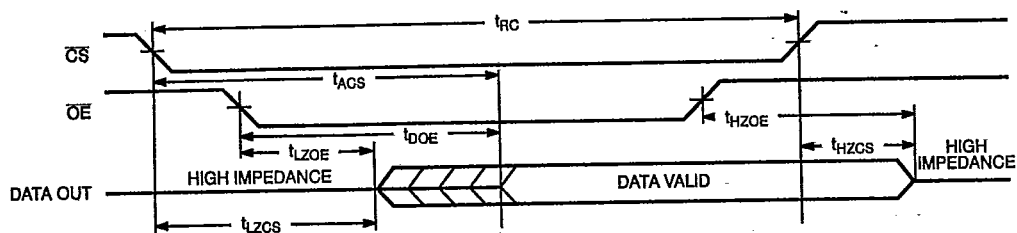
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CY7C170A

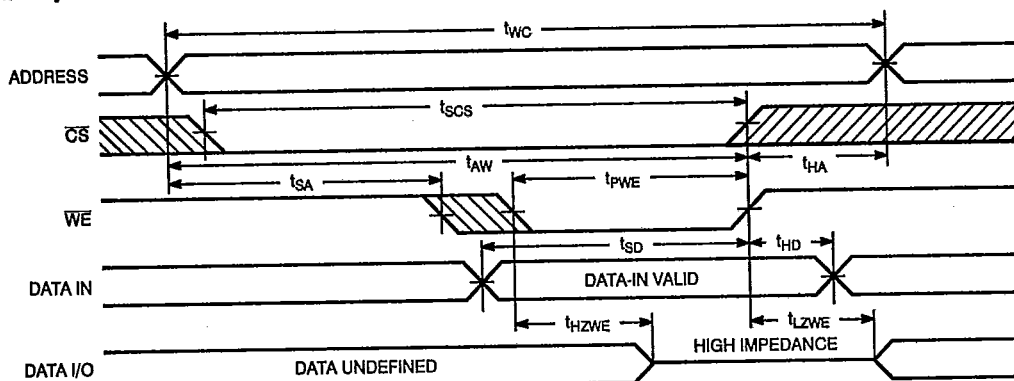
Switching Waveforms (continued)

Read Cycle No. 2^[9, 11]

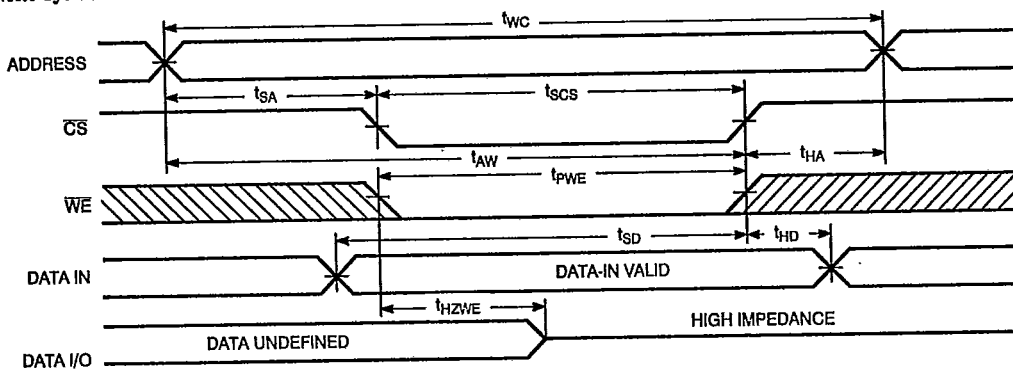
C170A-7

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SRAMS

Write Cycle No. 1^[8, 12]

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Write Cycle No. 2^[8, 12, 13]

C170A-9



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CY7C170A

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7C170A-15PC	P9	Commercial
	CY7C170A-15DC	D10	
	CY7C170A-15VC	V13	
20	CY7C170A-20PC	P9	Commercial
	CY7C170A-20DC	D10	
	CY7C170A-20VC	V13	
	CY7C170A-20DMB	D10	Military
	CY7C170A-20KMB	K73	
25	CY7C170A-25PC	P9	Commercial
	CY7C170A-25DC	D10	
	CY7C170A-25VC	V13	
	CY7C170A-25DMB	D10	Military
	CY7C170A-25KMB	K73	
35	CY7C170A-35PC	P9	Commercial
	CY7C170A-35DC	D10	
	CY7C170A-35VC	V13	
	CY7C170A-35DMB	D10	Military
	CY7C170A-35KMB	K73	
45	CY7C170A-45PC	P9	Commercial
	CY7C170A-45DC	D10	
	CY7C170A-45VC	V13	
	CY7C170A-45DMB	D10	Military
	CY7C170A-45KMB	K73	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL} Max.	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t _{RC}	7, 8, 9, 10, 11
t _{AA}	7, 8, 9, 10, 11
t _{OHA}	7, 8, 9, 10, 11
t _{ACS}	7, 8, 9, 10, 11
t _{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t _{WC}	7, 8, 9, 10, 11
t _{SCS}	7, 8, 9, 10, 11
t _{AW}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{SA}	7, 8, 9, 10, 11
t _{PWE}	7, 8, 9, 10, 11
t _{SD}	7, 8, 9, 10, 11
t _{HD}	7, 8, 9, 10, 11

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