DM2200 EDRAM
4Mb x 1 Enhanced Dynamic RAM

Product Specification

Features

- 2Kbit SRAM Cache Memory for 15ns Random Reads Within a Page
- Interleave SRAM Cache for 8ns Burst Read
- Fast 4Mbit DRAM Array for 35ns Access to Any New Page
- Write Posting Register for 15ns Random Writes and Burst Writes Within a Page (Hit or Miss)
- 256-byte Wide DRAM to SRAM Bus for 7.3 Gigabytes/Sec Cache Fill
- On-chip Cache Hit/Miss Comparators Maintains Cache Coherency on Writes
- Hidden Precharge and Refresh Cycles
- Extended 64ms Refresh Period for Low Standby Power
- Standard CMOS/TTL Compatible I/O Levels and +5 Volt Supply
- 300 Mil Plastic SOJ Package

Description

The Ramtron 4Mb enhanced DRAM (EDRAM) combines raw speed with innovative architecture to offer the optimum cost-performance solution for high performance local or system main memory. In most high speed applications, no-wait-state performance can be achieved without secondary SRAM cache and without interleaving main memory banks at system clock speeds of greater than 66MHz. The EDRAM outperforms conventional SRAM cache plus DRAM memory systems by minimizing processor wait states for all possible bus events, not just cache hits. The combination of input data and address latching, 2K of fast on-chip SRAM cache, and simplified on-chip cache control allows system level flexibility, performance, and overall memory cost reduction not available with any other high density memory component. Architectural similarity with JEDEC DRAMs allows a single memory controller design to support either slow JEDEC DRAMs or high speed EDRAMs. A system designed in this manner can provide a simple upgrade path to higher system performance.

Architecture

The EDRAM architecture has a simple integrated SRAM cache which allows it to operate much like a page mode or static column DRAM.

The EDRAM's SRAM cache is integrated into the DRAM array as tightly coupled row registers. Memory reads always occur from the cache row register. When the internal comparator detects a page hit, only the SRAM is accessed and data is available in 15ns from column address. When a page read miss is detected, the new DRAM row is loaded into the cache and data is available at the output all within 35ns from row enable. Subsequent reads within the page (burst reads or random reads) can continue at 15ns cycle time. Since reads occur from the SRAM cache, the DRAM precharge can occur simultaneously without degrading performance. The on-chip refresh counter with independent refresh bus allows the EDRAM to be refreshed during cache reads.

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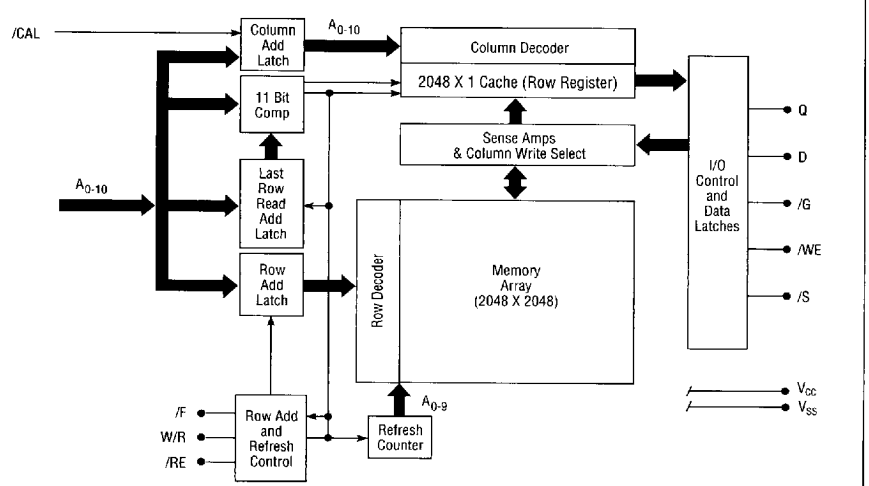
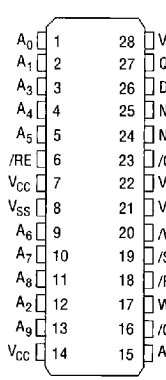
Functional Diagram



Pin Configuration



Memory writes are internally posted in 15ns and directed to the DRAM array. During a write hit, the on-chip address comparator activates a parallel write path to the SRAM cache to maintain coherency. The EDRAM delivers 15ns cycle page mode memory writes. Memory writes do not affect the contents of the cache row register except during a cache hit.

By integrating the SRAM cache as row registers in the DRAM array and keeping the on-chip control simple, the EDRAM is able to provide superior performance without any significant increase in die size over standard slow 4Mb DRAMs. By eliminating the need for SRAMs and cache controllers, system cost, board space, and power can all be reduced.

Functional Description

The EDRAM is designed to provide optimum memory performance with high speed microprocessors. As a result, it is possible to perform simultaneous operations to the DRAM and SRAM cache sections of the EDRAM. This feature allows the EDRAM to hide precharge and refresh operation during SRAM cache reads and maximize SRAM cache hit rate by maintaining valid cache contents during write operations even if data is written to another memory page. These new functions, in conjunction with the faster basic DRAM and cache speeds of the EDRAM, minimize processor wait states.

EDRAM Basic Operating Modes

The EDRAM operating modes are specified in the table below.

Hit and Miss Terminology

In this datasheet, "hit" and "miss" always refer to a hit or miss to the page of data contained in the SRAM cache row register. This is always equal to the contents of the last row that was read from (as modified by any write hit data). Writing to a new page does not cause the cache to be modified.

DRAM Read Hit

If a DRAM read request is initiated by clocking /RE with W/R low and /F and /CAL high, the EDRAM will compare the new row address to the last row read address latch (LRR; an 11-bit latch loaded on each /RE active read cycle). If the row address matches the LRR, the requested data is already in the SRAM cache and no DRAM memory reference is initiated. The data specified by the column address is available at the output pins at the greater of times t_{AC} or t_{GQV}. Since no DRAM activity is initiated, /RE can be brought high after time t_{RE1}, and a shorter precharge time, t_{RP1}, is required. It is possible to access additional SRAM cache locations by providing new column addresses to the multiplex address inputs. New data is available at the output at time t_{AC} after each column address changes. During read cycles, it is possible to operate in either static column mode with /CAL=high or page mode with /CAL clocked to latch the column address.

DRAM Read Miss

If a DRAM read request is initiated by clocking /RE with W/R low and /F and /CAL high, the EDRAM will compare the new row address to the LRR address latch (an 11-bit latch loaded on each /RE active read cycle). If the row address does not match the LRR, the requested data is not in SRAM cache and a new row must be fetched from the DRAM. The EDRAM will load the new row data into the SRAM cache and update the LRR latch. The data at the specified column address is available at the output pins at the greater of times t_{RAC}, t_{AC}, and t_{GQV}. It is possible to bring /RE high after time t_{RE} since the new row data is safely latched into SRAM cache. This allows the EDRAM to precharge the DRAM array while data is accessed from SRAM cache. It is possible to access additional SRAM cache locations by providing new column addresses to the multiplex address inputs. New data is available at the output at time t_{AC} after each column address change. During read cycles, it is possible to operate in either static column mode with /CAL=high or page mode with /CAL clocked to latch the column address.

DRAM Write Hit

If a DRAM write request is initiated by clocking /RE while W/R and /F are high, the EDRAM will compare the new row address to the LRR address latch (an 11-bit address latch loaded on each /RE active read). If the row address matches, the EDRAM will write data to both the DRAM array and selected SRAM cache simultaneously to maintain coherency. The write address and data are posted to the DRAM as soon as the column address is latched by bringing /CAL low and the write data is latched by bringing /WE low (both /CAL and /WE must be high when initiating the write cycle with the falling edge of /RE). The write address and data can be latched very quickly after the fall of /RE ($t_{RAH} + t_{ASC}$ for the column address and t_{DS} for the data). During a write burst sequence, the second write data can be posted at time t_{RSW} after /RE. Subsequent writes within a page can occur with write cycle time t_{PC}. With /G enabled and /WE disabled, it is possible to perform cache read operations while the /RE is activated in write hit mode. This allows read-modify-

EDRAM Basic Operating Modes

Function	/S	/RE	W/R	/F	A_{0-10}	Comment
Read Hit	L	↓	L	H	Row = LRR	No DRAM Reference, Data in Cache
Read Miss	L	↓	L	H	Row ≠ LRR	DRAM Row to Cache
Write Hit	L	↓	H	H	Row = LRR	Write to DRAM and Cache, Reads Enabled
Write Miss	L	↓	H	H	Row ≠ LRR	Write to DRAM, Cache Not Updated, Reads Disabled
Internal Refresh	X	↓	X	L	X	
Low Power Standby	H	H	X	X	X	1mA Standby Current
Unallowed Mode	H	↓	X	H	X	

H = High; L = Low; X = Don't Care; ↓ = High-to-Low Transition; LRR = Last Row Read

write, write-verify, or random read-write sequences within the page with 15ns cycle times (the first read cannot complete until after time t_{RAC2}). At the end of a write sequence (after /CAL and /WE are brought high and t_{RE} is satisfied), /RE can be brought high to precharge the memory. It is possible to perform cache reads concurrently with precharge. During write sequences, a write operation is not performed unless both /CAL and /WE are low. As a result, the /CAL input can be used as a byte write select in multi-chip systems. If /CAL is not clocked on a write sequence, the memory will perform a /RE only refresh to the selected row and data will remain unmodified.

DRAM Write Miss

If a DRAM write request is initiated by clocking /RE while W/R and /F are high, the EDRAM will compare the new row address to the LRR address latch (an 11-bit latch loaded on each /RE active read cycle). If the row address does not match, the EDRAM will write data to the DRAM array only and contents of the current cache is not modified. The write address and data are posted to the DRAM as soon as the column address is latched by bringing /CAL low and the write data is latched by bringing /WE low (both /CAL and /WE must be high when initiating the write cycle with the falling edge of /RE). The write address and data can be latched very quickly after the fall of /RE (t_{RAH} + t_{ASC} for the column address and t_{DS} for the data). During a write burst sequence, the second write data can be posted at time t_{RSW} after /RE. Subsequent writes within a page can occur with write cycle time t_{PC}. During a write miss sequence, cache reads are inhibited and the output buffers are disabled (independently of /G) until time t_{WRR} after /RE goes high. At the end of a write sequence (after /CAL and /WE are brought high and t_{RE} is satisfied), /RE can be brought high to precharge the memory. It is possible to perform cache reads concurrently with the precharge. During write sequences, a write operation is not performed unless both /CAL and /WE are low. As a result, /CAL can be used as a byte write select in multi-chip systems. If /CAL is not clocked on a write sequence, the memory will perform a /RE only refresh to the selected row and data will remain unmodified.

/RE Inactive Operation

It is possible to read data from the SRAM cache without clocking /RE. This option is desirable when the external control logic is capable of fast hit/miss comparison. In this case, the controller can avoid the time required to perform row/column multiplexing on hit cycles. This capability also allows the EDRAM to perform cache read operations during precharge and refresh cycles to minimize wait states. It is only necessary to select /S and /G and provide the appropriate column address to read data as shown in the table below. The row address of the SRAM cache accessed without clocking /RE will be specified by the LRR address latch loaded during the last /RE active read cycle. To perform a cache read in static column mode, /CAL is held high, and the cache contents at the specified column address will be valid at time t_{AC} after address is stable. To perform a cache read in page mode, /CAL is clocked to latch the column address. The cache data is valid at time t_{AC} after the column address is setup to /CAL.

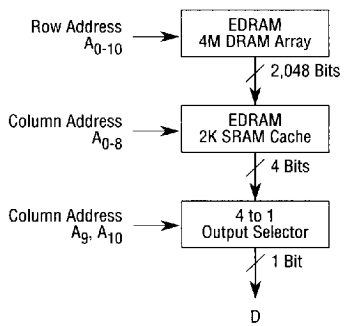
Function	/S	/G	/CAL	A_{0-10}
Cache Read (Static Column)	L	L	H	Column Address
Cache Read (Page Mode)	L	L	↕	Column Address

H = High; L = Low; X = Don't Care; ↕ = Transitioning

On-Chip SRAM Interleave

The DM2200 has on on-chip interleave of its SRAM cache which allows 8ns random accesses (t_{ACI}) to up to three data words (burst reads) following an initial read access (hit or miss). The SRAM cache is integrated into the DRAM array in a 512 x 4 organization. It is converted into a 2K x 1 page organization by using an on-chip address multiplexer to select one of four bits to the output pin D (as shown below). The specific databit selected to the output pin is determined by column addresses A_9 and A_{10}. System operation is consistent with the standard "Functional Description" and timing diagrams shown in this specification. See the note in the read timing diagrams and "Switching Characteristics" chart for the faster access and data hold times.

DM2200 Datapath Architecture



Internal Refresh

If /F is active (low) on the assertion of /RE, an internal refresh cycle is executed. This cycle refreshes the row address supplied by an internal refresh counter. This counter is incremented at the end of the cycle in preparation for the next /F refresh cycle. At least 1,024 /F cycles must be executed every 64ms. /F refresh cycles can be hidden because cache memory can be read under column address control throughout the entire /F cycle. /F cycles are the only active cycles during which /S can be disabled.

/CAL Before /RE Refresh ("/CAS Before /RAS")

/CAL before /RE refresh, a special case of internal refresh, is discussed in the "Reduced Pin Count Operation" section below.

/RE Only Refresh Operation

Although /F refresh using the internal refresh counter is the recommended method of EDRAM refresh, it is possible to perform an /RE only refresh using an externally supplied row address. /RE refresh is performed by executing a *write cycle* (W/R and /F are high) where /CAL is not clocked. This is necessary so that the current cache contents and LRR are not modified by the refresh operation. All combinations of addresses A_{0-9} must be sequenced every 64ms refresh period. A_{10} does not need to be cycled. Read refresh cycles are not allowed because a DRAM refresh cycle does not occur when a read refresh address matches the LRR address latch.

Low Power Mode

The EDRAM enters its low power mode when /S is high. In this mode, the internal DRAM circuitry is powered down to reduce standby current to 1mA.

Initialization Cycles

A minimum of 10 initialization (start-up) cycles are required before normal operation is guaranteed. A combination of eight /F refresh cycles and two read cycles to different row addresses are necessary to complete initialization.

Unallowed Mode

Read, write, or /RE only refresh operations must not be initiated to unselected memory banks by clocking /RE when /S is high.

Reduced Pin Count Operation

Although it is desirable to use all EDRAM control pins to optimize system performance, it is possible to simplify the interface to the EDRAM by either tying pins to ground or by tying one or more control inputs together. The /S input can be tied to ground if the low power standby mode is not required. The /CAL and /F pins can be tied together if hidden refresh operation is not required. In this case, a CBR refresh (/CAL before /RE) can be performed by holding the combined input low prior to /RE. The /WE input can be tied to /CAL if independent posting of column addresses and data are not required during write operations. In this case, both column address and write data will be latched by the combined input during writes. W/R and /G can be tied together if reads are not performed during write hit cycle. If these techniques are used, the EDRAM will require only three control lines for operation (/RE, /CAS [combined /CAL, /F, and /WE], and W/R [combined W/R and /G]). The simplified control interface still allows the fast page read/write cycle times, fast random read/write times, and hidden precharge functions available with the EDRAM.

Pin Descriptions

/RE — Row Enable

This input is used to initiate DRAM read and write operations and latch a row address as well as the states of W/R and /F. It is not necessary to clock /RE to read data from the EDRAM SRAM row registers. On read operations, /RE can be brought high as soon as data is loaded into cache to allow early precharge.

/CAL — Column Address Latch

This input is used to latch the column address and in combination with /WE to trigger write operations. When /CAL is high, the column address latch is transparent. When /CAL is low, the column address is closed and the output of the latch contains the address present while /CAL was high. /CAL can be toggled when /RE is low or high. However, /CAL must be high during the high-to-low transition of /RE except for /F refresh cycles.

W/R — Write/Read

This input along with /F specifies the type of DRAM operation initiated on the low going edge of /RE. When /F is high, W/R specifies either a write (logic high) or read operation (logic low).

/F — Refresh

This input will initiate a DRAM refresh operation using the internal refresh counter as an address source when it is low on the low going edge of /RE.

/WE — Write Enable

This input controls the latching of write data on the input data pins. A write operation is initiated when both /CAL and /WE are low.

/G — Output Enable

This input controls the gating of read data to the output data pin during read operations.

/S — Chip Select

This input is used to power up the I/O and clock circuitry. When /S is high, the EDRAM remains in its low power mode. /S must remain active throughout any read or write operation. With the exception of /F refresh cycles, /RE should never be clocked when /S is inactive.

D — Data Input

This input pin is used to write data to the EDRAM.

Q — Data Output

This output pin is used to read data from the EDRAM.

$A_{0\text{-}10}$ — Multiplex Address

These inputs are used to specify the row and column addresses of the EDRAM data. The 11-bit row address is latched on the falling edge of /RE. The 11-bit column address can be specified at any other time to select read data from the SRAM cache or to specify the write column address during write cycles.

V_{CC} Power Supply

These inputs are connected to the +5 volt power supply.

V_{SS} Ground

These inputs are connected to the power supply ground connection.

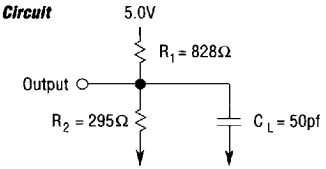
Pin Names

Pin Names	Function
A_0 - A_{10}	Address Inputs
/RE	Row Enable
D	Data In
Q	Data Out
/CAL	Column Address Latch
W/R	Write/Read Control
V_{CC}	Power (+5V)

Pin Names	Function
V_{SS}	Ground
/WE	Write Enable
/G	Output Enable
/F	Refresh Control
/S	Chip Select - Active/Standby Control
N.C.	No Connection

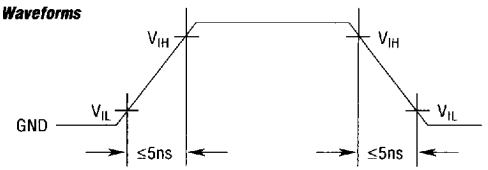
AC Test Load and Waveforms

Load Circuit



Input Waveforms

V_{IN} Timing Reference Point at V_{IL} and V_{IH}



Absolute Maximum Ratings

(Beyond Which Permanent Damage Could Result)

Description	Ratings
Input Voltage (V_{IN})	- 1 ~ 7v
Output Voltage (V_{OUT})	- 1 ~ 7v
Power Supply Voltage (V_{CC})	- 1 ~ 7v
Ambient Operating Temperature (T_A)	0 ~ 70°C
Storage Temperature (T_S)	-55 ~ 150°C
Static Discharge Voltage (Per MIL-STD-883 Method 3015)	>2000V
Short Circuit O/P Current (I_{OUT})	50mA*

*One output at a time; short duration.

Capacitance

Description	Max	Pins
Input Capacitance	7pf	A_0 - A_9
Input Capacitance	6pf	D
Input Capacitance	10pf	A_{10}, /CAL, /RE, W/R, /WE, /F, /S
Input Capacitance	2pf	/G
Output Capacitance	6pf	Q

Electrical Characteristics

(T_A = 0 - 70°C)

Symbol	Parameters	Min	Max	Test Conditions
V_{CC}	Supply Voltage	4.75V	5.25V	All Voltages Referenced to V_{SS}
V_{IH}	Input High Voltage	2.4V	6.5V	
V_{IL}	Input Low Voltage	-1.0V	0.8V	
V_{OH}	Output High Level	2.4V	—	I_{OUT} = - 5mA
V_{OL}	Output Low Level	—	0.4V	I_{OUT} = 4.2mA
$I_{i(L)}$	Input Leakage Current	-10µA	10µA	$0V \le V_{IN} \le 6.5V$, All Other Pins Not Under Test = 0V
$I_{O(L)}$	Output Leakage Current	-10µA	10µA	$0V \le V_{IN}$, $0V \le V_{OUT} \le 5.5V$

Symbol	Operating Current	33MHz Typ[1]	-15 Max	-20 Max	Test Condition	Notes
I_{CC1}	Random Read	110mA	215mA	170mA	/RE, /CAL, /G and Addresses Cycling: $t_C = t_C$ Minimum	2, 3
I_{CC2}	Fast Page Mode Read	65mA	115mA	90mA	/CAL, /G and Addresses Cycling: $t_{PC} = t_{PC}$ Minimum	2, 4
I_{CC3}	Static Column Read	55mA	110mA	85mA	/G and Addresses Cycling: $t_{SC} = t_{SC}$ Minimum	2, 4
I_{CC4}	Random Write	135mA	190mA	150mA	/RE, /CAL, /WE and Addresses Cycling: $t_C = t_C$ Minimum	2, 3
I_{CC5}	Fast Page Mode Write	50mA	135mA	105mA	/CAL, /WE and Addresses Cycling: $t_{PC} = t_{PC}$ Minimum	2, 4
I_{CC6}	Standby	1mA	1mA	1mA	All Control Inputs Stable ≥ V_{CC} - 0.2V	
I_{CCT}	Average Typical Operating Current	30mA	—	—	See "Estimating EDRAM Operating Power" Application Note	1

(1) "33MHz Typ" refers to worst case I_{CC} expected in a system operating with a 33MHz memory bus. See power applications note for further details. This parameter is not 100% tested or guaranteed.

(2) I_{CC} is dependent on cycle rates and is measured with CMOS levels and the outputs open.

(3) I_{CC} is measured with a maximum of one address change while /RE = V_{IL}.

(4) I_{CC} is measured with a maximum of one address change while /CAL = V_{IH}.

Switching Characteristics

(V_{CC} = 5V ± 5%, T_A = 0 - 70°C), C_L = 50pf

Symbol	Description	-15		-20		Units
		Min	Max	Min	Max	
t_{AC}[1]	Column Address Access Time for Addresses A_{0-8}		15		20	ns
t_{AC1}[1]	Column Address Access Time for Addresses A_9 and A_{10}		8		9	ns
t_{ACH}	Column Address Valid to /CAL Inactive (Write Cycle)	15		20		ns
t_{AQX}	Column Address Change to Output Data Invalid for Addresses A_{0-8}	5		5		ns
t_{AQX1}	Column Address Change to Output Data Invalid for Addresses A_9 and A_{10}	1		1		ns
t_{ASC}	Column Address Setup Time	5		5		ns
t_{ASR}	Row Address Setup Time	5		6		ns
t_C	Row Enable Cycle Time	65		85		ns
t_{C1}	Row Enable Cycle Time, Cache Hit (Row=LRR), Read Cycle Only	25		32		ns
t_{CAE}	Column Address Latch Active Time	6		7		ns
t_{CAH}	Column Address Hold Time	0		1		ns
t_{CH}	Column Address Latch High Time (Latch Transparent)	5		7		ns
t_{CHR}	/CAL Inactive Lead Time to /RE Inactive (Write Cycles Only)	-1		-1		ns
t_{CHW}	Column Address Latch High to Write Enable Low (Multiple Writes)	0		0		ns
t_{CQV}	Column Address Latch High to Data Valid		17		20	ns
t_{CQX}	Column Address Latch Inactive to Data Invalid for Addresses A_{0-8}	5		5		ns
t_{CQX1}	Column Address Latch Inactive to Data Invalid for Addresses A_9 and A_{10}	1		1		ns
t_{CRP}	Column Address Latch Setup Time to Row Enable	5		6		ns
t_{CWL}	/WE Low to /CAL Inactive	5		7		ns
t_{DH}	Data Input Hold Time	0		1		ns
t_{DS}	Data Input Setup Time	5		6		ns
t_{GQV}[1]	Output Enable Access Time		5		6	ns
t_{GQX}[2,3]	Output Enable to Output Drive Time	0	5	0	6	ns
t_{GQZ}[4,5]	Output Turn-Off Delay From Output Disabled (/G↑)	0	5	0	6	ns
t_{MH}	/F and W/R Mode Select Hold Time	0		1		ns
t_{MSU}	/F and W/R Mode Select Setup Time	5		6		ns
t_{NRH}	/CAL, /G, and /WE Hold Time For /RE-Only Refresh	0		0		ns
t_{NRS}	/CAL, /G, and /WE Setup Time For /RE-Only Refresh	5		6		ns
t_{PC}	Column Address Latch Cycle Time	15		20		ns
t_{RAC}[1]	Row Enable Access Time, On a Cache Miss		35		45	ns
t_{RAC1}[1]	Row Enable Access Time, On a Cache Hit (Limit Becomes t_{AC})		17		22	ns
t_{RAC2}[1,6]	Row Enable Access Time for a Cache Write Hit		35		45	ns
t_{RAH}	Row Address Hold Time	1.5		2		ns

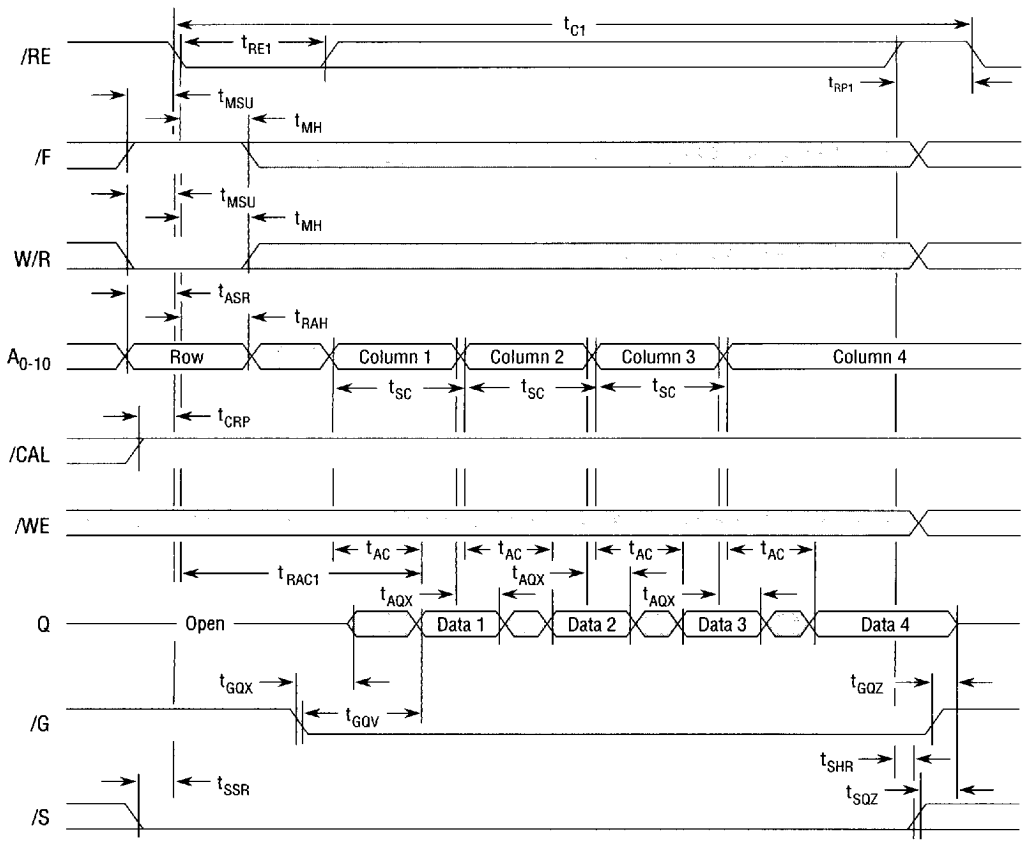
Switching Characteristics (continued)

(V_{CC} = 5V ± 5%, T_A = 0 - 70°C), C_L = 50pf

Symbol	Description	-15		-20		Units
		Min	Max	Min	Max	
t_{RE}	Row Enable Active Time	35	100000	45	100000	ns
t_{RE1}	Row Enable Active Time, Cache Hit (Row=LRR) Read Cycle	10		13		ns
t_{REF}	Refresh Period		64		64	ms
t_{RGX}	Output Enable Don't Care From Row Enable (Write, Cache Miss), O/P Hi Z	10		13		ns
t_{RP}(7)	Row Precharge Time	25		32		ns
t_{RP1}	Row Precharge Time, Cache Hit (Row=LRR) Read Cycle	10		13		ns
t_{RRH}	Read Hold Time From Row Enable (Write Only)	0		1		ns
t_{RSH}	Last Write Address Latch to End of Write	15		20		ns
t_{RSW}	Row Enable to Column Address Latch Low For Second Write	40		51		ns
t_{RWL}	Last Write Enable to End of Write	15		20		ns
t_{SC}	Column Address Cycle Time	15		20		ns
t_{SHR}	Select Hold From Row Enable	0		1		ns
t_{SQV}(1)	Chip Select Access Time		15		20	ns
t_{SQX}(2,3)	Output Turn-On From Select Low	0	15	0	20	ns
t_{SQZ}(4,5)	Output Turn-Off From Chip Select	0	10	0	13	ns
t_{SSR}	Select Setup Time to Row Enable	5		6		ns
t_T	Transition Time (Rise and Fall)	1	10	1	10	ns
t_{WC}	Write Enable Cycle Time	15		20		ns
t_{WCH}	Column Address Latch Low to Write Enable Inactive Time	5		7		ns
t_{WHR}	Write Enable Hold After /RE	0		1		ns
t_{WI}	Write Enable Inactive Time	5		7		ns
t_{WP}	Write Enable Active Time	5		7		ns
t_{WQV}(1)	Data Valid From Write Enable High		15		20	ns
t_{WQX}(2,5)	Data Output Turn-On From Write Enable High	0	15	0	20	ns
t_{WQZ}(3,4)	Data Turn-Off From Write Enable Low	0	15	0	20	ns
t_{WRP}	Write Enable Setup Time to Row Enable	5		5		ns
t_{WRR}	Write to Read Recovery (Following Write Miss)		18		20	ns

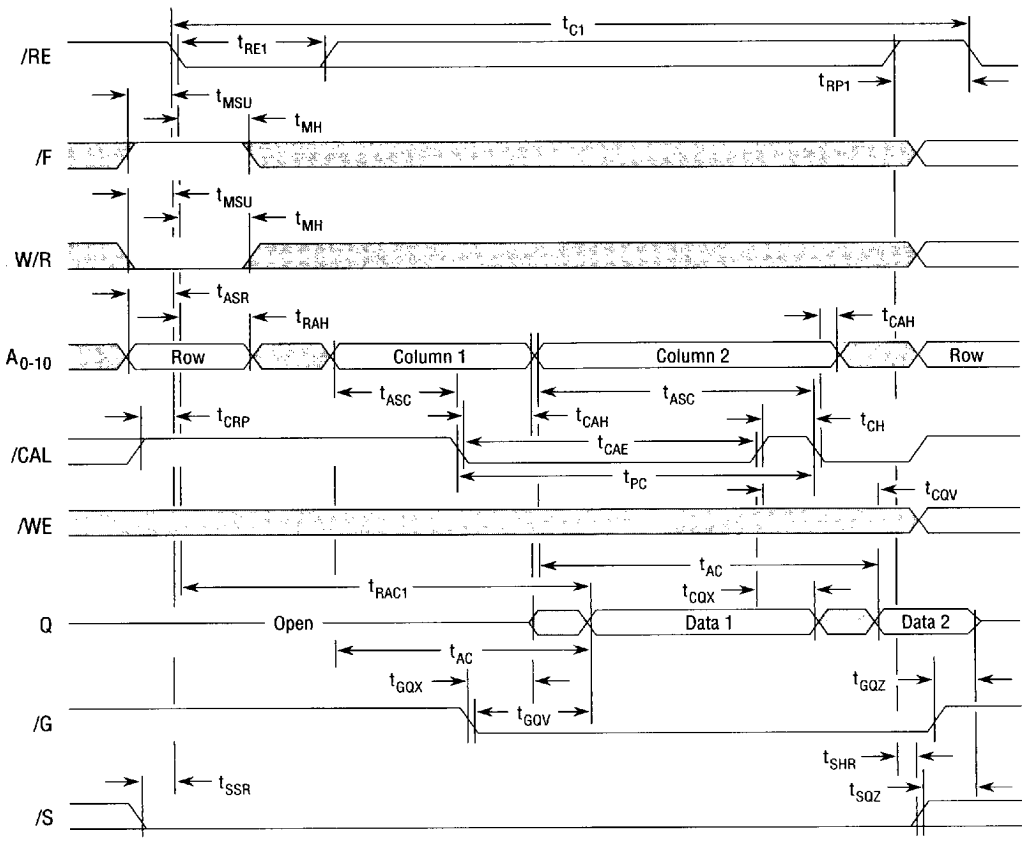
(1) V_{OUT} Timing Reference Point at 1.5V
(2) Parameter Defines Time When Output is Enabled (Sourcing or Sinking Current) and Not Referenced to V_{OH} or V_{OL}
(3) Minimum Specification is Referenced from V_{IH} and Maximum Specification is Referenced from V_{IL} on Input Control Signal
(4) Parameter Defines Time When Output Achieves Open-Circuit Condition and is Not Referenced to V_{OH} or V_{OL}
(5) Minimum Specification is Referenced from V_{IL} and Maximum Specification is Referenced from V_{IH} on Input Control Signal
(6) Access Parameter Applies When /CAL Has Not Been Asserted Prior to t_{RAC2}
(7) For Back-to-Back /F Refreshes, t_{RP}=40ns. For Non-consecutive /F Refreshes, t_{RP}=25ns and 32ns Respectively

/RE Active Cache Read Hit (Static Column Mode)



NOTES: 1. If column address 2, 3, or 4 modifies only address pin A_9 or A_{10}, then t_{AC} becomes t_{AC1} for data 2, 3, and 4, and t_{AQX} becomes t_{AQX1} for data 1, 2, and 3.

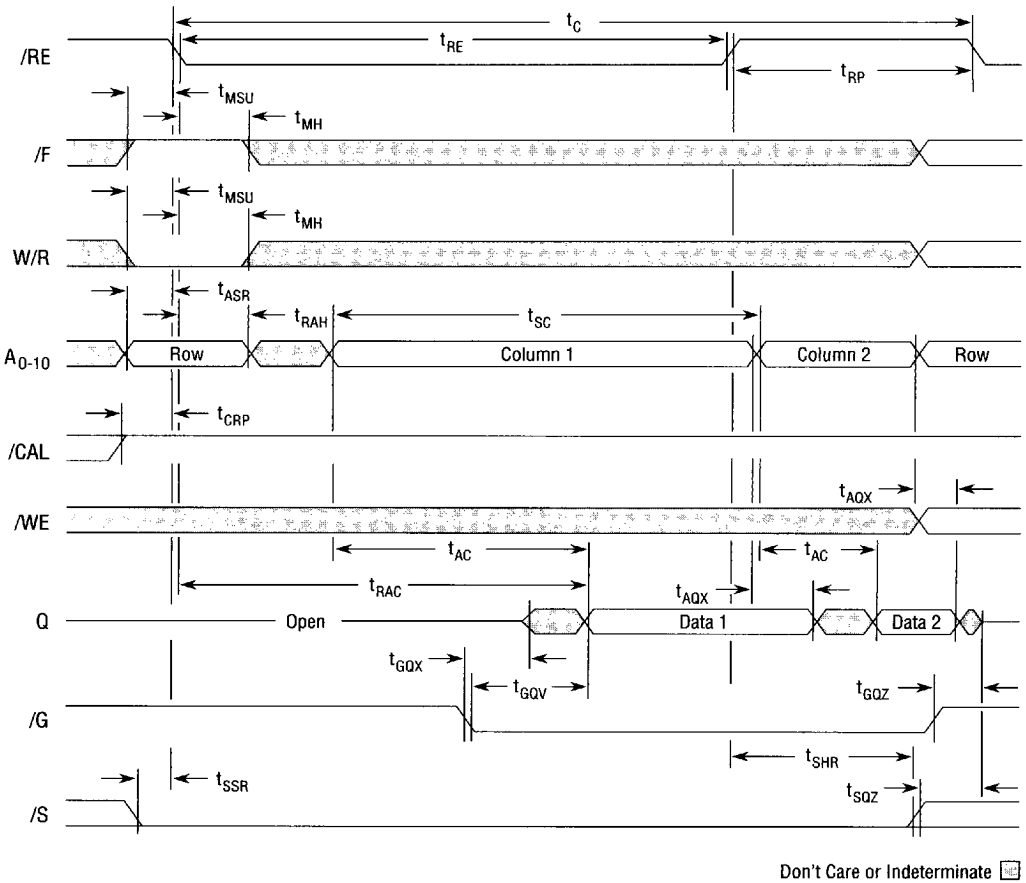
/RE Active Cache Read Hit (Page Mode)



NOTES: 1. If column address 2 modifies only address pin A_9 or A_{10}, then t_{AC} becomes t_{AC1} for data 2, and t_{CQX} becomes t_{CQX1} for data 1.

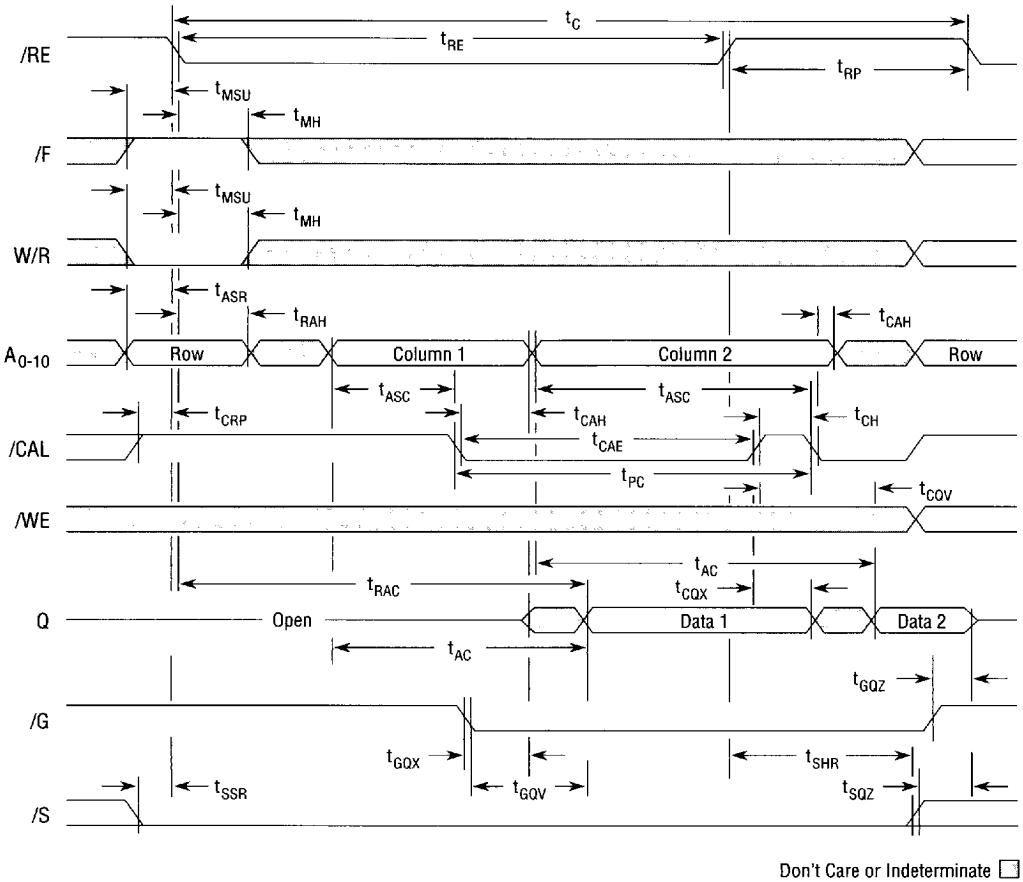
2

/RE Active Cache Read Miss (Static Column Mode)



NOTES: 1. If column address 2 modifies only address pin A_9 or A_{10}, then t_{AC} becomes t_{AC1} for data 2, and t_{AQX} becomes t_{AQX1} for data 1.

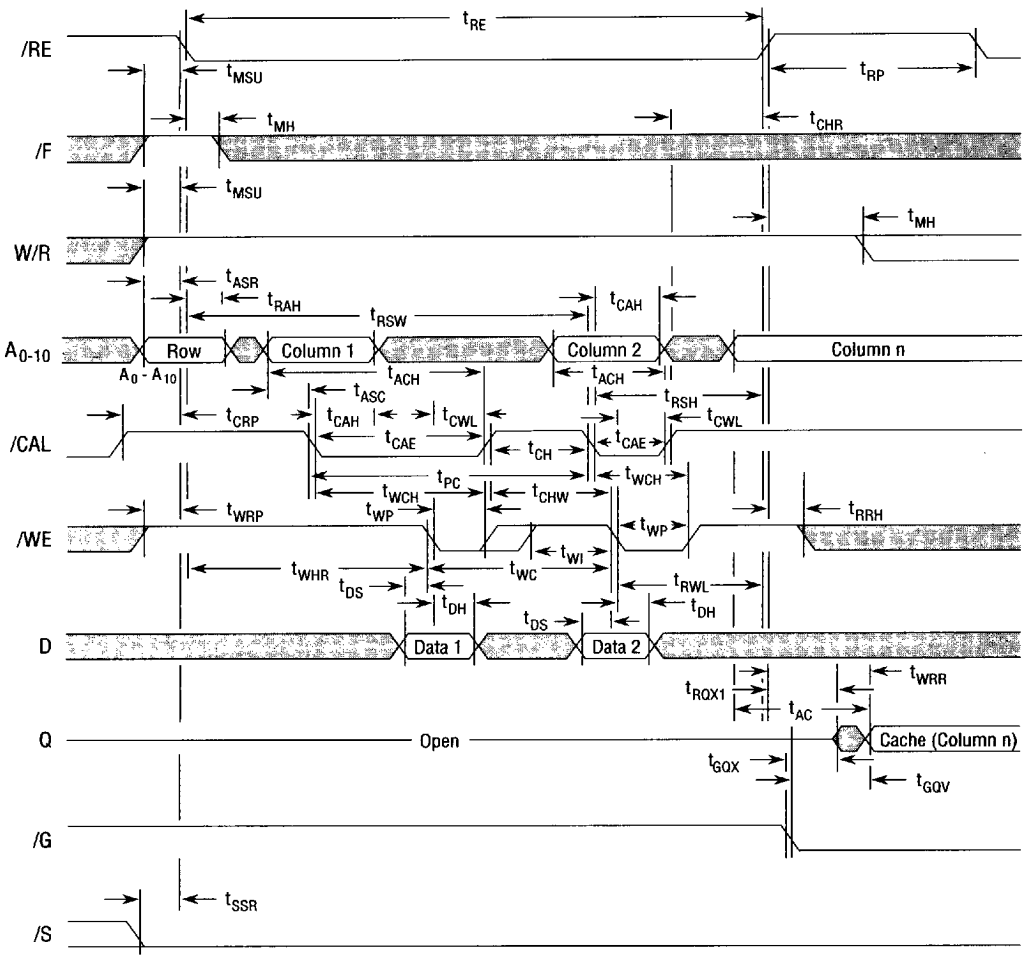
/RE Active Cache Read Miss (Page Mode)



NOTES: 1. If column address 2 modifies only address pin A_9 or A_{10}, then t_{AC} becomes t_{AC1} for data 2, and t_{CQX} becomes t_{CQX1} for data 1.

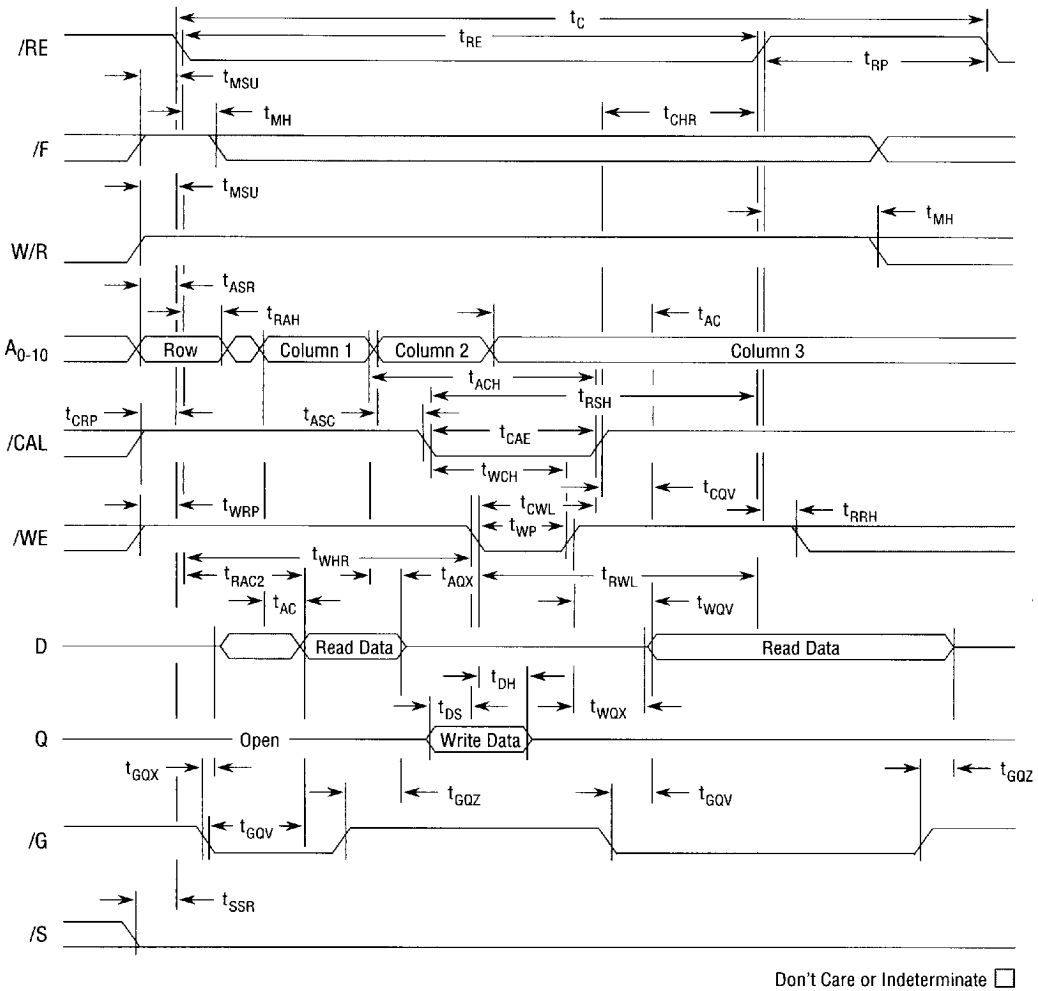
2

Burst Write (Hit or Miss) Followed By /RE Inactive Cache Reads



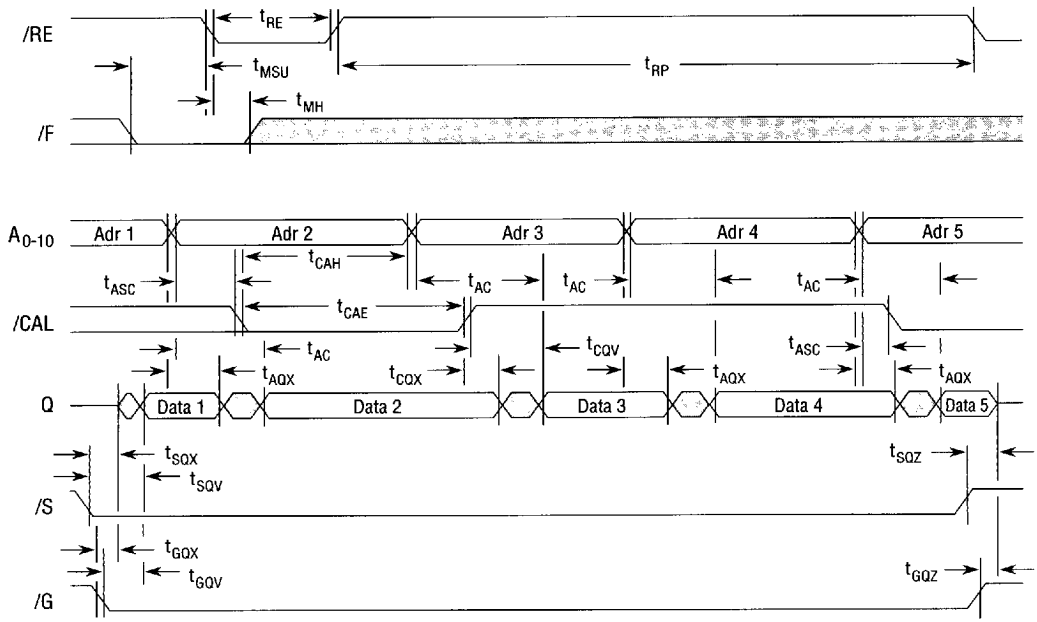
NOTES: 1. /G becomes a don't care after t_{RGX} during a write miss.

Page Read/Write During Write Hit Cycle (Can Include Read-Modify-Write)



NOTES: 1. If column address 2 modifies only address pin A_9 or A_{10}, then t_{AQX} becomes t_{AQX1}.

Hidden /F Refresh Cycle During Page Mode and Static Column Reads

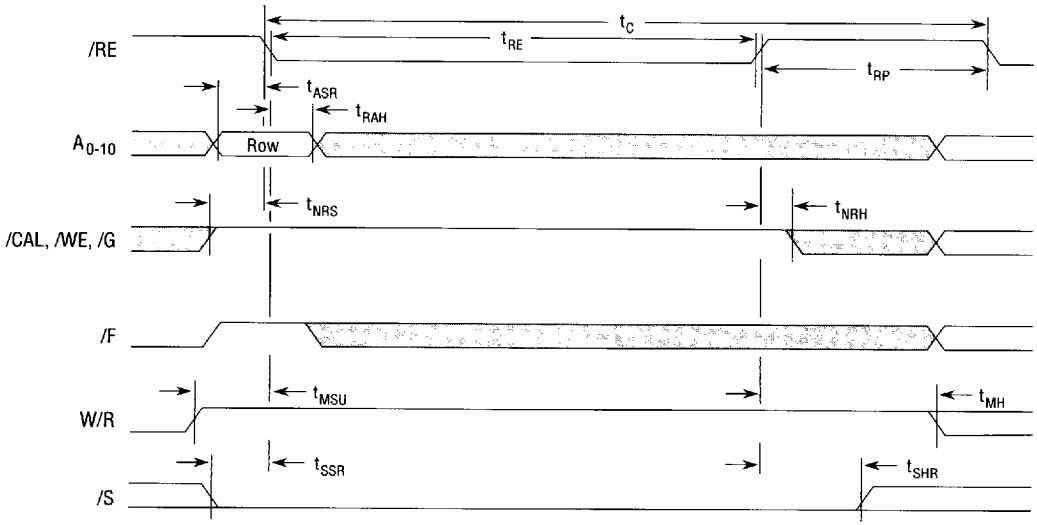


Don't Care or Indeterminate ☐

NOTES: 1. During /F refresh cycles, /S is a don't care unless cache reads are performed. For cache reads, /S must be low.

2. If column address 2, 3, 4, or 5 modifies only address pin A_9 or A_{10}, then t_{AC} becomes t_{AC1} for data 2, 3, 4, and 5, and t_{AQX} becomes t_{AQX1} for data 1, 2, 3, and 4.

/RE-Only Refresh

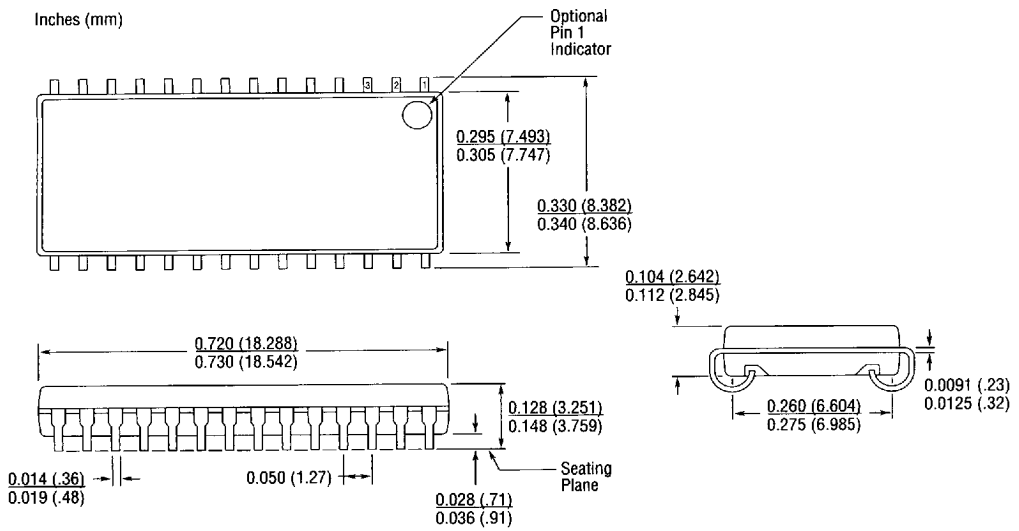


NOTES: 1. All binary combinations of A_{0-9} must be refreshed every 64ms interval. A_{10} does not have to be cycled, but must remain valid during row address setup and hold times.

2. /RE refresh is write cycle with no /CAL active cycle.

2

Mechanical Data
28 Pin 300 Mil Plastic SOJ Package



Part Numbering System

DM2200J - 15

Access Time from Cache in Nanoseconds
15ns
20ns

Packaging System
J = 300 Mil, Plastic SOJ

I/O Width
i.e., Power to Which 2 is Raised for I/O Width

Special Features Field
0 = No Write Per Bit
1 = Write Per Bit

Capacity in Bits
i.e., Power to Which 2 is Raised for Total Capacity

Dynamic Memory