DALLAS SEMICONDUCTOR

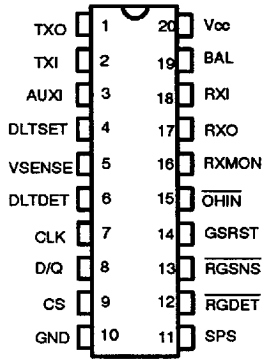
DS1360
Phantom DAA Chip

T-51-07-01

FEATURES

- Single-chip DAA controller for:
  - Modems
  - Speech interfaces
- Phantom operation reports loop current changes back to host
- Allows the DAA to use an existing phone line unobtrusively
- Transmit/receive interface connects directly to 600 ohm phone-line coupling transformers
- On-chip electronic 2- to 4-wire converter
- Integrates FCC Part–68 DAA requirements:
  - Ring detection
  - 2-second billing delay
  - Transmit power limiter
- Onboard, low-pass filtering of transmit and receive signals
- Replaces up to 20 discrete components
- Voice/data switching
- Software-controlled receive gain
- 3-wire serial control port
- +5 Volt single-supply operation
- DS1360S surface mount version available

PIN DESCRIPTION



DS1360 20–Pin DIP
(300 Mil.)

DESCRIPTION

The DS1360 Phantom DAA Chip is a CMOS device that integrates FCC requirements for interfacing data and voice to the telephone network. The DS1360 meets FCC Part-68 specifications such as 2-second billing delay, transmit signal power limiting, and ringing detection. It also offers programmable transmit and receive gains and an on-chip 2- to 4-wire converter (hybrid). By adding a coupling transformer, a relay, and an optocoupler, a complete DAA circuit can be quickly designed.

A unique feature of the DS1360 is its ability to sense loop current using an on-chip, 8-bit A/D converter. By using an external optocoupler (for proper isolation), the phone loop current can be digitized and monitored through the serial port by a host processor. The DS1360 can also be programmed by external resistors to report when the current has changed by a certain percentage. Loop current sensing is important for monitoring the activity of extension phones or for determining loop length for cable compensation.

PIN DESCRIPTION Table 1

PIN	SYM	TYPE	DESCRIPTION
1	TXO	O	**Transmit Output.** This is the transmit output which is the sum of the signals at AUXI and TXI (minus any attenuation needed to prevent excessive power transmission). This output can be connected to a telephone coupling transformer through an appropriate line matching resistor (typically 600 ohms).
2	TXI	I	**Transmit Input.** This is the transmit analog signal input which can be AC-coupled to any low-impedance source such as a modem chip output or an op-amp. The transmit limiter circuit will gradually attenuate the sum of the TXI and AUXI signals until the level output at TXO is less than 0.5 Vrms. If the sum of TXI and AUXI is less than 0.5 Vrms, then no adjustment is made. If more than 10 dB of attenuation is required, the TXO output is disabled until GSRST is toggled or power is cycled. This input is also controlled by the Control register in the software mode.
3	AUXI	I	**Auxiliary Input.** An auxiliary analog signal can be fed here to be summed with the TXI analog signal before transmission to the phone line. This input is controlled by the Control register in the software mode. The auxiliary input operates identically to the TXI input with regard to signal limiting and gain.
4	DLTSET	I	**Delta Voltage Set.** This pin is used in conjunction with the VSENSE pin in programming the voltage percentage at which the delta detector trips (DLTDET goes high).
5	VSENSE	I	**Voltage Sense In.** This is the input to the A/D converter which is used for the delta detector circuit or for digitizing low-frequency signals in general.
6	DLTDET	O	**Delta Detect Out.** This output goes high when the voltage at VSENSE has changed by more than a percentage as determined by external resistors. The operation of the delta detect circuit is controlled by the Control register in the software mode.
7	CLK	I	**Serial Clock In.** This input is used to clock serial port data in and out of the D/Q pin. The maximum clock frequency is 4 MHz. When SPS=0, this pin is used in conjunction with CS to program the RXMON gain.
8	D/Q	I/O	**Serial Port Data I/O.** This pin is used for transferring data to or from the serial port registers. Input data is sampled on rising edges of CLK; output data is updated on falling edges of CLK. When SPS=0, resampling of the DLTSET input is initiated by a rising edge at D/Q.
9	CS	I	**Chip Select Input.** This input should transition high to initiate serial port read or write operation. Returning CS to a logic 0 terminates a serial port operation. When SPS=0, this pin is used in conjunction with CLK to program the RXMON gain.
10	GND	I	**Ground.** This pin should be tied to system ground (0 volts).

11	SPS	I	**Serial Port Select.** This pin should be tied high in order to use the software mode; otherwise, tie this pin low for the hardware mode. The function of pins D/Q, CS, and CLK is affected by this input.
12	$\overline{\text{RGDET}}$	O	**Ring Detect Out.** This open-drain output goes active low whenever a proper ring signal is detected at the $\overline{\text{RGSNS}}$ input. Otherwise, this pin will go to a high-impedance state unless pulled up by an external resistor to the V_{CC} supply.
13	$\overline{\text{RGSNS}}$	I	**Ring Sense In.** This pin can be connected to the output of an optocoupled Ring Detect circuit. The Ring Detect circuit in the DS1360 will integrate the signal at $\overline{\text{RGSNS}}$ over the 20 Hz ring cycles to present a continuous logic 0 at $\overline{\text{RGDET}}$ that lasts for the duration of the ring burst (typically 2 seconds in the U.S.).
14	GSRST	I	**Gain Setting Reset.** When this input is at a logic 1, the gain settings for the transmit limiter circuit are reset to their default state. The limiter circuit begins adjusting the transmit level at TXO (only if the level is too high) when this pin returns low. The limiter gain settings are also reset upon power-up. This pin should only be used to transmit DTMF signals at a level higher than the normal -9 dBm limit specified for voice and data.
15	$\overline{\text{OHIN}}$	I	**Off-Hook In.** This input should be connected to the off-hook relay signal from the host system. When this input transitions low, the TXO output is disabled (forced to mid-supply) for at least 2 seconds only if a ring signal was detected within the last 8 seconds. Otherwise, the TXO output is enabled, except when the TXDIS bit = 1 or if in the power-down mode.
16	RXMON	O	**Receive Monitor Out.** This is a buffered, gain-selectable version of the receive hybrid output. The gain from RXI to RXMON is programmed using the Receive Monitor Gain register. This signal can be routed to an external speaker amplifier or a handset for audio monitoring of the receive signal. The load impedance should be $\geq$ 5K ohms.
17	RXO	O	**Receive Out.** The receive output of the hybrid is present at this pin. The gain from the RXI input to RXO is 1.5 dB (to make up for the loss through a typical coupling transformer). The load impedance should be $\geq$ 5K ohms.
18	RXI	I	**Receive In.** This is the receive input to the internal hybrid circuit.
19	BAL	–	**Balance Network.** An optional balance network can be attached at this pin for adjusting the return loss of the hybrid. Normally, this pin should be left floating if not used.
20	VCC	I	**Positive Supply In.** Tie this pin to +5 volts.

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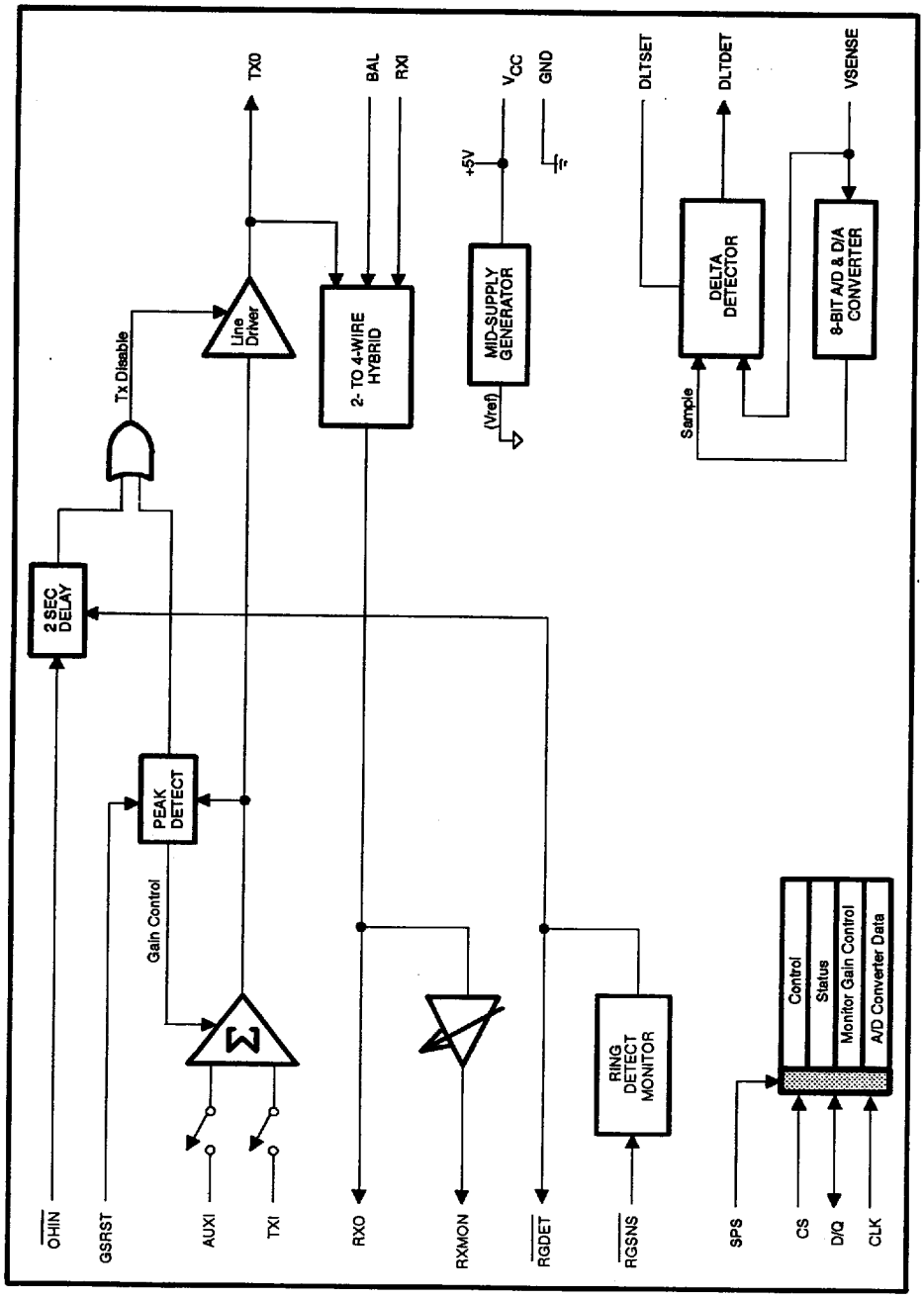
DS1360 BLOCK DIAGRAM Figure 1



OVERVIEW

The DS1360 Phantom DAA (Data Access Arrangement) Chip is a CMOS monolithic device that integrates many of the functions required by the FCC for interfacing voice and data to the telephone network. By adding a coupling transformer, an optocoupler, and an off-hook relay, an FCC Part-68-compatible DAA circuit can be quickly designed. Although the final system must still be tested and certified by an FCC approved testing lab, the DS1360 greatly reduces the design time as well as the component cost and board space for implementing the DAA function. A block diagram of the DS1360 is shown in Figure 1.

An integral 2- to 4-wire converter or hybrid circuit isolates transmit and receive signals for use with a telephone coupling transformer. The transmit output is specifically designed to drive telephone line impedances with low distortion using a single +5 volt supply. Voice and data signals can be multiplexed under software control to feed the transmit output. Automatic power limiting and a 2-second billing delay are included in the transmit path in order to meet FCC Part-68 requirements.

The receive section of the DS1360 is split into two paths. One path feeds the RXO output, which is normally connected to the input of a modem or FAX device. The other path is routed to a gain-programmable op-amp which then feeds the RXMON output. This output can be used to drive an external speaker or handset, although it can also be used with modem devices.

The ring detection circuit can take the raw output of an external optocoupled ring sensor and process it into a glitchless square wave that corresponds to the ring burst duty cycle. Ring detection is reported at both the $\overline{\text{RGDET}}$ pin and in the Status register.

An onboard, 8-bit, analog-to-digital (A/D) converter is used to digitize and process external low-frequency signals such as loop current, receive power level, or analog sensor outputs. Conversion samples are accessible through the serial port. The conversion time is typically 80 uS. The DS1360 also includes a Delta Detector circuit that optionally reports when the input signal to the A/D converter has changed by a certain percentage.

Control of the DS1360 is accomplished using either the software or hardware modes. In the hardware mode (SPS = 0), device operation is controlled by tying certain pins high or low. The software mode (SPS = 1) uses a 3-wire serial interface for accessing internal registers. These registers provide control and monitoring information for use by an external microcontroller or microprocessor.

A power-down mode is included for reducing power dissipation in low-power applications. The power-down mode is controlled by the PD bit in the Control register. The power-down mode is exited by either clearing the PD bit or by a high-to-low transition on $\overline{\text{RGSNS}}$.

TRANSMIT INPUT

A block diagram of the the transmit input circuitry is shown in Figure 2. The analog signals at AUXI and TXI are summed together and sent on to the line driver unless disabled by bits CTR.2 and/or CTR.3 in the Control register. These bits can be used as a mux for switching between voice and data when using the software mode (SPS = 1). In the hardware mode, AUXI and TXI are always enabled and switching must be done externally.

The peak detector circuit continuously samples the output of the input summing op-amp to determine if the level is too high. Signals routed on to the line driver must be less than -4dBm (0.5 Vrms) to meet FCC Part-68 limits for maximum transmission level (the line driver itself has unity gain). If the level to the line driver is higher than -4 dBm, the peak detector begins to attenuate the signal until it is in compliance (adjustment is only in the direction of increasing loss). The attenuation range is 10 dB; if more than 10 dB of loss is needed, the peak detector will disable the signal path to the line driver. Once the attenuation has reached a stable setting, it can only be reset by either taking GSRST high, by setting 'RSTPK' (CTR.1=1), or by cycling the power. Taking GSRST high resets the attenuation setting back to 0 dB (no loss), effectively disabling the signal limiting function for as long as GSRST is high. The peak detector returns to normal operation once GSRST goes low again.

TRANSMIT INPUT SECTION Figure 2

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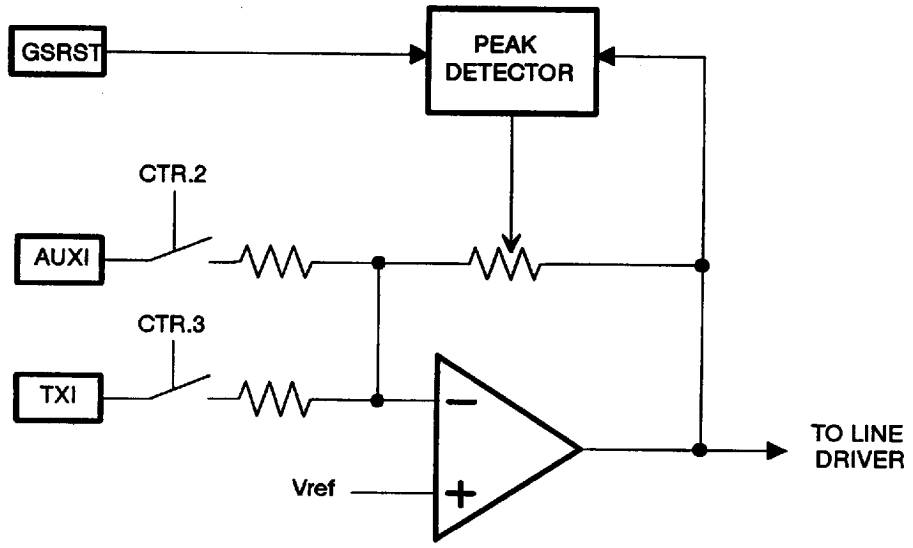

The GSRST input may also be taken high to transmit DTMF tones at the higher level of +2 dBm, resulting in -4 dBm on the telephone line. Part-68 permits a level of 0 dBm maximum for DTMF tone transmission. Once the DTMF digits have been sent, GSRST should be returned low to limit normal data transmission levels to -4 dBm maximum at the TXO output. Improvements in transmission quality throughout the telephone network have greatly reduced the need to transmit at higher levels; therefore, using GSRST in this manner is usually not necessary.

The attenuation steps are as follows: 0, -0.25, -0.5, -1.0, -2.0, -3.0, -6.0, -10.0, and infinite (signal path disabled). The initial steps are gradual to permit transmission near the maximum of -4 dBm at TXO. The limit of -4 dBm was chosen since the matching resistor to the telephone line will normally introduce another 6 dB of loss. Therefore, the resulting power on the line will be -10 dBm which is 1 dB less than the maximum level allowed by Part-68 of -9 dBm for data signals. The 1 dB margin is necessary for variations in the absolute accuracy of the peak detector due to changes in process, temperature, and supply voltage. The peak detector steps through the attenuation values until a level less than -4 dBm is reached.

It is important to note that the peak detector monitors and attenuates the sum of TXI and AUXI. If TXI and AUXI are both enabled and their respective signal levels are at -6 dBm, the sum may exceed -4 dBm which will cause the peak detector to introduce the appropriate amount of attenuation.

BILLING DELAY

An on-chip billing delay circuit is provided to meet Part-68 requirements to provide the network adequate time for billing information before modem data is sent. The billing delay is nominally set to 2.25 seconds, well within the two seconds required. The billing delay timer is triggered by a negative transition on $\overline{\text{OHIN}}$ which causes the TXO output to be squelched for at least two seconds. Afterwards, the TXO output begins to respond to signals at the TXI and AUXI inputs as described previously.

The billing delay only operates when going off-hook in answer to a ring signal. Specifically, if a ring burst has not been received in the eight seconds preceding $\overline{\text{OHIN}}$ going low, the billing delay is unused and TXO is enabled immediately. This permits the host system to go

off-hook when needing to immediately dial a number. It is then the responsibility of the answering modem to provide a 2-second delay before sending data.

TRANSMIT LINE DRIVER

The transmit line driver takes the output of the input summing op-amp and buffers it to the TXO pin. Normally, TXO would be connected through a line-matching resistor to a telephone coupling transformer. The resulting impedance attached to TXO is the matching resistor plus the telephone line impedance – typically 1.2K ohms (600 + 600 = 1.2K ohms). The line driver will actually drive up to 600 ohms without significant distortion up to the point of clipping. Clipping typically occurs when the signal at TXO is within 0.25 volts of either power supply rail.

The line driver also removes extraneous high-frequency signals using a 1-pole, low-pass filter with a break point at 12 KHz. This filter attenuates the clock switching noise that modem devices typically add to the modulated data signal as well as any coupled noise from the power supply. A typical clock switching frequency of 128 KHz would be attenuated by 20 dB before transmission out to TXO. A spectrum analyzer should be used to look at the TXO output to check that attenuation of out-of-band signals conforms to Part-68 requirements. Typically, the internal low-pass filter provides adequate attenuation.

The TXO output has a DC offset of $V_{CC}/2$ volts (2.5 volts if V_{CC} = 5 volts) and usually should be AC-coupled with a capacitor when connecting to a transformer. Typically, one leg of the transformer is hooked to ground which means that TXO would have to drive 2.5 volts into the large DC load of the line matching resistor if not AC-coupled. A value of 1 uF or more is usually adequate; lower values may introduce in-band attenuation of the transmit and receive signals. If a low impedance mid-supply is available in the system, then it may be tied to the transformer in lieu of ground. In that case, the coupling capacitor is not needed.

When the power-down mode is entered (PD=1 in the Control register), the TXO output is tri-stated to help conserve power. Note that the off-hook relay should disconnect the phone line connection when using the power-down mode since the TXO output is now in a high-impedance state (i.e., the reflected impedance back to the line is no longer 600 ohms).

2- TO 4-WIRE HYBRID T-51-07-01

The internal electronic 2- to 4-wire hybrid circuit splits the signal to/from the telephone line into separate transmit and receive signals. As illustrated in Figure 3, the hybrid consists of an op-amp which sums a portion of the TXO signal with the signal at RXI which is usually tied to the external coupling transformer. The receive gain from RXI to the output of the hybrid is about 1.5 dB to make up for the typical insertion loss of a coupling transformer. The hybrid assumes that the TXO component at RXI will be 6 dB lower than that at the TXO pin. As a result, the sum of the TXO signal through the inverting and non-inverting gain paths of the hybrid op-amp is theoretically 0, which means that only the receive signal from the other end of phone line should be present at the hybrid output (RXO). However, due to variations in the phone line impedances, the signal at RXI varies in phase and amplitude from the the ideal case; consequently, the TXO component is not completely cancelled by the hybrid. Typically, the return loss (the loss of the transmit signal through the hybrid) varies from 10 to 16 dB.

The return loss of the hybrid can be adjusted by an external compensation network attached to the BAL pin. External balancing is optional and in most cases the user can simply float this pin. The amplitude and phase of the signal routed to the non-inverting terminal of the hybrid op-amp can be programmed using external resistors and capacitors. When using external resistors, make sure to use values low enough to swamp out the internal resistor divider.

Another way to balance the hybrid is to change the external line-matching resistor (nominally 600 ohms) until the TXO component at RXI is exactly 6 dB lower than at TXO. Phase compensation may be added by tying a capacitor from either TXO or GND to the BAL pin. Note that the absolute values of the internal resistors connected to the BAL vary $\pm$ 20% ,while their ratio varies only $\pm$ 0.1%.

The output of the hybrid is sent on to the RXO pin and to a programmable gain op-amp which feeds the RXMON pin. RXO and RXMON are both designed to drive $\geq$ 5K ohm loads.

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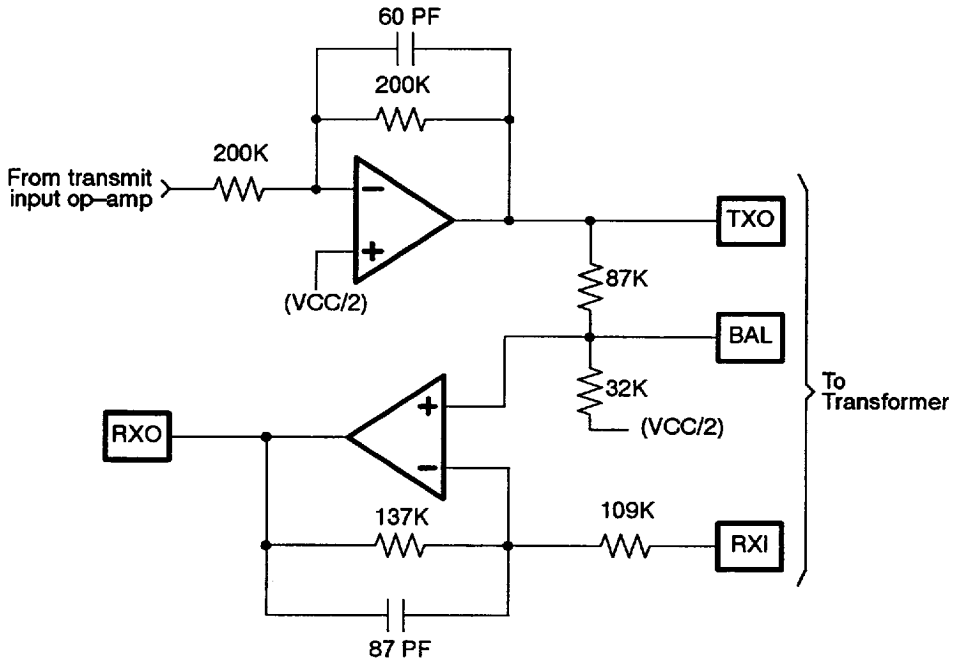
TRANSMIT DRIVER/ RECEIVE HYBRID SECTION Figure 3



RECEIVE MONITOR OUTPUT

The RXMON output is a gain-programmable version of the signal at RXO (RXMON is also 180 degrees out of phase with RXO). In the software mode, the gain from the hybrid output to RXMON can be programmed using the Receive Monitor Gain register. As shown in Table 2, eleven gain values ranging from +9.0 to -21 dB can be selected. An additional value (OFF) can be used to completely mute the RXMON output. This might be useful when using the DS1360 with a handset for voice/data switching. RXMON can also be connected to a speaker buffer amp for use with a monitor speaker. A monitor speaker is normally included in Hayes compatible modems; the AT command set in such modems specifies programmable speaker levels which can be easily implemented using RXMON.

In the hardware mode (SPS = 0), the gain for RXMON is programmed by using the CS and CLK multifunction pins. The four gain values supported are shown in Table 2.

HARDWARE MODE GAIN Table 2

CS	CLK	Gain (dB)
0	0	+6.0
0	1	0.0
1	0	-6.0
1	1	off

RING DETECTION

Ring detection can be accomplished using the $\overline{\text{RGSNS}}$ and $\overline{\text{RGDET}}$ pins with an external optocoupler sensor circuit (see Figure 4). The $\overline{\text{RGSNS}}$ input digitally integrates low-going pulses output from a ring sensing optocoupler. The integrated signal is then fed to the $\overline{\text{RGDET}}$ output which goes to a logic 0 when a valid ring signal has been received at $\overline{\text{RGSNS}}$. $\overline{\text{RGDET}}$ is an open-drain output and should be pulled up by an external resistor to define the off state (logic 1). The $\overline{\text{RGDET}}$ state is also reported by the Status register in the software mode; each ring occurrence is latched by the RGDET bit; a read operation of this register clears the RGDET bit until the next valid detection of a ring burst.

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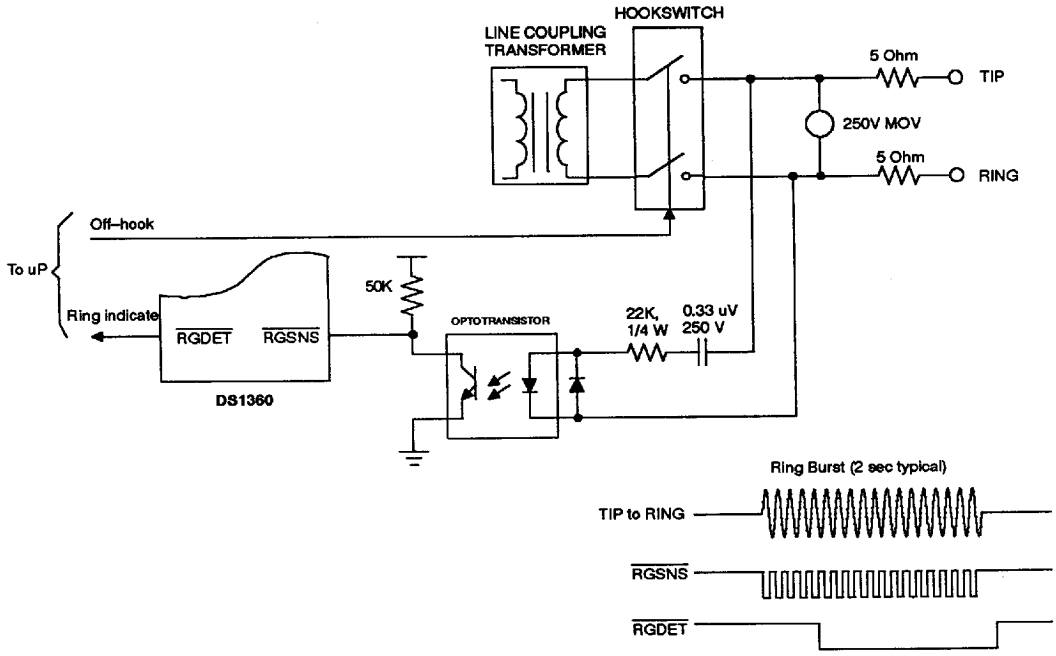
RING DETECTION OPERATION Figure 4



Ringing on the telephone line can be 15 to 68 Hz in frequency and 40 to 150 Vrms in amplitude. The task of the ring sensor circuit is to provide the $\overline{\text{RGSNS}}$ pin with low pulses corresponding to the ring signal exceeding some voltage threshold. Figure 4 shows a recommended circuit which provides the ring sensing as well as the 1000 Vrms isolation required by Part-68. The final processed ring detect signal is presented at $\overline{\text{RGDET}}$ which can then be used by a microprocessor. This circuit in Figure 4 also presents an on-hook AC impedance that complies with Part-68.

Low-going signals at $\overline{\text{RGSNS}}$ also cause the DS1360 to exit the power-down mode. The purpose of this feature is to allow a ring signal to wake up a system that is in a low-power state. Once powered up, the DS1360 internally clears the PD bit in the Control register.

A/D CONVERTER OPERATION

The DS1360 includes an 8-bit linear A/D converter for use with low-frequency and DC signals. The converter can sample either the VSENSE or DLTSET inputs, depending upon the mode the DS1360 is in. The result of the A/D conversion is placed in the A/D Data register (ADR) which can be read through the serial port. The coding for the 8-bit data sample is shown in Figure 5.

A/D CONVERTER TRANSFER FUNCTION Figure 5

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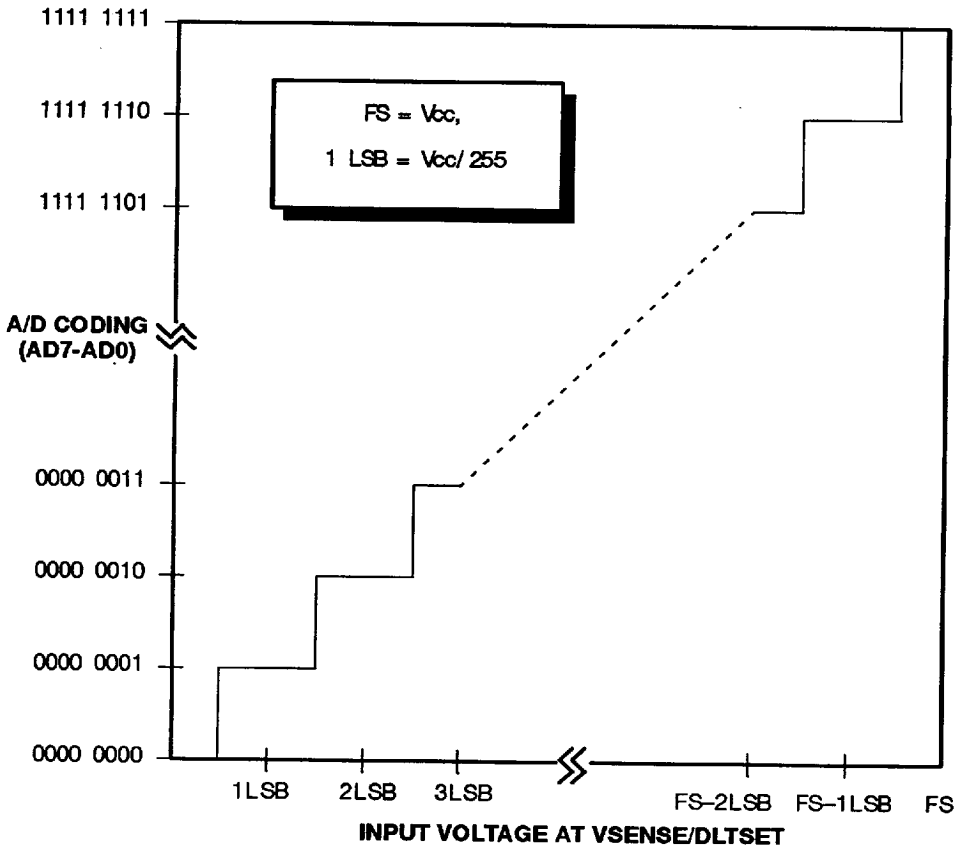

Input signals at VSENSE or DLTSET may be anywhere in the range from GND to V_{CC}; each step of the A/D converter is then $V_{CC}/255$ volts. For a typical Vcc = +5V, the A/D converter can resolve down to 20 mV. The absolute accuracy of the converter is entirely dependent upon Vcc; no internal reference is used. Signals connected to VSENSE should use the Vcc supply so that the changes in Vcc will not affect the A/D conversion accuracy. The input impedance is typically 8 pF to ground (GND).

The converter architecture uses a Successive-Approximation register (SAR) approach with an R-2R ladder DAC. This approach lends itself to quick conversion times (80 uS typically) with excellent accuracy and linearity. The converter does not include a sample-and-hold stage since the intended use is with slowly varying or DC signals (this does not preclude the use of an external sample and hold circuit). The clocking for the conversion process is derived from an internal 130 KHz oscillator that is also used for the billing delay timing.

DELTA DETECTOR

The delta detector is for use in a phantom modem by sensing changes in the DC loop current. Loop current sensing is important for detecting when extension devices on the telephone line go off-hook. For example, the DS1360 could be used in a FAX or modem application to know when the telephone handset was picked up. A Teleservicing application can use the Phantom feature to non-intrusively borrow the phone line when it is free and to release it when someone picks up an extension phone set.

DELTA DETECTOR SCHEMATIC Figure 6

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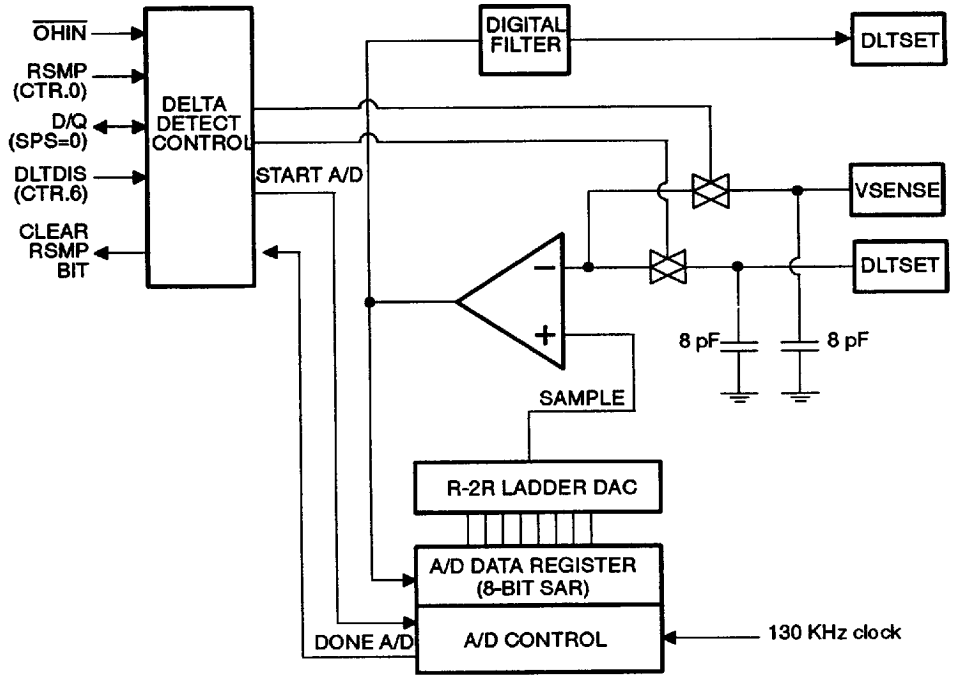


In the hardware mode (SPS = 0), the delta detect circuit reports changes in the voltage at VSENSE using the A/D converter. In this mode, the signal at DLTSET is automatically sampled 250 mS after each falling edge at $\overline{\text{OHIN}}$; this sample is stored in the R-2R DAC and then continuously compared to the voltage at VSENSE. When the voltage at VSENSE is lower than the old sample of DLTSET, the DLTDET pin transitions to a logic 1. DLTDET stays high until the DLTSET input goes back to a higher voltage or when $\overline{\text{OHIN}}$ goes high. To resample DLTSET after the automatic sample is taken, the D/Q pin can be used. A rising edge at D/Q in the hardware mode causes a new sample to be taken of DLTSET.

A resistor divider can be placed between the VSENSE and DLTSET inputs to program where the DLTDET triggers. For example, to detect a 35% change at VSENSE, one resistor would be 55% of the other. Figure 6 illustrates the operation of the delta detector. Figure 8 shows an application.

In the software mode, the delta detector can be controlled using the DLTDIS bit in the Control register. When DLTDIS = 1, the delta detector circuit is disabled (DLTDET is forced to a 0). An 8-bit A/D conversion of the signal on the VSENSE pin is initiated by setting the RSMP bit to a 1; when the conversion is complete, this bit is automatically cleared internally (the host can poll this bit to see when the conversion is done). Each conversion result is written into the ADR register which can then be retrieved by the host.

If the DLTDIS = 0, the delta detector is enabled and a sample of the DLTSET input is automatically taken after each high-to-low transition at $\overline{\text{OHIN}}$ (just as in the hardware mode). Setting the RSMP bit high in this mode initiates resampling of the DLTSET signal (not VSENSE) which is then continuously compared to the VSENSE signal. The DLTSET samples are stored in the ADR register. The DLTDET output can be used as an interrupt to

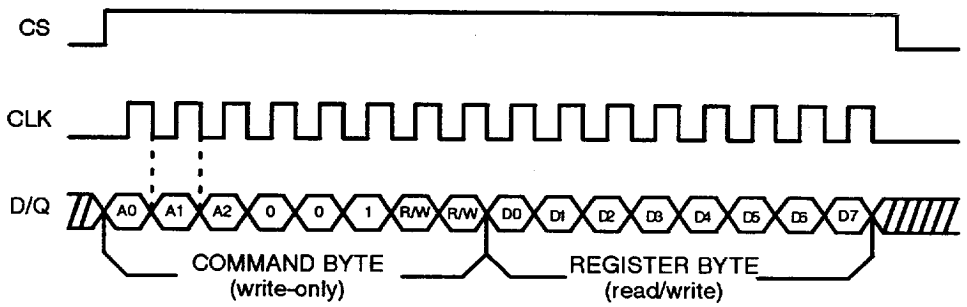
alert the host microprocessor of voltage changes as an alternative to polling of the serial port.

SERIAL PORT OPERATION

The serial control port of the DS1360 consists of three pins: CS, CLK, and D/Q. These three signals provide synchronous access of internal control and status registers. To use the serial port, the DS1360 must be placed in the software mode by tying the SPS (Serial Port Select) pin high. The host can then access the internal registers by transferring a 2-byte sequence; the first byte is write-only and provides command and register address information, while the second byte is the actual register data that is either read or written by the host. Data bytes to and from the DS1360 are always transferred LSB first. The serial port can be operated at any time even when the DS1360 is in the power-down mode. As shown in Figure 7, a serial port operation is initiated by first taking CS (Chip Select) high. The host then clocks in the command byte using a clock supplied to the CLK pin. Data written to the D/Q pin is sampled on rising edges of CLK. The first three bits indicate register address information, the next three bits are device selection bits, and the last two bits the type of operation (read or write). There are six registers available for host use.

The next eight clock cycles at CLK transfer data into or out of a particular register within the DS1360. For a write operation, the DS1360 samples data at D/Q on rising clock edges; for a read operation, data at D/Q is updated on falling clock edges. Note that for a read operation, the DS1360 will drive the D/Q line after the eighth falling edge of CLK. Once the last bit has been transferred, the CS line should be taken low to terminate the operation.

SERIAL PORT OPERATION[1] Figure 7



1. Command and register bytes are always read/written LSB first.

REGISTER ADDRESSES Table 3

REGISTER	ADDRESS[1] (A2,A1,A0)
CONTROL REGISTER	000
STATUS REGISTER	001
RECEIVE MONITOR GAIN	010
A/D DATA REGISTER	011
SPARE 1	100
SPARE 2	101

1. Address values 100 through 111 are used for factory test and should never be used.
2. Spares are read/write, temporary storage registers.

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REGISTER POWER-ON DEFAULT VALUES Table 4

REGISTER	VALUE
CTR	0000 0100 (AUXI input disabled)
STR	1111 0000
RMR	1111 1111 (RXMON off)
ADR	0000 0000
SP1	0000 0000
SP2	0000 0000

COMMAND BYTE (WRITE-ONLY) Table 5

R/W	R/W	1	0	0	A2	A1	A0

(MSB) (LSB)

SYMBOL	POSITION	NAME AND DESCRIPTION
R/W	CB.7	Determines read or write operation
R/W	CB.6	00 = write operation 11 = read operation 01,10 = undefined
1	CB.5	Device select bits
0	CB.4	
0	CB.3	
A2	CB.2	MSB of Register Address
A1	CB.1	
A0	CB.0	LSB of Device Address

CONTROL REGISTER (READ/WRITE) Table 6

0	TXODIS	DLTDIS	PD	TXE	AUXE	RSTPK	RSMP

(MSB) (LSB)

SYMBOL	POSITION	NAME AND DESCRIPTION
0	CTR.7	Unused; must be zero for proper operation.
TXODIS	CTR.6	Three-states TXO output and disconnects TXO from the internal hybrid. 0 = normal operation 1 = TXO high-impedance
DLTDIS	CTR.5	Delta Detect Disable. 0 = Delta detector enabled 1 = Delta detector disabled This bit is used to disable the operation of the delta detector circuit. The 8-bit A/D converter continues to operate in response to sample requests via the RSMP bit.
PD	CTR.4	Power Down control. 0 = normal operation 1 = power down When this bit is set to a 1, the DS1360 enters a low-power mode. All analog outputs (TXO, RXO, and RXMON) are disabled and the internal processing clock is halted. Power down mode is exited by either: 1) the PD bit being cleared by software or a power-up on V_{CC} or 2) a falling edge on the $\overline{RGSNS}$ pin.

TXDIS	**CTR.3**	Transmit input signal enable. 0 = TXI signal path enabled 1 = TXI signal path disabled
AUXDIS	**CTR.2**	Auxiliary input signal enable. 0 = AUXI signal path enabled 1 = AUXI signal path disabled
RSTPK	**CTR.1**	Reset transmit signal limiter peak detector. 0 = normal operation 1 = peak detector in reset state This bit must be cleared by the host to a 0 for proper operation of the transmit limiter function; otherwise, the transmit signal will pass through unattenuated.
RSMP	**CTR.0**	Resample signal present at VSENSE or DLTSET pin. 0 = normal operation 1 = take new sample (cleared internally) The 8-bit sample is stored in the the ADR register which can be read by the host. This bit is cleared internally after ADR is loaded with a new sample. RSMP resamples the VSENSE pin when DLTDIS=1 and the DLTSET pin when DLTDIS=0.

STATUS REGISTER (READ ONLY) Table 7

1	1	1	1	TXSQU	TXLVL	DLDET	RGDET
(MSB)							(LSB)

SYMBOL	POSITION	NAME AND DESCRIPTION
1	**STR.7**	Unused.
1	**STR.6**	Unused.
1	**STR.5**	Unused.
1	**STR.4**	Unused.
TXSQU	**STR.3**	Transmit output squelched due to excessive signal power. 0 = TXO output active 1 = TXO output squelched This bit latches to a 1 whenever the transmit attenuator is at its maximum loss. At this time, the transmit output (TXO) is squelched until GSRST or RSTPK is toggled.
TXLVL	**STR.2**	Transmit level adjustment. 0 = no level adjustment made 1 = level adjustment made This bit latches to a 1 whenever the transmit peak detector has forced the transmit signal limiter to increase its loss by a step. A read of the Status register clears this bit.
DLDET	**STR.1**	Delta detect at VSENSE pin. 0 = no delta change detected 1 = delta change detected This bit latches to a 1 whenever the voltage at VSENSE changes by the a certain percentage (see "Delta Detector" section). A read of the Status register clears this bit unless the condition still exists.
RGDET	**STR.0**	Ring detect. 0 = no ringing detected 1 = ring burst detected This bit latches to a 1 when a valid ring signal has been received at $\overline{\text{RGSNS}}$ (also indicated by the $\overline{\text{RGDET}}$ pin going low). A read of the Status register clears this bit until the next valid ring burst.

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RECEIVE MONITOR GAIN (READ/WRITE)[1] Table 8

1	1	1	1	G3	G2	G1	G0
(MSB)							(LSB)

SYMBOL	POSITION	NAME AND DESCRIPTION
1	RMR.7	Unused.
1	RMR.6	Unused.
1	RMR.5	Unused.
1	RMR.4	Unused.
G3-G0	RMR.3-0	Receive monitor output gain. These bits select the amount of gain from the output of the internal hybrid to the RXMON output. The mapping of these bits is shown below.

1. Unused bits RMR.7-RMR.4 will read back as 1's; however, it is recommended that these bits always be written as 0's to maintain compatibility with future options.

RECEIVE MONITOR GAIN MAPPING Table 9

G3 - G0	GAIN/LOSS
0000	+ 9.0 dB
0001	+ 6.0
0010	+ 3.0
0011	0.0
0100	- 3.0
0101	- 6.0
0110	- 9.0
0111	- 12.0
1000	- 15.0
1001	- 18.0
1010	- 21.0
1011-1111	OFF [1]

1. The OFF selection means that the RXMON output is forced to low-impedance mid-supply. It is also recommended that the 1111 selection be used for turning RXMON off since selections 1010-1110 may be used for additional gain settings on future versions of the DS1360. All gains except OFF are ± 1dB.

TYPICAL APPLICATION Figure 8

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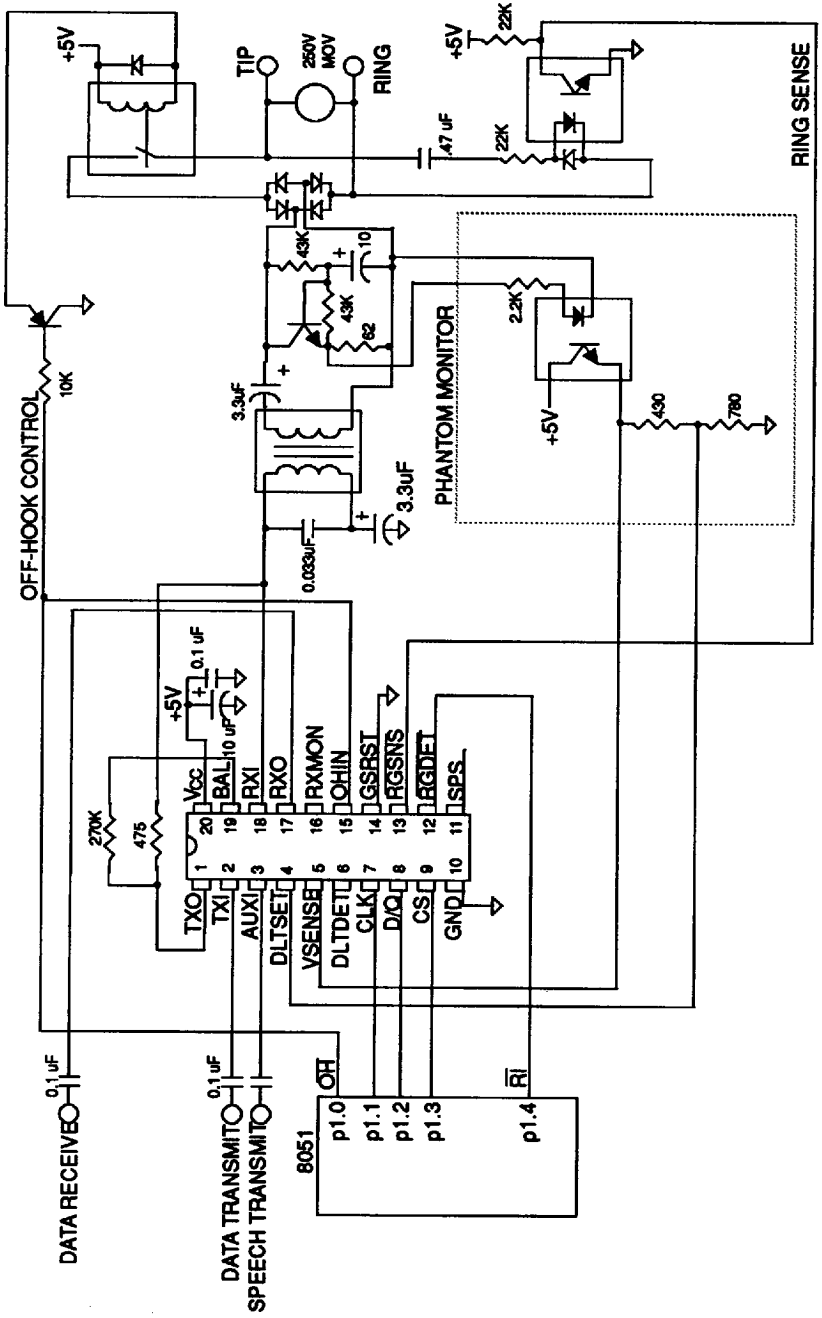


ABSOLUTE MAXIMUM RATINGS*

T-51-07-01

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0° C to +70° C)

PARAMETER	SYM	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		V_{cc}+0.3	V	
Logic 0	V_{IL}	-0.3		+0.8	V	
Supply	V_{CC}	4.5		5.5	V	3

CAPACITANCE (t_A= +25° C)

PARAMETER	SYM	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			10	pF	

DC ELECTRICAL CHARACTERISTICS (0° C to +70° C; V_{CC} = 5V ±10%)

PARAMETER	SYM	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current	I_{CCA}		5		mA	1
Power-Down Supply Current	I_{CCPD}		1	5	uA	2
Input Leakage	I_{ILK}	-1.0		+1.0	uA	
Output Leakage	I_{OLK}	-1.0		+1.0	uA	
Output Current (@2.4V)	I_{OH}	-1.0			mA	
Output Current (@0.4V)	I_{OL}	+4.0			mA	

NOTES:

1. Analog outputs unloaded.
2. PD bit = 1 (CTR.4).
3. Decouple with 10uF and 0.1uF capacitors.

TRANSMIT ANALOG CHARACTERISTICS (0° C to -70° C; V_{CC} = +5V ± 10%)

PARAMETER	MIN	TYP	MAX	UNITS	NOTES
Input AC Impedance (AUXI, TXI)		80		Kohms	1
Input Level Before TXO Squelched (GSRST=0)		±2.00		Vpk	2
Input Level Before Clipping (GSRST=1)		±2.25		Vpk	2
TXO Billing Delay	2.1	2.25		sec	3
TXO Output Level		0.475	0.540	Vrms	2
Transmit Attenuator Range (Before TXO squelched)	10			dB	2
TXO Harmonic Distortion			-55	dB	4
TXO Output Offset Voltage		±50		mV	
Output AC Impedance (TXO)		25		Ohms	1

NOTES:

1. Vtest = sine wave, 0.25 Vrms, @ 1 KHz.
2. Vtest = sine wave @ 1 KHz. Squelched refers to TXO being disabled.
3. Measured from falling edge of $\overline{\text{OHIN}}$. Ring must have been detected in previous 8 seconds.
4. TXO load = 600 ohms. TXI or AUXI = sine wave, 0.25 Vrms, 1 KHz.

RECEIVE ANALOG CHARACTERISTICS (0° C to 70° C; V_{CC} = +5V ±10%)

PARAMETER	MIN	TYP	MAX	UNITS	NOTES
Input AC Impedance (RXI)		110		Kohms	1
Input Level Before Clipping (RXI)		±2.0		Vpk	2
Output Offset Voltage (RXO, RXMON)		±50		mV	
Ring Detect Delay		100		mS	3

NOTES:

1. Vtest = sine wave, 0.707 Vrms, @ 1 KHz.
2. Clipping observed at RXO.
3. $\overline{\text{RGSNS}}$ = 20 Hz square wave.

A/D CONVERTER CHARACTERISTICS (0° C to 70° C; V_{CC} = +5V ±10%)

PARAMETER	MIN	TYP	MAX	UNITS	NOTES
Input AC Impedance (DLTSET, VSENSE)		500		Kohms	
Input Voltage Range (DLTSET, VSENSE)	0.0		Vcc	V	
Total Conversion Error		±.5	±1	LSB	
Conversion Time		80		usec	

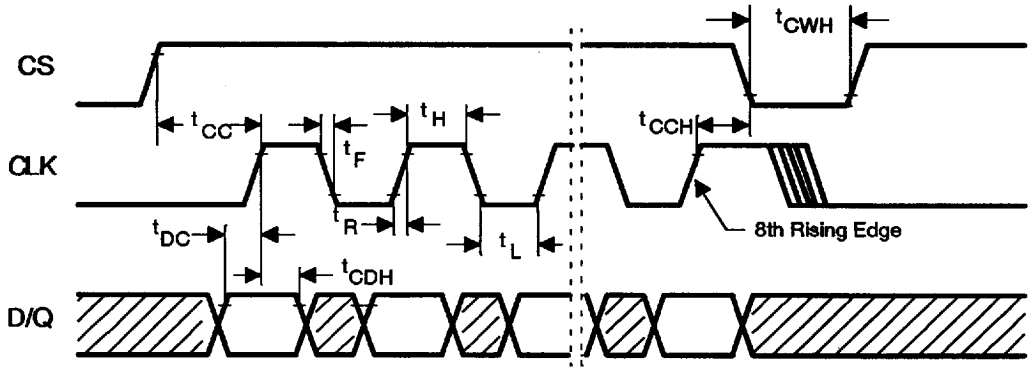
SERIAL PORT TIMING CHARACTERISTICS (0° C to +70° C; V_{CC} = 5V ± 10%)

PARAMETER	SYM	MIN	TYP	MAX	UNITS	NOTES
D/Q to CLK Setup	t_{DC}	35			ns	1
CLK to D/Q Hold	t_{CDH}	40			ns	1
CLK Low Time	t_{CL}	125			ns	1
CLK High Time	t_{CH}	125			ns	1
CLK Rise and Fall Times	t_R, t_F			100	ns	1
CS to CLK Setup	t_{CC}	250			ns	1
CLK to CS Hold	t_{CCH}	40			ns	1
CS Inactive Time	t_{CWH}	250			ns	1
CLK to D/Q Delay	t_{CDD}			75	ns	1
CS to D/Q High Z	t_{CDZ}					

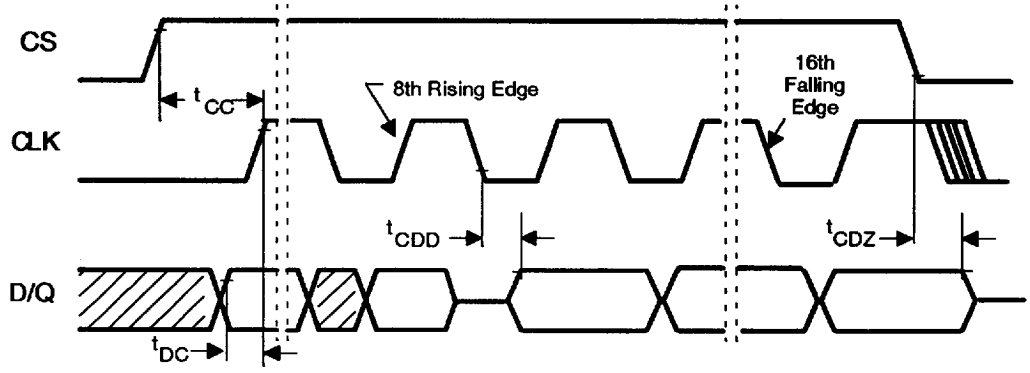
NOTES:

1. Measured at V_{IH} = 2.0V, V_{IL} = 0.8V, and 10ns maximum rise and fall times.

SERIAL PORT TIMING – WRITE REGISTER OPERATION Figure 9

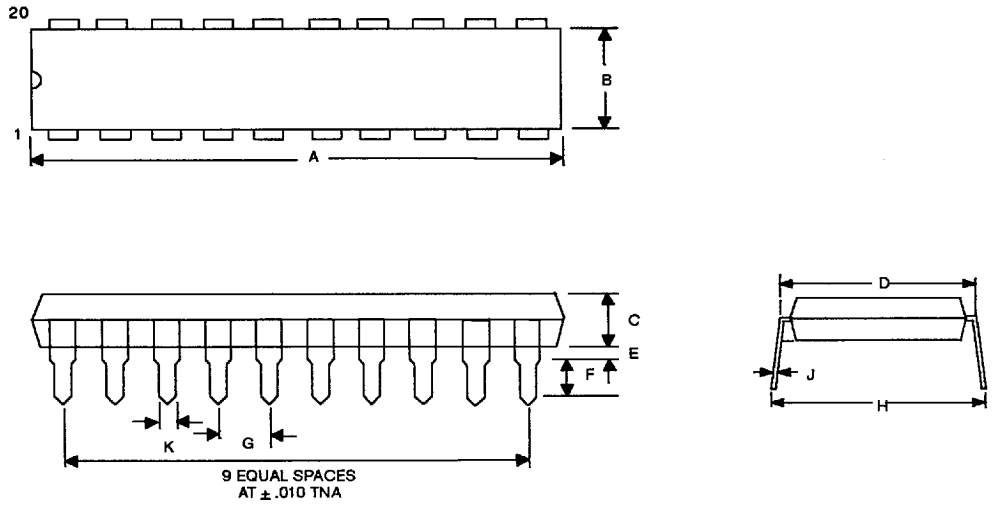


SERIAL PORT TIMING – READ REGISTER OPERATION Figure 10



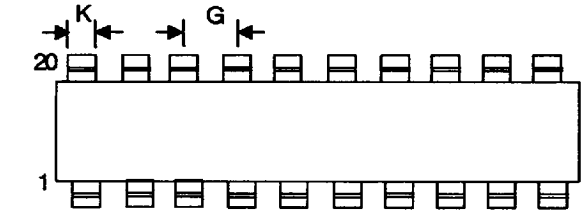
DS1360 PHANTOM DAA CHIP
20-PIN DIP

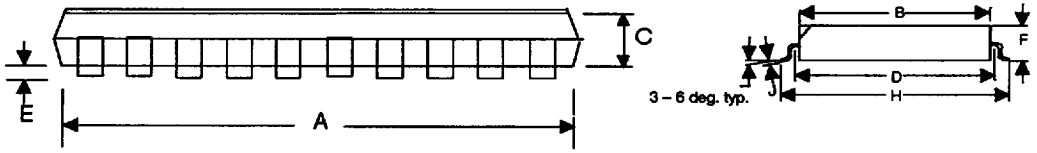
T-51-07-01



DIM	INCHES	
	MIN	MAX
A	0.960	1.040
B	0.240	0.260
C	0.120	0.140
D	0.290	0.310
E	0.015	0.040
F	0.110	0.130
G	0.090	0.110
H	0.320	0.370
J	0.008	0.012
K	0.015	0.021

DS1360S PHANTOM DAA CHIP
20-PIN SOIC





DIM	INCHES	
	MIN	MAX
A	0.500	0.511
B	0.290	0.300
C	0.089	0.095
D	0.325	0.330
E	0.008	0.012
F	0.097	0.105
G	0.046	0.054
H	0.400	0.410
J	0.006	0.011
K	0.013	0.019